

DIGITAL SYSTEMS LABORATORY WORK

MODUL 9 : DECODER



By :

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INFORMATION TECHNOLOGY

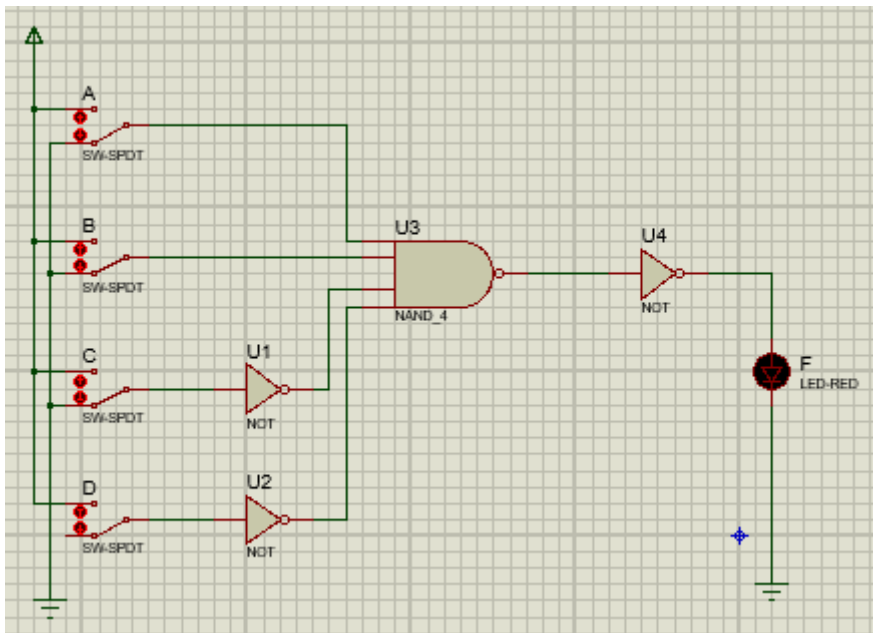
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 Date of Practicum : Friday, May 17 st 2019

### Trial 1. Make a simple decoder circuit

1. Make a decoder as shown in the following picture!



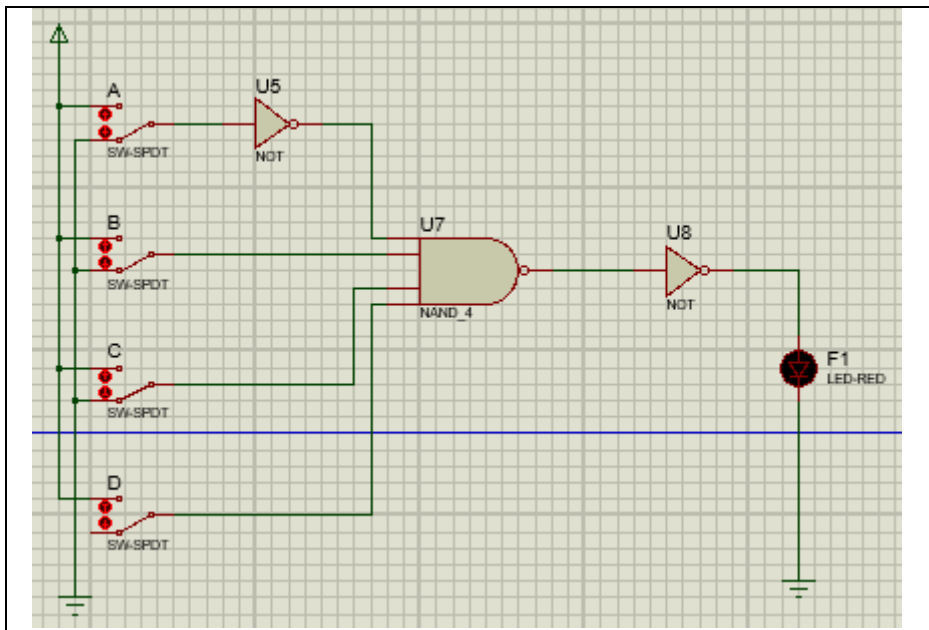
2. Fill in the blank column in the table!

A	B	C	D	F
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

3. Decoder (F) only work (ON) when : A = 1, B = 1, C = 0 dan D = 0.

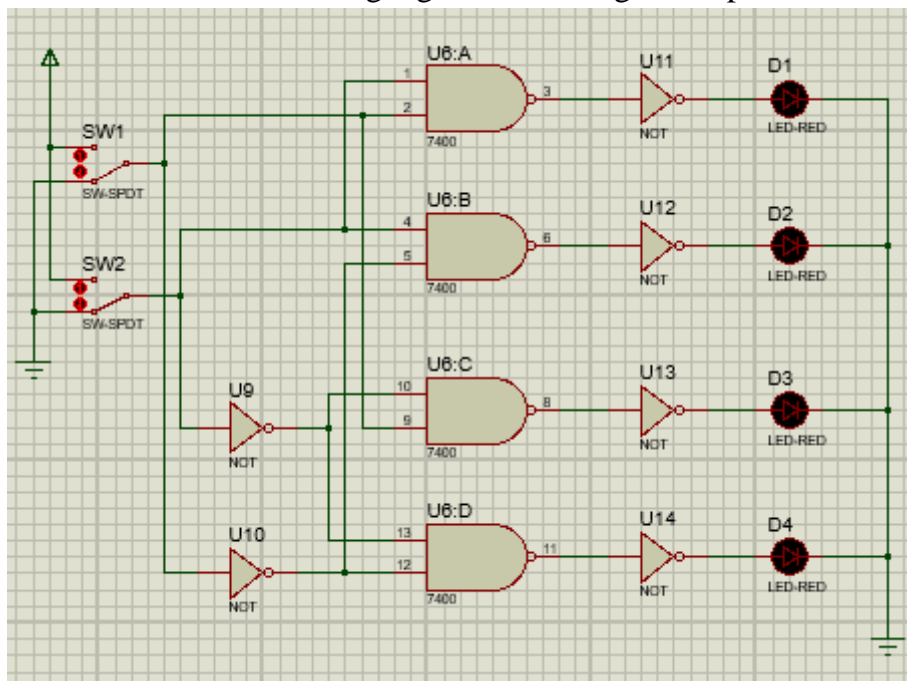
4. Based on the series and table above, try making a decoder that has the output as the following decoder function :

$$F = 1, \text{ if the condition } A = 0, B = 1, C = 1, D = . \quad (F=A'BCD)$$



## Trial 2.

1. Make a combination of logic gates following in the picture!



2. Fill in the blank column in the table!

INPUT		OUTPUT			
SW1	SW2	D1	D2	D3	D4
0	0	0	0	0	1
0	1	0	1	0	0

<b>1</b>	<b>0</b>	0	0	1	0
<b>1</b>	<b>1</b>	1	0	0	0

3. Every dioda (LED) show the ouput result by combination circuit :

$$D1 = SW_1 \cdot SW_2$$

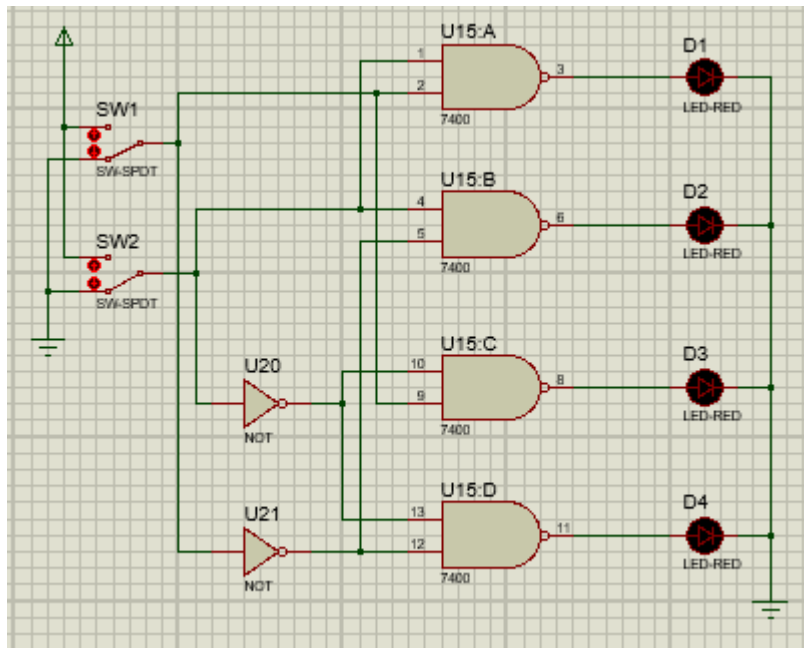
$$D2 = \overline{SW_1} \cdot SW_2$$

$$D3 = SW_1 \cdot \overline{SW_2}$$

$$D4 = \overline{SW_1} \cdot \overline{SW_2}$$

### Trial 3.

1. Make a combination of logic gates following in the picture!



2. Fill in the blank column in the table!

INPUT		OUTPUT			
SW1	SW2	D1	D2	D3	D4
<b>0</b>	<b>0</b>	1	1	1	0
<b>0</b>	<b>1</b>	1	0	1	1
<b>1</b>	<b>0</b>	1	1	0	1
<b>1</b>	<b>1</b>	0	1	1	1

3. Every dioda (LED) show the ouput result by combination circuit :

$$D1 = SW_1 \cdot SW_2$$

$$D2 = \overline{SW_1} \cdot SW_2$$

$$D3 = SW_1 \cdot \overline{SW_2}$$

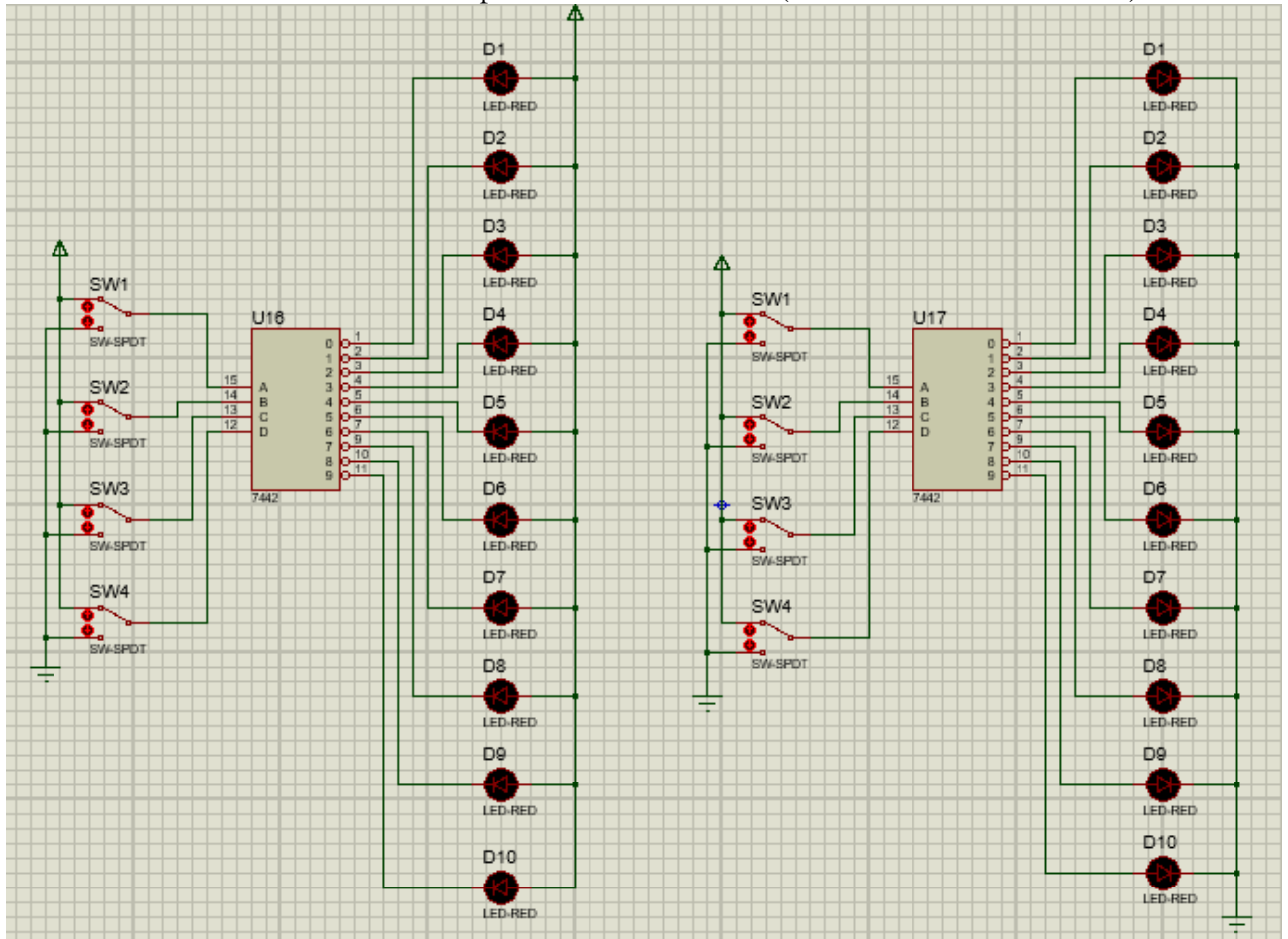
$$D4 = \overline{SW_1} \cdot \overline{SW_2}$$

4. Compare the result of truth tabel on the trial 2 and trial 3! Make a conclusion fom the trial 2 and trial 3.

With the NOT then it will influence the result of the LED output, so that the result of the LED output are there will inversely proportional with output which hasn't LED.

### **Trial 4.IC 7442 Decoder BCD-to-decimal**

1. Make the circuit as look n the picture! Use IC 7442 (BCD to decimal decoder)



### Decoder 7442 : Common anode LED circuit

### Common Cathode LED circuit

2. Fill in the blank column in the 7442 decoder truth table below!

- a. Common anode LED circuit

[illegible]

1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

b. Common cathode LED circuit

Input				Output									
SW4	SW3	SW2	SW1	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

## ASSIGNMENT

1. Look for datasheet from ic 7442! Look for schematic whic show logic gates compiler IC 7442!

Answer :

- **All Outputs Are High for Invalid Input Conditions**
- **Also for Application as**  
4-Line-to-16-Line Decoders  
3-Line-to-8-Line Decoders
- **Diode-Clamped Inputs**

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A	140 mW	17 ns
'LS42	35 mW	17 ns

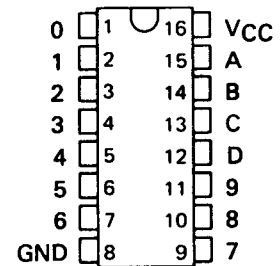
### description

These monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

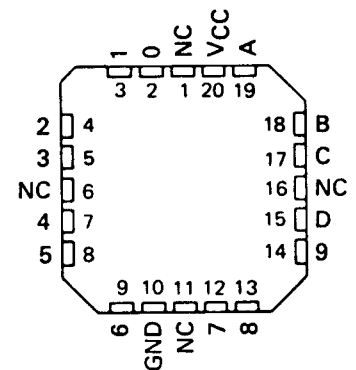
The '42A and 'LS42 feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

The SN5442A and SN54LS42 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7442A and SN74LS42 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5442A, SN54LS42 . . . J OR W PACKAGE  
SN7442A . . . N PACKAGE  
SN74LS42 . . . D OR N PACKAGE  
(TOP VIEW)

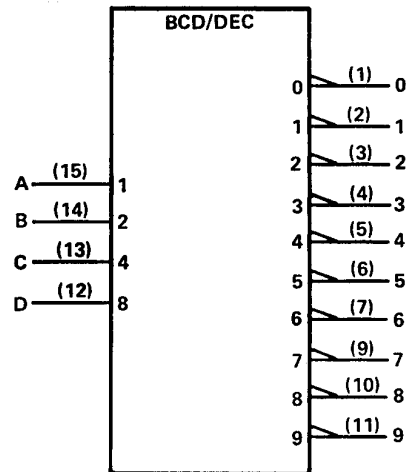


SN54LS42 . . . FK PACKAGE  
(TOP VIEW)



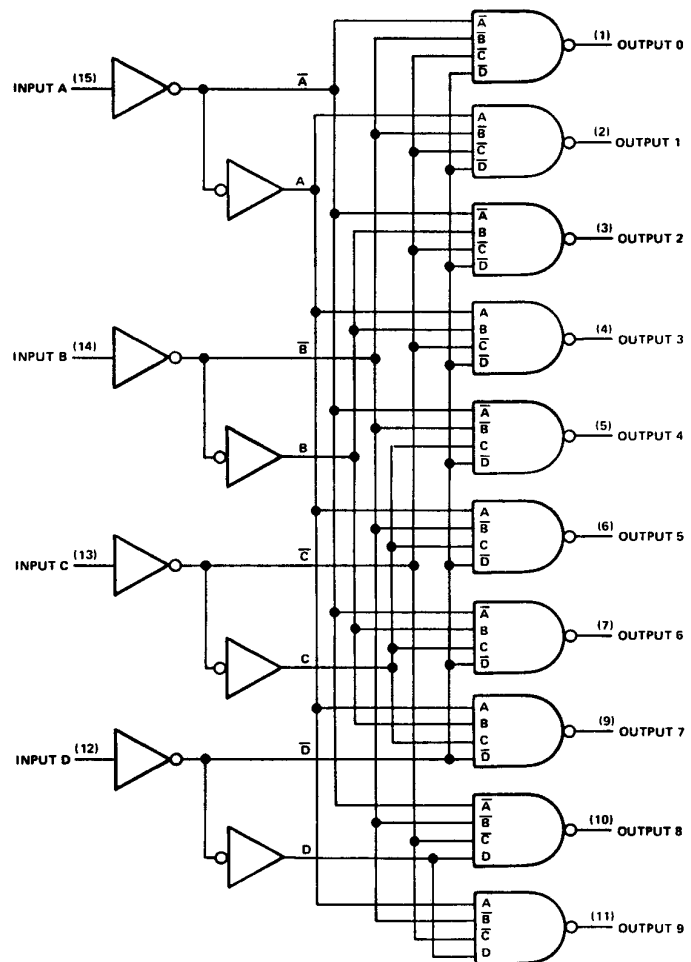
NC - No internal connection

logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

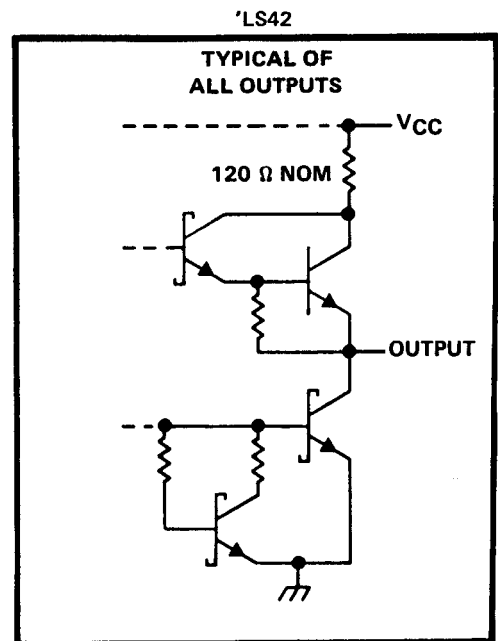
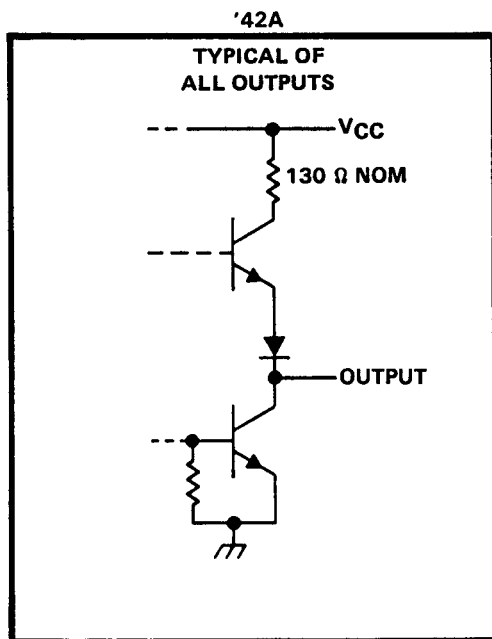
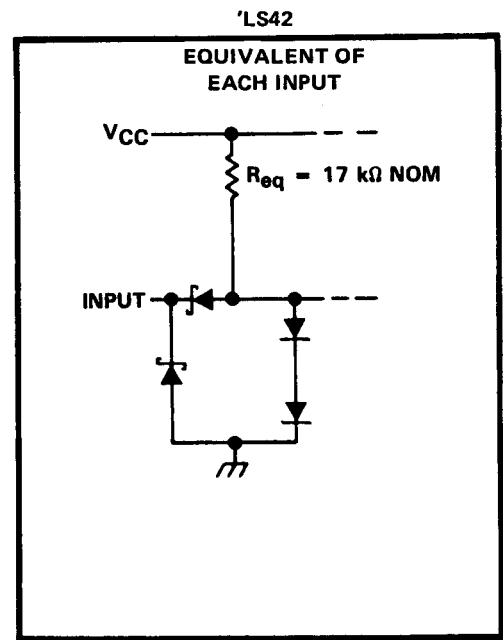
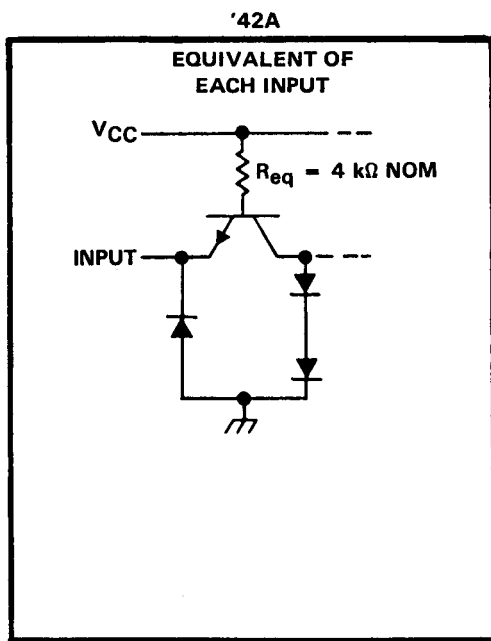
logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.



# schematics of inputs and outputs



## FUNCTION TABLE

[illegible]

H = high level, L = low level

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
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Input voltage: '42A ..... 5.5 V

'LS42..... 7 V

Operating free-air temperature range: SN5442A, SN54LS42 . . . . . -55°C to 125°C

SN7442A, SN74LS42 . . . . . 0°C to 70°C

**Storage temperature range** . . . . . **-65°C to 150°C**

**NOTE 1:** Voltage values are with respect to network ground terminal.

**NOTE 1: Voltage values are with respect to network ground terminal.**