Digital systems
Practicum 7

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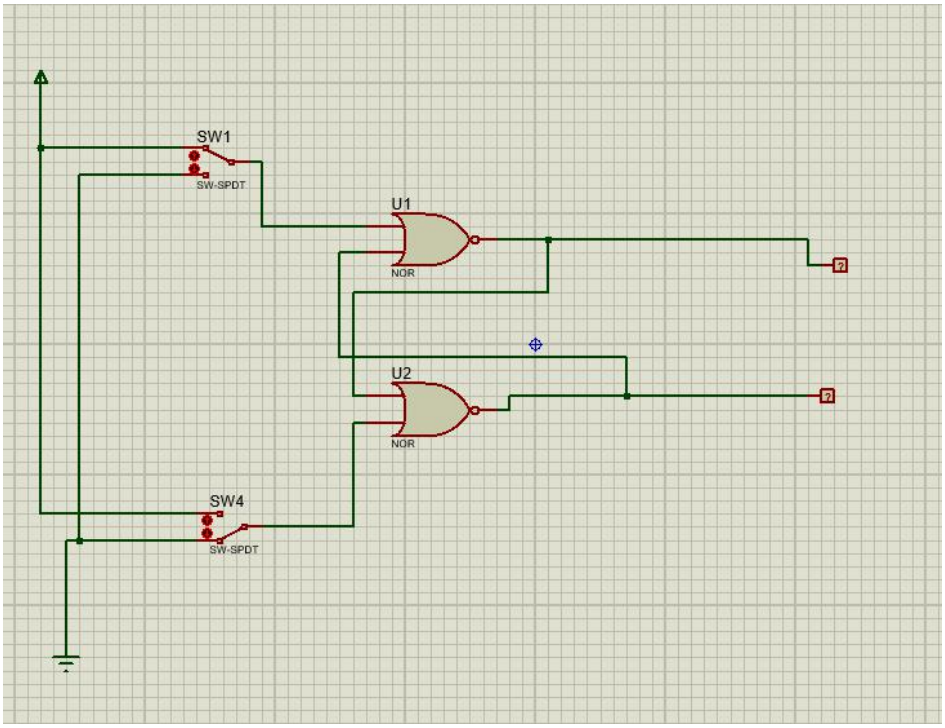
Experiment 1



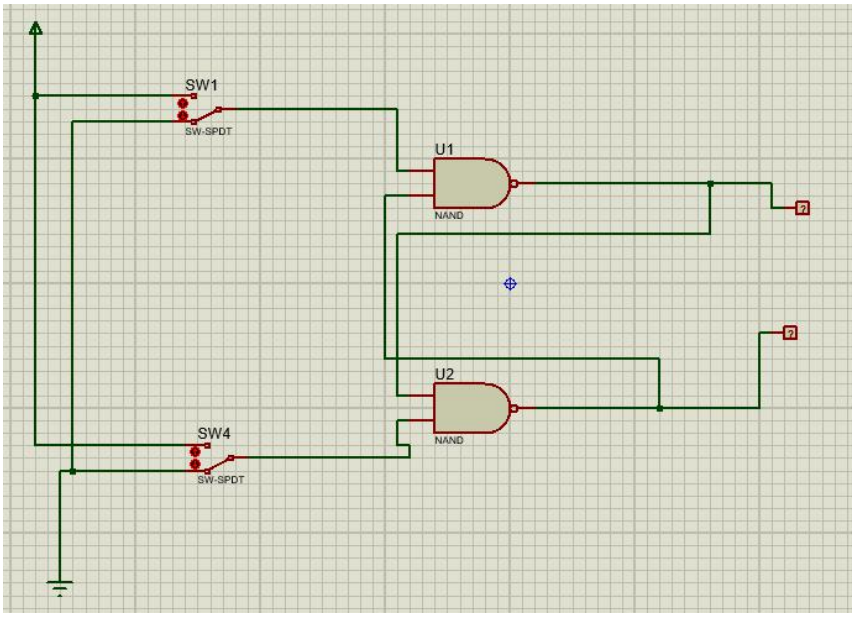
1.1 NOR Latch

1. Table based on simulation

	S (set)	R (reset)	qutput	
			Q	Q’
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

2. What will happen if we are given the condition S = R = 0?
   Answer: the output result are the same as the previous conditions.
3. Why is the condition S = R = 1 not allowes?
   Answer: because it can break the logic eqyation Q = not Q’.

Experiment 2



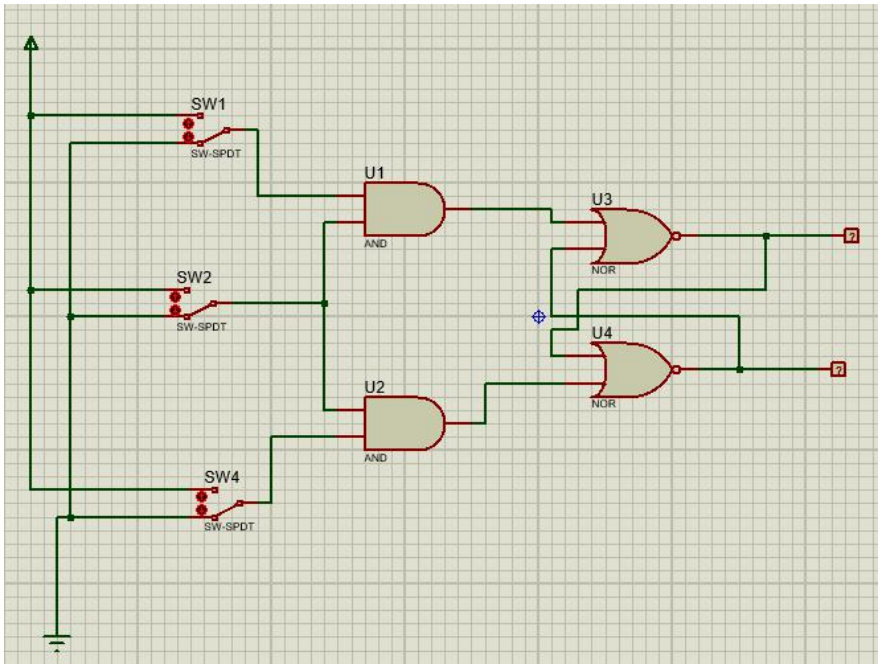
2.1 NAND Latch

1. Table based on simulation

	S (set)	R(reset)	qutput	
			Q	Q’
1	0	1	1	0
2	1	1	1	0
3	1	0	0	1
4	1	1	0	1
5	0	0	1	1

2. What will happen if we give the condition S = R = 1?
   Answer: the output reseult are the same as the previous conditions
3. Why is the condition S=R=0 not allowed?
   Answer: because it can break the logic equation Q = not Q’
4. Based on the flip-flop analysis above, what do you tthink of the statement
   “ flip flop and latch are used as data storage elements?”
   Answer: like data storage that can be used to store memory, such as circuits desc in sequential logic. When using read-only memory,the outpun and the next state depent not only on initial input, but also on the current state.

Experiment 3

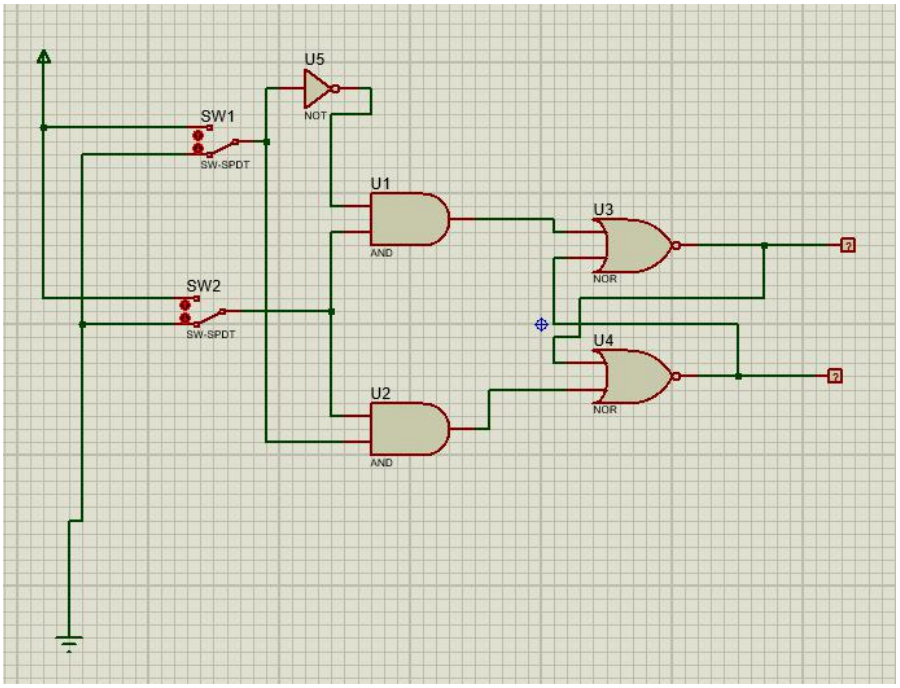


1. Table based on simulation

	S (set)	R (reset)	clock	qutput	
				Q	Q(t+1)
1	0	0	0	-	-
2	0	0	1	-	-
3	0	1	0	-	-
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

2. What will happen if we give the condition S=R=1 and the clock changes from 1 to 0?
   Answer: logic race condition detected during transsient analysis.
3. How can the above conditions occur?
   Answer : the output of the flip flop wont change as long as the clock pilse is 0.
4. Explain how RS flip flop work!
   Answer: SR or RS type flip flop is a type of flip flop has asynchronous input S (set) or R (Reset) or both, with output Q and Q'. input S and R can be symchronized by adding a clock input to the sirsuit. Q output cant respons to S and R inputs before input clock.

Experiment 4.



Flip flop

1. Table based on simulation

	D	clock	output	
			Q	Q(t+1)
1	0	0	0	0
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

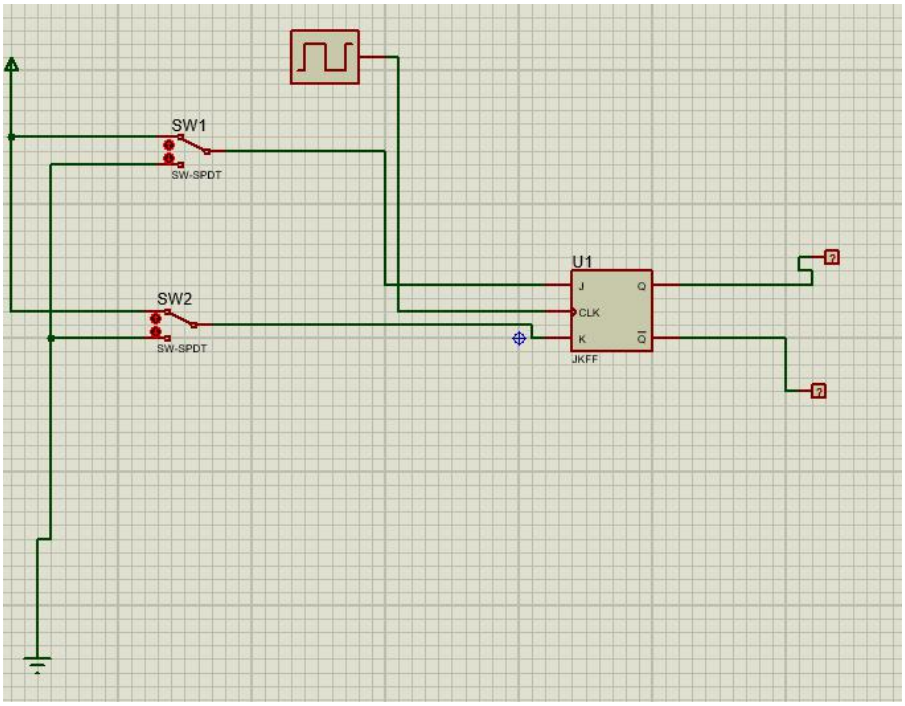
2. Explain how D flip flops work!

Answer: D flip flop has only one data input and one data clock. D is referred to as a flip flop delay or delay. Delay explains what happens to stored data, or at input D. data (0 or 1) is delayed by 1 pulsaclock from input to output Q. there are many ways to design this D flip flop circuit. Basically, D flip flop is a multivibator with a dual state (bistable)whose input D is transferred to the output after receiving a clock pulse.

3. What is functiun od the NOT gate on the flip flop D compared to the RS flip flop?

Answer: for the data input flow, SET gets input directly from the not get which is connected directly to input data then passes through the NAND gate and yhen produces the output.

Experiment 5



1. Table based of simulation

	J	K	Clock	output	
				Q	Q(t+1)
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	1

2. What will happen if J = K =0 and close rise up (change from 0 to 1)?
   Answer: output Q remains the last value or state
3. What will happen if j = k = 1 and close rise up?
   Answer: then u can adjust the flip flot or the reset
4. Explane how flip flop JK work!
   Answer: J and K are called control inputs to determine what the flip flop will do when receiving an increased clock pulse. RC circuits have short time consistants so that why convert clock pulse ibto narrow impulses.