

Digital systems

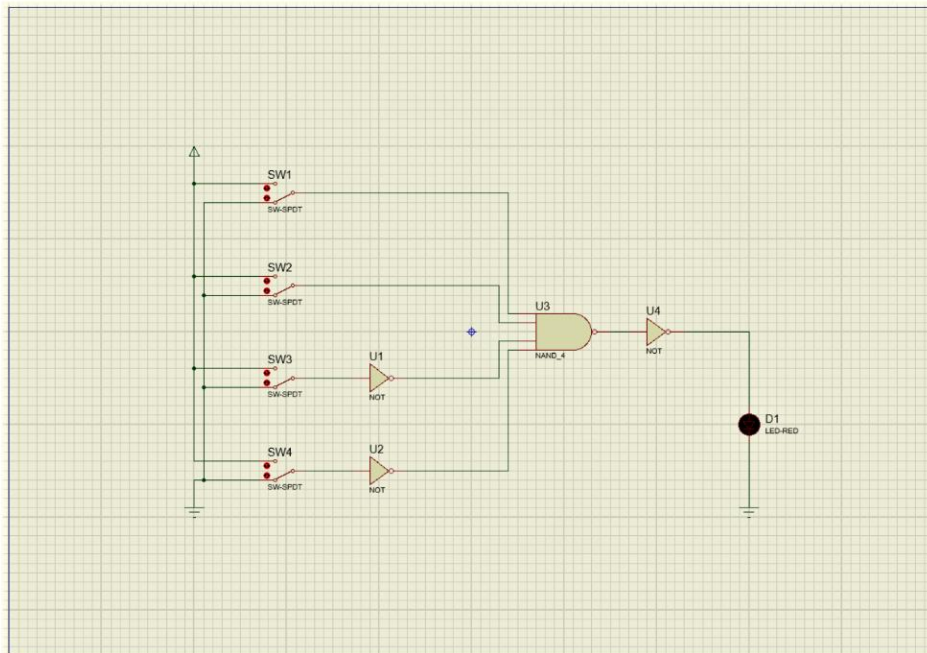
Practicum 9



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Experiment 1

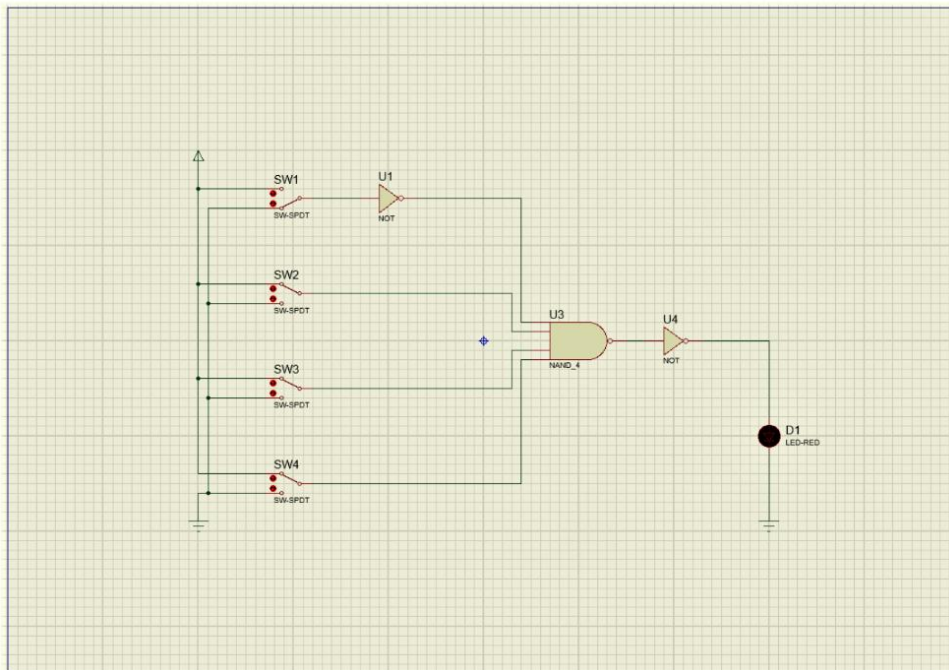


1. Column table

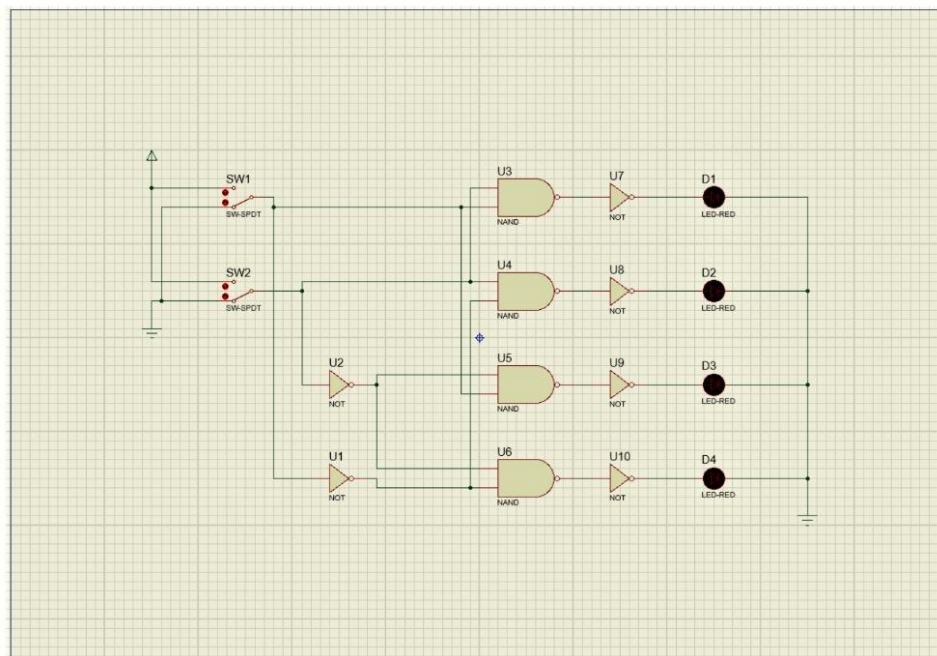
A	B	C	D	F
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

2. Decoder (F) only works (ON) when: A = 1, B = 1, C = 0, and D = 0.

3. Set of decoder that has output as a function: $F = 1$, if condition $A = 0, B = 1, C = 1, D = 1$. ($F = A'BCD$)



Experiment 2



1. Column table

Input		Output LED			
SW1	SW2	D1	D2	D3	D4
0	0	0	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	1	0	0	0

2. Output result from the logic gate combination

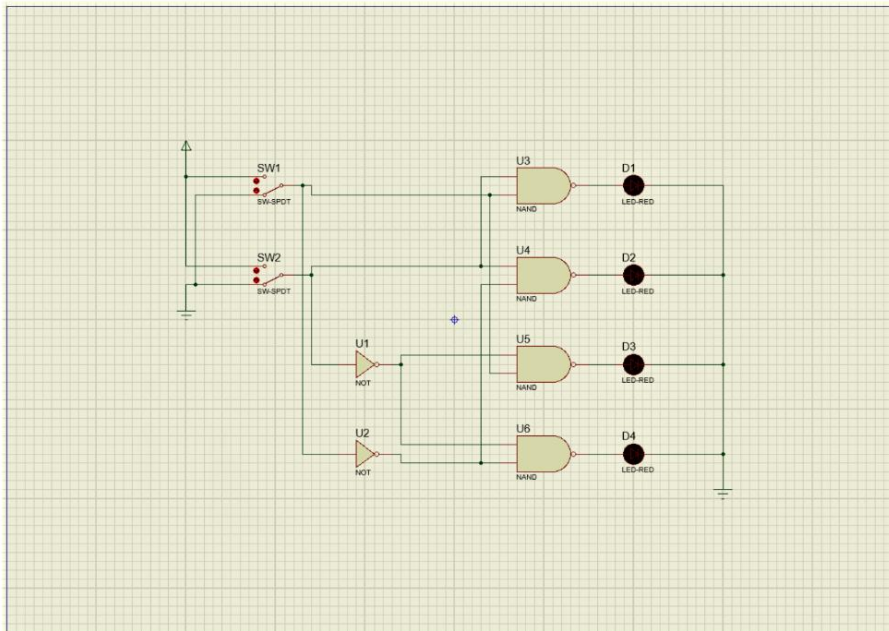
a. $D1 = SW1 \cdot SW2$

b. $D2 = \overline{SW1} \cdot SW2$

c. $D3 = SW1 \cdot \overline{SW2}$

d. $D4 = \overline{SW1} \cdot \overline{SW2}$

Experiment 3



1. Column table

Input		Output LED			
SW1	SW2	D1	D2	D3	D4
0	0	1	1	1	0
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	1	1	1

2. Output result from the logic gate combination

a. $D1 = SW1 \cdot SW2$

b. $D2 = \overline{SW1} \cdot SW2$

c. $D3 = SW1 \cdot \overline{SW2}$

d. $D4 = \overline{SW1} \cdot \overline{SW2}$

3. Conclusion from experiment 2 and 3

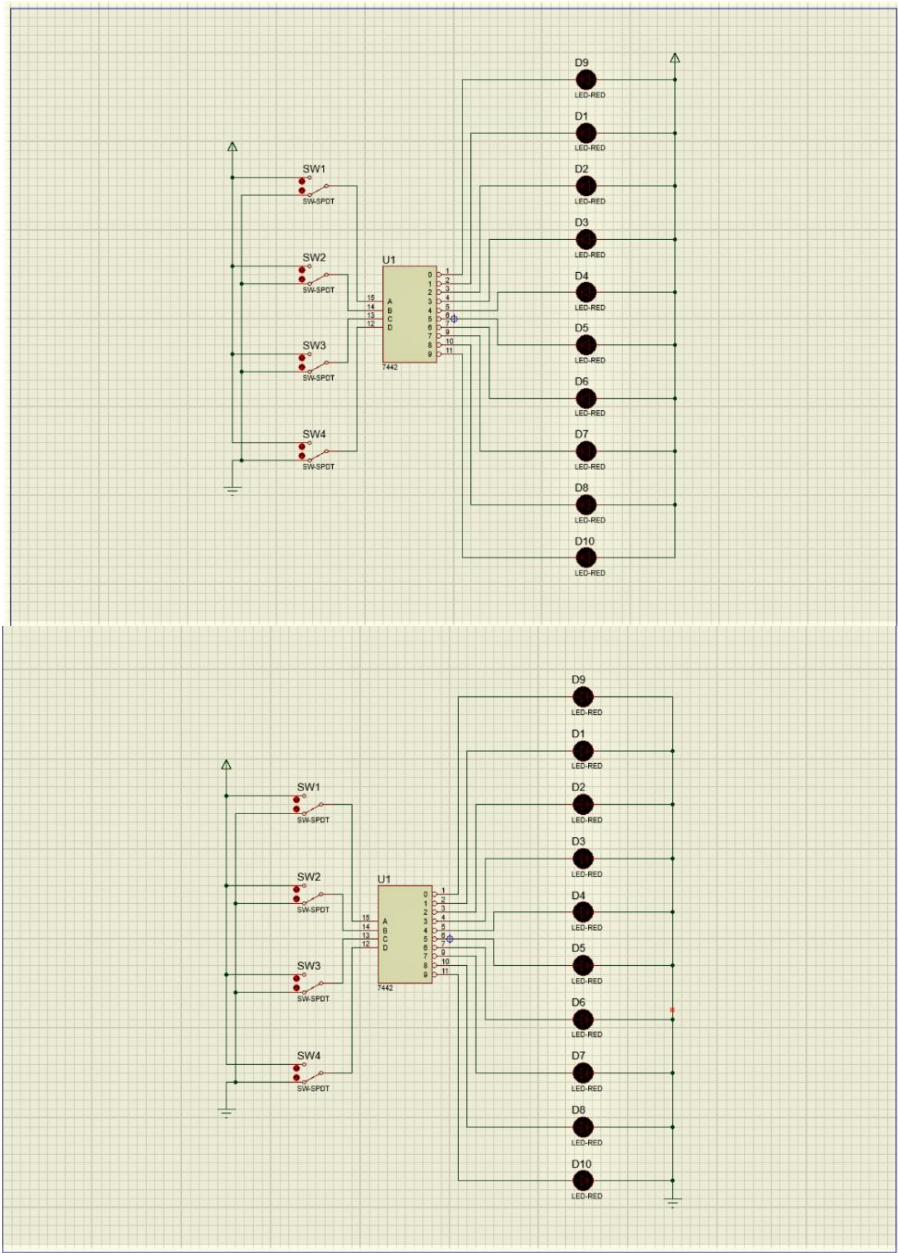
in the second experiment there is a NOT gate located after the

NAND gate, while in the third experiment there is no NOT gate

located after the NAND gate. so the output results in experiments 2

and 3 are very different

Experiment 4



1. Column table

a. Common anode LED

[illegible]

b. Common cathode LED

[illegible]