PRACTICUM DIGITAL SYSTEM MODUL 10 DIGITAL SYSTEM

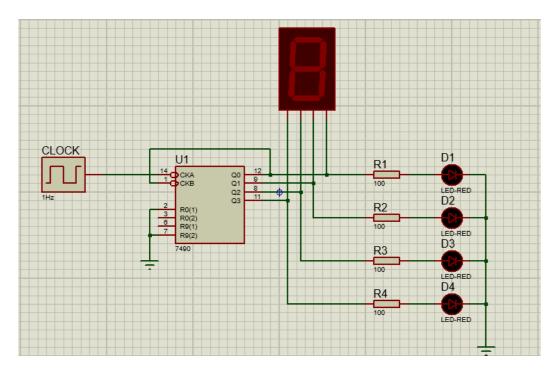


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Experiment 1

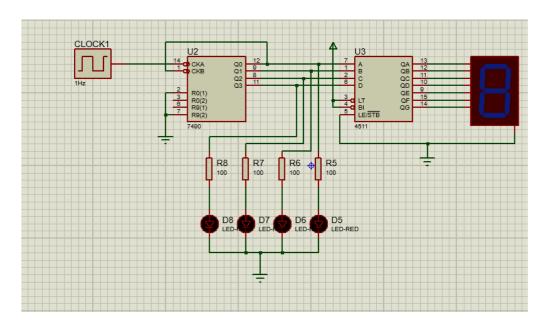
a) Circuit Board



b) Coloumn Table

Input		Output			
Clock	D1	D2	D3	D4	Seven Segment
1	0	0	0	0	0
2	1	0	0	0	-
3	0	1	0	0	2
4	1	1	0	0	3
5	0	0	1	0	4
6	1	0	1	0	S
7	0	1	1	0	6
8	0	1	1	0	٦-
9	0	0	0	1	8
10	1	0	0	1	9
11	0	0	0	0	0
12	1	0	0	0	
13	0	1	0	0	5

Experiment 2



a. Column Table

Input		Output			
Input Clock			D4	Seven	
CIOCK	DΙ	D2	DS	D4	Segment
1	0	0	0	0	0
2	1	0	0	0	1
3	0	1	0	0	2
4	1	1	0	0	3
5	0	0	1	0	4
6	1	0	1	0	5
7	0	1	1	0	Ь
8	0	1	1	0	٦
9	0	0	0	1	8
10	1	0	0	1	9
11	0	0	0	0	0

- b. Compare the experiment 1 with Experiment 2! Could you spot the similarity and the difference?
 - ⇒ The Experiment 1 in the number 6 and the Experiment 2 is different which means that Experiment 1 the output 7 seg is 5 and experiment 2 the result is b.
- c. Is that true which 7 seg-BCD same with BCD to 7 Segment decoder?
 - ⇒ No!1!1!

August 1986 Revised July 2001

DM7490A Decade and Binary Counter

General Description

The DM7490A monolithic counter contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated setto-nine inputs for use in BCD nine's complement applications

To use the maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table. A symmetrical divide-by-ten count can be obtained from the counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

Features

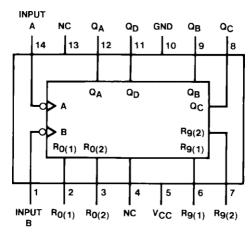
Typical power dissipation 145 mW

Count frequency 42 MHz

Ordering Code:

Order Number	Package Number	Package Description
DM7490AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Tables

BCD Count Sequence (Note 1)

	Outputs									
Count	QD	Qc	QB	QA						
0	L	L	L	L						
1	L	L	L	Н						
2	L	L	Н	L						
3	L	L	Н	Н						
4	L	Н	L	L						
5	L	Н	L	Н						
6	L	Н	Н	L						
7	L	Н	Н	Н						
8	Н	L	L	L						
9	Н	L	L	Н						

BCD Bi-Quinary (5-2) (Note 2)

	Outputs									
Count	QA	QD	Qc	QB						
0	L	L	L	L						
1	L	L	L	Н						
2	L	L	Н	L						
3	L	L	Н	Н						
4	L	Н	L	L						
5	Н	L	L	L						
6	Н	L	L	Н						
7	Н	L	Н	L						
8	Н	L	Н	Н						
9	Н	Н	L	L						

Reset/Count Function Table

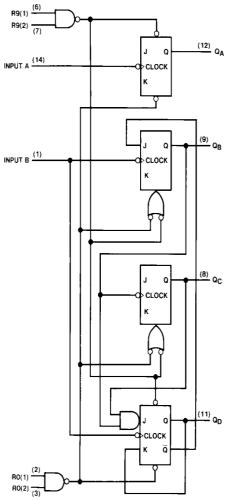
	Reset I		Out	puts					
R0(1)	R0(2)	R9(1)	R9(2)	Q_{D}	Q _D Q _C Q _B				
Н	Н	L	X	L	L	L	L		
Н	H	X	L	L	L	L	L		
X	X	Н	Н	Н	L	L	Н		
X	L	X	L		COUNT				
L	X	L	X	COUNT					
L	X	X	L	COUNT					
X	L	L	X		COU	JNT			

H = HIGH Level L = LOW Level X = Don't Care

Note 1: Output QA is connected to input B for BCD count.

Note 2: Output QD is connected to input A for bi-quinary count

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a HIGH level.

Absolute Maximum Ratings(Note 3) Supply

Voltage

5.5V Input Voltage

7V Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

0°C to +70°C Operating Free Air Temperature Range -65°C to +150°C Storage Temperature Range

Recommended Operating Conditions

Symbol	Parame	ter	Min	Nom	Max	Units
V _{CC}	Supply Voltage		4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage		2			V
$V_{\rm IL}$	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Currer	nt			-0.8	mA
I _{OL}	LOW Level Output Curren	t			16	mA
f_{CLK}	Clock Frequency	A	0		32	
	(Note 4)	В	0		16	MHz
tw	Pulse Width (Note	A	15			
	4)	В	30			ns
		Reset	15			
t _{REL}	Reset Release Time (Note 4)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 4: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

DC Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units	
V _I	Input Clamp Voltage	$V_{CC} = Min, I_I = -12 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4	3.4		V	
V _{OL}	LOW Level Output Voltage	$V_{CC} = Min$, $I_{OL} = Max$ $V_{IH} = Min$, $V_{IL} = Max$ (Note 6)		0.2	0.4	V	
II	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$				1	mA
I _{IH}	HIGH Level Input Current	$V_{CC} = Max$ $V_{I} = 2.7V$	A			80	
			Reset B			40 120	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = Max$ $V_{I} = 0.4V$	A			-3.2	
	input Current	V1= 0.4 V	Reset			-1.6	mA
			В			-4.8	
I_{OS}	Short Circuit Output Current	V _{CC} = Max (Note 7)		-18		-57	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 8)		_	29	42	mA

Note 5: All typicals are at $V_{CC} = 5V$, $T_A = 25$ °C.

Note 6: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 7: Not more than one output should be shorted at a time.

 $\textbf{Note 8:} \ I_{CC} \ is \ measured \ with \ all \ outputs \ open, \ both \ RO \ inputs \ grounded \ following \ momentary \ connection \ to \ 4.5V, \ and \ all \ other \ inputs \ grounded.$

AC Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25$ °C

		From (Input)	$\mathbf{R_L} = 400\Omega$	$R_L = 400\Omega$, $C_L = 15 pF$			
Symbol	Parameter	To (Output)	Min	Max	Units		
f _{MAX}	Maximum Clock	A to Q _A	32		MHz		
	Frequency	B to Q _B	16		MHZ		
t _{PLH}	Propagation Delay Time						
	LOW-to-HIGH Level Output	A to Q _A		16	ns		
t _{PHL}	Propagation Delay Time						
THL		A to Q _A		18	ns		
	HIGH-to-LOW Level Output						
t _{PLH}	Propagation Delay Time	A to Q _D		48	ns		
	LOW-to-HIGH Level Output						
t_{PHL}	Propagation Delay Time	A to Q _D		50	ns		
	HIGH-to-LOW Level Output						
t _{PLH}	Propagation Delay Time	B () O		16			
	LOW-to-HIGH Level Output	B to Q _B		16	ns		
t _{PHL}	Propagation Delay Time						
		B to Q _B		21	ns		
	HIGH-to-LOW Level Output						
t _{PLH}	Propagation Delay Time	B to Q _C		32	ns		
	LOW-to-HIGH Level Output						
t _{PHL}	Propagation Delay Time	B to Q _C		35	ns		
	HIGH-to-LOW Level Output						
t _{PLH}	Propagation Delay Time	B to Q _D		32	ns		
	LOW-to-HIGH Level Output	D to QD		32	lis		
t _{PHL}	Propagation Delay Time						
		B to Q _D		35	ns		
t	HIGH-to-LOW Level Output						
t _{PLH}	Propagation Delay Time	SET-9 to Q _A , Q _D		30	ns		
	LOW-to-HIGH Level Output						
PHL	Propagation Delay Time	SET-9 to Q _B , Q _C		40	ns		
	HIGH-to-LOW Level Output						
PHL	Propagation Delay Time	SET-0		40	ns		
	HIGH-to-LOW Level Output	Any Q		40	IIS		

$\begin{picture}(200,0)\put(0,0){P hysical Dimensions}\end{picture} in ches (millimeters) unless otherwise noted$ $\frac{0.740 - 0.770}{(18.80 - 19.56)}$ (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA $\frac{0.250\pm0.010}{(6.350\pm0.254)}$ PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX DEPTH OPTION 1 OPTION 02 0.135 ± 0.005 $\frac{0.300 - 0.320}{(7.620 - 8.128)}$ 3.060 (1.524) TYP 0.145 - 0.200(1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 $\frac{0.125 - 0.150}{(3.175 - 3.810)}$ 0.280 (7.112)-MIN $\frac{0.014-0.023}{(0.356-0.584)}\,\mathrm{TYP}$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

 $\frac{0.050\pm0.010}{(1.270-0.254)} \text{ TYP}$

0.100 ± 0.010 (2.540 ± 0.254)

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 $0.325 ^{\,+\,0.040}_{\,-\,0.015}$

N14A (REV F)

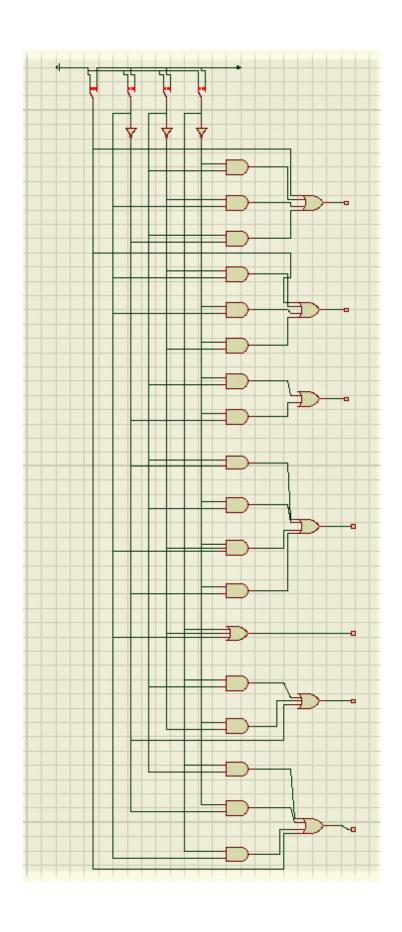
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Experiment 3

1. Table function of IC 4511

	Input					Output							D
Decimal Digit	LT	D	С	В	A	a	b	c	d	e	f	g	Display Output
0	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	L	0
1	Н	L	L	L	Н	L	Н	Н	L	L	L	L	1
2	Н	L	L	Н	L	Н	Н	L	Н	Н	L	Н	2
3	Н	L	L	Н	Н	Н	Н	Н	Н	L	L	Н	3
4	Н	L	Н	L	L	L	Н	Н	L	L	Н	Н	4
5	Н	L	Н	L	Н	Н	L	Н	Н	L	Н	Н	5
6	Н	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	6
7	Н	L	Н	Н	Н	Н	Н	Н	L	L	L	L	7
8	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	8
9	Н	Н	L	L	Н	Н	Н	Н	L	L	Н	Н	9
LT	L	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	8

- 2. The output "a" (highlight) in the table shows that LED works in seven common cathode segments
- 3. Each output shows the state of LED from seven segment various conditions
- 4. Each LED is controlled by a combination of logic gates.



5. Comparison truth table with set of BCD-to-7segment

The output results in the BCD-to-7-segment decoder circuit produce a value that exactly matches the truth table