PRACTICUM DIGITAL SYSTEM

MODUL 9

DIGITAL SYSTEM

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INFORMATION TECHNOLOGY

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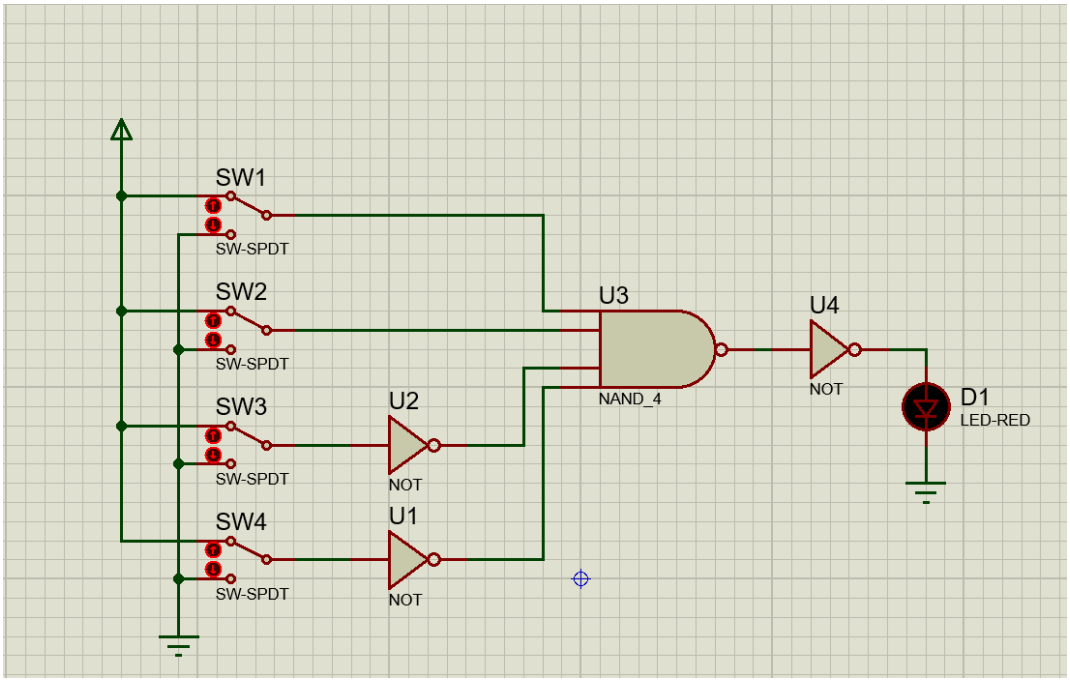
Experiment 1

a) Make a simple decoder



b) Truth table

A	B	C	D	F
0	0	0	0	**0**
1	0	0	0	**0**
0	1	0	0	**0**
1	1	0	0	**1**

0	0	1	0	**0**
1	0	1	0	**0**
0	1	1	0	**0**
1	1	1	0	**0**
0	0	0	1	**0**
1	0	0	1	**0**
0	1	0	1	**0**
1	1	0	1	**0**
0	0	1	1	**0**
1	0	1	1	**0**
0	1	1	1	**0**
1	1	1	1	**0**

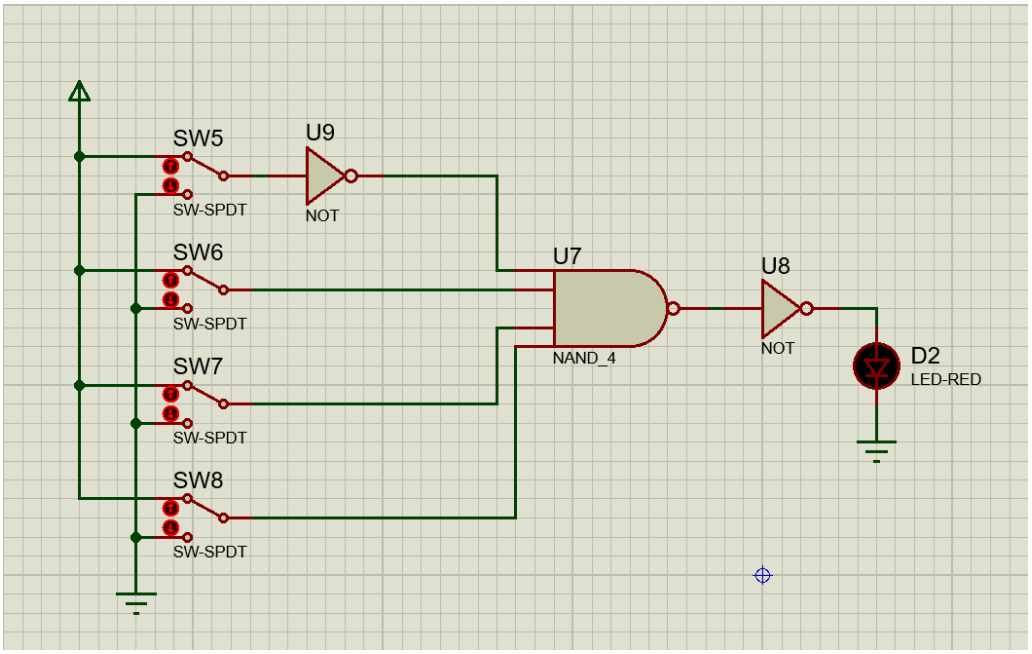
c) Decoder (F) just working (ON) when :

A = 1, B = 1, C = 0, D = 0

d) Decoder that have output

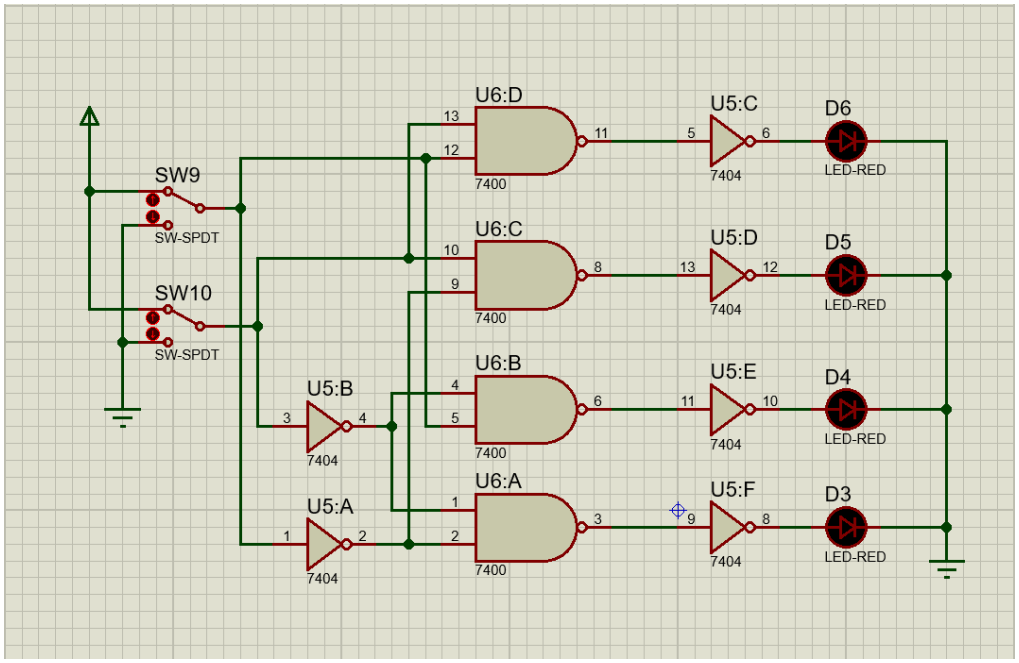
F = 1

A = 0 B = 1 C = 1 D = 1 (F = A'BCD)



Experiment 2

a. Make a combination of logic gate



b. Truth table

Input		Output LED			
SW1	**SW2**	**D1**	**D2**	**D3**	**D4**
0	**0**	**0**	**0**	**0**	**1**
0	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**0**
1	**1**	**1**	**0**	**0**	**0**

c. Each Diode (LED) Showed the output from the circuit combination :

D1 = SW1.SW2

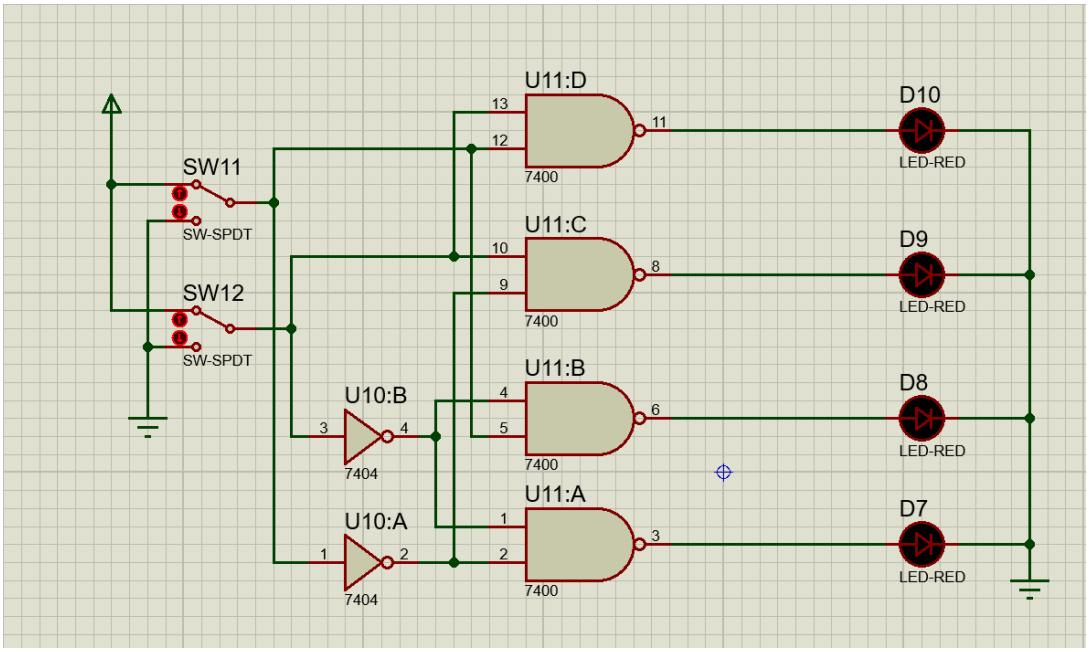
D2 = $\overline{SW1}$.SW2

D3 = SW1.$\overline{SW2}$

D4 = $\overline{SW1}$. $\overline{SW2}$

Experiment 3

a. Make a combination of logic gate



b. Truth table

Input		**Output LED**			
SW1	**SW2**	**D1**	**D2**	**D3**	**D4**
0	**0**	1	1	1	0
0	**1**	1	0	1	1
1	**0**	1	1	0	1
1	**1**	0	1	1	1

c. Each of Diode (LED) showed the output from the circuit combination :

D1 = $\overline{SW1.SW2}$

D2 = SW1. $\overline{SW2}$

D3 = $\overline{SW1}$.SW2

D4 = SW1.SW2

d. Conclusion

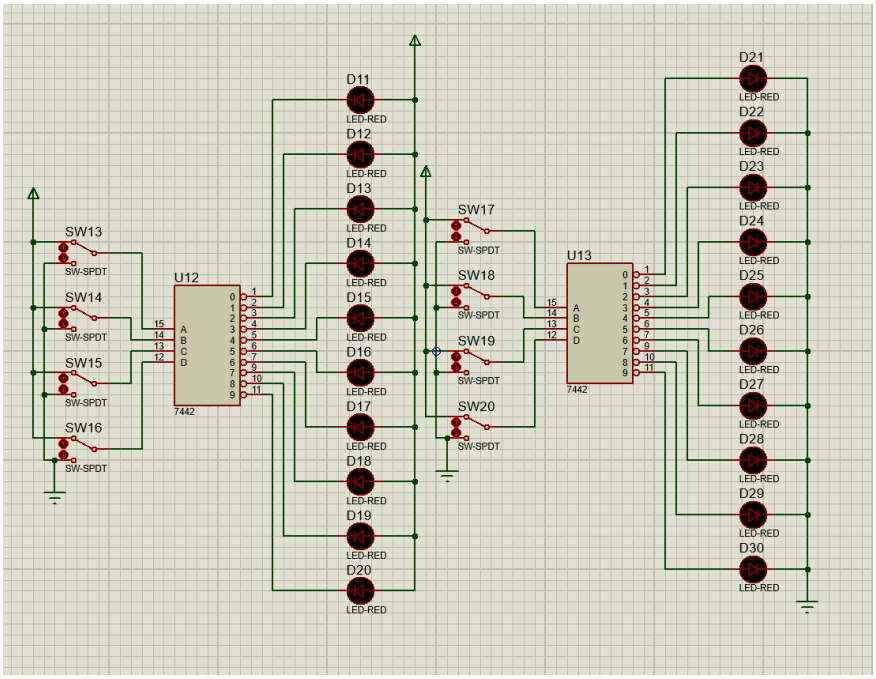
- Exercise 2 use AND gate
- Exercise 3 use NAND gate
- **NOT** affects the output of the LED.

  the output of the LED using **NOT** will be inversely proportional to the output of the LED that does not use **NOT**

Experiment 4

a) Circuit

a. Anode LED circuit



Picture 4.1 (Left Side is Common anode LED Circuit)

(The Right Side is Common Cathode LED Circuit)

b) Truth table

Anode LED circuit

Input				Output									
SW4	**SW3**	**SW2**	**SW1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	**0**	**0**	**0**	1	0	0	0	0	0	0	0	0	0
0	**0**	**0**	**1**	0	1	0	0	0	0	0	0	0	0
0	**0**	**1**	**0**	0	0	1	0	0	0	0	0	0	0
0	**0**	**1**	**1**	0	0	0	1	0	0	0	0	0	0
0	**1**	**0**	**0**	0	0	0	0	1	0	0	0	0	0
0	**1**	**0**	**1**	0	0	0	0	0	1	0	0	0	0
0	**1**	**1**	**0**	0	0	0	0	0	0	1	0	0	0
0	**1**	**1**	**1**	0	0	0	0	0	0	0	1	0	0

1	**0**	**0**	**0**	0	0	0	0	0	0	0	0	1	0
1	**0**	**0**	**1**	0	0	0	0	0	0	0	0	0	1
1	**0**	**1**	**0**	0	0	0	0	0	0	0	0	0	0
1	**0**	**1**	**1**	0	0	0	0	0	0	0	0	0	0
1	**1**	**0**	**0**	0	0	0	0	0	0	0	0	0	0
1	**1**	**0**	**1**	0	0	0	0	0	0	0	0	0	0
1	**1**	**1**	**0**	0	0	0	0	0	0	0	0	0	0
1	**1**	**1**	**1**	0	0	0	0	0	0	0	0	0	0

Cathode LED circuit

Input				**Output**									
SW4	**SW3**	**SW2**	**SW1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	**0**	**0**	**0**	0	1	1	1	1	1	1	1	1	1
0	**0**	**0**	**1**	1	0	1	1	1	1	1	1	1	1
0	**0**	**1**	**0**	1	1	0	1	1	1	1	1	1	1
0	**0**	**1**	**1**	1	1	1	0	1	1	1	1	1	1
0	**1**	**0**	**0**	1	1	1	1	0	1	1	1	1	1
0	**1**	**0**	**1**	1	1	1	1	1	0	1	1	1	1
0	**1**	**1**	**0**	1	1	1	1	1	1	0	1	1	1
0	**1**	**1**	**1**	1	1	1	1	1	1	1	0	1	1
1	**0**	**0**	**0**	1	1	1	1	1	1	1	1	0	1
1	**0**	**0**	**1**	1	1	1	1	1	1	1	1	1	0
1	**0**	**1**	**0**	1	1	1	1	1	1	1	1	1	1
1	**0**	**1**	**1**	1	1	1	1	1	1	1	1	1	1
1	**1**	**0**	**0**	1	1	1	1	1	1	1	1	1	1
1	**1**	**0**	**1**	1	1	1	1	1	1	1	1	1	1
1	**1**	**1**	**0**	1	1	1	1	1	1	1	1	1	1
1	**1**	**1**	**1**	1	1	1	1	1	1	1	1	1	1

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM7442A
BCD to Decimal Decoder

General Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

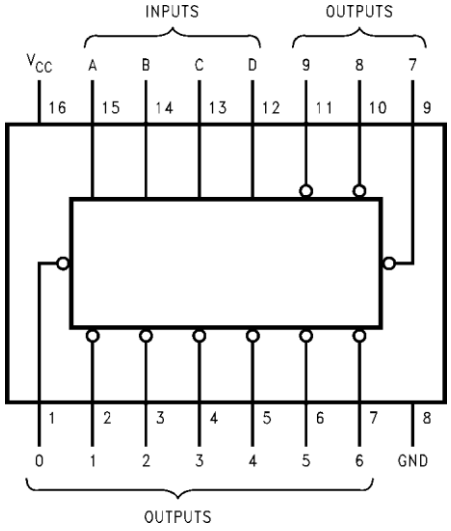
Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 140 mW
- Typical propagation delay 17 ns

Ordering Code:

Order Number	Package Number	Package Description
DM7442AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

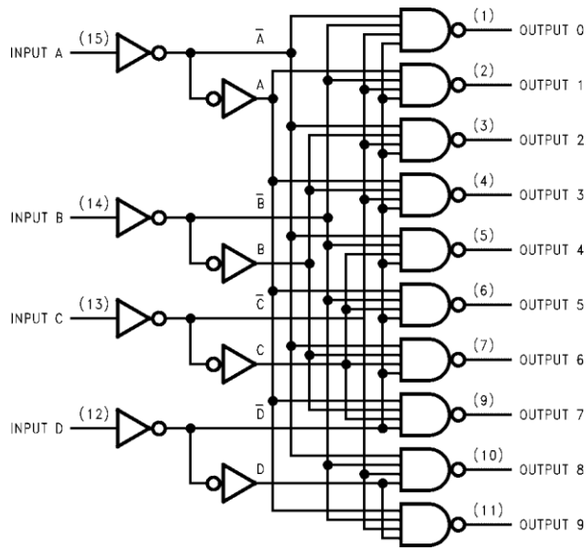


Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = HIGH Level
L = LOW Level

Logic Diagram



Absolute Maximum Ratings(Note 1) Supply

Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.8	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)		28	56	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

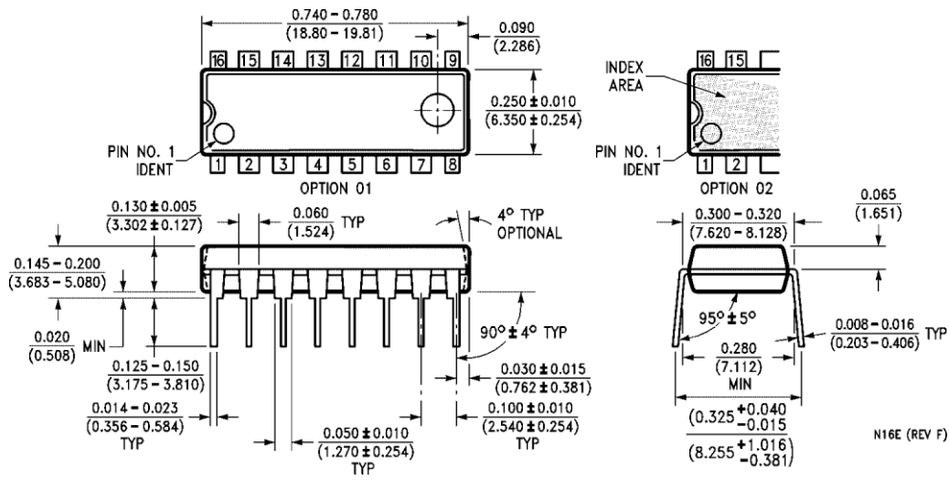
Note 4: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output from A, B, C or D through 2 Levels of Logic	C_L = 15 pF R_L = 400Ω		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output from A, B, C or D through 3 Levels of Logic			30	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output from A, B, C or D through 2 Levels of Logic			25	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output from A, B, C or D through 3 Levels of Logic			30	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E