PRACTICUM DIGITAL SYSTEM

MODUL 7

DIGITAL SYSTEM

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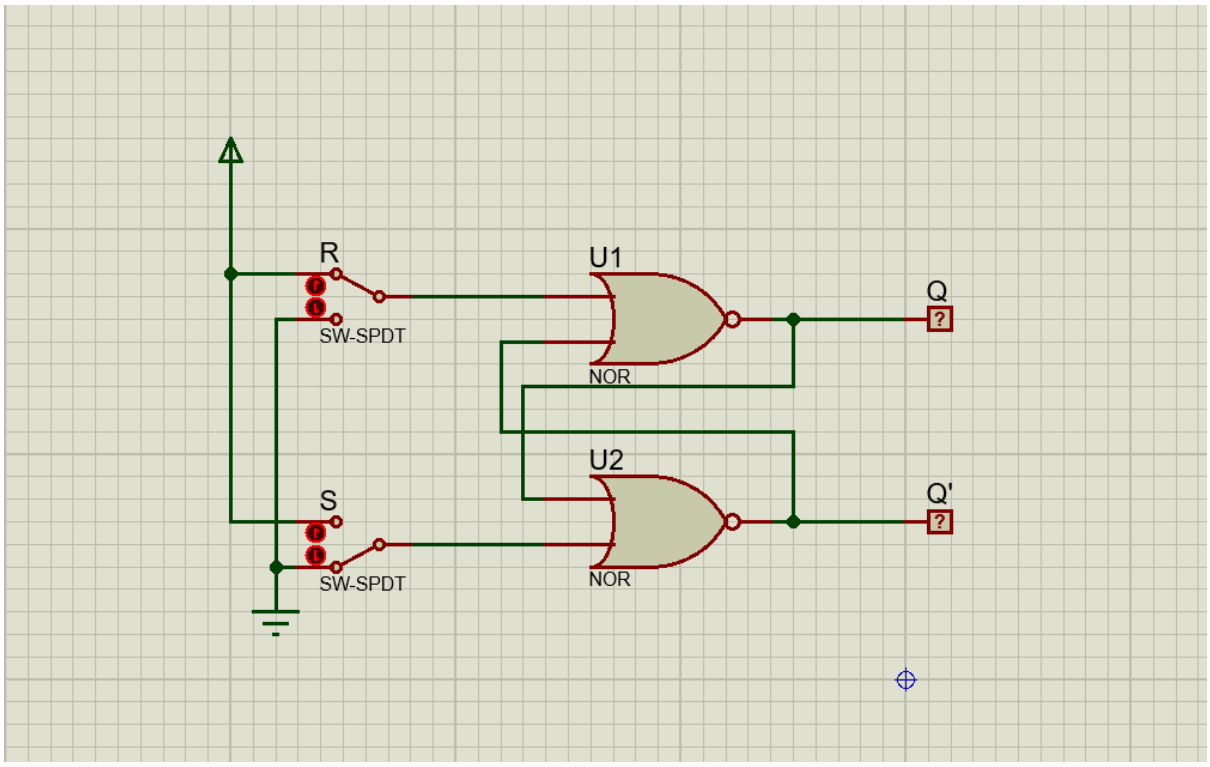
Experiment 1 (NOR Latch)



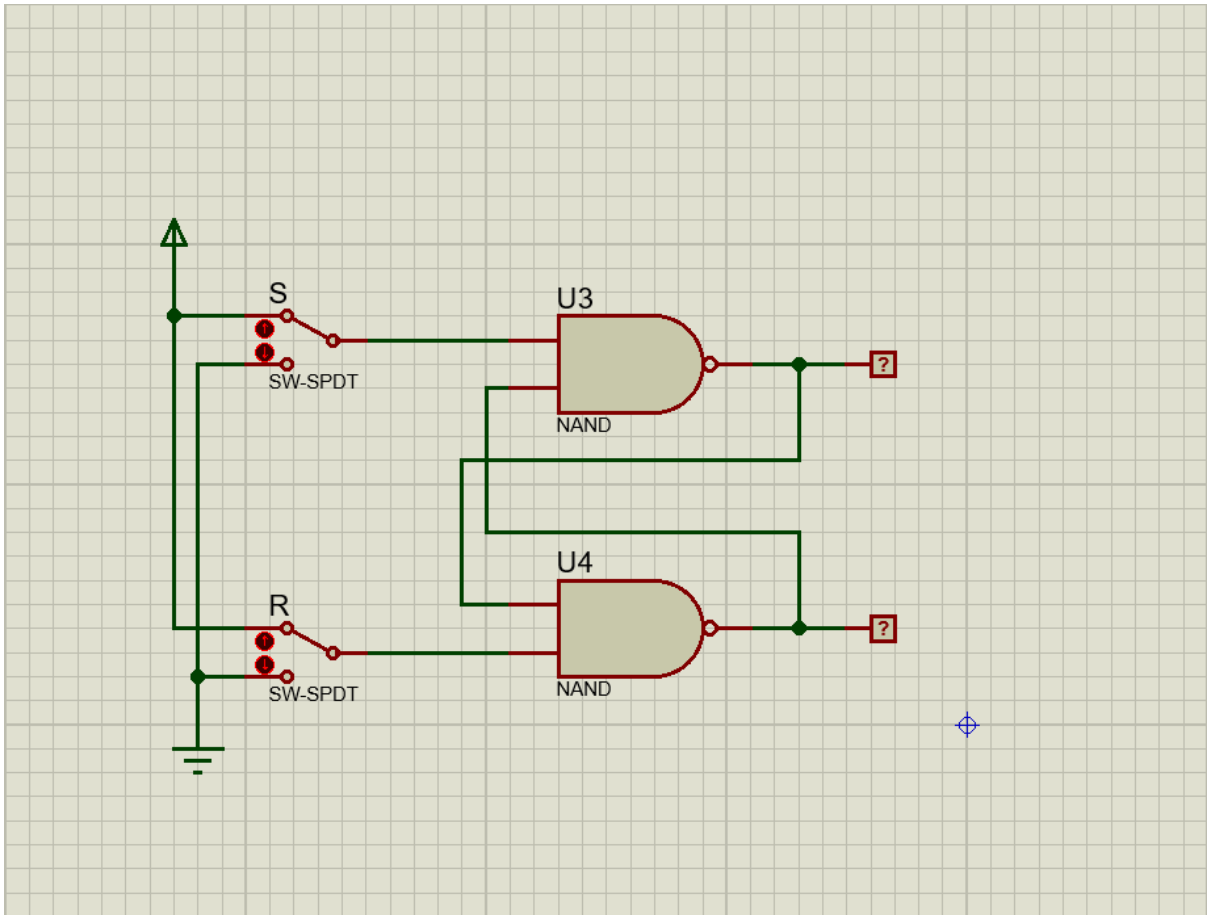
Picture 1.1 NOR Latch

	S (Set)	R (Reset)	Output	
			Q	Q’
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

Answer the question below!

a. What will happen if we give the condition S = R = 0?
   ⇨ The same as before, basically NOR Latch as the storage from output before.
b. Why the condition for S = R = 1, it is prohibited?
   ⇨ Because it can’t be the same and it will gives the output 0

Experiment 2. (NAND Latch)



Picture 2.1 NAND Latch

	S (Set)	R (Reset)	Output	
			Q	Q'
1	0	1	1	0
2	1	1	1	0
3	1	0	0	1
4	1	1	0	1
5	0	0	1	1

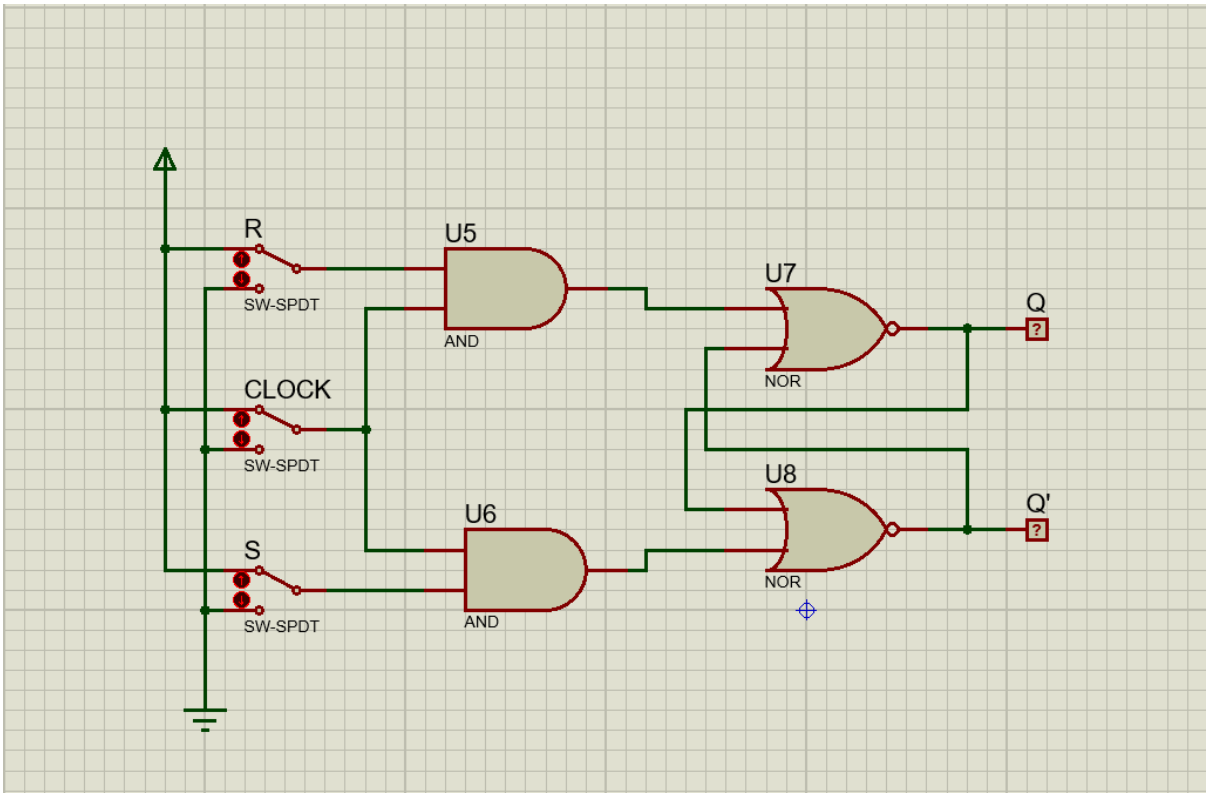
Answer the question below!

a. What will happen if we give the condition for S = R = 1?
   ⇨ As the data storage before, I mean it will give the output the same as before.
b. Why the condition S = R = 0 is prohibited?
   ⇨ Because it can be the same and will give the output 1

Based on the Circuit flip-flop above, what is your opinion about the statement "Flip-flop and latch use for an Element Storage data"?

⇨ Yes, it is true. Latch as the storage data that use in Electronics that has two stable states to store state Information.

Experiment 3 (Flip Flop RS)



Picture 3.1 Flip – Flop RS

	S (Set)	R (Reset)	Clock	Output	
				Q	$Q_{(t+1)}$
1	0	0	0	--	--
2	0	0	1	--	--
3	0	1	0	--	--
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

Answer the question below!

a. What will happen if we give the condition S = R = 1 and the clock changes from 1 into 0?
   ⇨ Simulation Error. “Logic race condition detected during transient system”

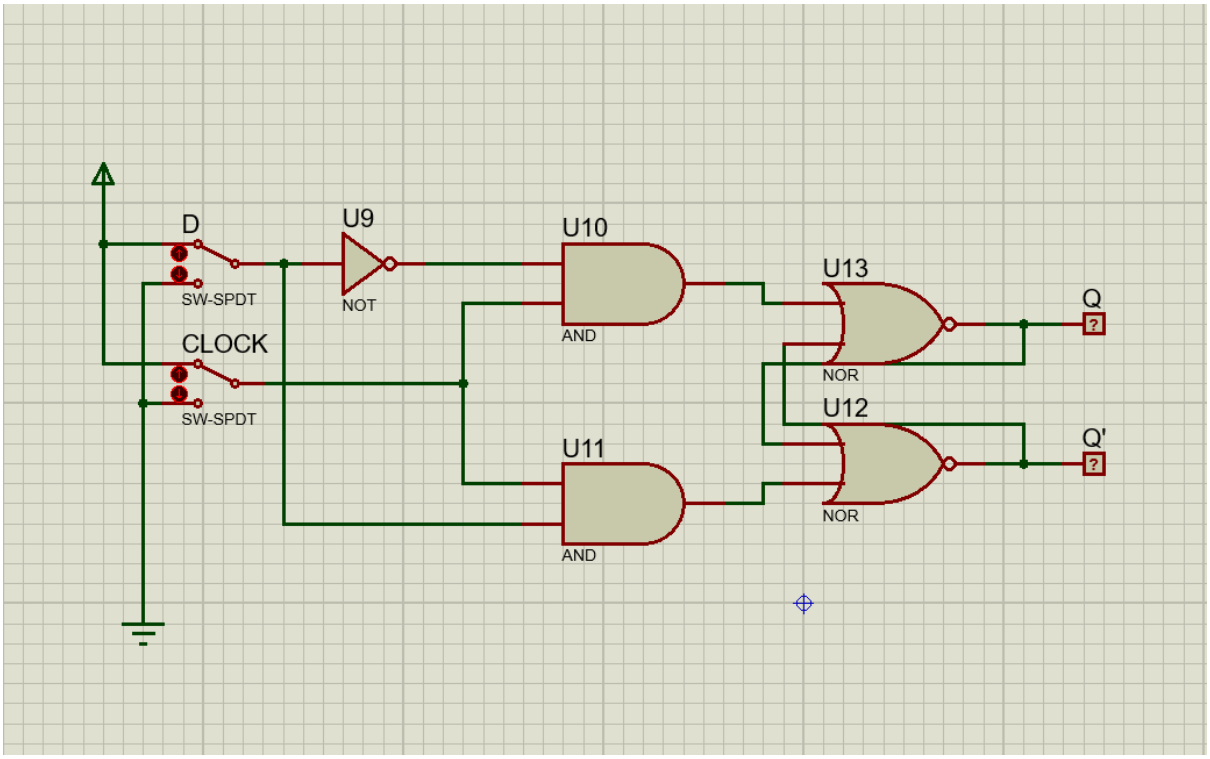
   How that’s possible?
   ⇨ Because S = R = 1 and clock changes from 1 into 0. And it is prohibited the clock in 0 condition.

Explain how Flip – Flop RS Works?

⇨ RS = 00 So it will lock the output before
RS = 01 it will changes the output Q to $Q_{(t+1)}$

RS = 10 it changes the output Q became 0
RS = 11 the prohibited one and error will occurs.
For the most Clock Has to Not 0 first, When you need to know the result in Flip-Flop RS without error your Clock has to 1 First then change the Set and Reset.

Experiment 4 (Flip – Flop D)



Picture 4.1 Flip Flop D

	D	Clock	Output	
			Q	$Q_{(t+1)}$
1	0	0	--	--
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

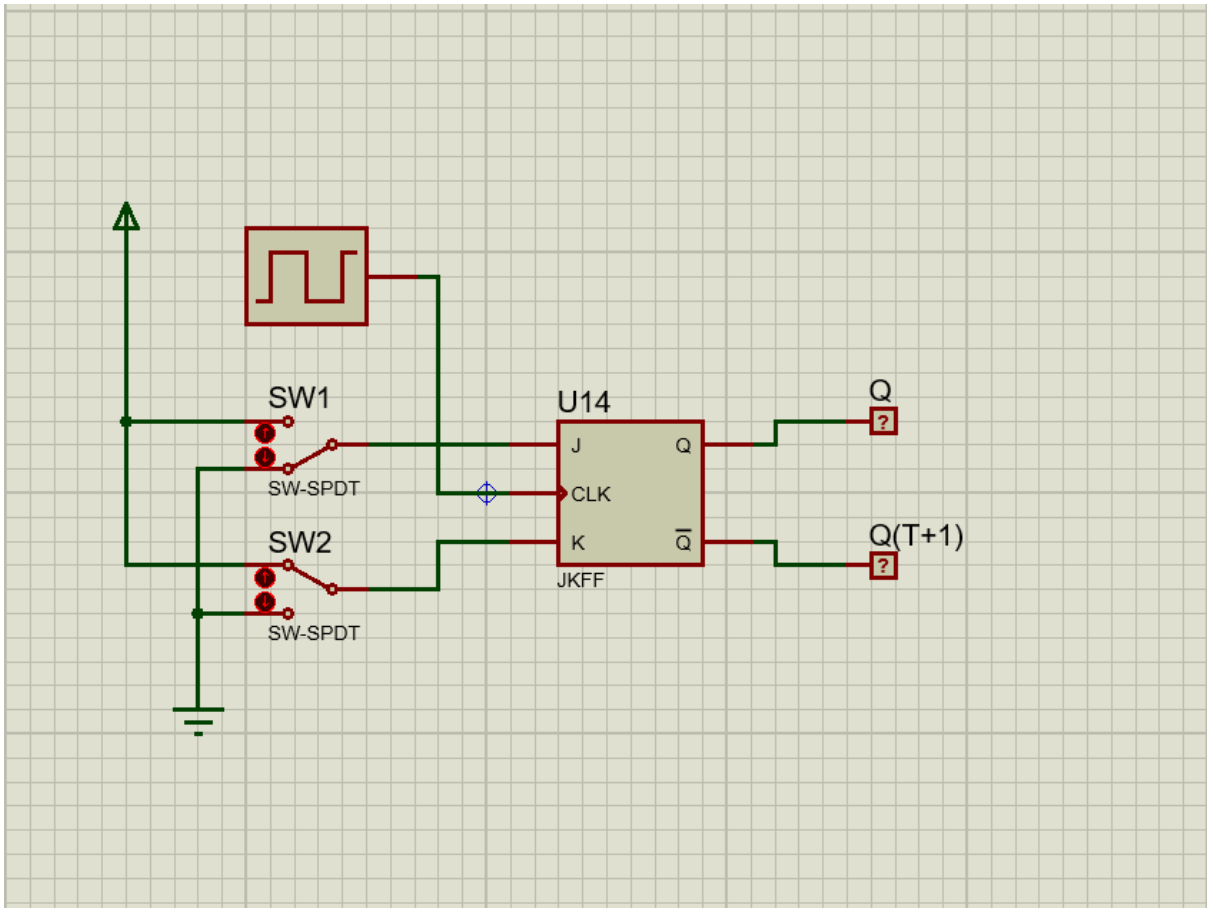
Explain How Flip – Flop D work!

- ⇨ If Clock Output is 0 so it could be as Latch and lock the Output before
  If Clock Output is 1 so it could change the Output Q

What is the Function of NOT gate in Flip – Flop D compared with Flip – Flop RS!

- ⇨ To solve the Prohibited condition in Flip – Flop RS

Experiment 5 (Flip – Flop JK)



Picture 5.1 Flip – Flop JK

	J	K	Clock	Output	
				Q	$Q_{(t+1)}$
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	1	1

What will happen if J = K = 0 and Clock rise up (Change from 0 to 1)?

- ⇨ Clock output will change overtime but doesn't change the output Q and $Q_{(t+1)}$

What will happen if J = K = 1, and Clock Rise Up?

- ⇨ If the Clock 1 so Output Q and $Q_{(t+1)}$ will be changed too.
- ⇨ If the Clock 0 so it will store the Output Q and $Q_{(t+1)}$

Explain how Flip – Flop Works!

- ⇨ How it works it is same as Flip – Flop RS just the prohibited condition (J = K = 1, Clock Up) can be done (Solved) .