DIGITAL SYSTEMS

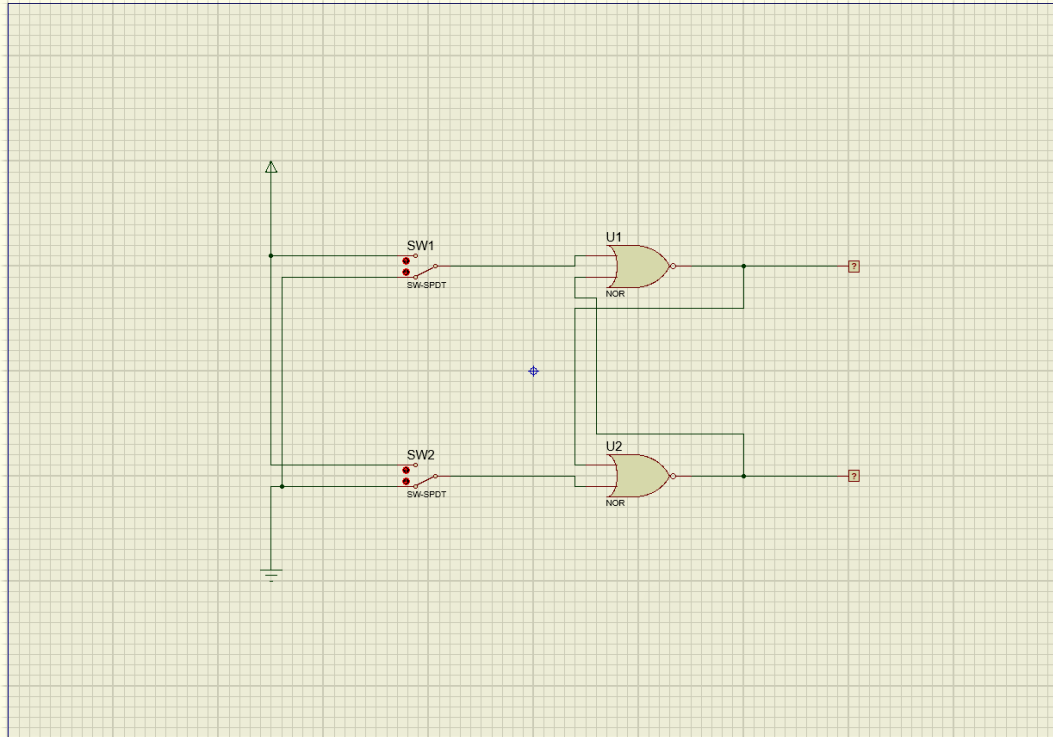**PRACTICUM 7**

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Experiment 1

Picture 1.1. NOR Latch

1. Table based on simulation

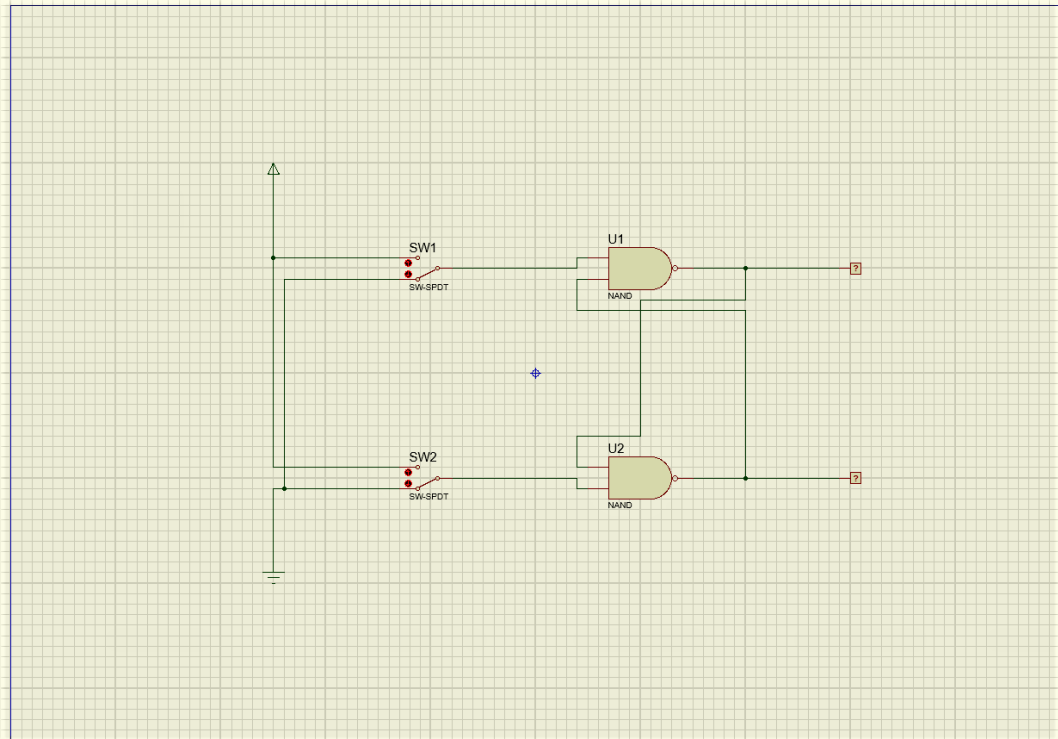|	S (Set)	R (Reset)	O	Output O'
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

2. What will happen if we are given the condition S = R = 0?

   Answer: The output results are the same as the previous conditions.

3. Why is the condition S = R = 1 not allowed?

   Answer: Because it can break the logic equation Q = not Q'.

Experiment 2

Picture 2.1. NAND Latch

1. Table based on simulation

	S (Set)	R (Reset)	O Output O'	
1	0	1	1	0
2	1	1	1	0
3	1	0	0	1
4	1	1	0	1
5	0	0	1	1

2. What will happen if we give the condition S = R = 1?

       Answer: The output results are the same as the previous conditions.

3. Why is the condition S = R = 0 not allowed?

       Answer: Because it can break the logic equation Q = not Q'.

4. Based on the flip-flop analysis above, what do you think of the statement "Flip-flop and latch are used as data storage elements"?

       Answer: Like data storage that can be used to store memory, such as circuits described in sequential logic. When using Read-only

Memory, the output and the next state depend not only on the initial input, but also on the current state.

Experiment 3
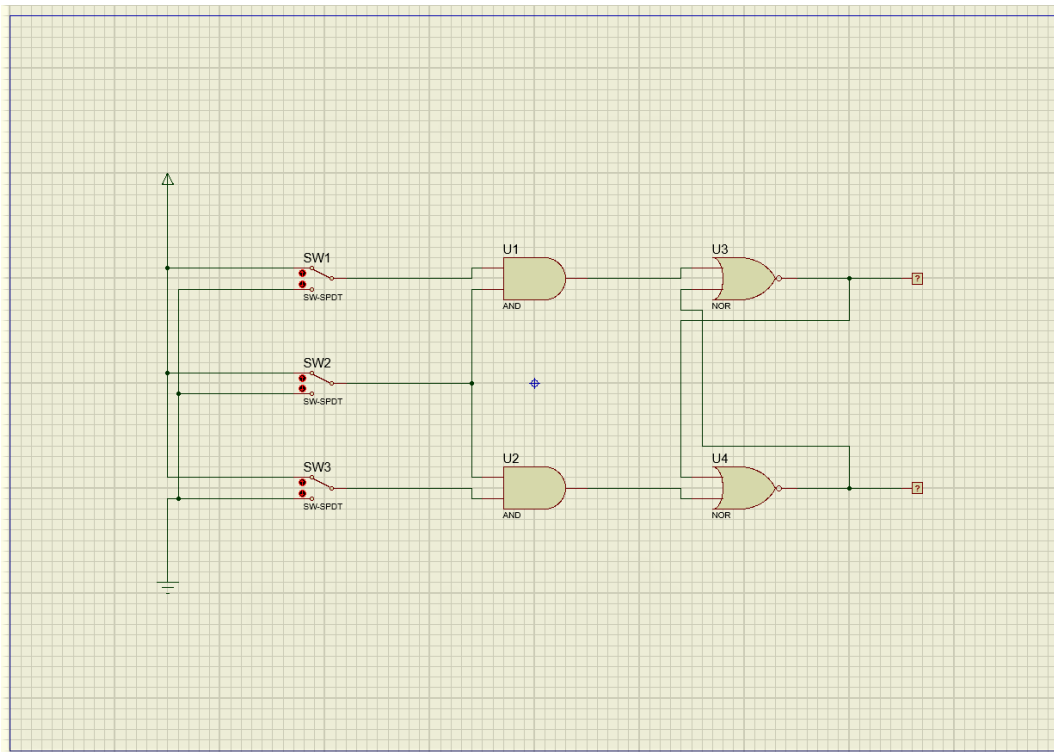
Picture 3.1. Flip-flop RS

1. Table based on simulation

	S (Set)	R (Reset)	CLOCK	Output	
				Q	$Q_{(t+1)}$
1	0	0	0	-	-
2	0	0	1	-	-
3	0	1	0	-	-
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

2. What will happen if we give the condition S = R = 1 and the clock changes from 1 to 0?

   Answer: Logic race condition detected during transient analysis.

3. How can the above conditions occur?

   Answer: The output of the flip-flop will not change as long as the clock pulse is 0.

4. Explain how RS flip-flops work!

    Answer: SR or RS type flip-flop is a type of flip-flop that has asynchronous input S (Set) or R (Reset) or both, with output Q and Q '. Input S and R can be synchronized by adding a clock input to the circuit. Q output cannot respond to S and R inputs before input clock.

Experiment 4
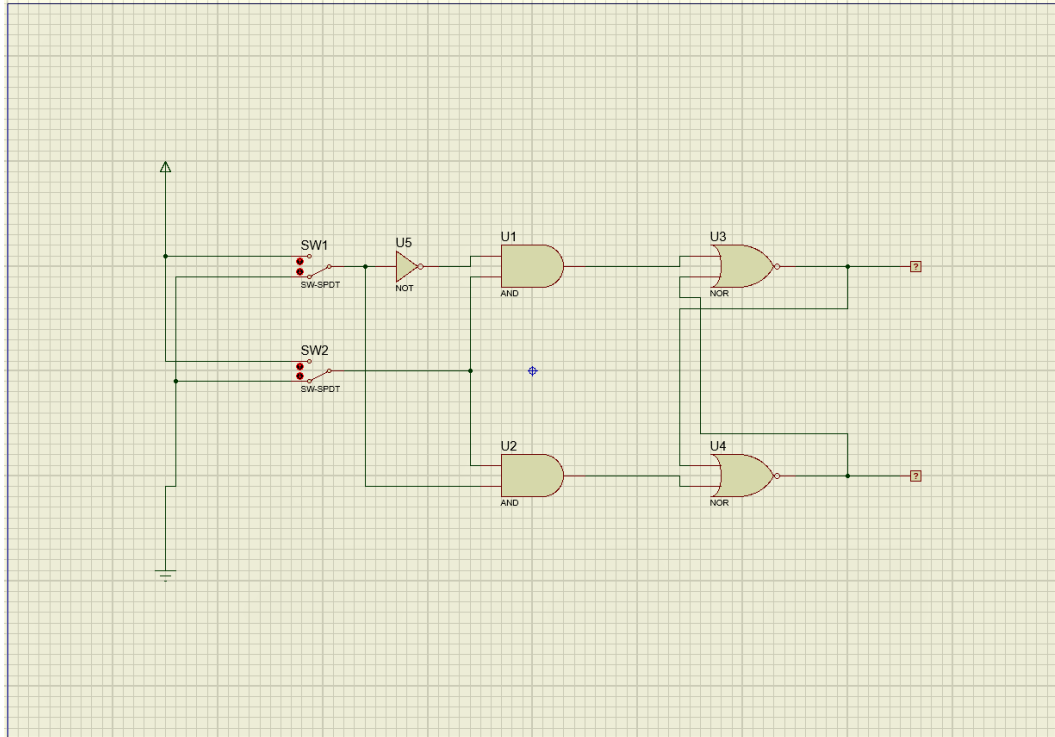
Picture 4.1. Flip-flop D

1. Table based on simulation

	D	CLOCK	Q Output Q$_{(t+1)}$	
1	0	0	0	0
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

2. Explain how D flip-flops work!

Answer: D flip-flop has only one data input and one input clock. "D" is referred to as a flip-flop delay or delay. "Delay" explains what happens to stored data, or at input D. Data (0 or 1) is delayed by 1 pulsaclock from input to output Q. There are many ways to design this D flip-flop circuit. Basically, D flip-flop is a

multivibrator with a dual state (bistable) whose input D is transferred to the output after receiving a clock pulse.

3. What is the function of the NOT gate on the flip-flop D compared to the RS flip-flop?

Answer: For the data input flow, SET gets input directly from the NOT gate which is connected directly to the input data then passes through the NAND gate and then produces the output. Whereas for the input RESET that arrives at the inverter gate and NOT gate before arriving at RESET, then the input is forwarded to the NAND gate before generating output.

Experiment 5
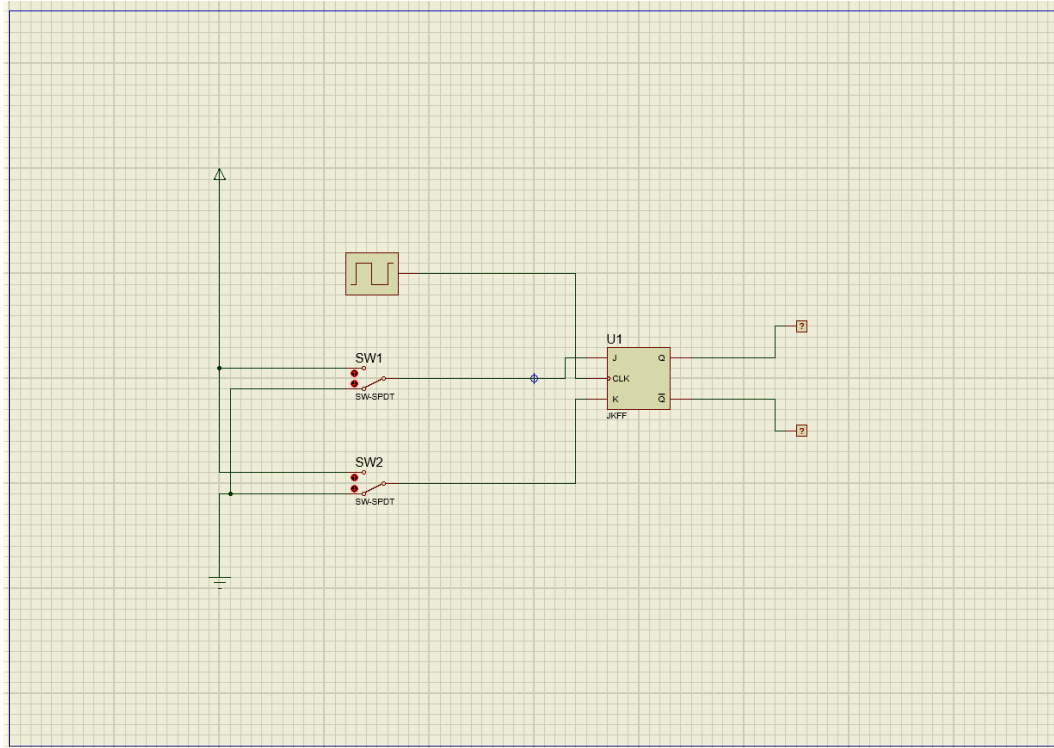
Picture 5.1. Flip-flop JK

1. Table based on simulation

	J	K	CLOCK	Output	
				Q	Q(t+1)
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	1

2. What will happen if J = K = 0, and clock rise up (change for 0 to 1)?

   Answer: Output Q remains the last value or state.

3. What will happen if J = K = 1, and clock rise up?

   Answer: Then you can adjust the flip-flop or reset it.

4. Explain how the JK flip-flop works!

Answer: J and K are called control inputs to determine what the flip-flop will do when receiving an increased clock pulse. RC circuits have short time constants so that they convert clock pulses into narrow impulses.