

**DIGITAL SYSTEMS**

**PRACTICUM 8**



**MOHAMMAD FAQIH EZA AMMAR**

**NIM: L200183178**

**INFORMATION TECHNOLOGY**

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DM7442A BCD to Decimal

## DM7442A BCD to Decimal Decoder

### General Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

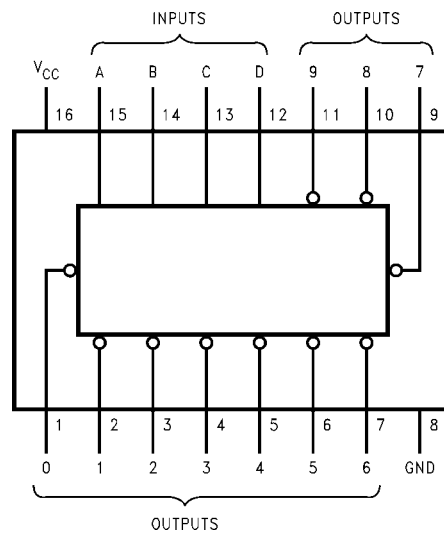
### Features

Diode clamped inputs  
Also for application as 4-line-to-16-line decoders;  
3-line-to-8-line decoders  
All outputs are high for invalid input conditions  
Typical power dissipation 140 mW  
Typical propagation delay 17 ns

### Ordering Code:

Order Number	Package Number	Package Description
DM7442AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

## Connection Diagram

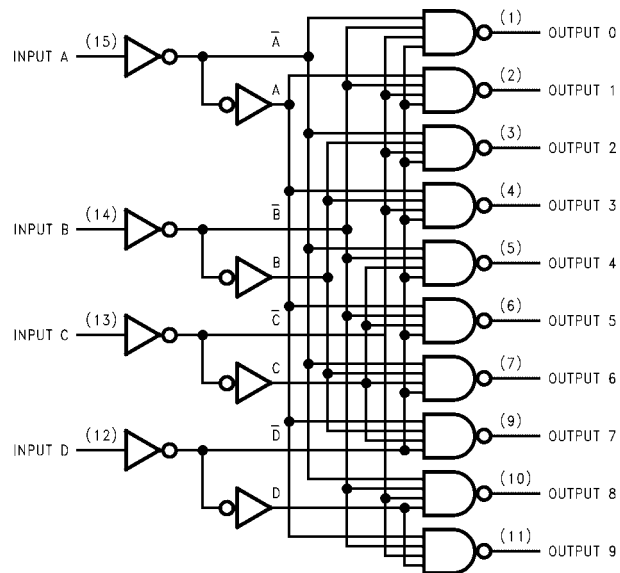


## Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = HIGH Level  
L = LOW Level

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			–0.8	mA
$I_{OL}$	LOW Level Output Current			16	mA
$T_A$	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12 \text{ mA}$			–1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.4	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$		0.2	0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4 \text{ V}$			40	μA
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			–1.6	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	–18		–55	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 4)		28	56	mA

**Note 2:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

**Note 3:** Not more than one output should be shorted at a time.

**Note 4:**  $I_{CC}$  is measured with all outputs open and all inputs grounded.

**Switching Characteristics**

at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ \text{C}$

Symbol	Parameter	Conditions	Min	Max	Units
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output from A, B, C or D through 2 Levels of Logic	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output from A, B, C or D through 3 Levels of Logic			30	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output from A, B, C or D through 2 Levels of Logic			25	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output from A, B, C or D through 3 Levels of Logic			30	ns

[illegible]

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