

DIGITAL SYSTEMS

PRACTICUM 10



MOHAMMAD FAQIH EZA AMMAR

NIM: L200183178

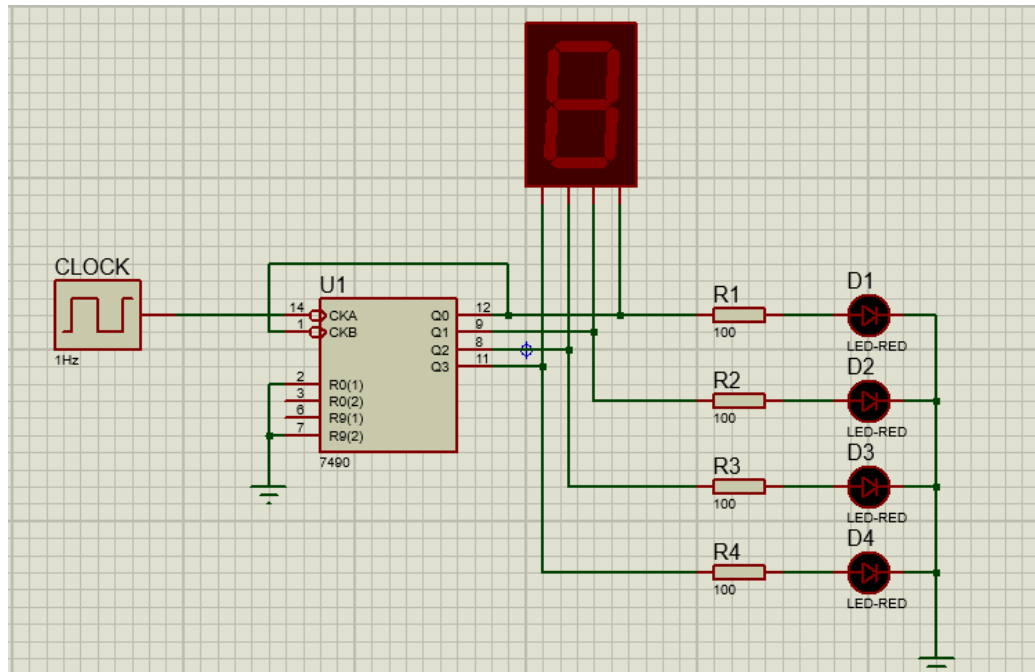
INFORMATION TECHNOLOGY

FACULTY OF COMMUNICATION AND INFORMATICS

UNIVERSITY OF MUHAMMADIYAH SURAKARTA

Experiment 1

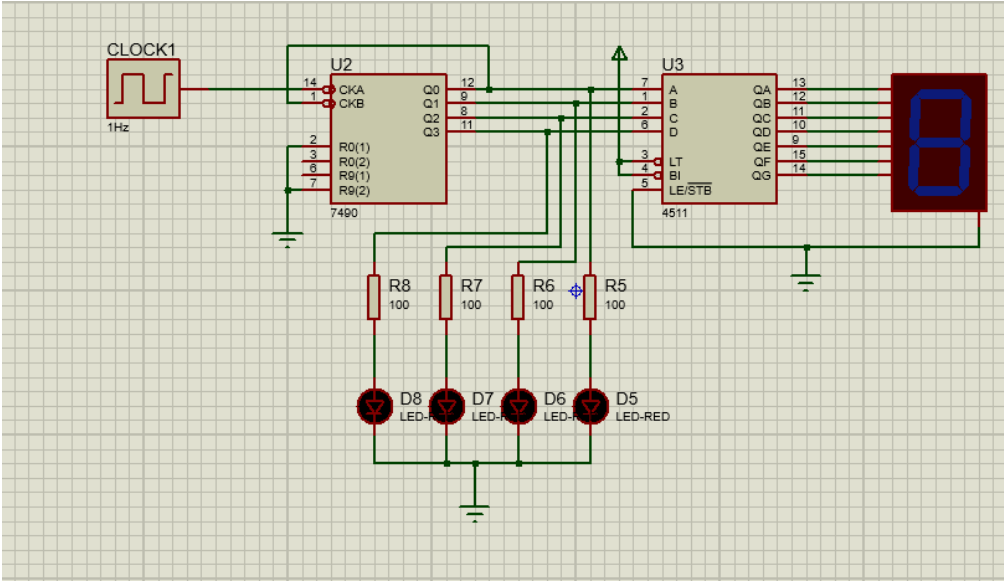
1. Circuit Board



2. Coloumn Table

| Input Clock | Output LED | | | | Output Seven Segment |
|----------------|------------|----|----|----|----------------------------|
| | D1 | D2 | D3 | D4 | |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 | 0 | 1 |
| 3 | 0 | 1 | 0 | 0 | 2 |
| 4 | 1 | 1 | 0 | 0 | 3 |
| 5 | 0 | 0 | 1 | 0 | 4 |
| 6 | 1 | 0 | 1 | 0 | 5 |
| 7 | 0 | 1 | 1 | 0 | 6 |
| 8 | 0 | 1 | 1 | 0 | 7 |
| 9 | 0 | 0 | 0 | 1 | 8 |
| 10 | 1 | 0 | 0 | 1 | 9 |
| 11 | 0 | 0 | 0 | 0 | 0 |
| 12 | 1 | 0 | 0 | 0 | 1 |
| 13 | 0 | 1 | 0 | 0 | 2 |

Experiment 2



1. Column Table

| Input Clock | Output LED | | | | Output Seven Segment |
|-------------|------------|----|----|----|----------------------|
| | D1 | D2 | D3 | D4 | |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 | 0 | 1 |
| 3 | 0 | 1 | 0 | 0 | 2 |
| 4 | 1 | 1 | 0 | 0 | 3 |
| 5 | 0 | 0 | 1 | 0 | 4 |
| 6 | 1 | 0 | 1 | 0 | 5 |
| 7 | 0 | 1 | 1 | 0 | b |
| 8 | 0 | 1 | 1 | 0 | 7 |
| 9 | 0 | 0 | 0 | 1 | 8 |
| 10 | 1 | 0 | 0 | 1 | 9 |
| 11 | 0 | 0 | 0 | 0 | 0 |

2. Compare the experiment 1 with Experiment 2! Could you spot the similarity and the difference?
- The Experiment 1 in the number 6 and the Experiment 2 is different which means that Experiment 1 the output 7 seg is 6 and experiment 2 the result is b.
3. Is that true which 7 seg-BCD same with BCD to 7 Segment decoder?
- No!!!

DM7490A

Decade and Binary Counter

General Description

The DM7490A monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table. A symmetrical divide-by-ten count can be obtained from the counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

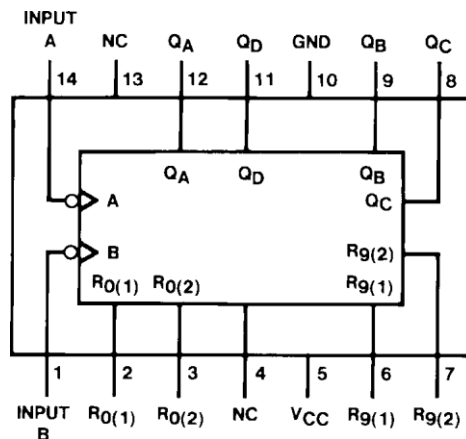
Features

Typical power dissipation
145 mW
Count frequency 42 MHz

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| DM7490AN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Connection Diagram



Function Tables

BCD Count Sequence (Note 1)

| Count | Outputs | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

BCD Bi-Quinary (5-2) (Note 2)

| Count | Outputs | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _A | Q _D | Q _C | Q _B |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

Reset/Count Function Table

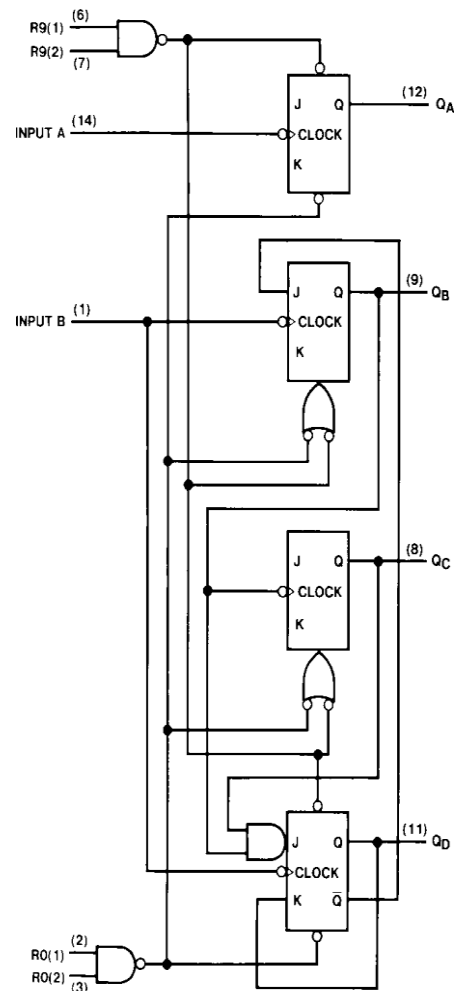
| Reset Inputs | | | | Outputs | | | |
|--------------|-------|-------|-------|----------------|----------------|----------------|----------------|
| R0(1) | R0(2) | R9(1) | R9(2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

H = HIGH
Level L = LOW
Level X = Don't
Care

Note 1: Output Q_A is connected to input B for BCD count.

Note 2: Output Q_D is connected to input A for bi-quinary count

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a HIGH level.

Absolute Maximum Ratings

(Note 3) Supply

Voltage

Input Voltage

7V

5.5V

Note 3: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Operating Free Air Temperature Range

0°C to +70°C

Storage Temperature Range

–65°C to +150°C

Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|------------------|--------------------------------|-------|------|-----|------|-------|
| V _{CC} | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| V _{IH} | HIGH Level Input Voltage | | 2 | | | V |
| V _{IL} | LOW Level Input Voltage | | | | 0.8 | V |
| I _{OH} | HIGH Level Output Current | | | | –0.8 | mA |
| I _{OL} | LOW Level Output Current | | | | 16 | mA |
| f _{CLK} | Clock Frequency (Note 4) | A | 0 | | 32 | MHz |
| | | B | 0 | | 16 | |
| t _w | Pulse Width (Note 4) | A | 15 | | | ns |
| | | B | 30 | | | |
| | | Reset | 15 | | | |
| t _{REL} | Reset Release Time (Note 4) | | 25 | | | ns |
| T _A | Free Air Operating Temperature | | 0 | | 70 | °C |

Note 4: T_A = 25°C and V_{CC} = 5V.

DC Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 5) | Max | Units |
|-----------------|-----------------------------------|---|-------|-----|-----------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = –12 mA | | | | –1.5 | V |
| V _{OH} | HIGH Level Output Voltage | V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min | | 2.4 | 3.4 | | V |
| V _{OL} | LOW Level Output Voltage | V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max (Note 6) | | | 0.2 | 0.4 | V |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 5.5V | | | | 1 | mA |
| I _{IH} | HIGH Level Input Current | V _{CC} = Max V _I = 2.7V | A | | | 80 | μA |
| | | | Reset | | | 40 | |
| | | | B | | | 120 | |
| I _{IL} | LOW Level Input Current | V _{CC} = Max V _I = 0.4V | A | | | –3.2 | mA |
| | | | Reset | | | –1.6 | |
| | | | B | | | –4.8 | |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 7) | | –18 | | –57 | mA |
| I _{CC} | Supply Current | V _{CC} = Max (Note 8) | | | 29 | 42 | mA |

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

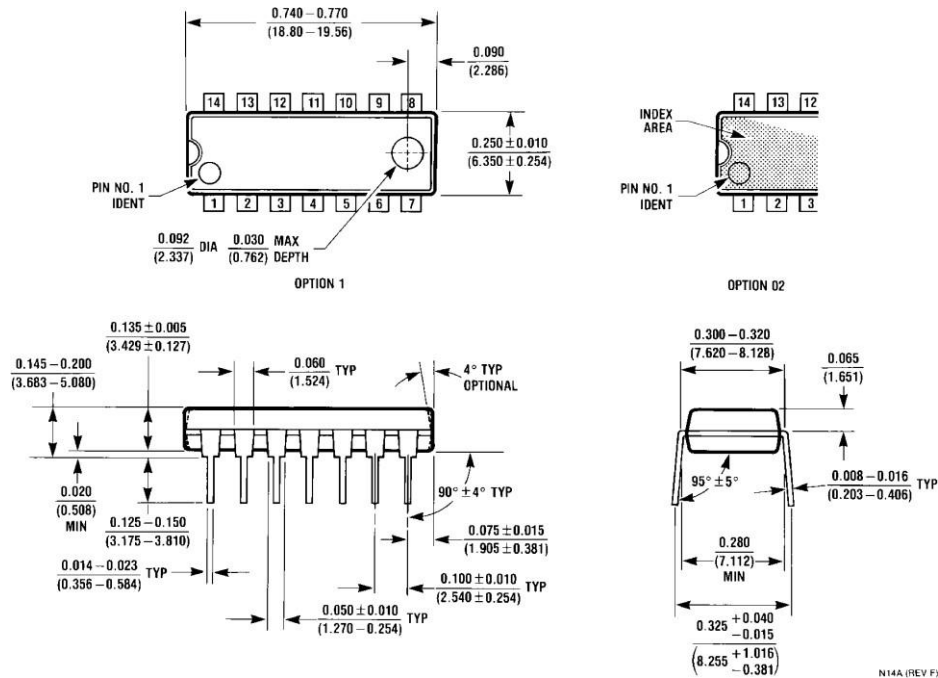
Note 6: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 7: Not more than one output should be shorted at a time.

Note 8: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

| AC Switching Characteristics | | | | | |
|--|--|-----------------------------|--|-----|-------|
| at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$ | | | | | |
| Symbol | Parameter | From (Input) To (Output) | $R_L = 400\Omega$, $C_L = 15\text{ pF}$ | | Units |
| | | | Min | Max | |
| f_{MAX} | Maximum Clock | A to Q_A | 32 | | MHz |
| | Frequency | B to Q_B | 16 | | |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | A to Q_A | | 16 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | A to Q_A | | 18 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | A to Q_D | | 48 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | A to Q_D | | 50 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | B to Q_B | | 16 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | B to Q_B | | 21 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | B to Q_C | | 32 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | B to Q_C | | 35 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | B to Q_D | | 32 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | B to Q_D | | 35 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | SET-9 to Q_A , Q_D | | 30 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | SET-9 to Q_B , Q_C | | 40 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | SET-0 Any Q | | 40 | ns |
| | | | | | |

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which,
 - (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

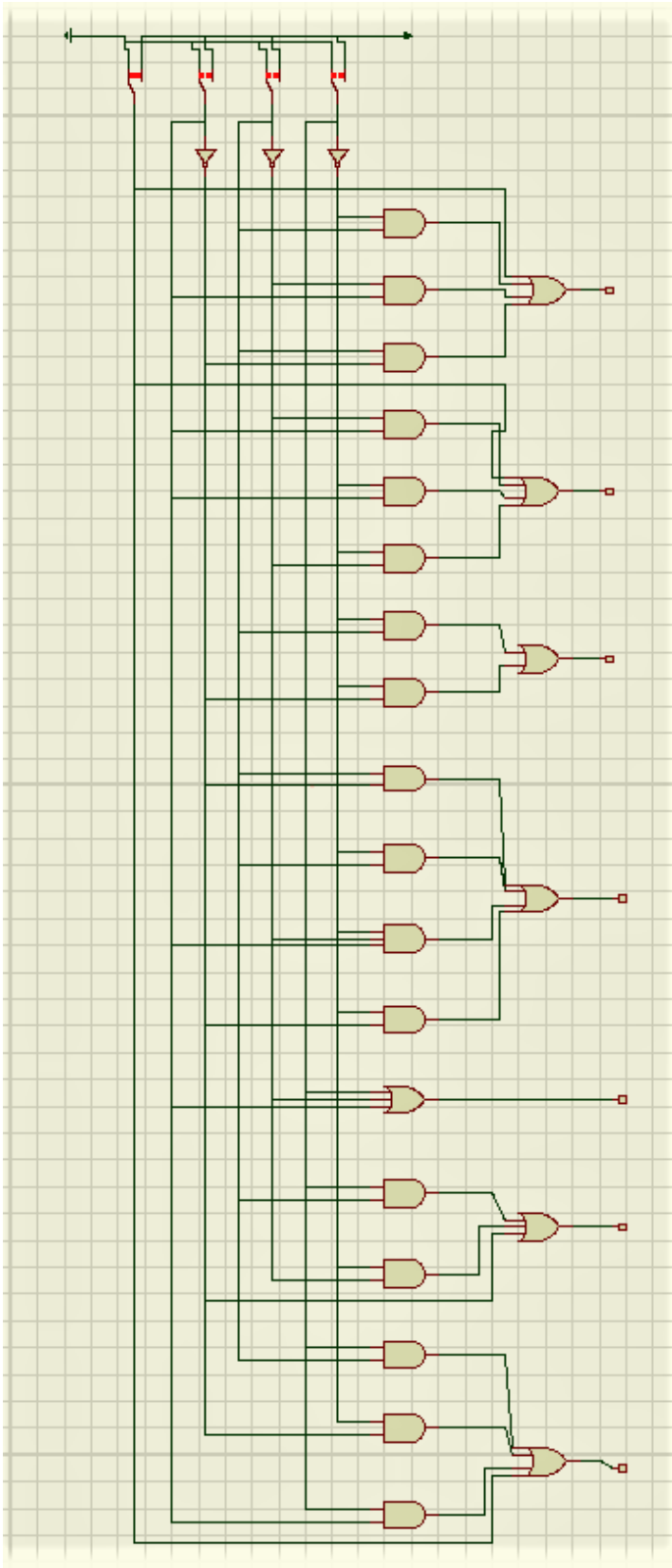
www.fairchildsemi.com

Experiment 3

1. Table function of IC 4511

| Decimal Digit | Input | | | | | Output | | | | | | | Display Output |
|---------------|-------|---|---|---|---|--------|---|---|---|---|---|---|----------------|
| | LT | D | C | B | A | a | b | c | d | e | f | g | |
| 0 | H | L | L | L | L | H | H | H | H | H | H | L | 0 |
| 1 | H | L | L | L | H | L | H | H | L | L | L | L | 1 |
| 2 | H | L | L | H | L | H | H | L | H | H | L | H | 2 |
| 3 | H | L | L | H | H | H | H | H | H | L | L | H | 3 |
| 4 | H | L | H | L | L | L | H | H | L | L | H | H | 4 |
| 5 | H | L | H | L | H | H | L | H | H | L | H | H | 5 |
| 6 | H | L | H | H | L | L | L | H | H | H | H | H | 6 |
| 7 | H | L | H | H | H | H | H | H | L | L | L | L | 7 |
| 8 | H | H | L | L | L | H | H | H | H | H | H | H | 8 |
| 9 | H | H | L | L | H | H | H | H | L | L | H | H | 9 |
| LT | L | X | X | X | X | H | H | H | H | H | H | H | 8 |

2. The output "a" (highlight) in the table shows that LED works in seven common cathode segments
3. Each output shows the state of LED from seven segment various conditions
4. Each LED is controlled by a combination of logic gates.



5. Comparison truth table with set of BCD-to-7segment

- The output results in the BCD-to-7-segment decoder circuit produce a value that exactly matches the truth table