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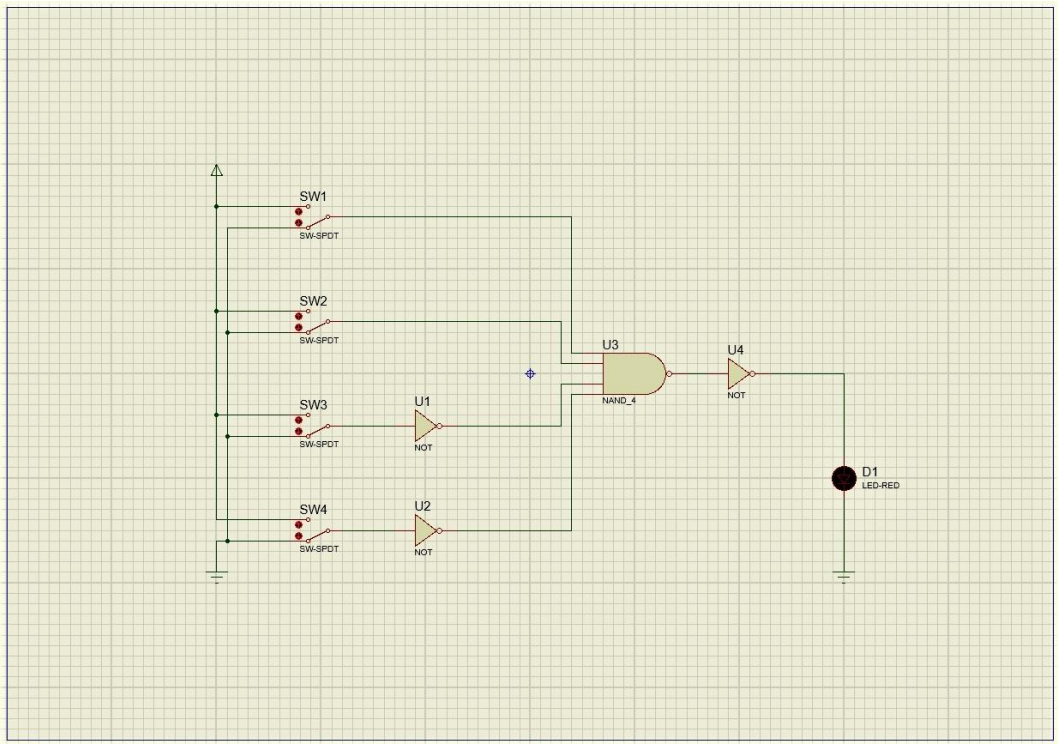
Experiment 1



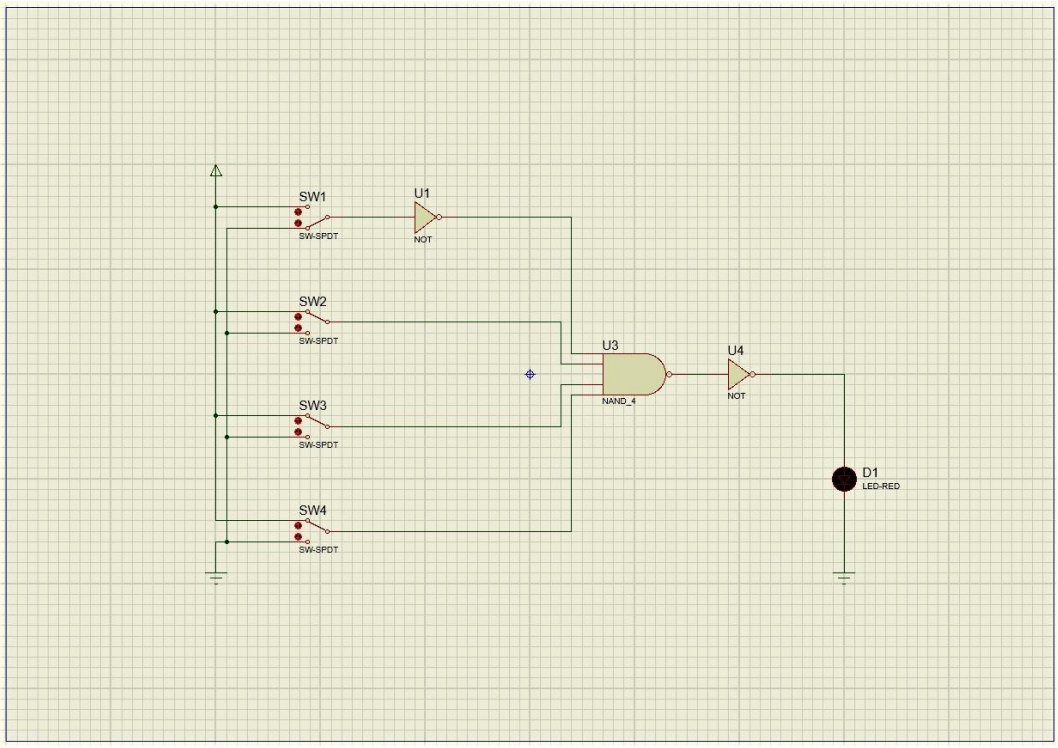
Picture 1.1. Set of decoder

1. Column table

A	B	C	D	F
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0

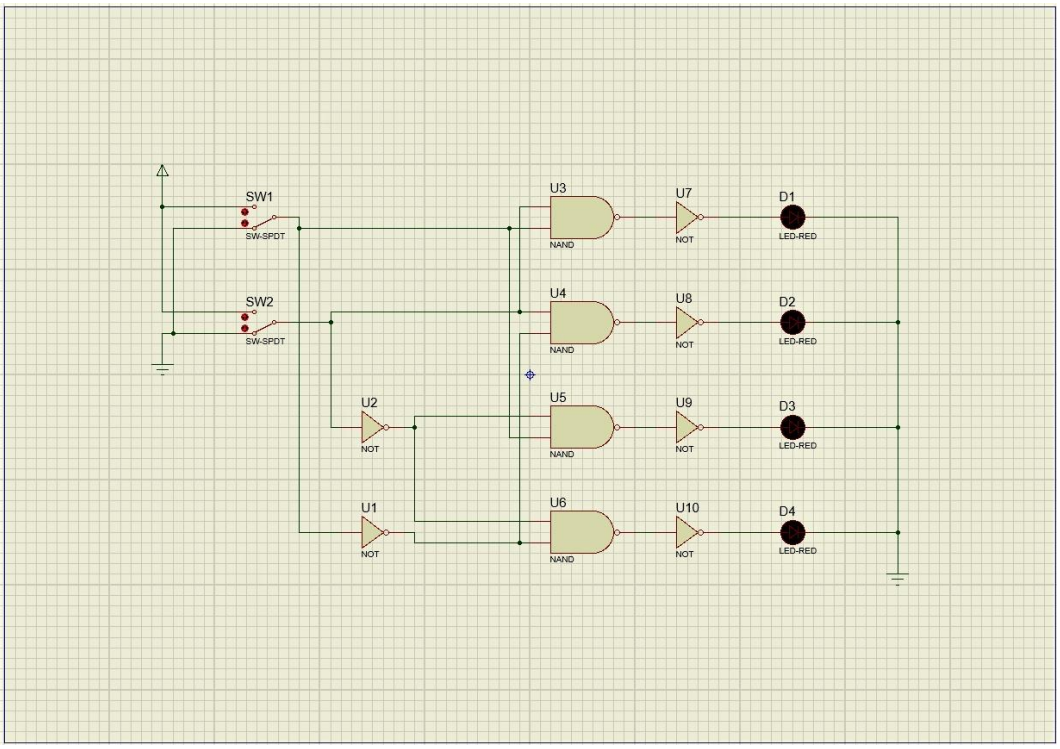
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

2. Decoder (F) only works (ON) when: A = 1, B = 1, C = 0, and D = 0.
3. Set of decoder that has output as a function: F = 1, if condition A = 0, B = 1, C = 1, D = 1. (F = A'BCD)



Picture 1.2. Set of decoder

Experiment 2



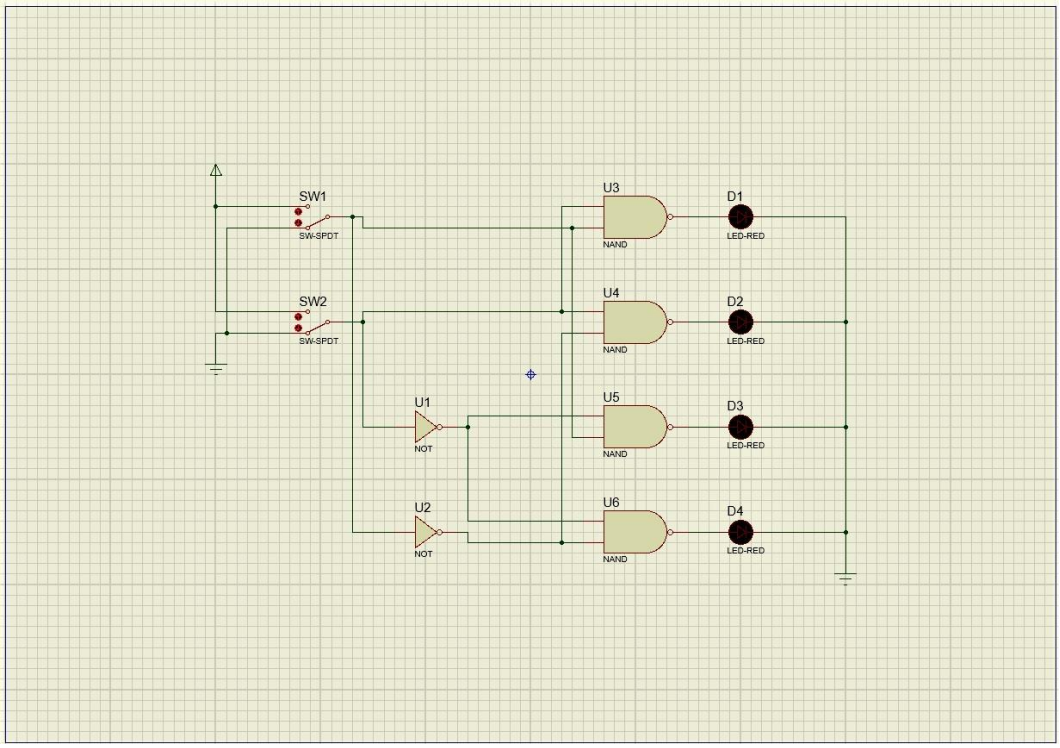
Picture 2.1. Logic gate combination

1. Column table

Input		**Output LED**			
SW1	**SW2**	**D1**	**D2**	**D3**	**D4**
0	0	0	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	1	0	0	0

2. Output result from the logic gate combination
    a. D1 = SW1 . SW2
    b. D2 = $\overline{SW1}$. SW2
    c. D3 = SW1 . $\overline{SW2}$
    d. D4 = $\overline{SW1}$. $\overline{SW2}$

Experiment 3



Picture 3.1. Logic gate combination

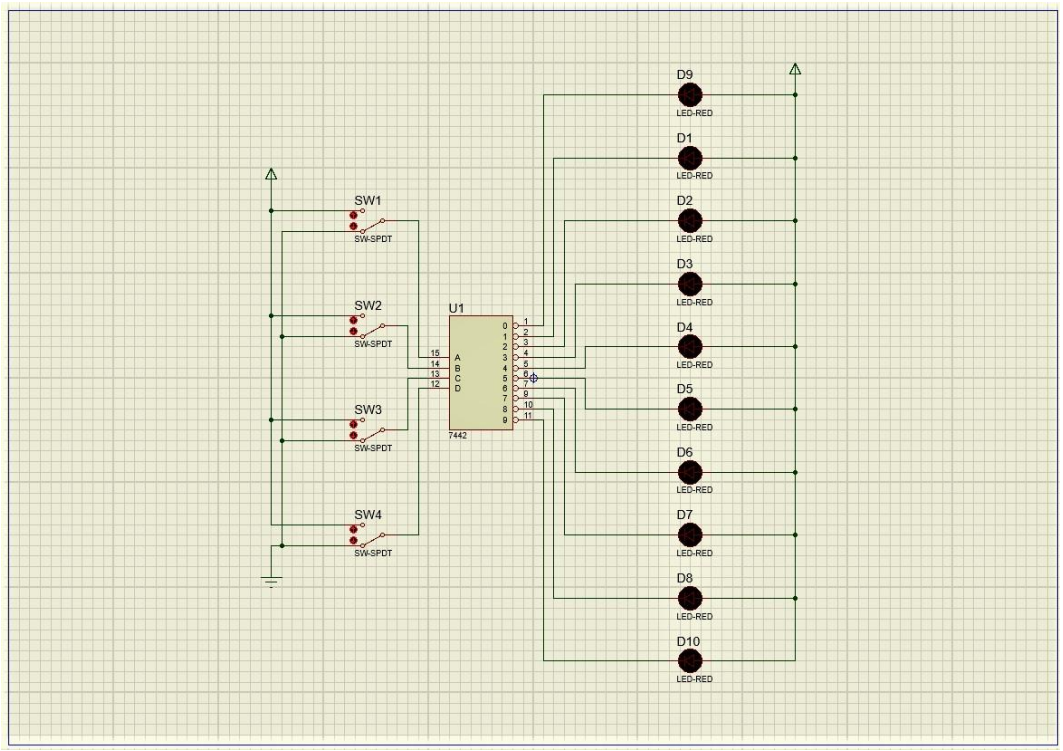
1. Column table

Input		**Output LED**			
SW1	**SW2**	**D1**	**D2**	**D3**	**D4**
0	0	1	1	1	0
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	1	1	1

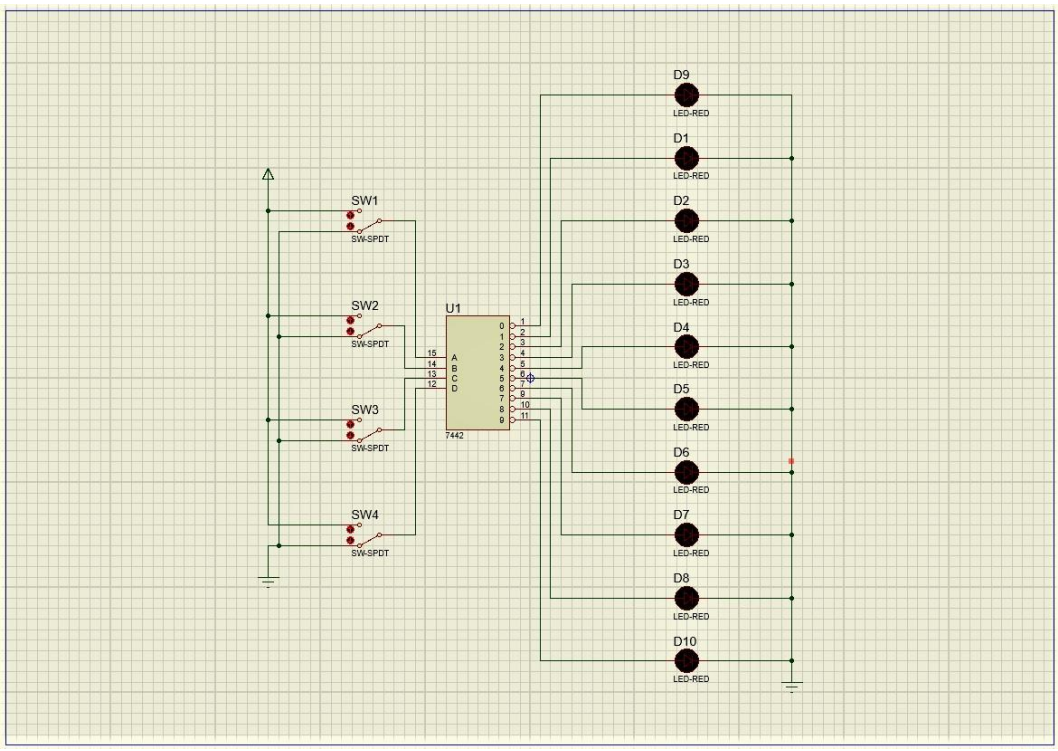
2. Output result from the logic gate combination
    a. D1 = SW1 . SW2
    b. D2 = $\overline{SW1}$. SW2
    c. D3 = SW1 . $\overline{SW2}$
    d. D4 = $\overline{SW1}$. $\overline{SW2}$
3. Conclusion from experiment 2 and 3

in the second experiment there is a NOT gate located after the NAND gate, while in the third experiment there is no NOT gate located after the NAND gate. so the output results in experiments 2 and 3 are very different

Experiment 4



Picture 4.1. Common anode LED circuit



Picture 4.2. Common cathode LED circuit

1. Column table

a. Common anode LED

Input				Output									
SW 1	**SW 2**	**SW 3**	**SW 4**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**1 0**
0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	1	0	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
0	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0

0	1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

b. Common cathode LED

Input				**Output**									
SW 1	**SW 2**	**SW 3**	**SW 4**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**1 0**
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1