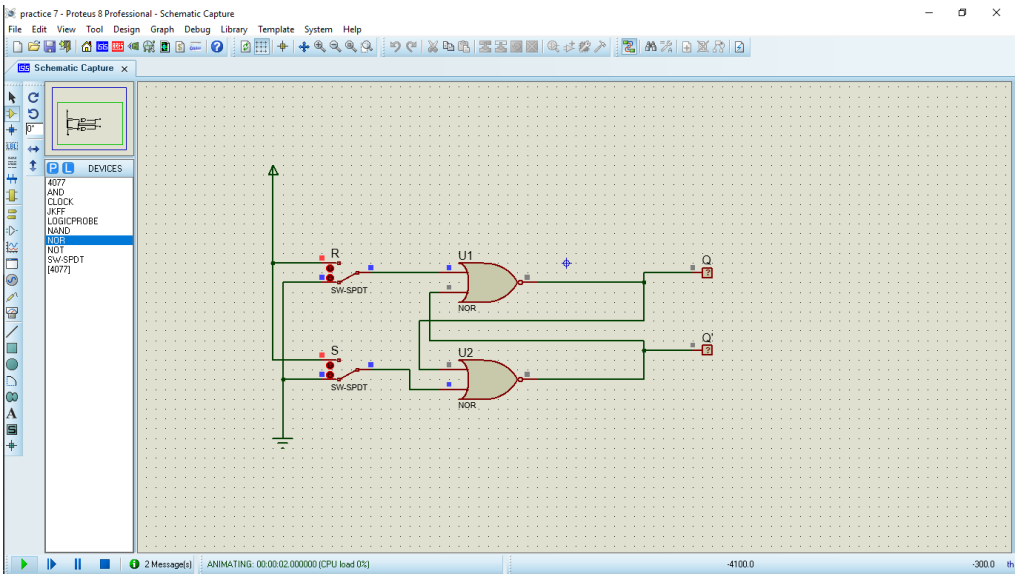
Name : Kemas Muhamad Kevin
Nim : L200184033

Test 1. **NOR Latch**

1. Make and simulation this NOR Latch.



2. Based on your simulation.

	S (Set)	R (Reset)	OutPut	
			Q	Q’
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

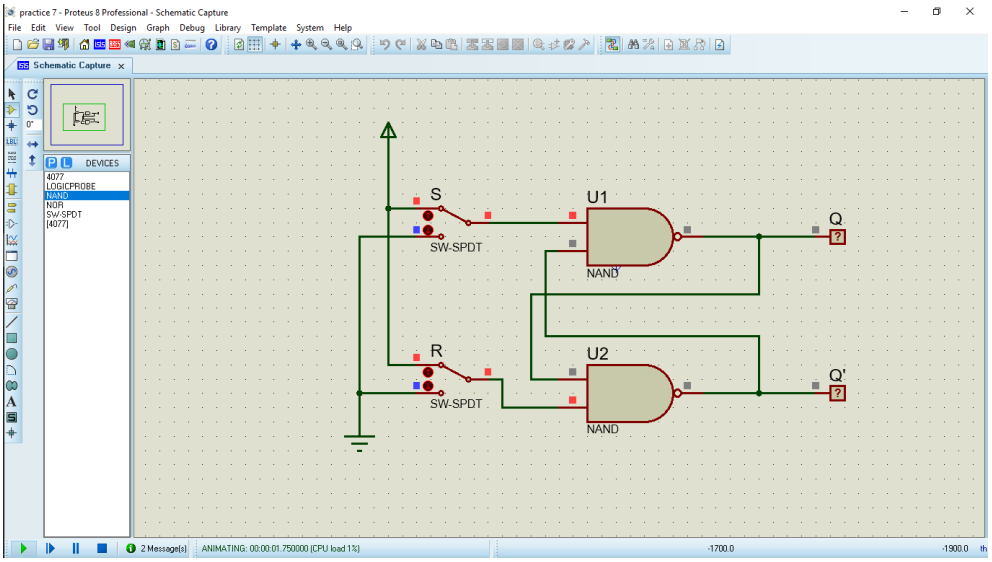
3. Answer the question.
   a. What will happen if we give the condition S = R = 0 !

      The result of Q and Q’ would be detected or constan.

   b. Why isn’t the condition S = R = 1 used !
      Because it can break the comparison q = qnot.

Test 2. **NAND Latch**

1. Make and simulation this NAND Latch.



2. Based on your simulation.

	S (Set)	R (Reset)	OutPut	
			Q	Q’
1	0	1	1	0
2	1	1	1	0
3	1	0	1	0
4	1	1	0	1
5	0	0	1	1

3. Answer the question.
   a. What will happen if we give the condition S = R = 0 !

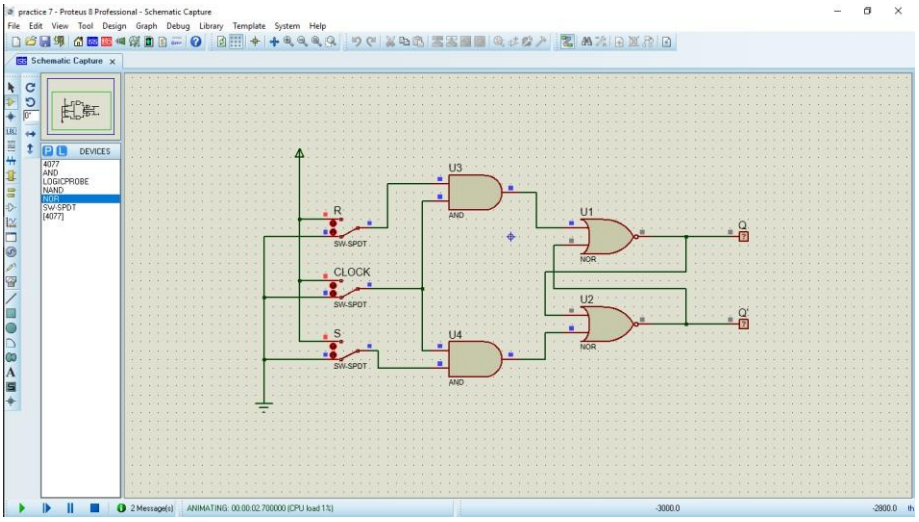
      The result of Q and Q’ will different.

   b. Why isn’t the condition S = R = 0 used !
      Because it gives the same output.

4. Based on analysis circuit at flip-flop. What is your opinion about “flip-flop and latch is used by storage element” :
   If S = 1, R = 0. so the result of Q will follow input S although has been changed to zero.

Test 3. **Flip-flop RS**

1. Make and simulation this Flip-flop RS.



2. Based on your simulation.

	S (Set)	R (Reset)	CLOCK	OutPut	
				Q	Q’
1	0	0	0	-	-
2	0	0	1	-	-
3	0	1	0	-	-
4	0	1	1	0	1
5	1	0	0	-	-
6	1	0	1	1	0
7	1	1	0	-	-
8	1	1	1	0	0

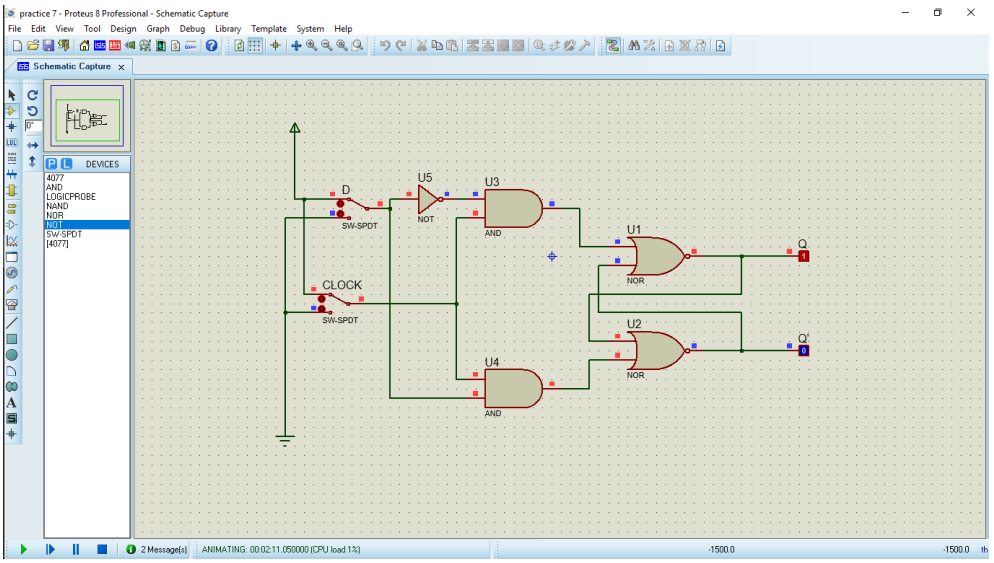
3. Answer the question.
   a. What will happen if we give the condition S = R = 1 and clock change from 1 to 0 !

      The result will be zero.

   b. How that condition can be ?
      Because the clock is zero, so if which one between S or R is changed the input, the output will be same.
4. Explain “How does Flip flop RS ” !
   Flip-flop RS does if the clock input is 1 and R or S is 1

Test 4. **Flip-flop D**

1. Make and simulation this Flip-flop RS.



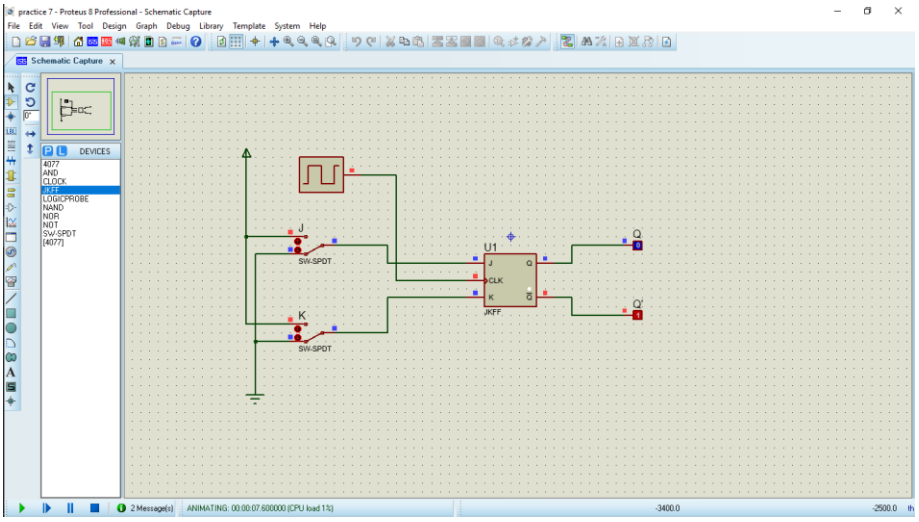
2. Based on your simulation.

	D	CLOCK	OutPut	
			Q	Q’
1	0	0	-	-
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

3. Explain how flip-flop D can does !
   If clock is used to store / lock the previous output condition.
4. What is the function of NOT gate of Flip-flop D compared Flip-Flop RS !
   In this case has 2 condition. On U3 has value is NOT D while U4 has value is D, so the result both of them will different result.

Test 5. **Flip-flop JK**

1. Make and simulation this Flip-flop RS.



2. Based on your simulation.

	J	K	CLOCK	OutPut	
				Q	Q’
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	1	0
7	1	1	0	0	1
8	1	1	1	0	1

3. Answer the question.
   a. What will happen if we give the condition J = K = 0 and clock rise up (change from 1 to 0) ?

      Clock will save the previous output condition.

   b. What will happen if J = K = 1, clock rise up ?
      The flip-flop can be adjusted or reset.

4. Explain “How does Flip flop JK ” !
   J & K are control input that determine what ever the flip-flop is going to do when receiving increased clock pulse.