DIGITAL SYSTEM

PRACTICUM REPORT 9 : DECODER

NIM : L200184040

NAME : AQSHAL FATWA IBRAHIM

INFORMATION TECHNOLOGY

FACULTY OF COMMUNICATION AND INFORMATICS

MUHAMMADIYAH UNIVERSITY OF SURAKARTA

2019

NIM

NAME : **L200184040**

CLASS : **AQSHAL FATWA IBRAHIM**

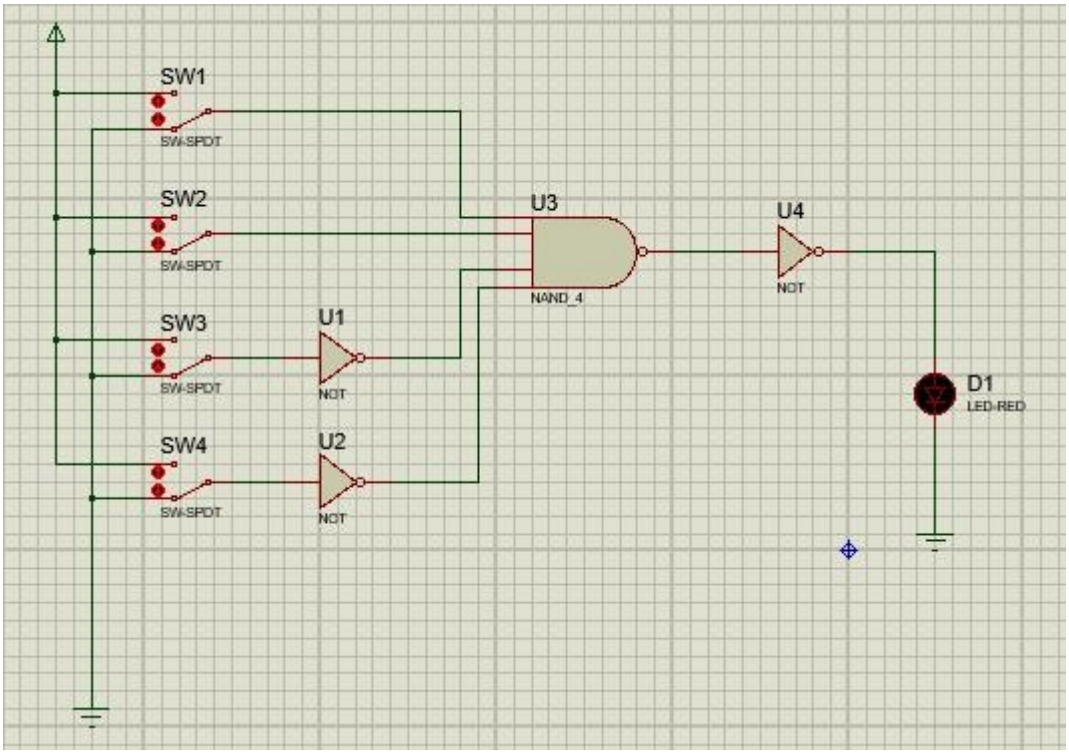
ASSISTANT : **X**

: **SALSA SASMITA MUKTI**

DATE OF PRACTICUM : **Friday, May 17th 2019**

exercise 1

a) Make a simple decoder



b) Truth table

A	B	C	D	F
0	0	0	0	**0**
1	0	0	0	**0**
0	1	0	0	**0**
1	1	0	0	**1**

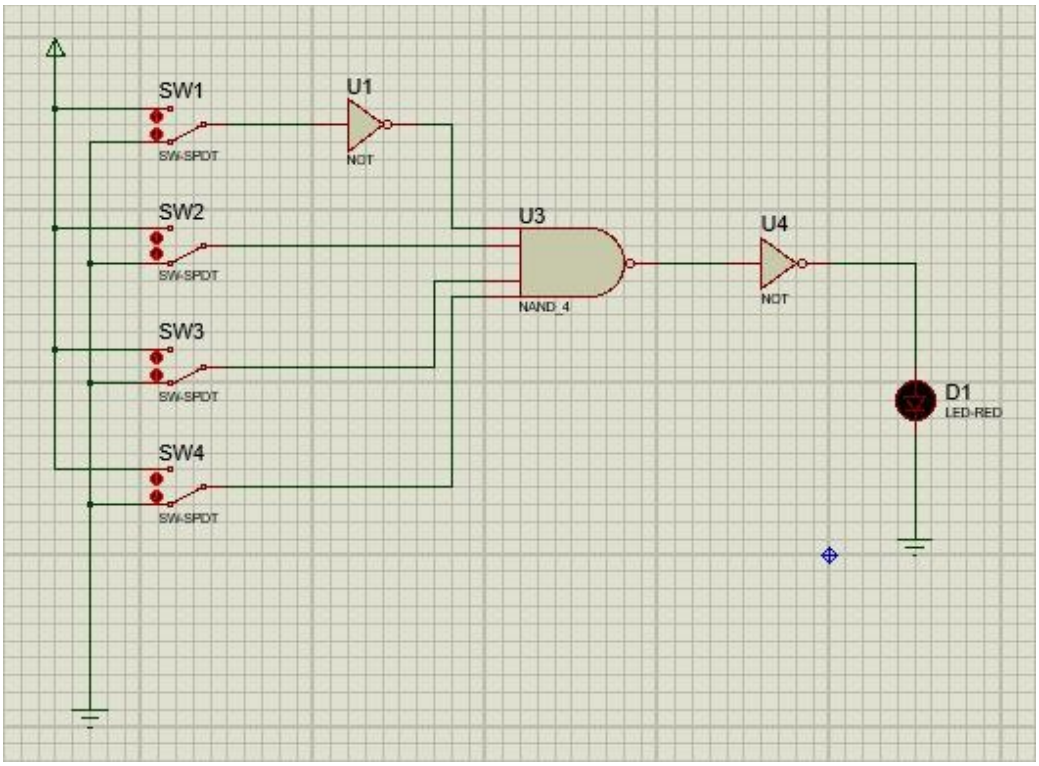
0	0	1	0	**0**
1	0	1	0	**0**
0	1	1	0	**0**
1	1	1	0	**0**
0	0	0	1	**0**
1	0	0	1	**0**
0	1	0	1	**0**
1	1	0	1	**0**
0	0	1	1	**0**
1	0	1	1	**0**
0	1	1	1	**0**
1	1	1	1	**0**

c) Decoder (F) just working (ON) when : <u>A = 1</u> <u>B = 1 C = 0 D = 0</u>

d) Decoder that have

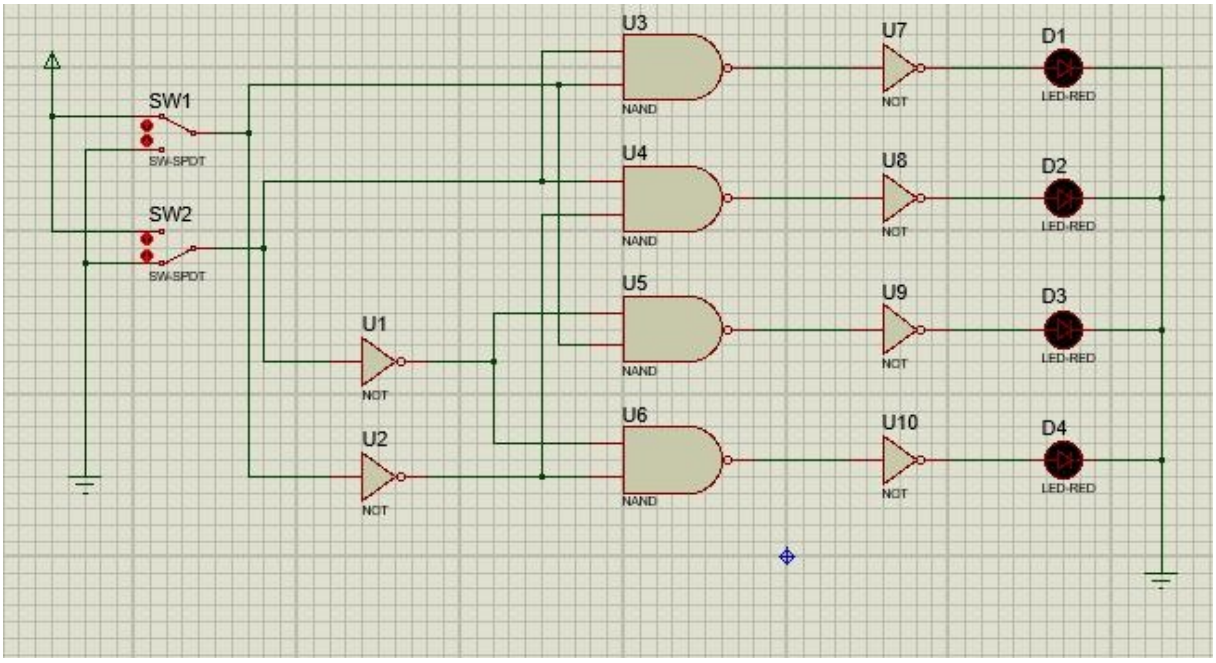
output F = 1

A = 0 B = 1 C = 1 D = 1 (F = A'BCD)



 # exercise 2

a) Make a combination of logic gate



b) Truth table

Input		Output LED			
SW1	**SW2**	**D1**	**D2**	**D3**	**D4**
0	**0**	**0**	**0**	**0**	**1**
0	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**0**
1	**1**	**1**	**0**	**0**	**0**

c) Each diode (LED) shows the output of a combination

circuit : D1 = ***SW1 . SW2***

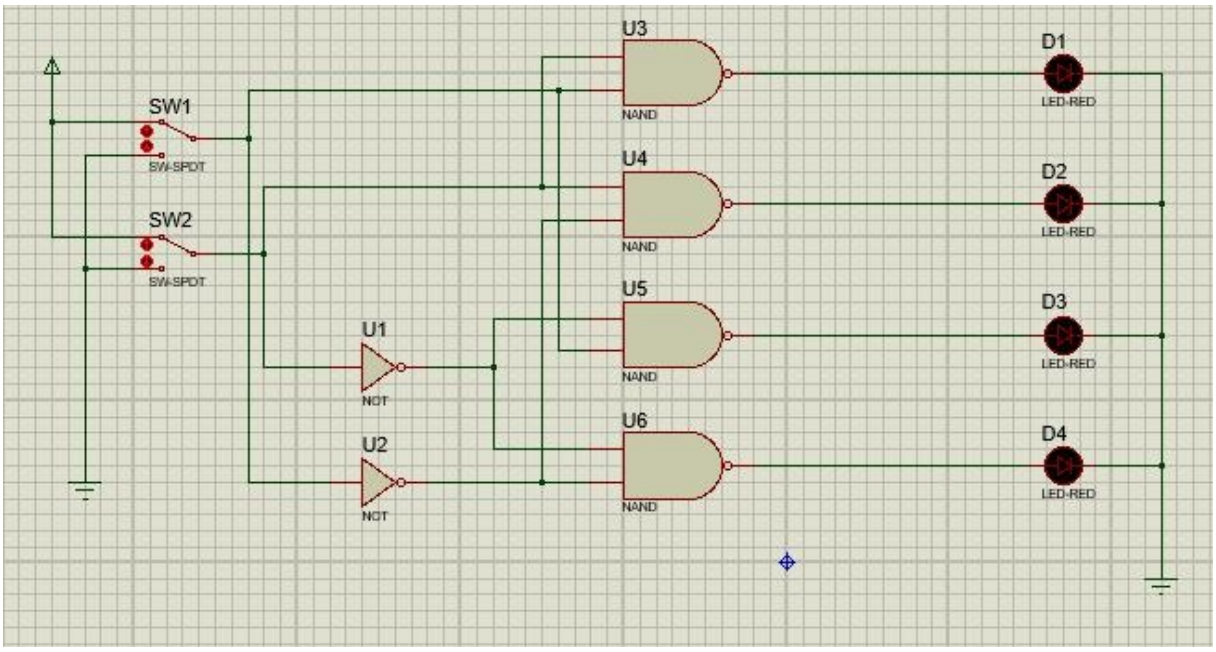
D2 = *SW1 . SW2*

D3 = *SW1 . SW2*

D4 = *SW1 . SW2*

 # exercise 3

a) Make a combination of logic gate



b) Truth table

Input		**Output LED**			
SW1	**SW2**	**D1**	**D2**	**D3**	**D4**
0	**0**	1	1	1	0
0	**1**	1	0	1	1
1	**0**	1	1	0	1
1	**1**	0	1	1	1

c) Each diode (LED) shows the output of a combination circuit :

D1 = ***SW1 . SW2***

D2 = *SW1 . SW2*

D3 = *SW1 . SW2*

D4 = *SW1 . SW2*

d) Conclusion

- Exercise 2 use AND gate
- Exercise 3 use NAND gate

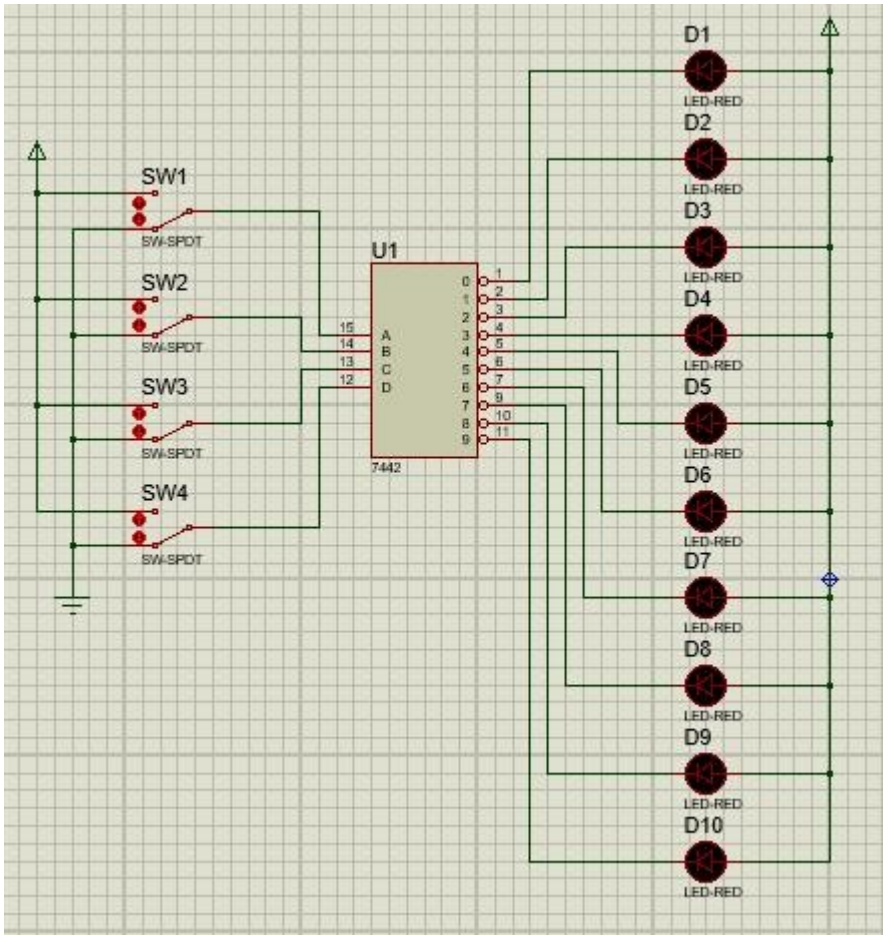
- **NOT** affects the output of the LED.

  the output of the LED using **NOT** will be inversely proportional to the output of the LED that does not use **NOT**

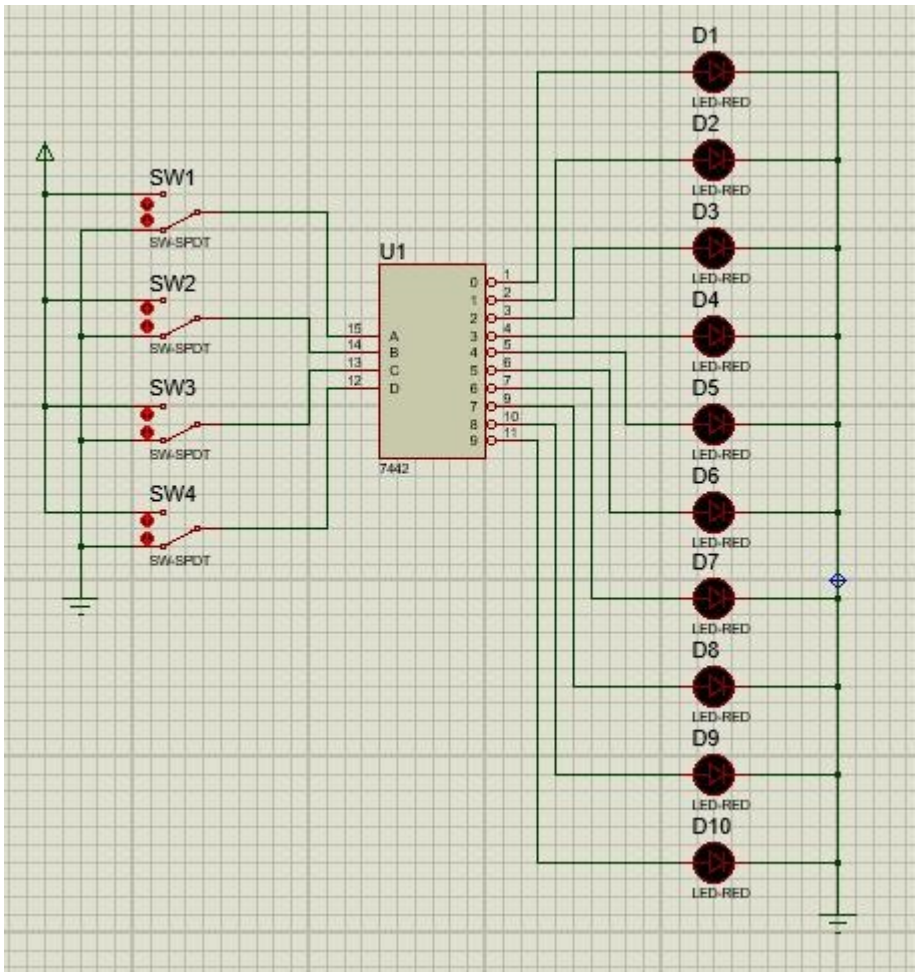
exercise 4

a) Circuit

- **Anode LED circuit**



- **Cathode LED circuit**



b) Truth table

- **Anode LED circuit**

Input				Output									
SW4	**SW3**	**SW2**	**SW1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	**0**	**0**	**0**	1	0	0	0	0	0	0	0	0	0
0	**0**	**0**	**1**	0	1	0	0	0	0	0	0	0	0
0	**0**	**1**	**0**	0	0	1	0	0	0	0	0	0	0
0	**0**	**1**	**1**	0	0	0	1	0	0	0	0	0	0
0	**1**	**0**	**0**	0	0	0	0	1	0	0	0	0	0
0	**1**	**0**	**1**	0	0	0	0	0	1	0	0	0	0
0	**1**	**1**	**0**	0	0	0	0	0	0	1	0	0	0
0	**1**	**1**	**1**	0	0	0	0	0	0	0	1	0	0

1	**0**	**0**	**0**	0	0	0	0	0	0	0	0	1	0
1	**0**	**0**	**1**	0	0	0	0	0	0	0	0	0	1
1	**0**	**1**	**0**	0	0	0	0	0	0	0	0	0	0
1	**0**	**1**	**1**	0	0	0	0	0	0	0	0	0	0
1	**1**	**0**	**0**	0	0	0	0	0	0	0	0	0	0
1	**1**	**0**	**1**	0	0	0	0	0	0	0	0	0	0
1	**1**	**1**	**0**	0	0	0	0	0	0	0	0	0	0
1	**1**	**1**	**1**	0	0	0	0	0	0	0	0	0	0

- **Cathode LED circuit**

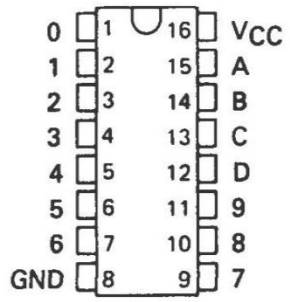
Input				**Output**									
SW4	**SW3**	**SW2**	**SW1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	**0**	**0**	**0**	0	1	1	1	1	1	1	1	1	1
0	**0**	**0**	**1**	1	0	1	1	1	1	1	1	1	1
0	**0**	**1**	**0**	1	1	0	1	1	1	1	1	1	1
0	**0**	**1**	**1**	1	1	1	0	1	1	1	1	1	1
0	**1**	**0**	**0**	1	1	1	1	0	1	1	1	1	1
0	**1**	**0**	**1**	1	1	1	1	1	0	1	1	1	1
0	**1**	**1**	**0**	1	1	1	1	1	1	0	1	1	1
0	**1**	**1**	**1**	1	1	1	1	1	1	1	0	1	1
1	**0**	**0**	**0**	1	1	1	1	1	1	1	1	0	1
1	**0**	**0**	**1**	1	1	1	1	1	1	1	1	1	0
1	**0**	**1**	**0**	1	1	1	1	1	1	1	1	1	1
1	**0**	**1**	**1**	1	1	1	1	1	1	1	1	1	1
1	**1**	**0**	**0**	1	1	1	1	1	1	1	1	1	1
1	**1**	**0**	**1**	1	1	1	1	1	1	1	1	1	1
1	**1**	**1**	**0**	1	1	1	1	1	1	1	1	1	1
1	**1**	**1**	**1**	1	1	1	1	1	1	1	1	1	1

 # additional assignment

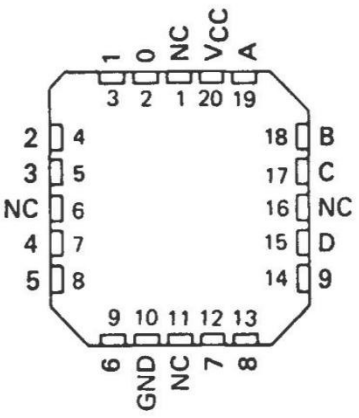
- **All Outputs Are High for Invalid Input Conditions**
- **Also for Application as**
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- **Diode-Clamped Inputs**

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A	140 mW	17 ns
'LS42	35 mW	17 ns

SN5442A, SN54LS42 . . . J OR W PACKAGE
SN7442A . . . N PACKAGE
SN74LS42 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS42 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

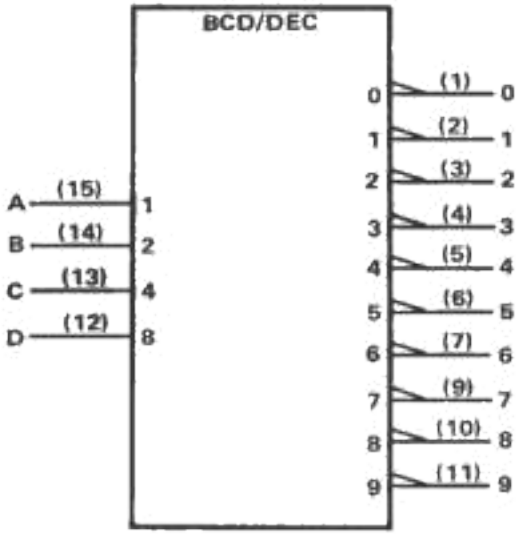
description

These monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'LS42 feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

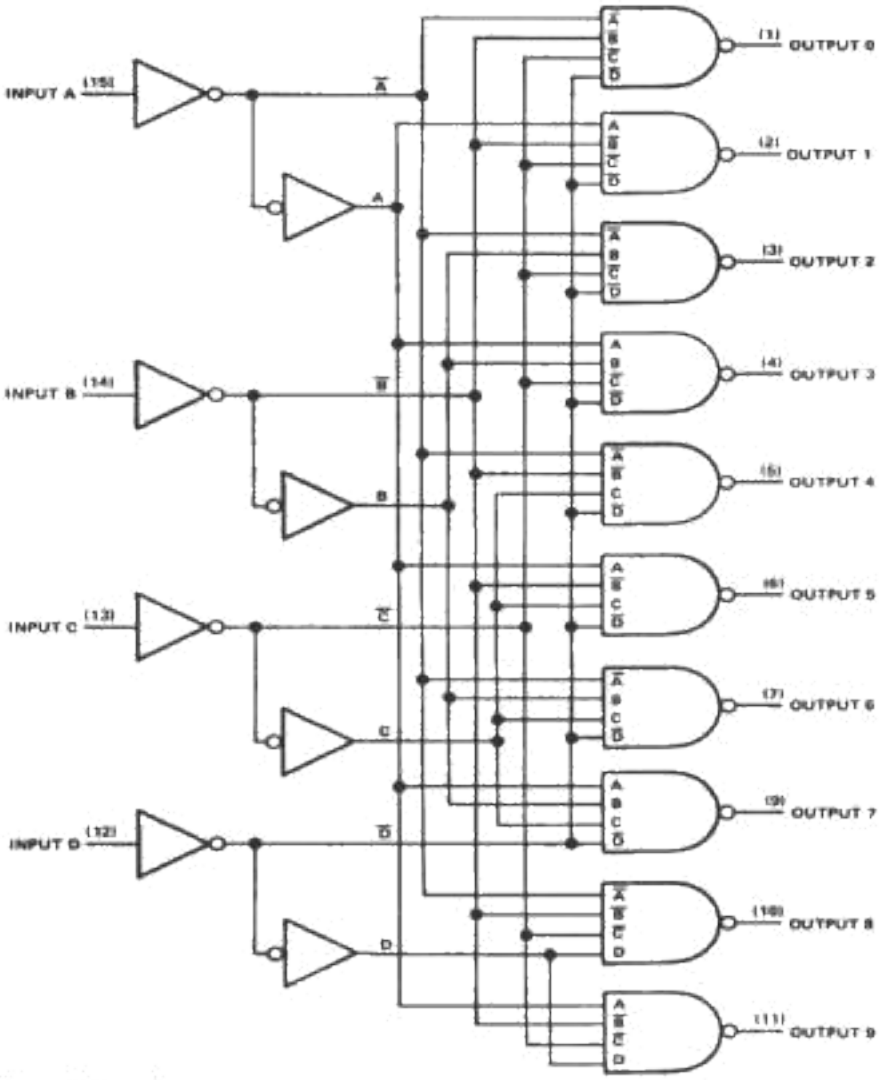
The SN5442A and SN54LS42 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7442A and SN74LS42 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

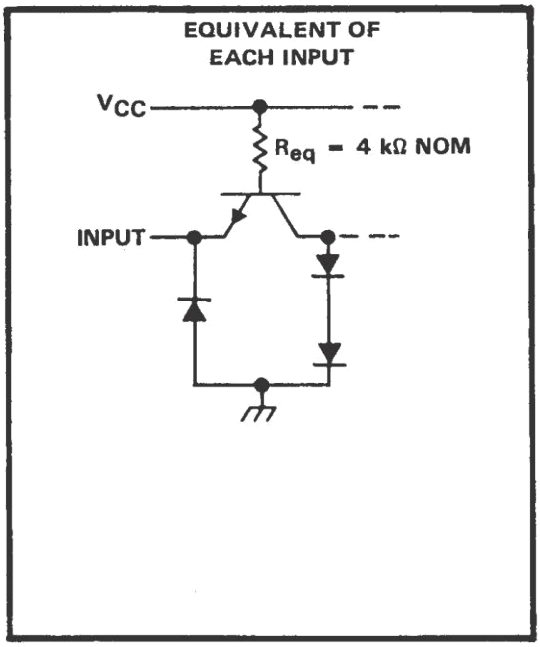
logic diagram (positive logic)



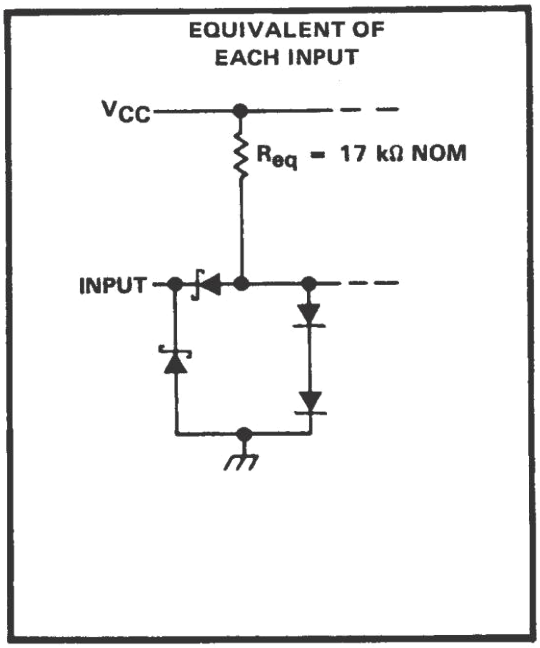
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

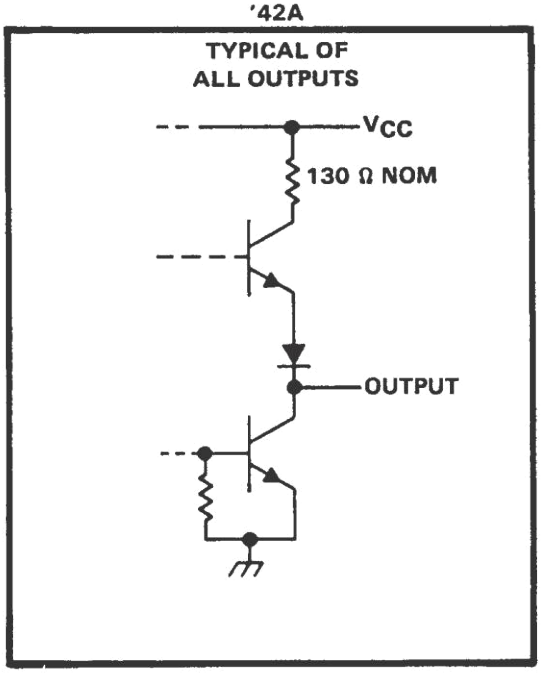
'42A



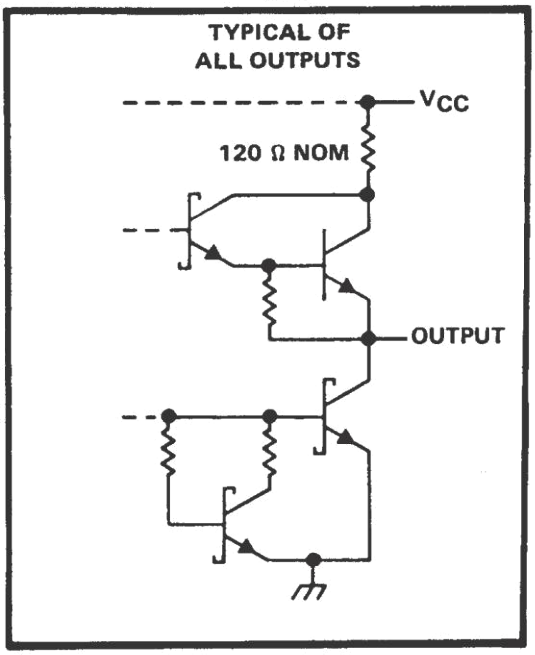
'LS42



'42A



'LS42



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '42A . . . . . 5.5 V
'LS42 . . . . . 7 V
Operating free-air temperature range: SN5442A, SN54LS42 . . . . . −55°C to 125°C
SN7442A, SN74LS42 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.