PRACTICAL REPORT

MODUL 3

DIGITAL SYSTEM

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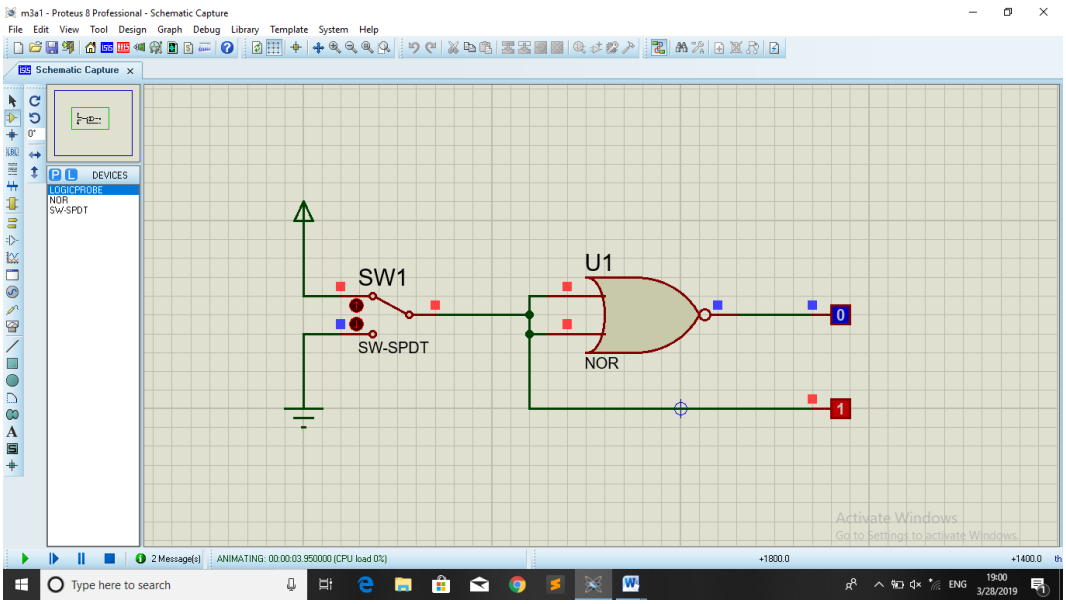
1. Trial 1: Substitution for Logic Gate Substitute

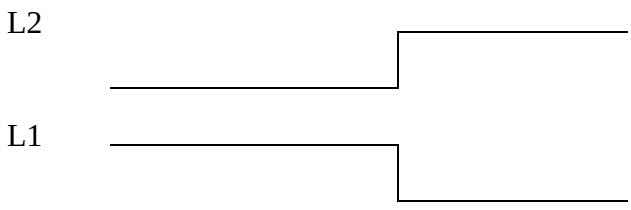
1. Make the circuit.



2. **L1 = NOT(L2 + L2) = L2**
3. Truth Table

SW1	L2	L1
0	0	1
1	1	0

4. Time Diagram

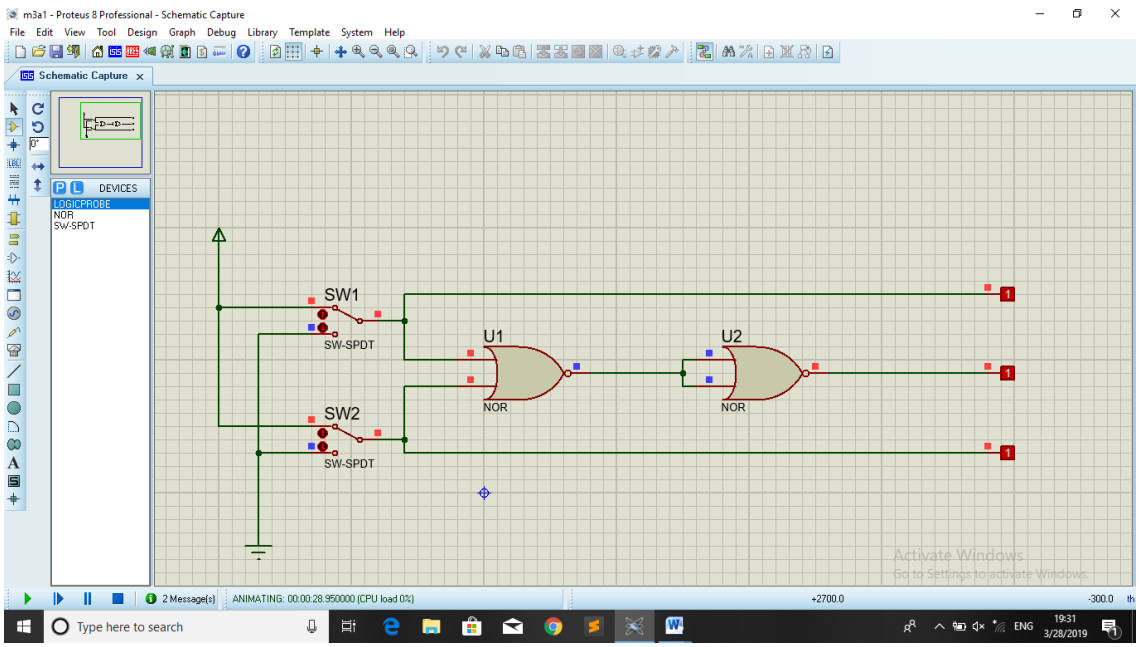


5. Conclusion:

   NOR gate in figure 4.3 form a logic from the **NOT** gate.

2. Trial 2: Substitution for Logic Gate Substitute

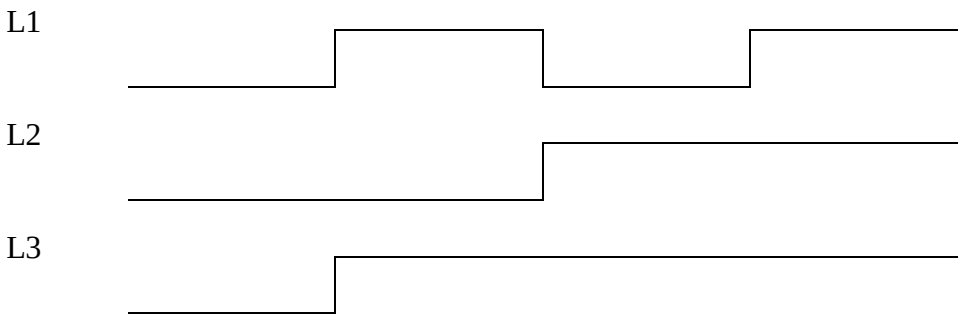
1. Make the circuit.



2. **L3 = NOT(NOT(L1+L2) = L1 + L2**
3. Truth Table

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	1

4. Time Diagram

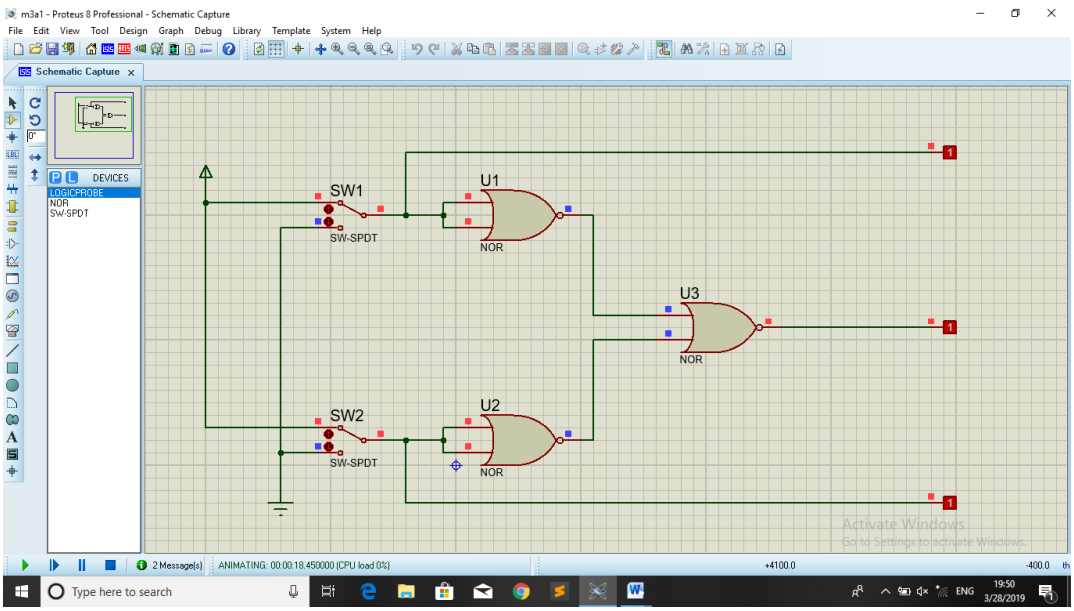


5. Conclusion:

   The NOR gate in figure 4.4 form a logic from the **OR** gate.

3. Trial 3: Substitution for Logic Gate Substitute

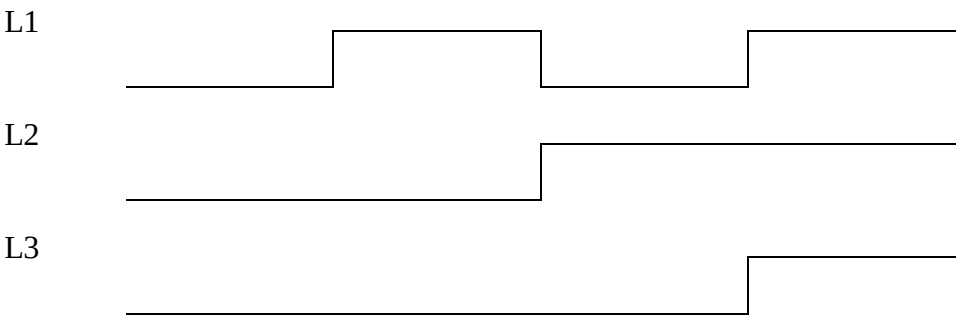
1. Make the circuit



2. **L3 = NOT(NOT(L1) + NOT(L2)) = L1 L2**
3. Truth Table

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	0
0	1	0	1	0
1	1	1	1	1

4. Time Diagram

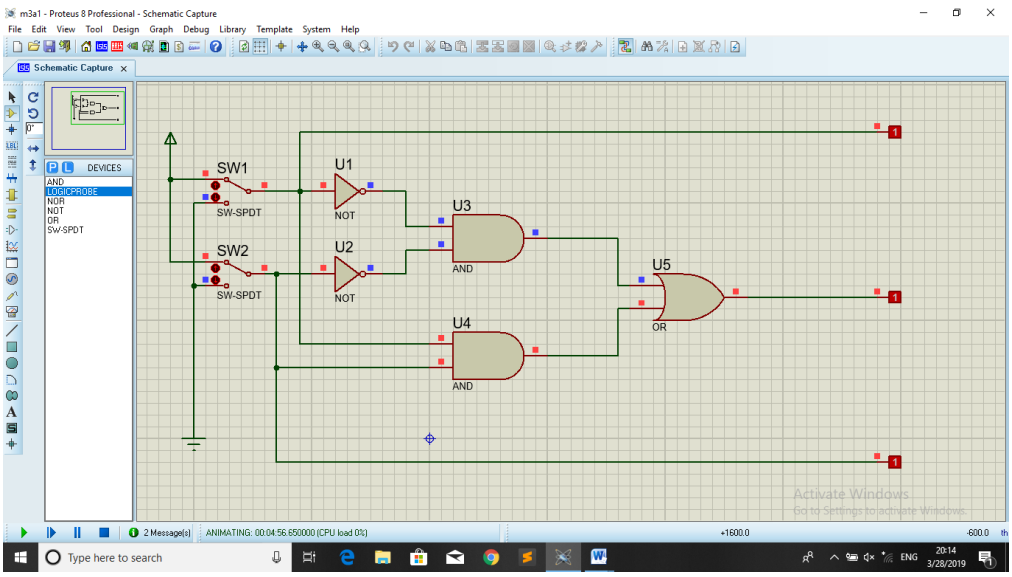


5. Conclusion

   The NOR gate in figure 4.5 form a logic from the **AND** gate.

4. Trial 4: Substitution for Logic Gate Substitute.

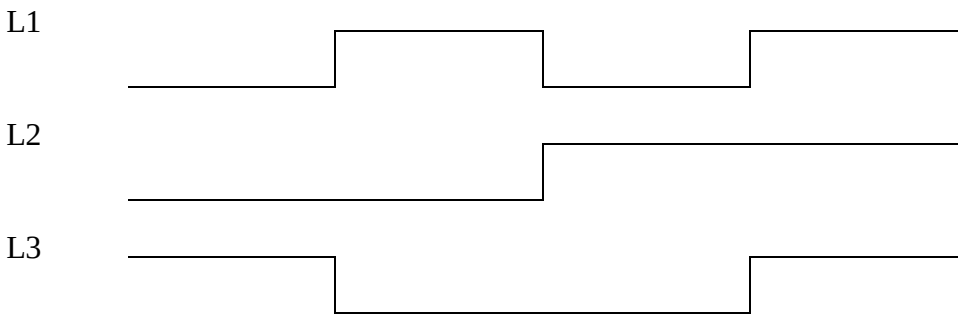
1. Make the circuit.



2. **L3 = NOT(*L*1*L*2) + L1 + L2 = NOT(L1 XOR L2)**
3. Truth Table

SW1	SW2	L1	L2	L3
0	0	0	0	1
1	0	1	0	0
0	1	0	1	0
1	1	1	1	1

4. Time Diagram

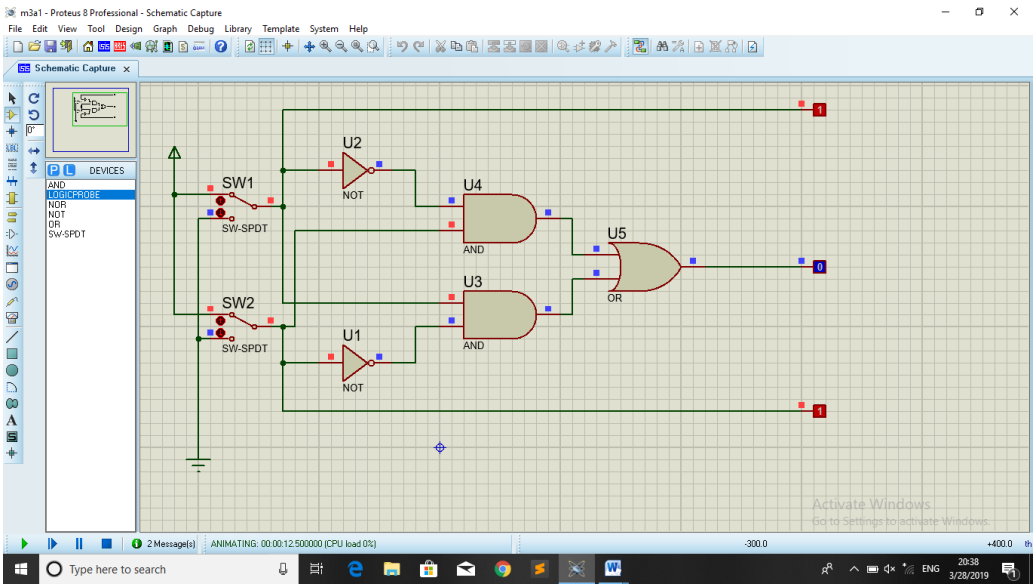


5. Conclusion

   The NOR gate in figure 4.5 form a logic from the **XNOR** gate.

5. Trial 5: Designing Boolean function to the circuit

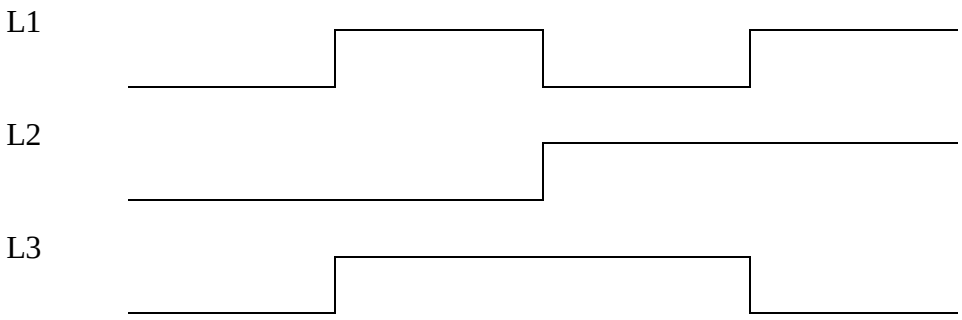
1. Make the circuit



2. **L3 = NOT(L1) L2 + L1 NOT(L2)**
3. Truth Table

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	0

4. Time Diagram



5. Conclusion

   The NOR gate in figure 4.5 form a logic from the **XOR** gate.