DIGITAL SYSTEMS

PRACTICUM 3

By:

GANNO TRIBUANA KURNIAJI

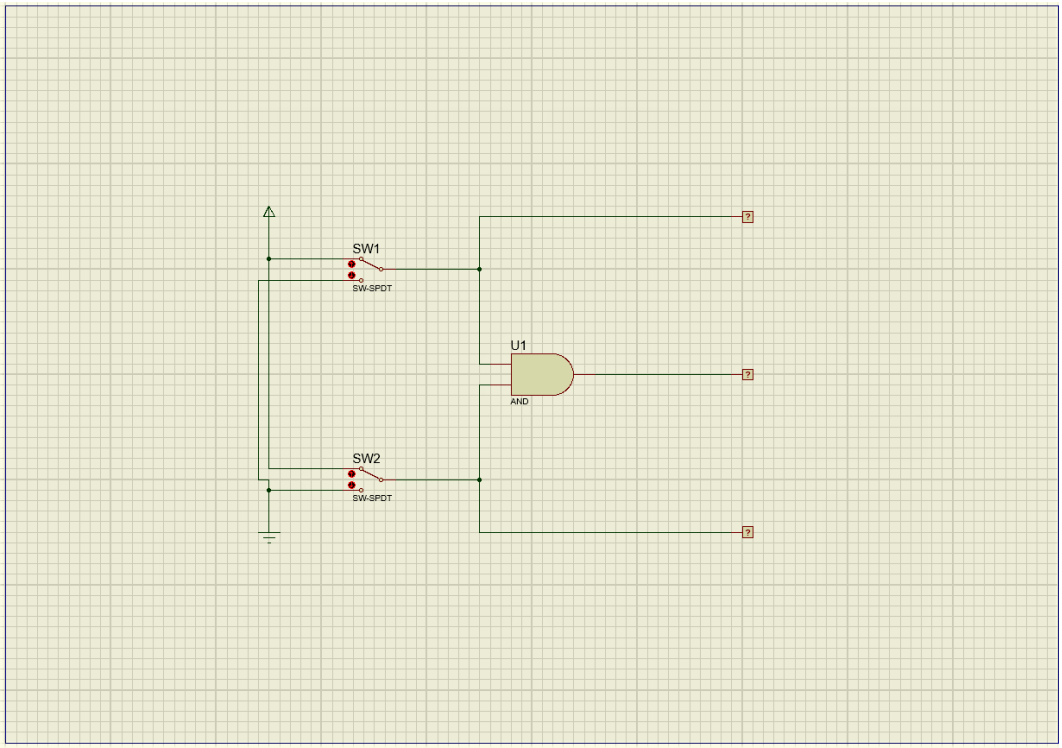
NIM: L200184092

INFORMATION TECHNOLOGY

FACULTY OF COMMUNICATION AND INFORMATICS

UNIVERSITY OF MUHAMMADIYAH SURAKARTA

Experiment 1. AND Gate



Picture 1.1. AND Gate

1. Truth table

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	0
0	1	0	1	0
1	1	1	1	1

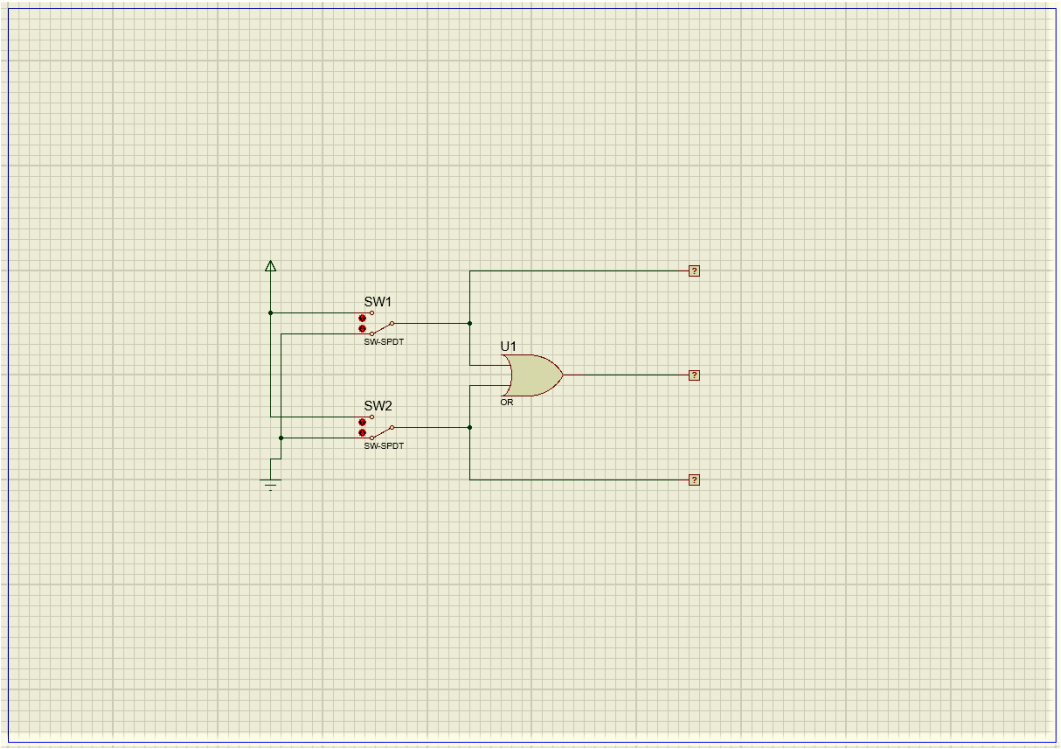
2. Time diagram

L1

L2

L3

Experiment 2. OR Gate



Picture 2.1. OR Gate

1. Truth table

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	1

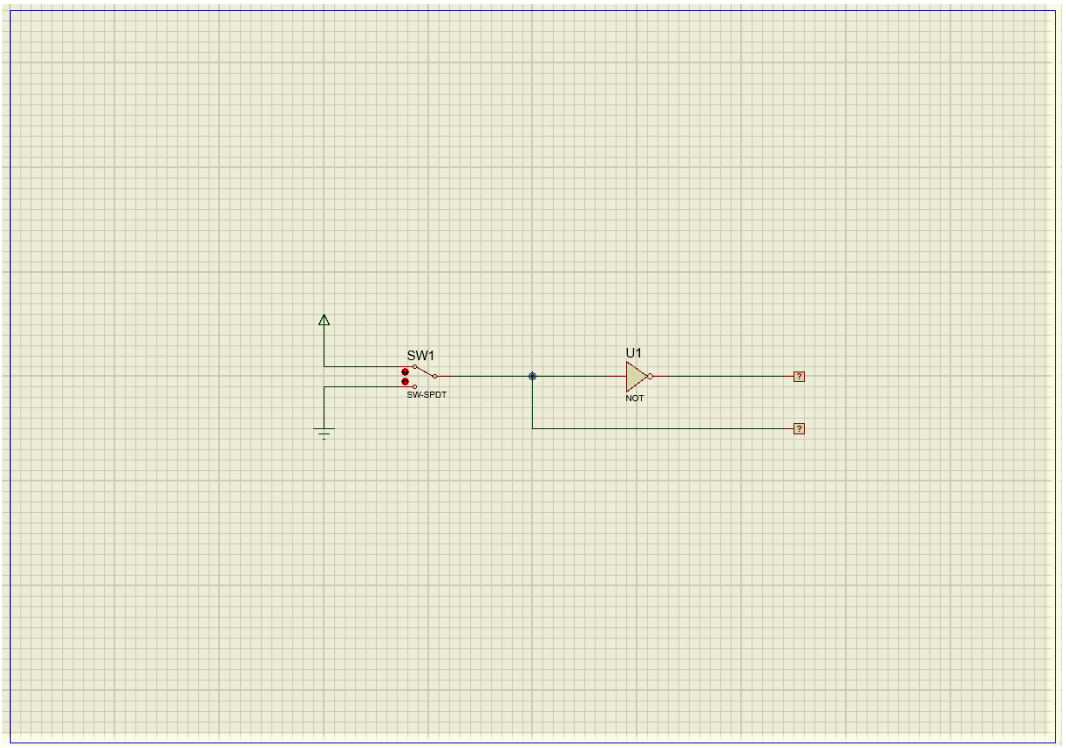
2. Time diagram

L1

L2

L3

Experiment 3. NOT Gate



Picture 3.1. NOT Gate

1. Truth table

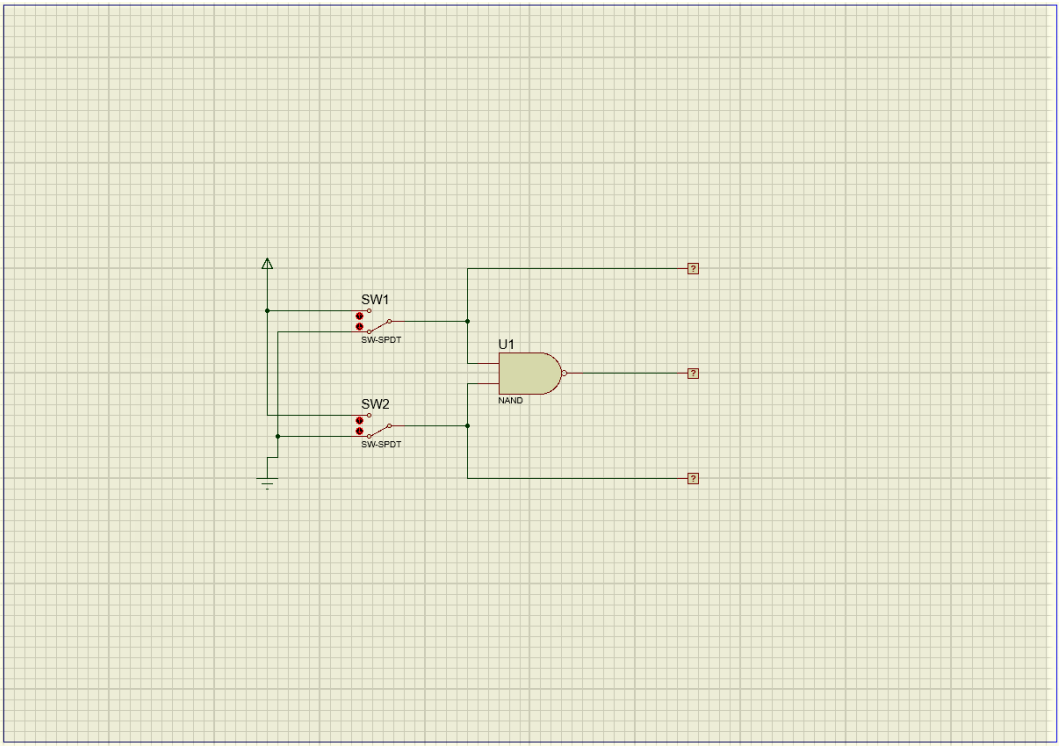
SW1	L1	L2
0	1	0
1	0	1

2. Time diagram

L1

L2

Experiment 4. NAND Gate



Picture 4.1. NAND Gate

1. Truth table

SW1	SW2	L1	L2	L3
0	0	0	1	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	0

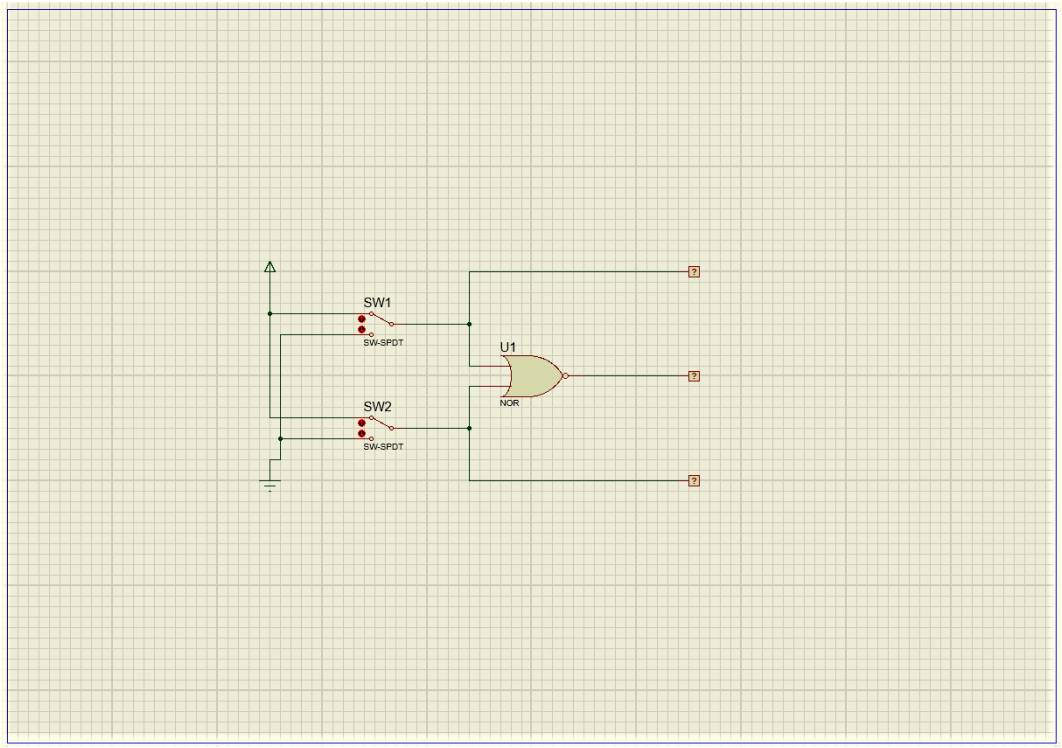
2. Time diagram

L1

L2

L3

Experiment 5. NOR Gate



Picture 5.1. NOR Gate

1. Truth table

SW1	SW2	L1	L2	L3
0	0	0	0	1
1	0	1	0	0
0	1	0	1	0
1	1	1	1	0

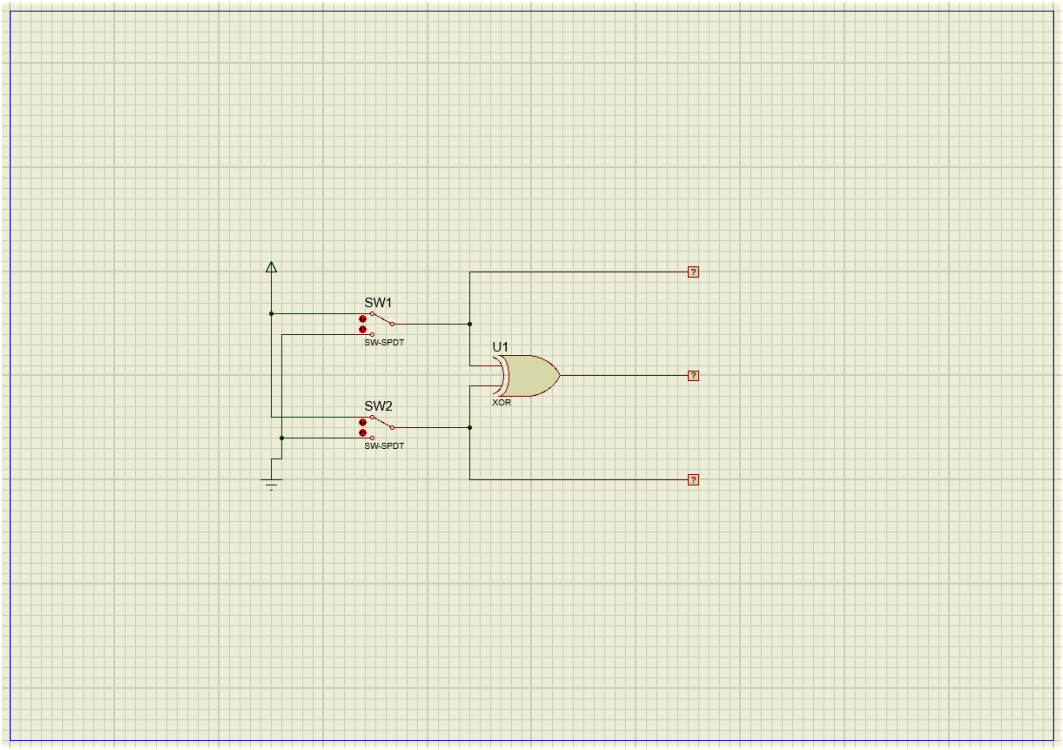
2. Time diagram

L1

L2

L3

Experiment 6. XOR Gate



Picture 6.1. XOR Gate

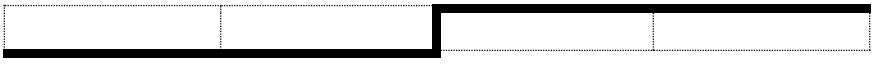
1. Truth Table

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	0

2. Time Diagram

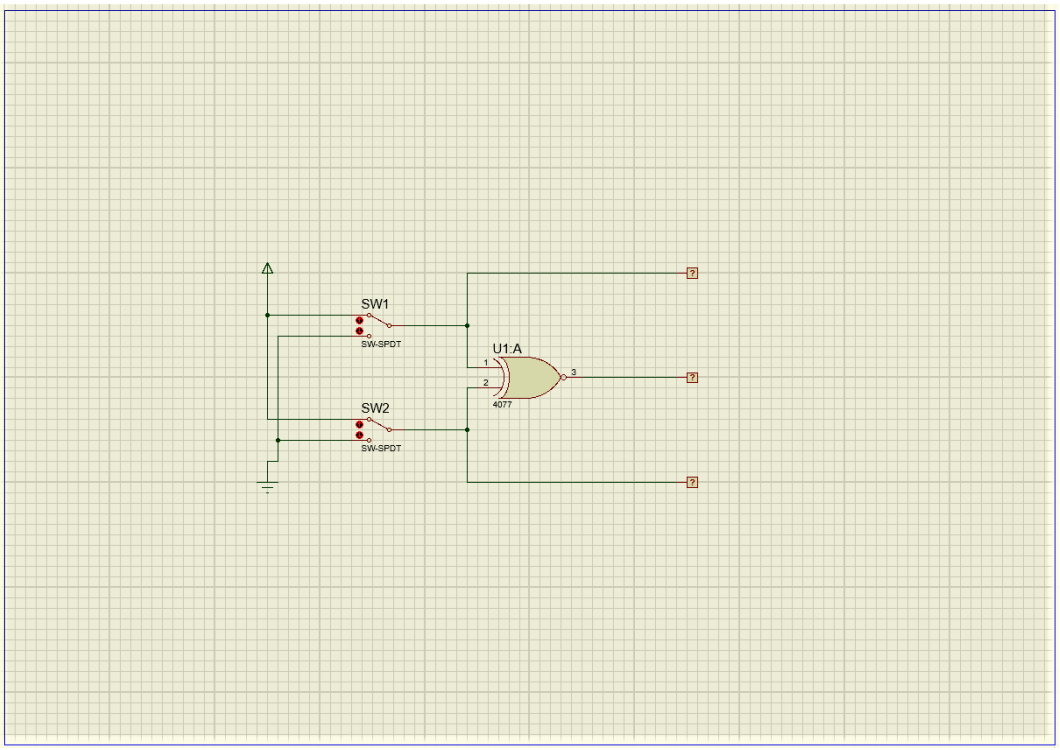
L1

L2



L3

Experiment 7. XNOR Gate



Picture 7.1. XNOR Gate

1. Truth Table

SW1	SW2	L1	L2	L3
0	0	0	0	1
1	0	1	0	0
0	1	0	1	0
1	1	1	1	1

2. Time Diagram

L1

L2

L3