

INFORMATION TECHNOLOGY
UNIVERSITY OF MUHAMMADIYAH SURAKARTA
DIGITAL SYSTEMS
12th PRACTICE



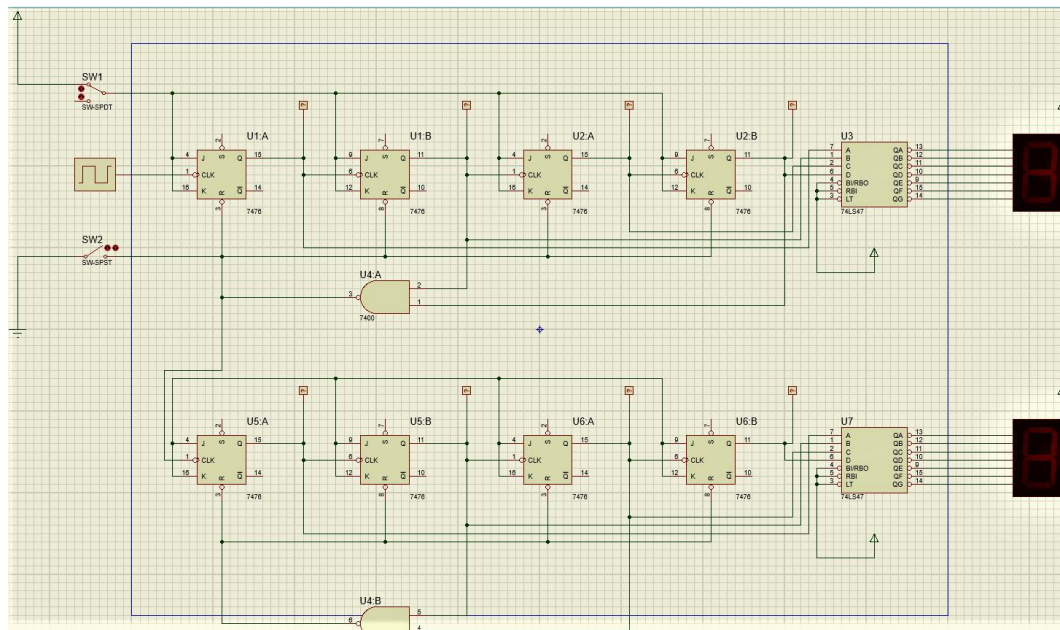
By:
SUFYAN HABIB ZAINI
NIM: L200184098

The circuit diagram illustrates a 4-bit counter implemented using four J-K flip-flops (U1 A, U1 B, U2 A, U2 B) and a 74LS47 decoder (U3). The counter is triggered by a square wave pulse from SW1. The output of the counter is connected to the inputs of the 74LS47 decoder, which drives a 7-segment display (U4 A) showing the decimal value of the counter's output. The 74LS47 decoder is configured with its active-low inputs (A, B, C, D) connected to the counter outputs and its active-low outputs (0-9) connected to the 7-segment display. The 74LS47 decoder is also connected to a 5V supply and ground.

1. What is the output seen in the seven segment?

Answer: The seven segment output is in the form of calculations from 1 to 9.

Experiment 2



Picture 2.1. Modulus 6 and Decoder circuit

1. What is the clock function in the series above?

Answer: To determine the speed of calculation.

2. Explain the usefulness of the SPDT Switch in the series above!

Answer: To check the value of the decoder.

3. Explain the usefulness of the SPST Switch in the series above!

4. Answer: To stop counting.