DIGITAL SYSTEM LABORATORY WORK

FLIP-FLOP APPLICATION

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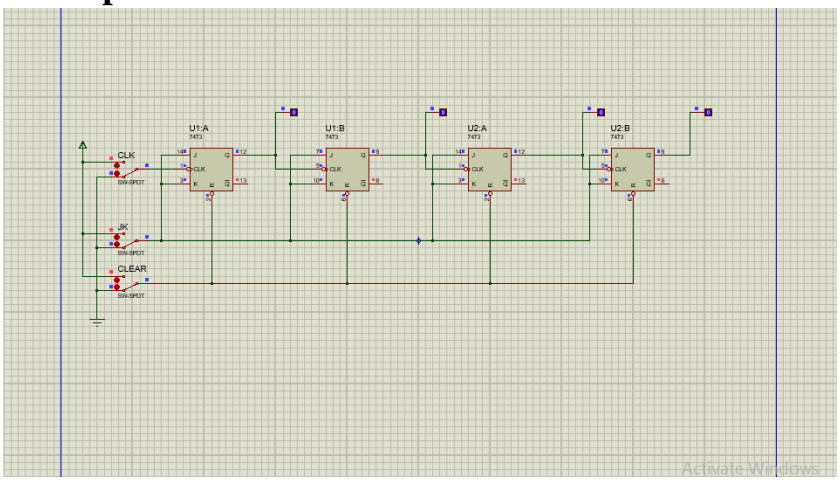
Attempt 1 : Make counter JK-FF

1. 

2. **Simulation the circuit**

	INPUT			OUTPUT			
	CLEAR	JK	CLK	A	B	C	D
1.	1	1	0	0	0	0	0
2.	1	1	1	0	0	0	0
3.	1	1	0	0	0	0	1
4.	1	1	1	0	0	0	1
5.	1	1	0	0	0	1	0
6.	1	1	1	0	0	1	0
7.	1	1	0	0	0	1	1
8.	1	1	1	0	0	1	1
9.	1	1	0	0	1	0	0
10.	1	1	1	0	1	0	0
11.	1	1	0	0	1	0	1
12.	1	1	1	0	1	0	1
13.	1	1	0	0	1	1	0
14.	1	1	1	0	1	1	0
15.	1	0	0	0	1	1	0
16.	1	0	1	0	1	1	0
17.	1	1	0	0	1	1	1

18.	1	1	1	0	1	1	1
19.	0	1	0	0	0	0	0
20.	0	1	1	0	0	0	0

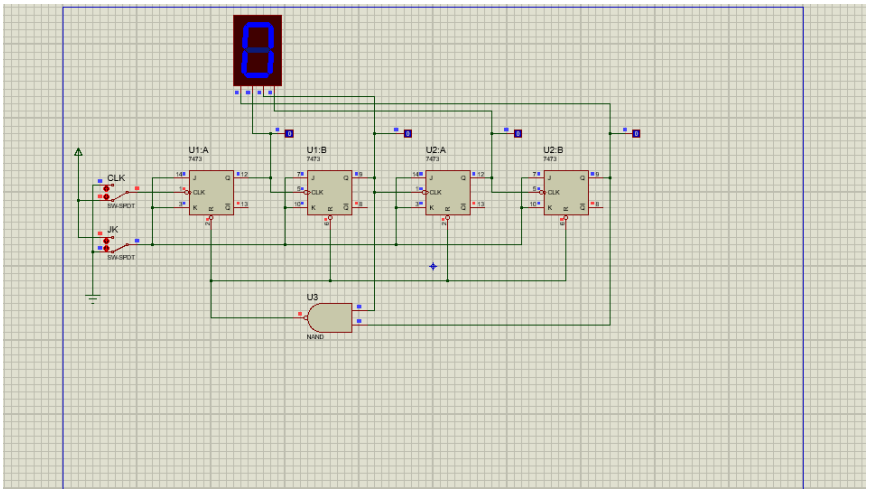
3. The Function

- Switch of CLK : Binary Saver
- Switch of JK : As a First counter
- Switch of CLEAR : To rearrage the condition of switch of JK

4. Inference

Output will be change if switch of CLK = 0, and output will be same if switch of JK = 0, and output not run or 0 if switch of CLEAR = 0

Attempt 2 : Counter MOD 10

1. 

2. Simulation the Circuit

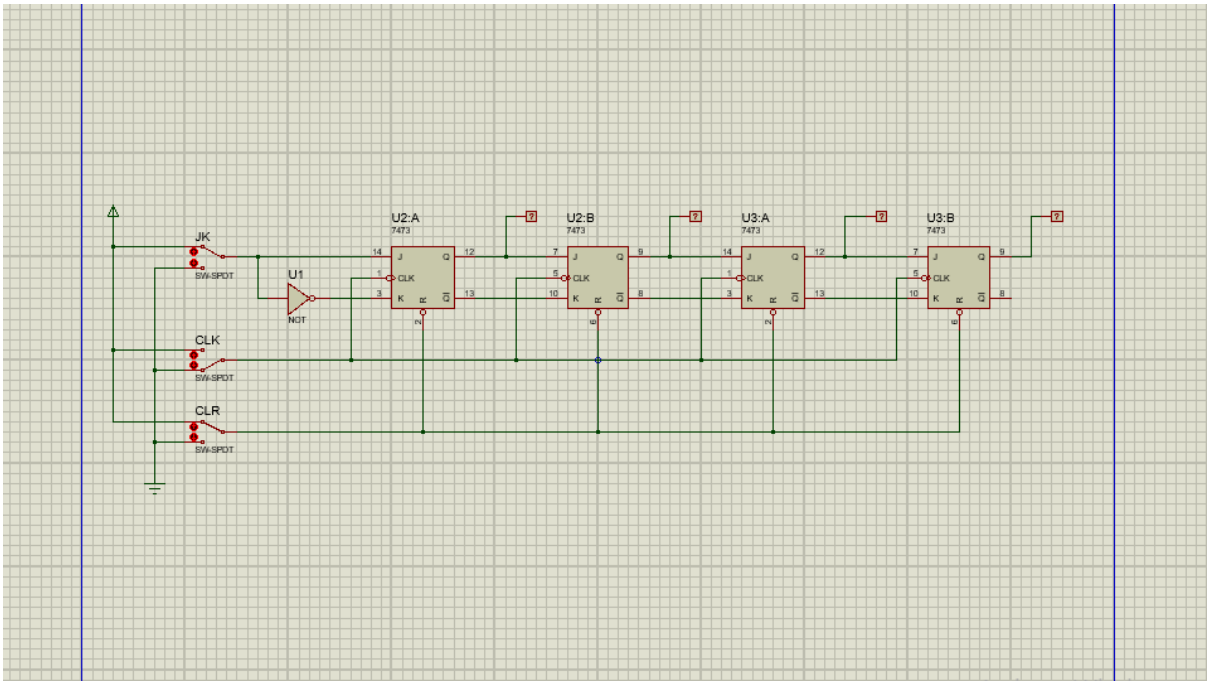
	INPUT		OUTPUT			
	JK	CLK	A	B	C	D
1.	1	0	0	0	0	0
2.	1	1	0	0	0	1
3.	1	0	0	0	0	1
4.	1	1	0	0	1	0
5.	1	0	0	0	1	0
6.	1	1	0	0	1	1
7.	1	0	0	0	1	1

8.	1	1	0	1	0	0
9.	1	0	0	1	0	0
10.	1	1	0	1	0	1
11.	1	0	0	1	0	1
12.	1	1	0	1	1	0
13.	1	0	0	1	1	0
14.	1	1	0	1	1	1
15.	1	0	0	1	1	1
16.	1	1	1	0	0	0
17.	1	0	1	0	0	0
18.	1	1	1	0	0	1
19.	1	0	1	0	0	1
20.	1	1	0	0	0	0
21.	0	0	0	0	0	0
22.	0	1	0	0	0	0
23.	1	0	0	0	0	0
24.	1	1	0	0	0	1

3. Inference

Output will be change if switch of JK and CLK is on or = 1

Attempt 3 : Make Register JK-FF

1. 

2. Simulation the switch

	CLR	JK	CLK	A	B	C	D
1.	0	X	-	0	0	0	0
2.	1	1	-	0	0	0	0
3.	1	1	*1*	0	0	0	1
4.	1	1	*2*	0	0	1	1
5.	1	1	*3*	0	1	1	1
6.	1	0	*4*	1	1	1	0
7.	1	0	*5*	1	1	0	0
8.	1	0	*6*	1	0	0	0
9.	1	0	*7*	0	0	0	0
10.	1	0	*8*	0	0	0	0
11.	1	1	*9*	0	0	0	1
12.	1	0	*10*	0	0	1	0
13.	1	0	*11*	0	1	0	0
14.	1	0	*12*	1	0	0	0
15.	1	0	*13*	0	0	0	0

3. Inference

if switch of CLEAR is off or 0, output cant be change. If switch of JK is on so output start from D and if off output start from A. And output can be change if switch of CLOCK is 0 or off