DIGITAL SYSTEM LABORATORY WORK

ASSIGMENT 2

By :

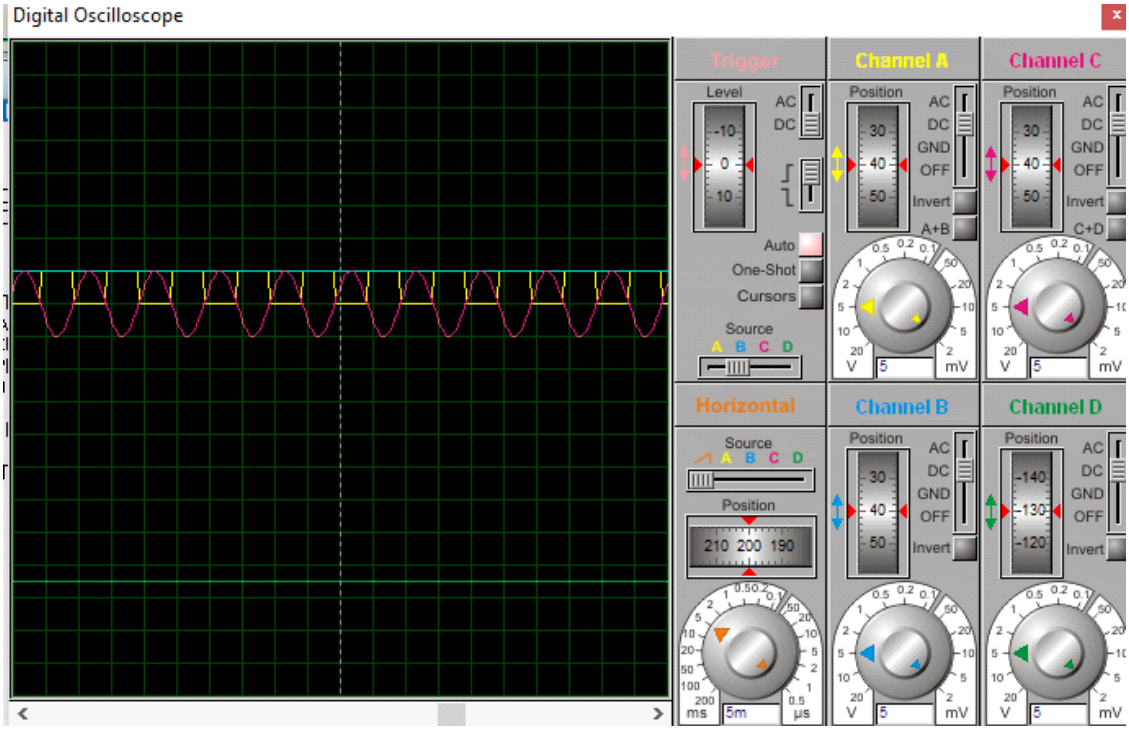
Nadhifah Chairunnisa

NIM : L200184137

INFORMATION TECHNOLOGY
FACULTY OF COMUNICATION AND INFORMATIC
MUHAMMADIYAH UNIVERSITY OF SURAKARTA

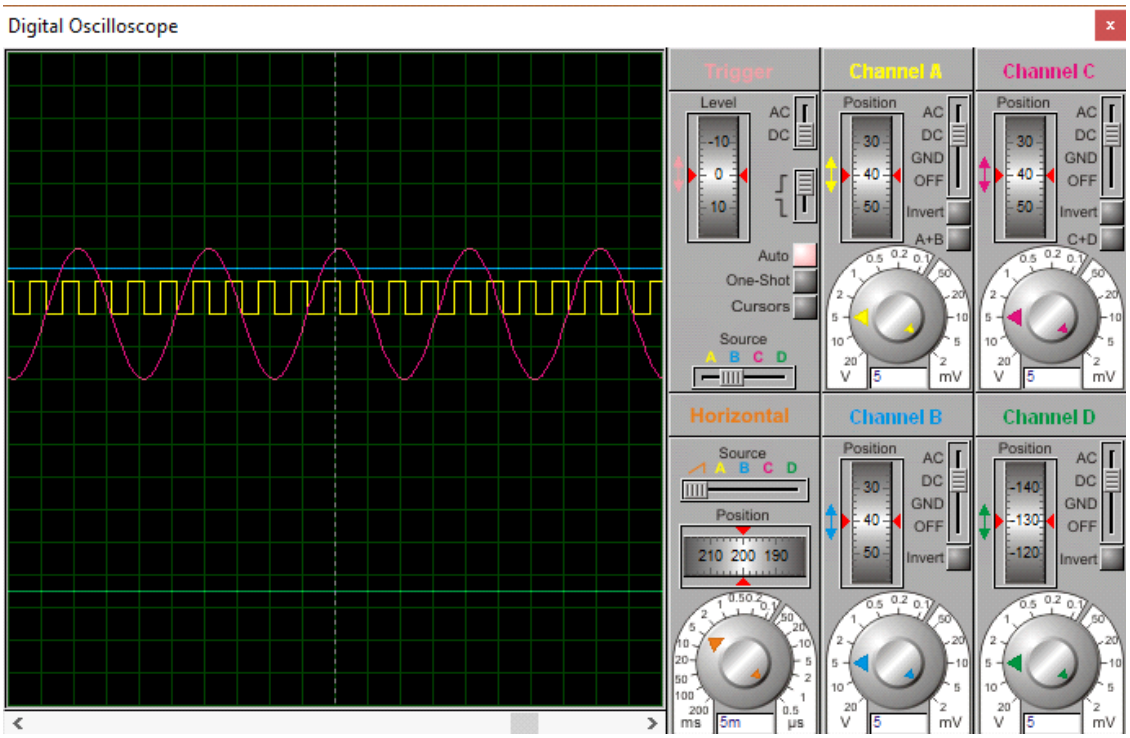
NIM : L200184137
NAME : NADHIFAH CHAIRUNNISA
CLASS : X
ASSISTANT : SALSA SASMITA MUKTI
DATE OF PRACTICUM : Thursday, March 14 2019

THE FIRTS EXPERIMENT



Vpp/div = 5 mV
Time/div = 5 m/s

Signal B and D is still straight, then signal C is bumpy signal, and signal A is case bumpy. Signal A, B, C, D are constant



Vpp/div = 5 mV
Time/div = 5 m/s

Signal B and D still straight, then signal C is bumpy signal, and signal A is case bumpy. Signal A, B, C, D are contant.

Answer the Question Below!

a. What is different betwenn analog signal and digital signal?

The analog signal like signal C that is bumpy signal
The digital signal like signal A that is case bumpy

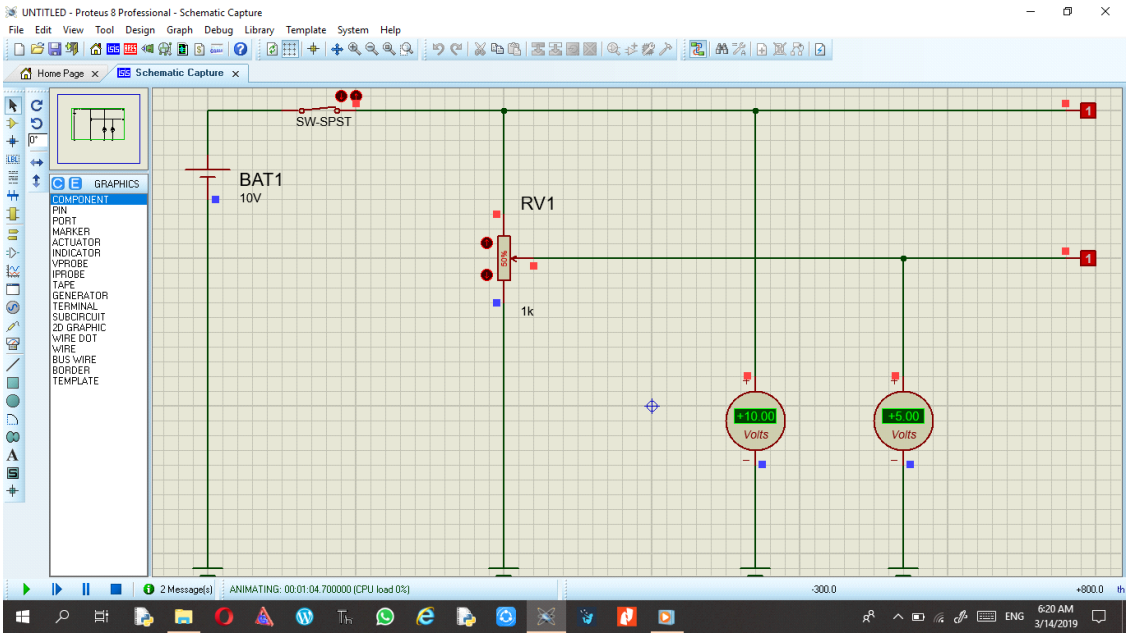
b. How the signal character of respective component?

1. The signal from Alternator (Analog / ~~Digital~~) because can't quantified and the signal is straight
2. The signal from Battery (Analog / ~~Digital~~) because the tension is over off
3. The signal from Clock Sourse (~~Analog~~ / Digital) because can quantified

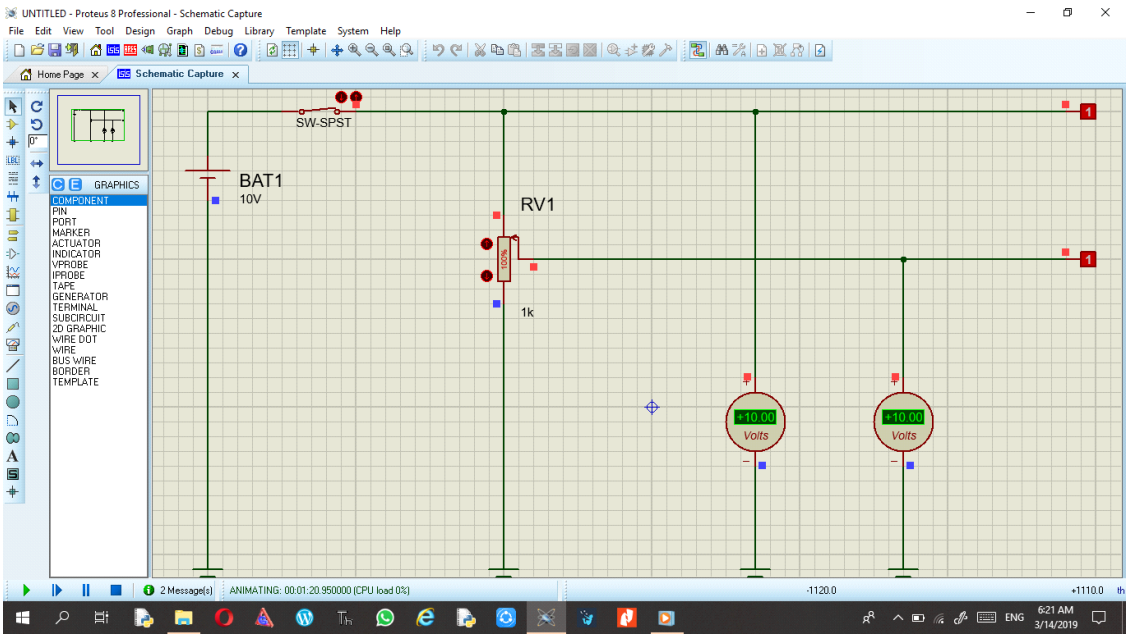
The conclusion

From the experiment type of Signal is can be distinguished from the signal occur in oscilloscope

THE SECOND EXPERIMENT



Voltmeter DC 1 : +10.00 volt
Voltmeter DC 2 : +5.00 volt
LogicProbe 1 is dirrect condition logic 1(high)
LogicProbe 2 is dirrect condition logic 1(high)


UNTITLED - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Home Page
Schematic Capture
SW-SPST
BAT1
10V
RV1
100%
1k
GRAPHICS
COMPONENT
PIN
PORT
MARKER
ACTUATOR
INDICATOR
VPROBE
IPROBE
TAPE
GENERATOR
TERMINAL
SUBCIRCUIT
2D GRAPHIC
WIRE DOT
WIRE
BUS WIRE
BORDER
TEMPLATE
+10.00
Volts
+10.00
Volts
2 Message(s)
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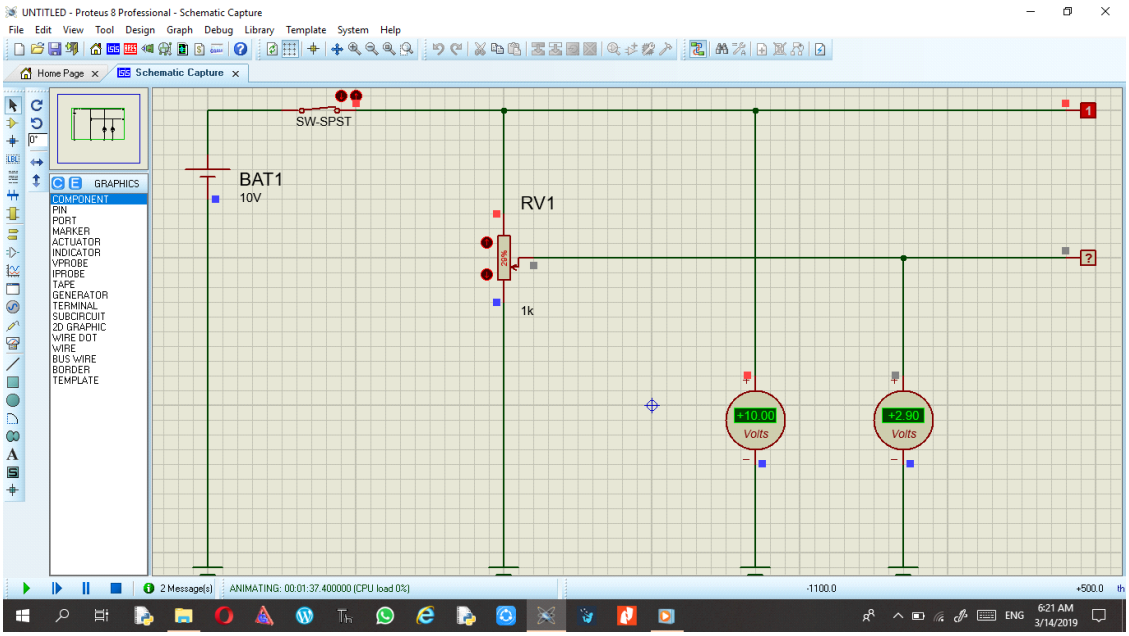
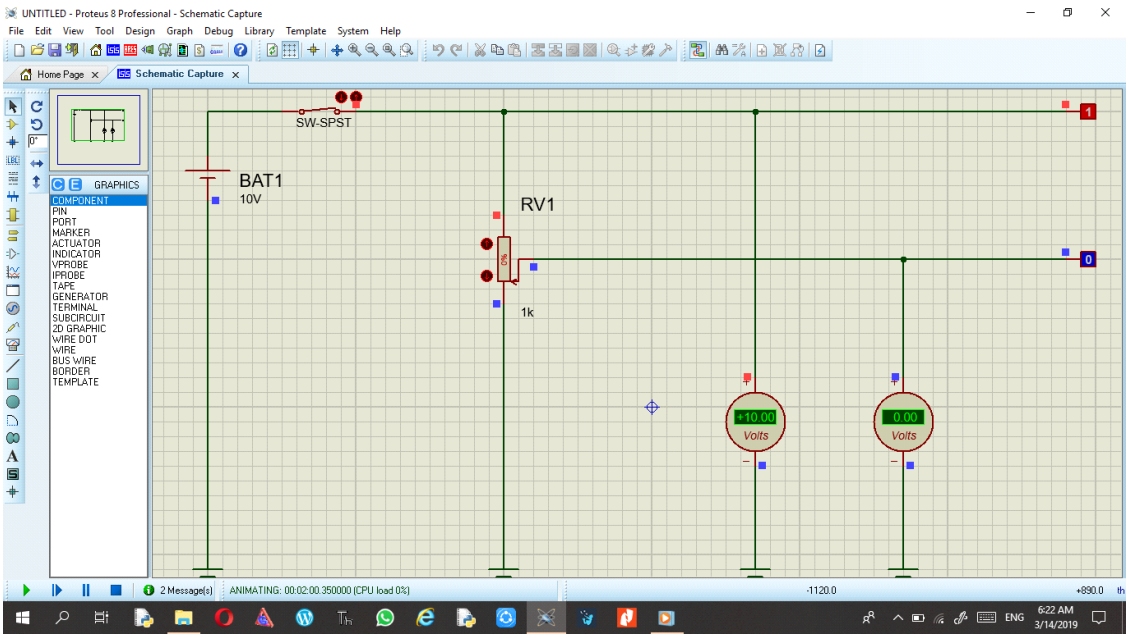
-1120.0
+1110.0
ENG
6:21 AM
3/14/2019


UNTITLED - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Home Page
Schematic Capture
SW-SPST
BAT1
10V
RV1
28%
1k
GRAPHICS
COMPONENT
PIN
PORT
MARKER
ACTUATOR
INDICATOR
VPROBE
IPROBE
TAPE
GENERATOR
TERMINAL
SUBCIRCUIT
2D GRAPHIC
WIRE DOT
WIRE
BUS WIRE
BORDER
TEMPLATE
+10.00
Volts
+2.90
Volts
2 Message(s)
ANIMATING: 00:01:37.400000 (CPU load 0%)
-1100.0
+500.0
ENG
6:21 AM
3/14/2019



LogicProbe 2 dirrect the logic condition **1(High),**
if Voltmeter DC 2 : +5.00 Volt until +10.00 Volt
LogicProbe 2 dirrect the logic condition **0(Low),**
if Voltmeter DC 2 : 0.00 Volt until +10.00 Volt

The Conclusion

When the RV 1 is up then the Voltmeter DC 2 and the LogicProbe is turn on.
When RV 1 is down then DC 2 participate to down until 0.00 and LogicProbe 2 is off