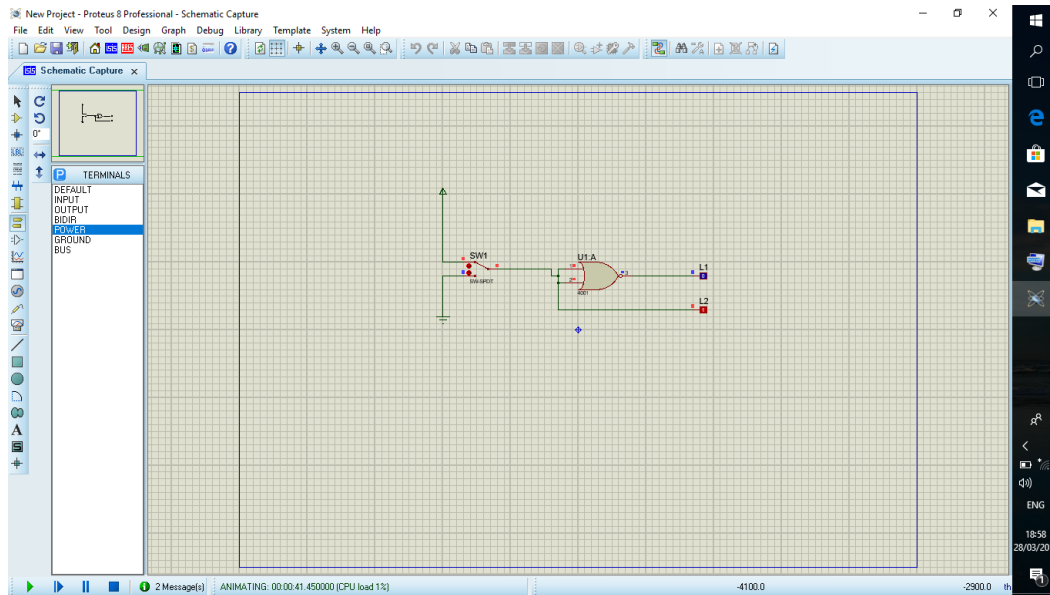


NAME : MOTWKE MHMOUD MAHMED ADAM

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CLASS : X

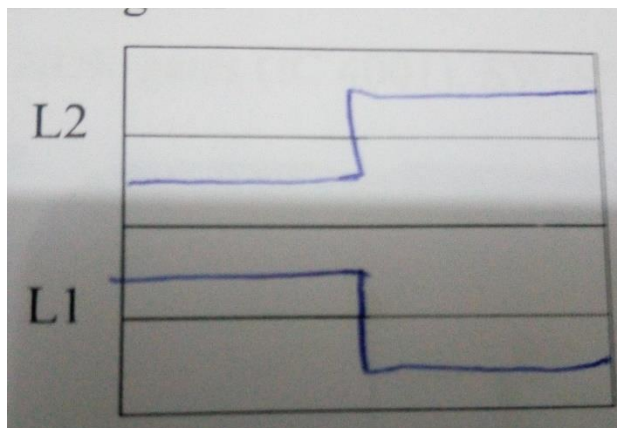
1. Figure 4.3.gate Variation 1



The truth table :

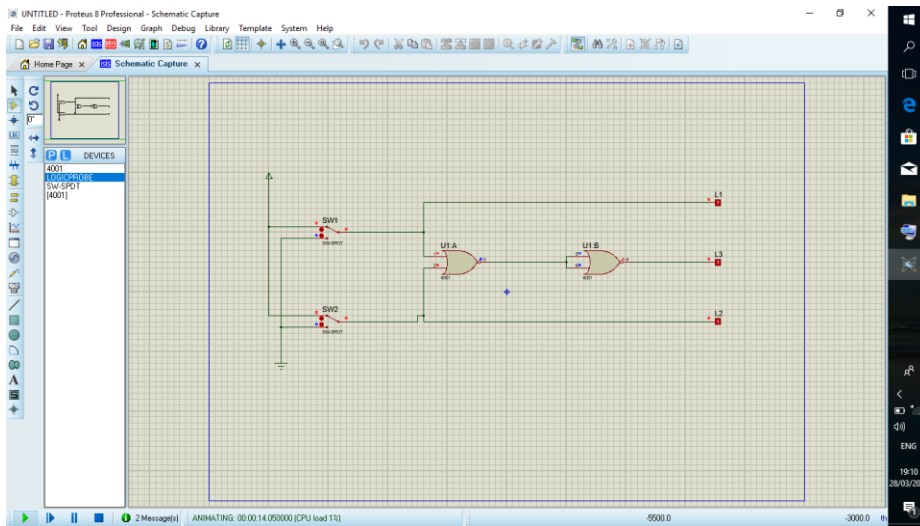
Sw1	L2	L1
0	0	1
1	1	0

TIME Diagram



Conclusion : NOR gate in Figure 4.3 produces NOT gate.

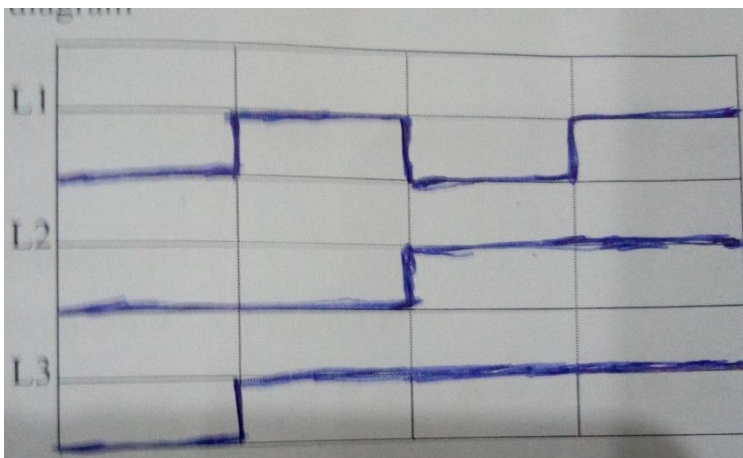
2. Figure 4.4 . Gate Variation 2



The truth table:

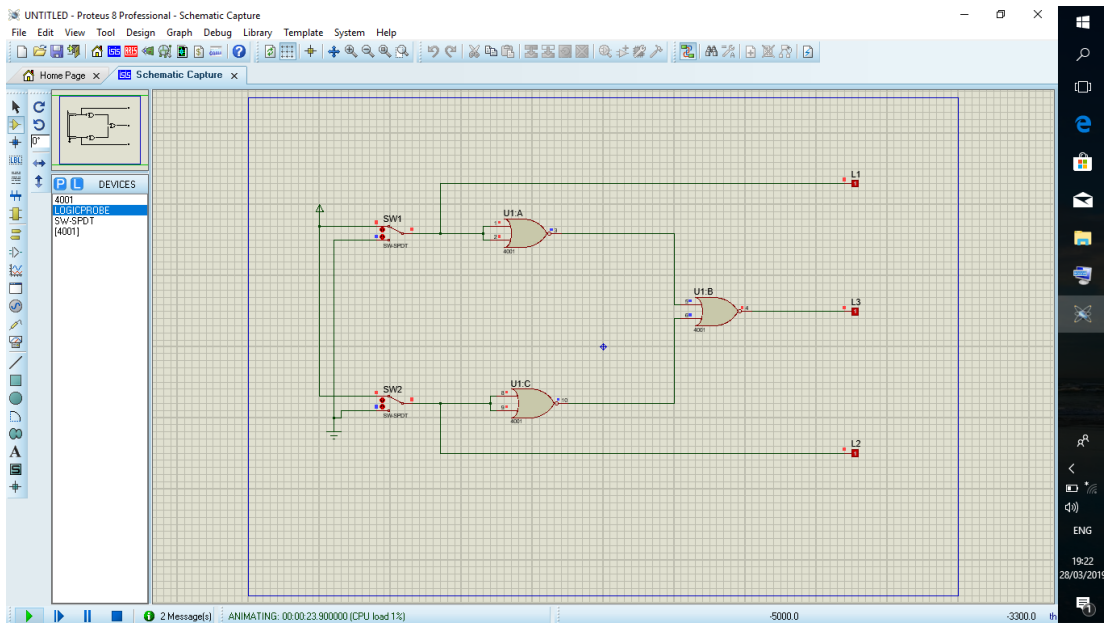
SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	1

TIME Diagram:



Conclusion : NOR gate in Figure 4.4 produces OR gate.

3. Figure 4.5. GATE Variation 3

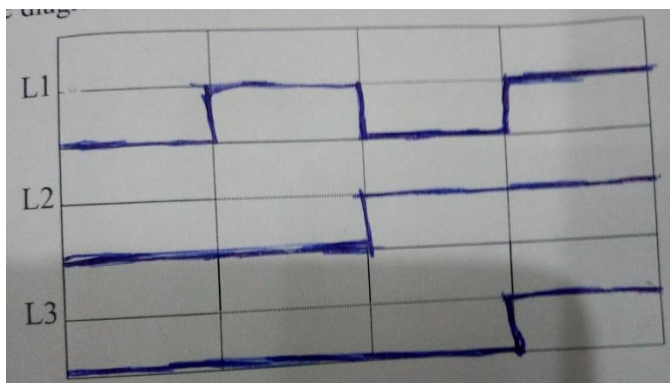


Boolean Function : $L3 = L1 + L2 = L1 . L2$

The truth table:

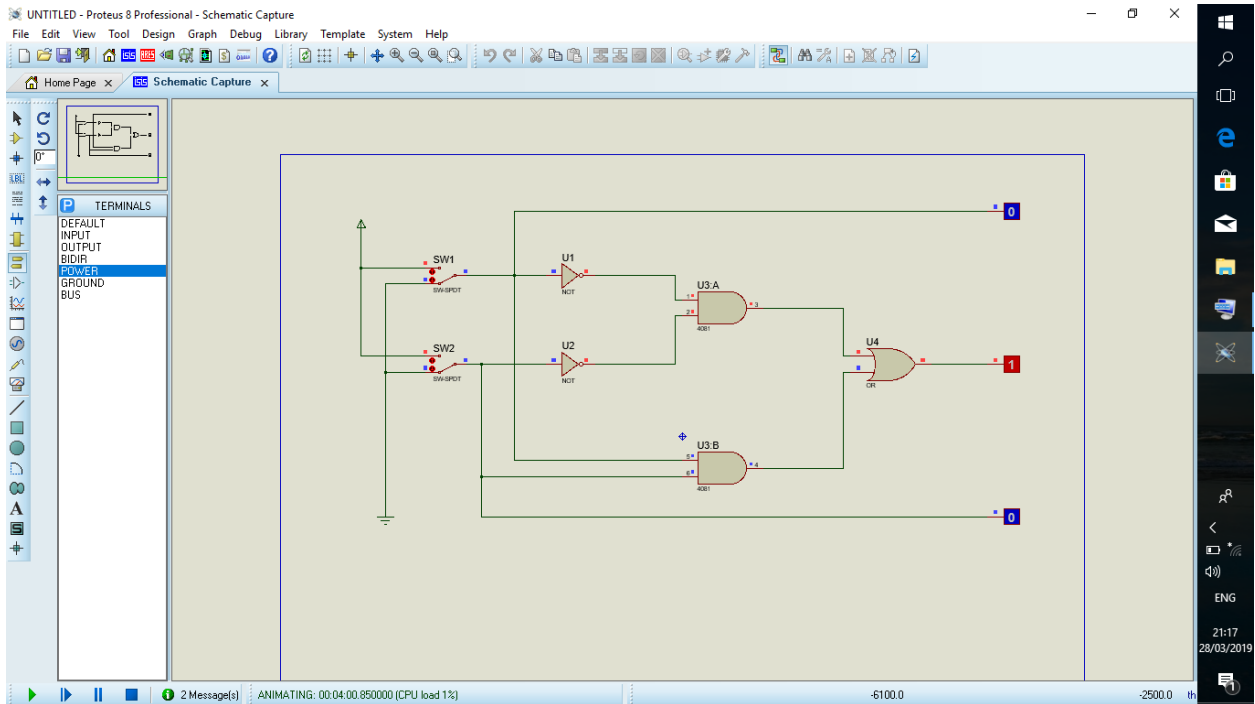
SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	0
0	1	0	1	0
1	1	1	1	1

TIME diagram:



Conclusin: NOR gate in Figure4.5 produces AND GATE.

4. Figure 4.6 GATE Variation 4

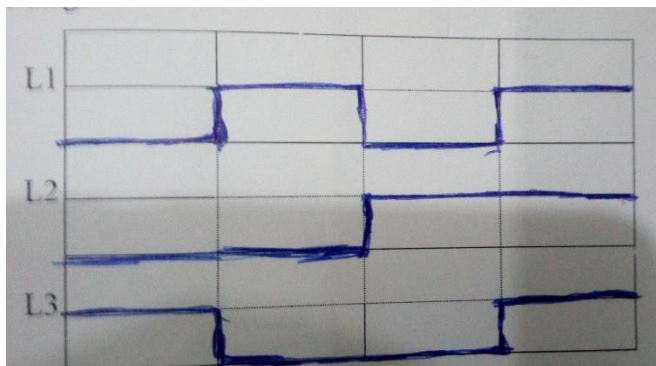


BOOLEAM Function: $L3 = L1L2 + L1L2 = L1 + L2$

THE truth table :

SW1	SW2	L1	L2	L3
0	0	0	0	1
1	0	1	0	0
0	1	0	1	0
1	1	1	1	1

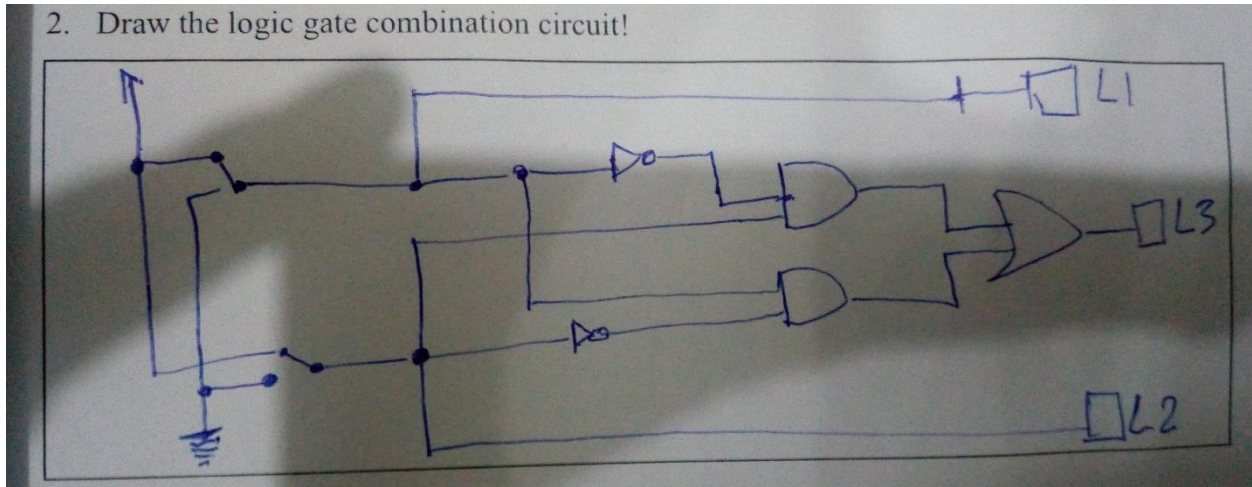
Time diagram :



Conclusion : the gate in 4.6 XNOR gate.

5. EXPERIMENT :

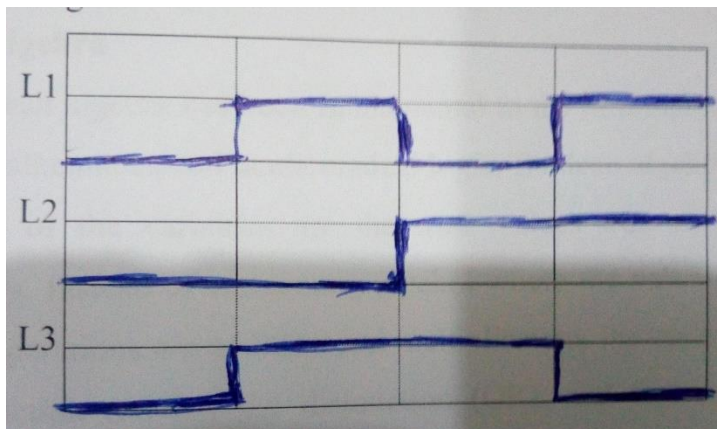
2. Draw the logic gate combination circuit!



THE TRUTH TABLE:

SW1	SW2	L1	L2	L3
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	1	1	0

TIME Diagram:



Conclusion : the combination of the gate above will

Produces XOR gate.