DIGITAL SYSTEM

10th PRACTICUM: FLIP - DECODER IMPLEMENTATION

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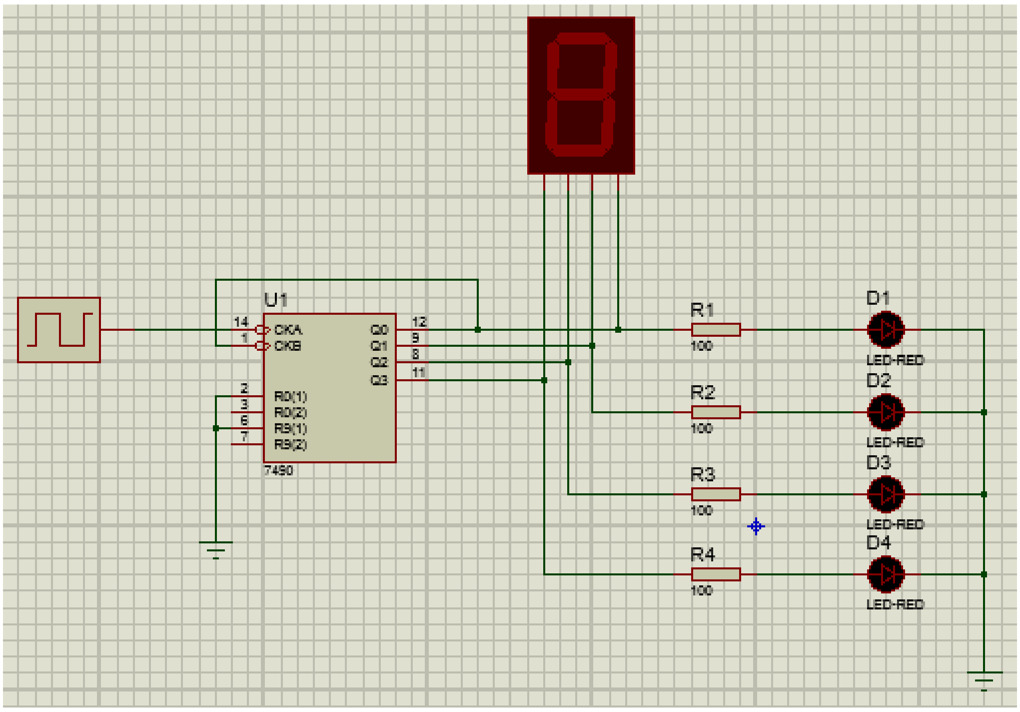
PRACTICUM ACTIVITIES

1st Experiment. Clock counter circuit

1. Make a counter below!

Use IC 7490 (Decade Counter), 7segment (7seg-BCD-red), resistor (res)



2. Fill in the blank fields in Table!

Input Clock	Output LED				Output Seven Segment
	D1	D2	D3	D4	
1	0	0	0	0	0
2	1	0	0	0	1
3	0	1	0	0	2
4	1	1	0	0	3
5	0	0	1	0	4
6	1	0	1	0	5
7	0	1	1	0	6
8	1	1	1	0	7
9	0	0	0	1	8
10	1	0	0	1	9
11	0	0	0	0	0
12	1	0	0	0	1
13	0	1	0	0	2

3. Task : look for datasheet references about IC 7490! Look at the constituent logic gate and report it to the practicing lecturer / assistant!

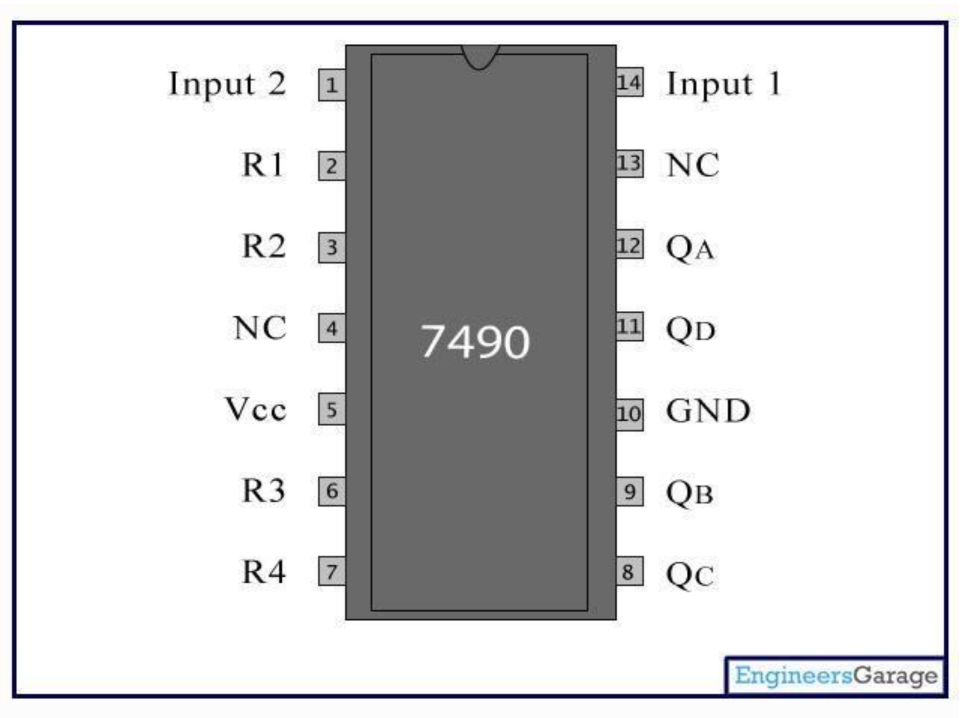
The **74LS90** is a simple counter, i.e. it can count from 0 to 9 cyclically in its natural mode. It counts the input pulses and the output is received as a 4-bit binary number through pins Q_A, Q_B, Q_C and Q_D. The binary output is reset to 0000 at every tenth pulse and count starts from 0 again. A pulse is also generated (probably at pin 9) as it resets its output to 0000. The chip can count up to other maximum numbers and return to zero by changing the modes of 7490. These modes are set by changing the connection of reset pins R_1 - R_4. For example, if either R_1 & R_2 are high or R_3 & R_4 are ground, then it will reset Q_A, Q_B, Q_C and Q_D to 0. If resets R_3 & R_4 are high, then the count on Q_A, Q_B, Q_C and Q_D goes to 1001.

The other high counts can be generated by connecting two or more **7490 ICs**. For example, if two 7490 are connected in a manner that input of one becomes the output of other, the second IC will receive a pulse on every tenth count and will reset at every hundredth count. Thus this system can count from 0 to 99 and give corresponding BCD outputs.

7490 has an inbuilt divide by two and divide by five counters which can be connected in different fashion by changing the connections. It can be used as a divide by 10 counter by connecting Q_A with (clock) input2, grounding all the reset pins, and giving pulse at (clock) input1. This enables the cascade connection of the inbuilt counters. It can also be used as a divide by 6 counter by connecting Q_A with input2, grounding R_3 & R_4, and giving pulse at input1.

By connecting Q_A with input1, 7490 can be used for BCD counting whereas by connecting Q_D with input2, it can be used for bi-quinary counting. Bi-quinary is a system for storing decimal digits in a four-bit binary number. The bi-quinary code was used in the abacus.

Pin Diagram:



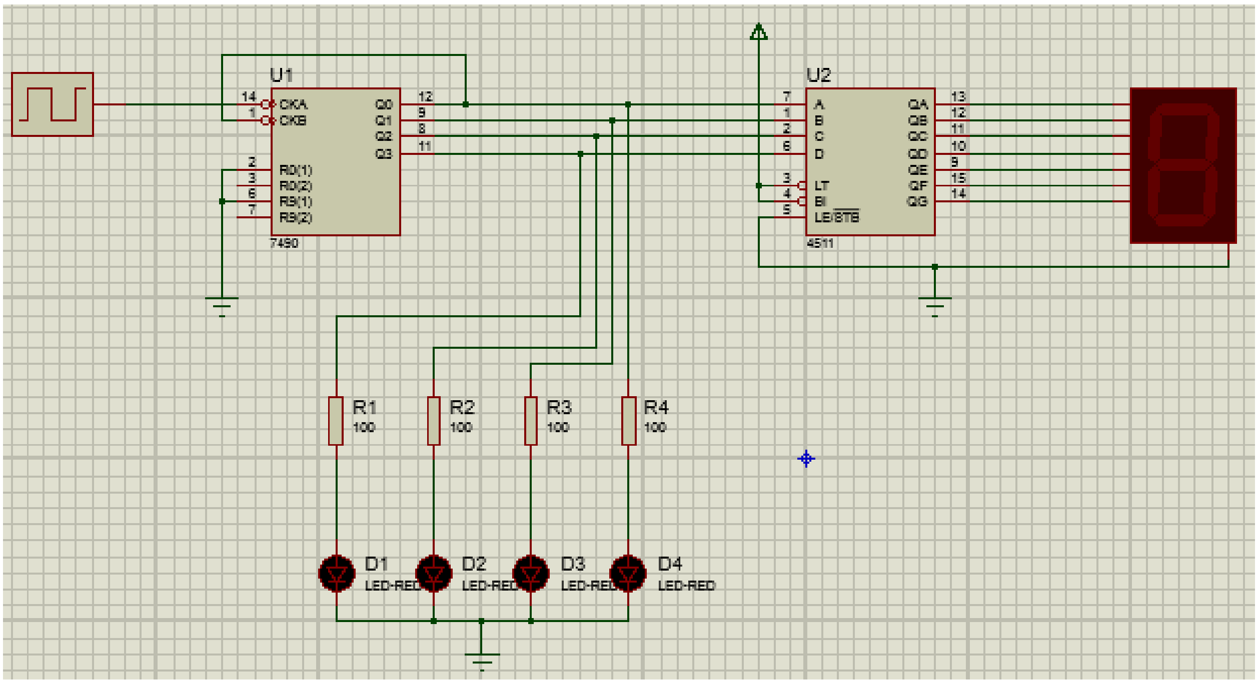
Pin Description:

Pin No	Function	Name
1	Clock input 2	Input2
2	Reset1	R1
3	Reset2	R2
4	Not connected	NC
5	Supply voltage; 5V (4.75V – 5.25V)	Vcc
6	Reset3	R3
7	Reset4	R4
8	Output 3, BCD Output bit 2	Q_C
9	Output 2, BCD Output bit 1	Q_B
10	Ground (0V)	Ground
11	Output 4, BCD Output bit 3	Q_D
12	Output 1, BCD Output bit 0	Q_A
13	Not connected	NC
14	Clock input 1	Input1

2nd Experiment. Addition of a BCD-7-segment Decoder

1. Create a circuit like in experiment 1

Add a circuit with IC 4511 and 7segment common cathode



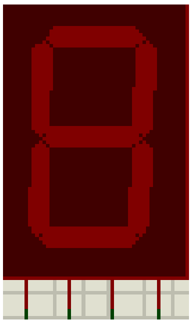
2. Fill in the blank fields in Table!

Input Clock	Output LED				Output Seven Segment
	D1	D2	D3	D4	
1	0	0	0	0	0
2	1	0	0	0	1
3	0	1	0	0	2
4	1	1	0	0	3
5	0	0	1	0	4
6	1	0	1	0	5
7	0	1	1	0	6
8	1	1	1	0	7
9	0	0	0	1	8
10	1	0	0	1	9
11	0	0	0	0	0

3. Compare experiment 1 and experiment 2! Can you see the equation?

<u>The equations in experiments 1 and 2 are located or from the RED-LED.</u>

4. Is it true that 7seg-BCD is the same as the BCD-to-7segment decoder? (…Yes… / …**No**…)



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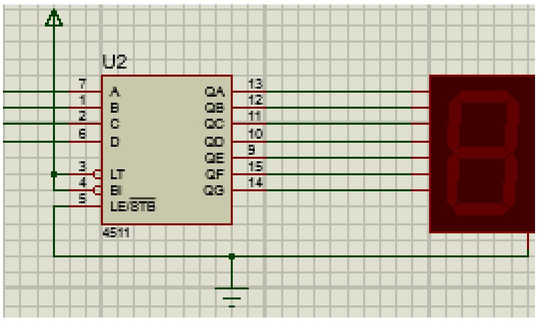


Because it changes when it's blue.

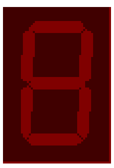
3rd Experiment. Look inside the BCD-to-7segment decoder

1. Note the function table IC 4511

Decimal Digit	*Input*					*Output*							Display *Output*
	LT	D	C	B	A	a	b	c	d	e	f	g	
0	H	L	L	L	L	H	H	H	H	H	H	L	0
1	H	L	L	L	H	L	H	H	L	L	L	L	1
2	H	L	L	H	L	H	H	L	H	H	L	H	2
3	H	L	L	H	H	H	H	H	H	L	L	H	3
4	H	L	H	L	L	L	H	H	L	L	H	H	4
5	H	L	H	L	H	H	L	H	H	L	H	H	5
6	H	L	H	H	L	L	L	H	H	H	H	H	6
7	H	L	H	H	H	H	H	H	L	L	L	L	7
8	H	H	L	L	L	H	H	H	H	H	H	H	8
9	H	H	L	L	H	H	H	H	L	L	H	H	9
LT	L	X	X	X	X	H	H	H	H	H	H	H	8

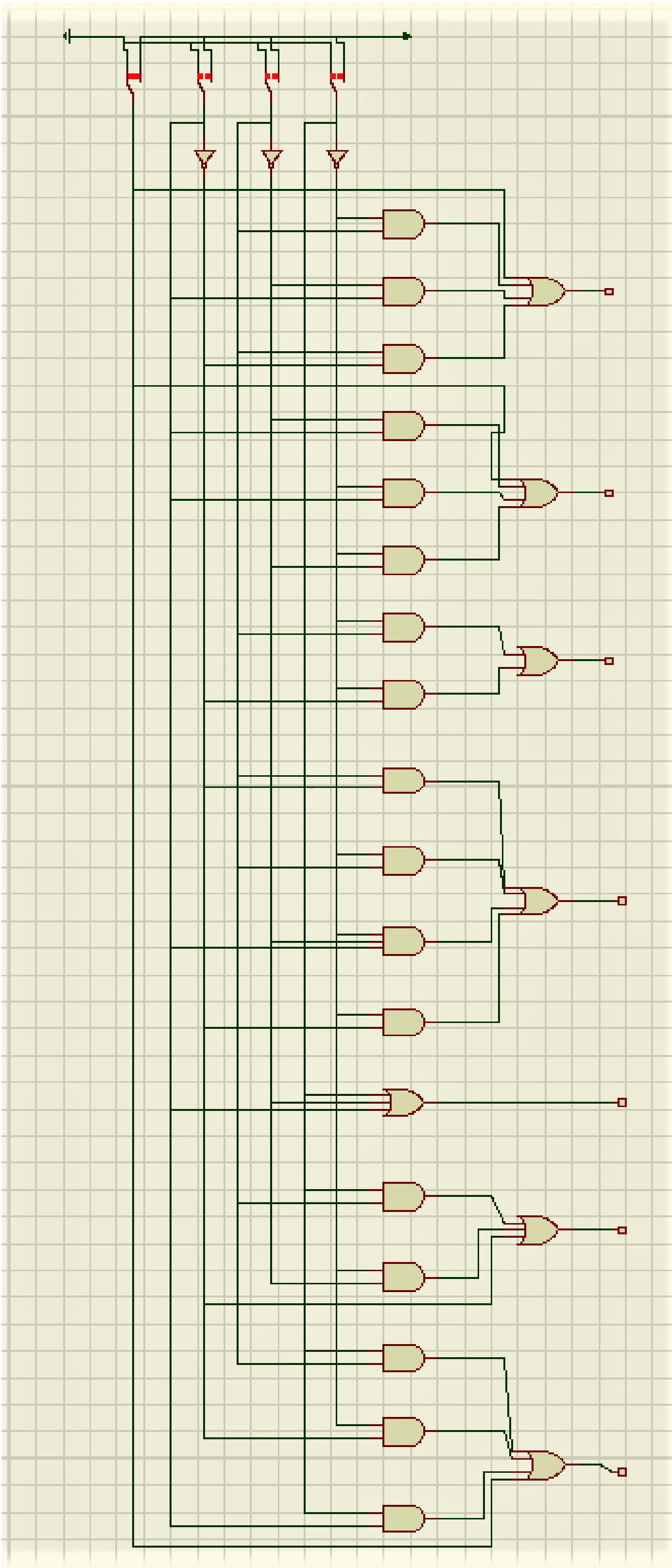
2. The output "a" (highlight) in the table shows the LED in the seven segment Common cathode.
3. Each output shows the state of LED from seven segment various conditions

Common Cathode



4. Each LED is controlled by a combination of logic gates.

The complete logic diagram of the BCD-to-7segment decoder is shown in the following figure.



Assigment

Try making the BCD-7 decoder series above, and compare it to the truth table at point number 1!

<u>The output results in the BCD-to-7-segment decoder circuit produce a value that exactly matches the truth table</u>