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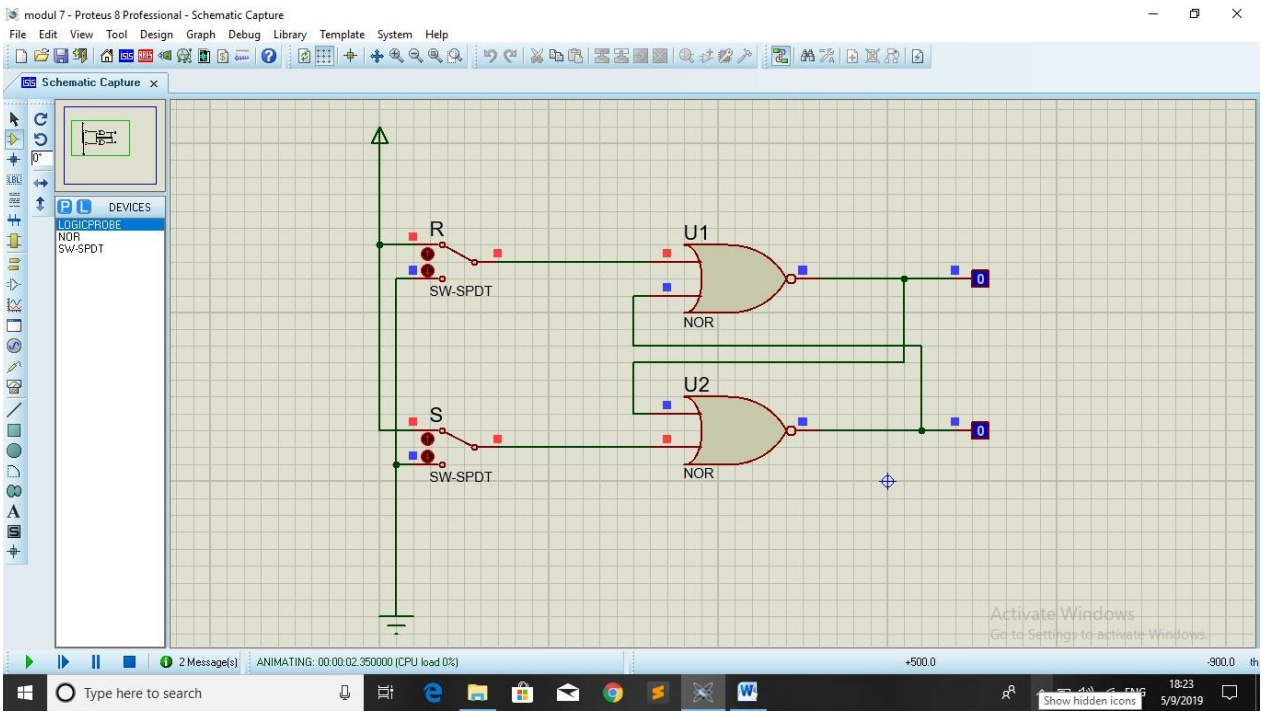
Class : X

Experiment 1



1. Make and simulate the NOR latch!
2. Based on your simulation, fill the blanks!

	S	R	Output	
			Q	Q’
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

3. Answer the following questions!
   a. What will happen if the condition given was S = R = 0?

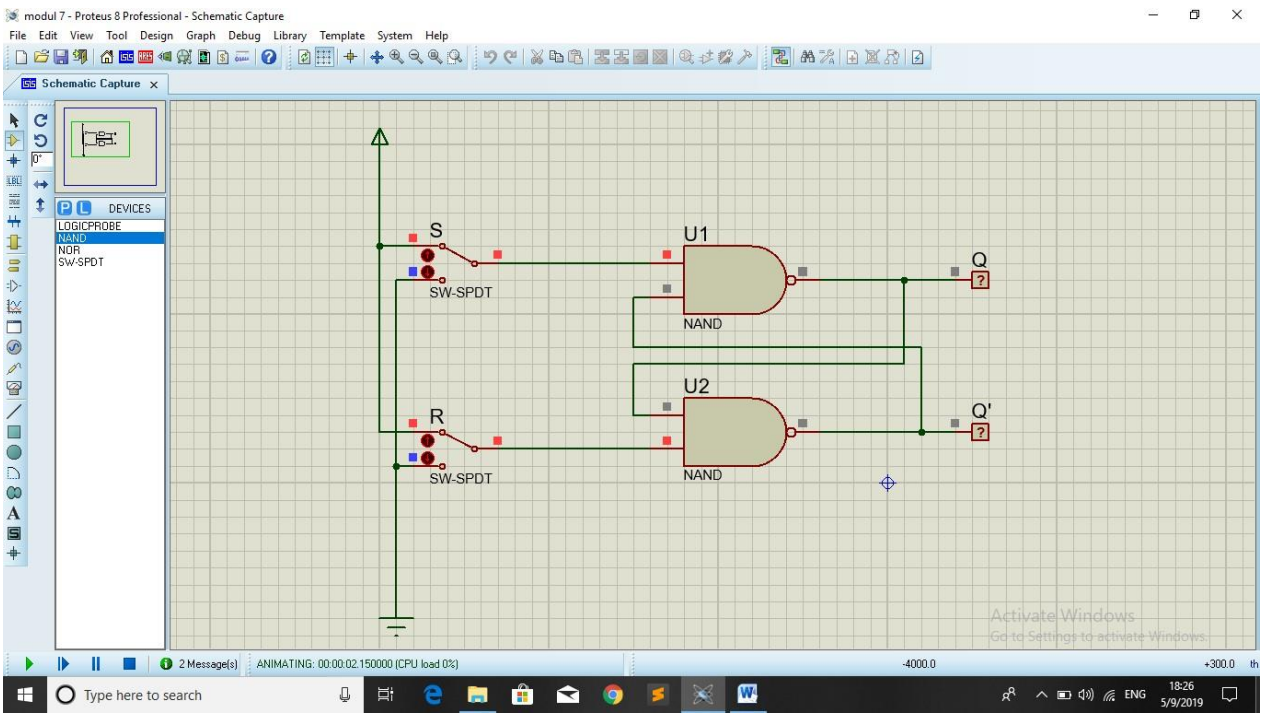
The output value depends on the output in the previous condition

Why the condition S = R = 1 is not allowed?

Because the output of this condition will be Q = Q' = 0 (Q can't be the same with Q')

Experiment 2

1. Make and simulate the NAND latch!



2. Based on your simulation, fill the blanks!

	S	R	Output	
			Q	Q'
1	0	1	1	0
2	1	1	1	0
3	1	0	0	1
4	1	1	0	1

3. Answer the following questions!
   a. What will happen if we gave the S =R = 1 condition?

The output value depends on the output in the previous condition

b. Why the condition S = R = 1 is not allowed?

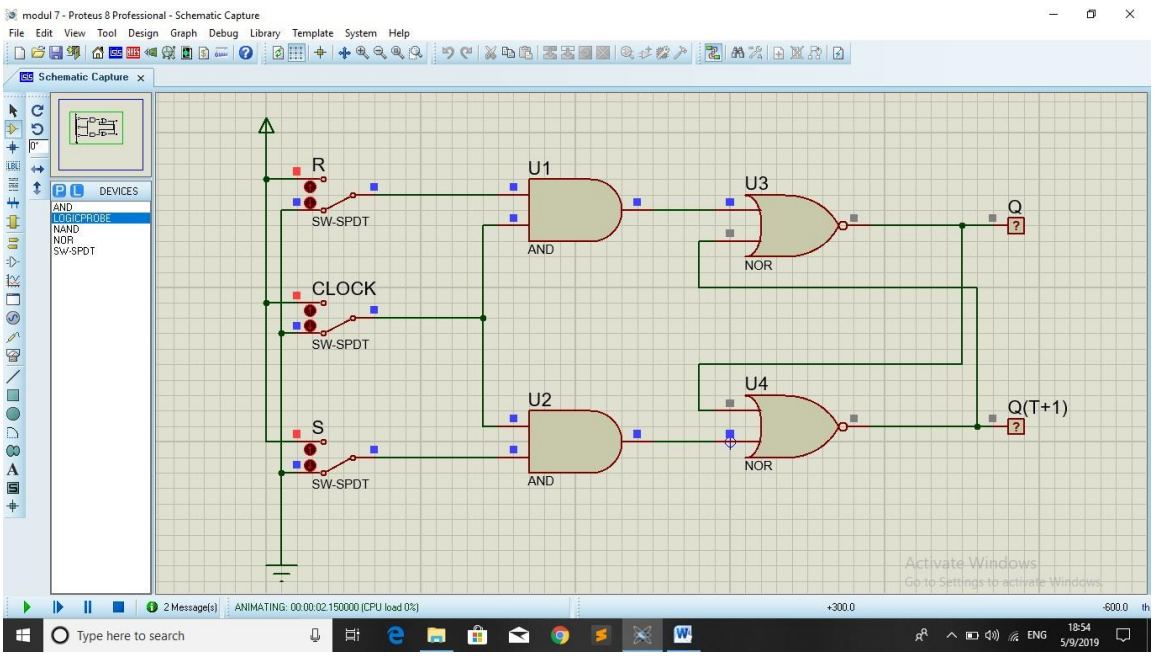
Because the output of this condition will be Q = Q' = 1 (Q can't be the same with Q')

4. Based on the flip-flop circuit above, what's your opinion about "Flip-flop and latch are used to data storing element"

True, because it can memorize / save the state / condition value when asked (use the Reset switch)

Experiment 3

1. Make and simulate the RS Flip-flop!



2. Based on your simulation, fill the blanks!

	S	R	CLOCK	Output	
				Q	Q’
1	0	0	0	-	-
2	0	0	1	-	-
3	0	1	0	-	-
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

3. Answer the following questions!
   a. What will happen if the condition S = R = 1 was given and the clock changes from 1 to 0?

      Error will occur; *“Logic race condition detected during transient analysis”*

   b. How was that happened?

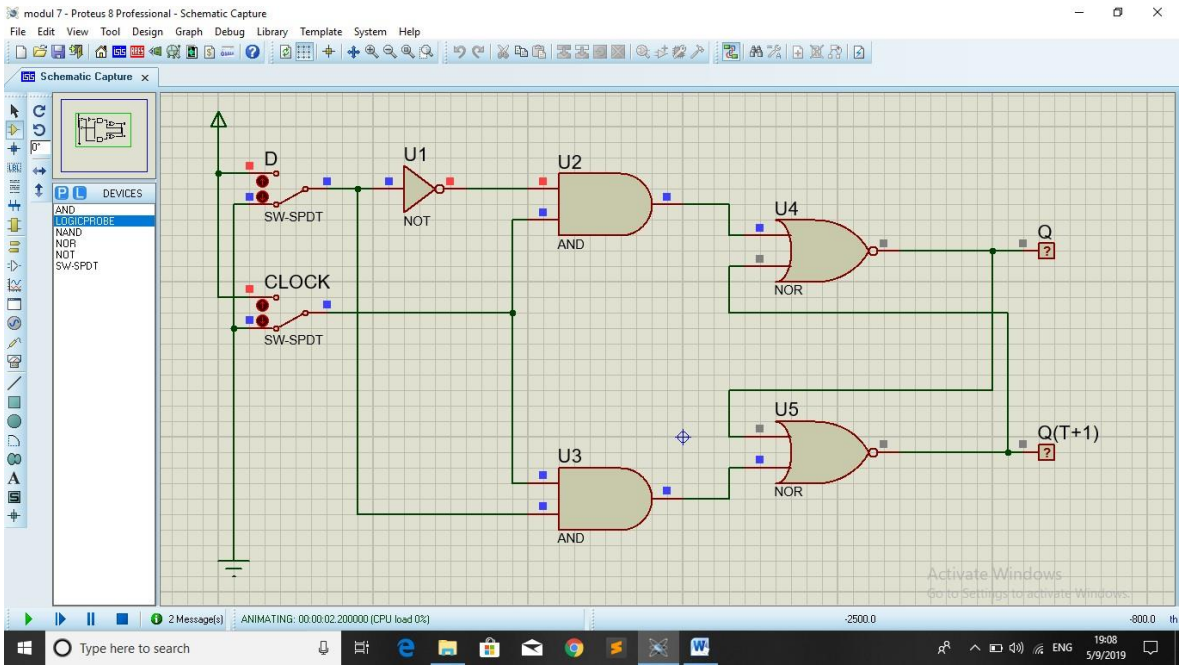
      The flip-flop saved the wrong value, Q = Q(t+1) = 0

4. Explain how the RS Flip-flop works!

   Clock will lock / store / save the previous output condition whenever the clock was turned from 1 to 0

Experiment 4

1. Make and simulate the D Flip-flop



2. Based on your simulation, fill the blanks!

	D	CLOCK	Output	
			Q	Q(t+1)
1	0	0	-	-
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

3. Explain how does D Flip-flop works!

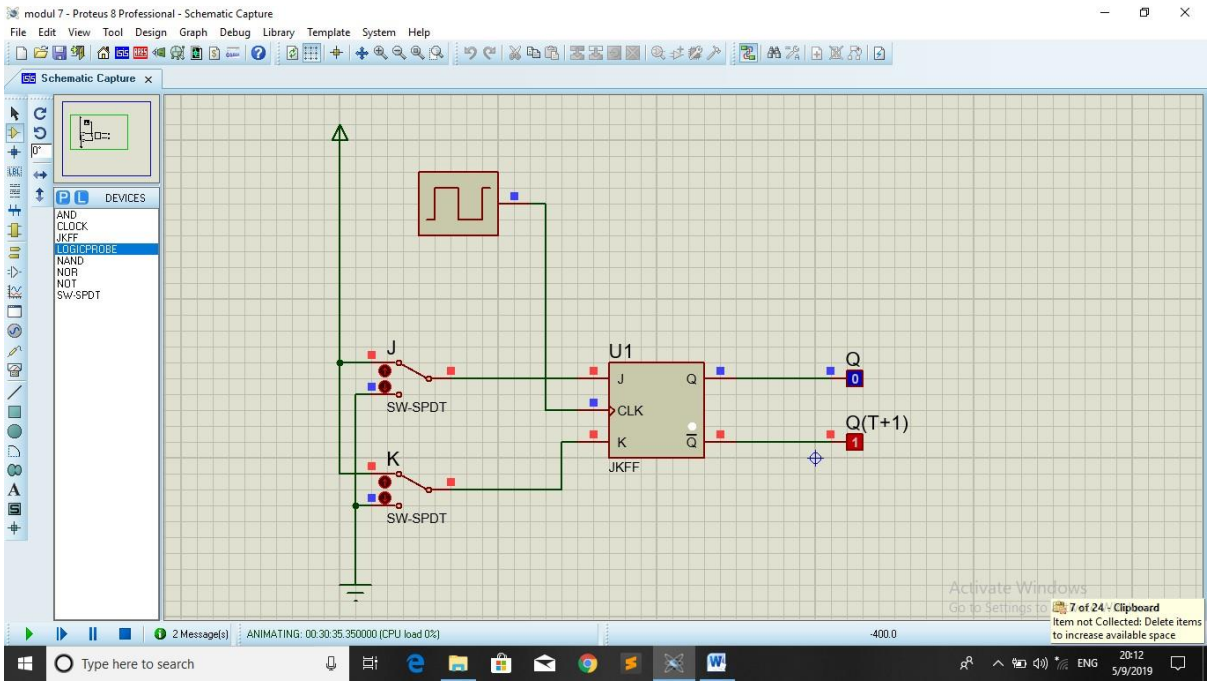
   D Flip-flop have 1 condition input only. Clock is used to store / lock the previous output condition.

4. What is the function of the NOT gate?

   RS Flip-flop has 2 condition input that determine each other output values (Q and Q'), meanwhile D Flip-flop only has one. So the NOT gate is used to make all the output (Q and Q') has a different value.

Experiment 5

1. Make and simulate the JK Flip-flop!



2. Based on your simulation, fill the blanks!

	J	K	CLOCK	Output	
				Q	Q(t+1)
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	1	0
7	1	1	0	0	1
8	1	1	1	0	1

3. Answer the following questions!
   a. What will happen if J = K = 0, and the clock rise up (change from 0 to 1)?

      Clock will lock / store / save the previous output condition

   b. What will happen if J = K = 1 and the clock rises up?

      The flip-flop can be adjusted or reset.

4. Explain how JK flip-flop works!

   J and K are control inputs that determine whatever the flip-flop is going to do when receiving increased clock pulse. The RC circuit has short time constants that transform the clock pulse into narrow impulses.