Signal		
/tbregisterfile/clk		
/tbregisterfile/reset		
/tbregisterfile/enable		
/tbregisterfile/rd1		
/tbregisterfile/rd2		
/tbregisterfile/wr		
/tbregisterfile/add_wr	22	8
/tbregisterfile/add_rd1	22	8
/tbregisterfile/add_rd2	28	8
/tbregisterfile/datain	0	18446744073709551615
/tbregisterfile/out1	X	0 ... 18446744073709551615
/tbregisterfile/out2	X	184467440737095...

0 ps   5000 ps   10000 ps   15000 ps   20000 ps

Entity:tbregisterfile Architecture:testa Date: Thu Apr 14 10:38:43 AM CEST 2016   Row: 1 Page: 1