FET Characteristics Trainer

NV6512

Operating Manual

Ver 1.1

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FET Characteristics Trainer

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Introduction

NV6512 "FET Characteristics Trainer" is a compact, ready to use experiment board. This is useful for students to plot different characteristics of an N- channel field effect transistor and to understand operation of an FET in different regions. With the help of this trainer, student can also evaluate Drain resistance, Transconductance, Amplification factor, and DC drain resistance. It can be used as stand alone unit with inbuilt (SMPS) DC power supply provided with it.

Features

- **Exclusive and compact design**
- **+12V, -5V inbuilt power supplies**
- **Inbuilt voltmeter and ammeter**
- **Diagrammatic representation for the ease of connections**
- **Provided with an extensive operating manual**
- **Two years warranty**

Technical Specifications

Mains supply	**:**	230 V ±10%, 50 Hz
DC Power supply	**:**	+12V, -5V
FET	**:**	J112A
Voltmeter		
Range	**:**	200mV to 200V
Display	**:**	$3^{1/2}$ digit
Ammeter	**:**	
Range	**:**	2μA to 200mA
Display	**:**	$3^{1/2}$ digit
Dimensions(mm)	**:**	W240 x D345 x H110

Theory

Field-effect transistor :

The field-effect transistor (FET) is a type of transistor that relies on an electric field to control the shape and hence the conductivity of a 'channel' in a semiconductor material. Field-effect transistors are so named because a weak electrical signal coming in through one electrode, creates an electrical field through the rest of the transistor.

Composition :

The FET can be constructed from a number of semiconductors, silicon being by far the most common. Most FETs are made with conventional bulk semiconductor processing techniques, using the single crystal semiconductor wafer as the active region, or channel.

Among the more unusual body materials are amorphous silicon, polycrystalline silicon or other amorphous semiconductors in thin-film transistors or organic field effect transistors that are based on organic semiconductors and often apply organic gate insulators and electrodes.

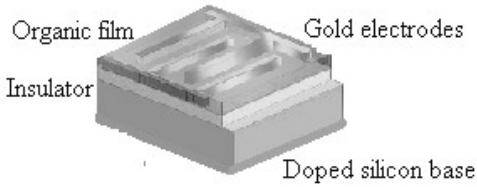


Figure 1

“Cleanliness is next to godliness” applies to the manufacture of field effect transistors. Though it is possible to make bipolar transistors outside of a clean room, it is a necessity for field effect transistors. Even in such an environment, manufacture is tricky because of contamination control issues. The unipolar field effect transistor is conceptually simple, but difficult to manufacture. Most transistors today are a metal oxide semiconductor variety of the field effect transistor contained within integrated circuits. However, discrete JFET devices are available.

FET operation :

A field effect transistor (FET) is a unipolar device, conducting as current using only one kind of charge carrier. If it is based on an N-type slab of semiconductor, the carriers are electrons. Conversely, a P-type based device uses only holes. At the circuit level, field effect transistor operation is simple. A voltage applied to the gate, input element, controls the resistance of the channel, the unipolar region between the gate regions. Generally two types of FET are used: (1) Junction field effect transistor (JFET), (2) Metal oxide semiconductor field effect transistor (MOSFET).

Construction of JFET :

The junction field effect transistor (JFET) is constructed in the following two ways:

1. N channel JFET

2. P channel JFET

N channel JFET :

It consists of a thin bar of N type semiconductor with two junctions with the P type semiconductor near the center, at opposite sides of the bar. Thus we get two P-N junctions on either side of the bar. Both the P type semiconductors are internally connected together (i.e., both have the common one terminal). This terminal is called the gate and is represented by the letter G. When this terminal is given a potential, the P type semiconductor of both the junctions are at same potential.

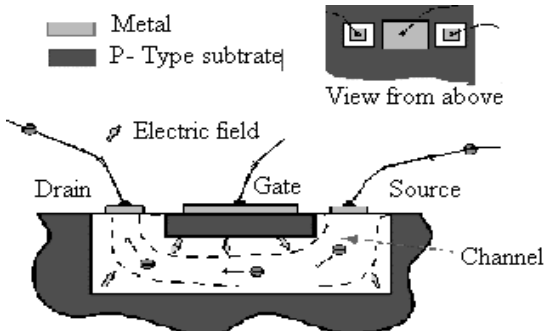


Figure 2

The region between the two junctions is called the channel. The terminals from the either ends of the N type semiconductor are called the source and drain which are represented by the letters S and D respectively in Figure 2. When a potential difference is applied between the drain D and the source S, the majority charge carriers of N channel (i.e., electrons) move in accordance with the applied potential. As a result, current flows through the channel.

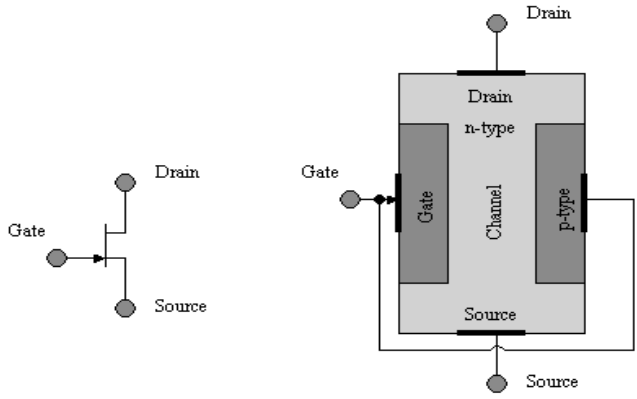


Figure 3

P channel JFET :

It consists of a thin bar of P type semiconductor with two junctions with the N type semiconductor near the center, at opposite sides of the bar. Thus we get two P-N junctions on either side of the bar. Both the N type semiconductors are internally connected together (i.e., both have the common one terminal) as shown in Figure 4. The common terminal is called the gate G. The terminals extending out of two ends of the P semiconductor are called th source S and drain D. When a potential difference is applied between the drain D and the source S, the majority charge carriers of P channel (i.e., holes) move in accordance with the applied potential. As a result, the current flows through the channel.

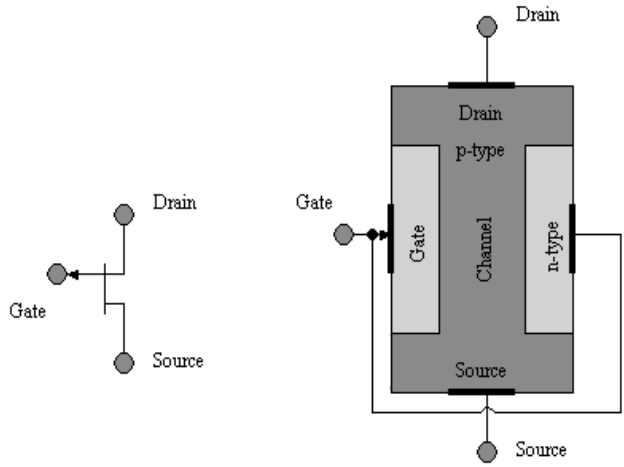


Figure 4

Operation of JFET :

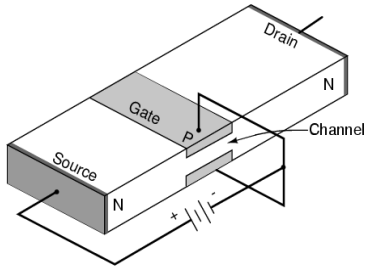


Figure 5

A properly biased N-channel junction field effect transistor (JFET) is shown in Figure 5 above. The gate constitutes a diode junction to the source to drain semiconductor slab. The gate is reverse biased. If a voltage (or an ohmmeter) were applied between the source and drain, the N-type bar would conduct in either direction because of the doping. Neither gate nor gate bias is required for conduction. If a gate junction is formed as shown, conduction can be controlled by the degree of reverse bias.

Figure below 6(a) shows the depletion region at the gate junction. This is due to diffusion of holes from the P-type gate region into the N-type channel, giving the charge separation about the junction, with a non-conductive depletion region at the junction. The depletion region extends more deeply into the channel side due to the heavy gate doping and light channel doping.

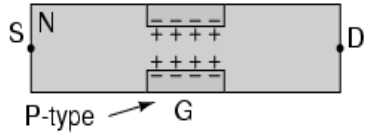


Figure 6(a)

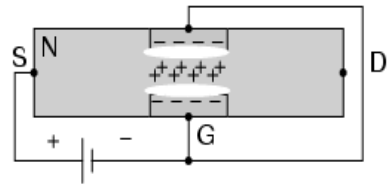


Figure 6(b)

N-channel JFET: Figure 6(a) Depletion at gate diode. Figure 6(b) Reverse biased gate diode increases depletion region.

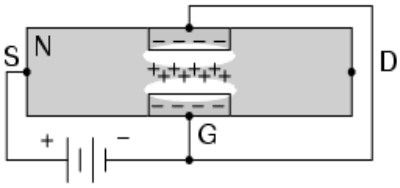


Figure 6(c)

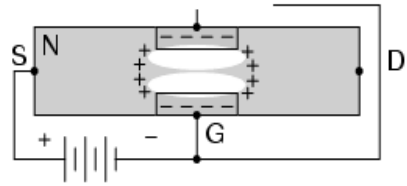


Figure 6(d)

Figure 6(c) Increasing reverse bias enlarges depletion region. Figure 6(d) Increasing reverse bias pinches-off the S-D channel.

The thickness of the depletion region can be increased Figure above 6(b) by applying moderate reverse bias. This increases the resistance of the source to drain channel by narrowing the channel. Increasing the reverse bias at 6(c) increases the depletion region, decreases the channel width and increases the channel resistance. Increasing the reverse bias V_{GS} at 6(d) will pinch-off the channel current. The channel resistance will be very high. This V_{GS} at which pinch-off occurs is V_P, the pinch-off voltage. It is typically a few volts. In summation, the channel resistance can be controlled by the degree of reverse biasing on the gate.

The source and drain are interchangeable, and the source to drain current may flow in either direction for low level drain battery voltage (<0.6 V). That is, the drain battery may be replaced by a low voltage AC source. For a high drain power supply voltage, to 10's of volts for small signal devices, the polarity must be as indicated in Figure below 7(a). This drain power supply, distorts the depletion region, enlarging it on the drain side of the gate. This is a more correct representation for common DC drain supply voltages, from a few to tens of volts. As drain voltage V_{DS} is increased, the gate depletion region expands toward the drain. This increases the length of the narrow channel, increasing its resistance a little. We say "a little" because large resistance changes are due to changing gate bias. Figure below 7(b) shows the schematic symbol for an N-channel field effect transistor compared to the silicon cross-section at 7(a). The gate arrow points in the same direction as a junction diode. The “pointing” arrow and “non-pointing” bar correspond to P and N-type semiconductors, respectively.

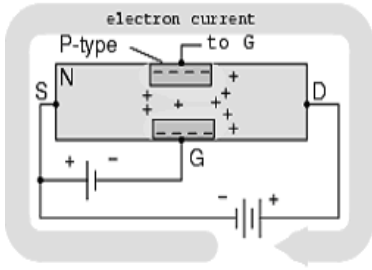


Figure 7(a)

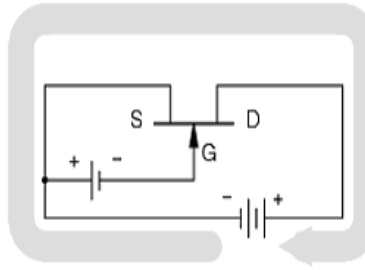


Figure 7(b)

N-channel JFET electron current flow from source to drain in Figure 7(a) cross-section, Figure 7(b) schematic symbol.

Figure 7(a) above shows a large electron current flow from (-) battery terminal, to FET source, out the drain, returning to the (+) battery terminal. This current flow may be controlled by varying the gate voltage. A load in series with the battery is an amplified version of the changing gate voltage.

P-channel field effect transistors are also available. The channel is made of P-type material. The gate is a heavy N-type region. All the voltage sources are reversed in the P-channel circuit (Figure 8(a) below) as compared with the more popular N-channel device. Also note the arrow points out of the gate of the schematic symbol Figure 8(b) of the P-channel field effect transistor.

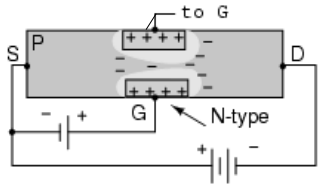


Figure 8(a)

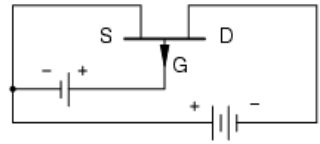


Figure 8(b)

P-channel JFET: Figure 8(a) N-type gate, P-type channel, reversed voltage sources compared with N-channel device. Figure 8(b) Note reversed gate arrow and voltage sources on schematic.

Uses :

FET is a voltage controlled current device so its characteristics are the curves which represent relationship between different DC currents and voltages.

These are helpful in studying different region of operation of a Field effect transistor when connected in a circuit. The two important characteristics of a Field Effect Transistor are:

1. Output /Drain characteristic.

Transfer characteristic.

Output / Drain Characteristics :

It is the curve plotted between output drain current I_D versus output drain to source voltage V_{DS} for constant values of input Gate to source voltage V_{GS} as shown in Figure 9.

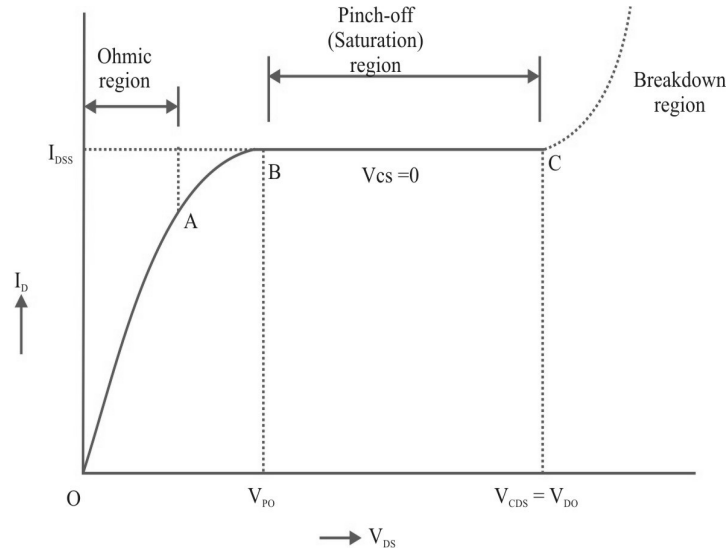


Figure 9

It can be subdivided into following four regions:

Ohmic region OA :

This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

Curve AB :

In this region, I_D increases at inverse square law rate up to point B which is called Pinch-off point. This progressive fall in the rate of increase of I_D is caused by the square law increase in the depletion region at each gate up to point B where the two regions are closest without touching each other. The drain to source voltage V_{DS} corresponding to point B is called pinch-off voltage V_{PO}.

Pinch-off region BC :

It is also known as saturation region or 'amplifier' region. Here, JFET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}. Drain current in this region is given by Shockley's equation. It is the normal operating region of the JFET when used as an amplifier.

$$I_D = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{PO}}\right)^2\right]$$

$$I_D = I_{DSS}\left[-\left(\frac{V_{GS}}{V_{GS(off)}}\right)^2\right]$$

Breakdown region :

If V_{DS} is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where I_D increases to an extensive value. This happens because the reversed biased gate channel PN junction undergoes avalanche breakdown when small change in V_{DS} produce very large change in I_D.

JFET characteristics with external bias :

Figure 10 shows a family of I_D versus V_{DS} curves for different values of V_{GS}. It is seen that as the negative gate bias voltage is increased:

Pinch-off voltage V_P is reached at a lower value of V_{DS} than $V_{GS} = 0$. Value of V_{DS} for breakdown is decreased.

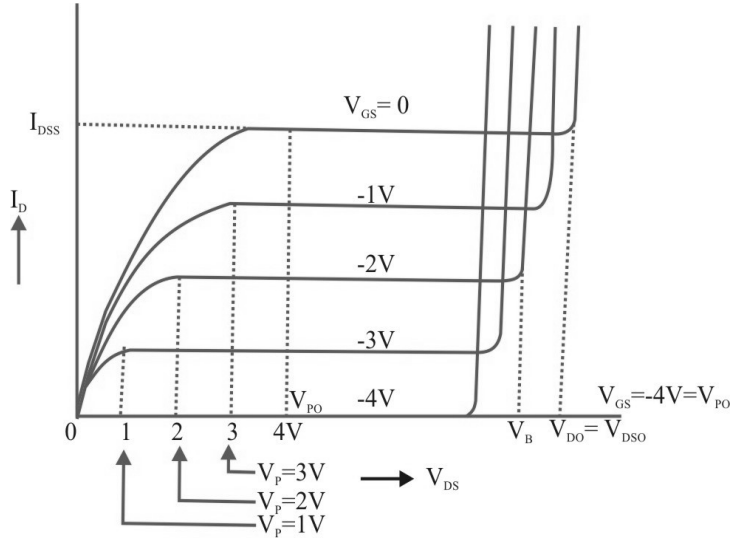


Figure 10

Transfer characteristic :

It is the curve plotted between output drain current versus input Gate to source voltage for constant values of output drain to source voltage as shown in Figure 11.

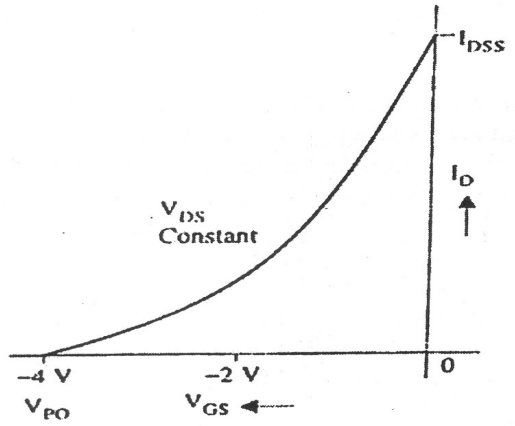


Figure 11

It is similar to the transconductance characteristics of a vacuum tube or a transistor. It is shows that when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $I_D = 0$, $V_{GS} = V_{PO}$.

$$I_D = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{PO}}\right)^2\right]$$

The transfer characteristic approximately follows the equation

$$I_D = I_{DSS}\left[-\left(\frac{V_{GS}}{V_{GS(off)}}\right)^2\right]$$

$$V_{GS} = V_{GS(off)}\left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/2}\right]$$

The above equation can be written as

These characteristics can also be obtained from the drain/output characteristics by reading off V_{GS} and I_{DSS} values for different values of V_{DS}.

The various parameters of a JFET can be obtained from its two characteristics. The main parameters of a JFET when connected in common source mode are

AC Drain Resistance, r_d :

It is the ac resistance between drain and source terminals when JFET is

$$r_D = \frac{\text{change on } V_{DS}}{\text{change on } I_D}$$

operating in the pinch-off region. It is given by

$$r_D = \frac{V_{DS}}{I_D} \text{ at constant } V_{GS}$$

at V_{GS} constant or

An alternative name is dynamic drain resistance. It is given by the slope of the drain characteristics in the pinch off region. It is sometimes written as r_{ds} emphasizing the fact that it is the resistance from drain to source. Since r_d is usually the output resistance of a JFET, it may also be expressed as an output admittance Y_{os}. Obviously, $Y_{os} = 1/r_d$. It has a very high value.

Transconductance, g_m :

$$g_m = \frac{\text{change on } I_D}{\text{change on } V_{GS}}$$

It is simply the slope of transfer characteristics

$$r_D = \frac{I_D}{V_{GS}} \text{ at constant } V_{DS}$$

at constant V_{GS} or

Its unit is Siemens (S) /mho. It is also called forward transconductance (g_{fs}) or forward transadmittance Y_{FS}. The transconductance measured at I_{DSS} is written as g_{mo}.

Mathematically

$$g_m = g_{mo}\left[1 - \left(\frac{V_{GS}}{V_P}\right)\right]$$

Amplification factor, μ :

It is given by

$$\mu = \frac{\text{change on } V_{DS}}{\text{change on } V_{DS}} \text{ at } I_D \text{ constant or}$$

$$\mu = \frac{V_{DS}}{V_{DS}} \text{ at constant } I_{DS}$$

It can be proved from above that

$$\mu = g_m \times r_D = g_{FS} \times r_D$$

DC drain resistance, R_{DS} :

It is also called the static or ohmic resistance of the channel. It is given by

$$R_{DS} = \frac{V_{DS}}{I_D}$$

Experiment

Objective :

Study of the characteristics of JFET (Junction Field Effect Transistor) in common source configuration and to evaluate:

1. **AC drain resistance**
2. **Transconductance**
3. **Amplification factor**
4. **Drain resistance**

Equipments needed :

1. 2 mm patch cords.

Circuit diagram :

Circuit used to plot different characteristics of transistor is shown in Figure 12.

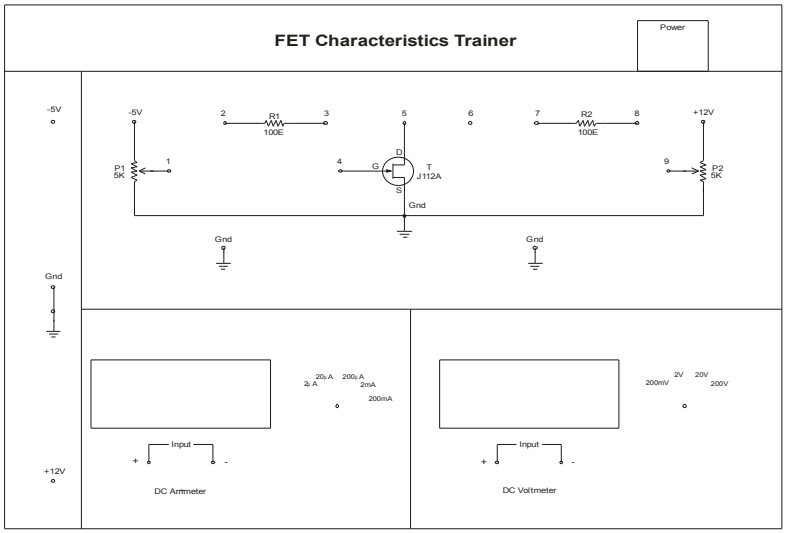


Figure 12

Procedure :

1. Connect 2mm patch cord to -5V and +12V DC power supplies from inbuilt supplies and also connect ground of supplies to common ground.
2. Connect test point 2 of resistance R1 to the potentiometer P1 at test point 1 and another terminal of resistance R1of test point 3 to gate terminal at test point 4.
3. Connect drain terminal of test point 5 to test point 6.
4. Connect test point 8 of resistance R2 to test point 9 of potentiometer P2.
5. **To plot drain characteristics proceed as follows :**

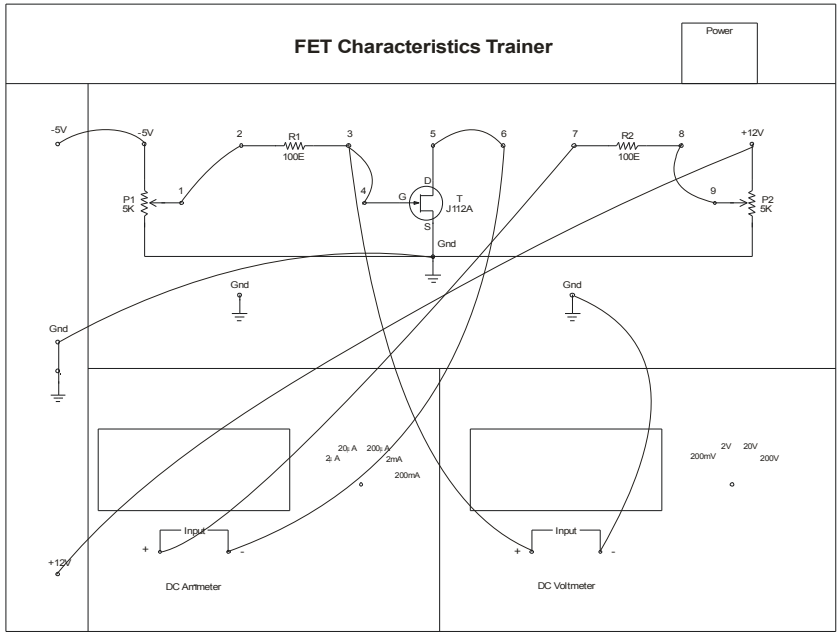


Figure 13

6. Rotate both potentiometers P1 and P2 fully in CCW (counter clock wise) direction.

7. Connect inbuilt DC ammeter between test point 6 and 7, to measure output drain current I_D (mA).

8. Connect positive terminal of inbuilt DC voltmeter to test point 3 and negative terminal to Gnd, to set the value of input voltage V_{GS}.

9. Switch "on" the power supply.

10. Rotate potentiometer P_1 and set the value of input gate to source voltage at some constant value (0V, -1V, -2V, -3V…….).

11. Now disconnect DC voltmeter to test point 3 and Gnd and connect inbuilt DC voltmeter to test point 5 and Gnd to measure output voltage V_{DS}.

12. Vary the potentiometer P2 so as to increase the value of output drain to source voltage V_{DS} from zero to 10V in step and measure the corresponding values of output drain current I_D for different constant values of input gate to source voltage V_{GS}.

13. Rotate potentiometer P2 fully in CCW direction.

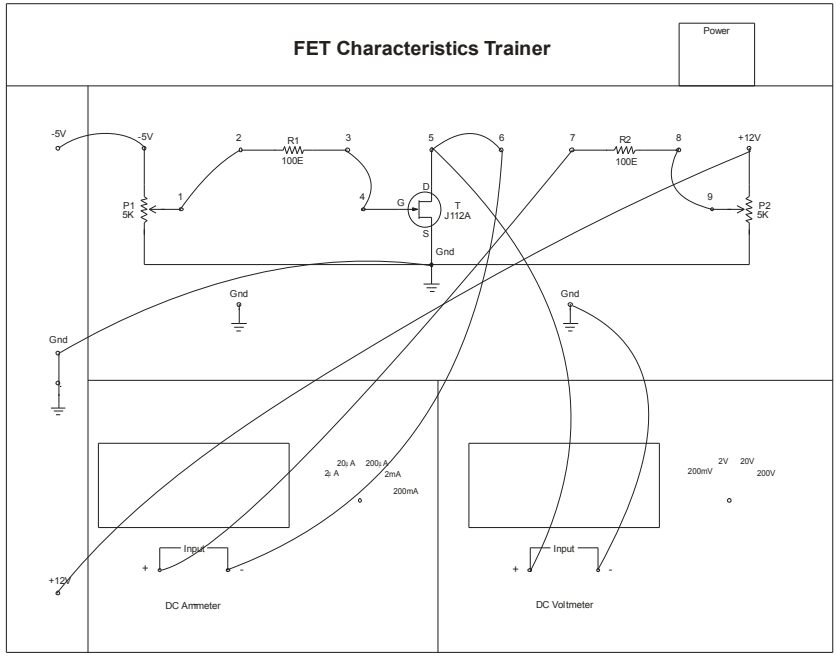


Figure 14

14. Repeat the procedure from step 4 for different sets of input voltage V_{GS}.

15. Plot a curve between output voltage V_{DS} and output current I_D at different constant values of input gate to source voltage as shown in Figure 14. Using suitable scale with the help of observation table 1. This curve is the required output/drain characteristic.

Observation table 1 :

S. no.	Output voltage V_{DS} (volt)	Output Drain current I_D (mA) at constant Value of input voltage			
		V_{GS} = 0V	V_{GS} = -1V	V_{GS} = -2V	V_{GS} = -3V
1.	0.0V				
2.	1.0V				
3.	2.0V				
4.	3.0V				
5.	4.0V				
6.	5.0V				
7.	6.0V				
8.	7.0V				
9.	8.0V				

To plot Transfer characteristic proceed as follows :

1. Switch "off" the power supply.

2. Rotate both potentiometers P1 and P2 fully in CCW (counter clock wise) direction.

3. Connect DC ammeter between test point 6 and 7 as their indicated position to measure output drain current I_D (mA).

4. Connect positive terminal of inbuilt DC voltmeter to test point 5 and negative terminal to Gnd, to set the value of output voltage V_{DS}.

5. Switch "on" the power supply.

6. Vary potentiometer P_2 and set a value of output voltage V_{DS} at some constant value (1 V, 2V, 3V.....).

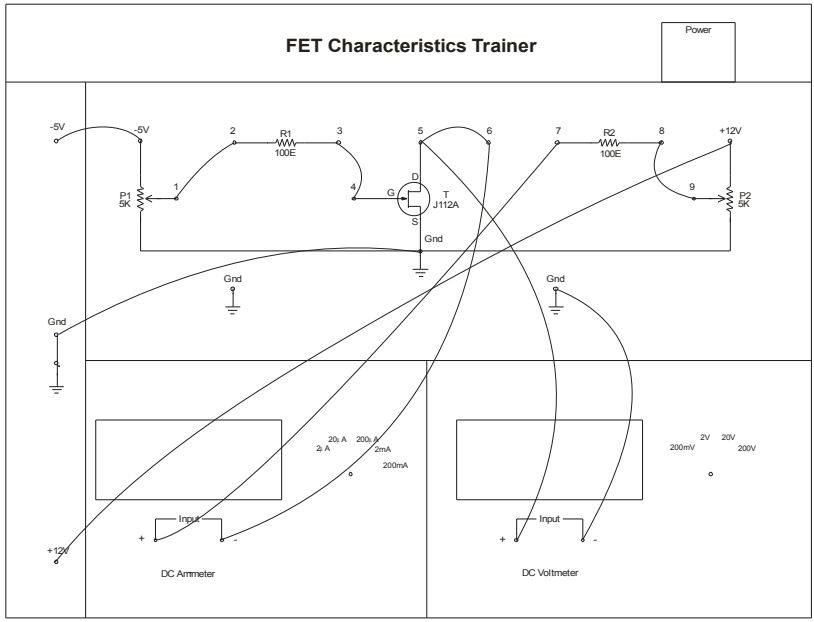


Figure 15

7. Now disconnect DC voltmeter to test point 5 and Gnd.

8. Connect inbuilt DC voltmeter to test point 3 and Gnd to measure input voltage V_{GS}.

9. Vary the potentiometer P_1 so as to increase the value of input voltage V_{GS} from zero to maximum value in step and measure the corresponding values of output current I_D in an observation table 2.

10. Rotate potentiometer P1 in CCW direction.

11. Now disconnect DC voltmeter to test point 3 and Gnd and again connect to test point 5 and Gnd for output drain to source voltage V_{DS} and set at constant value.

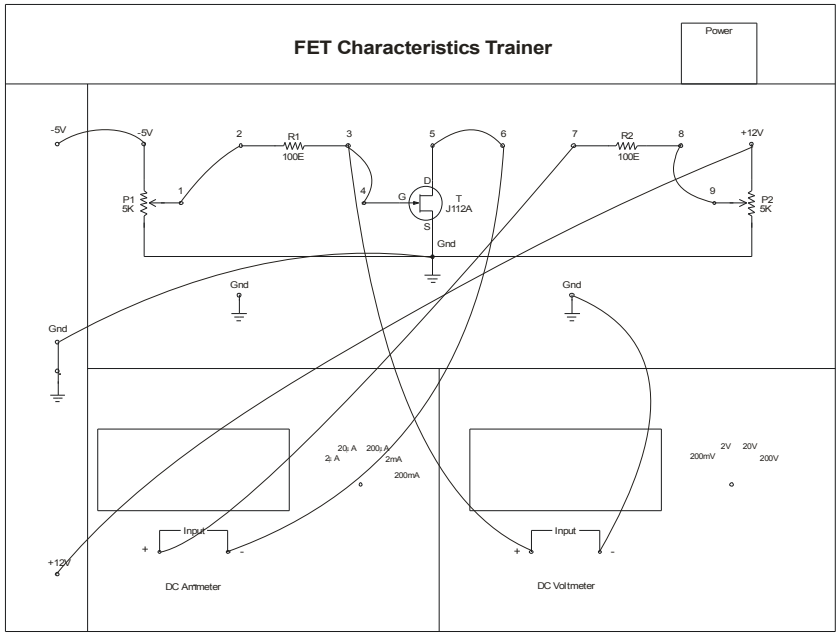


Figure 16

12. Repeat the procedure from step 6 for different sets of output voltage V_{DS}.

13. Plot a curve between input voltage V_{GS} and output current I_D at different constant values of output drain to source voltage as shown in Figure 16. Using suitable scale with the help of observation table 2. This curve is the required transfer characteristic.

Observation table 2 :

S. No.	Input voltage V_{GS} (volt)	Output Drain current I_D (mA) at constant value of input voltage				
		V_{DS} = 1V	V_{DS} = 2V	V_{DS} = 3V	V_{DS} = 4V	V_{DS} = 5V
1.	0.0V					
2.	-0.5V					
3.	-1.0V					
4.	-1.5V					
5.	-2.0V					
6.	-2.5V					
7.	-3.0V					

Calculations :

AC Drain Resistance, r_d :

It is the AC resistance between drain and source terminals when JFET is operating in the pinch-off region. To calculate AC drain resistance calculate the slope of the drain characteristics in the pinch off region obtained from Observation table 1.

$$r_D = \frac{\text{change on } V_{DS}}{\text{change on } I_D} \text{ at } V_{GS} \text{ constant or}$$

$$r_D = \frac{V_{DS}}{I_D} \text{at constant } V_{GS}$$

It has a very high value.

Transconductance, g_m :

To calculate transconductance determine slope of the transfer characteristics obtained from observation table 2.

$$g_m = \frac{\text{change on } I_D}{\text{change on } V_{GS}} \text{ at constant } V_{GS} \text{ or}$$

$$r_D = \frac{I_D}{V_{GS}} \text{ at constant } V_{DS}$$

Its unit is Siemens (S) / mho.

Amplification factor, μ :

It is given by

$$\mu = \frac{\text{change on } V_{DS}}{\text{change on } V_{DS}} \text{ at } I_D \text{ constant or}$$

$$\mu = \frac{V_{DS}}{V_{DS}} \text{ at constant } I_{DS}$$

$$\text{Or } \mu = g_m * r_d$$

DC drain resistance, R_{DS} :

It is also called the static or ohmic resistance of the channel. It is given by

$$R_{DS} = \frac{V_{DS}}{I_D}$$

Results: AC

Drain Resistance r_d = _____

Transconductance, g_m = _____

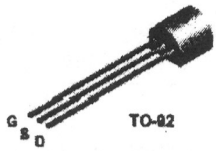
Amplification factor μ = _____

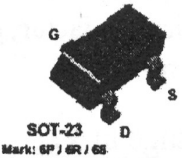
DC drain resistance, R_{DS} = _____

Data Sheets

J111
J112
J113

MMBFJ111
MMBFJ112
MMBFJ113





NOTE: Source & Drain are interchangeable

N-Channel Switch

This device is designed for low level analog switching, sample and hold circuits and chopper stabilized amplifiers. Sourced from Process 51.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	35	V
V_{GS}	Gate-Source Voltage	- 35	V
I_{GF}	Forward Gate Current	50	mA
T_{op}, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		J111-113	*MMBFJ111-113	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

*Device mounted on FR-4 PCB 1.8" X 1.6" X 0.06."

Electrical Characteristics

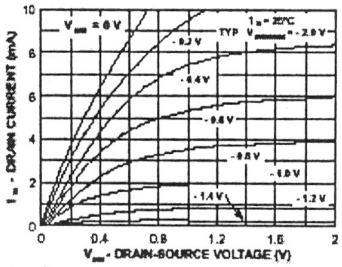
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Max	Units
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = - 1.0 µA, V_{DS} = 0		- 35		V
I_{GSS}	Gate Reverse Current	V_{GS} = - 15 V, V_{DS} = 0			- 1.0	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5.0 V, I_D = 1.0 µA	111	- 3.0	- 10	V
			112	- 1.0	- 5.0	V
			113	- 0.5	- 3.0	V
$I_{D(off)}$	Drain Cutoff Leakage Current	V_{DS} = 5.0 V, V_{GS} = - 10 V			1.0	nA
ON CHARACTERISTICS						
I_{DSS}	Zero-Gate-Voltage Drain Current*	V_{DS} = 15 V, I_{GS} = 0	111	20		mA
			112	5.0		mA
			113	2.0		mA
$r_{DS(on)}$	Drain-Source On Resistance	V_{DS} ≤ 0.1 V, V_{GS} = 0	111		30	Ω
			112		50	Ω
			113		100	Ω
SMALL-SIGNAL CHARACTERISTICS						
$C_{d(gs)}$ $C_{s(gd)}$	Drain-Gate & Source-Gate On Capacitance	V_{ds} = 0, V_{gs} = 0, f = 1.0 MHz			28	pF
$C_{d(gd)}$	Drain-Gate Off Capacitance	V_{ds} = 0, V_{gs} = - 10 V, f = 1.0 MHz			5.0	pF
$C_{s(gd)}$	Source-Gate Off Capacitance	V_{ds} = 0, V_{gs} = - 10 V, f = 1.0 MHz			5.0	pF

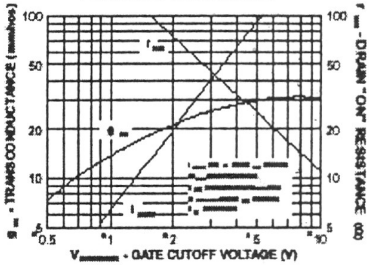
*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 3.0%

Typical Characteristics

Common Drain-Source



Parameter Interactions



Warranty

1. We guarantee the product against all manufacturing defects for 24 months from the date of sale by us or through our dealers.
2. The guarantee does not cover perishable item like cathode ray tubes, crystals, batteries, photocells etc.
3. The guarantee will become void, if
   - **a)** The product is not operated as per instruction given in the instruction manual.
   - **b)** The agreed payment terms and other conditions of sale are not followed.
   - **c)** The customer resells the instrument to another party.
   - **d)** Any attempt is made to service and modify the instrument.
4. The non-working of the product is to be communicated to us immediately giving full details of the complaints and defects noticed specifically mentioning the type, serial number of the product and date of purchase etc.
5. The repair work will be carried out, provided the product is dispatched securely packed and insured. The transportation charges shall be borne by the customer.

List of Accessories

1. 2mm Patch Cord 8” (Red)..... 4 Nos.
2. 2mm Patch Cord 8” (Black) ..... 4 Nos.
3. 2mm Patch Cord 8” (Blue) .....4 Nos.
4. Operating Manual.....1 No.