Design Projects

MILP Neural Network for Machine Learning

Multi-Layer Perceptron Neural Network

- Multi-Layer Perceptron Neural Network
  - A. Design Structure of SLP Neural Network
  - B. Sigmoid Neuron

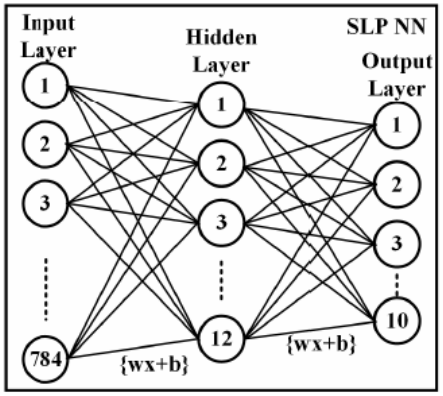


FIGURE 12.18
Design Structure of SLP Neural Network

$$hn_i = \frac{1}{1 + exp(-\sum_{j=1}^{784} wh_{ij} \times x_j - bh_i)}$$

$$on_i = \frac{1}{1 + exp(-\sum_{j=1}^{12} wo_{ij} \times x_j - bo_i)}$$

TABLE 8.2
IEEE 754 Format for FP Numbers

FP	**1.0**	**2.0**	**3.0**	**4.0**	**5.0**	**6.0**
HW	3f800000	40000000	40400000	40800000	40a00000	40c00000
FP	**7.0**	**8.0**	**9.0**	**10.0**	**11.0**	**12.0**
HW	40e00000	41000000	41100000	41200000	41300000	41400000
FP	**-1.0**	**-2.0**	**-3.0**	**-4.0**	**-5.0**	**-6.0**
HW	bf800000	c0000000	c0400000	c0800000	c0a00000	c0c00000
FP	**-7.0**	**-8.0**	**-9.0**	**-10.0**	**-11.0**	**-12.0**
HW	c0e00000	c1000000	c1100000	c1200000	c1300000	c1400000

- Streaming Design on Sigmoid Neurons

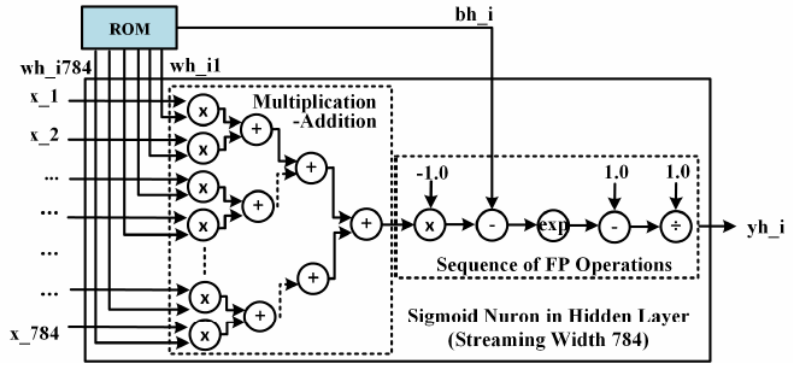


FIGURE 12.19
Streaming Design Structure of Hidden-Layer Neuron

$$hn_i = \frac{1}{1 + exp(-\sum_{j=1}^{784} wh_{ij} \times x_j - bh_i)}$$

$$on_i = \frac{1}{1 + exp(-\sum_{j=1}^{12} wo_{ij} \times x_j - bo_i)}$$

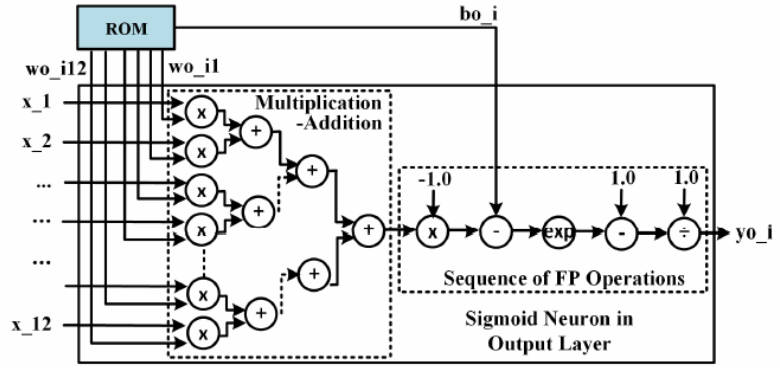


FIGURE 12.20
Streaming Design Structure of Output-Layer Neuron

Project Requirements

- Project #1: Design FP Multiplier-Subtractor (MS)
  - Include the FPU_ls_lib.v into your project
  - Design the fp_ms using the FP multiplier and FP subtractor as design intellectual properties (IPs)
  - Build the simulation environment with test cases below:
    - On input to the FP multiplier is -1.0
    - Feeding in pipelined/consecutive FP 12.0 and -10.0 (dot product) to the multiplier
    - Feeding in pipelined/consecutive FP -2.0 and 2.0 (bias bh_i) to the subtractor

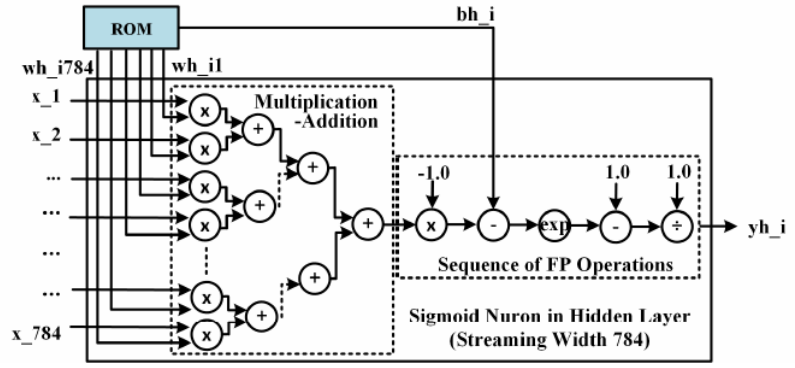


FIGURE 12.19
Streaming Design Structure of Hidden-Layer Neuron

TABLE 8.2
IEEE 754 Format for FP Numbers

FP	1.0	2.0	3.0	4.0	5.0	6.0
HW	3f800000	40000000	40400000	40800000	40a00000	40c00000
FP	7.0	8.0	9.0	10.0	11.0	12.0
HW	40e00000	41000000	41100000	41200000	41300000	41400000
FP	-1.0	-2.0	-3.0	-4.0	-5.0	-6.0
HW	bf800000	c0000000	c0400000	c0800000	c0a00000	c0c00000
FP	-7.0	-8.0	-9.0	-10.0	-11.0	-12.0
HW	c0e00000	c1000000	c1100000	c1200000	c1300000	c1400000

Project Requirements

- Project #2: Design FP sequence of Multiplier-Subtractor-Subtractor-Reciprocal (MSSR)
  - Design the fp_mssr by adding the FP subtractor and FP reciprocal to the Project 1.
  - Build the simulation environment with test cases below:
    - Testing io_a-1.0 for the second FP subtractor
    - Testing 1.0/io_a for the FP reciprocal
    - Feeding in pipelined/consecutive FP 12.0 and -10.0 (dot product) to the multiplier
    - Feeding in pipelined/consecutive FP -2.0 and 2.0 (bias bh_i) to the subtractor

TABLE 8.2
IEEE 754 Format for FP Numbers

FP	**1.0**	**2.0**	**3.0**	**4.0**	**5.0**	**6.0**
HW	3f800000	40000000	40400000	40800000	40a00000	40c00000
FP	**7.0**	**8.0**	**9.0**	**10.0**	**11.0**	**12.0**
HW	40e00000	41000000	41100000	41200000	41300000	41400000
FP	**-1.0**	**-2.0**	**-3.0**	**-4.0**	**-5.0**	**-6.0**
HW	bf800000	c0000000	c0400000	c0800000	c0a00000	c0c00000
FP	**-7.0**	**-8.0**	**-9.0**	**-10.0**	**-11.0**	**-12.0**
HW	c0e00000	c1000000	c1100000	c1200000	c1300000	c1400000

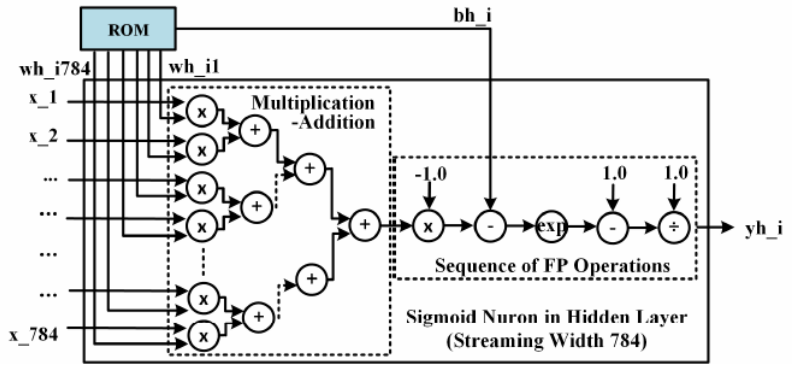


FIGURE 12.19
Streaming Design Structure of Hidden-Layer Neuron

Project Requirements

- Project 3: Design FP Dot Product
  - Include the FPU_ls_lib.v into your project
  - Design the fp_dot using the FP multiplier and FP subtractor as design intellectual properties (IPs)
    - The streaming width is four, meaning the input vector size is 4

$$z = [w0, w1, w2, w3] * \begin{bmatrix} x0 \\ x1 \\ x2 \\ x3 \end{bmatrix}$$

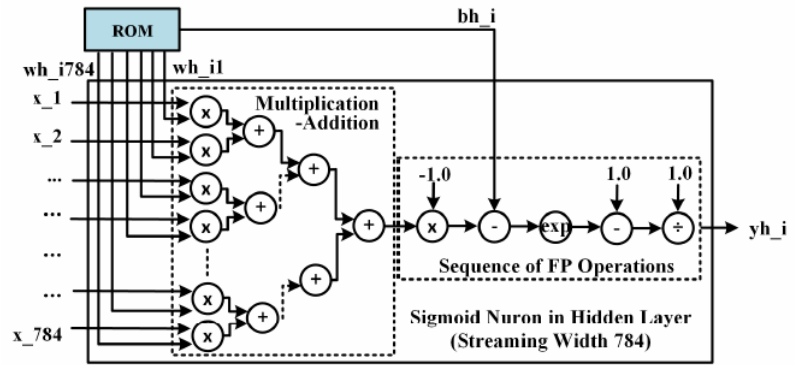


FIGURE 12.19
Streaming Design Structure of Hidden-Layer Neuron

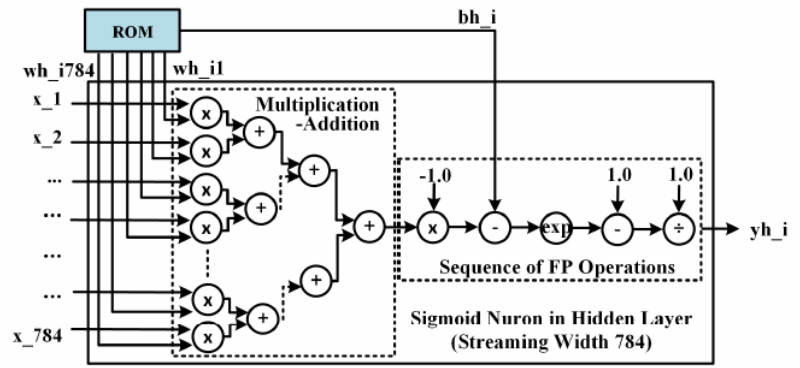
$$hn_i = \frac{1}{1 + exp(-\sum_{j=1}^{784} wh_{ij} \times x_j - bh_i)}$$

Project Requirements

- Project 3: Design FP Dot Product
  - Build the simulation environment with test cases below

$$[w0, w1, w2, w3] * \begin{bmatrix} x0 \\ x1 \\ x2 \\ x3 \end{bmatrix} = [1.0, 2.0, 3.0, 1.0] * \begin{bmatrix} 1.0 \\ 2.0 \\ 2.0 \\ 1.0 \end{bmatrix}$$

$$[w0, w1, w2, w3] * \begin{bmatrix} x0 \\ x1 \\ x2 \\ x3 \end{bmatrix} = [1.0, 2.0, 3.0, 1.0] * \begin{bmatrix} -1.0 \\ -2.0 \\ -1.0 \\ -2.0 \end{bmatrix}$$



$$hn_i = \frac{1}{1 + exp(-\sum_{j=1}^{784} wh_{ij} \times x_j - bh_i)}$$

FIGURE 12.19
Streaming Design Structure of Hidden-Layer Neuron

Project Requirements

- Project 4: Design a sigmoid neuron using the FPUs provided.
  - Integrate project 2 and 3 as the sigmoid neuron
  - Build the simulation environment with two test cases below
    - $[w0, w1, w2, w3] * \begin{bmatrix} x0 \\ x1 \\ x2 \\ x3 \end{bmatrix} = [1.0, 2.0, 3.0, 1.0] * \begin{bmatrix} 1.0 \\ 2.0 \\ 2.0 \\ 1.0 \end{bmatrix}$
    - $[w0, w1, w2, w3] * \begin{bmatrix} x0 \\ x1 \\ x2 \\ x3 \end{bmatrix} = [1.0, 2.0, 3.0, 1.0] * \begin{bmatrix} -1.0 \\ -2.0 \\ -1.0 \\ -2.0 \end{bmatrix}$
    - The bias input bh_i is FP -2.0 and 2.0 for the two dot products, respectively

Evaluation Rubric

- Grading rubric
  - Submit your report and the project to Canvas
    - In the report, screenshot the design code, testbench, and the simulation results
  - Grading policy
    - Introduction and conclusion (2 pts)
    - Design code (2 pts)
    - Testbench (1 pt)
    - Simulation results
      - All the signals must be ***clearly shown*** in the screenshot waveform (2 pts)
      - The FP inputs and outputs must be shown in ***float32*** format (1 pts)
      - The ***correctness*** of the simulation results (2 pts)

Thanks!

CRC Publisher Book: Integrated Circuit Design

Associate Professor, UHCL
yangxia@uhcl.edu

Affiliate Faculty, LBL
xiaokunyang@lbl.gov