Super deterministic:

LLM Models Quantum Measurement

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Chapter 1

AI Observation

Artificial intelligence was once a novel concept theorized by Alan Turing after the publication of his 1936 Princeton Dissertation On "Computable Numbers, with an Application to the Entscheidungs problem" (With support from von Neumann) (Gribbin, 2016); is now one of the most significant technological domain. Coupled with the historic decline in computer memory and storage costs, the necessary components are required to power the Vector databases to fulfill its hunger for data.

The technology at the heart of this epoch rests in Bhargava, Witkowski, Shah, and Thomson's paper titled "What's the Magic Word? A Control Theory of LLM Prompting" [1] allows us to rethink the control structures that interact with the boolean logic, as addressed in Andrea Liu's 2024 Oppenheimer Lecture talk "Particle Systems that can Learn Themselves"[2]

My approach will be holistic. first, describe the Neuron: Its functionality in the body and our abstraction of it. Then, I will briefly describe the Standing waves model for an atom and our quantum abstraction. Next, we will discuss the difference between Quantum Machine Learning vs. Classical Machine Learning. Afterward, I will focus on Designing a Machine Learning System that is capable of training a nematode brain[3] to recursive self-learning through a federated model using the Qiskit framework[4] created and maintained by IBM Research remotely cohered with a classical CMOS ML model using Meta's Llama 3[5]. Then we will explore the possibility of creating an intranet between the University of Southern California's Discover Expedition[6] with The University of Texas at Austin's Quantum Computer [7]

[1]Bhargava, A., Witkowski, C., Shah, M., & Thomson, M. (2024, January 3). What's The magic word? A control theory of LLM prompting. arXiv.org. https://arxiv.org/abs/2310.04444

[2]YouTube. (2024, April 25). The 2024 Oppenheimer lecture featuring Andrea Liu. YouTube. https://www.youtube.com/watch?v=7hz4cs-hGew

[3]OpenWorm. GitHub. (n.d.). https://github.com/openworm

[4]"Qiskit: IBM quantum computing. Qiskit | IBM Quantum Computing. (n.d.). https://www.ibm.com/quantum/qiskit

[5]Meta Llama. (n.d.). https://llama.meta.com/

[6]Home. DiscoverExpedition. (2023, November 3). https://discoverexpedition.usc.edu/

[7]Quantum computing. Quantum Computing | Texas Computing. (n.d.). https://computing.utexas.edu/research/quantum-computing

Chapter 2

LLM Abstraction

Upon observing the words before you the portion of your brain that observes a system that is capable of modeling quantum states, defined as: *The probabilistic outcome determined: upon observing the representational spin of any coherent two-level system.*
According to Kaur, Bagchi, and Pati's paper "Remote Creation of Quantum Coherence via Indefinite Causal Order"[1] is remotely cohered to the system it propagates. When describing Von Neumann's (discredited) theory of hidden Variables Gribbin writes in "Computing with Quantum Cats"[2] "The Copenhagen Interpretation says that even though the evolution of the wave is deterministic, the process of collapse introduces an element of probability into the outcomes of experiments- that is, we can never know perfectly all of the starting conditions."[3] With this intuition, I intend to model a Quantum Messaging System to prove Bell's Inequality

$$S = \langle x \cdot y \rangle_{(0,0)} + \langle x \cdot y \rangle_{(0,1)} + \langle x \cdot y \rangle_{(1,0)} - \langle x \cdot y \rangle_{(1,1)} \leq 2 \tag{2.1}$$

to build upon the Nature article titled "Experimental loophole-free violation of a Bell inequality using entangled electron spins separated by 1.3 km " Hensen, B., Bernien, H., Dréau, A. et al. set up the solution " where $\langle x \cdot y \rangle_{(a,b)}$ denotes the expectation value of the product of x and y for input bits a and b." "Quantum theory predicts that the Bell inequality can be significantly violated in the following setting. We add one particle, for example an electron, to each box. The spin degree of freedom of the electron forms a two-level system with eigenstates $|\uparrow\rangle$ and $|\downarrow\rangle$. For each trial, the two spins are prepared into the entangled state $|\psi^-\rangle = (|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)/\sqrt{2}$. The spin in box A is then measured along direction Z (for input bit $a = 0$) or X (for $a = 1$) and the spin in box B is measured along $(-\mathrm{Z} + \mathrm{X})/\sqrt{2}$ (for $b = 0$) or $(-\mathrm{Z} - \mathrm{X})/\sqrt{2}$ (for $b = 1$). If the measurement outcomes are used as outputs of the boxes, quantum theory predicts a value of $S = 2\sqrt{2}$, showing that the combination of locality and realism is fundamentally incompatible with the predictions of quantum mechanics."

[1] Kaur, J., Bagchi, S., & Pati, A. K. (2023, February 8). Remote creation of quantum coherence via indefinite causal order. arXiv.org. https://arxiv.org/abs/2103.04894

[2] Gu, Mile. "Computing with Quantum Cats: From Colossus to Qubits." AIP Publishing, AIP Publishing, 1 Jan. 2015, doi.org/10.1063/PT.3.2660. ,

[3] Hensen, B., et al. "Experimental Loophole-Free Violation of a Bell Inequality Using Entangled Electron Spins Separated by 1.3 Km." arXiv.Org, 24 Aug. 2015, arxiv.org/abs/1508.05949.

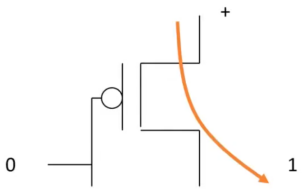
Chapter 3

Quantum Measurement

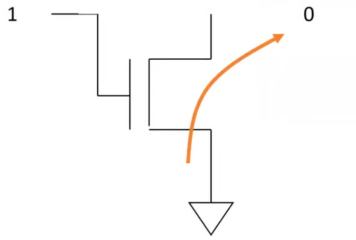
Introduction To computation

- How is Quantum computing compared to Classical Computing

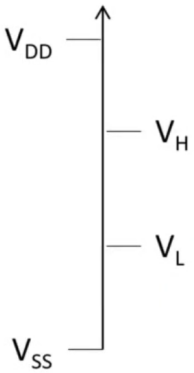
    1. When a voltage propagates a (Classical) transistor we can deterministically record a fault tolerant[1] binary value with a desecrate mechanism.



- Compare and contrast: CMOS. NMOS, Josephson Logic[2]
  When the input is 0, our pull-up transistor (P-type transistor) is on, and that connects the out-



put to the + power supply. When the input is 1 our pull-up transistor comes off, and the pull-down transistor (N-type) comes on. → Connect to Ground

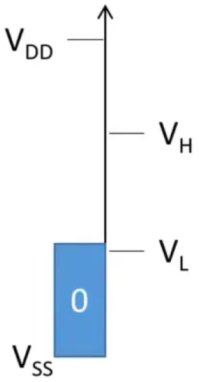


Voltages and Logic levels[3] V_{DD} at the top and V_{SS} at the back. in steady state, V_{SS} the logic levels go to one of the power supply levels (V_{DD} or V_{SS}), but setting a single

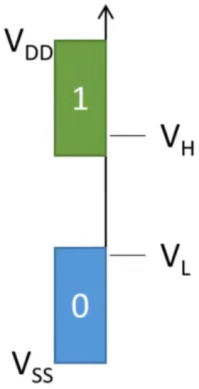
[1] According toDr. William D. Oliver "The error rate is probably better than one part in $10^{-}20$" or 1.0×10^{-20}

[2] ©2016, 2023 Marilyn Wolf All rights reserved. | University of Nebraska | DISCoVER Expedition Seminar Series

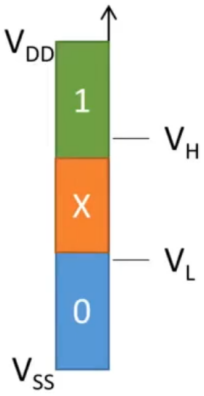
[3] ©2016, 2023 Marilyn Wolf All rights reserved. | University of Nebraska | DISCoVER Expedition Seminar Series



voltage to be a logic level is unwise and entity Impractical. To remedy this, let us develop some ranges for these voltages to represent a logic 0.



Anywhere from V_{SS} (Ground) up to this V_L level. That's a logic 0. Next is our range for a logic 1; from V_{DD} down toV_H. You will notice that there is a gap. We could define V_H and V_L such as those levels touch, But then we will have some possible confusion

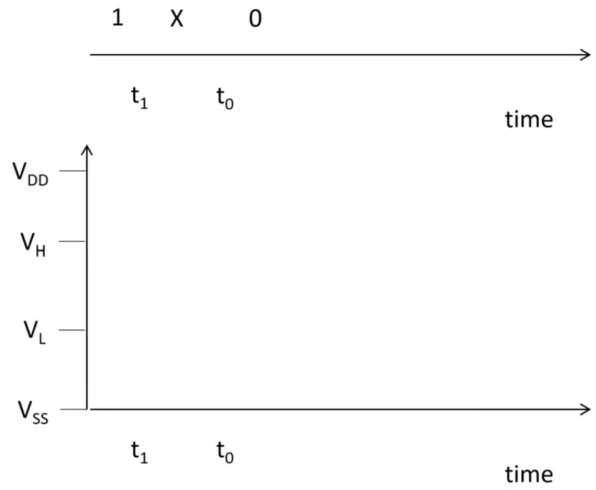


when a signal is right around that transition level. It is better to define a range of unknown values called

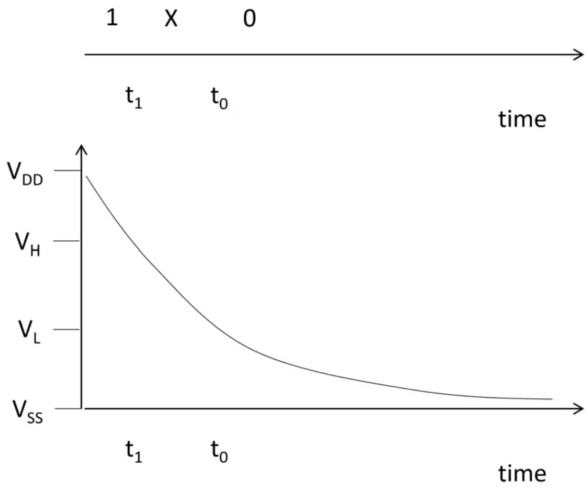
$$X$$

. So, as a logic single transition, it will go from 0 through the X range up to 1. Or from 1 through the x range down to 0. We do not want it to end up in the x range because then we do not know what value the gate wants us to compute, but we do want to have a separation zone between a logic 1 and a logic 0; we don't want a tiny amount of random noise to send us directly from 0 to 1 Voltage waveforms and logic levels[4] We can start to think about how

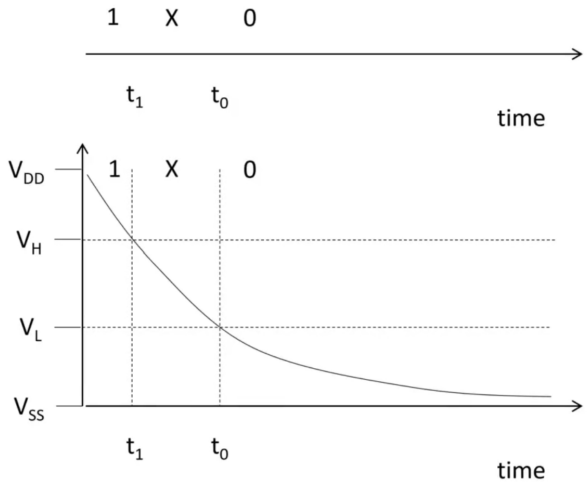
[4]



those logic levels play out with Time. Okay, so we have a time axis here and we can look at this in the discreet space in which we start at



a 1 go through x, and end at 0. We can then look at the continuous singles that are actually what logic singles constitute on a chip.

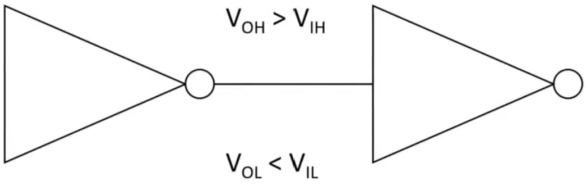


So, in this case, we go down from the high power supply down to V_{SS} and we will cross the boundary between different zone at differing times. You can see that we cross the boundary at t_1 we cross the boundary from logic 1 to logic x. Then at time t_0 we cross the boundary from the x region to the logic 0. So, while taking this continuous signal and extracting it into discrete values from 0, 1, and x, we can assign real value times for these events (when I go from 1 to x or from x to 0). So far, we have only been talking

about one gate; what about two gates? One that talk to another. Logic level compatibility[5]
Noise margins measure compatibility:

$$NM_H = V_{OH} - V_{IH} \tag{3.1}$$
$$NM_L = V_{IL} - V_{OL} \tag{3.2}$$
$$\tag{3.3}$$

I/O LowV_{OL}
I/O HighV_{OH}
Noise-Margin LowNM_L
Noise-Margin HighNM_H



Well, have V output low

$$V_{OL}$$

the output voltage level for the logic 0 from the left-hand gate. We have V output high

$$V_{OH}$$

the output voltage level for the logic 1 for the left-hand gate. We want the right-hand gate to see a logic 0 when its preceding gate sends a 0 and a logic 1 when its preceding gate sends a 1. The input gate has its own levels. It has a voltage level V input low V_{IL} that is the maximum at which that gate will consider that input a 0. We have a V input high V_{IH} that is the maximum at which that gate will consider that input a 1. We want V_{OL} to be below V_{IL}; otherwise, the left-hand gate could think it is sending a 0, but the right-hand gate sees an x. Similarly, We want V_{OH} to be larger V_{IH}; otherwise, if the left-hand gate sends a 1, we don't want the right-hand gate to see an x. So, the difference between output and input levels is called noise-margin.

$$NM$$

We have noise-margin Low

$$NM_L$$

and noise-margin High.

$$NM_H$$

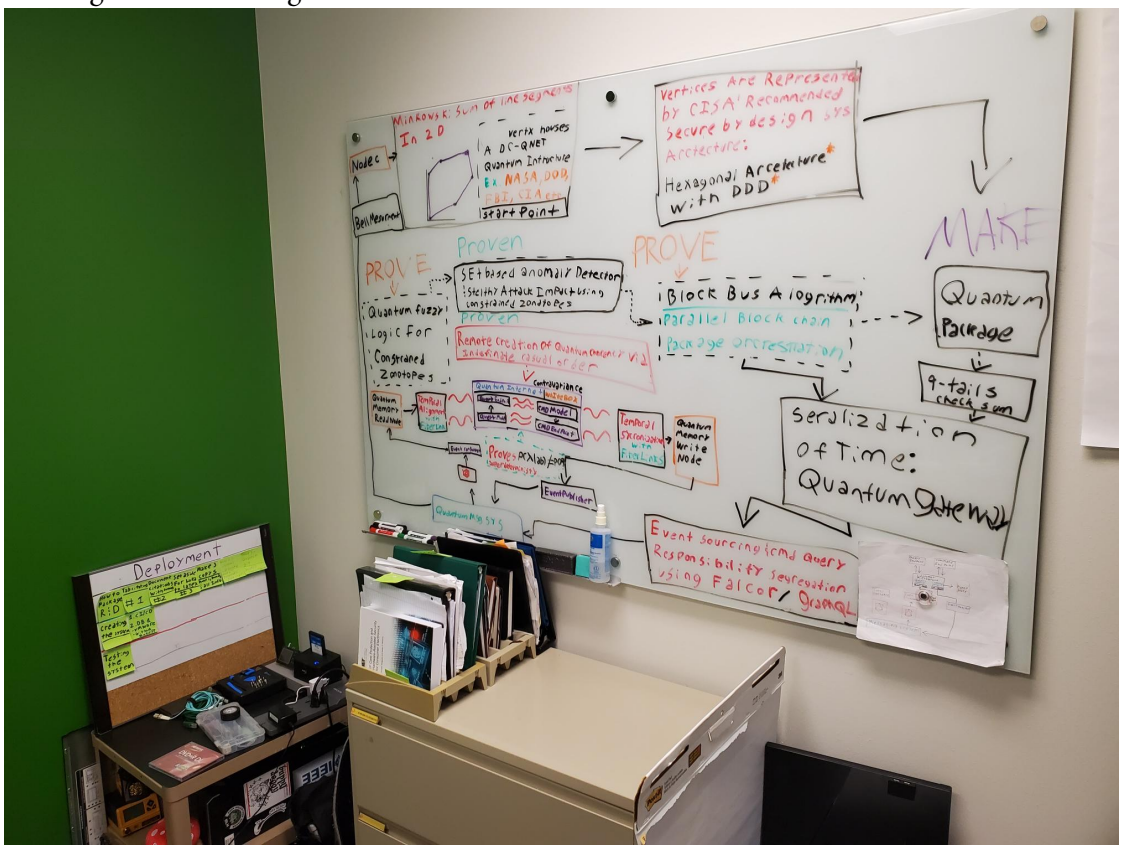
In some of the older logic technologies, high-low noise margins can be very different; they are more symmetric in CMOS. Moving on to more dynamic behavior

[5]

Chapter 4

Open Question: How do we make such a measurement?

Pending Further investigation



Chapter 5

Conclusion

Chapter 6

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Table 6.1: Review Committee Members