

CS:APP Chapter 4

Computer Architecture

Overview

第4章 处理器体系结构 概述



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课程概览 Course Outline



背景 Background

- 指令集 Instruction sets
- 逻辑设计 Logic design

顺序实现 Sequential Implementation

- 一个简单但是不是很快的处理器设计 A simple, but not very fast processor design

流水线 Pipelining

- 让更多的事情同时运行 Get more things running simultaneously

流水线实现 Pipelined Implementation

- 让它发挥作用 Make it work

高级主题 Advanced Topics

- 性能分析 Performance analysis

- 2 - ■ 高性能处理器设计 High performance processor design

覆盖的内容 Coverage



我们的方法 Our Approach

- 针对特定指令集进行设计 Work through designs for particular instruction set
 - Y86-64是Intel x86-64的简化版本 Y86-64 – a simplified version of the Intel x86-64
 - 如果了解一个，或多或少会了解全部 If you know one, you more-or-less know them all
- 工作在“微体系结构”级 Work at “microarchitectural” level
 - 将基本硬件块组装进整个处理器结构中 Assemble basic hardware blocks into overall processor structure
 - » 内存、功能单元等 Memories, functional units, etc.
 - 用控制逻辑驱动以确保每条指令正确地流动 Surround by control logic to make sure each instruction flows through properly

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我们的方法 Our Approach

- 使用简单的硬件描述语言来描述控制逻辑 Use simple hardware description language to describe control logic
 - 可以扩展和修改 Can extend and modify
 - 通过模拟仿真进行测试 Test via simulation
 - 转换设计使用Verilog硬件描述语言 Route to design using Verilog Hardware Description Language
 - » 参见网站旁注: See Web aside ARCH:VLOG

安排 Schedule



Part A

- 指令集体系结构 Instruction set architecture
- 逻辑设计 Logic design

作业: 编写和测试汇编代码程序 *Assignment:* Write & test assembly code programs

Part B

- 顺序实现 Sequential implementation
- 流水线和初始流水线实现 Pipelining and initial pipelined implementation

作业: 增加新指令到顺序实现 *Assignment:* Add new instructions to sequential implementation

Part C

- 让流水线工作 Making the pipeline work
- 现代处理器设计 Modern processor design

作业: 优化程序+流水线以实现性能最大化 *Assignment:* Optimize program+pipeline for maximum performance