IST HOMEWORKS a.y. 24/25

The **GOAL** of the IST homework for this year is the **design**, **fabrication** (i.e., simulation of fabrication in *SPROCESS*), and **verification** (through electrical simulations in *SDEVICE*) of an **SOI Planar transistor.**
The assignments provide you only the transistor gate nominal physical length *Lg*, and the transistor type (*p* or *n*).

The homework is split into three phases **(all mandatory)**:

1) Pen&Paper Design of the assigned SOI transistor depending on your assignment, with the assigned gate length *Lg*. In Fig. 1, you find a figure highlighting a reference structure for the transistor. **The sizes, ratios, and proportions reported there are indicative**.
This is a design, so you have to choose the structure and the sizes of the transistor, you can also choose if and which optimization to add (LDDs, Halos, Metal Gate, silicides, etc …). A very basic and simple structure is accepted for the homework. What you **HAVE TO DO** is to follow the **specifications** of the design, which are the following:

a) **The gate nominal (physical) channel length (*Lg*) has to be the one assigned to your group.**

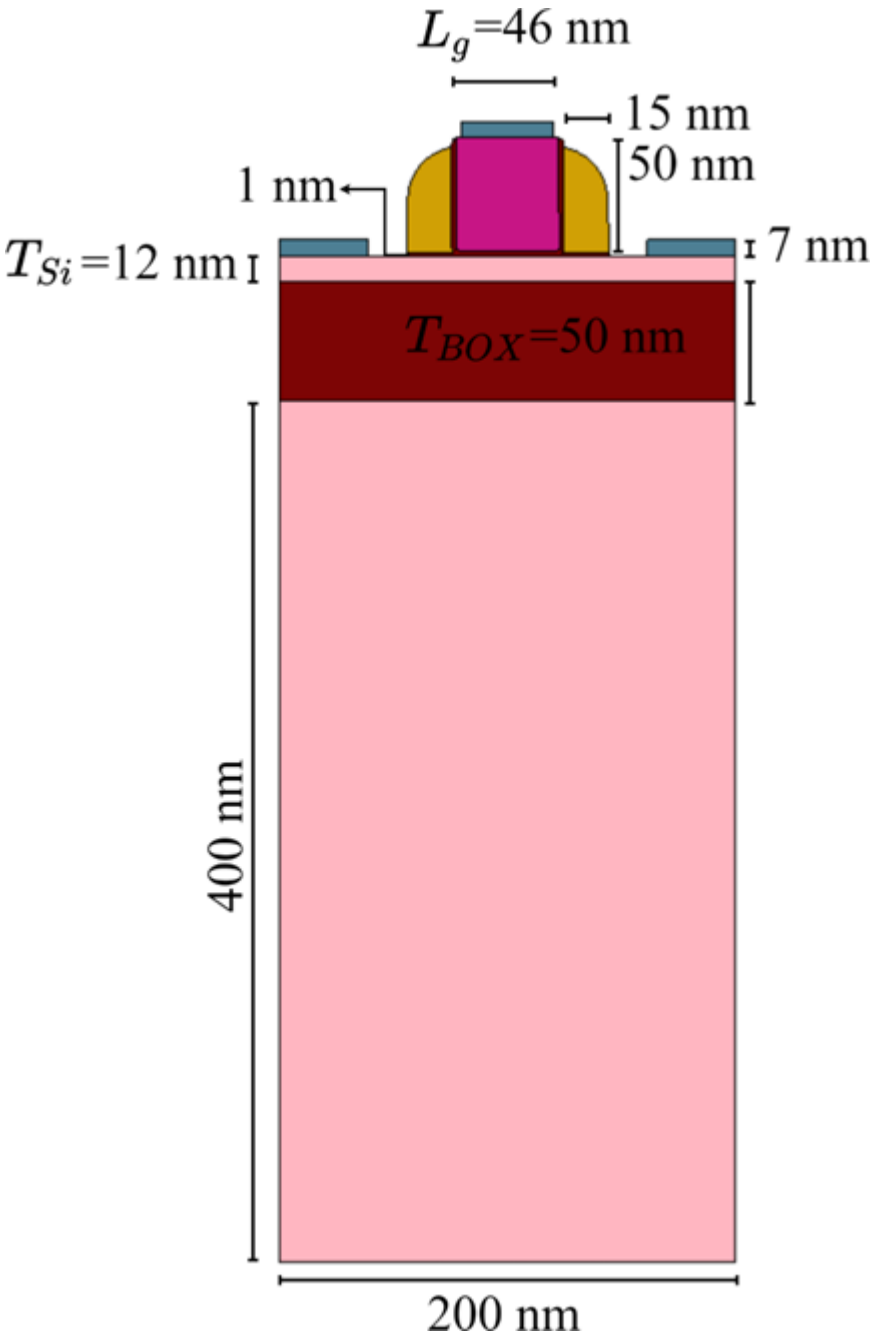
b) **The transistor has to be of the correct type assigned to your group (SOI N-TYPE, SOI P-TYPE).** REMEMBER that SOI transistors have the Buried OXide (BOX) just under the Silicon overlayer (layer in which the planar device is fabricated)!

c) **The transistor has to work, which means the output of the electrical simulation has to correspond to the correct behavior of a transistor assigned to you. It is not requested that you optimize the process to get the best possible performance. Nevertheless, the transistor has to be a transistor :-) i.e. it has to present a relevant modulation of the current thanks to the gate voltage.**

Everything else is left to your choice, on the basis of what you learned during the theoretical lectures of the course. It is up to you to choose if and what advanced techniques exploit to make your transistor work as expected. You can either use the reference structure of this document, look at some technical and scientific papers describing SOI transistors or choose them by yourself because you believe that to be the right choice. There are no wrong choices (as long as the specifications are met), **remember only to motivate each of your choices.**

The motivations behind your design choices must be reported in the final report, otherwise you will incur some penalties in the evaluation.

Fig. 1. REFERENCE SOI STRUCTURE (sizes are just an example!)



2) <u>Simulation of the fabrication process</u> of the transistor using Sentaurus Process. In order to do that use the commands of *sprocess_fps.cmd* of Lab1 (tutorial) as a template. **Obviously, you should modify it to get the desired structure.**

3) <u>Electrical simulation</u> of the device with Sentaurus Device. In order to do that use the commands of *sdevice_des.cmd* of Lab1 (tutorial) as a template.

REQUESTED FILES TO EVALUATE YOUR HOMEWORK:

- **Report:** *pdf* file describing the designed transistor and the design choice that you make. It must also contain the output of the most significant fabrication steps (structure snapshots) and the output of the final physical simulation (transcharacteristic of the device). PLEASE BE SURE THAT IMAGES ARE UNDERSTABLE (e.g. set enough high resolution) :-)

- **Sentaurus simulation files:** zip the command files used to run the simulations: “sprocess_fps.cmd”, “sdevice_des.cmd”.

Please read carefully this document, pay attention also to the correction policy and design/project requirements at the end of the document!

Correction Policy and Requirements:

In the following we specify the fundamental requirements for your project report. We also report the related penalty on the project mark if the requirement is not satisfied.

1. The designed transistor **has to** behave correctly. This means that it must show a **minimum Ion/Ioff ratio of 10^4** as indicated from the IRDS technology roadmap. This is a compulsory requirement, if not satisfied the evaluation is not sufficient. If at the end of your project, the designed transistor does present an Ion/Ioff ratio lower than 10^4 do not try to “hide” it but comment on the possible reasons why this does not happen and how to investigate and ameliorate your device.

The penalty related to this requirement is up to 15% on the project mark.

2. The pen and paper design should be inserted in your final report, together with the design choices and strategies you decide to adopt.

The penalty related to this requirement is up to 10% on the project mark.

3. Always report the design choices and strategies you adopt, the reasons behind the physical parameters you use (e.g. ion implantation dose/energy, …).

The penalty related to this requirement is up to 5% on the project mark.

4. Characterize the obtained transistor through the calculation of the most important figures of merit (Vth, SS, DIBL, Ion/Ioff). Please **specify the conditions and the methods** under which you calculate them and the supply voltage.

The penalty related to this requirement is up to 5% on the project mark.

5. If you obtain unexpected results you should investigate the reasons. To do that you should analyze the simulation results you obtain, e.g. by plotting the mobility, electric field (longitudinal and transversal), carrier concentration, space charge, etc…

The penalty related to uncommented or unjustified unexpected results is up to 5% on the project mark.

6. This is an official technical report, so please avoid grammatical and syntax errors. Furthermore, also the readability and logical implications are important to transmit what you desire to those who read your report.

The penalty related to grammatical errors, wrong theoretical implications/deductions, undefined parameters, wrong/unspecified measurement units is up to 5% on the project mark.

7. You can get the maximum mark (cum laude) of the final project part of the exam by doing the compulsory parts only. You are not required to use advanced processes (e.g. replace metal gate, silicides, …).

Nevertheless, exactly as for the laboratory part, if you use advanced technological processes you can gain extra points, useful to compensate for possible mistakes in the compulsory part. The same holds for additional analyses you decide to perform.

The recompense related to advanced technologies or additional analyses is up to 20% on the project mark.