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DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATIONS
Master's Degree in Electronic Engineering

Integrated Systems Technology
PROJECT REPORT

SOI MOSFET process

and electrical characterization

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Contents

Abstract

This report aims to describe the realization and electrical simulation of a fully depleted Silicon-on-insulator (FD-SOI) MOSFET according to the given specifications. In particular, the report is divided into three parts:

1. pen & paper design of the transistor, depending on the assigned type (n-type) and channel length ($L_{ch} = 60\,nm$) (Section 1);
2. description of the fabrication process of the MOSFET, given the geometrical and physical specifications (Section 2): at first, a very simple and basic structure with poly gate was analyzed; then, a second structure was realized using more advanced techniques in order to optimize the performance and improve the figures of merit of the device;
3. demonstration of the correct behavior of the transistor by performing an electrical simulation that returns the transcharacteristics $V_{gs} \mapsto I_{ds}(V_{gs})$ (Section 3). To analyze the performance of the device, several figures of merit were measured, e.g., the currents I_{on} and I_{off}, the I_{on}/I_{off} ratio, the drain-induced barrier lowering (DIBL) and the subthreshold slope (SS) of the IV characteristics.

To reach these goals, the advanced TCAD tool Synopsys Sentaurus™ was used. This program, which is nowadays the industry standard for the modeling of electronic devices, is a fully featured 2D and 3D device simulator and is composed of many tools handled by a common graphical manager (Sentaurus Workbench, a.k.a. SWB).

In order to carry out the project, only few of them were necessary:

1. the fabrication of the device was carried out using **Sentaurus Process**;
2. electrical simulations were performed with **Sentaurus Device**;
3. analysis and post-processing of the results were performed with either **Sentaurus Visual**, which is particularly useful for the graphical visualization of the results of the various process steps, or **Sentaurus Inspect**, which is more suitable for the analysis of the output of the electrical simulations.

Since Sentaurus only works in Unix environment, the lab session was set up on the server `integratedsystemstech.polito.it`, where the operating system CentOS 7 runs.

1 Pen & paper design

1.1 Specifications

The specifications of the simulated device, whose structure is shown in Figure 1.1, are the following:

- n-type SOI planar MOSFET, with a nominal gate length $L_{ch} = 60\,nm$ and a minimum I_{on}/I_{off} ratio of 10^4, as indicated by the IRDS technology roadmap.

  It is possible to notice that the assigned channel length is approximately the minimum resolution that can be obtained with standard photolithography, so it is not necessary to exploit advanced technological processes, e.g., EUV (Extreme UV photolithography) or SIT (Sidewall Image Transfer).

  Furthermore, L_{ch} is long enough to minimize the impact of SCEs (short-channel effects) such as roll-off and drain-induced barrier lowering (aka DIBL). We are therefore confident about the possibility to obtain satisfactory values for the required FoM;

- a 2D reference frame Oxy is defined so that the x axis identifies the vertical coordinate and the y axis is parallel to the transistor *length*;

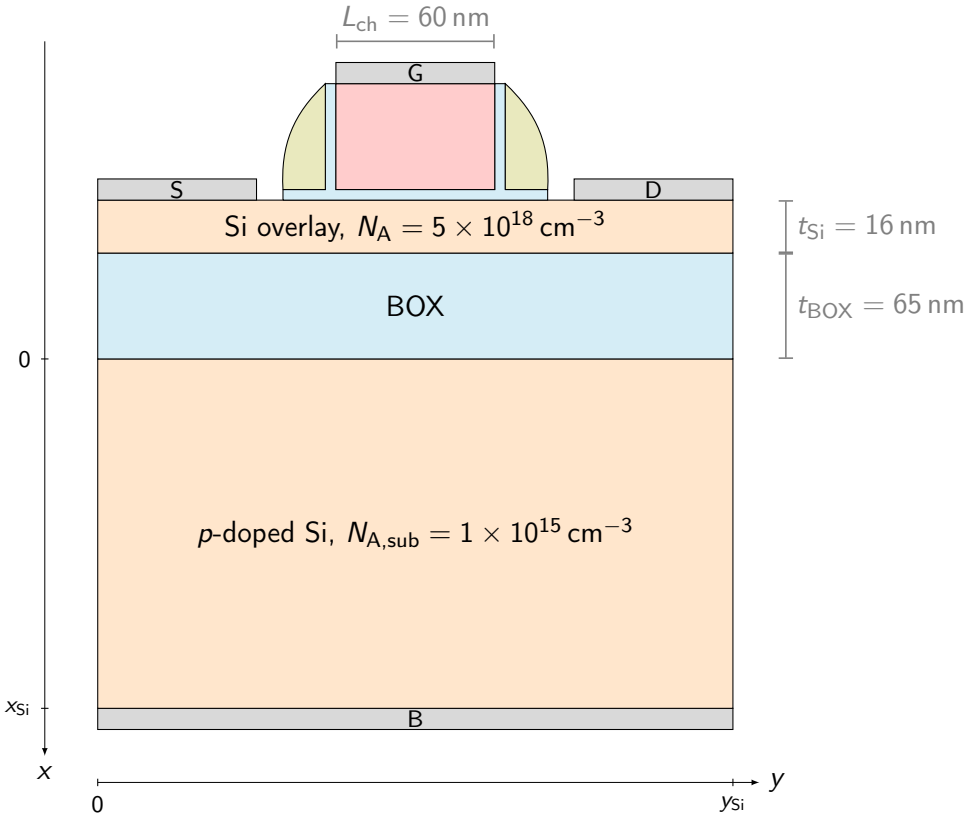


Figure 1.1: Structure for the FD-SOI n-MOSFET.

- $x = 0$ identifies the top part of the substrate and incrementing x corresponds to moving towards the bottom of the substrate;
- $y = 0$ identifies the leftmost part of the substrate and incrementing y corresponds to moving rightwards, i.e., from source to drain;
- the transistor is assumed to be uniform in the along-width direction, so the third coordinate is neglected for the sake of simplicity: in fact, the simulation of a 3D structure has a far higher computational cost than a 2D one.

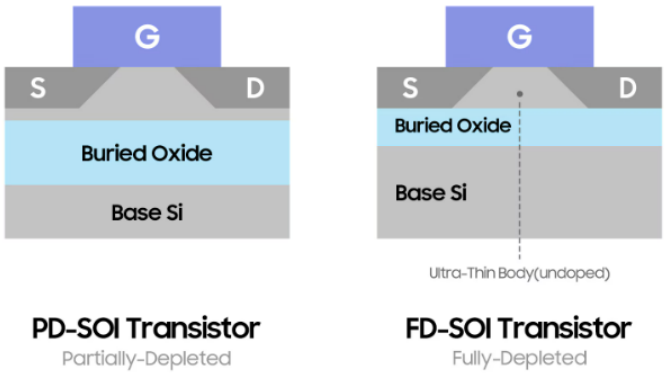
1.2 Design choices

The main design choices that were made during the pen & paper design are here reported. Most geometrical parameters are obtained from the reference structure shown in the text of the project according to the technological scaling rule:

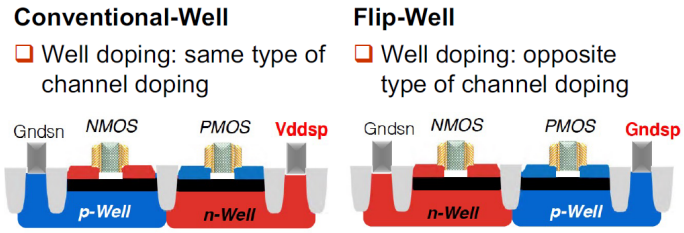
$$d' = \frac{d}{k}, \quad \text{where } \frac{1}{k} := \frac{L'_{ch}}{L_{ch}} \tag{1.1}$$

which is valid for both planar and vertical dimensions and holds irrespectively of the scaling policy (Constant Voltage Scaling, Constant Field Scaling or Generalized Scaling).

Partially or fully depleted SOI. A comparison between partially depleted (PD) and fully depleted (FD) SOI technologies is shown in Figure 1.2a.



(a) PD-SOI vs FD-SOI



(b) Conventional vs flip well

Figure 1.2: Comparison between conventional and flip well UTBB transistors.

Although **PD-SOI** wafers, which are characterized by thickness of the Si overlay $t_{Si} > 100\,\text{nm}$, are easier and cheaper to produce, their main disadvantages are represented by floating-body effect and high S/D parasitic capacitance.

Therefore, the assignment is carried out using **FD-SOI** technology, which is characterized by $t_{Si} < 50\,\text{nm}$ and not only provides better electrostatic control, but is also useful to prevent SCEs.

Conventional or flip well. In UTBB technology, two types of well doping exist depending on the relative doping of substrate and channel, as Figure 1.2b shows.

In **conventional well** technology (left), well doping is the same type of channel doping (both *p*-type for *n*MOS and both *n*-type for *p*MOS); in **flip well** technology, well doping is the opposite type as channel doping.

To optimize the performance of the designed transistor, conventional well doping was chosen. In fact, this technique makes it possible to operate effectively in RBB mode (reverse-body biasing) because the negative body bias range ($V_B < 0$) is wider than the positive one: in these operating conditions, it is possible to:

- strongly reduce I_{off} with respect to nominal conditions ($V_B = 0$), thus "killing" static power consumption;
- slightly increase I_{on} and decrease the threshold voltage V_{th} with respect to nominal conditions ($V_B = 0$). These variations can be exploited either to increase the clock frequency ($f_{ck} \propto I_{on}$) or to decrease dynamic power consumption by scaling V_{dd} ($P_{dyn} \propto V_{dd}^2$).

Gate length. $L_{ch} = 60\,\text{nm}$, assigned by the specifications of the project.

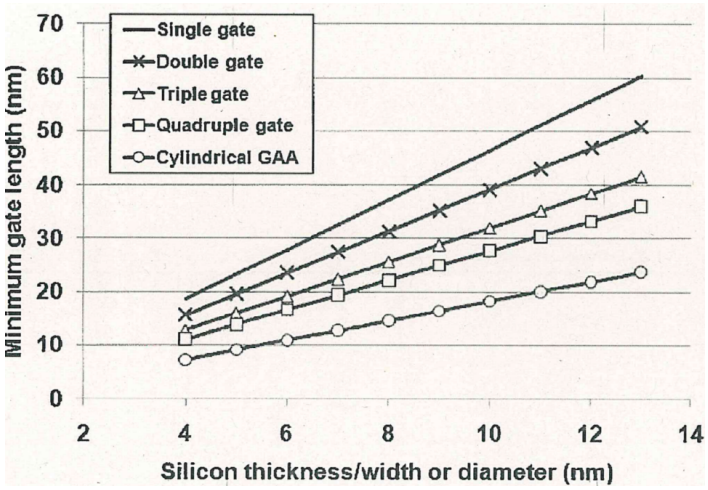
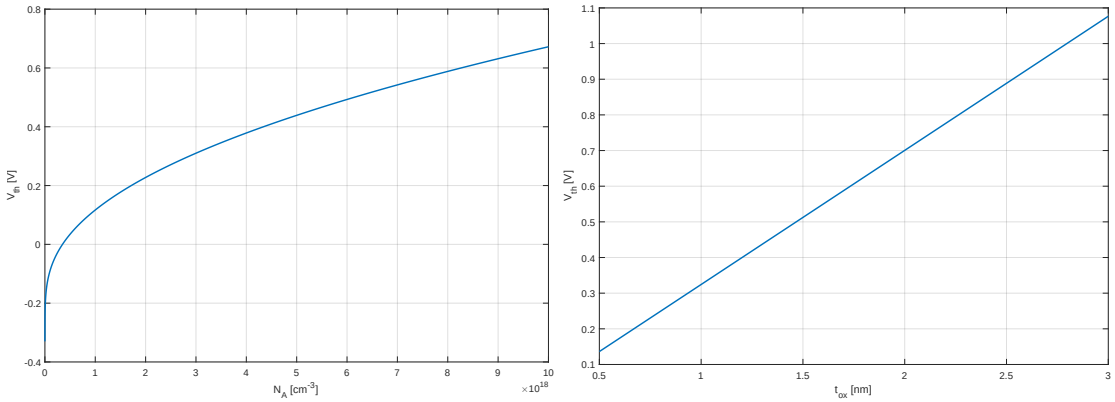


Figure 1.3: Relation between the quantity that determines the electrostatic control of a MOS device (t_{Si} for SOI technology, fin thickness for FinFET technology, nanowire diameter for GAAFET technology) and the minimum gate length that ensures DIBL $< 100\,\text{mV/V}$.



(a) $N_A \mapsto V_{th}(N_A)$, $t_{ox} = 1.3\,\text{nm}$ **(b)** $t_{ox} \mapsto V_{th}(t_{ox})$, $N_A = 5 \times 10^{18}\,\text{cm}^{-3}$

Figure 1.4: Threshold voltage of the transistor as function of the doping of the Si overlay N_A (left) and the oxide thickness t_{ox} (right). Notice that $V_{th} \sim \sqrt{N_A}$ and $V_{th} \sim t_{ox}$.

Buried oxide (BOX) thickness. $t_{BOX} = 65\,\text{nm}$, obtained scaling the reference SOI structure shown in the text of the project.

Si overlay thickness and doping level. $t_{Si} = 16\,\text{nm}$, obtained scaling the reference SOI structure shown in the text of the project and coherent with Figure 1.3 (single gate line), from which we can derive the technological thumb rule:

$$\frac{L_{ch}}{t_{Si}} \approx 4 \tag{1.2}$$

The doping level of the Si overlay is chosen according to the desired value for V_{th}; in fact, the threshold voltage of a *n*MOS transistor is given by the following formula (Figure 1.4):

$$V_{th} = V_{FB} + 2\Phi_p + \gamma_B \sqrt{2\Phi_p} \tag{1.3}$$

where

- $q\Phi_p$ is the distance between the intrinsic Fermi level E_{Fi} and the two quasi-Fermi levels of electrons and holes in the semiconductor:

$$q\Phi_p = E_{Fi} - E_F = k_B T \ln \frac{N_A}{n_i}, \quad \text{where } n_i = 1.45 \times 10^{10}\,\text{cm}^{-3} \text{ at } T = 300\,\text{K} \tag{1.4}$$

- γ_B is the body-effect coefficient:

$$\gamma_B = \frac{\sqrt{2q\epsilon_S N_A}}{C_{ox}} \tag{1.5}$$

- V_{FB} is the flat-band voltage:

$$V_{FB} = -V_{bi} = \Phi_M - \Phi_{sp} = \frac{1}{q}\left[q\Phi_M - q\chi_S - \frac{1}{2}E_g - q\Phi_p\right] \tag{1.6}$$

The larger the channel doping, the higher the threshold voltage, but increasing N_A degrades the device performance in terms of SCE, carrier mobility and dopant fluctuations; a large channel doping will also increase band-to-band tunneling leakage between the body and drain. As a consequence, a reasonable trade-off must be found.

As a starting point, the channel doping $N_A = 1 \times 10^{18}\,\text{cm}^{-3}$ was chosen; the final result that maximizes the device performance is $N_A = 5 \times 10^{18}\,\text{cm}^{-3}$ (see Section 3 for further details).

Gate oxide (GOX) thickness. $t_{ox} = 1.5\,\text{nm}$, obtained scaling the reference SOI structure shown in the text of the project and then rounded.

For the sake of simplicity, at the beginning a standard SiO_2 gate was realized (see Section 2.1), but this solution is not optimal: in fact, to obtain good performance (low V_{th}, high I_{on}), a very low t_{ox} is necessary, increasing the probability of direct tunneling and increasing the leakage gate current:

$$I_{gate} \propto \text{TR} = \exp\left(-\frac{4}{3}\sqrt{\frac{8\pi m^\star}{h^2}}\,\frac{q\Phi_B^{3/2}}{qV_{gs}}\,t_{ox}\right) \tag{1.7}$$

where TR is the *transmission coefficient* for direct tunneling.

To solve this problem, SiO_2 should be replaced by a HK material like HfO_2, that has $\epsilon_{HK} \approx 24 \simeq 6\epsilon_{ox}$ and can provide the same C_{ox} as SiO_2 with a much higher thickness:

$$C_{HK} = C_{ox} \implies \frac{\epsilon_{HK}}{t_{HK}} = \frac{\epsilon_{ox}}{t_{ox}} \tag{1.8}$$

which allows for the definition of the *equivalent oxide thickness* EOT:

$$\text{EOT} \equiv t_{ox} = \frac{\epsilon_{ox}}{\epsilon_{HK}}\,t_{HK} \tag{1.9}$$

This technique is implemented, together with RMG technology, in Section 2.2 (see below for further details on the choice of t_{HK}).

Si substrate dimensions and doping level. $x_{Si} \times y_{Si} = 200 \times 300\,\text{nm}$. x_{Si} is reduced with respect to the text of the project (400 nm) in order to reduce the simulation time, while y_{Si} has been calculated so that gate, spacers and contacts can all be located on the wafer with the correct spacing between the elements.

In order to realize a conventional-well *n*MOS transistor, the substrate is *p*-doped with boron (B) atoms with a doping concentration $N_{A,sub} = 1 \times 10^{15}\,\text{cm}^{-3}$.

Spacers dimensions. $x_{\text{spacer}} \times y_{\text{spacer}} = 65 \times 20\,\text{nm}$, obtained scaling the reference SOI structure shown in the text of the project.

Contact dimensions. $x_{\text{contact}} \times y_{\text{contact}} = 9 \times 60\,\text{nm}$, obtained scaling the reference SOI structure shown in the text of the project.

2 Fabrication process

In this section, the fabrication process of the device is explained in details; as already said, the tool Sentaurus Process (aka SPROCESS) is exploited. The description is divided into two parts:

1. in Section 2.1, the fabrication process for the standard FD-SOI transistor with poly gate is presented; the code for the simulation is reported in Appendix B.1, and snapshots of all the process steps are shown in Appendix B.3;
2. in Section 2.2, the fabrication process for the FD-SOI transistor with RMG technology is presented; the code for the simulation is reported in Appendix C.1, and snapshots of the process steps that differ with respect to the previous implementation are shown in Appendix C.3.

2.1 SOI with poly gate

2.1.1 Mesh definition

The first step in the fabrication process of the MOSFET is the definition of the initial mesh, that will then be refined in the areas of interest for the electrical simulations by means of proper *refineboxes*. Unlike the first lab experience, where a bulk transistor had to be realized, in this case the device under analysis is a SOI transistor, so the mesh of the Si substrate can be coarser.

For this reason, an initial mesh was generated with a spacing of 10 nm along the x axis, up to the position $x = 20\,\text{nm}$, and then gradually increasing until reaching 100 nm for the lower part, which is almost meaningless for the simulation.

As far as the y direction is concerned, a uniform spacing of 20 nm was chosen.

The necessary commands are the following:

```
line x location= 0.0      spacing= 10.0<nm>  tag= SiTop
line x location= 20.0<nm> spacing= 20.0<nm>
line x location= 0.2<um>  spacing= 100.0<nm>  tag= SiBottom

line y location= 0.0      spacing= 20<nm> tag= Mid
line y location= 0.15<um> spacing=20<nm>  tag= Right
```

2.1.2 Wafer definition

Once the mesh is declared, the SOI wafer used for the realization of the transistor must be defined. The substrate is declared as a rectangular region of Si, defined using the tags `SiTop`, `SiBottom`, `Mid` and `Right` specified during the definition of the mesh (Figure B.1).

The necessary commands are the following:

```
region Silicon xlo= SiTop xhi= SiBottom ylo= Mid yhi= Right
init concentration= 1.0e+15<cm-3> field= Boron !DelayFullD
AdvancedCalibration
```

To create the buried oxide and the Si overlay, two steps are needed:

- **Buried oxide** (Figure B.2): deposition of a layer of SiO_2 with thickness $t_{BOX} = 65\,nm$:

```
deposit material= {Oxide} type= isotropic thickness=0.065
```

- **Si overlay** (Figure B.3): deposition of a layer of SiO_2 with thickness $t_{Si} = 16\,nm$ and doping level $N_A = 5 \times 10^{18}\,cm^{-3}$, chosen after many attempts to maximize the performance, as already anticipated in the previous paragraphs and better explained in Section 3:

```
deposit material = {Silicon} type= isotropic thickness=0.016 \
    fields.values= {Boron= 5e18}
```

Notice that this is only an approximation of the actual processes employed for the fabrication of SOI wafers (e.g., SIMOX technology or smart-cut), but an accurate description of these techniques is above the scope of this project. Therefore, the process described above can be considered a reasonable alternative.

Eventually, the following commands are used to perform a remesh operation, that takes into account the fact that the layers added in the subsequent steps will modify the original grid:

```
grid set.min.normal.size= 1.0<nm> set.normal.growth.ratio.2d= 1.5
mgoals accuracy = 1e-5
```

2.1.3 Gate oxide growth

At this point the first difference between the two fabrication process can be appreciated. In the poly-gate transistor a simple dielectric layer of gate oxide needs to be placed right now; for the structure with metal gate in Section 2.2, instead, this step can be postponed as it is part of a different technological process.

The isolation layer of SiO_2 is created by a thermal oxidation of the silicon on the substrate surface. The type of process used is dry as it involves O_2 molecules and features a good control of the thickness. The temperature of 700 °C and the time exposure of 30 seconds allow reaching the desired 1.5 nm thickness (Figure B.4):

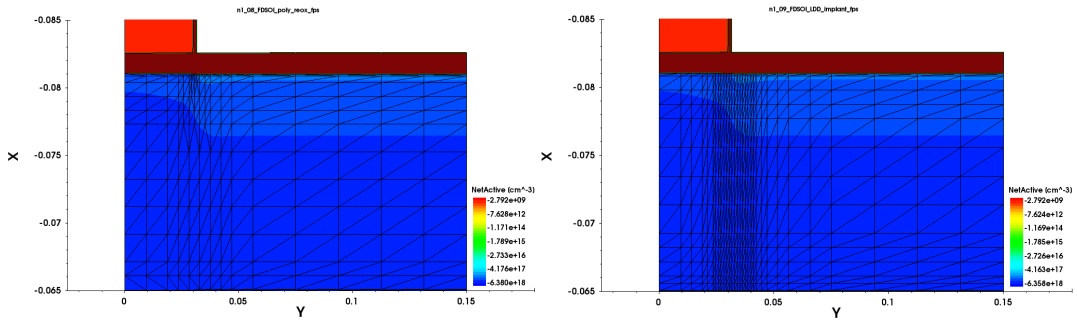
```
diffuse temperature= 700<C> time= 0.5<min> O2
```

2.1.4 Poly-Si gate creation

Above the gate oxide a 65 nm layer of poly-Si is deposited uniformly (Figure B.5). An half channel large mask in positive resist is defined on the left side and the photolithography process shapes half of the gate profile. Then also the SiO_2 is etched, but no mask is needed for this process since the poly-Si itself behaves as mask (Figures B.6 and B.7).

As for the previous laboratories, only half transistor is fabricated to reduce the simulation time, the structure will be mirrored only at the end. The full list of commands is reported down here:

```
deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.065}
mask name= gate_mask left=-1 right= 30<nm>
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.067}
                mask = gate_mask
etch material= {Oxide} type= anisotropic time= 1 rate= {0.002}
```



(a) Before remeshing **(b)** After remeshing

Figure 2.1: Result of the *refinebox* command used just before LDD implantation.

It can be noticed that, even if the gate is 65 nm thick and the SiO_2 is 1.5 nm thick, the poly-Si is etched with a rate of 67 nm/minute and the oxide is etched with a rate of 2 nm/minute, both for 1 minute. This is done to keep into account tolerances and to avoid residual materials.

One final layer of SiO_2, thicker than the gate oxide, is grown over the substrate and over the poly-Si (Figure B.8) to protect them during the upcoming spacers etching process:

```
diffuse temperature= 850<C> time= 0.5<min> O2
```

2.1.5 LDD implantation

After the gate creation, the LDD region is created. Firstly a remeshing must be performed, in order to get a denser mesh in the region interested by the doping process (Figure 2.1). Then the implantation of As is performed, with a dose $N' = 4 \times 10^{13}\,\mathrm{cm}^{-2}$ and an energy of 0.01 keV. These numbers were found after some attempts, starting from the ones used in the first laboratory and doing some optimization iterations until a proper shape of the LDD region was achieved. A rapid thermal annealing is done in the end to activate the dopants (Figures B.9 and B.10):

```
refinebox Silicon min= {-0.081 0.025} max= {-0.065 0.04} \
        xrefine= {0.003 0.005} \
        yrefine= {0.002} add
grid remesh

implant Arsenic dose= 4e13<cm-2> energy= 0.01<keV> tilt= 0 rotation= 0
```

2.1.6 Spacers creation

A 20 nm layer of Si_3N_4 is deposited isotropically over the wafer (Figure B.11). Then anisotropic etching is performed so that a 20 nm thick spacer remains on the side of the gate (Figure B.12). After that, the residual SiO_2 not covered by the spacer is etched (Figure B.13). None of these two etching processes requires a mask, however a mindful choice of the tolerance can avoid oxide residuals like the ones in Figure 2.2:

```
deposit material= {Nitride} type= isotropic time= 1 rate= {0.02}

etch material= {Nitride} type= anisotropic time = 1 rate= {0.025} \
        isotropic.overetch= 0.01

etch material= {Oxide} type= anisotropic time= 1 rate= {0.002}
```

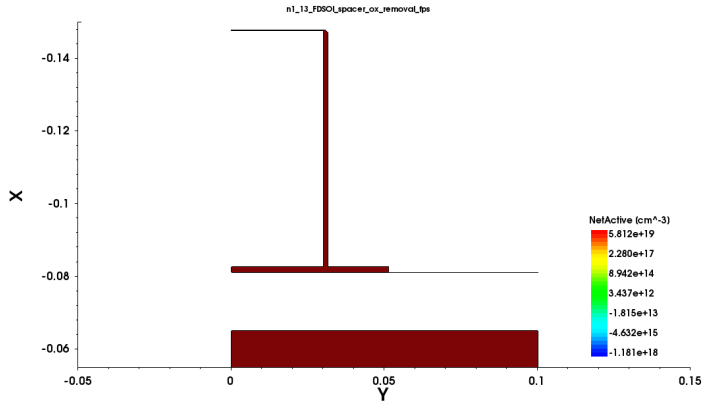


Figure 2.2: Wrong attempt of oxide removal: hiding all the other material, we see that an extremely thin layer of SiO_2 has survived to the etching process.

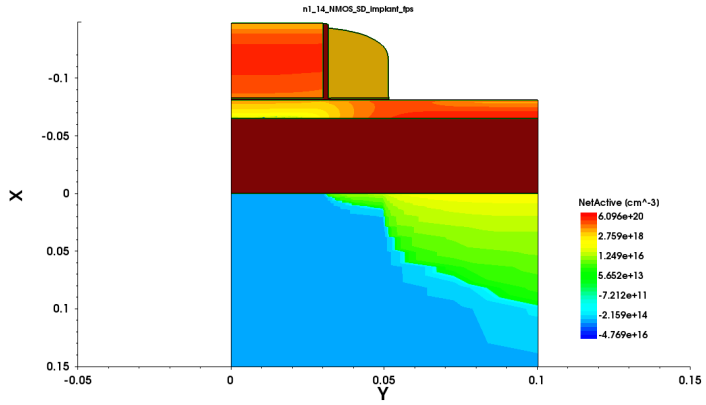


Figure 2.3: One of many wrong attempts of source/drain implantation: a too high implantation energy created a doped region below the buried oxide.

2.1.7 S & D implantation

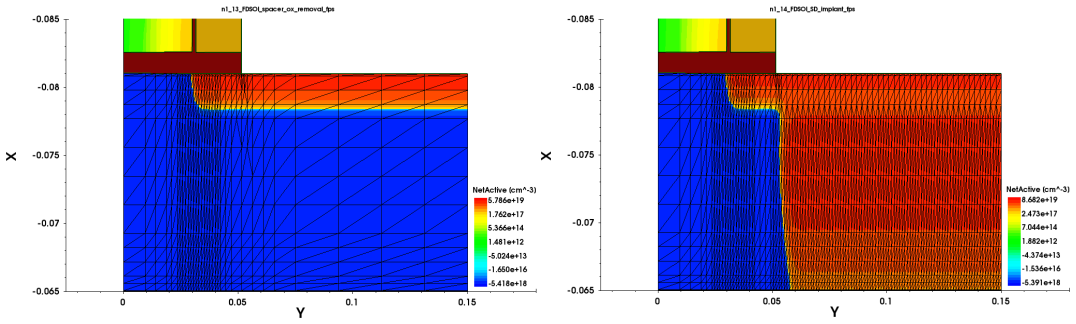
An ion implantation of As and a final rapid thermal annealing are performed to create the source/drain active areas (Figures B.14 and B.15). Preliminarily, another *refinebox* is defined to increase the accuracy of the simulation, as shown in Figure 2.4.

The regions covered by the spacers are protected and they become the source/drain extensions. As for the LDD, also for this implantation the dose and the energy were chosen after many optimization attempts. An example of failed implantation attempt is shown in Figure 2.3:

```
refinebox Silicon min= {-0.076 0.05} max= {-0.065 0.15} \
        xrefine= {0.003 0.005} \
        yrefine= {0.002} add
grid remesh
implant Arsenic dose= 7e13<cm-2> energy= 4<keV> \
        tilt= 7<degree> rotation= -90<degree>
```

2.1.8 Contacts

The last step is the creation of metal contact pads. Two masks are defined, one for the source/drain contact and the other for the gate contact.



(a) Before remeshing **(b)** After remeshing

Figure 2.4: Result of the *refinebox* command used just before S/D implantation.

A 9 nm layer of aluminum is deposited isotropically over the wafer, then a first anisotropic etching is performed using the source/drain contact mask (Figure B.16 and B.17).

At this point, a second isotropic etching is needed, since residual aluminum is present next to the spacers side (Figure B.18).

The gate contact pad is created through an aluminum deposition masked by the gate contact mask (Figure B.19). In the end, the structure is mirrored to get the full transistor:

```
deposit material= {Aluminum} type= isotropic thickness= 0.009
mask name= contacts_mask left= 0.09<um> right= 1.0<um>
etch material= {Aluminum} type= anisotropic thickness= 0.01
                mask= contacts_mask
etch material= {Aluminum} type= isotropic thickness= 0.01
                mask= contacts_mask
mask name= gate_mask2 left=-1 right= 30<nm> negative
deposit material= {Aluminum} type= anisotropic thickness= 0.009
                mask= gate_mask2
transform reflect left
```

2.1.9 Remeshing for device simulation

After the process simulation described in the previous paragraphs, the structure needs to be remeshed for device simulation because the requirements of the device simulator differ from those of the process simulator and, if the mesh is left unchanged, the risk of non-convergence problems is very high.

This step is usually performed using tools of the SWB separate from SPROCESS, e.g., Sentaurus Structure Editor or Sentaurus Mesh, but it is also possible to implement it directly in Sentaurus Process as an add-on to the standard simulation flow. In this way the process is much simpler because there is no need to learn a different syntax tool and coordinates and variables defined within the flow can be exploited.

Before any remeshing operation is performed, it is recommended to cancel the previously designed mesh settings, in order to avoid conflicts between the process and the device mesh; furthermore, the mesh *delaunization*[1] type must be changed from the default conformal type to `boxmethod`, which is more suitable for device simulation. The necessary commands are the following:

[1] Delaunization is an algorithm related to finite-element computation, based on the triangulation of the simulation domain.

```
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines
line clear
pdbSet Grid SnMesh DelaunayType boxmethod
```

Once this step is over, the new mesh can be defined. In principle, the whole structure obtained with SPROCESS should be remeshed accurately because the meshing requirements for process and device simulation are different.

As pointed out in the first laboratory experience, the process mesh should be refined in the zones where gradients of dopant profiles are present; for device simulation, on the other hand, it is advisable to refine the mesh in the active regions important for transport properties, e.g., the channel inversion layer, S/D interfaces, GOX and contacts.

Since this refinement process would have taken too much time, however, it was decided to proceed in a much simpler way: after clearing the old mesh and changing the delaunization type, the *refineboxes* used for the process simulation were redefined, using the following commands:

```
refinebox Silicon min= {-0.081 -0.04} max= {-0.065 -0.025} \
        xrefine= {0.003 0.005} \
        yrefine= {0.002}
refinebox Silicon min= {-0.076 -0.15} max= {-0.065 -0.05} \
        xrefine= {0.003 0.005} \
        yrefine= {0.002}
refinebox Silicon min= {-0.081 0.025} max= {-0.065 0.04} \
        xrefine= {0.003 0.005} \
        yrefine= {0.002}
refinebox Silicon min= {-0.076 0.05} max= {-0.065 0.15} \
        xrefine= {0.003 0.005} \
        yrefine= {0.002}
refinebox Silicon min= {-0.076 -0.02} max= {-0.065 0.02} \
        xrefine= {0.005 0.005} \
        yrefine= {0.005}
grid remesh
```

Although this procedure is not optimal, it indeed allows obtaining enough accurate simulation results.

The last step is contact definition, which in SPROCESS must be performed after remeshing for device simulation. The necessary commands are listed below:

```
contact bottom name = substrate Silicon
contact name = gate x = -0.152 y = 0.0 Aluminum
contact name = source x = -0.085 y = -0.12 Aluminum
contact name = drain x = -0.085 y = 0.1 Aluminum
```

2.2 SOI with RMG

2.2.1 Dummy Poly-Si gate

At the beginning of this presentation (Section 1.2) we have discussed about the advantage of a gate oxide with an higher ϵ_{ox}, the fabrication processes to realize it are described here. Since the substrate is the same as for FD-SOI transistor with poly gate the Figure B.3 can be taken as reference.

This time the Poly-Si is placed directly on silicon and physical variations can happen by chance but it doesn't matter because its purpose is only to fill the gate region and not a technological one. The reoxidation process is required anyway to keep a SiO_2 layer below the spacers (Figure C.1, C.2, C.3), however the command for the material deposition, etching and reoxidation are unchanged:

```
deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.065}
mask name= gate_mask left=-1 right= 30<nm>
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.067} \
                mask = gate_mask
diffuse temperature= 850<C> time= 0.5<min> O2
```

2.2.2 LDD, spacers, S & D implantation

After the creation of the dummy gate structure, the fabrication process proceeds with the exact same steps described for the poly-Si gate transistor:

- LDD implantation and RTA (Figure C.5);
- deposition of Si_3N_4 (Figure C.6);
- anisotropic etching Si_3N_4 to create the spacers (Figure C.7);
- etching of the residual SiO_2 (Figure C.8);
- S/D implantation and RTA (Figures C.9 and C.10).

2.2.3 Gate stack creation

After the S/D implant, anisotropic etching is performed to remove the poly-Si dummy gate and an empty trench remains (Figure C.11).

In the RMG technology, the gate stack can be made with different materials according to the needs. We chose SiO_2 and HfO_2 as dielectrics and tungsten as metal; we also realized a version of the transistor with only SiO_2 as dielectric and W as metal, which is not reported here to avoid redundancy but is addressed in the electrical simulations.

The thickness of the dielectric layers was chosen specifically to get a total equivalent oxide thickness equal to the gate oxide thickness of the poly-Si gate transistor. In this way the RMG transistor and the poly-Si gate transistor have similar thresholds and a meaningful comparison of their figures of merit can be done after the simulation.

We set the thickness of the SiO_2 to 1 nm, the thickness of the HfO_2 is evaluated as follows:

$$t_{ox} = 1.5\,\text{nm} \tag{2.1}$$

$$t_{SiO_2} = 1\,\text{nm} \tag{2.2}$$

$$\text{EOT} = t_{ox} - t_{SiO_2} = 0.5\,\text{nm} = \frac{\epsilon_{SiO_2}}{\epsilon_{HfO_2}} t_{HfO_2} \tag{2.3}$$

$$\epsilon_{SiO_2} = 3.9 \tag{2.4}$$

$$\epsilon_{HfO_2} = 24 \tag{2.5}$$

$$t_{HfO_2} = \frac{24}{3.9} \cdot 0.5\,\text{nm} = 3\,\text{nm} \tag{2.6}$$

To deposit the SiO_2, HfO_2 and tungsten, we exploited the `polygon` command, which allows specifying the points that delimit a region and fills that region with the specified material. We are aware that we are not simulating any physical process by using this command.

At the beginning, we had tried to use the `deposit ... mask` command, but this procedure left every time a thin column of residual material over the oxide next to the spacer. This residual material required a complex etching procedure, therefore we decided to use the `polygon` command for the sake of simplicity, favoring the correctness of the final result over the physical accuracy of the fabrication process.

Issuing the following sequence of commands, firstly a 1 nm layer of SiO_2 is grown (Figure C.12), then a 3 nm layer of HfO_2 is deposited (Figure C.13) and lastly the gate trench is filled with tungsten (Figure C.14):

```
mask name= gate_mask2 left=-1 right= 30<nm> negative
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.067}
                mask = gate_mask2

deposit material= {Oxide} type= polygon
                polygon= {-0.081 0 -0.081 0.03 -0.082 0.03 -0.082 0}

deposit material= {HfO2} type= polygon
                polygon= {-0.082 0 -0.082 0.03 -0.085 0.03 -0.085 0}

deposit material= {Tungsten} type= polygon
                polygon= {-0.085 0 -0.085 0.03 -0.146 0.03 -0.146 0}
```

2.2.4 Contacts

After the RMG process, aluminum contact pads are created with the same commands used for the poly-Si gate transistor. Then the structure is mirrored to get the full RMG transistor (Figure C.15).

2.2.5 Remeshing for device simulation

Similarly to what has been done for the poly-Si gate transistor, a remeshing procedure is performed at the end of the fabrication process to avoid non-convergence problems during the simulation.

3 Device simulation

3.1 Setup of the electrical simulations

We now have to perform electrical simulations to verify the behavior of the fabricated devices, whose complete structures are shown in Figures 3.1, 3.2 and 3.3.

The simulation steps are described in the files reported in Appendix B.2 and C.2. The commands are the same in all the three cases and the outline followed during the simulations is very similar to the one described in the first laboratory report.

The parameters used for the simulations are the following:

- supply voltage $V_{dd} = 2\,V$;
- temperature $T = 300\,K$.

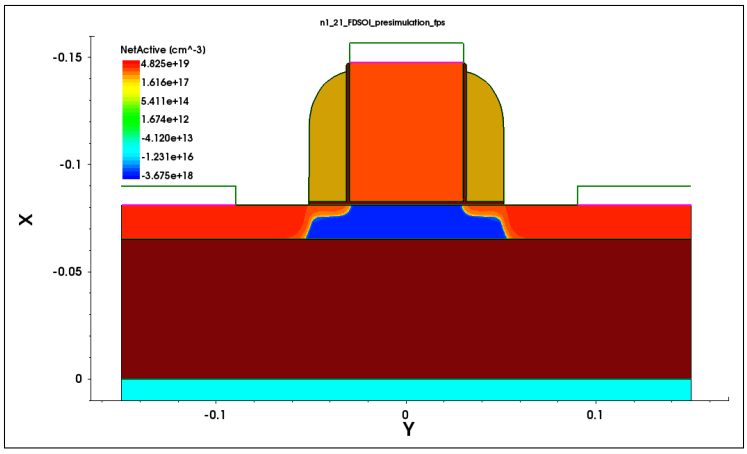


Figure 3.1: Presimulation structure for the FD-SOI transistor with standard poly-Si gate.

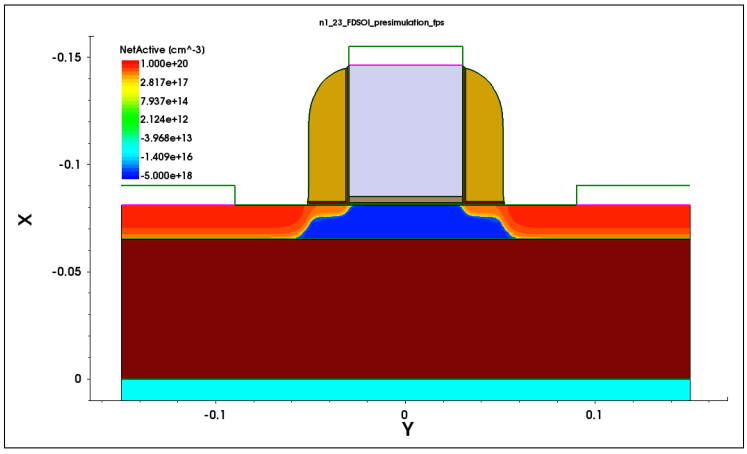


Figure 3.2: Presimulation structure for the FD-SOI transistor with RMG technology and HK gate oxide.

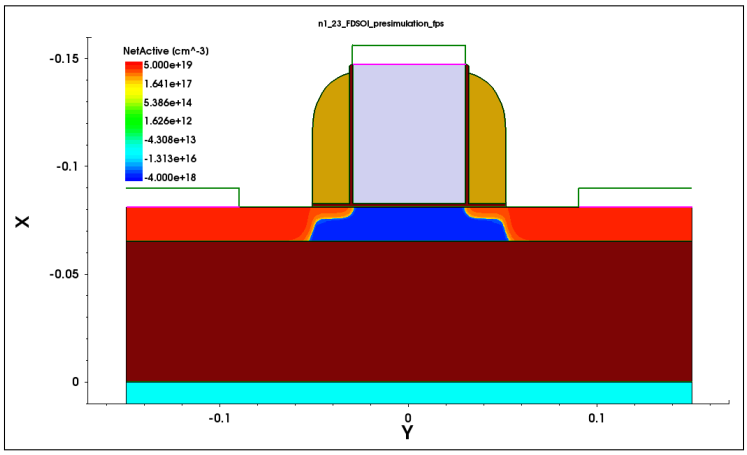


Figure 3.3: Presimulation structure for the FD-SOI transistor with RMG technology and standard SiO_2 gate oxide.

In all cases, we estimated the main figures of merit of the transistor, i.e., I_{on}, I_{off}, I_{on}/I_{off}, V_{th}, SS and DIBL.

The electrical simulations performed to evaluate the performance of the transistors are divided into two parts.

1. First of all, a voltage ramp from 0 to V_{dd} is applied first to the drain and then to the gate electrode. The necessary commands are reported below:

```
quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-6
Goal {name= "drain" voltage = 2})
{coupled { Poisson  Electron Hole }
CurrentPlot ( Time = (range = (0 2) intervals = 200))
Plot(FilePrefix = "IDVD" Time=(2.0))}

quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-6
Goal {name= "gate" voltage = 2})
{coupled { Poisson Electron Hole }
CurrentPlot ( Time = (range = (0 2) intervals = 200))
Plot(FilePrefix = "IDVG" Time=(2.0))}
```

   Notice that, to avoid problems of convergence of Newton's method for solving Poisson's equations, a value of `MinStep=1e-6` is set: at first, the simulator tries to solve these equations with an initial step equal to `InitialStep=0.005`; if the method does not converge, it will attempt again by reducing the it until `MinStep` is reached.

   In this way, it is possible to estimate almost all the required FoM. The **currents** I_{on} and I_{off} can be easily measured starting from their definitions:

$$I_{on} = I_{ds}(V_{gs} = V_{ds} = V_{dd}) \tag{3.1a}$$
$$I_{off} = I_{ds}(V_{gs} = 0, V_{ds} = V_{dd}) \tag{3.1b}$$

   The **threshold voltage** is the point where the second derivative of the $V_{gs} \mapsto I_{ds}(V_{gs})$ characteristic is maximum, while the **subthreshold slope** is the reciprocal of the slope of the $V_{gs} \mapsto I_{ds}(V_{gs})$ characteristic below threshold in logarithmic scale. Both quantities can be calculated either using the calculator provided by Sentaurus Inspect or post-processing the curves with MATLAB™:

$$\mathrm{SS} := \left(\frac{\partial \left(\log_{10} I_{ds} \right)}{\partial V_{gs}} \right)^{-1} \tag{3.2}$$

2. Then, in order to evaluate the **DIBL**, the equilibrium solution of the structure is re-loaded and a new simulation is performed, this time by ramping the drain electrode from 0 up to 0.2 V and then doing the same with the gate electrode from 0 to V_{dd}. The DIBL effect can be estimated by calculating the parameter η, which is the slope of the $V_{th}(V_{ds})$ curve:

$$V_{th}(V_{ds}) = V_{th0} - \eta V_{ds}, \quad \text{where } \eta = \frac{V_{th}(V_{ds} = 2\,\mathrm{V}) - V_{th}(V_{ds} = 0.2\,\mathrm{V})}{2\,\mathrm{V} - 0.2\,\mathrm{V}} \tag{3.3}$$

3.2 Interpretation of the results

The results of all the simulations are reported in Table 3.1 and can be observed in Figures 3.4, 3.5 (poly-gate transistor), 3.7 (RMG transistor) and 3.8.

Table 3.1: Figures of merit of the transistor under analysis, comparison between the results obtained with the standard poly gate and RMG technology.

Version	I_{on} [mA/µm]	I_{off} [µA/µm]	I_{on}/I_{off}	V_{th} [mV]	SS [mV/dec]	DIBL [mV/V]
poly v1	0.883	6.703	1.31×10^{2}	40	120.259	–
poly v2	0.657	1.60×10^{-2}	4.11×10^{4}	220	69.853	–
poly v3	0.416	1.08×10^{-6}	1.99×10^{8}	480	63.996	−22.222
RMG + SiO_2	0.664	8.00×10^{-7}	8.30×10^{8}	480	63.854	−11.111
RMG + SiO_2 + HfO_2	0.571	0.11×10^{-7}	2.70×10^{9}	520	63.968	−11.111

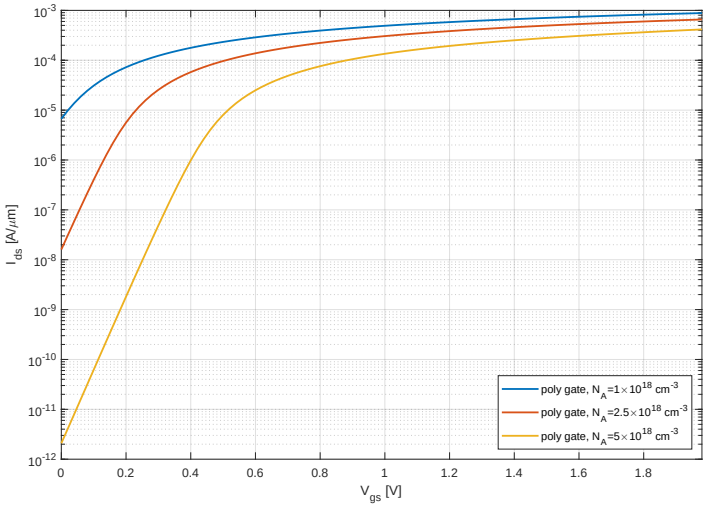


Figure 3.4: Comparison between the transcharacteristics obtained with different levels of the doping concentration of the Si overlay (poly gate).

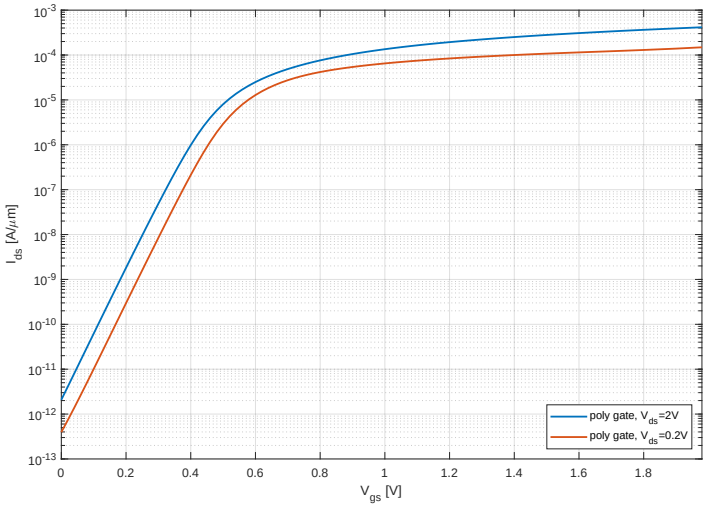


Figure 3.5: Transcharacteristics at $V_{ds} = 2\,V$ and $V_{ds} = 0.2\,V$ in the range $0 \div 2\,V$ (poly v3).

3.2.1 SOI with poly gate

At first, the poly-gate transistor was simulated with Si overlay doping $N_A = 1 \times 10^{18}\,\mathrm{cm}^{-3}$ (poly v1, blue curve in Figure 3.4), with very unsatisfactory results in terms of performance: there is no relevant modulation of the current thanks to the gate voltage and the I_{on}/I_{off} ratio is far from the minimum value of 10^4 imposed by the IRDS roadmap.

To solve this issues, N_A was gradually increased up to the final value $N_A = 5 \times 10^{18}\,\mathrm{cm}^{-3}$ (poly v3, yellow curve in Figure 3.4).

The following facts can be pointed out.

- Consistently with the theoretical considerations of Section 1.2, as N_A increases V_{th} increases as well; compatibly with tolerances and process variations, the final value (poly v3, $V_{th} = 480\,\mathrm{mV}$) is consistent with the result expected from the analytical formula ($V_{th} = 439\,\mathrm{mV}$), evaluated with the MATLAB™ code in Appendix A.

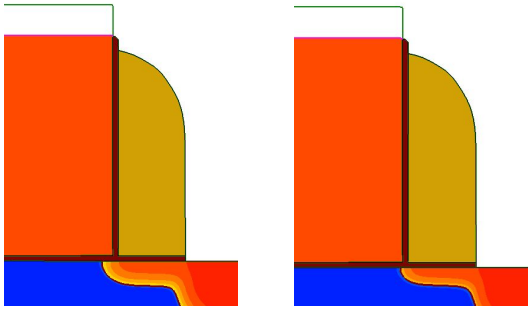
- Thanks to the increase in V_{th}, I_{on} slightly increases from v1 to v3, while I_{off} is significantly reduced, increasing the I_{on}/I_{off} ratio up to 2×10^8 (poly v3). The variations of I_{on} and I_{off} are consistent with the expected theoretical behaviour (I_{on} quadratically increasing with V_{th}, I_{off} exponentially decreasing with V_{th}):

$$I_{on} = \frac{\mu_n C_{ox} W}{2L} (V_{dd} - V_{th})^2 \propto (V_{dd} - V_{th})^2 \tag{3.4}$$

$$I_{off} = \frac{\mu_n C_{dep} W}{L} V_T^2 \exp\left(-\frac{V_{th}}{m V_T}\right) \propto \exp\left(-\frac{V_{th}}{m V_T}\right) \tag{3.5}$$

- As expected by the increase in I_{on}/I_{off}, SS and DIBL get nearer to the ideal values $SS = 60\,\mathrm{mV/dec}$ and $\eta = 0\,\mathrm{mV/V}$.

- From Figure 3.6, we see that when $N_A = 1 \times 10^{18}\,\mathrm{cm}^{-3}$ (poly v1) the extensions are partially overlapped with the region of the channel underlying the gate, while this problem disappears when $N_A = 5 \times 10^{18}\,\mathrm{cm}^{-3}$ (poly v3): this allows for a better electrostatic control of the channel.



(a) poly v1 **(b)** poly v3

Figure 3.6: A small fraction of the LDD region was extended below the gate (left), this issue was solved by increasing N_A (right).

- The main potential problem of such a high N_A is mobility degradation, which is typically solved with strained Si technology[2], not used in this project for the sake of simplicity (the

[2] Growth of a SiGe layer under the transistor (*n*MOS) or implantation of Ge atoms in the S/D diffusions (*p*MOS): since SiGe has a lower lattice constant with respect to Si, this generates a tensile stress in the *n*MOS ($\mu_n \uparrow$) and a compressive stress in the *p*MOS ($\mu_p \uparrow$).

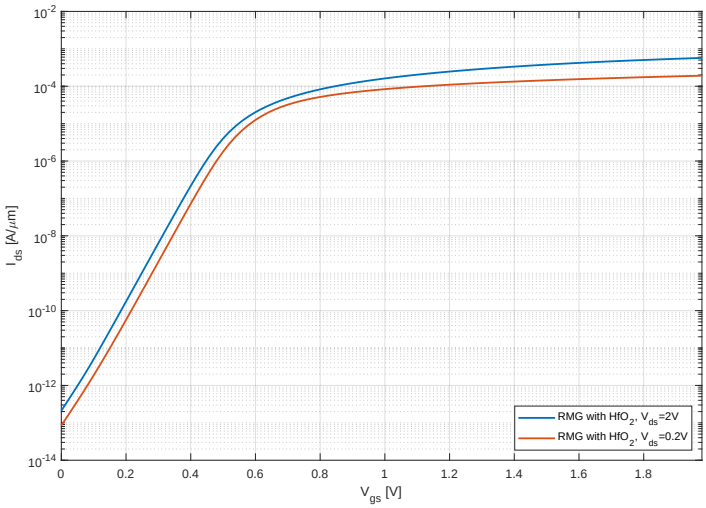


Figure 3.7: Transcharacteristics at $V_{ds} = 2\,V$ and $V_{ds} = 0.2\,V$ in the range $0 \div 2\,V$ (RMG with HfO_2).

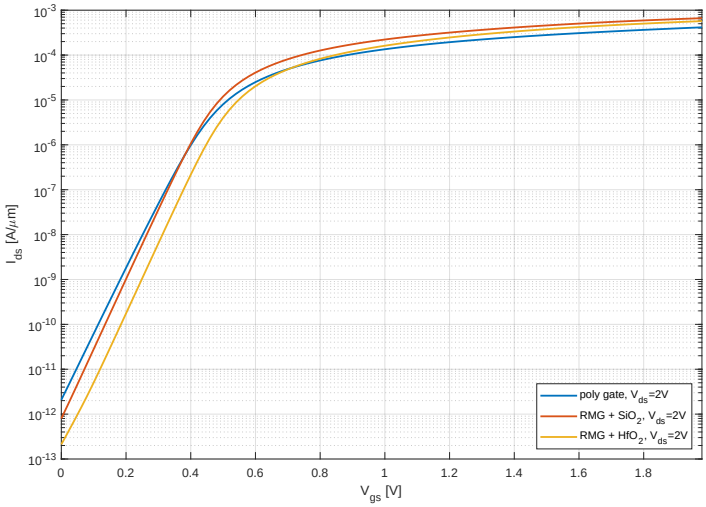


Figure 3.8: Comparison between the transcharacteristics with poly gate and RMG.

results are already very satisfactory).

3.2.2 SOI with RMG

Before simulating the final device, that is the RMG transistor with SiO_2 and HfO_2 as gate dielectrics (as already described in section 2.2), we attempted to fabricate and simulate an RMG transistor using only the SiO_2 as gate dielectric, keeping the same t_{ox} of the poly-Si gate transistor.

We do not report here the fabrication steps for this version of the RMG transistor, firstly because they are almost the same of the other processes already described and then because it was only an attempt, it was performed with the purpose of comparing the performances of poly-Si gate and metal gate under the same conditions.

Today's devices are usually realized using more than one dielectric in the gate stack. In the evolution of MOS technology, poly-Si gates were introduced because metals cannot be used as hard mask, so two independent photolithography processes were required to create the metal gate and S/D implantations, leading to possible misalignments between the gate and the S/D regions.

Poly-Si is a material that can be used as hard mask, making possible to perform auto-aligning S/D implantations. However, metal gates offers better performances than poly-Si gates, especially in terms of gate leakage, that is why RMG technology was introduced in later years.

From Table 3.1 it can be observed that the RMG + SiO_2 transistor has higher I_{on} and lower I_{off} than the poly-Si transistor, as expected. This leads to a 4× increase of the I_{on}/I_{off} ratio, while the two transistors have the same threshold voltage.

The subthreshold slope does not change in a visible way with RMG, the DIBL instead is halved, although it was already low with the poly-Si gate since we are not working with a very short channel transistor.

Finally, the RMG + SiO_2 + chHfO2 transistor proves itself to be the best solution: the I_{off} current is dramatically decreased, leading to a one order of magnitude increase of I_{on}/I_{off}.

The threshold voltage is slightly increased with respect to the poly-Si transistor, although we designed the gate stack in such a way to keep the threshold unchanged (section 2.2.3). The subthreshold slope and the DIBL seem to be not affected by the addition of the HfO_2 layer.

A Theoretical calculations

```
close all,
clearvars,
clc,
format long e

%% Global settings
set(groot, 'defaultLineLineWidth', 1.5)
set(groot, 'defaultAxesXGrid', 'on')
set(groot, 'defaultAxesYGrid', 'on')
set(groot, 'defaultFigurePosition', [400 250 900 600])

%% Reference geometrical parameters
Lch_init = 46; % channel length [nm]
Tsi_init = 12; % Si overlay thickness [nm]
Tbox_init = 50; % BOX thickness [nm]
Tox_init = 1; % GOX thickness [nm]
xsi_init = 400; % [nm]
ysi_init = 200; % [nm]
xspacer_init = 50; % [nm]
yspacer_init = 15; % [nm]
xcontact_init = 7; % [nm]
ycontact_init = Lch_init; % [nm]

%% Scaling of the geometrical parameters
Lch = 60; % [nm]
k = Lch_init / Lch; % scaling factor
Tsi = Tsi_init / k;
Tbox = Tbox_init / k;
Tox = Tox_init / k;

xsi = 200; % for simulation purposes
ysi = ysi_init / k;
xspacer = xspacer_init / k;
yspacer = yspacer_init / k;
xcontact = xcontact_init / k;
ycontact = ycontact_init / k;

fprintf('Channel length Lg = %.0f nm, scaling factor k = %.0f\n', Lch, k);
fprintf('Silicon overlay thickness: Tsi = %.0f nm\n', Tsi);
fprintf('BOX thickness: Tbox = %.0f nm\n', Tbox);
fprintf('GOX thickness: Tox = %.0f nm\n', Tox);
fprintf('Silicon substrate dimensions: xsi x ysi = (%.0f nm) x (%.0f nm)\n', xsi, ysi);
fprintf('Spacers dimensions: xspacer x yspacer = (%.0f nm) x (%.0f nm)\n', xspacer,
yspacer);
fprintf('Contact dimensions: xcontact x ycontact = (%.0f nm) x (%.0f nm)\n', xcontact,
ycontact);

%% Calculation of the expected threshold voltage
tox = Tox * 1e-7; % oxide thickness [cm]
Na = 5e18; % doping Si overlay [cm^-3]
tox_range = linspace(0.5e-7, 3e-7, 1e4);
Na_range = linspace(1e14, 1e19, 1e4);

nint = 1.45e10; % intrinsic concentration Si [cm^-3]
Affinity = 4.05; % [eV]
Eg = 1.12; % [eV]
```

```
kB = 1.380649e-23; % Boltzmann constant [J/K]
qel = 1.602176634e-19; % Elementary charge [C]
c = physconst('LightSpeed') * 1e2; % light velocity [cm/s]
mu0 = 4 * pi * 1e-9; % magnetic permeability of vacuum [H/cm]
eps0 = 1 / (mu0*c^2); % electric permittivity of vacuum [F/cm]
epsR_Si = 11.7; % Si relative permittivity
epsR_SiO2 = 3.9; % SiO2 relative permittivity
epsSi = eps0 * epsR_Si; % Si permittivity [F/cm]
epsSiO2 = eps0 * epsR_SiO2; % SiO2 permittivity [F/cm]
T = 300; % absolute temperature [K]
Vt = kB * T / qel; % thermal voltage [V]

Cox = @(tox) epsSiO2 ./ tox; % oxide capacitance
q_PhiM = Affinity; % workfunction of the poly gate
q_PhiP = @(Na) Vt .* log( Na ./ nint ); % EFi - EF
q_PhiSP = @(Na) Affinity + ( Eg / 2 ) + q_PhiP(Na); % workfunction of the Si overlay
VFB = @(Na) q_PhiM - q_PhiSP(Na); % flat-band voltage
gammaB = @(Na, tox) sqrt( 2 .* qel .* epsSi .* Na ) ./ Cox(tox); % body-effect coeff
threshold = @(Na, tox) VFB(Na) + 2 .* q_PhiP(Na) + gammaB(Na, tox) .* sqrt( 2 *
q_PhiP(Na) ); % threshold voltage

Vth_expected = threshold(Na, tox);
fprintf('Expected threshold: Vth=%.0f mV\n', Vth_expected*1e3);

figure % threshold vs Na with fixed oxide thickness
plot(Na_range, threshold(Na_range, tox))
xlabel('N_A [cm^{-3}]')
ylabel('V_{th} [V]')
exportgraphics(gcf, 'Figures/threshold_vs_Na.pdf')

figure % threshold vs tox with fixed doping level
plot(tox_range*1e7, threshold(Na, tox_range))
xlabel('t_{ox} [nm]')
ylabel('V_{th} [V]')
exportgraphics(gcf, 'Figures/threshold_vs_tox.pdf')
```

B SOI with poly gate

B.1 Command file *sprocess_fps.cmd*

```
# 2D MOSFET UTBB FDSOI (n type, 60 nm technology, conventional well process)
# ------------------------------------------------------
math coord.ucs

# Declare initial grid (half structure)
# ------------------------------------------------------
line x location= 0.0      spacing= 10.0<nm>  tag= SiTop
line x location= 20.0<nm> spacing= 20.0<nm>
line x location= 0.2<um>  spacing= 100.0<nm>  tag= SiBottom
line y location= 0.0      spacing= 20<nm> tag= Mid
line y location= 0.15<um> spacing=20<nm>  tag= Right

# Silicon substrate definition
# ------------------------------------------------------
region Silicon xlo= SiTop xhi= SiBottom ylo= Mid yhi= Right

# Initialize the simulation
```

```
# ------------------------------------------------------
init concentration= 1.0e+15<cm-3> field= Boron !DelayFullD
AdvancedCalibration
struct tdr=n@node@_01_FDSOI_substrate0; # p-type Si substrate

# SOI wafer preparation (BOX + p-type Si overlay)
# Alert: this is only an approximation of the real procedure! (typically smart-cut)
# ------------------------------------------------------
deposit material= {Oxide} type= isotropic thickness=0.065
struct tdr=n@node@_02_FDSOI_box; # buried oxide deposition

deposit material = {Silicon} type= isotropic thickness=0.016 fields.values= {Boron=
5e18}
struct tdr=n@node@_03_FDSOI_soi; # silicon overlay deposition

# Global mesh settings for automatic meshing in newly generated layers
# ------------------------------------------------------
grid set.min.normal.size= 1.0<nm> set.normal.growth.ratio.2d= 1.5
mgoals accuracy = 1e-5

# Gate oxidation
# ------------------------------------------------------
diffuse temperature= 700<C> time= 0.5<min> O2
struct tdr=n@node@_04_FDSOI_tox;

# Poly gate deposition (60 nm channel length)
# ------------------------------------------------------
deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.065}
struct tdr= n@node@_05_FDSOI_gate_dep;

# Poly gate pattern/etch
# anisotropic etching, poly thickness (65 nm) + tolerance (2 nm) to avoid residuals
# ------------------------------------------------------
mask name= gate_mask left=-1 right= 30<nm>
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.067} \
  mask = gate_mask
struct tdr= n@node@_06_FDSOI_gate_poly_etch;

# GOX pattern/etch
# anisotropic etching, GOX thickness (1.5 nm) + tolerance (0.5 nm) to avoid residuals
# ------------------------------------------------------
etch material= {Oxide} type= anisotropic time= 1 rate= {0.002}
struct tdr= n@node@_07_FDSOI_gate_oxide_etch;

# Poly reoxidation
# ------------------------------------------------------
diffuse temperature= 850<C> time= 0.5<min> O2
struct tdr= n@node@_08_FDSOI_poly_reox;

# LDD implantation and diffusion
# ------------------------------------------------------
refinebox Silicon min= {-0.081 0.025} max= {-0.065 0.04} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002} add
grid remesh

implant Arsenic dose= 4e13<cm-2> energy= 0.01<keV> tilt= 0 rotation= 0
struct tdr= n@node@_09_FDSOI_LDD_implant;

```

```
diffuse temperature= 1050<C> time= 0.1<s>
struct tdr= n@node@_10_FDSOI_LDD_diffuse;

# Nitride spacers
# -----------------------------------------------------
deposit material= {Nitride} type= isotropic time= 1 rate= {0.02}
struct tdr= n@node@_11_FDSOI_spacer_dep;

etch material= {Nitride} type= anisotropic time = 1 rate= {0.025} \
  isotropic.overetch= 0.01
struct tdr= n@node@_12_FDSOI_spacer_etch;

etch material= {Oxide} type= anisotropic time= 1 rate= {0.002}
struct tdr= n@node@_13_FDSOI_spacer_ox_removal;

# Source/drain implantation
# -----------------------------------------------------
refinebox Silicon min= {-0.076 0.05} max= {-0.065 0.15} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002} add
grid remesh

implant Arsenic dose= 7e13<cm-2> energy= 4<keV> \
  tilt= 7<degree> rotation= -90<degree>
struct tdr= n@node@_14_FDSOI_SD_implant;

# Final RTA
# -----------------------------------------------------
diffuse temperature= 1050<C> time= 5.0<s>
struct tdr= n@node@_15_FDSOI_SD_diffuse;

# Contacts
# -----------------------------------------------------
deposit material= {Aluminum} type= isotropic thickness= 0.009
struct tdr= n@node@_16_FDSOI_Al_dep; # Aluminium deposition

mask name= contacts_mask left= 0.09<um> right= 1.0<um>
etch material= {Aluminum} type= anisotropic thickness= 0.01 \
  mask= contacts_mask
struct tdr= n@node@_17_FDSOI_Al_anisotropic_etch; # Aluminum anisotropic etching

etch material= {Aluminum} type= isotropic thickness= 0.01 \
  mask= contacts_mask
struct tdr= n@node@_18_FDSOI_Al_isotropic_etch; # Aluminum isotropic etching

mask name= gate_mask2 left=-1 right= 30<nm> negative
deposit material= {Aluminum} type= anisotropic thickness= 0.009 \
  mask= gate_mask2
struct tdr= n@node@_19_FDSOI_gate_contact; # gate contact creation

# Reflect
# -----------------------------------------------------
transform reflect left
struct tdr= n@node@_20_FDSOI_reflect; # Final structure

# Remeshing
# -----------------------------------------------------
refinebox clear
refinebox clear.interface.mats
```

```
refinebox !keep.lines
line clear
pdbSet Grid SnMesh DelaunayType boxmethod

refinebox Silicon min= {-0.081 -0.04} max= {-0.065 -0.025} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.076 -0.15} max= {-0.065 -0.05} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.081 0.025} max= {-0.065 0.04} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.076 0.05} max= {-0.065 0.15} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.076 -0.02} max= {-0.065 0.02} \
  xrefine= {0.005 0.005} \
  yrefine= {0.005}
grid remesh

# Contacts
# -----------------------------------------------------
contact bottom name = substrate Silicon
contact name = gate x = -0.152 y = 0.0 Aluminum
contact name = source x = -0.085 y = -0.12 Aluminum
contact name = drain x = -0.085 y = 0.1 Aluminum
struct tdr= n@node@_21_FDSOI_presimulation
exit
```

B.2 Command file *sdevice_des.cmd*

```
File
{
*INPUT FILES
Grid ="n1_21_FDSOI_presimulation_fps.tdr"
* physical parameters
Parameter = "sdevice.par"

*OUTPUT FILES
Plot = "n@node@_des.tdr"
* electrical characteristics at the electrodes
Current= "n@node@_des.plt"
}

Electrode
{
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="substrate" Voltage=0.0}
}

Thermode
{
{ Name = "source" Temperature = 300 }
{ Name = "drain" Temperature = 300 }
```

```
{ Name = "gate" Temperature = 300 }
{ Name = "substrate" Temperature = 300 }
}

Physics
{
  EffectiveIntrinsicDensity(NoBandGapNarrowing)
  Mobility(DopingDependence,HighFieldSaturation)
  Recombination(SRH)
  Temperature=300
}

Plot
{
  Potential ElectricField/Vector
  eEparallel eEnormal
  hEparallel hEnormal
  eDensity hDensity SpaceCharge
  Affinity IntrinsicDensity
  eCurrent/Vector hCurrent/Vector TotalCurrentDensity/Vector
  eMobility hMobility eVelocity hVelocity
  Doping DonorConcentration AcceptorConcentration
  DonorPlusConcentration AccepMinusConcentration
  ConductionBandEnergy ValenceBandEneergy
  eQuasiFermiEnergy hQuasiFermiEnergy
  eAvalancheGeneration hAvalancheGeneration
  BandGap DielectricConstant
}

Math
{
  Extrapolate
  * use full derivatives in Newton method
  Derivatives
  * control on relative errors
  RelErrControl
  * relative error= 10^(-Digits)
  Digits=5
  * maximum number of iteration at each step
  Iterations=100
  ExitOnFailure
}

Solve
{
############ VDS=2V, VGS sweep 0-2V ##############
  Poisson
  Coupled { Poisson Electron Hole  }
  Plot(FilePrefix="equil")

quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-6
Goal {name= "drain" voltage = 2})
{coupled { Poisson  Electron Hole }
CurrentPlot ( Time = (range = (0 2) intervals = 200))
Plot(FilePrefix = "IDVD" Time=(2.0))}

quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-6
Goal {name= "gate" voltage = 2})
{coupled { Poisson Electron Hole }
```

```
85  CurrentPlot ( Time = (range = (0 2) intervals = 200))
86  Plot(FilePrefix = "IDVG" Time=(2.0))}
87
88  ############ VDS=0.2V, VGS sweep 0-2V ##############
89    Load(FilePrefix= "equil")
90
91  NewCurrentPrefix = "IDVD_VD0d2_"
92  quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-6
93  Goal {name= "drain" voltage = 0.2})
94  {coupled { Poisson  Electron Hole }
95  CurrentPlot ( Time = (range = (0 0.2) intervals = 200))
96  Plot(FilePrefix = "IDVD_VD0d2_" Time=(2.0))}
97
98  NewCurrentPrefix = "IDVG_VD0d2_"
99  quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-6
100 Goal {name= "gate" voltage = 2})
101 {coupled { Poisson Electron Hole }
102 CurrentPlot ( Time = (range = (0 2) intervals = 200))
103 Plot(FilePrefix = "IDVG_VD0d2_" Time=(2.0))}
104 }
```

B.3 Process steps

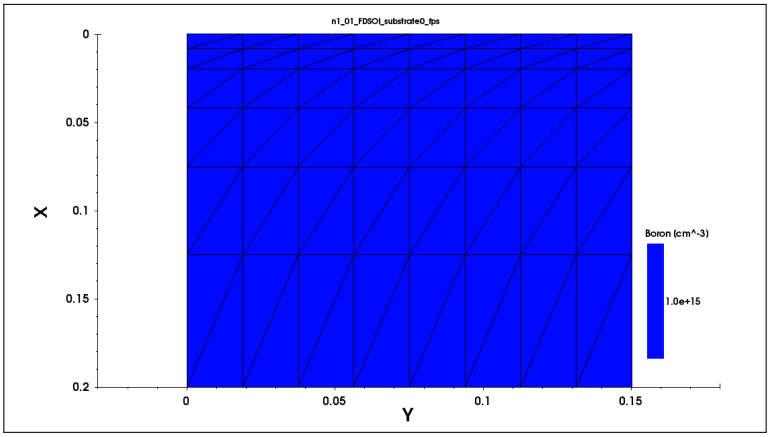


Figure B.1

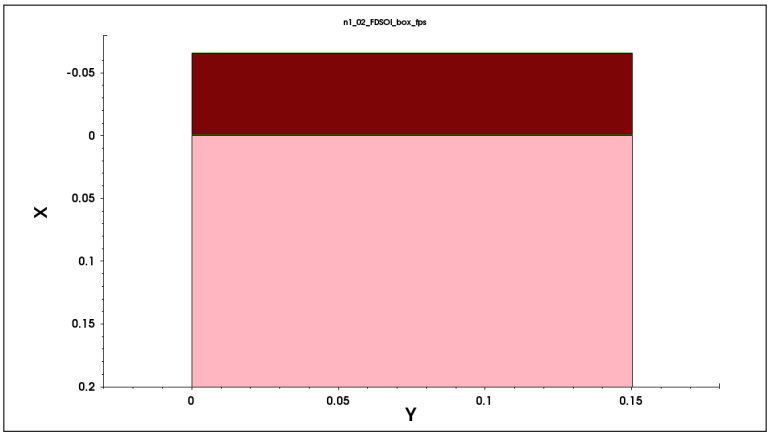


Figure B.2

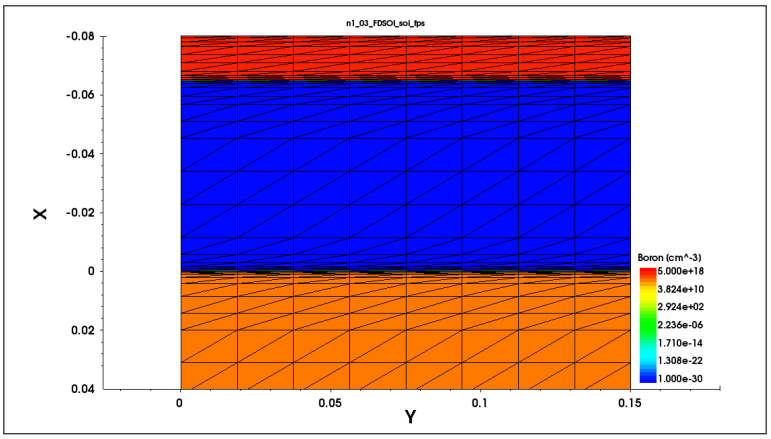


Figure B.3

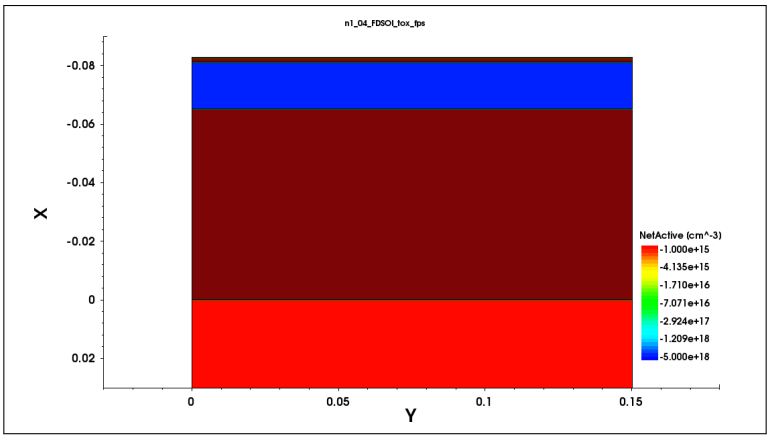


Figure B.4

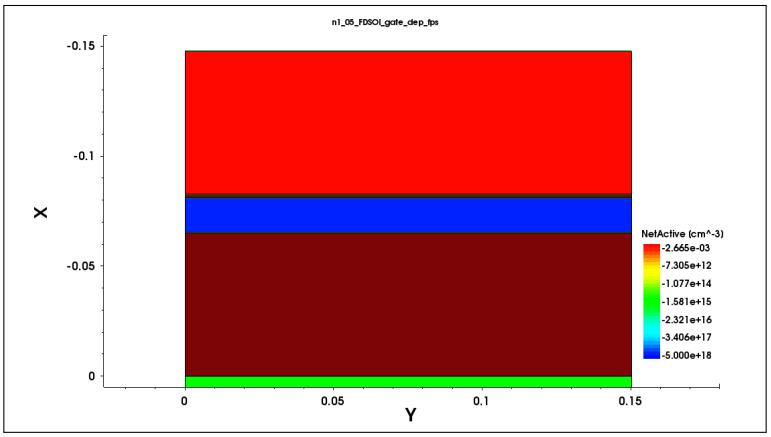


Figure B.5

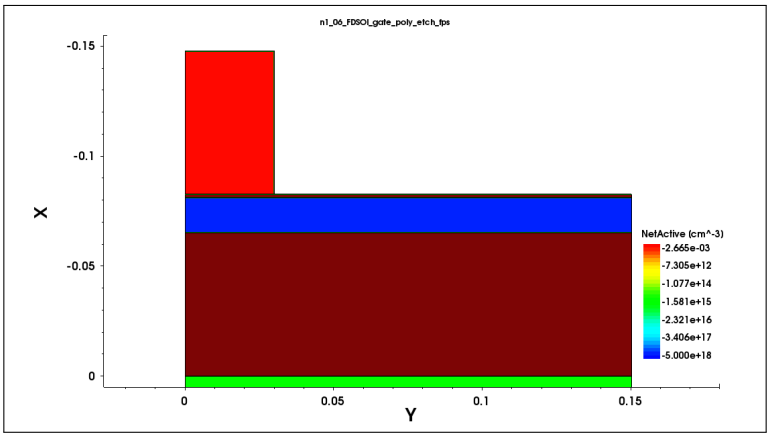


Figure B.6

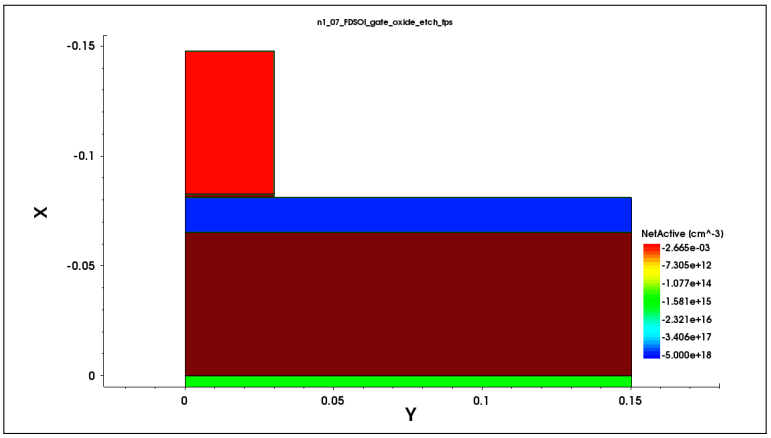


Figure B.7

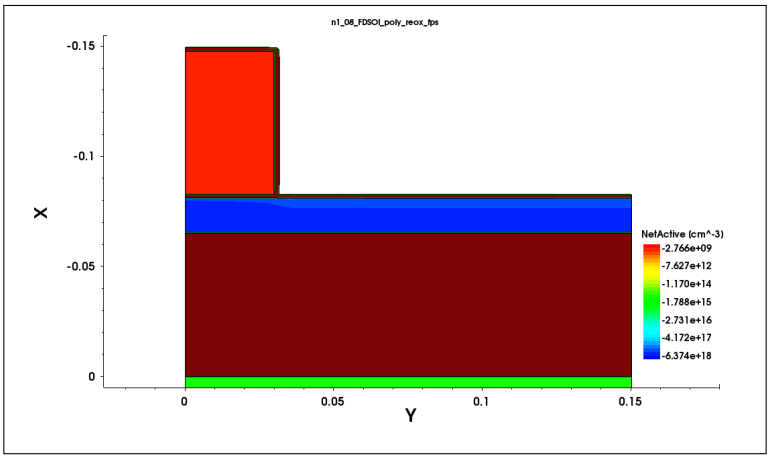


Figure B.8

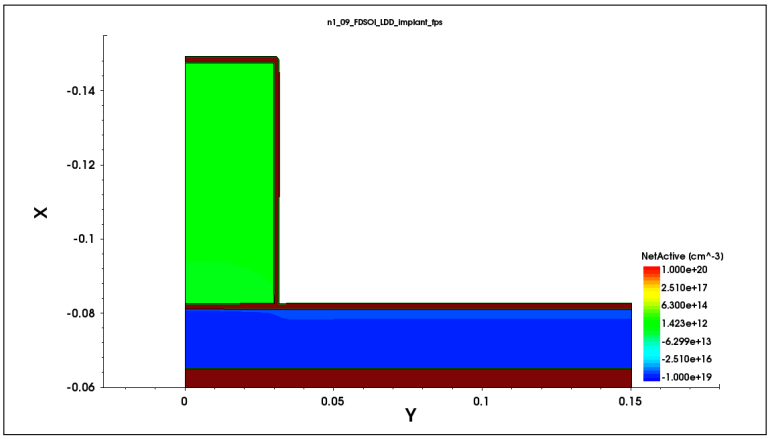


Figure B.9

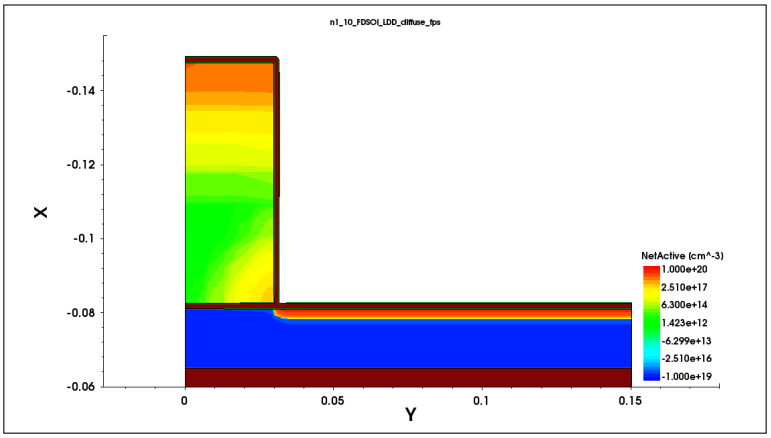


Figure B.10

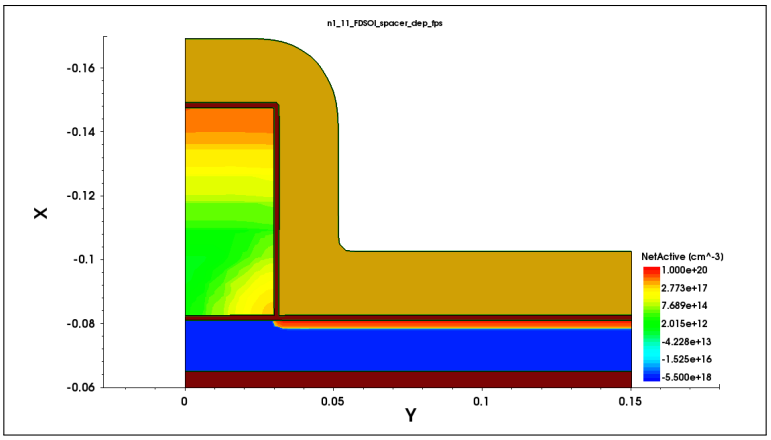


Figure B.11

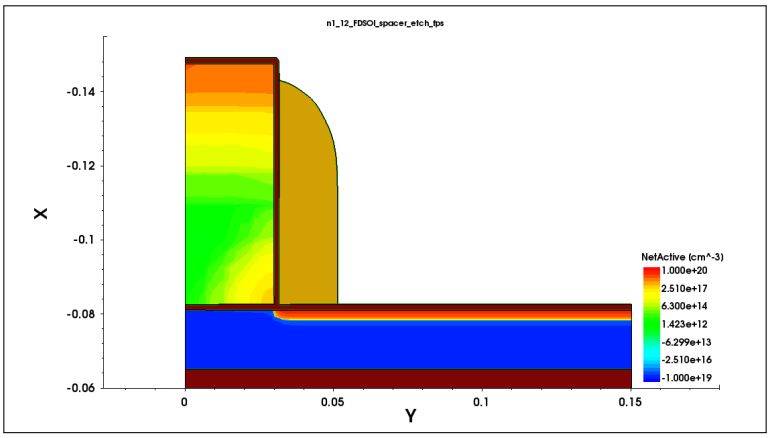


Figure B.12

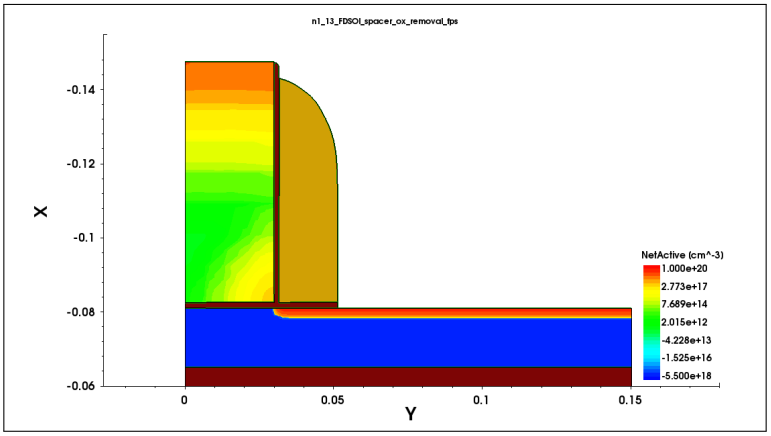


Figure B.13

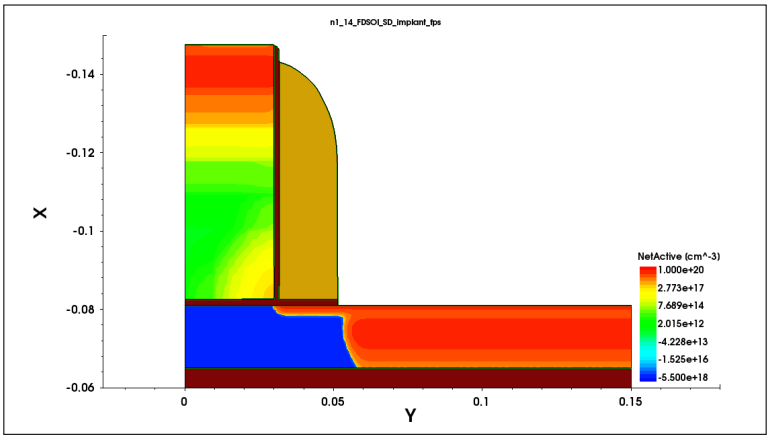


Figure B.14

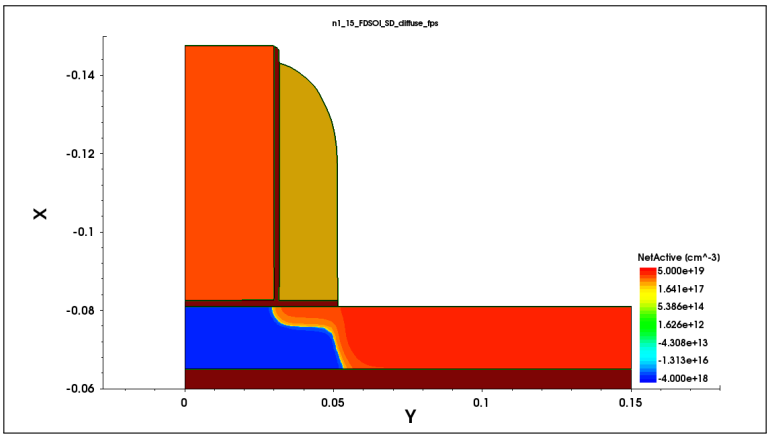


Figure B.15

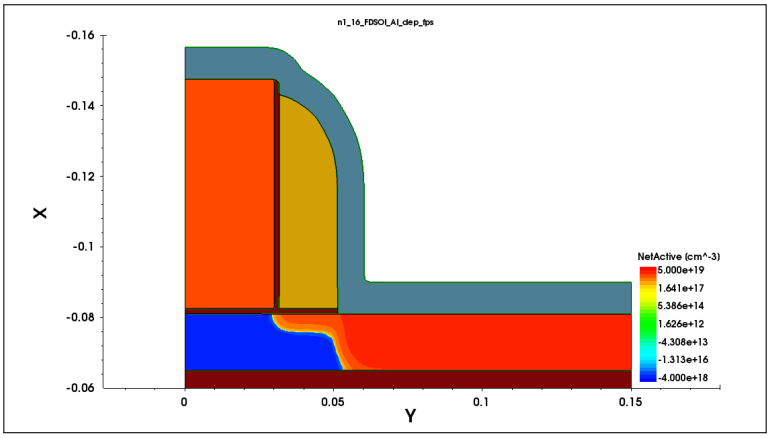


Figure B.16

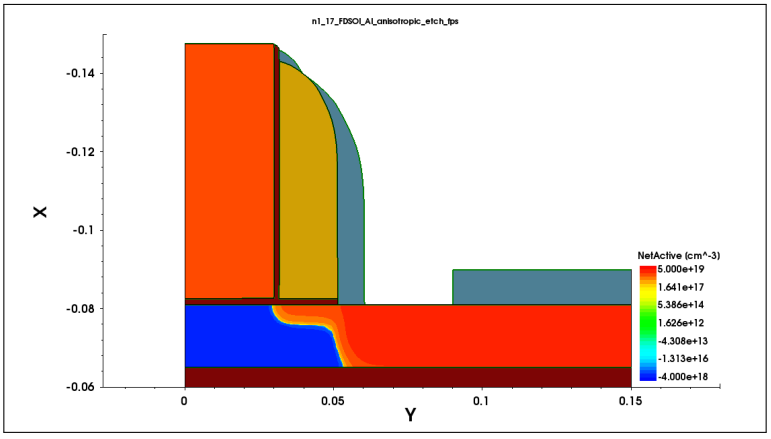


Figure B.17

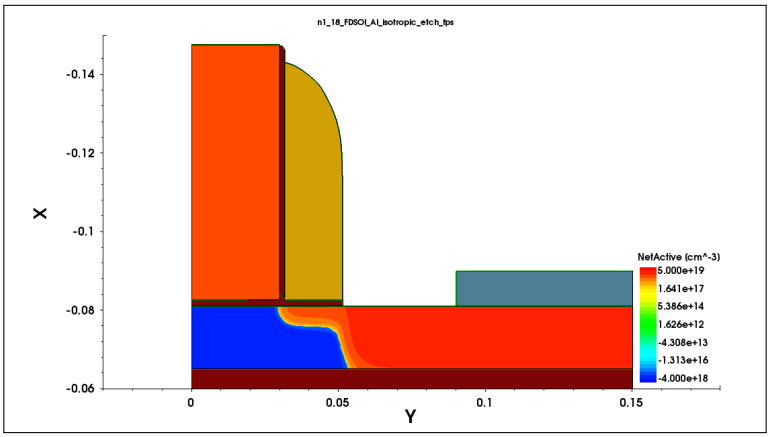


Figure B.18

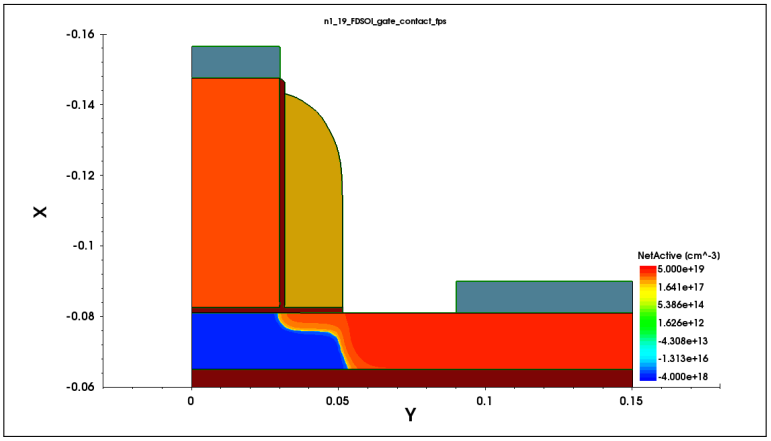


Figure B.19

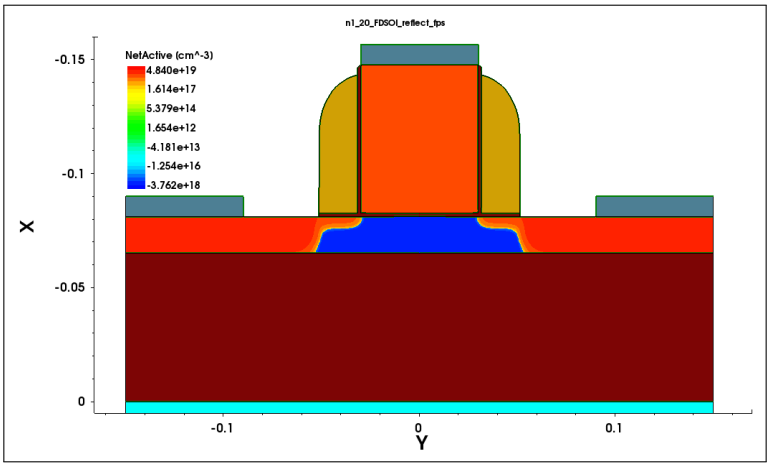


Figure B.20

C SOI with RMG

C.1 Command file *sprocess_fps.cmd*

```
# 2D MOSFET UTBB FDSOI (n type, 60 nm technology, conventional well process)
# ------------------------------------------------------
math coord.ucs

# Declare initial grid (half structure)
# ------------------------------------------------------
line x location= 0.0      spacing= 10.0<nm>  tag= SiTop
line x location= 20.0<nm> spacing= 20.0<nm>
line x location= 0.2<um>  spacing= 100.0<nm>  tag= SiBottom
line y location= 0.0      spacing= 20<nm> tag= Mid
line y location= 0.15<um> spacing=20<nm>  tag= Right

# Silicon substrate definition
# ------------------------------------------------------
region Silicon xlo= SiTop xhi= SiBottom ylo= Mid yhi= Right

# Initialize the simulation
# ------------------------------------------------------
init concentration= 1.0e+15<cm-3> field= Boron !DelayFullD
AdvancedCalibration
struct tdr=n@node@_01_FDSOI_substrate0; # p-type Si substrate

# SOI wafer preparation (BOX + p-type Si overlay)
# Alert: this is only an approximation of the real procedure! (typically smart-cut)
# ------------------------------------------------------
deposit material= {Oxide} type= isotropic thickness=0.065
struct tdr=n@node@_02_FDSOI_box; # buried oxide deposition

deposit material = {Silicon} type= isotropic thickness=0.016 fields.values= {Boron=
5e18}
struct tdr=n@node@_03_FDSOI_soi; # silicon overlay deposition

# Global mesh settings for automatic meshing in newly generated layers
# ------------------------------------------------------
grid set.min.normal.size= 1.0<nm> set.normal.growth.ratio.2d= 1.5
mgoals accuracy = 1e-5

# Dummy gate deposition (60 nm channel length)
# ------------------------------------------------------
deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.065}
struct tdr= n@node@_04_FDSOI_gate_dep;

# Poly gate pattern/etch
# anisotropic etching, poly thickness (65 nm) + tolerance (2 nm) to avoid residuals
# mask only half-channel length to reduce simulation time
# ------------------------------------------------------
mask name= gate_mask left=-1 right= 30<nm>
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.067} \
  mask = gate_mask
struct tdr= n@node@_05_FDSOI_gate_poly_etch;

# Poly reoxidation
# ------------------------------------------------------
diffuse temperature= 850<C> time= 0.5<min> O2
```

```
struct tdr= n@node@_06_FDSOI_poly_reox;

# LDD implantation and diffusion
# ------------------------------------------------------
refinebox Silicon min= {-0.081 0.025} max= {-0.065 0.04} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002} add
grid remesh

implant Arsenic dose= 4e13<cm-2> energy= 0.01<keV> tilt= 0 rotation= 0
struct tdr= n@node@_07_FDSOI_LDD_implant;

diffuse temperature= 1050<C> time= 0.1<s>
struct tdr= n@node@_08_FDSOI_LDD_diffuse;

# Nitride spacers
# ------------------------------------------------------
deposit material= {Nitride} type= isotropic time= 1 rate= {0.02}
struct tdr= n@node@_09_FDSOI_spacer_dep;

etch material= {Nitride} type= anisotropic time = 1 rate= {0.022} \
  isotropic.overetch= 0.01
struct tdr= n@node@_10_FDSOI_spacer_etch;

etch material= {Oxide} type= anisotropic time= 1 rate= {0.002}
struct tdr= n@node@_11_FDSOI_spacer_ox_removal;

# Source/drain implantation
# ------------------------------------------------------
refinebox Silicon min= {-0.076 0.05} max= {-0.065 0.15} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002} add
grid remesh

implant Arsenic dose= 7e13<cm-2> energy= 2<keV> \
        tilt= 7<degree> rotation= -90<degree>
struct tdr= n@node@_12_FDSOI_SD_implant;

# Final RTA
# ------------------------------------------------------
diffuse temperature= 1050<C> time= 5.0<s>
struct tdr= n@node@_13_FDSOI_SD_diffuse;

# RMG
# ------------------------------------------------------
mask name= gate_mask2 left=-1 right= 30<nm> negative
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.067} \
  mask = gate_mask2
struct tdr= n@node@_14_FDSOI_dummy_gate_etch;
deposit material= {Oxide} type= polygon polygon= {-0.081 0 -0.081 0.03 -0.082 0.03
-0.082 0}
struct tdr= n@node@_15_FDSOI_SiO2_deposition;

deposit material= {HfO2} type= polygon polygon= {-0.082 0 -0.082 0.03 -0.085 0.03 -0.085
0}
struct tdr= n@node@_16_FDSOI_HfO2_deposition;

deposit material= {Tungsten} type= polygon polygon= {-0.085 0 -0.085 0.03 -0.146 0.03
-0.146 0}
```

```
struct tdr= n@node@_17_FDSOI_rmg_deposition;

# Contacts
# ------------------------------------------------------
deposit material= {Aluminum} type= isotropic thickness= 0.009
struct tdr= n@node@_18_FDSOI_Al_dep; # Aluminium deposition

mask name= contacts_mask left= 0.09<um> right= 1.0<um>
etch material= {Aluminum} type= anisotropic thickness= 0.01 \
     mask= contacts_mask
struct tdr= n@node@_19_FDSOI_Al_anisotropic_etch; # Aluminum anisotropic etching

etch material= {Aluminum} type= isotropic thickness= 0.01 \
     mask= contacts_mask
struct tdr= n@node@_20_FDSOI_Al_isotropic_etch; # Aluminum isotropic etching

deposit material= {Aluminum} type= anisotropic thickness= 0.009 \
     mask= gate_mask2
struct tdr= n@node@_21_FDSOI_gate_contact; # gate contact creation

# Reflect
# ------------------------------------------------------
transform reflect left
struct tdr= n@node@_22_FDSOI_reflect; # Final structure

# Remeshing
# ------------------------------------------------------
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines
line clear
pdbSet Grid SnMesh DelaunayType boxmethod

refinebox Silicon min= {-0.081 -0.04} max= {-0.065 -0.025} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.076 -0.15} max= {-0.065 -0.05} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.081 0.025} max= {-0.065 0.04} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.076 0.05} max= {-0.065 0.15} \
  xrefine= {0.003 0.005} \
  yrefine= {0.002}
refinebox Silicon min= {-0.076 -0.02} max= {-0.065 0.02} \
  xrefine= {0.005 0.005} \
  yrefine= {0.005}
grid remesh

# Contacts
# ------------------------------------------------------
contact bottom name = substrate Silicon
contact name = gate x = -0.152 y = 0.0 Aluminum
contact name = source x = -0.085 y = -0.12 Aluminum
contact name = drain x = -0.085 y = 0.1 Aluminum
struct tdr= n@node@_23_FDSOI_presimulation
exit
```

C.2 Command file *sdevice_des.cmd*

```
File
{
*INPUT FILES
Grid ="n1_23_FDSOI_presimulation_fps.tdr"
* physical parameters
Parameter = "sdevice.par"

*OUTPUT FILES
Plot = "n@node@_des.tdr"
* electrical characteristics at the electrodes
Current= "n@node@_des.plt"
}

Electrode
{
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="substrate" Voltage=0.0}
}

Thermode
{
{ Name = "source" Temperature = 300 }
{ Name = "drain" Temperature = 300 }
{ Name = "gate" Temperature = 300 }
{ Name = "substrate" Temperature = 300 }
}

Physics
{
  EffectiveIntrinsicDensity(NoBandGapNarrowing)
  Mobility(DopingDependence,HighFieldSaturation)
  Recombination(SRH)
  Temperature=300
}

Plot
{
  Potential ElectricField/Vector
  eEparallel eEnormal
  hEparallel hEnormal
  eDensity hDensity SpaceCharge
  Affinity IntrinsicDensity
  eCurrent/Vector hCurrent/Vector TotalCurrentDensity/Vector
  eMobility hMobility eVelocity hVelocity
  Doping DonorConcentration AcceptorConcentration
  DonorPlusConcentration AccepMinusConcentration
  ConductionBandEnergy ValenceBandEneergy
  eQuasiFermiEnergy hQuasiFermiEnergy
  eAvalancheGeneration hAvalancheGeneration
  BandGap DielectricConstant
}

Math
{
```

```
  Extrapolate
  * use full derivatives in Newton method
  Derivatives
  * control on relative errors
  RelErrControl
  * relative error= 10^(-Digits)
  Digits=5
  * maximum number of iteration at each step
  Iterations=100
  ExitOnFailure
}

Solve
{
############ VDS=2V, VGS sweep 0-2V ##############
  Poisson
  Coupled { Poisson Electron Hole  }
  Plot(FilePrefix="equil")

quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-8
Goal {name= "drain" voltage = 2})
{coupled { Poisson  Electron Hole }
CurrentPlot ( Time = (range = (0 2) intervals = 200))
Plot(FilePrefix = "IDVD" Time=(2.0))}

quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-8
Goal {name= "gate" voltage = 2})
{coupled { Poisson Electron Hole }
CurrentPlot ( Time = (range = (0 2) intervals = 200))
Plot(FilePrefix = "IDVG" Time=(2))}

############ VDS=0.2V, VGS sweep 0-2V ##############
  Load(FilePrefix= "equil")

NewCurrentPrefix = "IDVD_VD0d2_"
quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-8
Goal {name= "drain" voltage = 0.2})
{coupled { Poisson  Electron Hole }
CurrentPlot ( Time = (range = (0 0.2) intervals = 200))
Plot(FilePrefix = "IDVD_VD0d2_" Time=(2.0))}

NewCurrentPrefix = "IDVG_VD0d2_"
quasistationary (InitialStep=0.005 MaxStep = 0.1 MinStep=1e-8
Goal {name= "gate" voltage = 2})
{coupled { Poisson Electron Hole }
CurrentPlot ( Time = (range = (0 2) intervals = 200))
Plot(FilePrefix = "IDVG_VD0d2_" Time=(2))}
}
```

C.3 Process steps

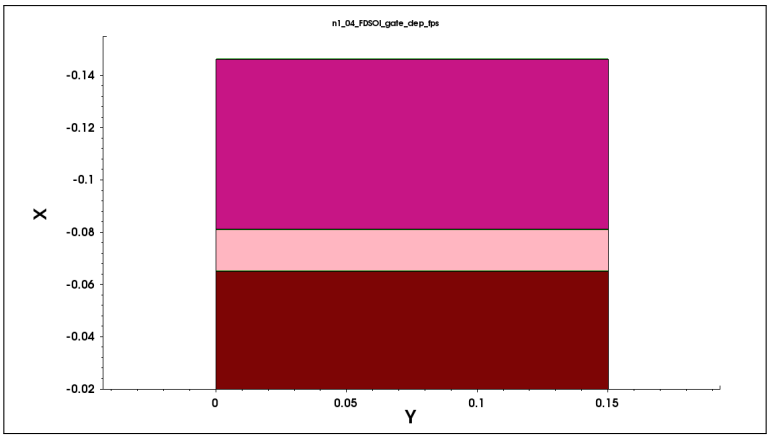


Figure C.1

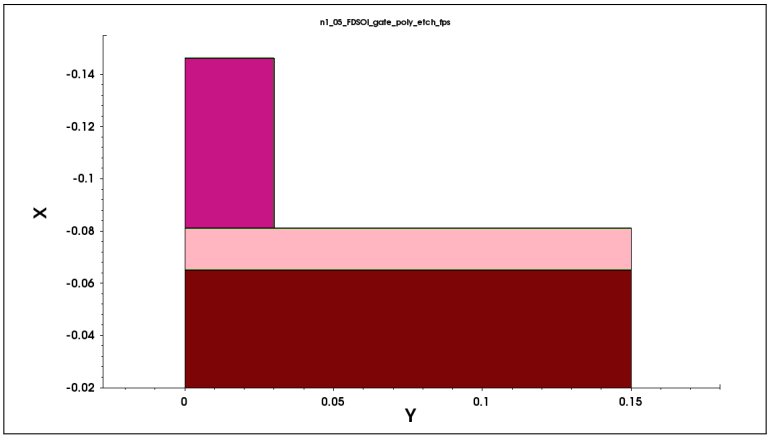


Figure C.2

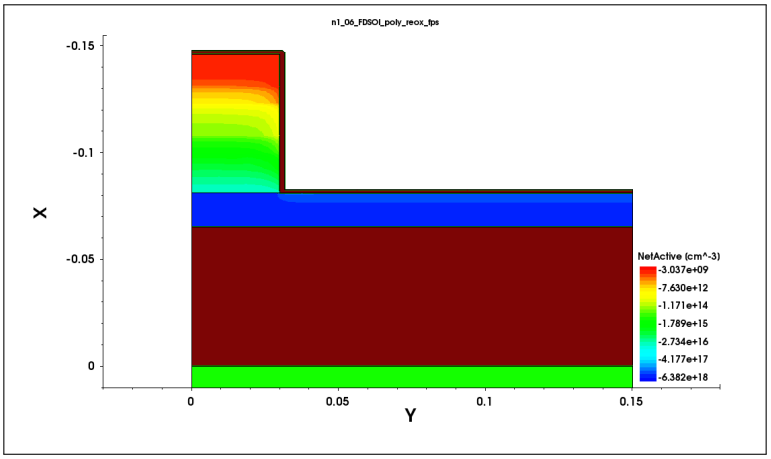


Figure C.3

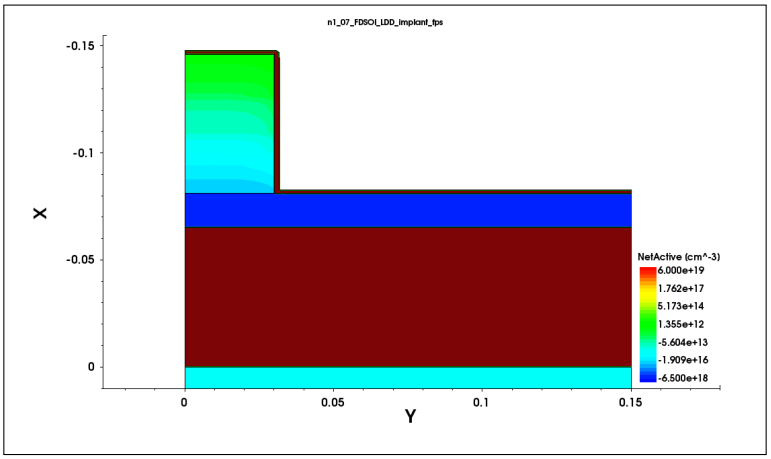


Figure C.4

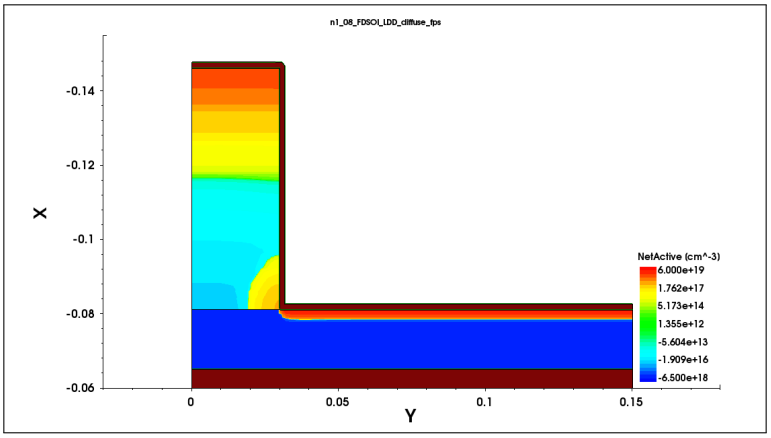


Figure C.5

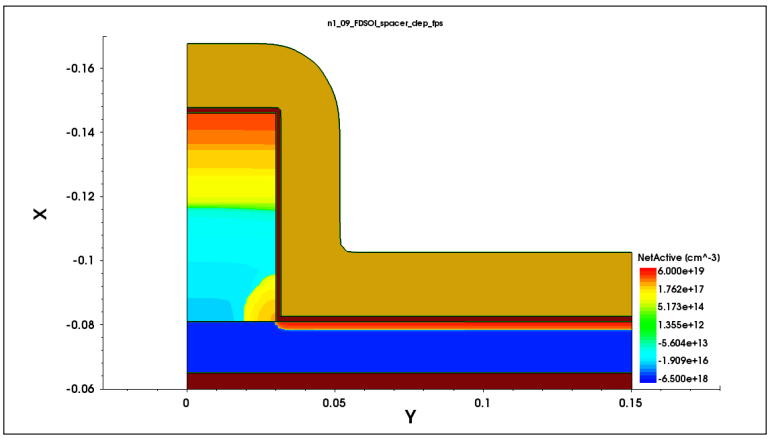


Figure C.6

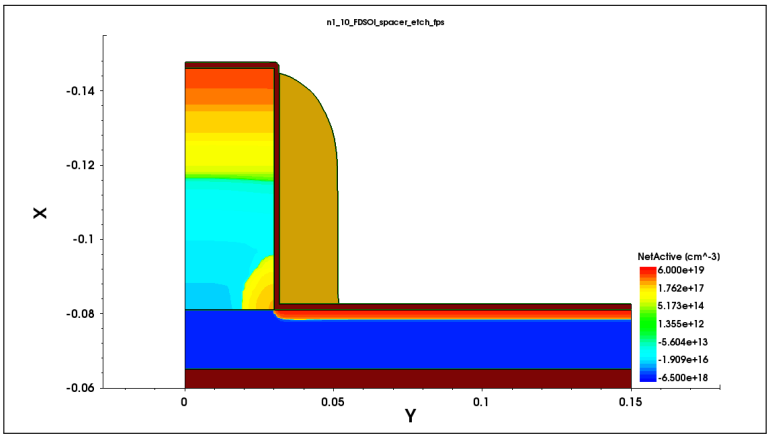


Figure C.7

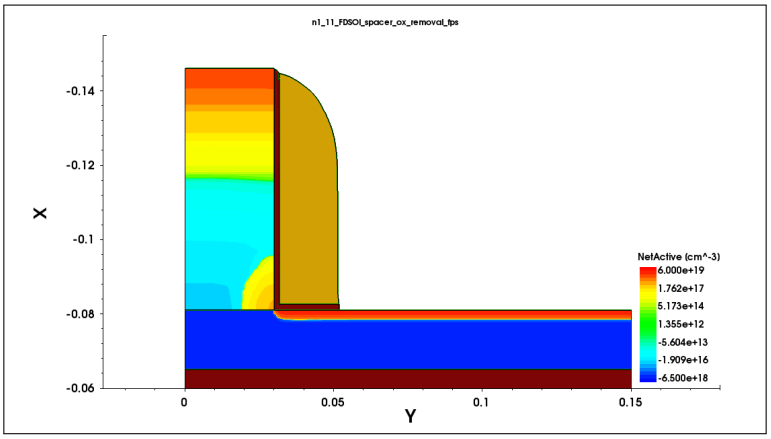


Figure C.8

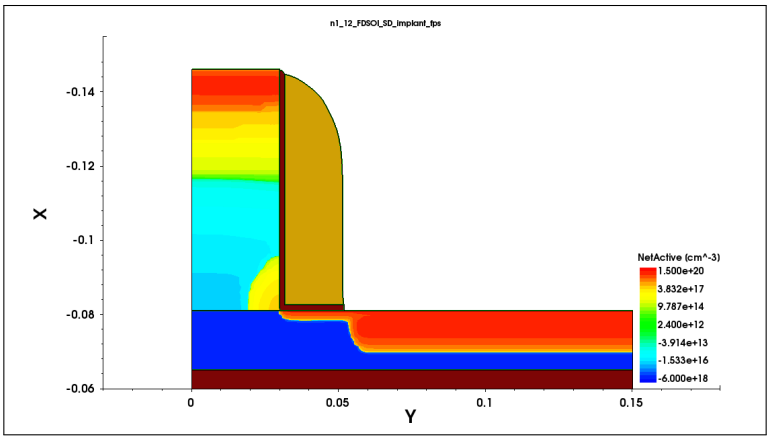


Figure C.9

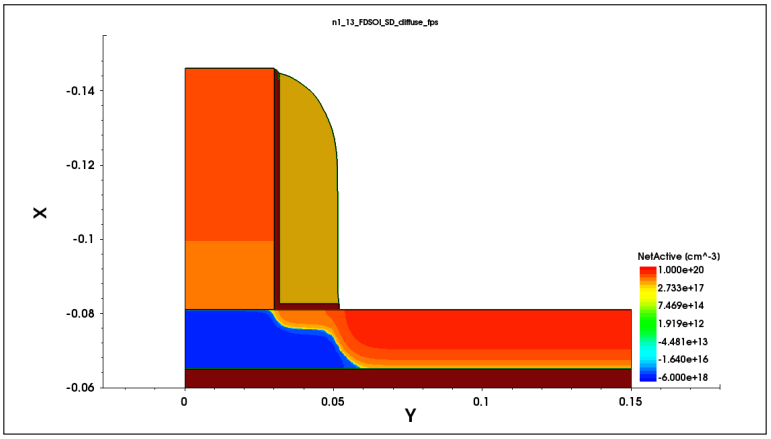


Figure C.10

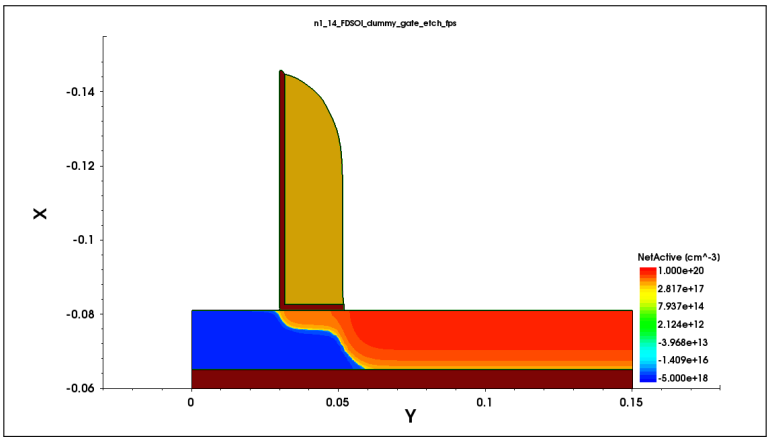


Figure C.11

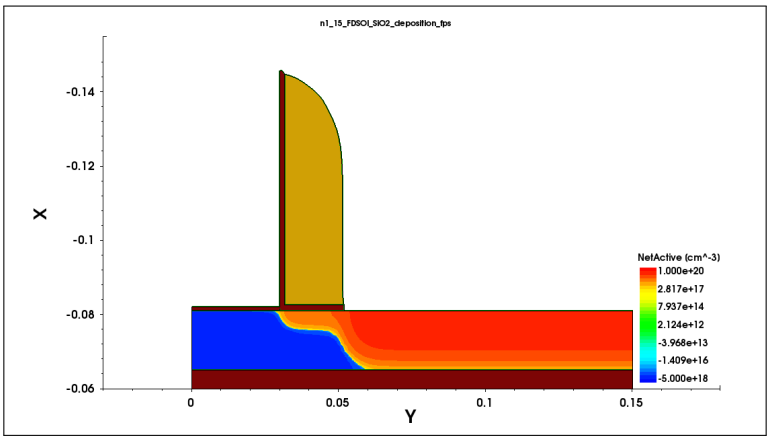


Figure C.12

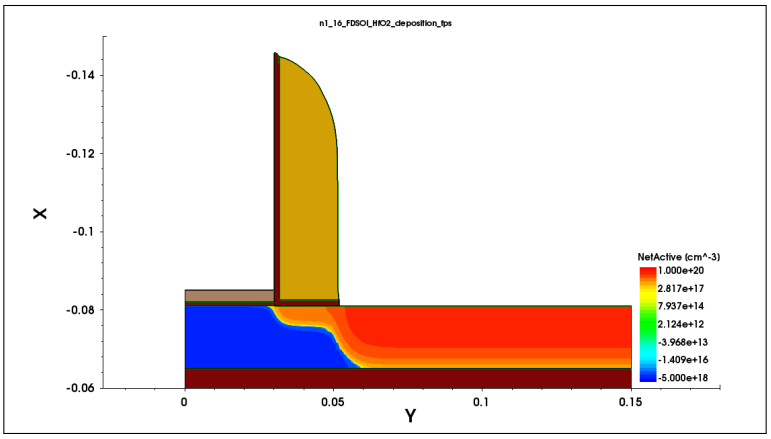


Figure C.13

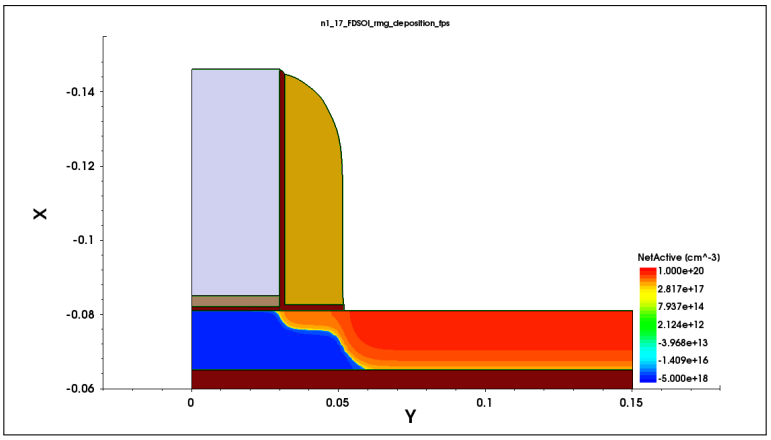


Figure C.14

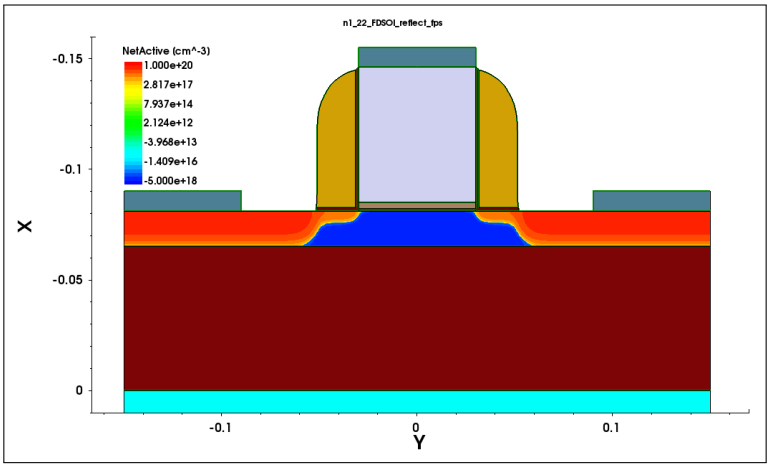


Figure C.15

D Data analysis

```
close all,
clearvars,
clc,
format long e

%% Global settings
set(groot, 'defaultLineLineWidth', 1.5)
set(groot, 'defaultAxesXGrid', 'on')
set(groot, 'defaultAxesYGrid', 'on')
set(groot, 'defaultFigurePosition', [400 250 900 600])

%% Import data
filename = 'Output/trans_v1.txt';
A = importdata(filename);
Vgs_v1 = A.data(103:end,1);
Ids_v1 = A.data(103:end,2);

filename = 'Output/trans_v2.txt';
A = importdata(filename);
Vgs_v2 = A.data(103:end,1);
Ids_v2 = A.data(103:end,2);

filename = 'Output/trans_v3.txt';
A = importdata(filename);
Vgs_v3 = A.data(103:end,1);
Ids_v3 = A.data(103:end,2);

filename = 'Output/trans_v3_low.txt';
A = importdata(filename);
Vgs_v3_low = A.data(:,1);
Ids_v3_low = A.data(:,2);

filename = 'Output/trans_rmg.txt';
A = importdata(filename);
Vgs_rmg = A.data(103:end,1);
Ids_rmg = A.data(103:end,2);

filename = 'Output/trans_rmg_low.txt';
A = importdata(filename);
Vgs_rmg_low = A.data(:,1);
Ids_rmg_low = A.data(:,2);

filename = 'Output/trans_HfO2.txt';
A = importdata(filename);
Vgs_HfO2 = A.data(103:end,1);
Ids_HfO2 = A.data(103:end,2);

filename = 'Output/trans_HfO2_low.txt';
A = importdata(filename);
Vgs_HfO2_low = A.data(:,1);
Ids_HfO2_low = A.data(:,2);

%% Calculations
Vds = 2; % [V]
Vds_low = 0.2; % [V]

```

```
Ioff_v1 = Ids_v1(1); % [A/um]
Ion_v1 = Ids_v1(end); % [A/um]
on_off_ratio_v1 = Ion_v1 / Ioff_v1;
Vth_v1 = threshold(Vgs_v1, Ids_v1); % [V]
SS_v1 = subthreshold_slope(Vgs_v1, Ids_v1); % [mV/dec]

Ioff_v2 = Ids_v2(1); % [A/um]
Ion_v2 = Ids_v2(end); % [A/um]
on_off_ratio_v2 = Ion_v2 / Ioff_v2;
Vth_v2 = threshold(Vgs_v2, Ids_v2); % [V]
SS_v2 = subthreshold_slope(Vgs_v2, Ids_v2); % [mV/dec]

Ioff_v3 = Ids_v3(1); % [A/um]
Ion_v3 = Ids_v3(end); % [A/um]
on_off_ratio_v3 = Ion_v3 / Ioff_v3;
Vth_v3 = threshold(Vgs_v3, Ids_v3); % [V]
Vth_v3_low = threshold(Vgs_v3_low, Ids_v3_low); % [V]
SS_v3 = subthreshold_slope(Vgs_v3, Ids_v3); % [mV/dec]
DIBL_v3 = 1000 * ( Vth_v3 - Vth_v3_low ) / ( Vds - Vds_low ); % [mV/V]
gm_v3 = 1000 * gradient(Ids_v3) ./ gradient(Vgs_v3); % [mS/um]

Ioff_rmg = Ids_rmg(1); % [A/um]
Ion_rmg = Ids_rmg(end); % [A/um]
on_off_ratio_rmg = Ion_rmg / Ioff_rmg;
Vth_rmg = threshold(Vgs_rmg, Ids_rmg); % [V]
Vth_rmg_low = threshold(Vgs_rmg_low, Ids_rmg_low); % [V]
SS_rmg = subthreshold_slope(Vgs_rmg, Ids_rmg); % [mV/dec]
DIBL_rmg = 1000 * ( Vth_rmg - Vth_rmg_low ) / ( Vds - Vds_low ); % [mV/V]
gm_rmg = 1000 * gradient(Ids_rmg) ./ gradient(Vgs_rmg); % [mS/um]

Ioff_HfO2 = Ids_HfO2(1); % [A/um]
Ion_HfO2 = Ids_HfO2(end); % [A/um]
on_off_ratio_HfO2 = Ion_HfO2 / Ioff_HfO2;
Vth_HfO2 = threshold(Vgs_HfO2, Ids_HfO2); % [V]
Vth_HfO2_low = threshold(Vgs_HfO2_low, Ids_HfO2_low); % [V]
SS_HfO2 = subthreshold_slope(Vgs_HfO2, Ids_HfO2); % [mV/dec]
DIBL_HfO2 = 1000 * ( Vth_HfO2 - Vth_HfO2_low ) / ( Vds - Vds_low ); % [mV/V]
gm_HfO2 = 1000 * gradient(Ids_HfO2) ./ gradient(Vgs_HfO2); % [mS/um]

%% Results
fprintf('VERSION 1 (NA = 1e18 cm^-3)\n')
fprintf('Vth = %.0f mV\n', Vth_v1*1e3);
fprintf('Ion = %.3f mA/um @ Vds=2V\n', Ion_v1*1e3);
fprintf('Ioff = %.3f uA/um @ Vds=2V\n', Ioff_v1*1e6);
fprintf('Ion/Ioff ratio: %.3f\n', on_off_ratio_v1);
fprintf('SS = %.3f mV/dec\n\n', SS_v1);

fprintf('VERSION 2 (NA = 2.5e18 cm^-3)\n')
fprintf('Vth = %.0f mV\n', Vth_v2*1e3);
fprintf('Ion = %.3f mA/um @ Vds=2V\n', Ion_v2*1e3);
fprintf('Ioff = %10e uA/um @ Vds=2V\n', Ioff_v2*1e6);
fprintf('Ion/Ioff ratio: %10e\n', on_off_ratio_v2);
fprintf('SS = %.3f mV/dec\n\n', SS_v2);

fprintf('VERSION 3, poly gate (NA = 5e18 cm^-3)\n')
fprintf('Vth = %.0f mV @ Vds = 2V, Vth = %.0f mV @ Vds = 0.2V\n', Vth_v3*1e3,
Vth_v3_low*1e3);
fprintf('Ion = %.3f mA/um @ Vds=2V\n', Ion_v3*1e3);
fprintf('Ioff = %10e uA/um @ Vds=2V\n', Ioff_v3*1e6);
```

```
fprintf('Ion/Ioff ratio: %10e\n', on_off_ratio_v3);
fprintf('SS = %.3f mV/dec\n', SS_v3);
fprintf('DIBL = %.3f mV/V\n\n', DIBL_v3);

fprintf('VERSION 3, RMG with SiO2 (NA = 5e18 cm^-3)\n')
fprintf('Vth = %.0f mV @ Vds = 2V, Vth = %.0f mV @ Vds = 0.2V\n', Vth_rmg*1e3,
Vth_rmg_low*1e3);
fprintf('Ion = %.3f mA/um @ Vds=2V\n', Ion_rmg*1e3);
fprintf('Ioff = %10e uA/um @ Vds=2V\n', Ioff_rmg*1e6);
fprintf('Ion/Ioff ratio: %10e\n', on_off_ratio_rmg);
fprintf('SS = %.3f mV/dec\n', SS_rmg);
fprintf('DIBL = %.3f mV/V\n\n', DIBL_rmg);

fprintf('VERSION 3, RMG with HfO2 (NA = 5e18 cm^-3)\n')
fprintf('Vth = %.0f mV @ Vds = 2V, Vth = %.0f mV @ Vds = 0.2V\n', Vth_HfO2*1e3,
Vth_HfO2_low*1e3);
fprintf('Ion = %.3f mA/um @ Vds=2V\n', Ion_HfO2*1e3);
fprintf('Ioff = %10e uA/um @ Vds=2V\n', Ioff_HfO2*1e6);
fprintf('Ion/Ioff ratio: %10e\n', on_off_ratio_HfO2);
fprintf('SS = %.3f mV/dec\n', SS_HfO2);
fprintf('DIBL = %.3f mV/V\n', DIBL_HfO2);

%% Plots
figure
semilogy(Vgs_v1, Ids_v1)
hold on
semilogy(Vgs_v2, Ids_v2)
semilogy(Vgs_v3, Ids_v3)
xlabel('V_{gs} [V]')
ylabel('I_{ds} [A/\mum]')
legend('poly gate, N_A=1\times10^{18} cm^{-3}', ...
    'poly gate, N_A=2.5\times10^{18} cm^{-3}', ...
    'poly gate, N_A=5\times10^{18} cm^{-3}', ...
    Location = 'southeast')
xlim([min(Vgs_v3) max(Vgs_v3)])
exportgraphics(gcf, 'Figures/comparison_v123.pdf')

figure
semilogy(Vgs_v3, Ids_v3)
hold on
semilogy(Vgs_v3_low, Ids_v3_low)
xlabel('V_{gs} [V]')
ylabel('I_{ds} [A/\mum]')
legend('poly gate, V_{ds}=2V', 'poly gate, V_{ds}=0.2V', Location = 'southeast')
xlim([min(Vgs_v3) max(Vgs_v3)])
exportgraphics(gcf, 'Figures/trans_poly.pdf')

figure
semilogy(Vgs_rmg, Ids_rmg)
hold on
semilogy(Vgs_rmg_low, Ids_rmg_low)
xlabel('V_{gs} [V]')
ylabel('I_{ds} [A/\mum]')
legend('RMG, V_{ds}=2V', 'RMG, V_{ds}=0.2V', Location = 'southeast')
xlim([min(Vgs_rmg) max(Vgs_rmg)])
exportgraphics(gcf, 'Figures/trans_rmg.pdf')

figure
semilogy(Vgs_HfO2, Ids_HfO2)
```

```
hold on
semilogy(Vgs_HfO2_low, Ids_HfO2_low)
xlabel('V_{gs} [V]')
ylabel('I_{ds} [A/\mum]')
legend('RMG with HfO_2, V_{ds}=2V', 'RMG with HfO_2, V_{ds}=0.2V', Location =
'southeast')
xlim([min(Vgs_HfO2) max(Vgs_HfO2)])
exportgraphics(gcf, 'Figures/trans_HfO2.pdf')

figure
semilogy(Vgs_v3, Ids_v3)
hold on
semilogy(Vgs_rmg, Ids_rmg)
semilogy(Vgs_HfO2, Ids_HfO2)
xlabel('V_{gs} [V]')
ylabel('I_{ds} [A/\mum]')
legend('poly gate, V_{ds}=2V', 'RMG + SiO_2, V_{ds}=2V', 'RMG + HfO_2, V_{ds}=2V', ...
    Location = 'southeast')
xlim([min(Vgs_rmg) max(Vgs_rmg)])
exportgraphics(gcf, 'Figures/trans_poly_rmg_comparison.pdf')

figure
plot(Vgs_v3, gm_v3)
hold on
plot(Vgs_rmg, gm_rmg)
semilogy(Vgs_HfO2, gm_HfO2)
xlabel('V_{gs} [V]')
ylabel('g_m [mS/\mum]')
legend('poly gate, V_{ds}=2V', 'RMG + SiO_2, V_{ds}=2V', 'RMG + HfO_2, V_{ds}=2V', ...
    Location = 'southeast')
xlim([min(Vgs_rmg) max(Vgs_rmg)])
exportgraphics(gcf, 'Figures/gm_poly_rmg_comparison.pdf')

%% Function to calculate the threshold voltage
function [Vth] = threshold(Vgs, Ids)
    diff1 = gradient(Ids) ./ gradient(Vgs); % first derivative
    diff2 = gradient(diff1) ./ gradient(Vgs); % second derivative
    [~, pos] = max(diff2); % inflection point
    Vth = Vgs(pos); % threshold voltage
end

%% Function to calculate the subthreshold slope
function [SS] = subthreshold_slope(Vgs, Ids)
    difflog = diff(log10(Ids)) ./ diff(Vgs);
    [peak, ~] = max(difflog);
    SS = 1000 / peak; % [mV/dec]
end
```