GAVRT DSS-28 Monitor and Control System Specification

December 24, 2006

1. Radiometer System (RSS) Physical Layout

The radiometer system consists of two cryogenic front-ends, A and B, a receiver box, and a power supply box, all located at the vertex of the 34m DSS-28 antenna as shown in Figure 1 below:

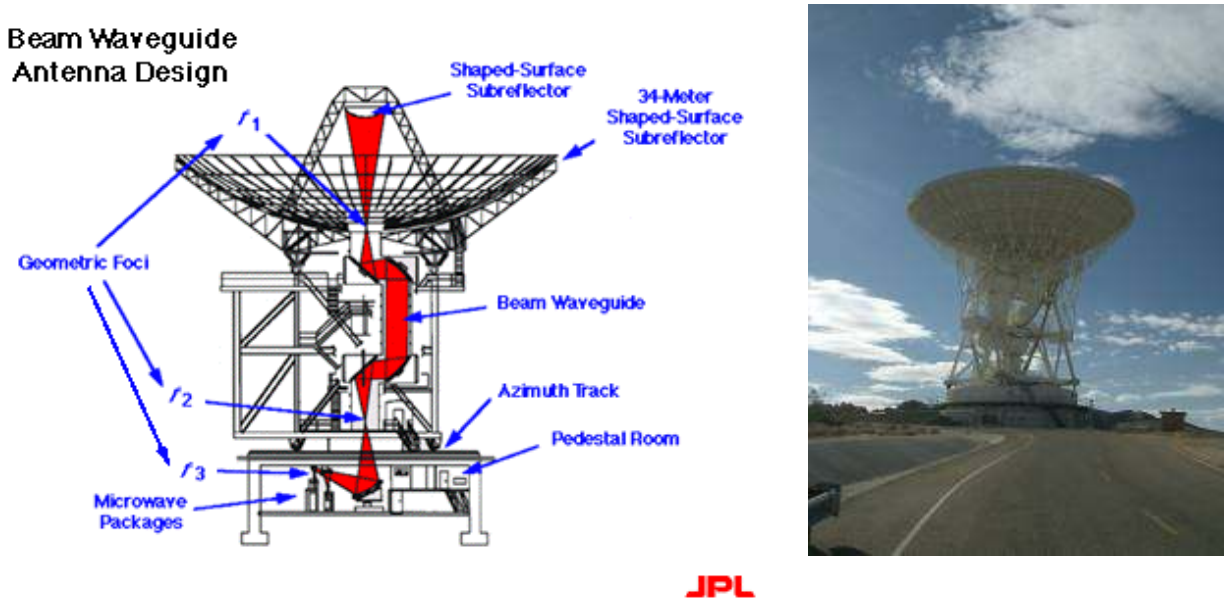

Figure 1 - DSS28 antenna. The radiometric system will be entirely located at f1 and the control computer is located in the pedestal room.

The antenna vertex is accessible for installation and maintenance with by stairways and a short (12') vertical ladder with the antenna pointed at zenith. A rotating tertiary reflector of diameter approximately 2m, to be located at the center of the vertex region, will be used to select front-end A or B. The front ends are cabled to the receiver box which will contain the monitor and control (M/C) system and the receivers as shown in the block diagrams, Figures 2-4. The M/C system will communicate via multi-mode optical fibers to a control computer in the antenna pedestal room and this computer is then accessible via the internet to other locations.

There are 16 receiver channels in the receiver box with selectable polarizations (RCP, LCP, V, and H), center frequency (1 to 15 GHz), and bandwidth (2 GHz to 100 MHz). The total power output of these receivers are used for measurements of broadband continuum radio astronomy signals and these total power with integration time down to 1ms are the highest data rate input into the M/C system. For analysis of the spectrum within each receiver channel, 8 of the 16 channels as selected through a matrix switch,

are fed through wideband single-mode optical fibers to spectrometers which can be located in the pedestal room or at DSS-13.

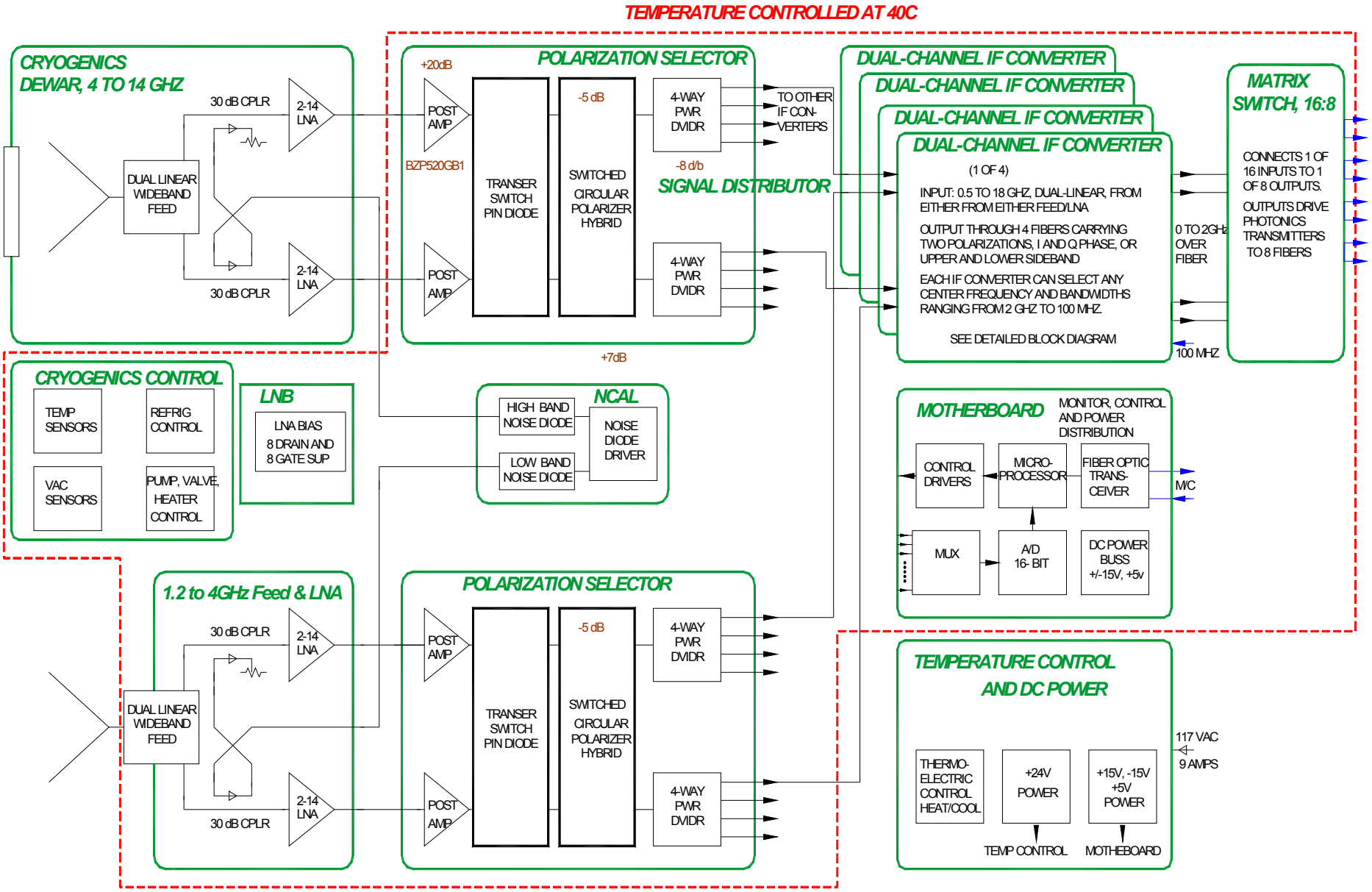

Figure 2 - Complete block diagram of the GAVRT DSS28 radiometer subsystem.

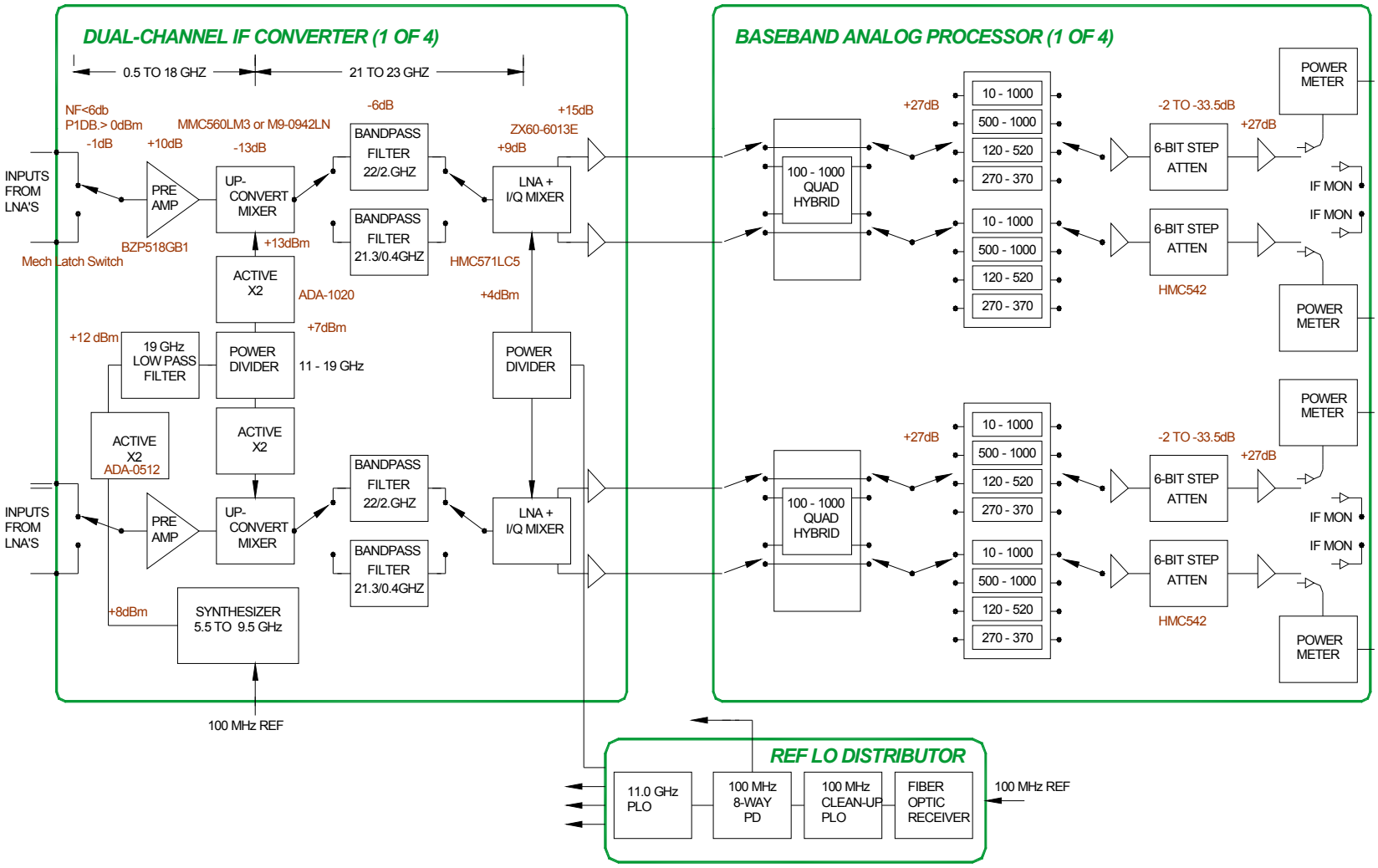

Figure 3 - Detail block diagram of IF converter and baseband analog processor.

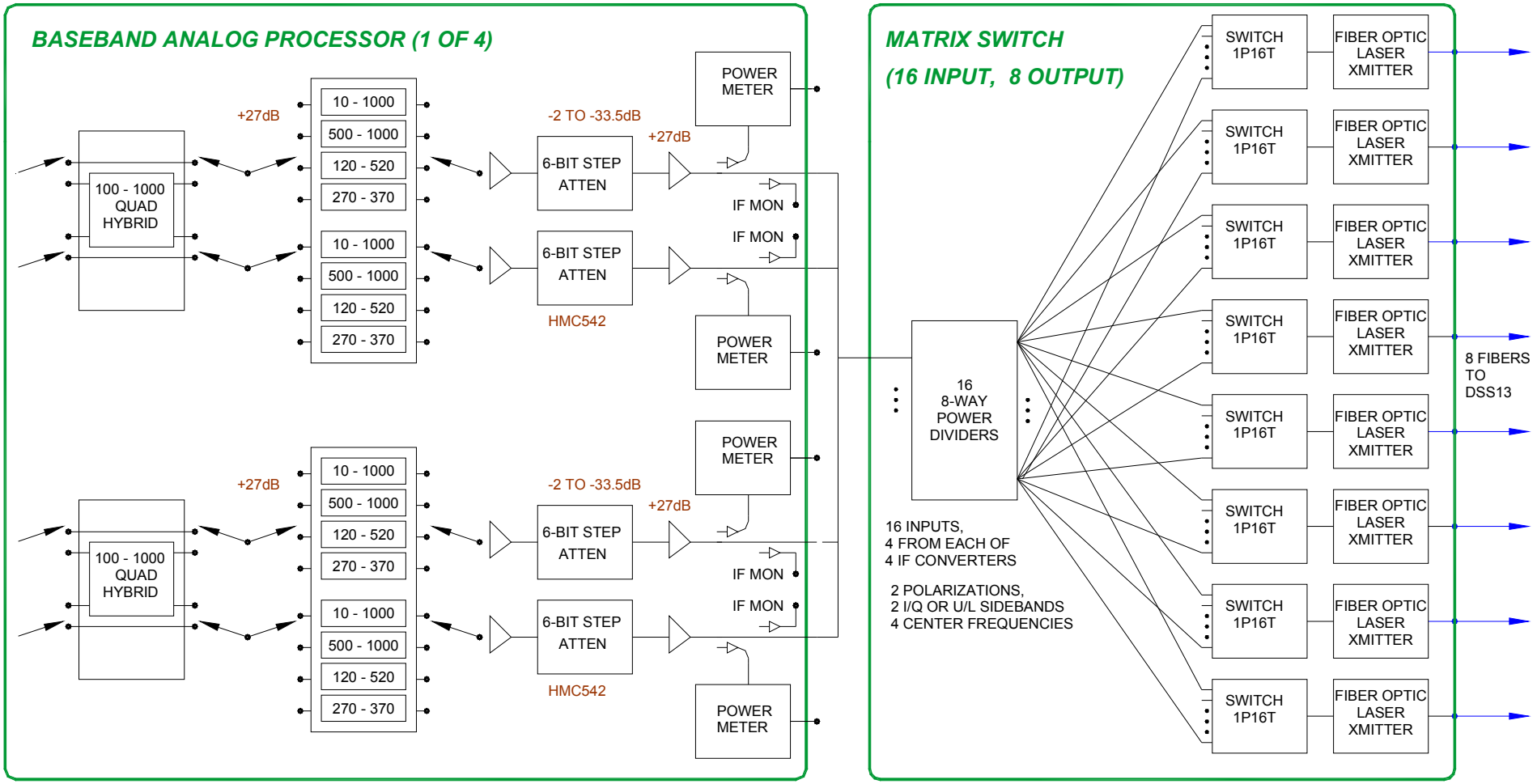

Figure 4 - Block diagram of baseband processor and matrix switch.

2. M/C Subsystem Data Rate, Volume, and Rate Requirements

The initial requirements are tabulated at the bottom of Table 1 but to allow for ease in implementation and future growth, approximately a factor of two greater capability should be available as follows"

RSS to control computer download rate: 800K bits/sec
RSS from control upload rate: 32K bits/sec
Digital control lines: 384
Digital monitor lines: 64
Analog 12-bit monitor lines: 64

The latency for high speed control and monitor signal described in the next section shall be < 5us. All other signals shall have a latency < 1ms with the understanding that the mechanical coaxial relays in the system may require 20ms for completion and the frequency synthesizers have 50ms acquisition time.

3. M/C Synchronization Requirements

A block diagram of the M/C system is shown in Figure 5 and a list of the M/C variables and data rates is shown in Table 1. The system communicates with the antenna control computer through a serial high-speed fiber connection (Ethernet or USB) and through fiber sync signals in the 1Hz to 1000Hz range which are also carried by multi-mode fibers. The sync signals allow synchronization of the antenna pointing system and radiometer functions as follows:

A. Polarization Switch - To enable accurate measurements of weakly polarized signals diode transfer switches in the polarization selector module provide rapid switching between either H and V linear polarization or RCP and LCP circular polarization. The selection of linear or circular and the selection of the rapid switching, lock in transfer state, or lock in direct state are controlled by control system bits.

B. Noise Cal - To enable noise adding radiometer modes either a low level (2K) noise calibration signal and/or a high level (200K) calibration signal can be modulated with the sync signal in conjunction with slow control bits which select either modulated, on, or off for each noise calibration signal.

C. Total Power Integrators - Integrators realized by voltage-to-frequency converters and counters are enabled and reset by the sync signals. A 10 us delay will be built into the enable of the integrator to allow transients from the polarization switch or noise cal switch to die out before integration starts. The readout of all 16 total power integrators with 24 bits each must occur within 1ms after the integrator reset - a rate of 384K bits/sec.

Note that two hardware (on fiber) sync signals are required. One square-wave at a 500 Hz max rate to control A. and B. and another at a 1000 Hz max rate to control the integrators. It should be possible to use only the 1000 Hz signal and divide by two with phase ambiguity removed through a slow control bit.

3. M/C Subsystem Special Requirements

A. Integration with motherboard - A large motherboard mounted on the door of the 8" x 36" x 48" receiver box is planned to facilitate all power and M/C connections to receiver modules through D-type, off-the-shelf ribbon cables. The M/C subsystem should either be built into this board or have a simple way of making of the order of 300 connections to the receivers.

B. Local maintenance mode - For service on the antenna, it should be possible for all control signals to be locally commanded and all monitor signals locally observed without connection of an external computer. A small keyboard and display are desirable.
C. Low RFI - The receiver box will house sensitive amplifiers in the 10 MHz to ! GHz range and the spectrum in this frequency range will be further analyzed for small spectral line signals. These baseband amplifiers will be shield but radiation from the M/C system should also be minimized.
D. Reduce engineering costs - The system is a "one of a kind" and the design costs should be minimized by making use of existing products, standard protocols, and past experience of the responsible engineer.
E. Issues to be considered - Error detection, power on sequence, buffering, grounding

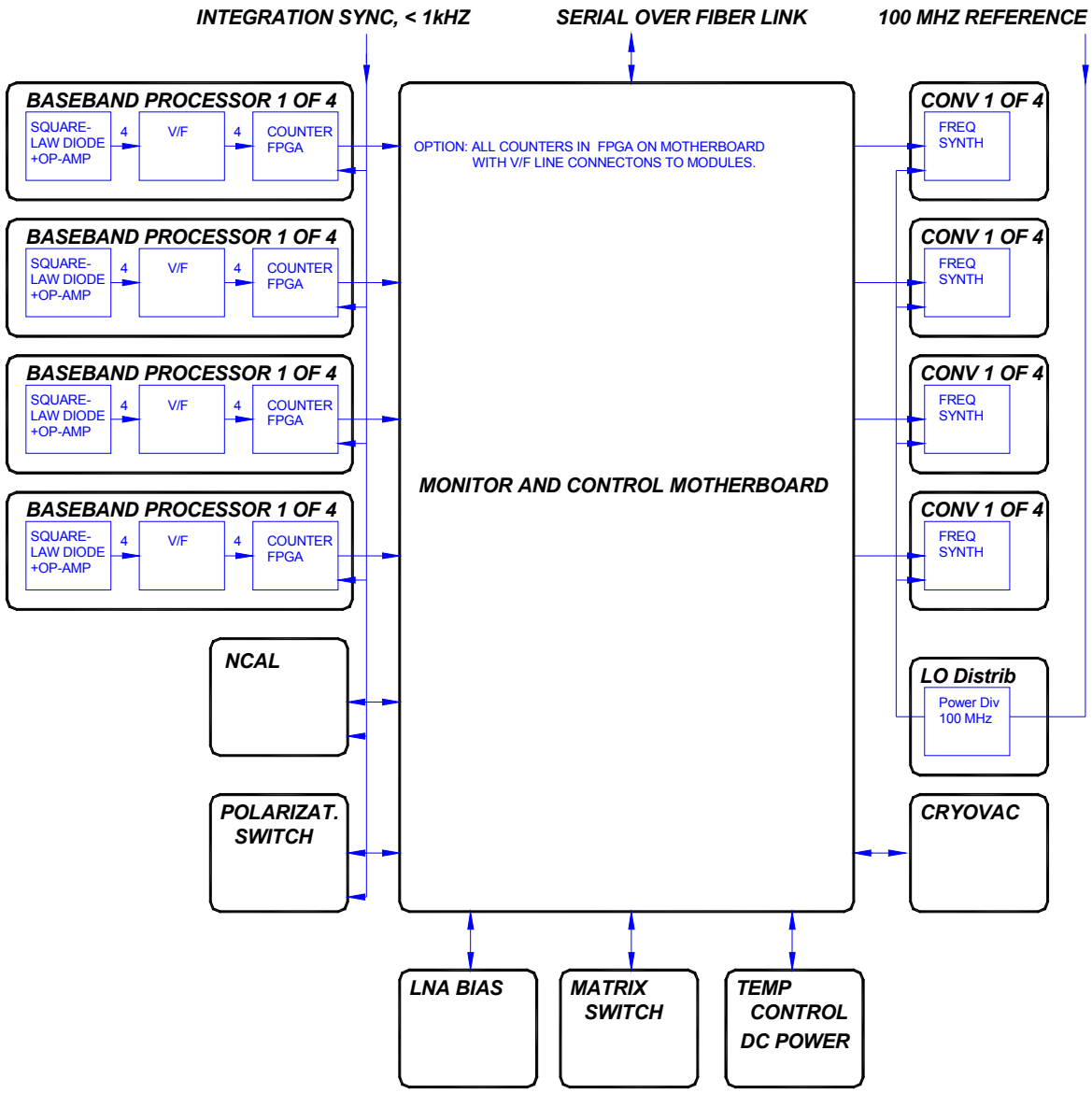

Figure 5 - Block diagram of M/C system.

Table 1 - M/C Functions and Data Rates as of Dec 23, 2006

DSS28 Radiometer System Monitor and Control Functions

23-Dec-06

Function	M/C	Variable	Bits	Fastest Update Time, sec	Remarks	Bits/sec C	Bits/sec M	DigOut Bits	Dig Mon	Ana Mon
Polarization Selector										
Receiver A, Circular or Linear Pol	C	APol	1	1	Latency 50 ms, "1" is circular, "0" is linear	1		1		
Receiver A, Pol Transfer Switch	C	APolX	2	0.001	Bits select polarization direct, transferred, or modulated	2000		2		
Receiver B, Pol Transfer Switch	C	BPolX	2	0.001	by sync signal	2000		2		
Receiver B Circular or Linear Pol	C	BPol	1	1	Latency 50 ms, "1" is circular, "0" is linear	1		1		
Converter 1										
Total Power, F1, PolA, USB or I	M	PAU	24	0.001	Power meter integrated during sync signal high		24000	Serial		
Total Power, F1, PolA, LSB or Q	M	PAL	24	0.001	Power meter integrated during sync signal high		24000	Serial		
Total Power, F1, PolB, USB or I	M	PBU	24	0.001	Power meter integrated during sync signal high		24000	Serial		
Total Power, F1, PolA, LSB or Q	M	PBL	24	0.001	Power meter integrated during sync signal high		24000	Serial		
Frequency Syntbesizer 1	C	F1	16	0.1	RS422 interface to synthesizer module	160			Serial	
Receiver A or B input switch	C	IN1	1	1	Latency 50 ms, "1" is A, "0" is B	1		1		
Receiver A or B input switch state	M	IN1S	1	1			1		1	
First bandwidth switch	C	B1	1	1	Latency 50 ms, "1" is 2000 MHz, "0" is 400 MHz	1		1		
First bandwidth switch state	M	B1S	1	1			1		1	
I/Q or USB/LSB mode	C	M1	1	1	Latency 50 ms, "1" is I/Q and "0" is USB/LSB	1		1		
I/Q or USB/LSB state	M	M1S	1	1			1		1	
PolA Bandwidth	C	BWPA	3	1	Modes are 0-1000, 500-1000, 100-500, 270-370, or Ext MH	3		3		
PolA Bandwidth state	M	BWPAS	3	1			3		3	
PolB Bandwidth	C	BWPB	3	1	Modes are 0-1000, 500-1000, 100-500, 270-370, or Ext MH	3		3		
PolB Bandwidth State	M	BWPBS	3	1			3		3	
PolA mode A attenuator	C	ATENAA	6	1	0 to 31.5 dB in 0.5 dB steps	6		6		
PolA mode B attenuator	C	ATENAB	6	1		6		6		
PolB mode A attenuator	C	ATENBA	6	1		6		6		
PolB mode B attenuator	C	ATENBB	6	1		6		6		
Temperature Monitor	M	TC1	12	1			12			1
Converters 2, 3, and 4										
(Identical to Converter 1)						579	288063	99	27	
Matrix Switch										
Line 1	C	L1	4	1	Could be switched at .001s intervals if desired	4		4		
LIne 2	C	L2	4	1		4		4		
Line 3	C	L3	4	1		4		4		
Line 4	C	L4	4	1		4		4		
Line 5	C	L5	4	1		4		4		
Line 6	C	L6	4	1		4		4		
Line 7	C	L7	4	1		4		4		
Line 8	C	L8	4	1		4		4		
Noise Source M/C	C	NSAH	2	0.001	200K noise source, receiver A	2000		2		
	C	NSAL	2	0.001	2K noise source, receiver A	2000		2		
	M	NSTM	12	1	Noise source temperature monitor		12			1
	C	NSBH	2	0.001	200K noise source, receiver B	2000		2		
	C	NSBL	2	0.001	2K noise source, receiver B	2000		2		
Cryogenics M/C	C	CA	2	1	Receiver A cryogenic mode (heat, cool, off)	2		2		
	M	CAV	12	1	Receiver A vacuum monitor		12			1
	M	CAT	12	1	Receiver A temperature monitor		12			1
	C	CAH	2	1	Receiver A outside window heater/blower	2		2		
	C	CB	2	1	Receiver B cryogenic mode (heat, cool, off)	2		2		
	M	CBV	12	1	Receiver B vacuum monitor		12			1
	M	CBT	12	1	Receiver B temperature monitor		12			1
	C	CBH	2	1	Receiver B outside window heater/blower	2		2		
LNA Bias Monitor	M	LNAVA	12	1	LNA drain current, verical polarization, receiver A		12			1
	M	LNAHA	12	1			12			1
	M	LNAVB	12	1			12			1
	M	LNAHB	12	1			12			1
Housekeeping										
Current monitor, +5V	M	V1	12	1			12			1
Current monitor, +15V	M	V2	12	1			12			1
Current monitor, -15V	M		12	1			12			1
Current monitor, 24V	M		12	1			12			1
Volage monitor, +5V	M		12	1			12			1
Voltage monitor, +15V	M		12	1			12			1
Voltage monitor, -15V	M		12	1			12			1
Voltage monitor, 24V	M		12	1			12			1
Temperature monitor	M		12	1			12			1
Temperature monitor	M		12	1			12			1
Temperature monitor	M		12	1			12			1
Temperature monitor	M		12	1			12			1
					Totals	**12,814**	**384,336**	**186**	**36**	**22**