

GPIO ASSIGNMENT

PIN	De	fine	CFG	Function
PIN	De	rine	LFG	Function
PAO	THS	PERVVBUSO	3/1	
PAl	TCK	/DRVVBUS1	3/1	JTAG /USB
PA2	TD	D/WPS	3/1	7058
PA3	TDI		3	1
PA4	UAR	T-TX	3	
PA5	UAR	T-RX	3	UART
PA6		NC	7	
PA7		NC	7	
PA8		NC	7	1
PA9		NC	7	-
PA10		NC	7	1
PA11	WA	KE-HOST	0	GPIO
PA12		NC	7	
PA13		NC	7	†
PA14		NC	7	
PA15	ST	ATUS-LED	1	LED
PA16		NC	1	
PA17		NC	2	
PA18		NC	7	
PA19		NC	7	1
PA20		NC	7	
PA21		NC	7	

	Define	CFG	Function
C0	NWE	2/3	
C1	NALE	2/3	1
C2	NCLE	2/3	1
C3	NCE1	2/3	1
C4	NCE0	2	1
C5	NRE	2/3	1
C6	NRB0	2/3	NAND
C7	NRB1	2	/eMMC /NOR
C8	NDQ0	2/3	
C9	NDQ1	2/3	
C10	NDQ2	2/3	1
C11	NDQ3	2/3	
C12	NDQ4	2/3	
C13	NDQ5	2/3	
C14	NDQ6	2/3	
C15	NDQ7	2/3	
C16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	GND	7	
PD2	GND	7	Ä
PD3	GND	7	不能能改本组gpio状态
PD4	GND	7	· 500 · 400 · 400
PD5	GND	7	甾GF
PD6	GND	7	# oiv
PD7	GND	7	(4)
PD8	GND	7	1
PD9	GND	7	
PD10	GND	7	
PD11	GND	7	
PD12	GND	7	
PD13	GND	7	
PD14	GND	7	
PD15	GND	7	
PD16	GND	7	
PD17	NC	7	

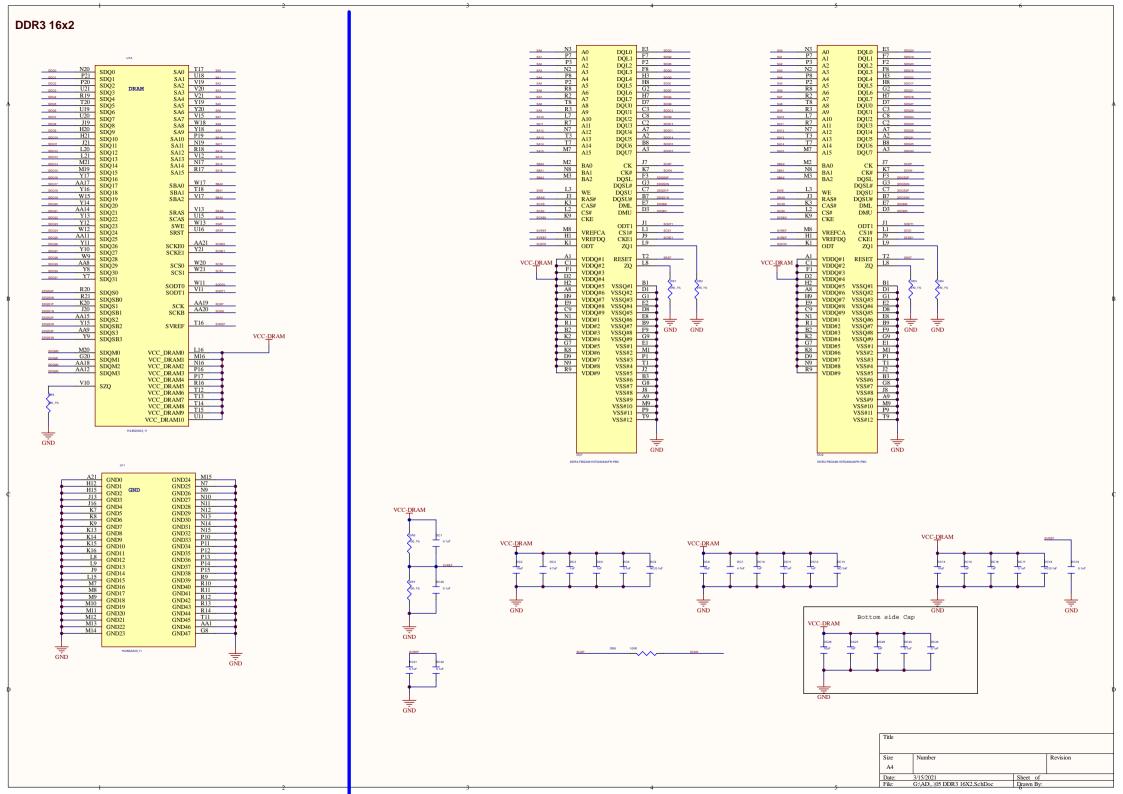
PIN	Define	CFG	Function
PE0	NC	7	
PE1	NC	7	1
PE2	NC	7	1
PE3	NC	7	1
PE4	NC	7	1
PE5	NC	7	
PE6	NC	7	
PE7	NC	7	1
PE8	NC	7	
PE9	NC	7	
PE10	NC	7	
PE11	NC	7	1
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	†

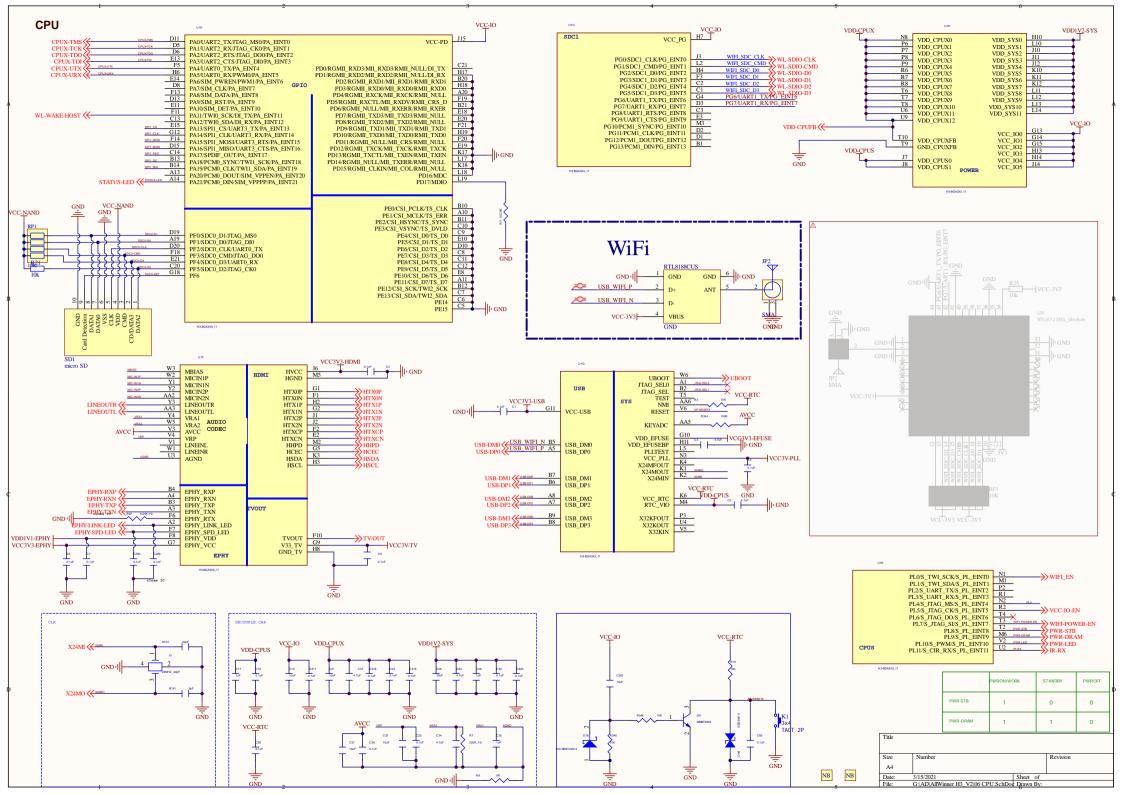
PIN	Define	CFG	Function
PF0	NC	2	
PF1	NC	2	
PF2	NC	2	
PF3	NC	2	
PF4	NC	2	
PF5	NC	2	
PF6	DET	0	

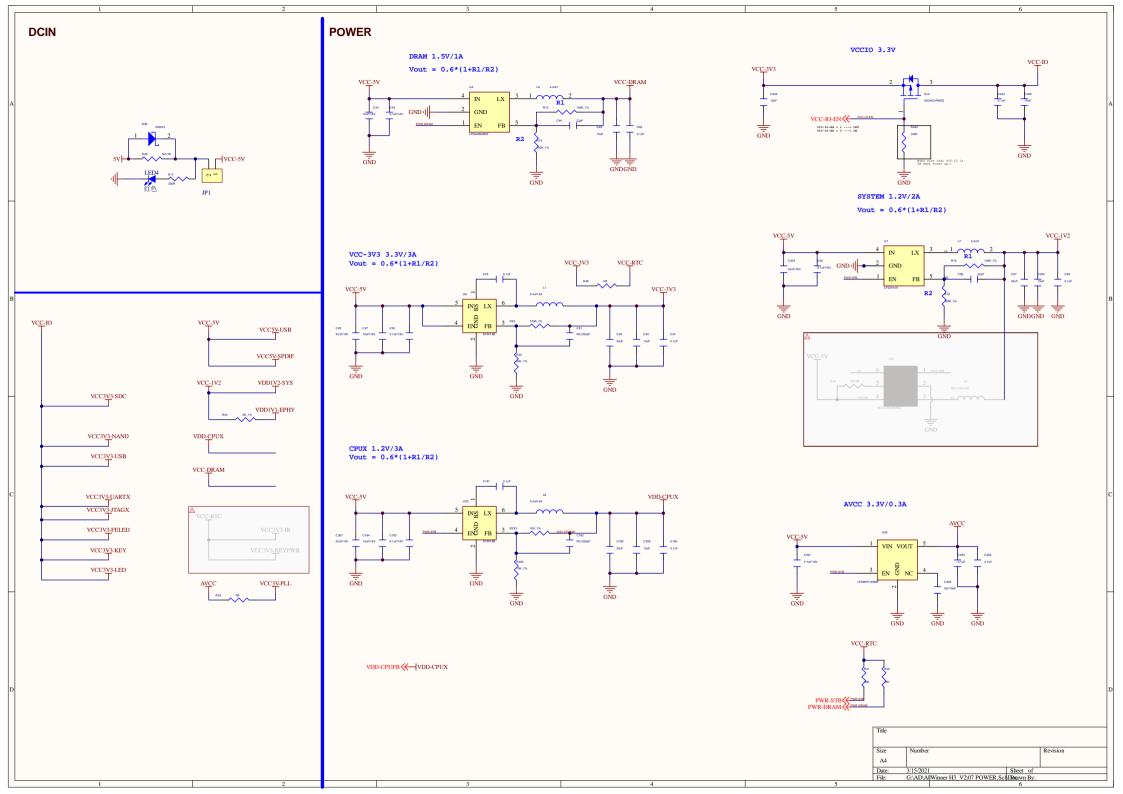
	Derrine	0.0	unccion
PG0	CLK	7	SB
PG1	CMD	7	SDIO-WIFI
PG2	D0	7	IPI
PG3	D1	7	1
PG4	D2	7	
PG5	D3	7	
PG6	NC	7	
PG7	NC	7	
PG8	NC	7	
PG9	NC	7	
PG10	NC	7	
PG11	NC	7	
PG12	NC	7	
PG13	NC	7	

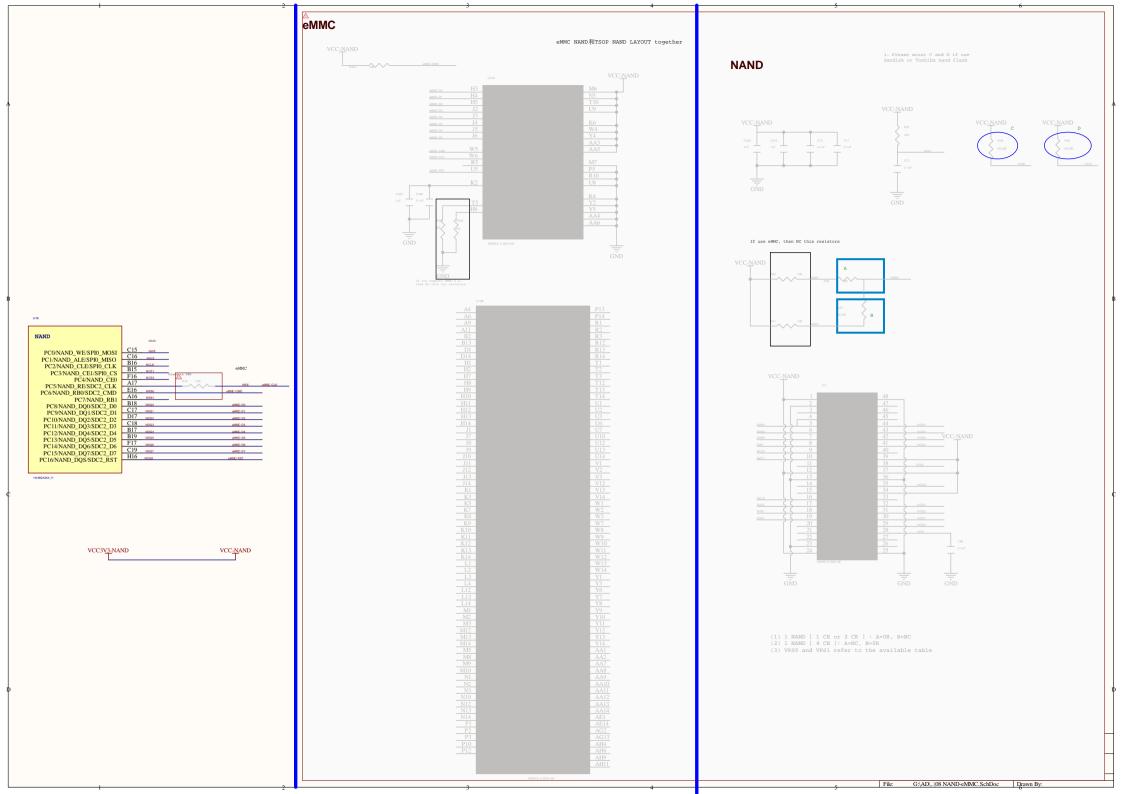
PIN	Define	CFG	Function
PL0	WIFI_EN	2	WIFI_EN
PL1	NC	2	
PL2	NC	1	
PL3	NC	1	†
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	NC	7	
PL7	WIFI-PWR-EN	7	
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

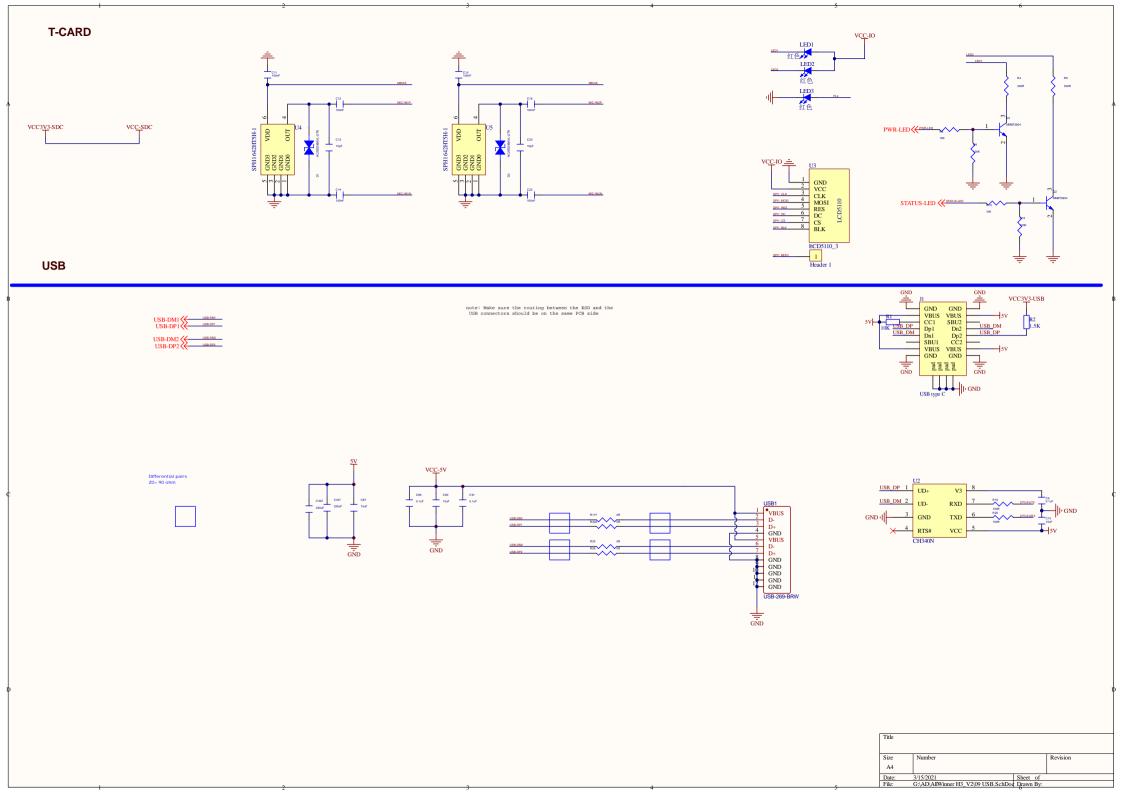
Title		
Size	Number	Revision
A4		
Date:	3/15/2021	Sheet of
File:	G:\AD\\04 GPIO ASSIGNMENT.S	chDocDrawn By:

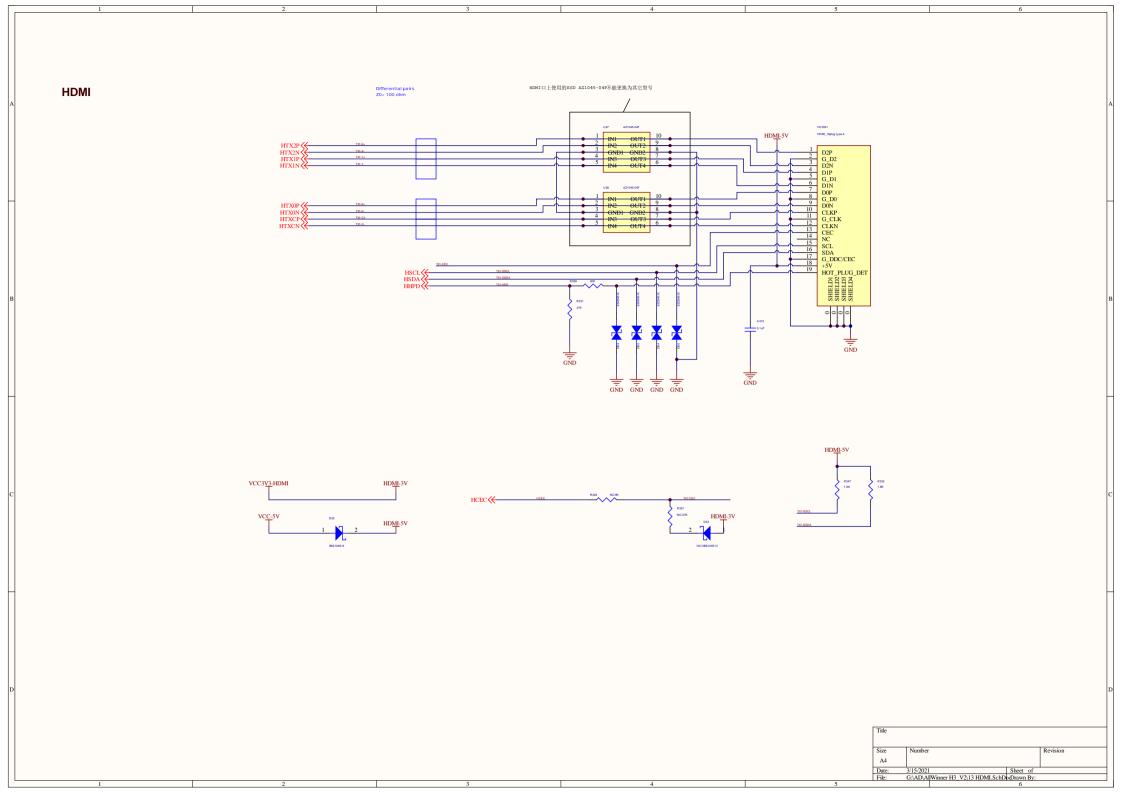




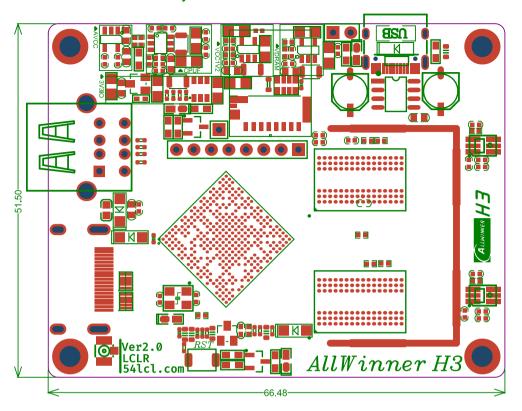






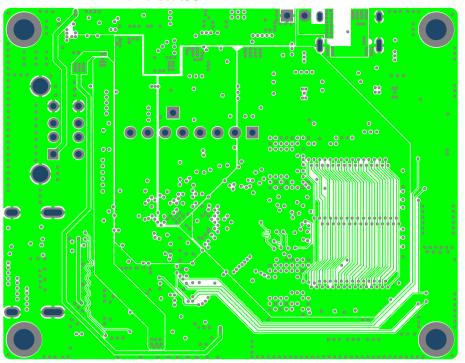


TOP Overlayer



GND02

PWR03



Bottom Overlayer

