Chenglong **Li**

Computer Network · PhD. Student

College of Computer, National University of Defense Technology, Changsha, China

lichenglong17@nudt.edu.cn | LCLinVictory

Summary

Current a PhD. student in College of Computer, National University of Defense Technology. Research interest includes SDN, hardware/software co-design and Time-Sensitive Network. Proficient at C/C++, Verilog development. Familiar with Linux kernel, network driver . Interested in devising a better problem-solving method for challenging tasks, and learning new technologies and tools if the need arises.

Education

NUDT(National University of Defense Technology) *Changsha, China*

PhD. Student in Computer Science and Technology (College of Computer) *Sept. 2020 - Now*

- PhD. candidates ranked 2/19.

NUDT(National University of Defense Technology) *Changsha, China*

M.S. in Cyberspace Security (College of Computer) *Sept. 2017 - Jul. 2020*

- Awarded for outstanding performance.

HIT(Harbin Institute of Technology) *Harbin, China*

B.S. in Information Security (College of Computer) *Sept. 2013 - Jul. 2017*

- Awarded the title of outstanding graduates.

Professional Background

Major Courses

Master *NUDT, China*

Focus on Computer Network

- Advanced Computer Network (B), Router Principle and Design (A), Cyberspace Security Synthesis (High performance trusted Network) (B).

Undergraduate *HIT, China*

Focus on Development Basics

- Computer Network (100/100), Database System (98.4/100), Operating System (91/100), Software Engineering (88/100), Digital Logic Design (92/100), Computer Composition Principle (87.5/100).

Awards

2017 **Meritorious Winner,** Mathematical Contest In Modeling Certificate of Achievement *U.S.A*

Publications

Enabling Packet Classification with Low Update Latency for SDN Switch on FPGA *Sustainability 2020*

Chenglong Li, Tao Li, Junnan Li, Zilin Shi, Baosheng Wang *SCI Indexed.*

Update Latency Optimization of Packet Classification for SDN Switch on FPGA *IEEE FCCM 2020*

Chenglong Li, Tao Li, Junnan Li, Zilin Shi, Baosheng Wang *EI Indexed.*

Memory Optimization for Bit-Vector-Based Packet Classification on FPGA *Electronics 2019*

Chenglong Li, Tao Li, Junnan Li, Dagang Li, Hui Yang, Baosheng Wang *SCI Indexed.*

Brief Announcement : A Memory Optimized Architecture for Multi-Field Packet Classification *ACM SPAA 2019*

Chenglong Li, Tao Li, Junnan Li, Hui Yang, Baosheng Wang *EI Indexed.*

MsBV: A Memory Compression Scheme for Bit-Vector-Based Classification Lookup Tables *IEEE Access 2020*

Zilin Shi, Hui Yang, Junnan Li, **Chenglong Li**, Tao Li, Baosheng Wang *SCI Indexed.*

PipeCache: High Hit Rate Rule-Caching Scheme Based on Multi-Stage Cache Tables *Electronics 2020*

Jialun Yang, Tao Li, Jinli Yan, Junnan Li, **Chenglong Li**, Baosheng Wang. *SCI Indexed*

Selected Projects

Packet Classification system for Software-Defined-Network *NUDT, China*

Laboratory Project *Mar. 2019 - Sept. 2019*

- A hardware packet classification pipeline on FPGA for SDN switches.
- Optimized schemes based on Bit-Vector (BV) algorithm for Memory Consumption and Update Latency.
- Supporting various kind rules: including Accessing Control List (ACL), Firewall, IP Chain (IPC) and OpenFlow 1.0.

DNS Authoritative Server FPGA-accelerated Design. *NUDT, China*

Laboratory Project *Mar. 2018 - Jun. 2018*

- Using the perfect hash algorithm to avoid hash conflict, offload the DNS authoritative query response into a pipeline on FPGA.
- A hardware/software co-acceleration architecture designed based on the FAST platform of the research group.

Reverse Analysis and Blocking of FASP Protocol. *HIT, China*

Laboratory Project *Mar. 2017 - Jun. 2017*

- Conversing analysis of the famous private data transmission protocol FASP in the field of biological information.
- Obtained the transmission mechanism and main command field format.
- A blocking technique is proposed using the Netfilter framework in Linux.

Presentation

Update Latency Optimization of Packet Classification for SDN Switch on FPGA *IEEE FCCM 2020, Fayetteville, Arkansas, U.S.A*

Poster Session 2: Datacenter and Infrastructure *May. 3-6, 2020*

- Introduced the SplitBV which can provide update latency guarantee for the BV-based packet classification.
- Showed that our approach can reduce 73% and 36% update latency on average for 5-tuple rules and OpenFlow1.0 rules respectively.

A Memory Optimized Architecture for Multi-Field Packet Classification *ACM SPAA 2019, Phoenix, AZ, U.S.A*

Brief Announcement Speaker *Jun. 22-24, 2019*

- Introduced the WeeBV which can reduce memory consumption for the BV-based packet classification.
- Showed that our approach can reduce 37% and 41% memory consumption on average for 5-tuple rules and OpenFlow1.0 rules respectively.

The survey and improvement of BV-based packet classification algorithm *Yang Tong's Group, Peking University, China*

Speaker at <Seminar on Network switching and Table Lookup Technology> *Dec. 25, 2018*

- Introduced the research review of the Bit-Vector (BV)-based packet classification.
- Introduced how to reduce the memory consumption for BV-based algorithm without damaging high performance.

Extracurricular Activity

Sports Hobby

- Road running (3 times a week, 3Km each time).
- Cycling (achieved 20Km tour of Moon Island in Changsha City).
- Skiing (learned at fifteen, my hometown is famous as *"The Ice City"*).