

LCR CHASSIS MANAGER

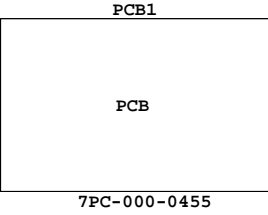
9/9/2024:
Removed C31, C48-C50, C121, C124, C440-C443, C455-C457, C460-C464, C532-C534

9/10/2024:
Reduced size of R37, R38, R207, R208, R228, R232, R233, R417 from 0402 to 0201
Reduced size of C54, C55 from 0603 to 0402

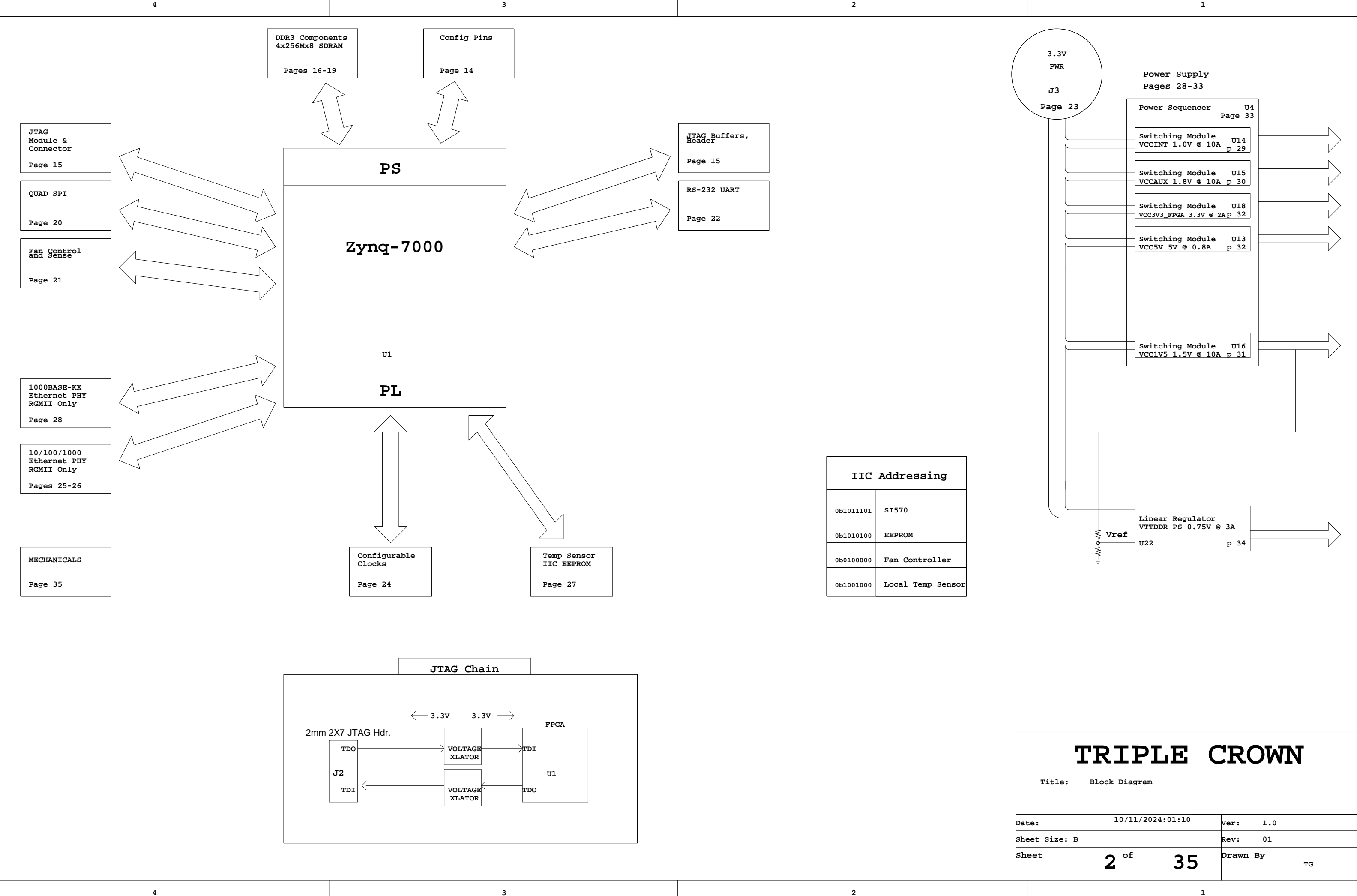
10/22/2024:
Changed part number of U35 from 88E1116R to 88E1512
Added L13-L15, C31, C48, C49
Removed C34, C38, C39, C41, C52, R15, R46-R49, R245, R247, R248

10/31/2024:
Disconnected 4 mounting holes from GND and connected to CHASSIS-1_GND
Disconnected 4 mounting holes from GND and connected to CHASSIS-2_GND
Added C38, C39, C41, C121 between CHASSIS-1_GND and GND
Added C34, C50, C52, C124 between CHASSIS-2_GND and GND
Swapped some DDR3 DQ signals within byte groupings 0, 1, 2, 3

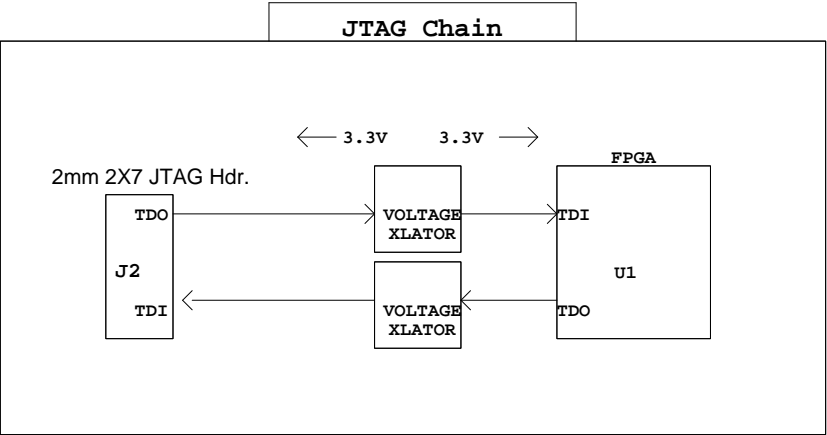
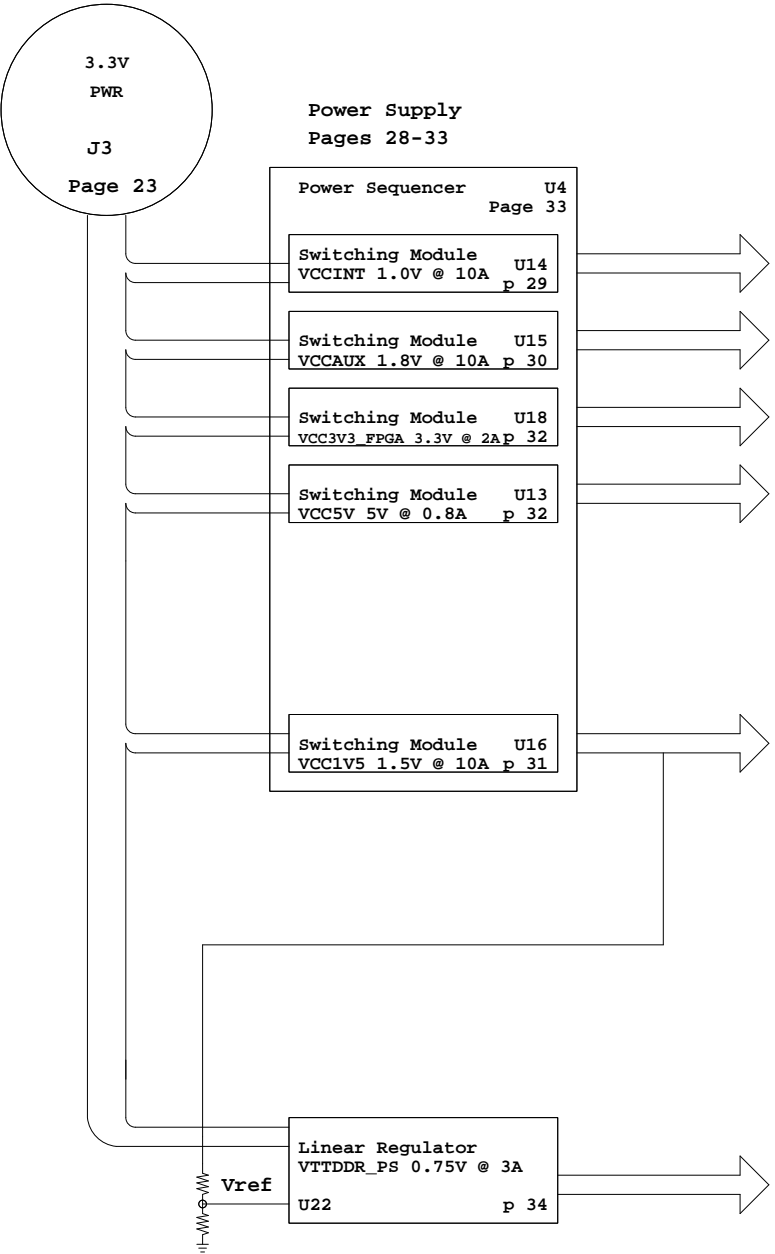
11/8/2024:
Removed C433, C434, C444, C465-C467
Changed C148 part number to C1608X5R1A106K080AC
Changed PCB part number from 7PC-000-0455.PCB to 7PC-000-0455



TRIPLE CROWN			
Title:		ASSY P/N: 7CM-100-0001-1	
LCR CHASSIS MANAGER		PCB P/N: 7PC-000-0455	
		SCH P/N: 7PC-000-0455-SCH.SCH	
Date:	10/11/2024:01:10	Ver:	1.0
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IIC Addressing	
0b1011101	SI570
0b1010100	EEPROM
0b0100000	Fan Controller
0b1001000	Local Temp Sensor



TRIPLE CROWN			
Title: Block Diagram			
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XC7Z020

BANK 13
XC7Z020CLG484

VCC3V3_FPGA

AA10 VCCO_13_AA10
AB3 VCCO_13_AB3
T5 VCCO_13_T5
U8 VCCO_13_U8
V11 VCCO_13_V11
W4 VCCO_13_W4
Y7 VCCO_13_Y7

IO_0_13_R7
IO_L1P_T0_13_V10
IO_L1N_T0_13_V9
IO_L2P_T0_13_V8
IO_L2N_T0_13_W8
IO_L3P_T0_DQS_13_W11
IO_L3N_T0_DQS_13_W10
IO_L4P_T0_13_V12
IO_L4N_T0_13_W12
IO_L5P_T0_13_U12
IO_L5N_T0_13_U11
IO_L6P_T0_13_U10
IO_L6N_T0_VREF_13_U9
IO_L7P_T1_13_AA12
IO_L7N_T1_13_AB12
IO_L8P_T1_13_AA11
IO_L8N_T1_13_AB11
IO_L9P_T1_DQS_13_AB10
IO_L9N_T1_DQS_13_AB9
IO_L10P_T1_13_Y11
IO_L10N_T1_13_Y10
IO_L11P_T1_SRCC_13_AA9
IO_L11N_T1_SRCC_13_AA8
IO_L12P_T1_MRCC_13_Y9
IO_L12N_T1_MRCC_13_Y8
IO_L13P_T2_MRCC_13_Y6
IO_L13N_T2_MRCC_13_Y5
IO_L14P_T2_SRCC_13_AA7
IO_L14N_T2_SRCC_13_AA6
IO_L15P_T2_DQS_13_AB2
IO_L15N_T2_DQS_13_AB1
IO_L16P_T2_13_AB5
IO_L16N_T2_13_AB4
IO_L17P_T2_13_AB7
IO_L17N_T2_13_AB6
IO_L18P_T2_13_Y4
IO_L18N_T2_13_AA4
IO_L19P_T3_13_R6
IO_L19N_T3_VREF_13_T6
IO_L20P_T3_13_T4
IO_L20N_T3_13_U4
IO_L21P_T3_DQS_13_V5
IO_L21N_T3_DQS_13_V4
IO_L22P_T3_13_U6
IO_L22N_T3_13_U5
IO_L23P_T3_13_V7
IO_L23N_T3_13_W7
IO_L24P_T3_13_W6
IO_L24N_T3_13_W5
IO_25_13_U7

R7 NC=
V10 NC=
V9 NC=
V8 NC=
W8 NC=
W11 NC=
W10 BP GPIO OUT5 23
V12 TEMP SENSE2_SCL 23
W12 TEMP SENSE2_SDA 23
U12 BP GPIO IN0 23
U11 BP GPIO IN1 23
U10 BP GPIO IN2 23
U9 BP GPIO IN3 23
AA12 BP GPIO IN4 23
AB12 BP GPIO IN5 23
AA11 BP GPIO IN6 23
AB11 BP GPIO IN7 23
AB10 NC=
AB9 NC=
Y11 NC=
Y10 NC=
AA9 NC=
AA8 NC=
Y9 NC=
Y8 NC=
Y6 NC=
Y5 NC=
AA7 NC=
AA6 NC=
AB2 IIC_SCL_MAIN_LS 27
AB1 IIC_SDA_MAIN_LS 27
AB5 TEMP SENSE4_SCL 23
AB4 TEMP SENSE4_SDA 23
AB7 TEMP SENSE3_SCL 23
AB6 TEMP SENSE3_SDA 23
Y4 UART0_A0 23
AA4 UART0_A1 23
R6 UART0_A2 23
T6 UART0_A3 23
T4 UART0_EN 23
U4 NC=
V5 NC=
V4 NC=
U6 NC=
U5 NC=
V7 BP GPIO OUT4 23
W7 BP GPIO OUT1 23
W6 BP GPIO OUT0 23
W5 BP GPIO OUT3 23
U7 NC=

U1

Zynq Bank 13

TRIPLE CROWN

Title: Zynq Bank 13

Date:	10/11/2024:01:10	Ver:	1.0
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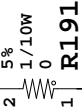
XC7Z020

BANK 33
XC7Z020CLG484

VCC3V3_FPGA

AA20	VCCO_33_AA20
AB13	VCCO_33_AB13
U18	VCCO_33_U18
V21	VCCO_33_V21
W14	VCCO_33_W14
Y17	VCCO_33_Y17

IO_0_33_U19	U19	FAN_FULL_SPEED_R_N	21
IO_L1P_T0_33_T21	T21	NC=	
IO_L1N_T0_33_U21	U21	NC=	
IO_L2P_T0_33_T22	T22	NC=	
IO_L2N_T0_33_U22	U22	NC=	
IO_L3P_T0_DQS_33_V22	V22	NC=	
IO_L3N_T0_DQS_33_W22	W22	NC=	
IO_L4P_T0_33_W20	W20	NC=	
IO_L4N_T0_33_W21	W21	NC=	
IO_L5P_T0_33_U20	U20	NC=	
IO_L5N_T0_33_V20	V20	NC=	
IO_L6P_T0_33_V18	V18	NC=	
IO_L6N_T0_VREF_33_V19	V19	NC=	
IO_L7P_T1_33_AA22	AA22	UART1_RX	22
IO_L7N_T1_33_AB22	AB22	UART1_TX	22
IO_L8P_T1_33_AA21	AA21	BP_GPIO_OUT7	23
IO_L8N_T1_33_AB21	AB21	BP_GPIO_OUT6	23
IO_L9P_T1_DQS_33_Y20	Y20	PS2_FAIL#	23
IO_L9N_T1_DQS_33_Y21	Y21	PS1_FAIL#	23
IO_L10P_T1_33_AB19	AB19	FAN_FAIL_N	21,4
IO_L10N_T1_33_AB20	AB20	IPMB-A_SDA	23
IO_L11P_T1_SRCC_33_Y19	Y19	NC=	
IO_L11N_T1_SRCC_33_AA19	AA19	NC=	
IO_L12P_T1_MRCC_33_Y18	Y18	NC=	
IO_L12N_T1_MRCC_33_AA18	AA18	NC=	
IO_L13P_T2_MRCC_33_W17	W17	BP_GPIO_OUT2	23
IO_L13N_T2_MRCC_33_W18	W18	NC=	
IO_L14P_T2_SRCC_33_W16	W16	NC=	
IO_L14N_T2_SRCC_33_Y16	Y16	NC=	
IO_L15P_T2_DQS_33_U15	U15	FAN_SCL	21
IO_L15N_T2_DQS_33_U16	U16	FAN_SDA	21
IO_L16P_T2_33_U17	U17	TEMP_SENSE1_SCL	23
IO_L16N_T2_33_V17	V17	TEMP_SENSE1_SDA	23
IO_L17P_T2_33_AA17	AA17	PS1_INH#	23
IO_L17N_T2_33_AB17	AB17	PS_ENABLE#	23
IO_L18P_T2_33_AA16	AA16	NVMRO	23
IO_L18N_T2_33_AB16	AB16	SYSRESET#	23
IO_L19P_T3_33_V14	V14	IPMB-B_SDA	23
IO_L19N_T3_VREF_33_V15	V15	IPMB-B_SCL	23
IO_L20P_T3_33_V13	V13	NC=	
IO_L20N_T3_33_W13	W13	NC=	
IO_L21P_T3_DQS_33_W15	W15	NC=	
IO_L21N_T3_DQS_33_Y15	Y15	NC=	
IO_L22P_T3_33_Y14	Y14	NC=	
IO_L22N_T3_33_AA14	AA14	UART0_TX	23
IO_L23P_T3_33_Y13	Y13	IPMB-A_SCL	23
IO_L23N_T3_33_AA13	AA13	UART0_RX	23
IO_L24P_T3_33_AB14	AB14	G_DISC#	23
IO_L24N_T3_33_AB15	AB15	PS2_INH#	23
IO_25_33_U14	U14	NC=	



R191

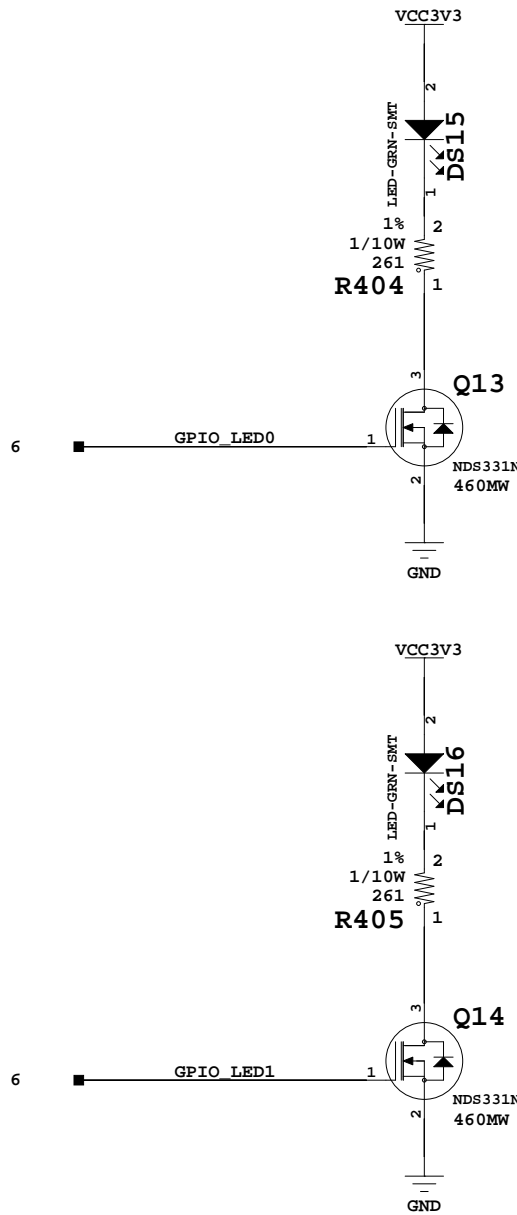
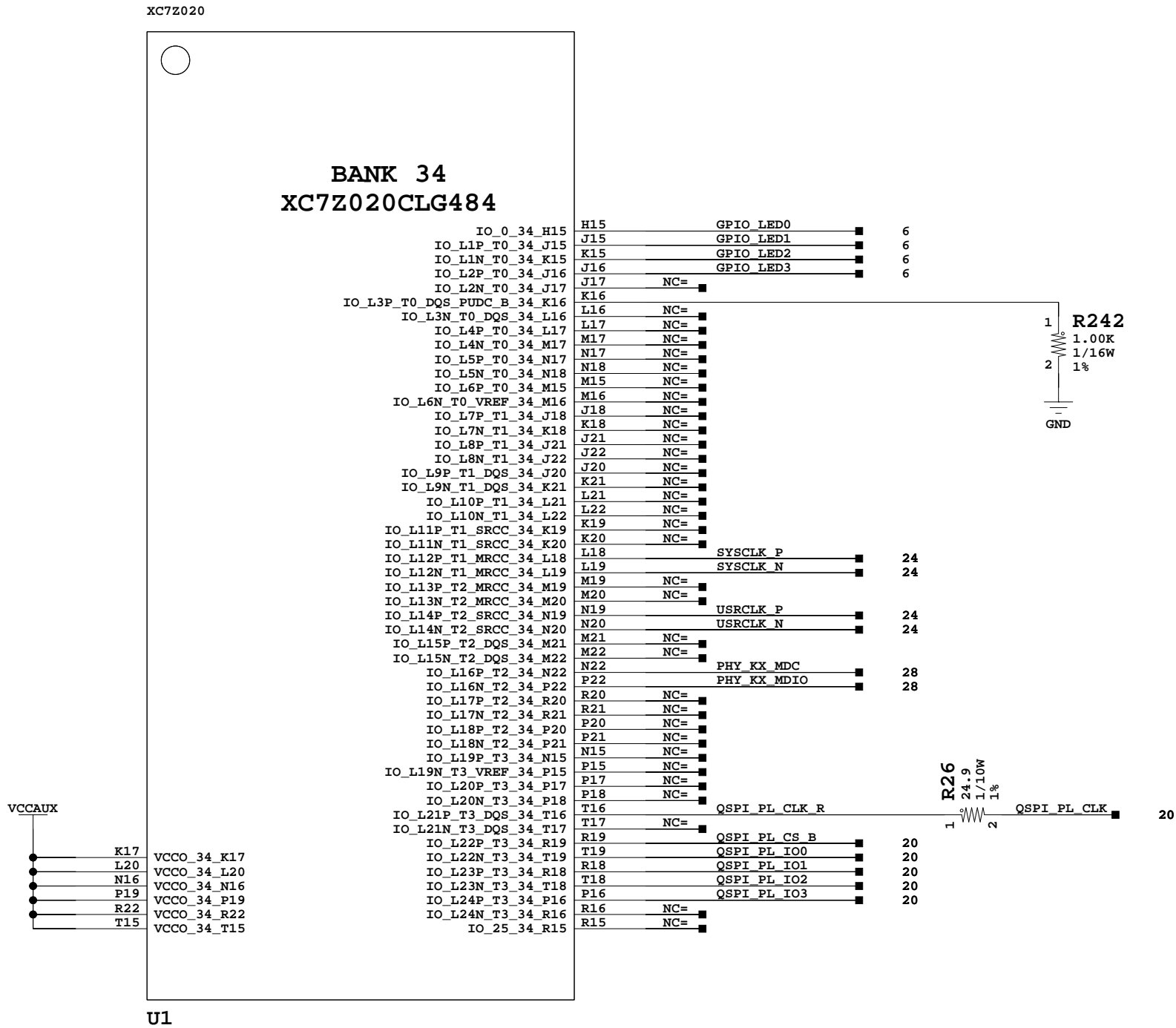
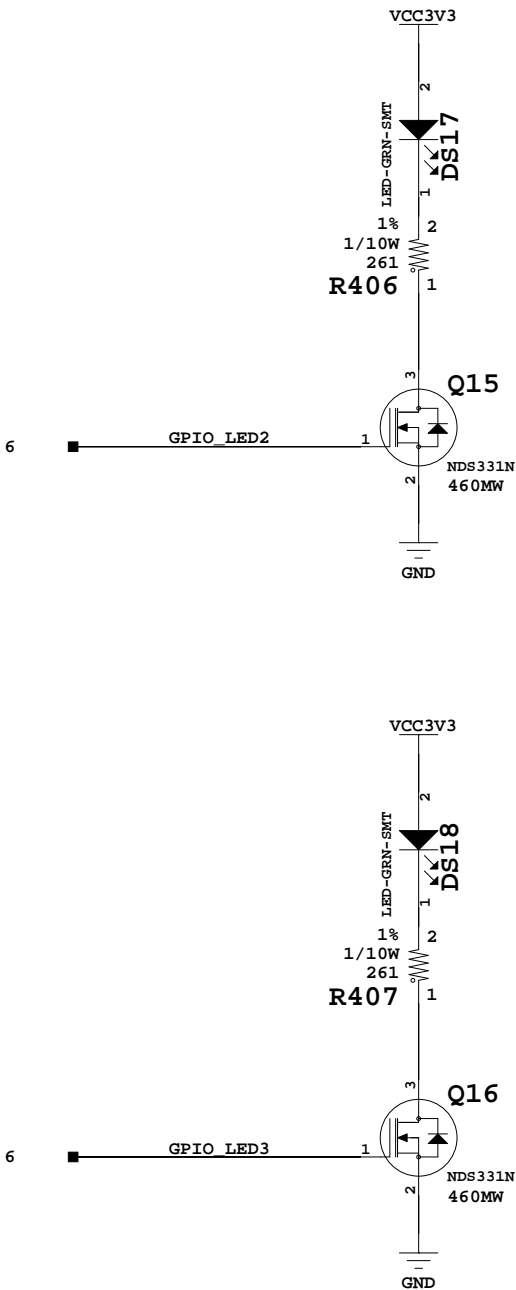
U1

Zynq Bank 33

TRIPLE CROWN

Title: Zynq Bank 33

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Zynq Bank 34

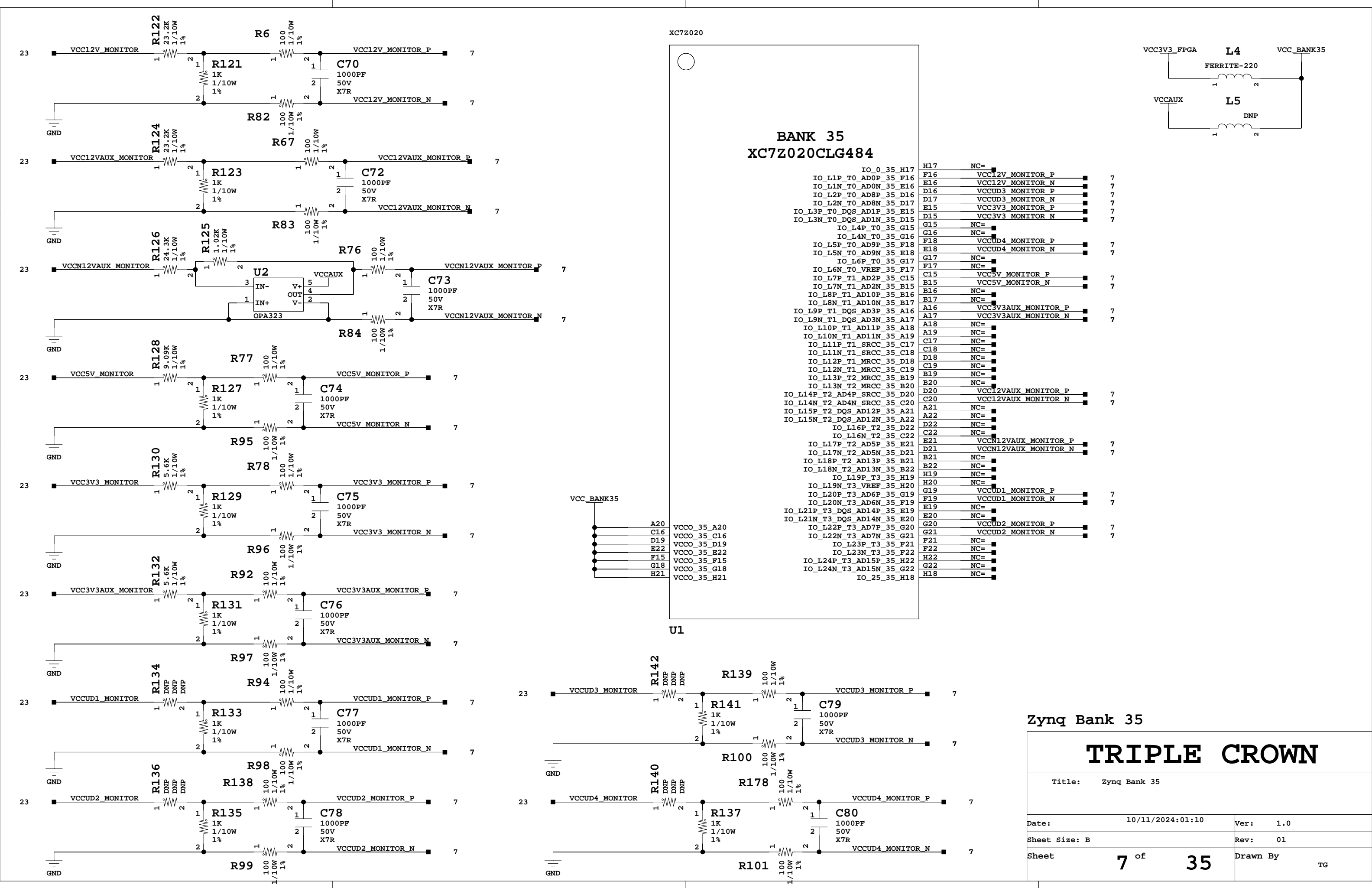
TRIPLE CROWN

Title: Zynq Bank 34

Date: 10/11/2024:01:10 Ver: 1.0

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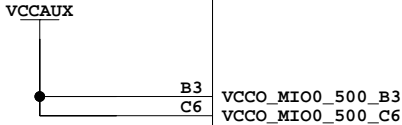
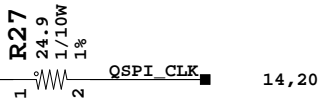


Zynq Bank 35		
TRIPLE CROWN		
Title: Zynq Bank 35		
Date: 10/11/2024:01:10	Ver: 1.0	
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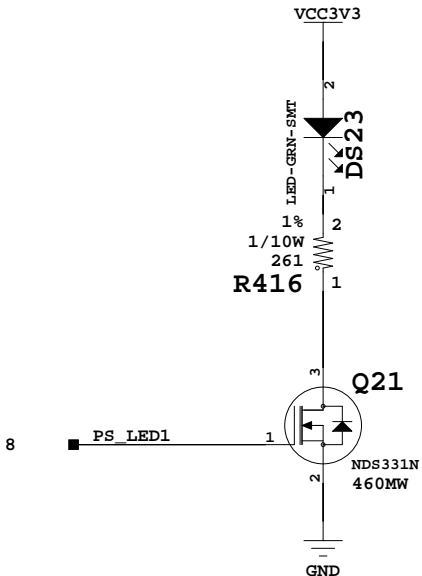
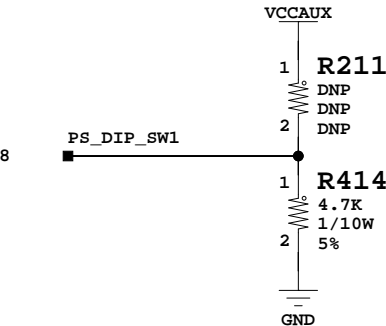
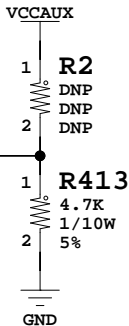
XC7Z020

BANK 500
XC7Z020CLG484

PS_CLK_500_F7	F7	PS_CLK	24
PS_POR_B_500_B5	B5	PS_POR_B	20, 25, 28, 33
PS_MIO15_500_E6	E6	NC=	
PS_MIO14_500_B6	B6	PS_DIP_SW0	8
PS_MIO13_500_A6	A6	NC=	
PS_MIO12_500_C5	C5	PS_DIP_SW1	8
PS_MIO11_500_B4	B4	PHY_RESET_B_AND	25
PS_MIO10_500_G7	G7	PS_LED1	8
PS_MIO9_500_C4	C4	PHY_KX_RESET_B_AND	28
PS_MIO8_500_E5	E5	PS_MIO8_LED0	8
PS_MIO7_500_D5	D5	QSPI_PL_RESET_B_AND	20
PS_MIO6_500_A4	A4	QSPI_CLK_R	
PS_MIO5_500_A3	A3	QSPI_IO3	14, 20
PS_MIO4_500_E4	E4	QSPI_IO2	14, 20
PS_MIO3_500_F6	F6	QSPI_IO1	14, 20
PS_MIO2_500_A2	A2	QSPI_IO0	14, 20
PS_MIO1_500_A1	A1	QSPI_CS_B	20
PS_MIO0_500_G6	G6	NC=	



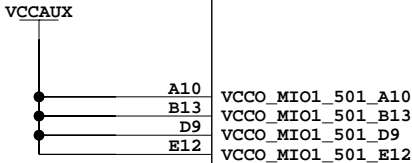
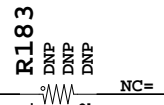
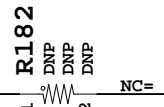
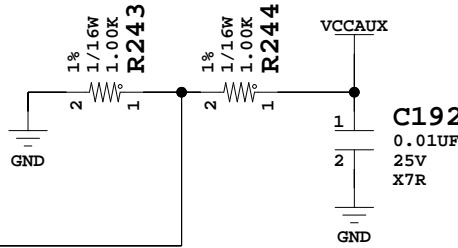
U1



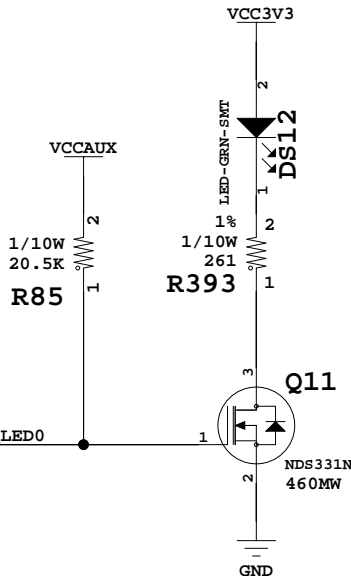
XC7Z020

BANK 501
XC7Z020CLG484

PS_MIO_VREF_501_F8	F8	PS_MIO_VREF_501_F8	
PS_MIO17_501_E9	E9	PHY_TXD0	25
PS_MIO19_501_E10	E10	PHY_TXD2	25
PS_MIO21_501_F11	F11	PHY_TX_CTRL	25
PS_MIO23_501_E11	E11	PHY_RXD0	25
PS_MIO25_501_F12	F12	PHY_RXD2	25
PS_MIO27_501_D7	D7	PHY_RX_CTRL	25
PS_MIO29_501_E8	E8	PHY_KX_TXD0	28
PS_MIO31_501_F9	F9	PHY_KX_TXD2	28
PS_MIO33_501_G13	G13	PHY_KX_TX_CTRL	28
PS_MIO35_501_F14	F14	PHY_KX_RXD0	28
PS_MIO38_501_F13	F13	PHY_KX_RXD3	28
PS_MIO40_501_E14	E14	NC=	
PS_MIO42_501_D8	D8	NC=	
PS_MIO44_501_E13	E13	NC=	
PS_MIO46_501_D12	D12	NC=	
PS_MIO48_501_D11	D11	NC=	
PS_MIO50_501_D13	D13	PS_SCL_MAIN	
PS_MIO52_501_D10	D10	PHY_MDC	25
PS_SRST_B_501_C9	C9	PS_SRST_B	15
PS_MIO16_501_D6	D6	PHY_TX_CLK	25
PS_MIO18_501_A7	A7	PHY_TXD1	25
PS_MIO20_501_A8	A8	PHY_TXD3	25
PS_MIO22_501_A14	A14	PHY_RX_CLK	25
PS_MIO24_501_B7	B7	PHY_RXD1	25
PS_MIO26_501_A13	A13	PHY_RXD3	25
PS_MIO28_501_A12	A12	PHY_KX_TX_CLK	28
PS_MIO30_501_A11	A11	PHY_KX_TXD1	28
PS_MIO32_501_C7	C7	PHY_KX_TXD3	28
PS_MIO34_501_B12	B12	PHY_KX_RX_CLK	28
PS_MIO36_501_A9	A9	PHY_KX_RXD1	28
PS_MIO37_501_B14	B14	PHY_KX_RXD2	28
PS_MIO39_501_C13	C13	PHY_KX_RX_CTRL	28
PS_MIO41_501_C8	C8	NC=	
PS_MIO43_501_B11	B11	NC=	
PS_MIO45_501_B9	B9	NC=	
PS_MIO47_501_B10	B10	NC=	
PS_MIO49_501_C14	C14	NC=	
PS_MIO51_501_C10	C10	PS_SDA_MAIN	
PS_MIO53_501_C12	C12	PHY_MDIO	25



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Zynq Banks 500, 501

TRIPLE CROWN

Title: Zynq Banks 500, 501

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XC7Z020

BANK 502
XC7Z020CLG484

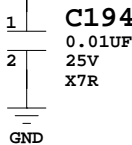
PS_DDR_DRST_B_502_F3	F3	PS_DDR3_RESET_B	16,17,18,19
PS_DDR_DQ0_502_D1	D1	PS_DDR3_DQ3	16
PS_DDR_DQ1_502_C3	C3	PS_DDR3_DQ4	16
PS_DDR_DQ2_502_B2	B2	PS_DDR3_DQ0	16
PS_DDR_DQ3_502_D3	D3	PS_DDR3_DQ2	16
PS_DDR_DM0_502_B1	B1	PS_DDR3_DM0	16
PS_DDR_QS_P0_502_C2	C2	PS_DDR3_QS0_P	16
PS_DDR_QS_N0_502_D2	D2	PS_DDR3_QS0_N	16
PS_DDR_DQ4_502_E3	E3	PS_DDR3_DQ6	16
PS_DDR_DQ5_502_E1	E1	PS_DDR3_DQ7	16
PS_DDR_DQ6_502_F2	F2	PS_DDR3_DQ5	16
PS_DDR_DQ7_502_F1	F1	PS_DDR3_DQ1	16
PS_DDR_DQ8_502_G2	G2	PS_DDR3_DQ8	16
PS_DDR_DQ9_502_G1	G1	PS_DDR3_DQ10	17
PS_DDR_DQ10_502_L1	L1	PS_DDR3_DQ9	17
PS_DDR_DQ11_502_L2	L2	PS_DDR3_DQ13	17
PS_DDR_DM1_502_H3	H3	PS_DDR3_DM1	17
PS_DDR_QS_P1_502_H2	H2	PS_DDR3_QS1_P	17
PS_DDR_QS_N1_502_J2	J2	PS_DDR3_QS1_N	17
PS_DDR_DQ12_502_L3	L3	PS_DDR3_DQ14	17
PS_DDR_DQ13_502_K1	K1	PS_DDR3_DQ11	17
PS_DDR_DQ14_502_J1	J1	PS_DDR3_DQ12	17
PS_DDR_DQ15_502_K3	K3	PS_DDR3_DQ15	17
PS_DDR_A14_502_G4	G4	PS_DDR3_A14	16,17,18,19
PS_DDR_A13_502_F4	F4	PS_DDR3_A13	16,17,18,19
PS_DDR_A12_502_H4	H4	PS_DDR3_A12	16,17,18,19
PS_DDR_A11_502_G5	G5	PS_DDR3_A11	16,17,18,19
PS_DDR_A10_502_J3	J3	PS_DDR3_A10	16,17,18,19
PS_DDR_A9_502_H5	H5	PS_DDR3_A9	16,17,18,19
PS_DDR_A8_502_J5	J5	PS_DDR3_A8	16,17,18,19
PS_DDR_A7_502_J6	J6	PS_DDR3_A7	16,17,18,19
PS_DDR_A6_502_J7	J7	PS_DDR3_A6	16,17,18,19
PS_DDR_A5_502_K5	K5	PS_DDR3_A5	16,17,18,19
PS_DDR_A4_502_K6	K6	PS_DDR3_A4	16,17,18,19
PS_DDR_A3_502_L4	L4	PS_DDR3_A3	16,17,18,19
PS_DDR_VRN_502_M7	M7	PS_VRN	9
PS_DDR_VRP_502_N7	N7	PS_VRP	9
PS_DDR_CKP_502_N4	N4	PS_DDR3_CLK_P	16,17,18,19
PS_DDR_CKN_502_N5	N5	PS_DDR3_CLK_N	16,17,18,19
PS_DDR_A2_502_K4	K4	PS_DDR3_A2	16,17,18,19
PS_DDR_A1_502_M5	M5	PS_DDR3_A1	16,17,18,19
PS_DDR_A0_502_M4	M4	PS_DDR3_A0	16,17,18,19
PS_DDR_BA2_502_M6	M6	PS_DDR3_BA2	16,17,18,19
PS_DDR_BA1_502_L6	L6	PS_DDR3_BA1	16,17,18,19
PS_DDR_BA0_502_L7	L7	PS_DDR3_BA0	16,17,18,19
PS_DDR_ODT_502_P5	P5	PS_DDR3_ODT	16,17,18,19
PS_DDR_CS_B_502_P6	P6	PS_DDR3_CS_B	16,17,18,19
PS_DDR_CKE_502_V3	V3	PS_DDR3_CKE	16,17,18,19
PS_DDR_WE_B_502_R4	R4	PS_DDR3_WE_B	16,17,18,19
PS_DDR_CAS_B_502_P3	P3	PS_DDR3_CAS_B	16,17,18,19
PS_DDR_RAS_B_502_R5	R5	PS_DDR3_RAS_B	16,17,18,19
PS_DDR_DQ16_502_M1	M1	PS_DDR3_DQ16	18
PS_DDR_DQ17_502_T3	T3	PS_DDR3_DQ21	18
PS_DDR_DQ18_502_N3	N3	PS_DDR3_DQ22	18
PS_DDR_DQ19_502_T1	T1	PS_DDR3_DQ19	18
PS_DDR_DM2_502_P1	P1	PS_DDR3_DM2	18
PS_DDR_QS_P2_502_N2	N2	PS_DDR3_QS2_P	18
PS_DDR_QS_N2_502_P2	P2	PS_DDR3_QS2_N	18
PS_DDR_DQ20_502_R3	R3	PS_DDR3_DQ18	18
PS_DDR_DQ21_502_T2	T2	PS_DDR3_DQ17	18
PS_DDR_DQ22_502_M2	M2	PS_DDR3_DQ20	18
PS_DDR_DQ23_502_R1	R1	PS_DDR3_DQ23	18
PS_DDR_DQ24_502_AA3	AA3	PS_DDR3_DQ27	19
PS_DDR_DQ25_502_U1	U1	PS_DDR3_DQ24	19
PS_DDR_DQ26_502_AA1	AA1	PS_DDR3_DQ29	19
PS_DDR_DQ27_502_U2	U2	PS_DDR3_DQ26	19
PS_DDR_DM3_502_AA2	AA2	PS_DDR3_DM3	19
PS_DDR_QS_P3_502_V2	V2	PS_DDR3_QS3_P	19
PS_DDR_QS_N3_502_W2	W2	PS_DDR3_QS3_N	19
PS_DDR_DQ28_502_W1	W1	PS_DDR3_DQ31	19
PS_DDR_DQ29_502_Y3	Y3	PS_DDR3_DQ30	19
PS_DDR_DQ30_502_W3	W3	PS_DDR3_DQ28	19
PS_DDR_DQ31_502_Y1	Y1	PS_DDR3_DQ25	19
PS_DDR_VREF0_502_H7	H7		
PS_DDR_VREF1_502_P7	P7		

VCC1V5_PS

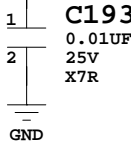
E2	VCC0_DDR_502_E2
F5	VCC0_DDR_502_F5
H1	VCC0_DDR_502_H1
J4	VCC0_DDR_502_J4
K7	VCC0_DDR_502_K7
M3	VCC0_DDR_502_M3
N6	VCC0_DDR_502_N6
R2	VCC0_DDR_502_R2
V1	VCC0_DDR_502_V1

U1

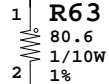
VTTVREF_PS



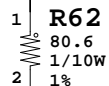
VTTVREF_PS



VCC1V5_PS



PS_VRN
PS_VRP



GND

Zynq Bank 502

TRIPLE CROWN

Title: Zynq Bank 502

Date: 10/11/2024:01:10 Ver: 1.0

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Sheet 9 of 35 Drawn By TG

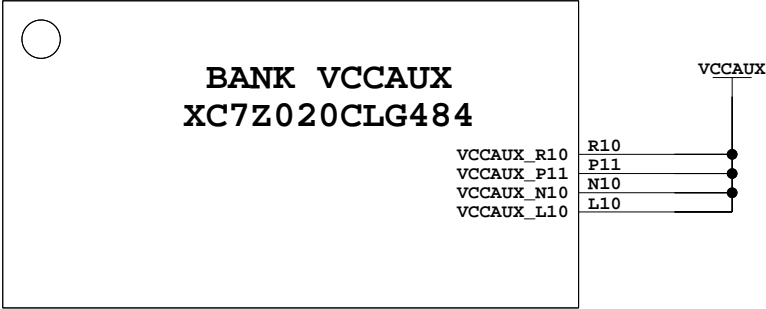
Increase width of VCCPLL route to as wide as possible (target is > 20 mils)

Reduce the length of VCCPLL route as much as possible

Place C538 inside the VIA field to provide as short as possible connection to VCCPLL (H10) and GND

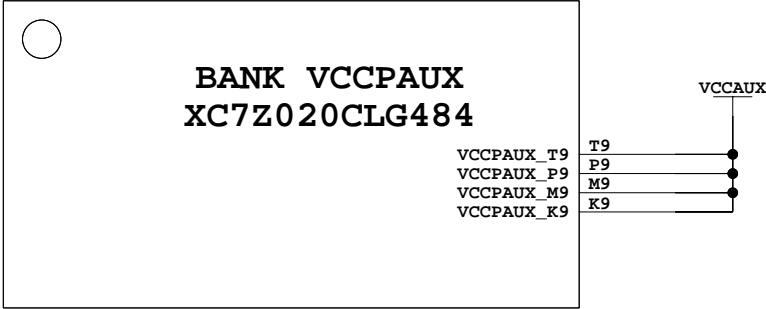
Place C539 inside the open space cross adjacent to H10 for the short possible connection to VCCPLL

XC7Z020



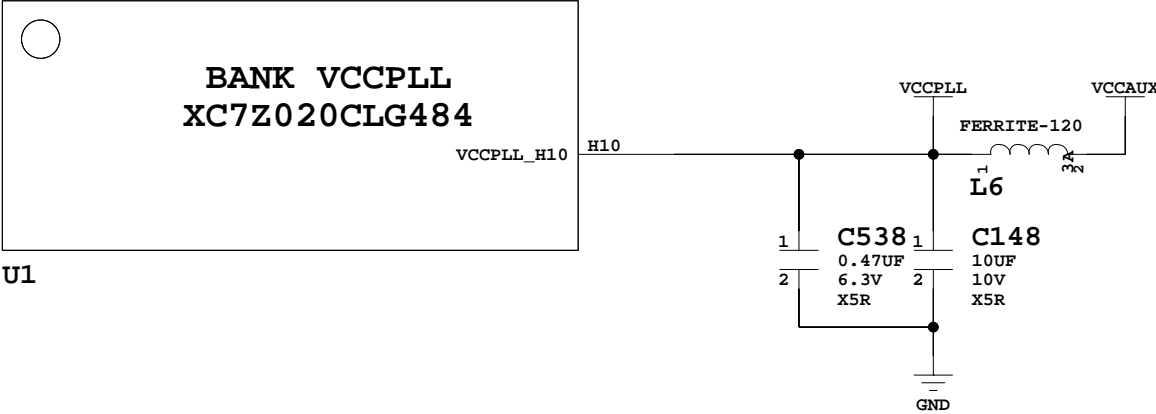
U1

XC7Z020



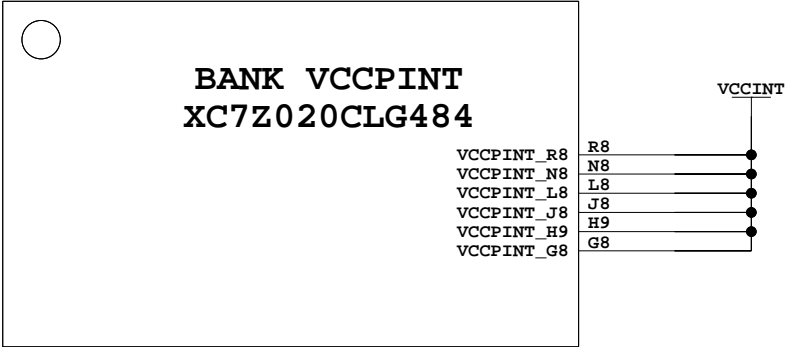
U1

XC7Z020



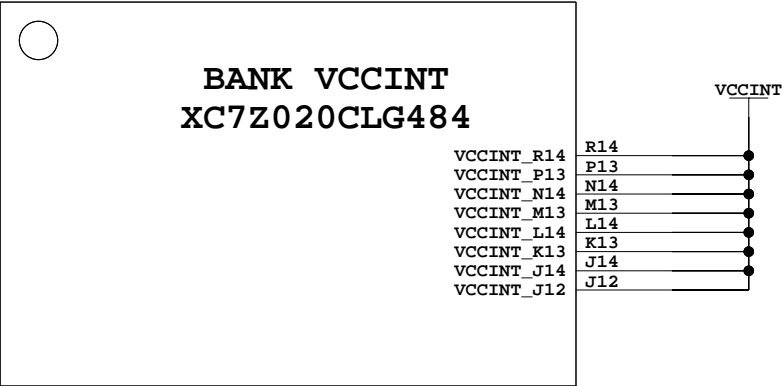
U1

XC7Z020



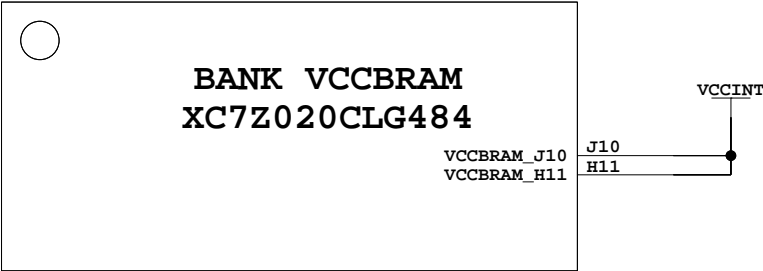
U1

XC7Z020



U1

XC7Z020



U1

Zynq Power Pins

TRIPLE CROWN

Title: Zynq Power Pins

Date: 10/11/2024:01:11 Ver: 1.0

Sheet Size: B Rev: 01

Sheet 10 of 35 Drawn By TG

XC7Z020

BANK GND
XC7Z020CLG484

- GND_Y22

GND_Y12

GND_Y2

GND_W19

GND_W9

GND_V16

GND_V6

GND_U13

GND_U3

GND_T20

GND_R17

GND_R13

GND_R11

GND_R9

GND_P14

GND_P12

GND_P10

GND_P8

GND_P4

GND_N21

GND_N13

GND_N9

GND_N1

GND_M18

GND_M14

GND_M10

GND_M8

GND_L15

GND_L13

GND_L9

GND_L5

GND_K22

GND_K14

GND_K10

GND_K8

GND_K2

GND_J19

GND_J13

GND_J11

GND_J9

GND_H16

GND_H14

GND_H12

GND_H8

GND_H6

GND_G3

GND_F20

GND_F10

GND_E17

GND_E7

GND_D14

GND_D4

GND_C21

GND_C11

GND_C1

GND_B18

GND_B8

GND_AB18

GND_AB8

GND_AA15

GND_AA5

GND_A15

GND_A5
- Y22

Y12

Y2

W19

W9

V16

V6

U13

U3

T20

R17

R13

R11

R9

P14

P12

P10

P8

P4

N21

N13

N9

N1

M18

M14

M10

M8

L15

L13

L9

L5

K22

K14

K10

K8

K2

J19

J13

J11

J9

H16

H14

H12

H8

H6

G3

F20

F10

E17

E7

D14

D4

C21

C11

C1

B18

B8

AB18

AB8

AA15

AA5

A15

A5

GND

U1

Zynq GND

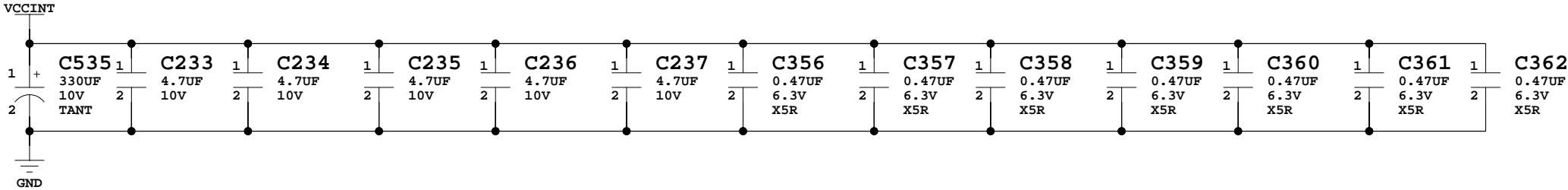
TRIPLE CROWN

Title: Zynq GND

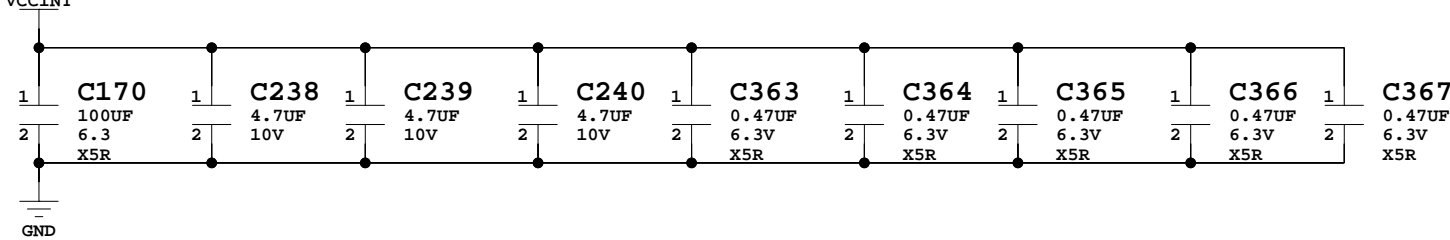
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size:	B	Rev:	
Sheet	11 of 35	Drawn By	TG

BYPASS CAPACITORS

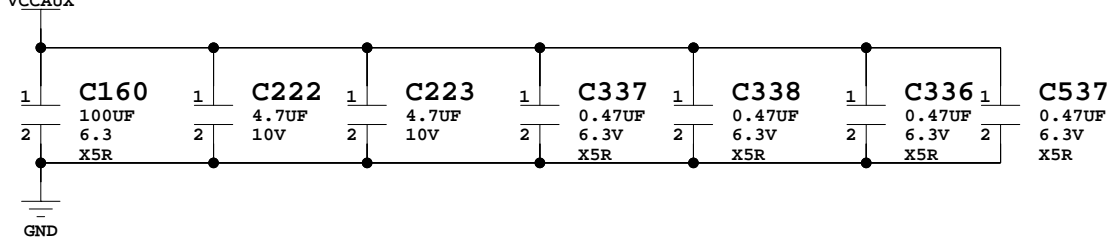
VCCINT_PL 330uF (1), 4.7uF (5), 0.47uF (7)



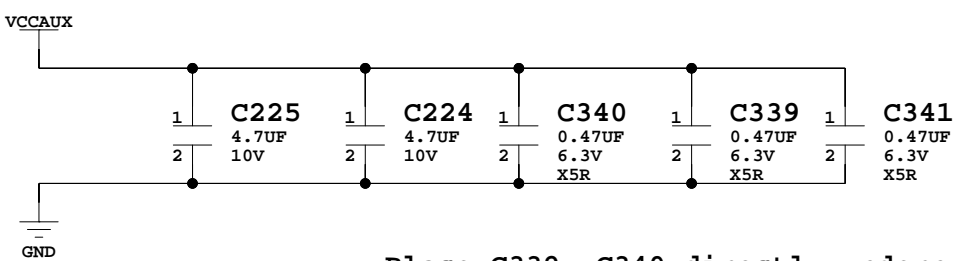
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



VCCAUX 100uF (1), 4.7uF (2), 0.47uF (4)

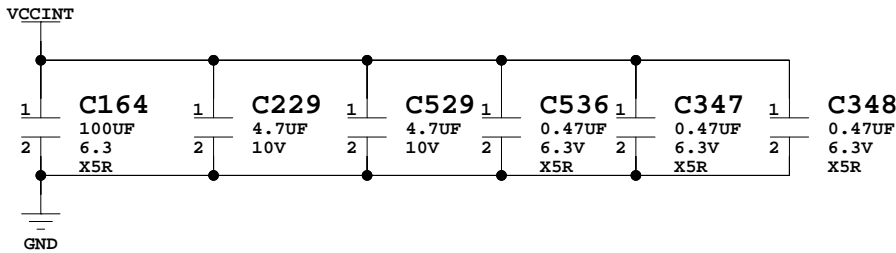


VCCPAUX 100uF (0), 4.7uF (2), 0.47uF (3)

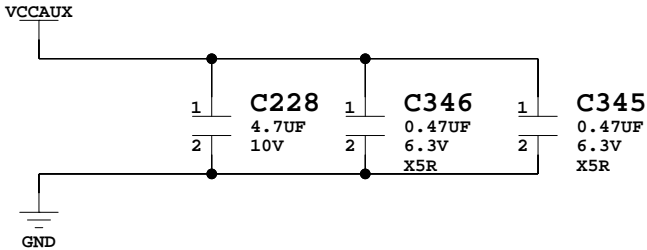


Place C339, C340 directly underneath the FPGA as short as possible connection to VCCPAUX and GND

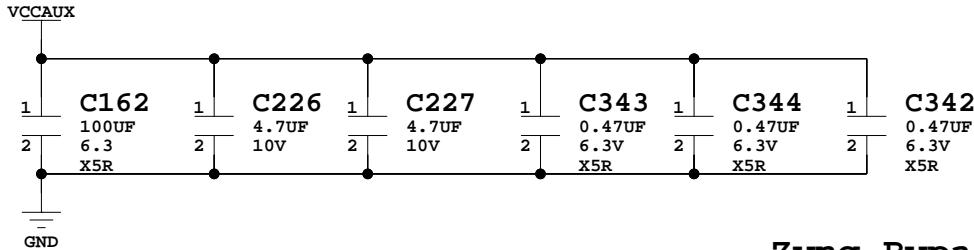
VCCBRAM 100uF (1), 4.7uF (2), 0.47uF (3)



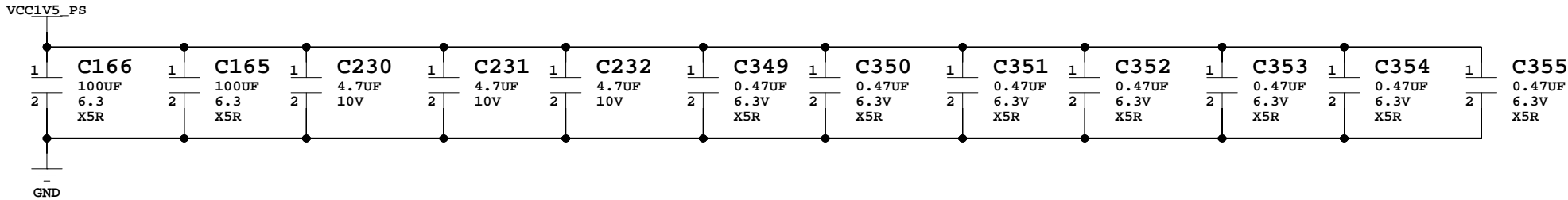
VCCP0_PS 100uF (0), 4.7uF (1), 0.47uF (2)



VCCP1_PS 100uF (1), 4.7uF (2), 0.47uF (3)



VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)



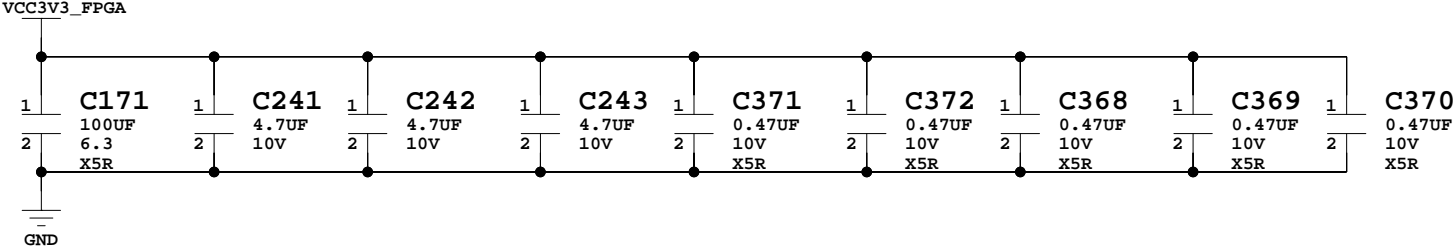
Zynq Bypass Capacitors

TRIPLE CROWN

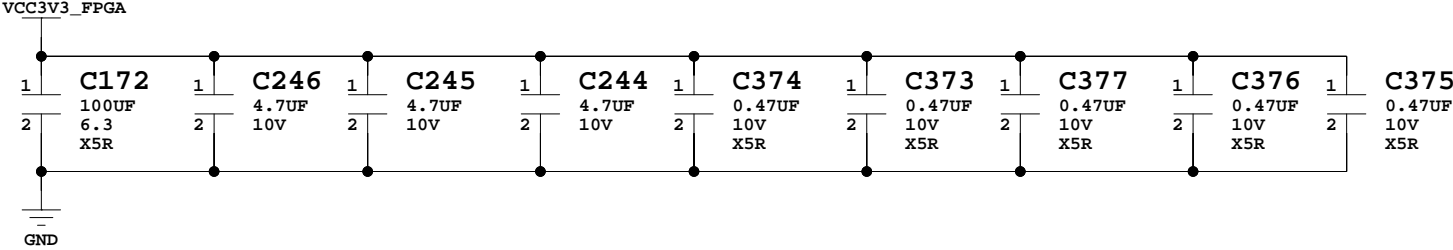
Title: Zynq Bypass Capacitors

Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	12 of 35	Drawn By	TG

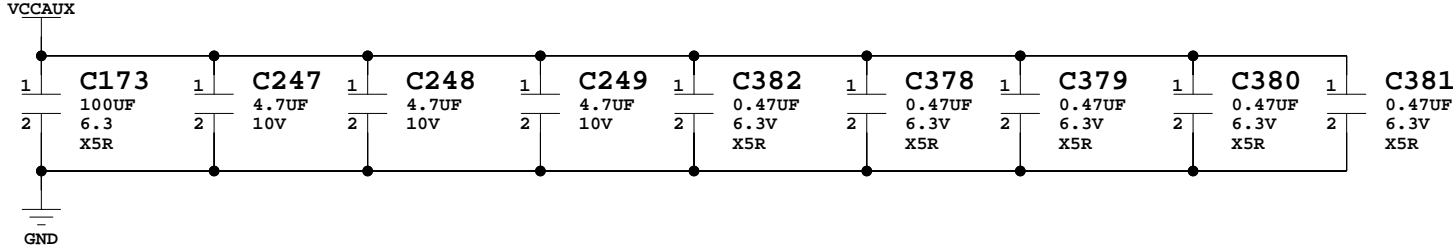
Bank 13 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



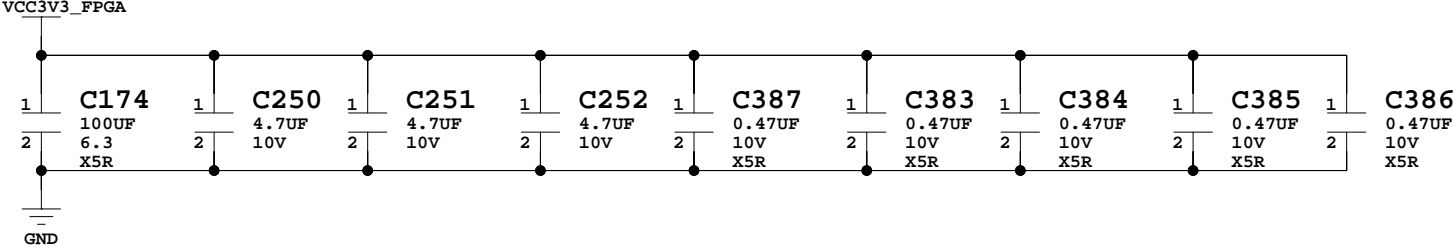
Bank 33 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 34 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



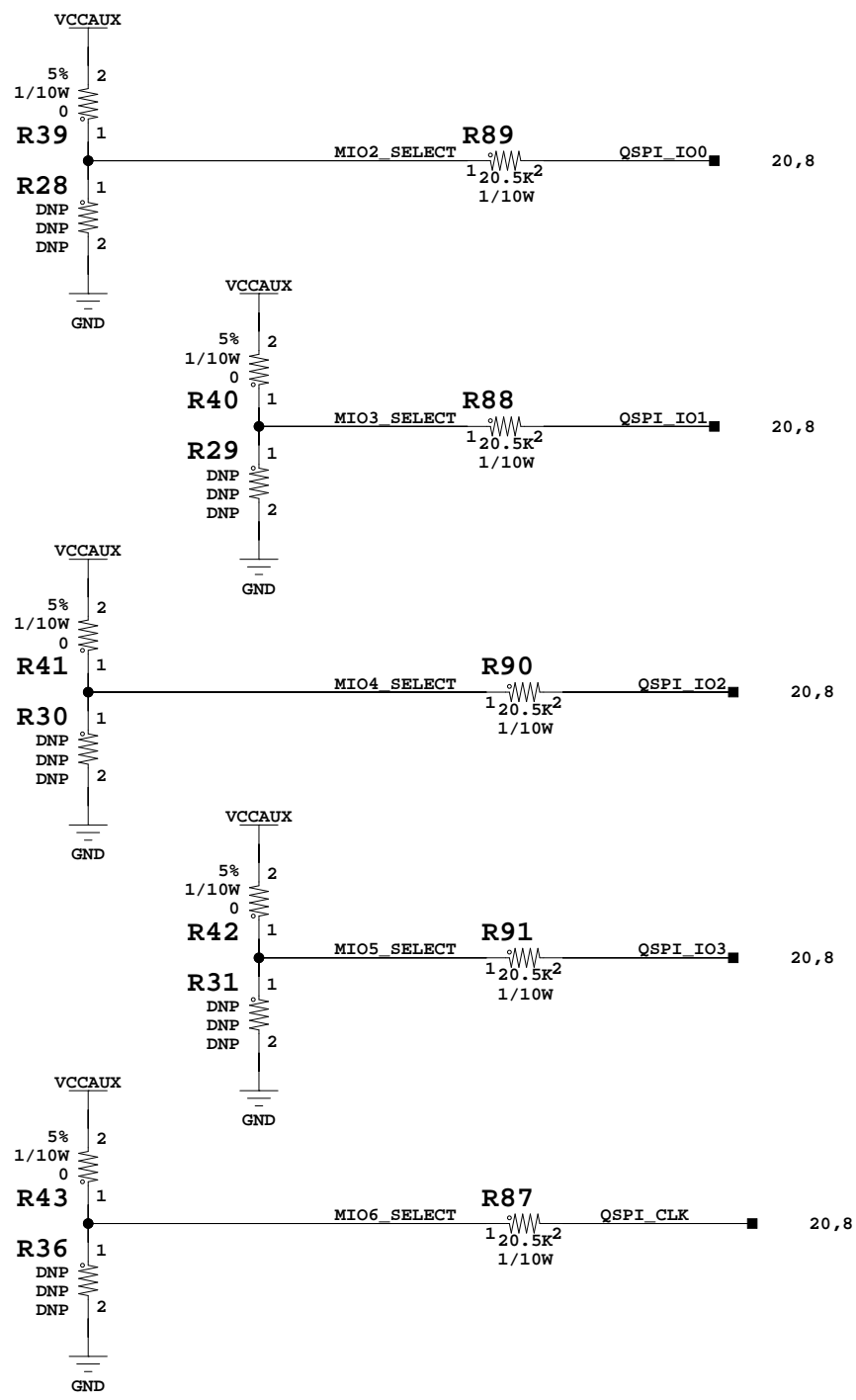
Bank 35 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Zynq Bypass Capacitors

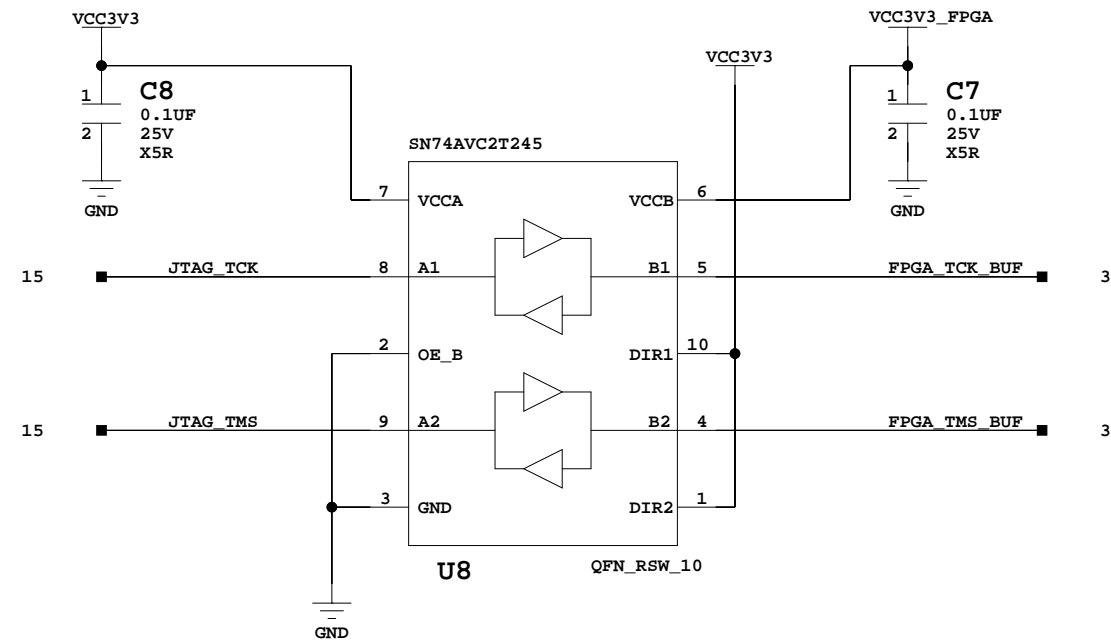
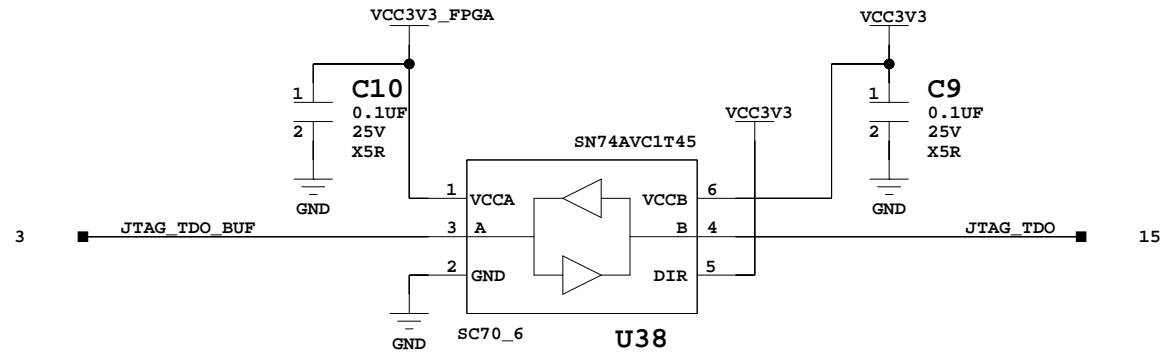
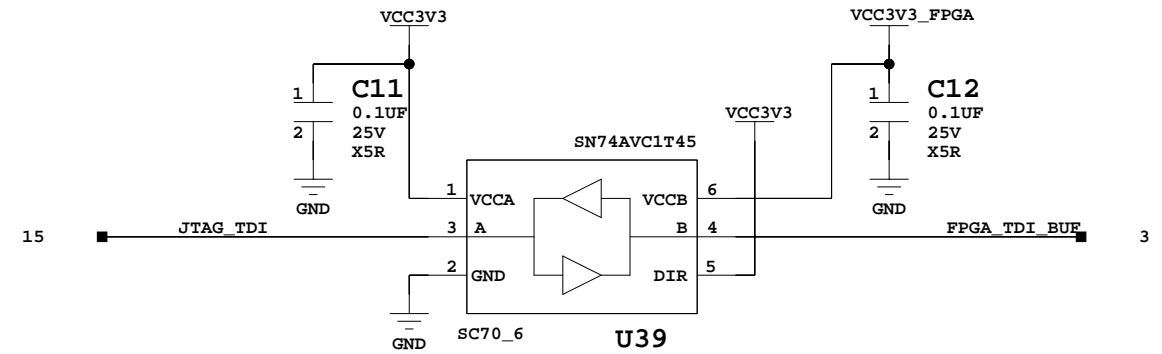
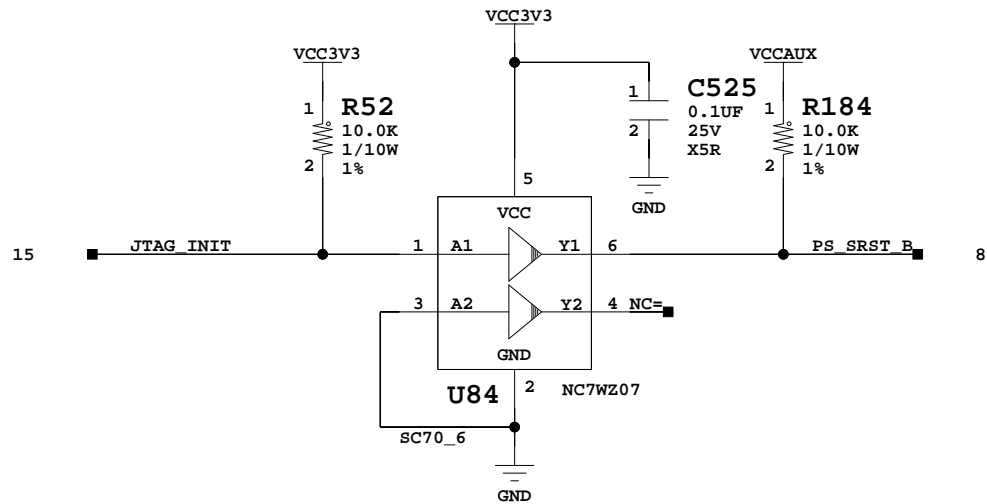
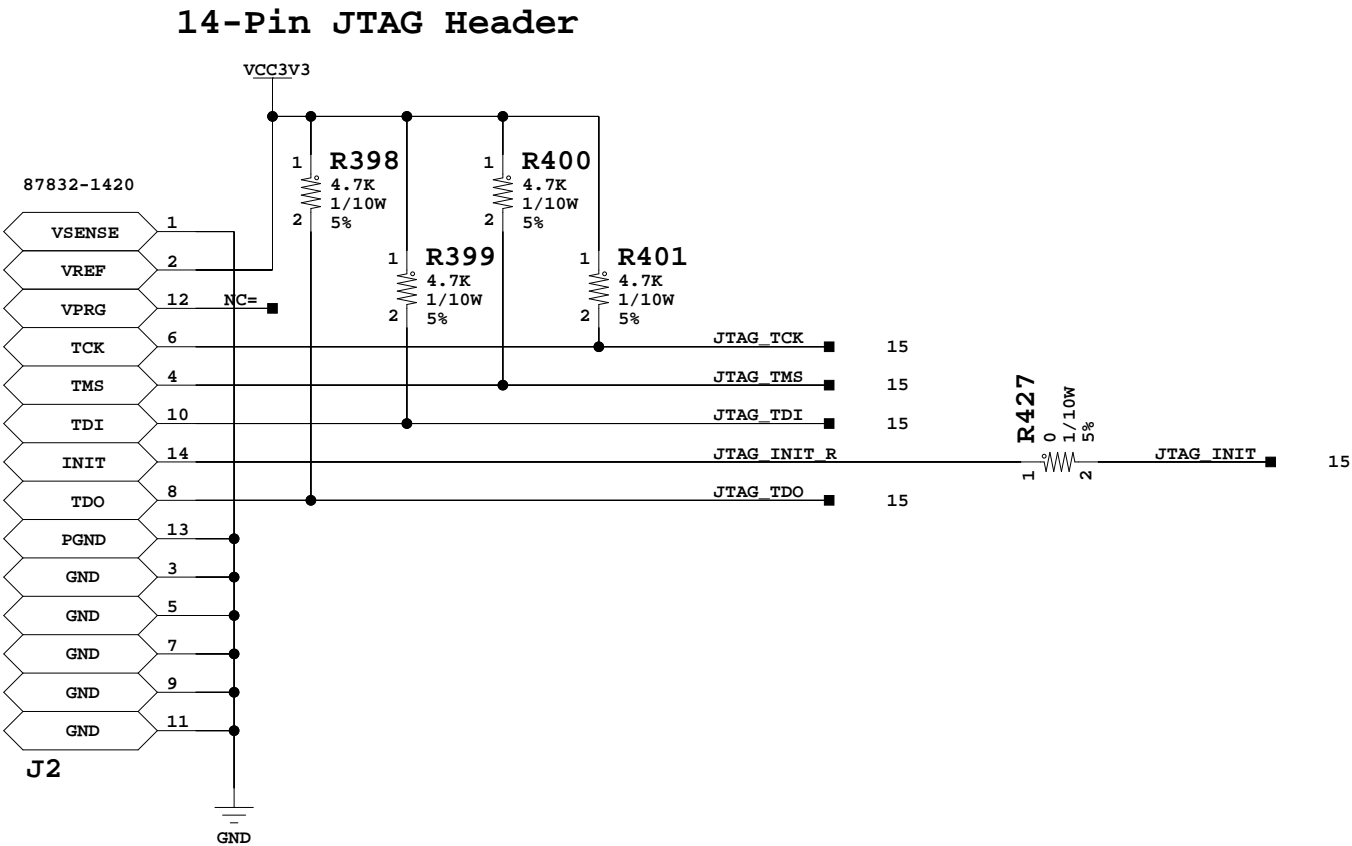
TRIPLE CROWN	
Title: Zynq Bypass Capacitors	
Date: 10/11/2024:01:10	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 13 of 35	Drawn By TG

MIO[6:2] SELECTION HEADERS



Zynq Config Pins

TRIPLE CROWN	
Title: Zynq Config Pins	
Date: 10/11/2024:01:10	Ver: 1.0
Sheet Size: B	Rev: 02
Sheet 14 of 35	Drawn By TG



JTAG Buffers, JTAG Hdr

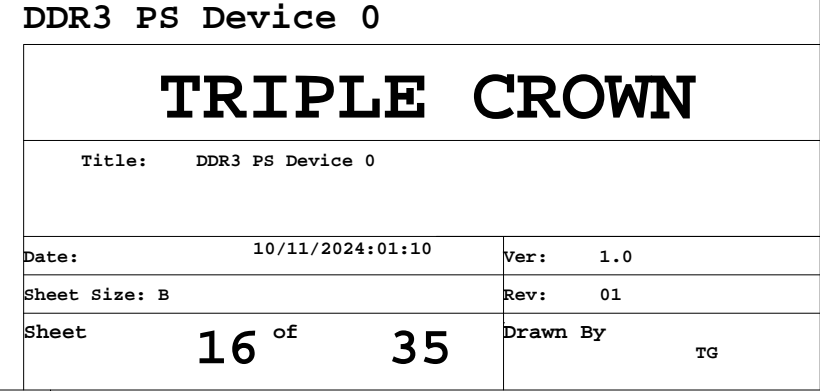
TRIPLE CROWN

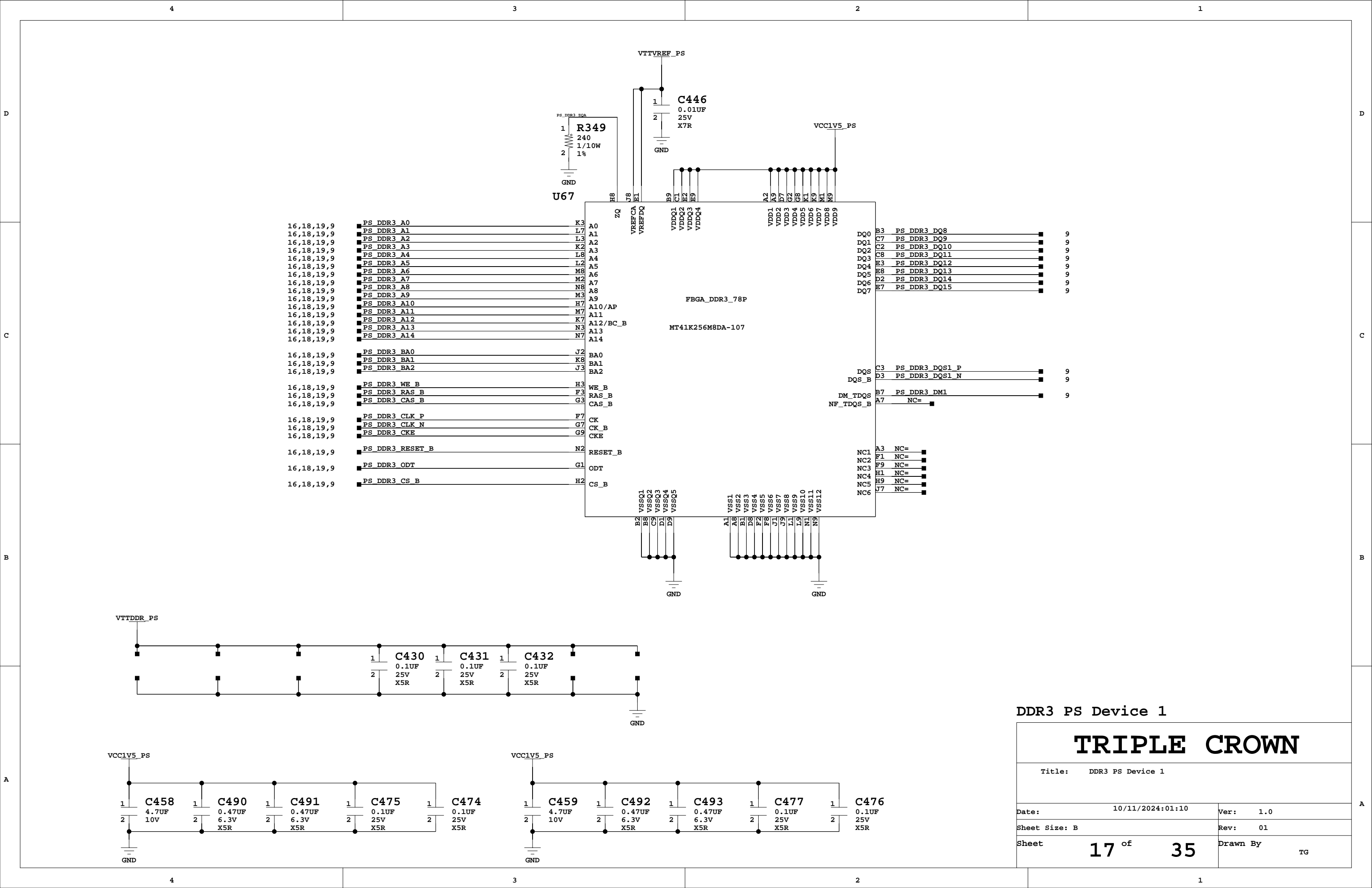
Title: JTAG Buffers, JTAG Hdr

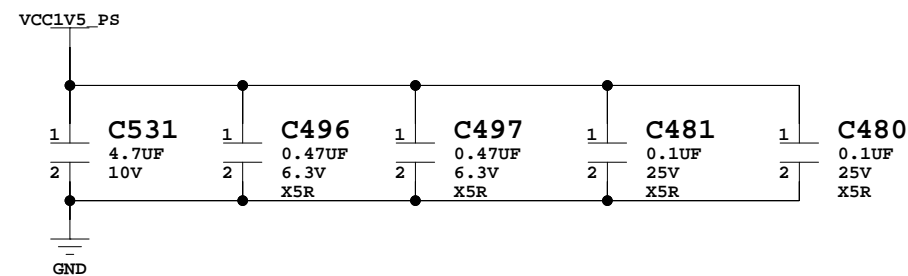
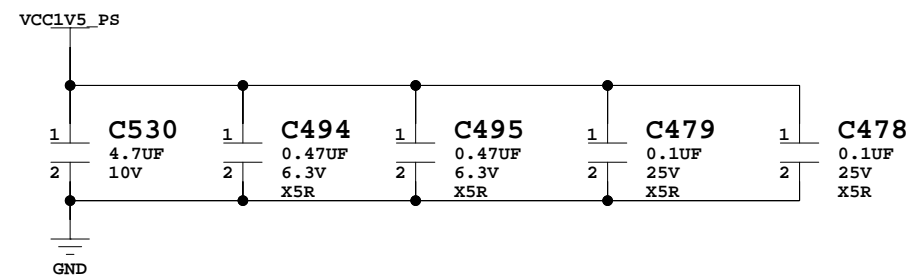
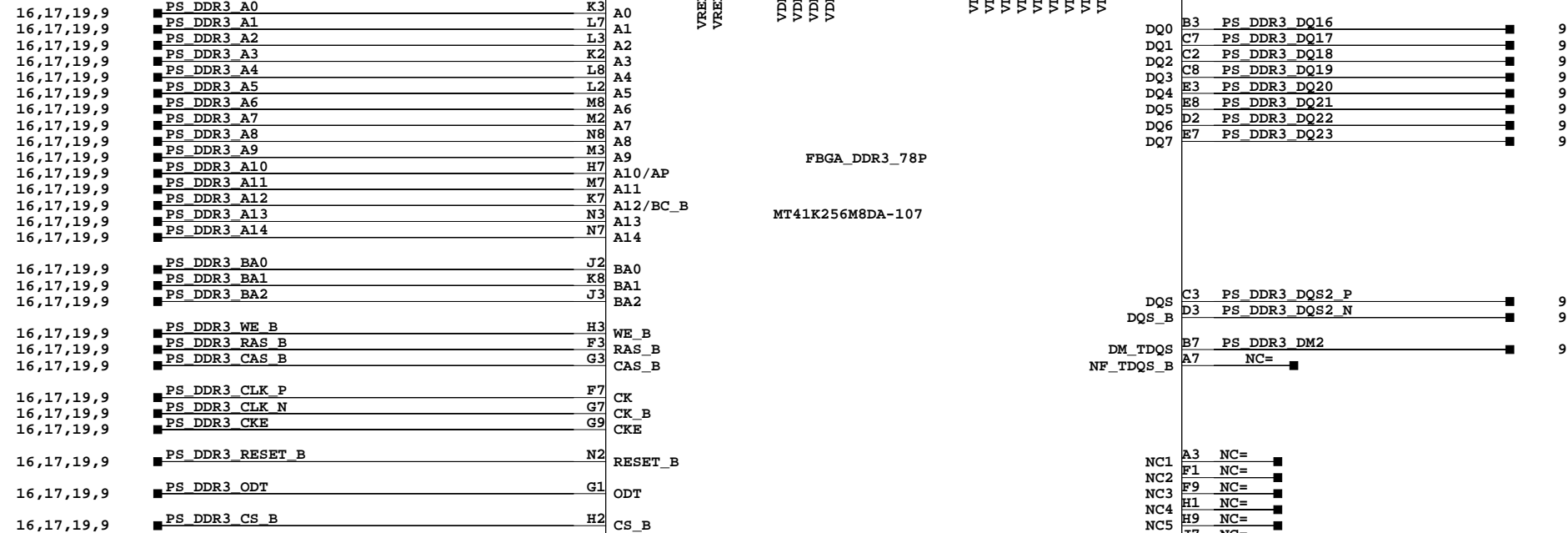
Date: 10/11/2024:01:10 Ver: 1.0

Sheet Size: B Rev: 01

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DDR3 PS Device 2

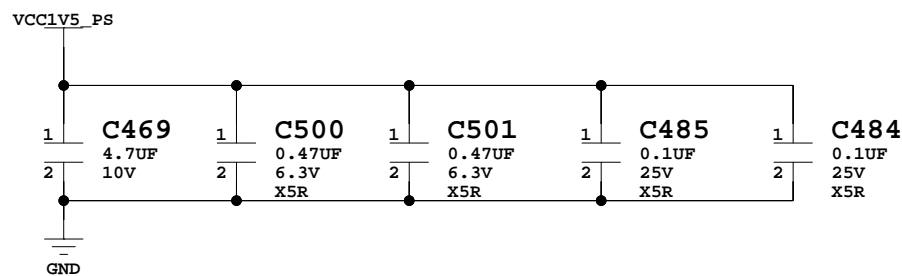
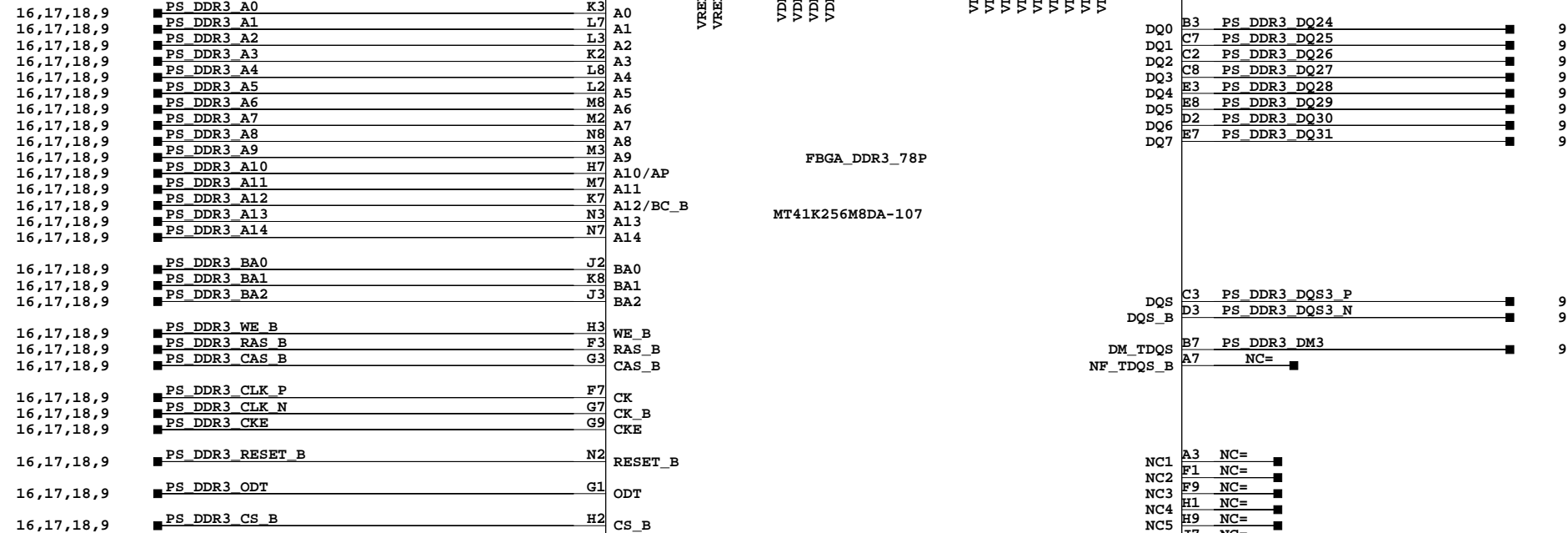
TRIPLE CROWN

Title: DDR3 PS Device 2

Date:	10/11/2024:01:10	Ver:	1.0
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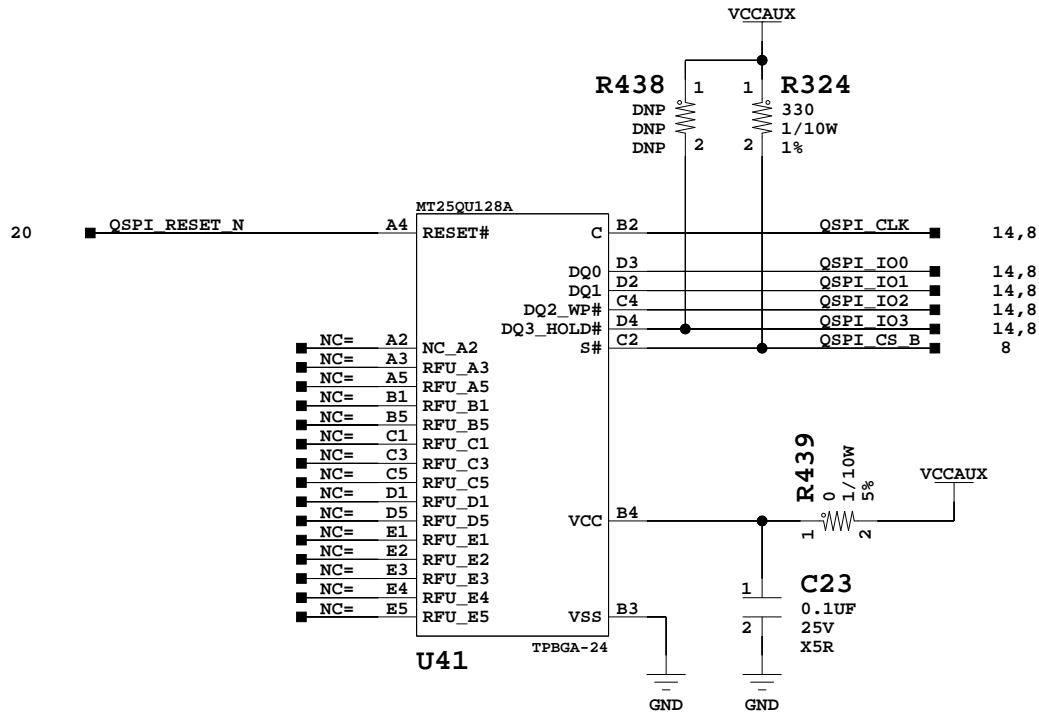
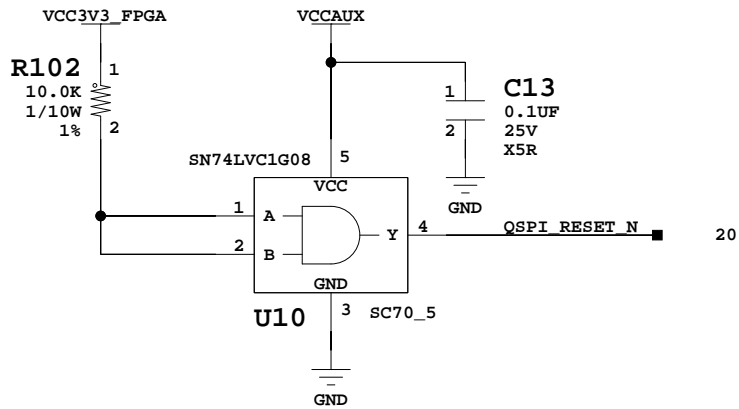
Sheet Size: B	Rev: 01
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Sheet	18 of 35	Drawn By	TG
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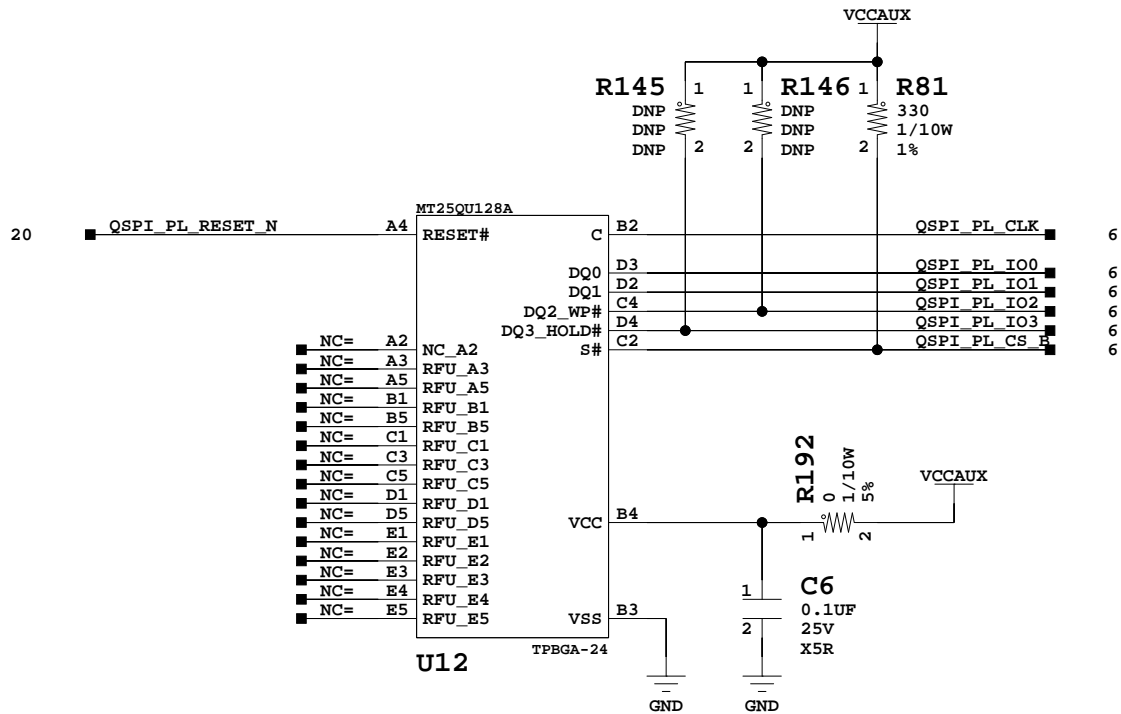
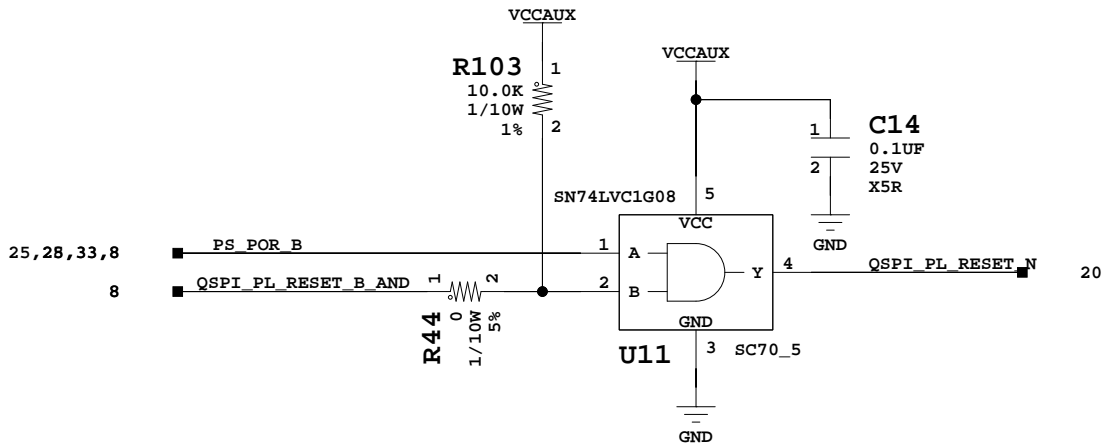


TRIPLE CROWN

Sheet	19 of 35	Drawn By	TG
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PS Quad SPI



PL Quad SPI

Quad SPI

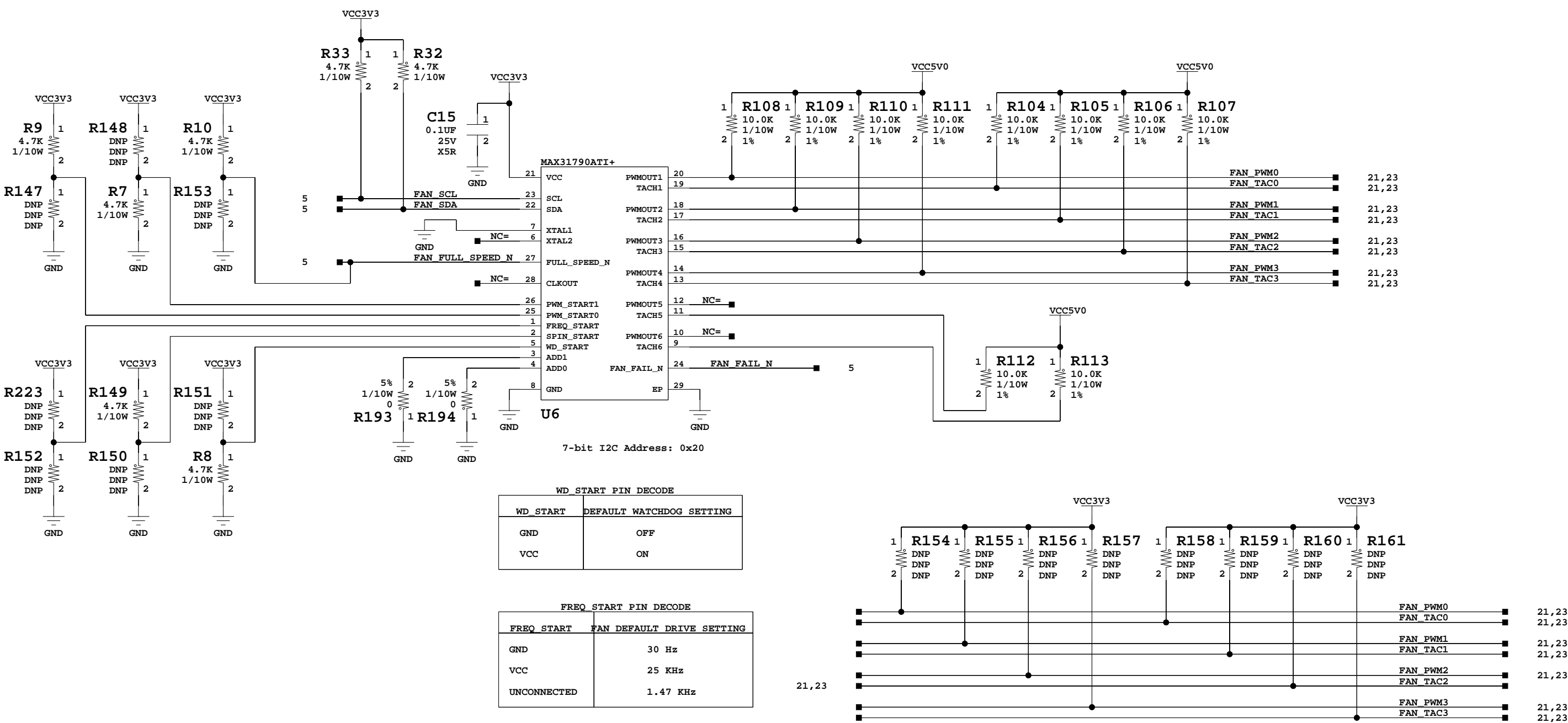
TRIPLE CROWN

Title: Quad SPI

Date: 10/11/2024:01:10 Ver: 1.0

Sheet Size: B Rev: 01

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WD_START PIN DECODE	
WD_START	DEFAULT WATCHDOG SETTING
GND	OFF
VCC	ON

FREQ_START PIN DECODE	
FREQ_START	FAN DEFAULT DRIVE SETTING
GND	30 Hz
VCC	25 KHz
UNCONNECTED	1.47 KHz

PWM_START PINS DECODE		
PWM_START0	PWM_START1	PWM DUTY CYCLE (%)
GND	GND	0
GND	UNCONNECTED	30
GND	VCC	40
UNCONNECTED	GND	50
UNCONNECTED	VCC	60
VCC	GND	75
VCC	VCC	100

Fan Control and Sense

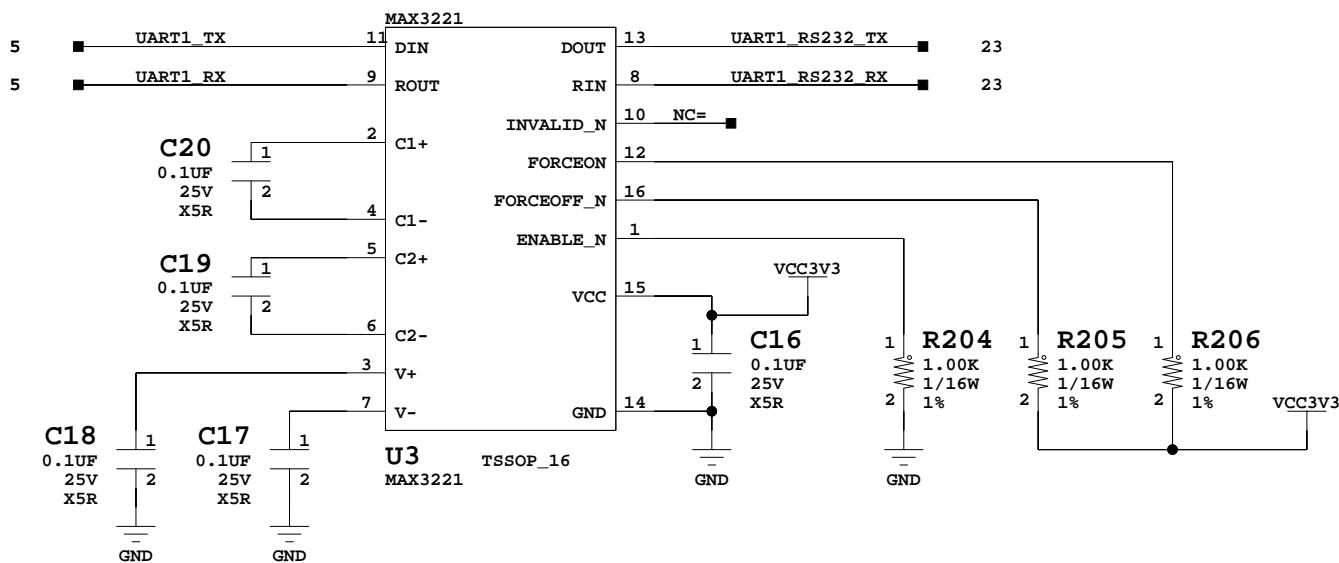
TRIPLE CROWN

Title: Fan Control and Sense

Date: 10/11/2024:01:10 Ver: 1.0

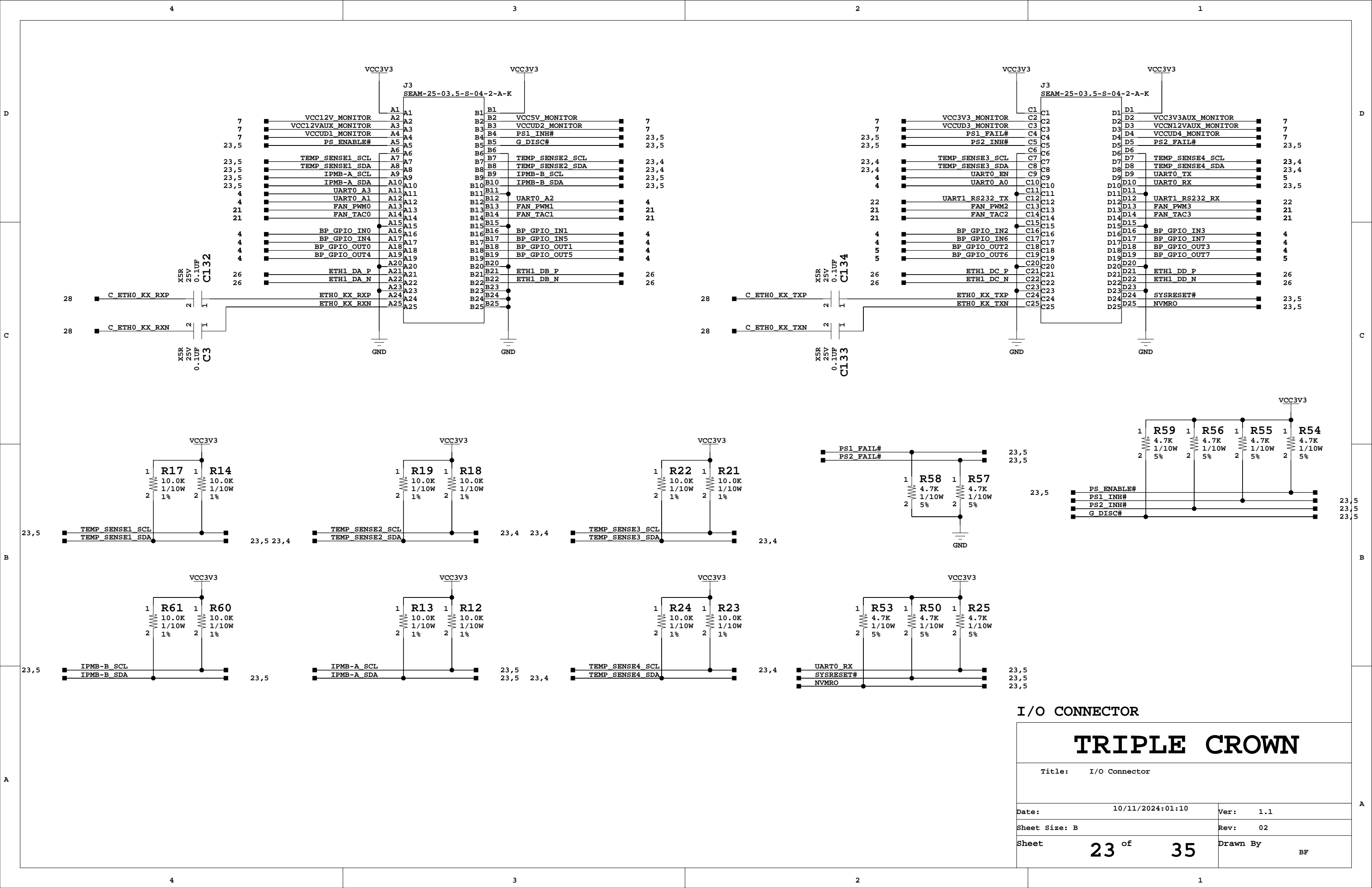
Sheet Size: B Rev: 01

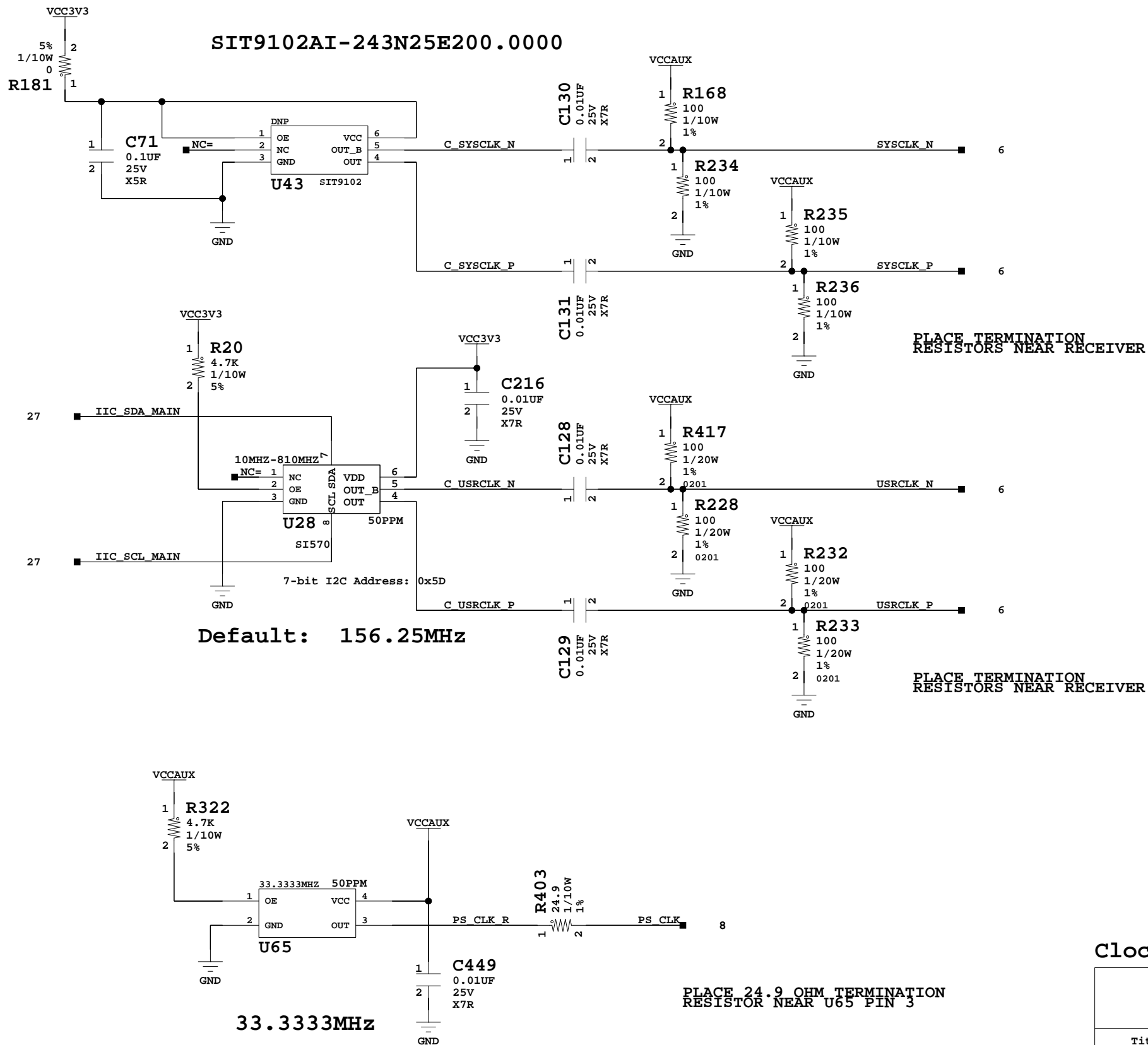
Sheet 21 of 35 Drawn By TG



RS-232 UART

TRIPLE CROWN			
Title: RS-232 UART			
Date:	10/11/2024:01:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	22 of 35	Drawn By	BF





Clocks

TRIPLE CROWN

Title: Clocks

Date: 10/11/2024:01:10 Ver: 1.0

Sheet Size: B Rev: 01

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D

C

B

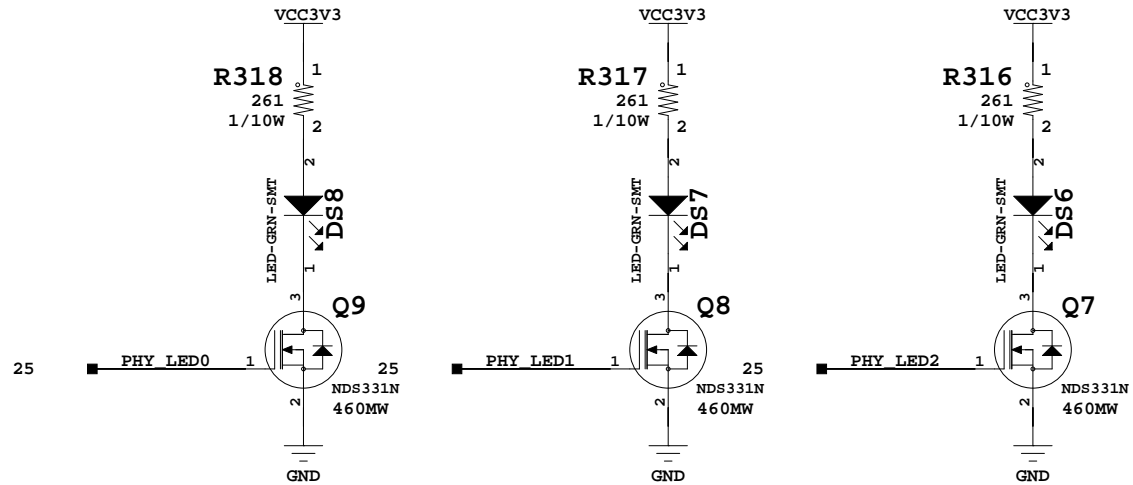
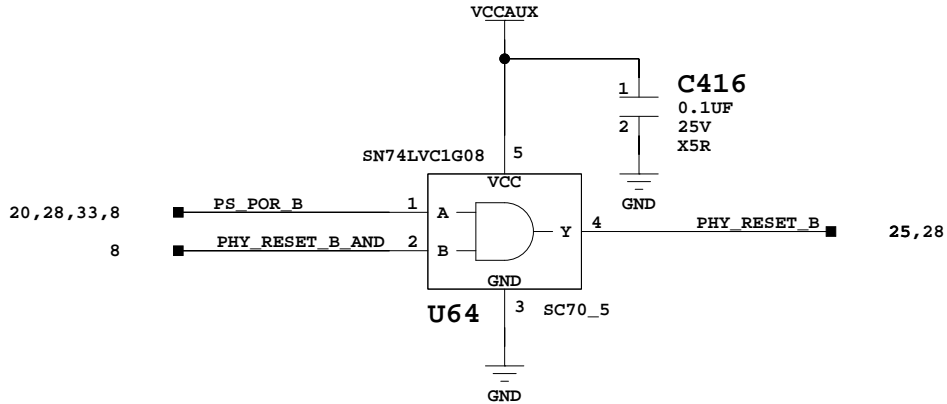
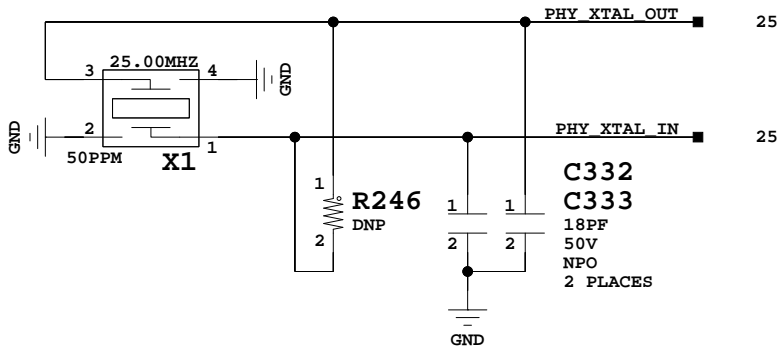
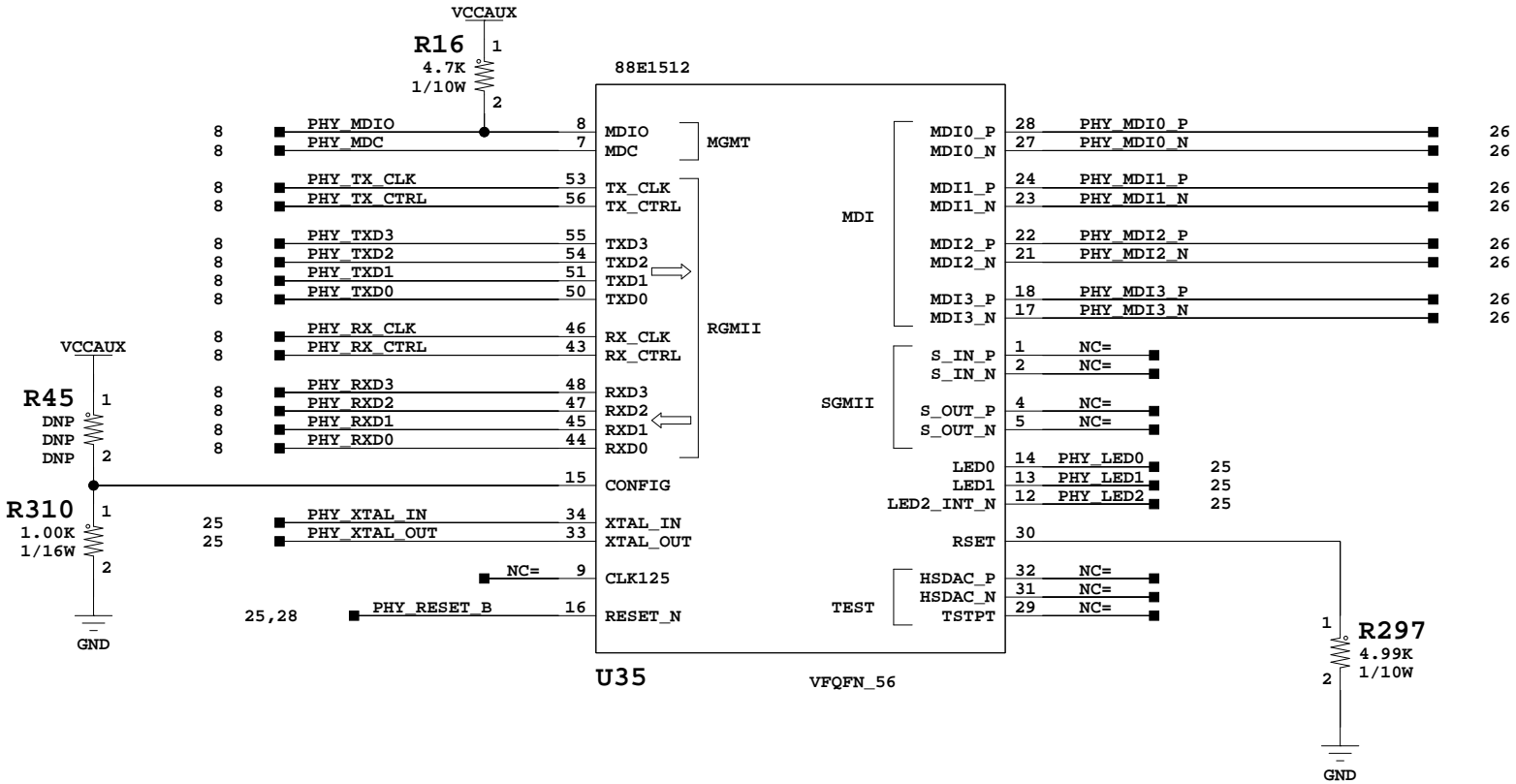
A

D

C

B

A



GEM / MDIO

TRIPLE CROWN

Title: GEM / MDIO

Date: 10/11/2024:01:10 Ver: 1.0

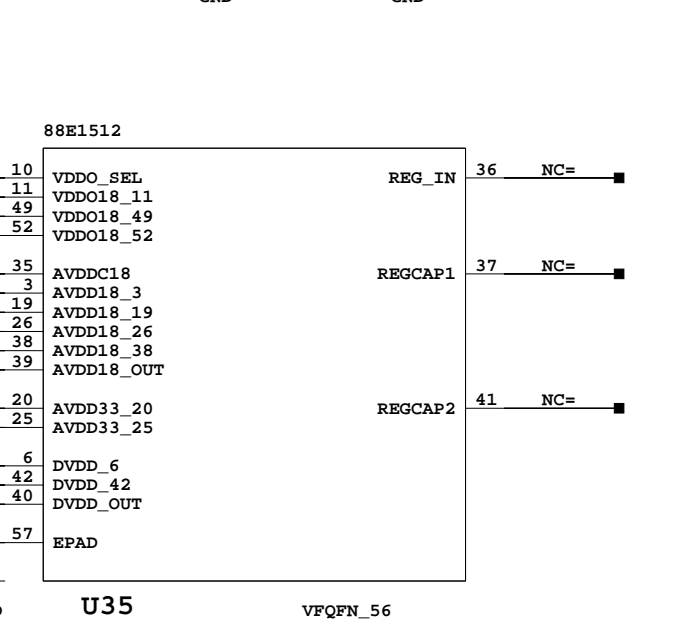
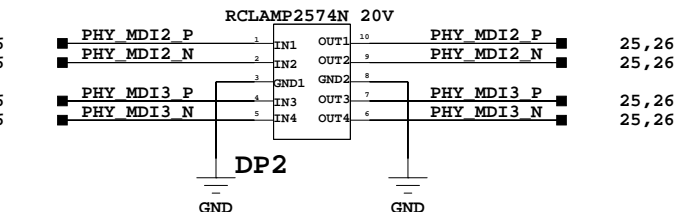
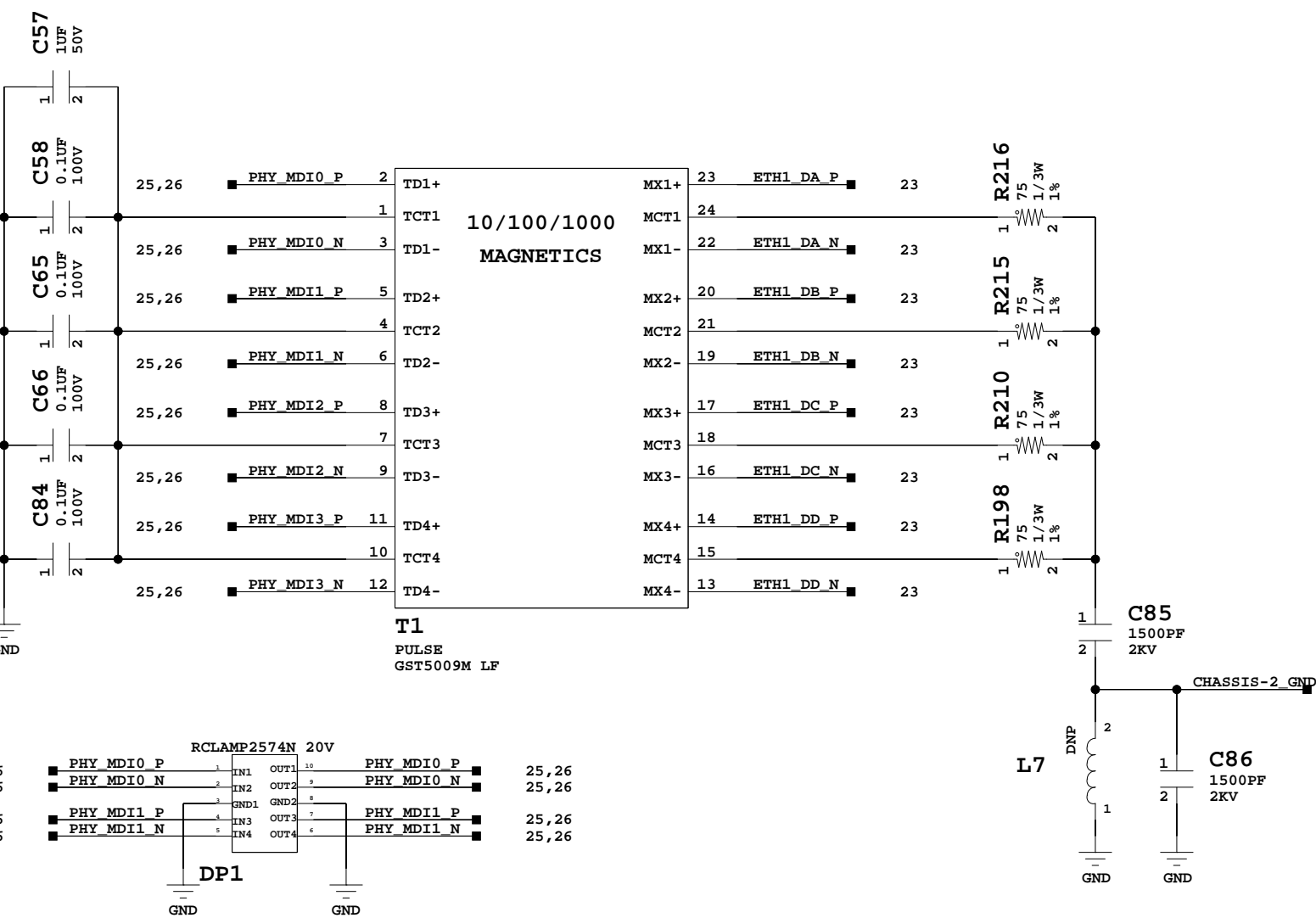
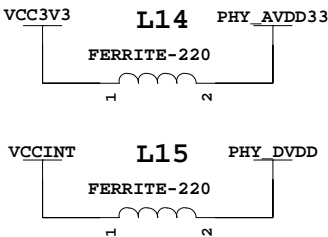
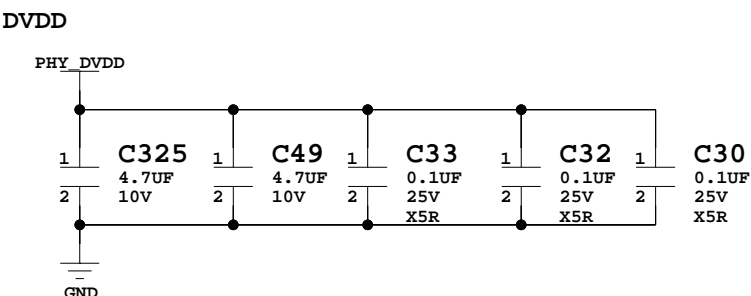
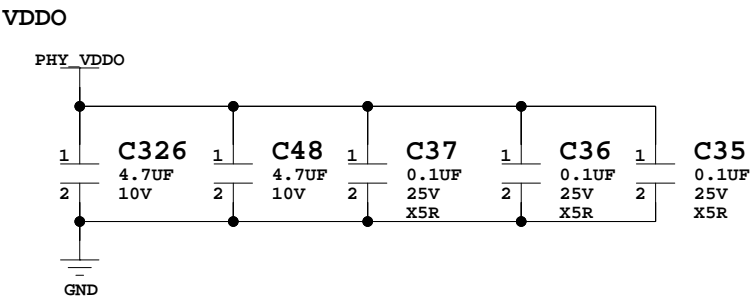
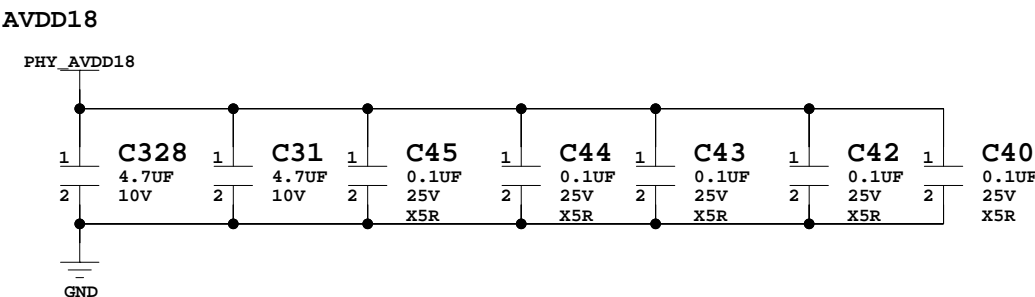
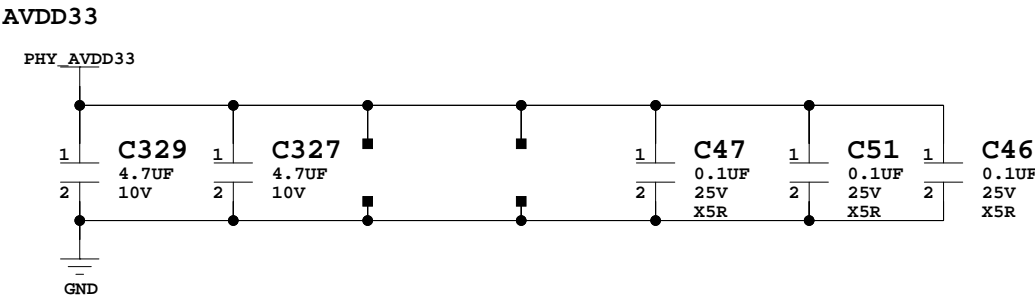
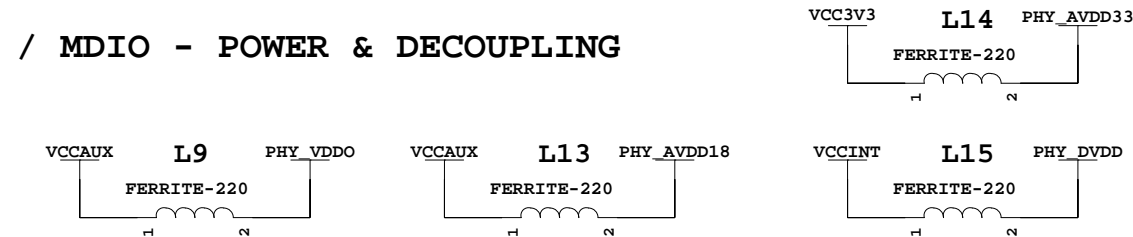
Sheet Size: B Rev: 01

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SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.

GEM / MDIO - POWER & DECOUPLING



Chassis GND Accessible on PCB?

GEM / MDIO

TRIPLE CROWN

Title: GEM / MDIO

Date: 10/11/2024:01:10

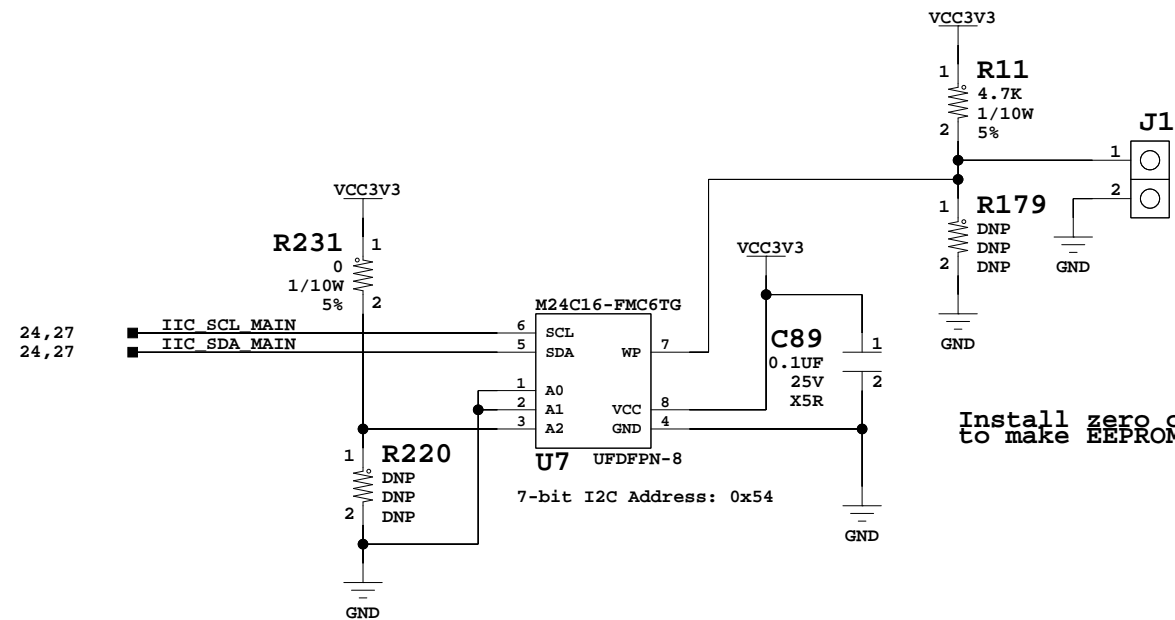
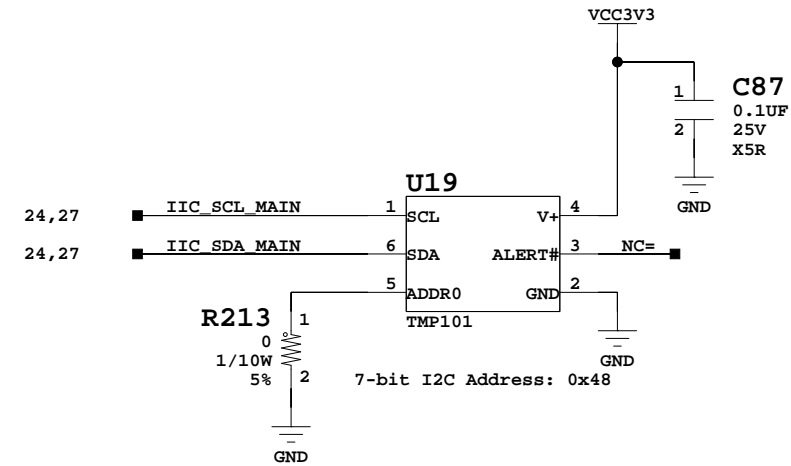
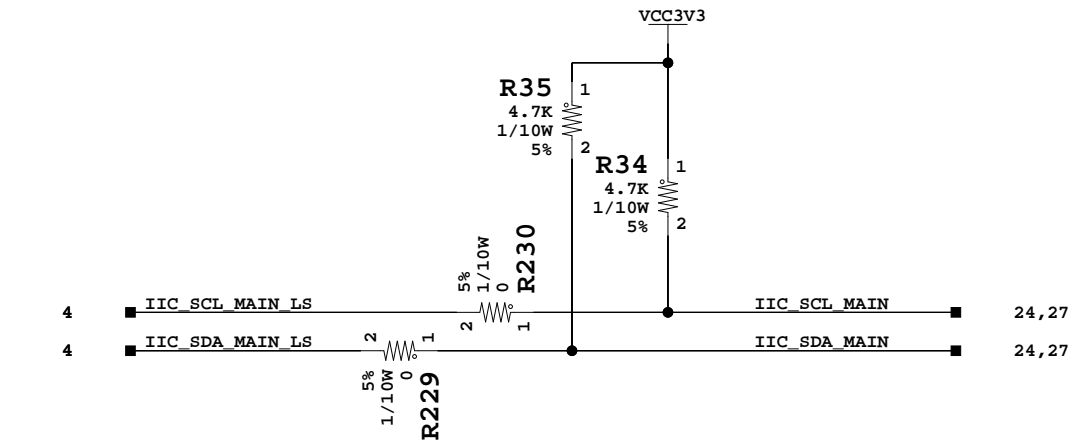
Ver: 1.0

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Rev: 01

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Drawn By TG



EEPROM, TEMPERATURE SENSOR

TRIPLE CROWN

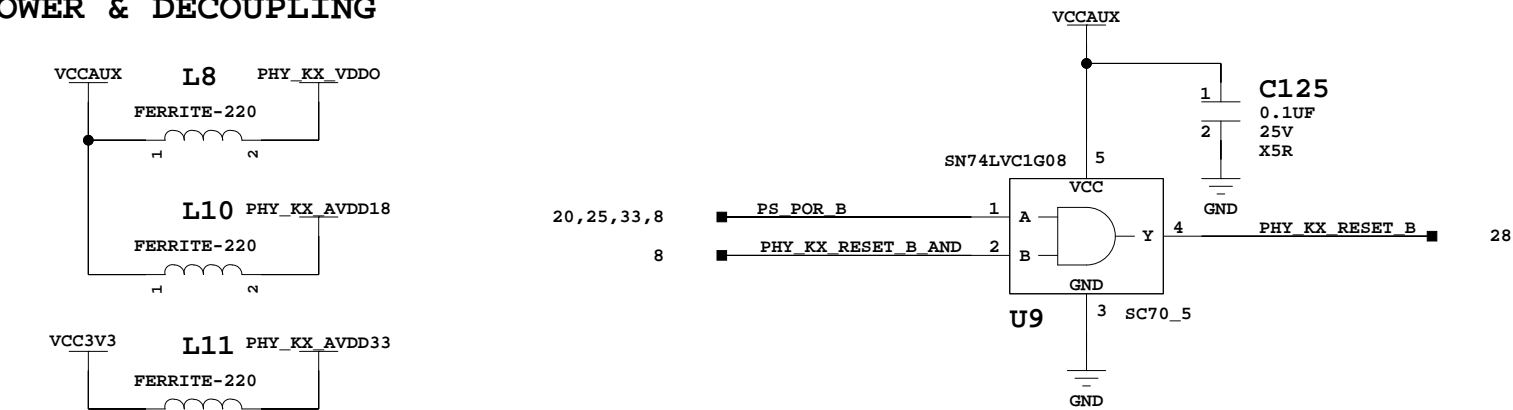
Title: EEPROM, TEMPERATURE SENSOR

Date: 10/11/2024:01:10 Ver: 1.1

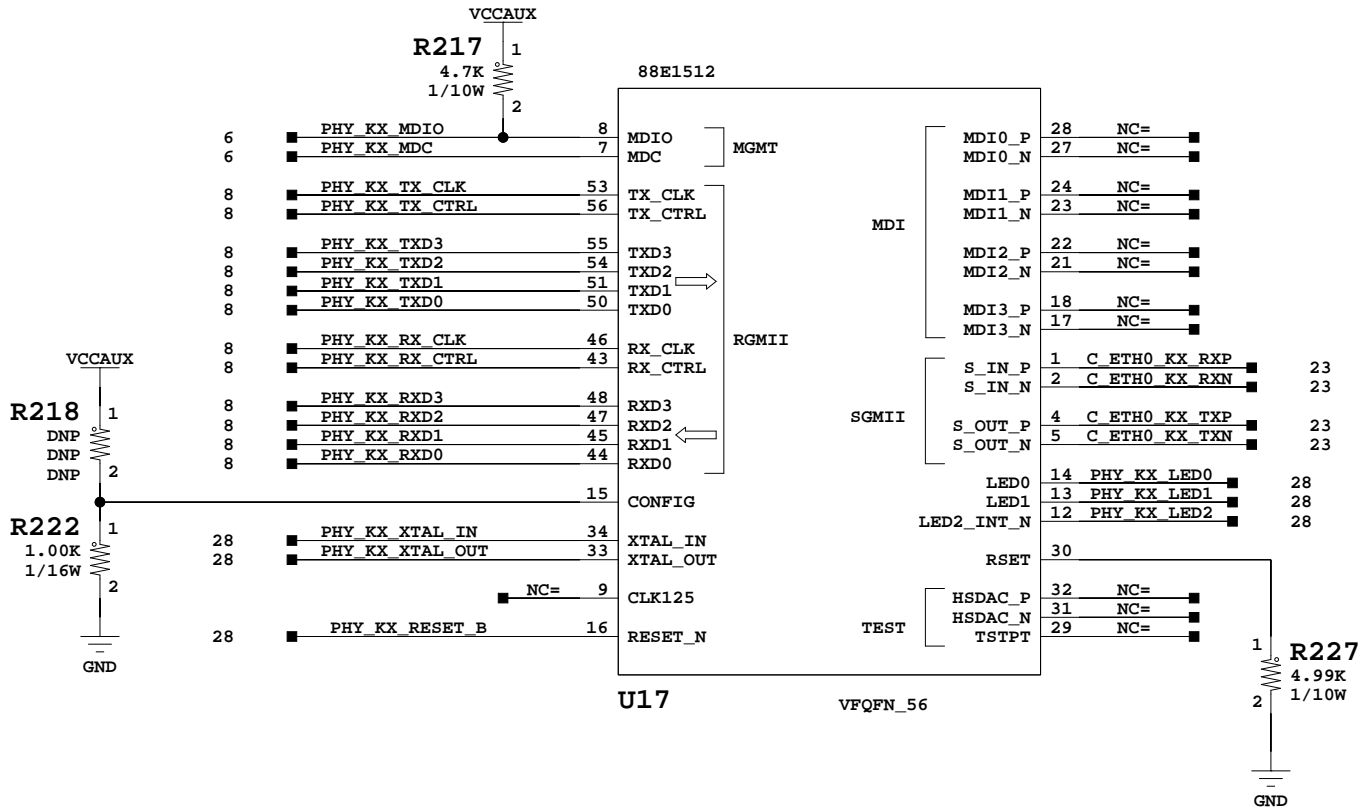
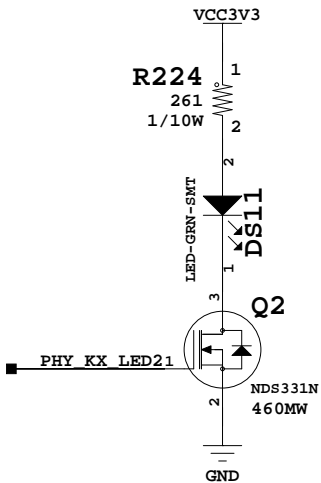
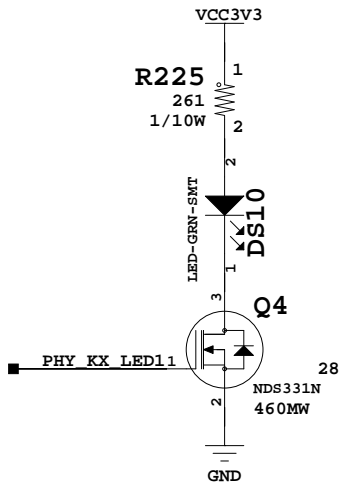
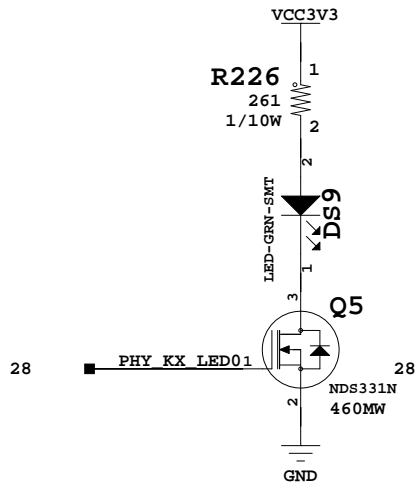
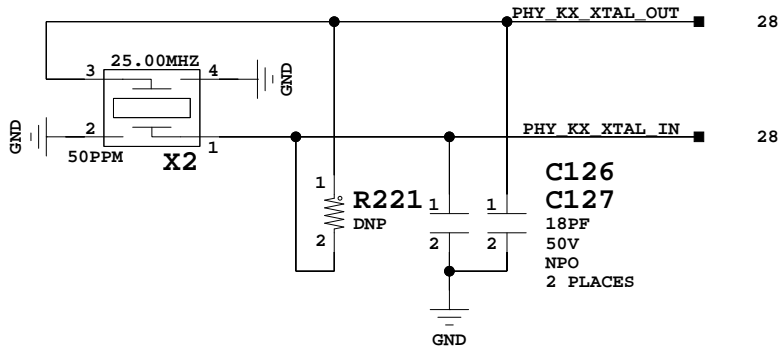
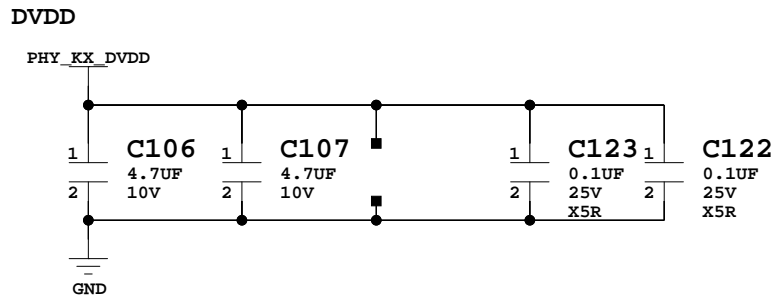
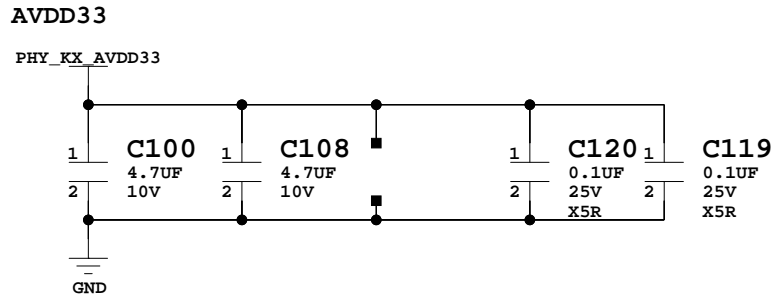
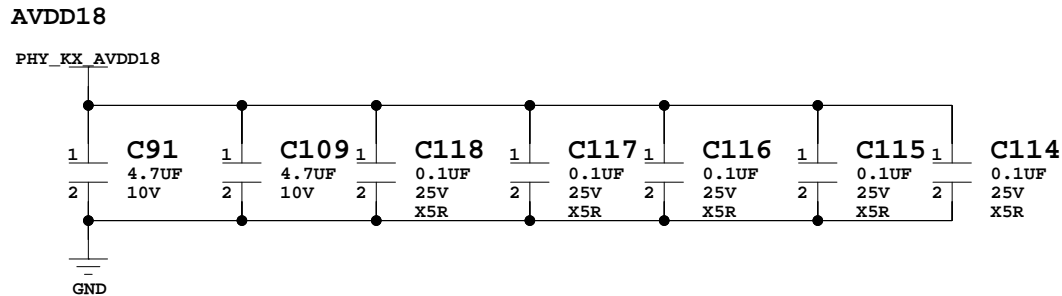
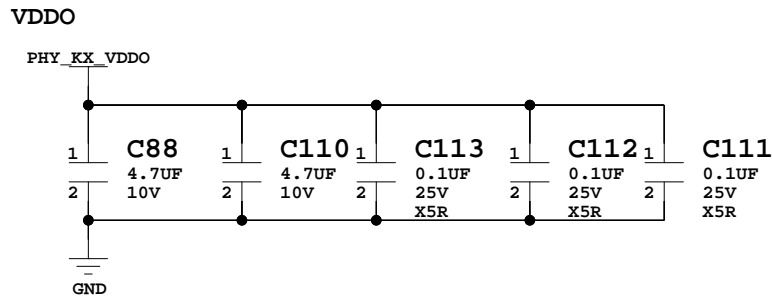
Sheet Size: B Rev: 02

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POWER & DECOUPLING



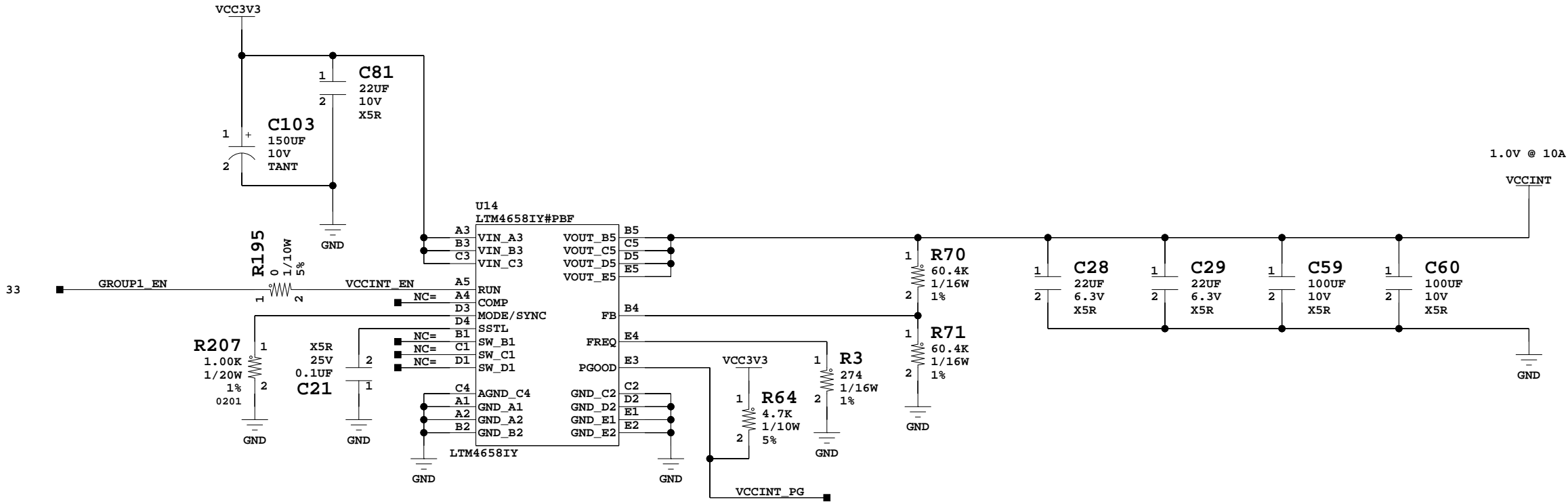
ADD SEPARATE FPGA RESET CONTROL?



1000BASE-KX Ethernet

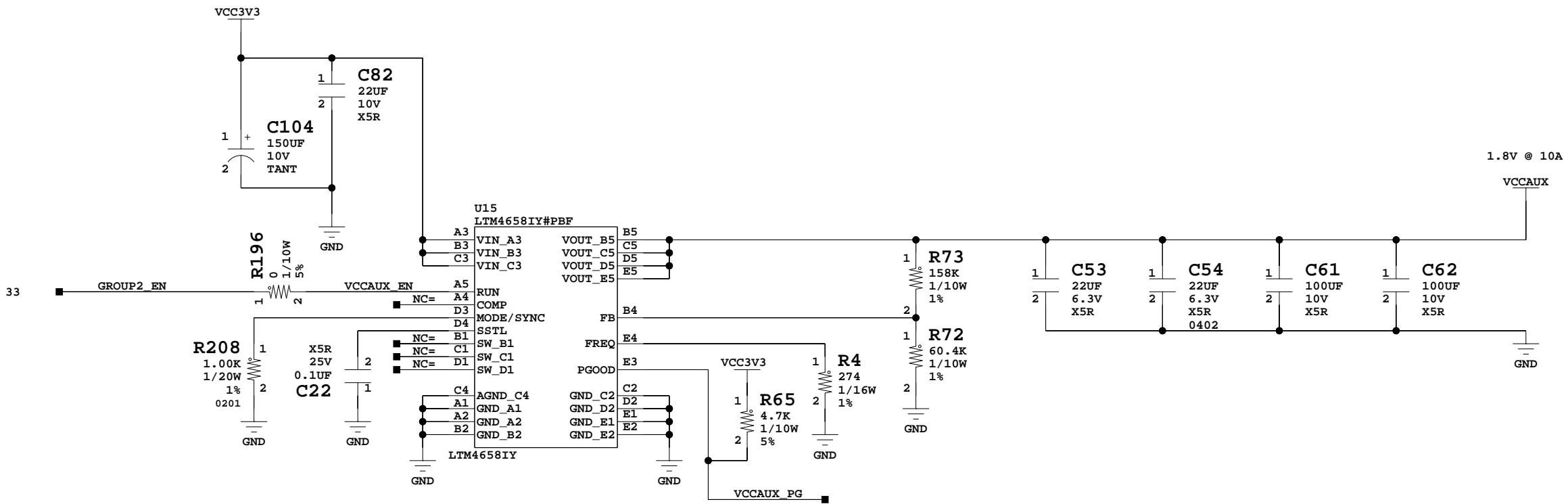
TRIPLE CROWN

Title: 1000BASE-KX Ethernet		
Date: 10/11/2024:01:10	Ver: 1.0	
Sheet Size: B	Rev: 01	
Sheet 28 of 35	Drawn By TG	



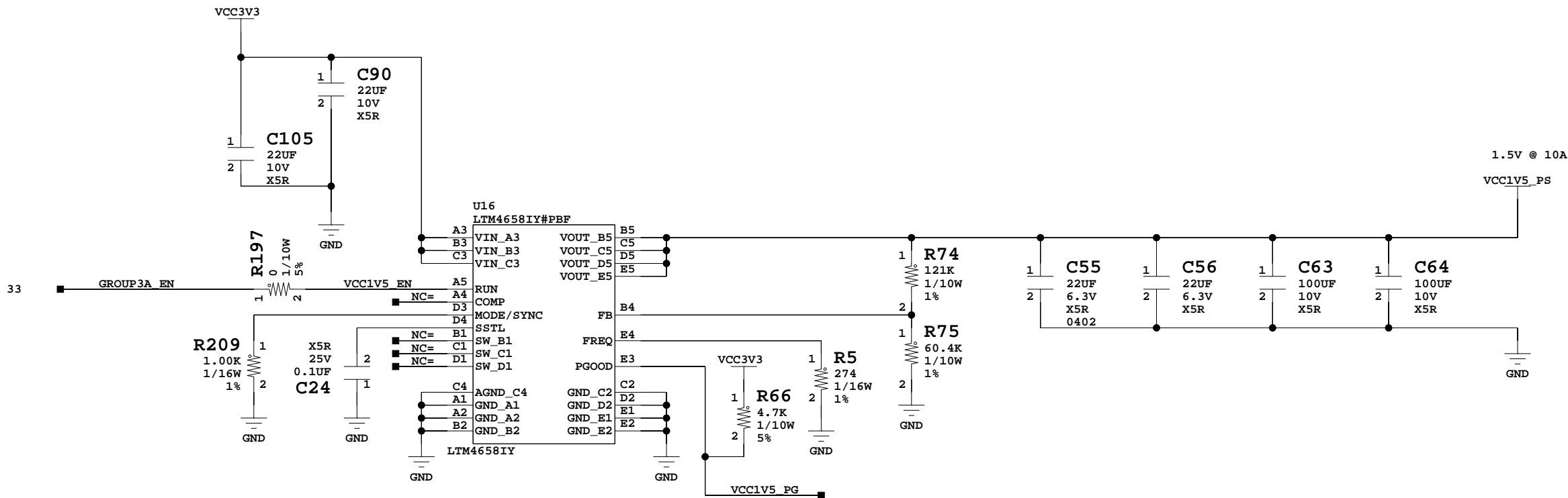
1.0V 10A Power Regulator

TRIPLE CROWN			
Title: 1.0V 10A Power Regulator			
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size:	B	Rev:	01
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1.8V 10A Power Regulator

TRIPLE CROWN			
Title: 1.8V 10A Power Regulator			
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
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1.5V 10A Power Regulator

TRIPLE CROWN

Title: 1.5V 10A Power Regulator

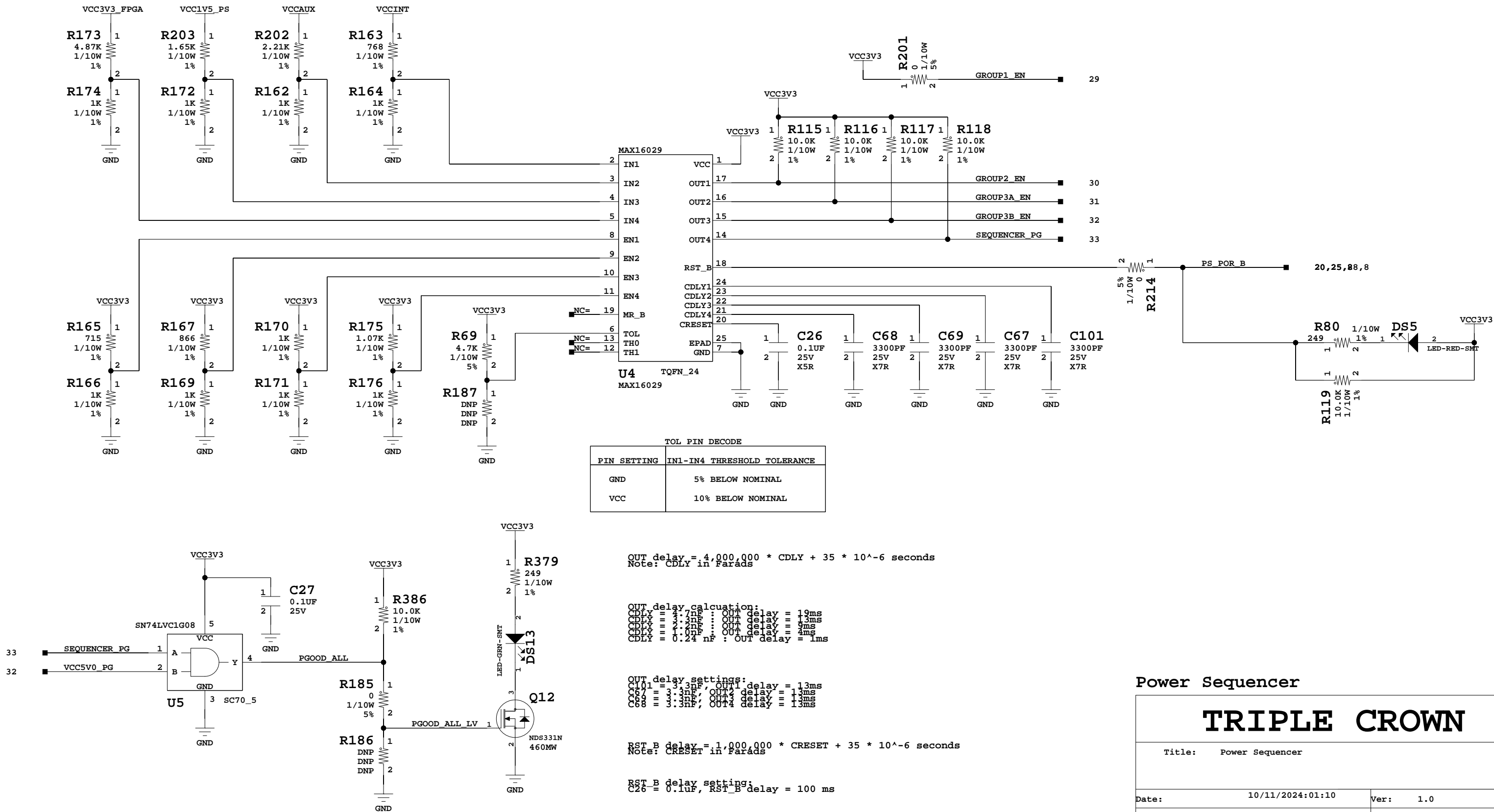
Date: 10/11/2024:01:10 Ver: 1.0

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Power Sequence Order

- 1: VCCINT (1.0V)
2: VCCAUX (1.8V), VCCPLL (1.8V)
3: VCC1V5 (1.5V), VCC3.3V_FPGA (3.3V), VCC5V0 (5V)



Power Sequencer

TRIPLE CROWN

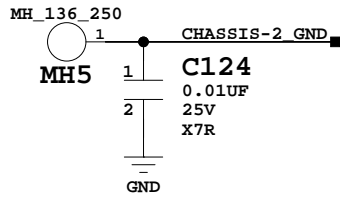
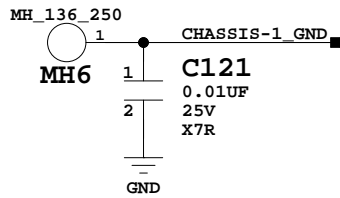
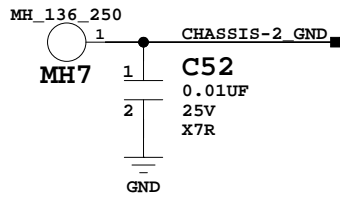
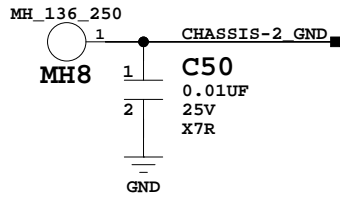
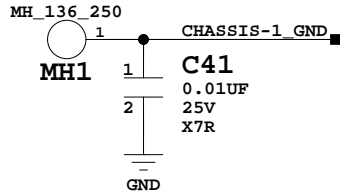
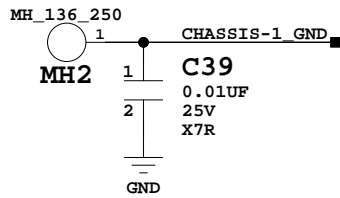
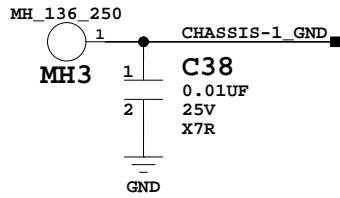
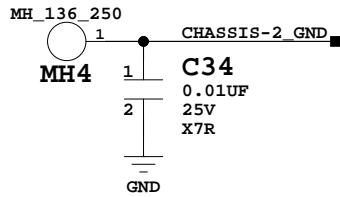
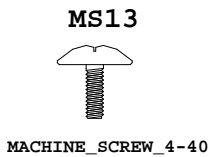
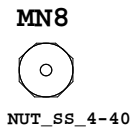
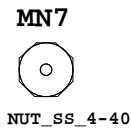
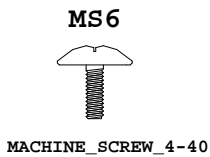
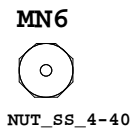
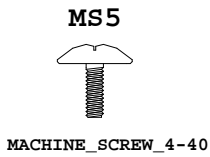
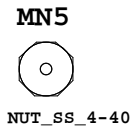
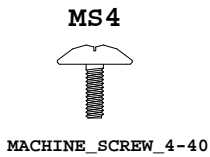
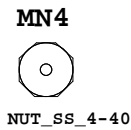
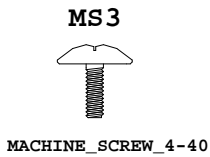
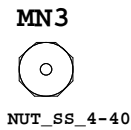
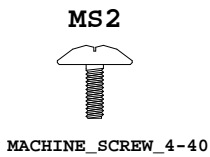
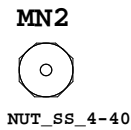
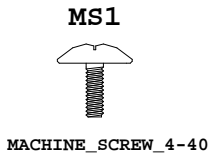
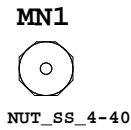
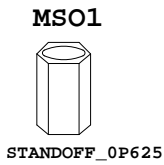
Title: Power Sequencer

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Update P/Ns
for
Mechanical Parts



Mechanical Components

TRIPLE CROWN

Title: Mechanical Components

Date: 10/11/2024:01:11 Ver: 1.0

Sheet Size: B Rev: 01

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