LCR CHASSIS MANAGER

9/9/2024:
Removed C31, C48-C50, C121, C124, C440-C443, C455-C457, C460-C464, C532-C534

9/10/2024:
Reduced size of R37, R38, R207, R208, R228, R232, R233, R417 from 0402 to 0201
Reduced size of C54, C55 from 0603 to 0402

10/22/2024:
Changed part number of U35 from 88E1116R to 88E1512
Added L13-L15, C31, C48, C49
Removed C34, C38, C39, C41, C52, R15, R46-R49, R245, R247, R248

10/31/2024:
Disconnected 4 mounting holes from GND and connected to CHASSIS-1_GND
Disconnected 4 mounting holes from GND and connected to CHASSIS-2_GND
Added C38, C39, C41, C121 between CHASSIS-1_GND and GND
Added C34, C50, C52, C124 between CHASSIS-2_GND and GND
Swapped some DDR3 DQ signals within byte groupings 0, 1, 2, 3

11/8/2024:
Removed C433, C434, C444, C465-C467
Changed C148 part number to C1608X5R1A106K080AC
Changed PCB part number from 7PC-000-0455.PCB to 7PC-000-0455

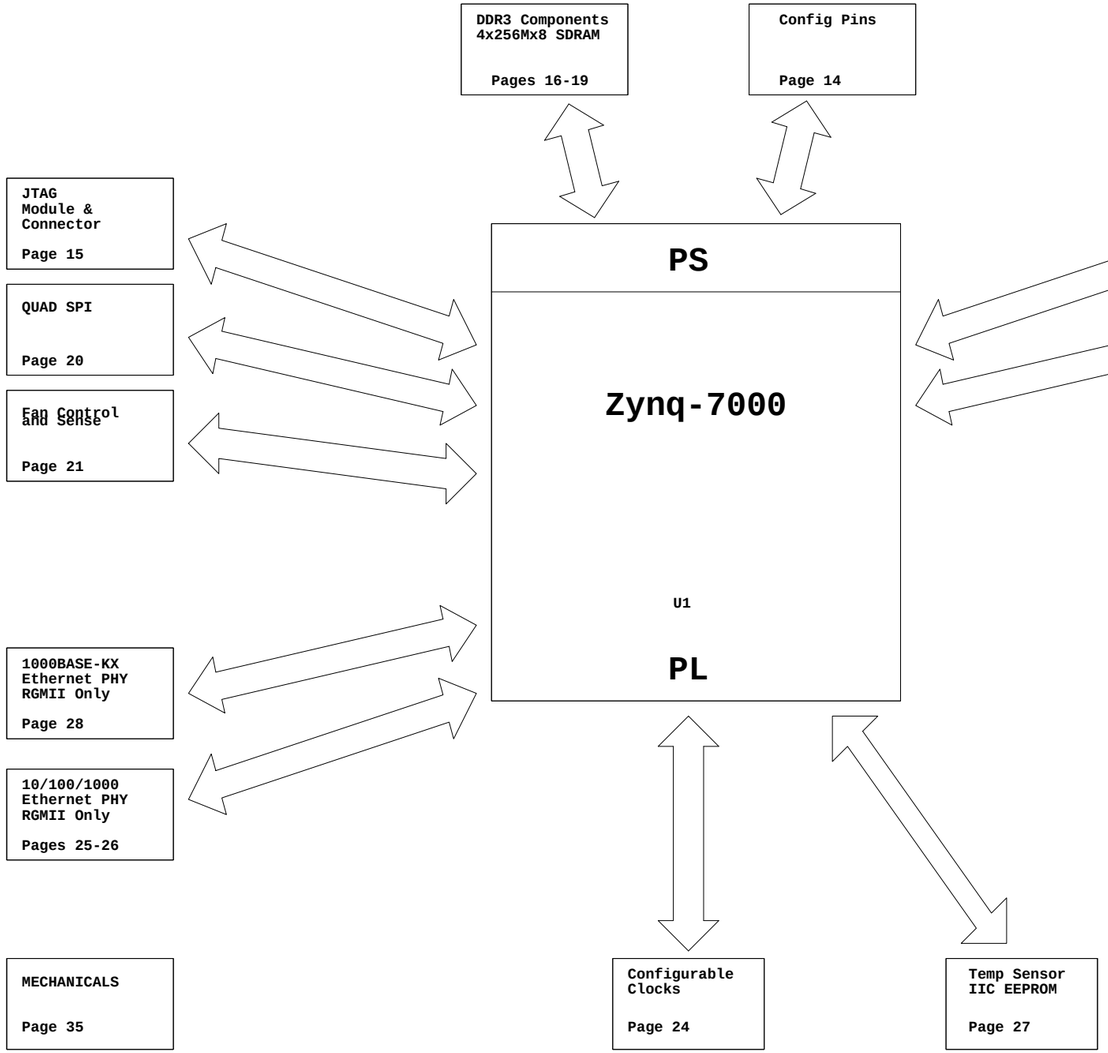
PCB1

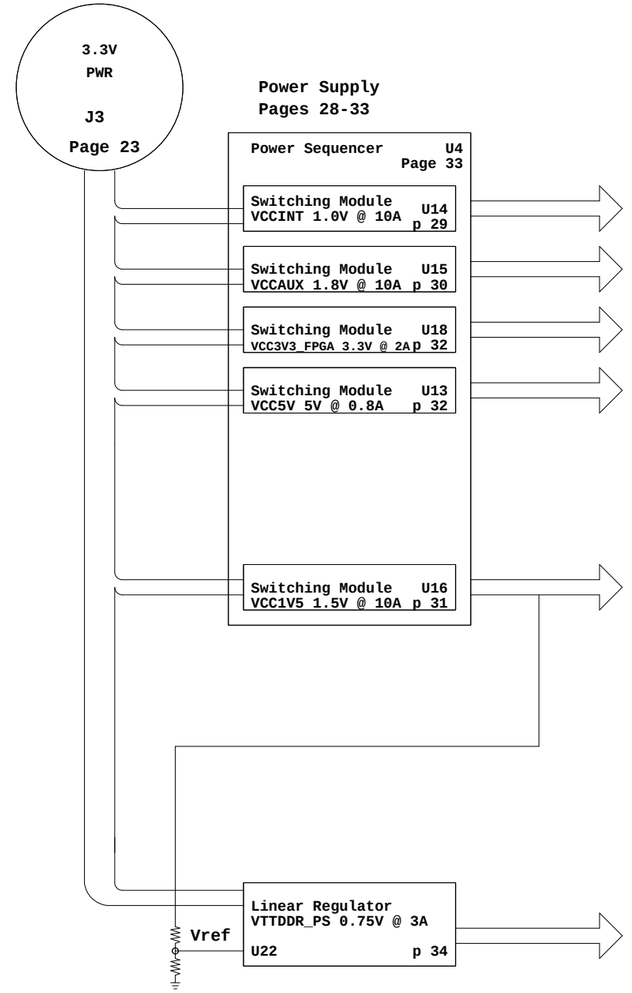
PCB

7PC-000-0455

TRIPLE CROWN

Title: LCR CHASSIS MANAGER	ASSY P/N: 7CM-100-0001-1 PCB P/N: 7PC-000-0455 SCH P/N: 7PC-000-0455-SCH.SCH
Date: 10/11/2024:01:10	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 1 of 35	Drawn By TG

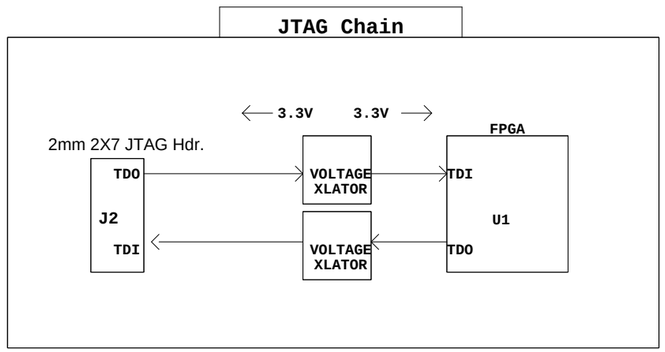




IIC Addressing

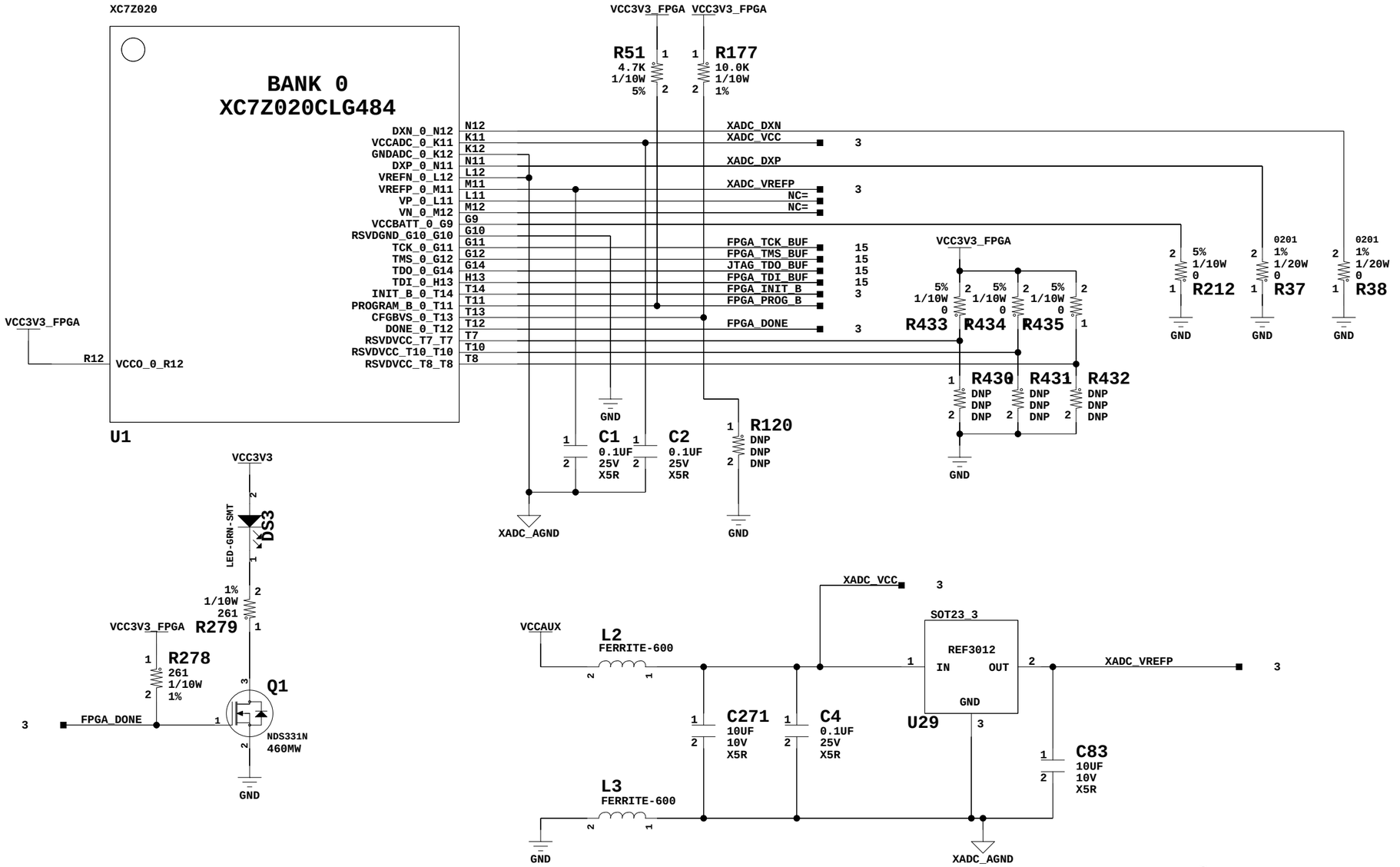
0b1011101	SI570
0b1010100	EEPROM
0b0100000	Fan Controller
0b1001000	Local Temp Sensor

JTAG Chain



TRIPLE CROWN

Title:	Block Diagram		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	2 of 35	Drawn By	TG

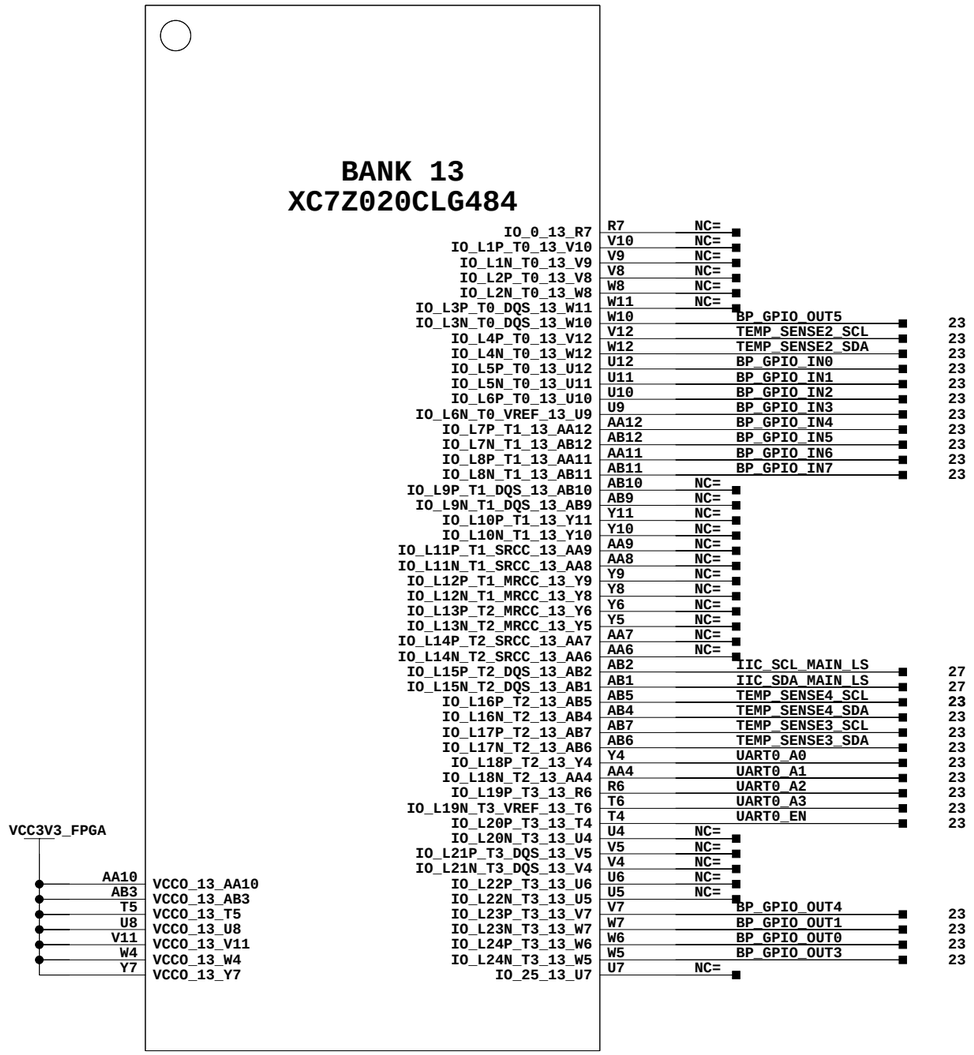


Zynq Bank 0

TRIPLE CROWN

Title:	Zynq Bank 0		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	3 of 35	Drawn By	TG

XC7Z020

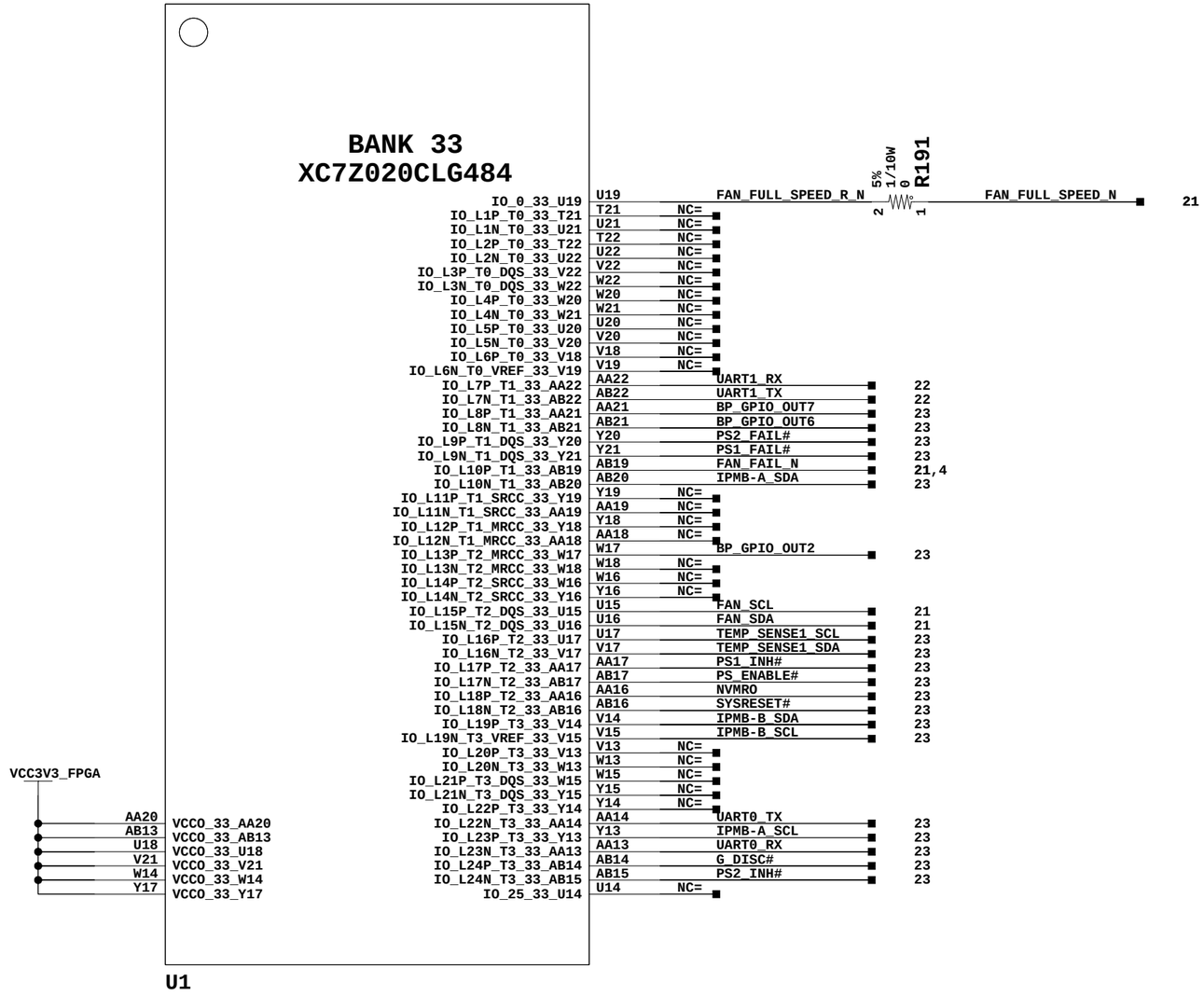


Zynq Bank 13

TRIPLE CROWN

Title:	Zynq Bank 13		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	4 of 35	Drawn By	TG

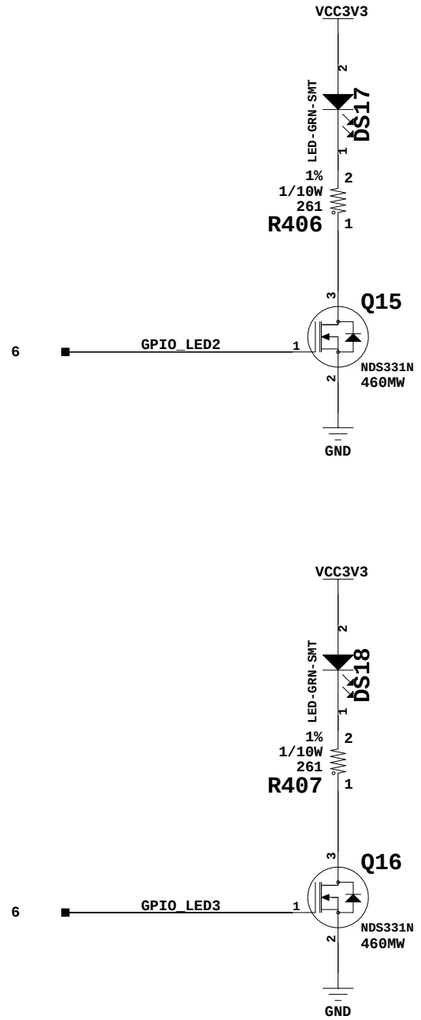
XC7Z020

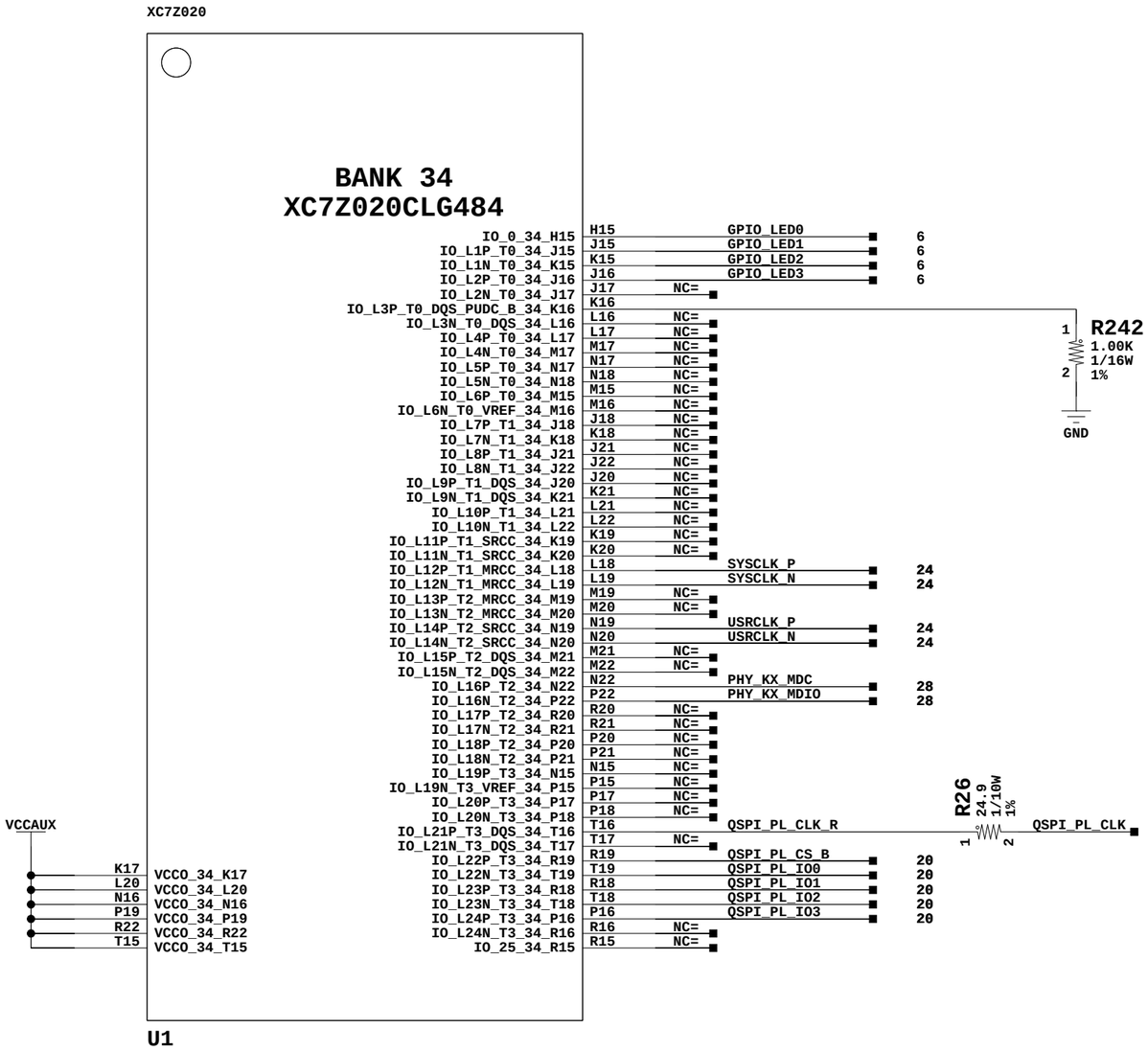


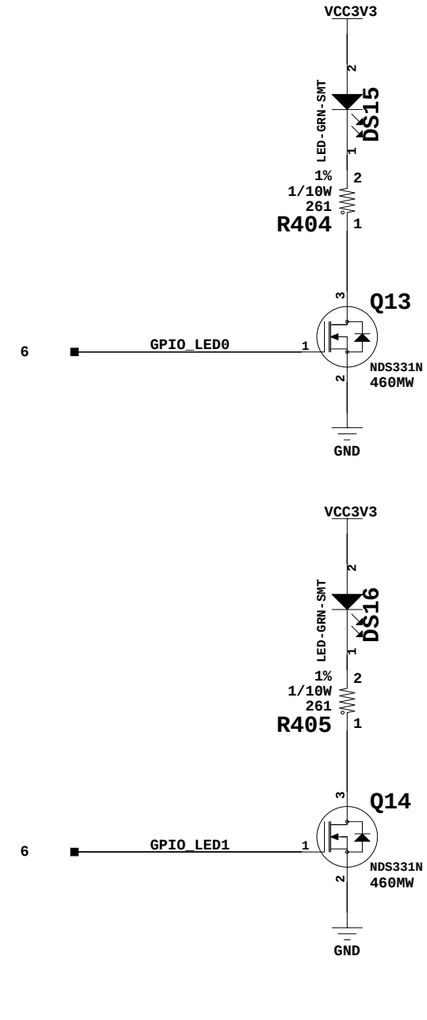
Zynq Bank 33

TRIPLE CROWN

Title:	Zynq Bank 33		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	5 of 35	Drawn By	TG



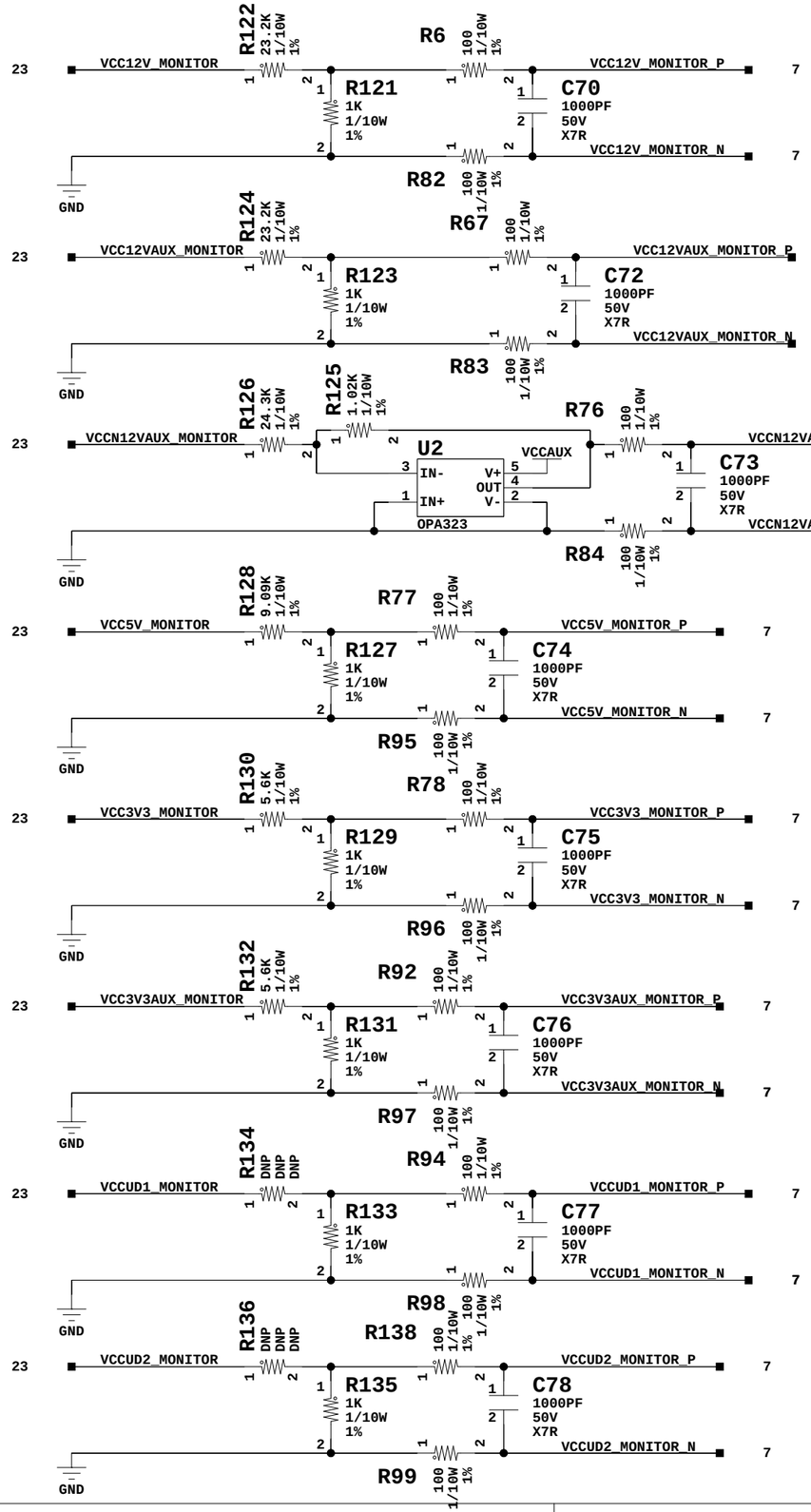


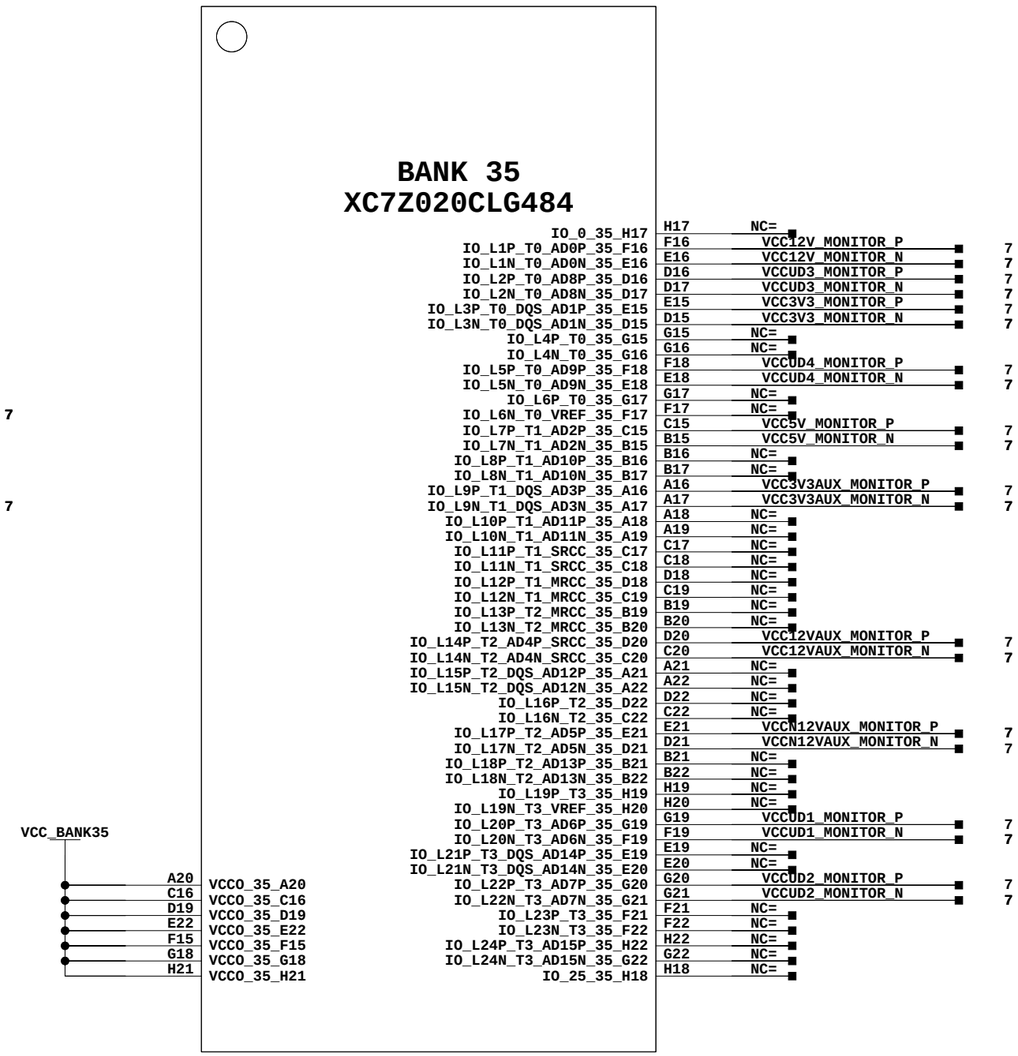


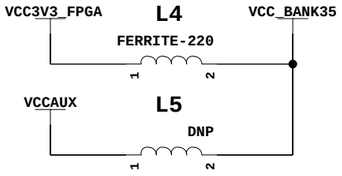
Zynq Bank 34

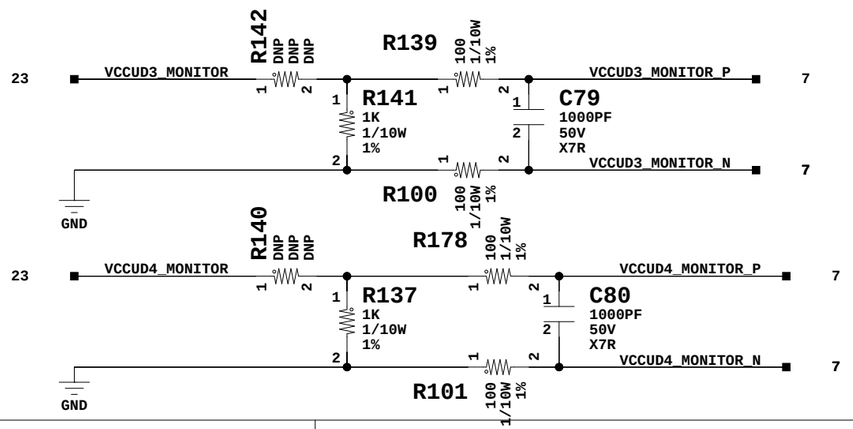
TRIPLE CROWN

Title:	Zynq Bank 34		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	6 of 35	Drawn By	TG





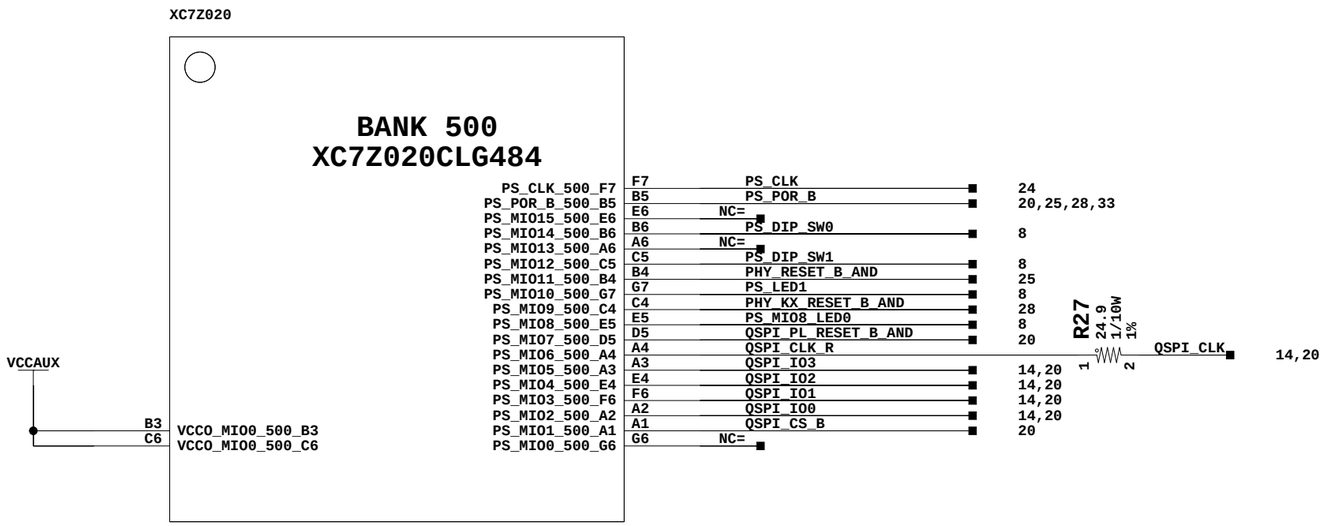


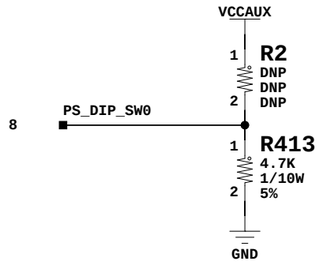


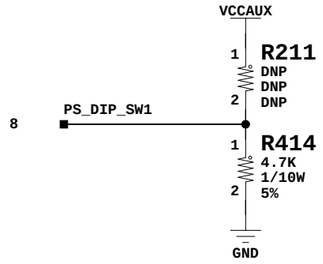
Zynq Bank 35

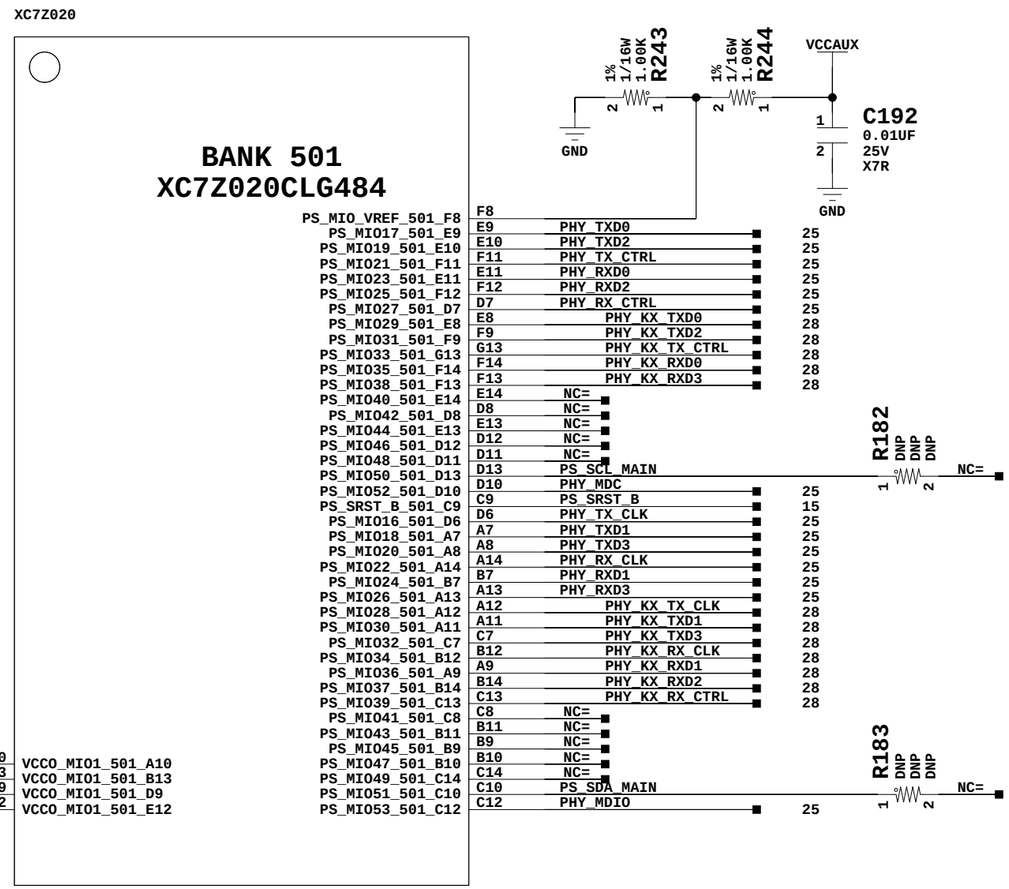
TRIPLE CROWN

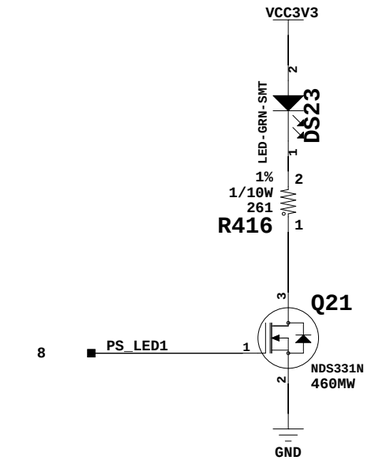
Title: Zynq Bank 35	
Date: 10/11/2024:01:10	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 7 of 35	Drawn By TG

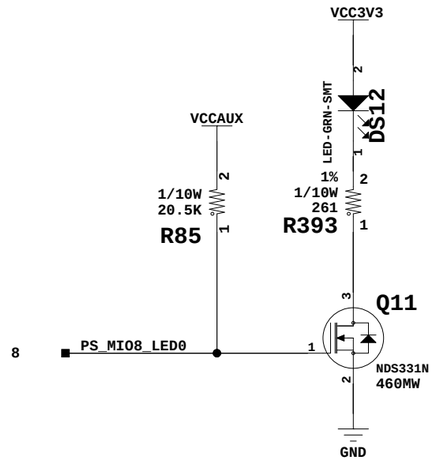












Zynq Banks 500, 501

TRIPLE CROWN

Title:	Zynq Banks 500, 501		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	8 of 35	Drawn By	TG

XC7Z020

BANK 502
XC7Z020CLG484

PS_DDR_DRST_B_502_F3	F3	PS_DDR3_RESET_B	16,17,18,19
PS_DDR_DQ0_502_D1	D1	PS_DDR3_DQ3	16
PS_DDR_DQ1_502_C3	C3	PS_DDR3_DQ4	16
PS_DDR_DQ2_502_B2	B2	PS_DDR3_DQ0	16
PS_DDR_DQ3_502_D3	D3	PS_DDR3_DQ2	16
PS_DDR_DM0_502_B1	B1	PS_DDR3_DM0	16
PS_DDR_DQS_P0_502_C2	C2	PS_DDR3_DQS0_P	16
PS_DDR_DQS_N0_502_D2	D2	PS_DDR3_DQS0_N	16
PS_DDR_DQ4_502_E3	E3	PS_DDR3_DQ6	16
PS_DDR_DQ5_502_E1	E1	PS_DDR3_DQ7	16
PS_DDR_DQ6_502_F2	F2	PS_DDR3_DQ5	16
PS_DDR_DQ7_502_F1	F1	PS_DDR3_DQ1	16
PS_DDR_DQ8_502_G2	G2	PS_DDR3_DQ8	17
PS_DDR_DQ9_502_G1	G1	PS_DDR3_DQ10	17
PS_DDR_DQ10_502_L1	L1	PS_DDR3_DQ9	17
PS_DDR_DQ11_502_L2	L2	PS_DDR3_DQ13	17
PS_DDR_DM1_502_H3	H3	PS_DDR3_DM1	17
PS_DDR_DQS_P1_502_H2	H2	PS_DDR3_DQS1_P	17
PS_DDR_DQS_N1_502_J2	J2	PS_DDR3_DQS1_N	17
PS_DDR_DQ12_502_L3	L3	PS_DDR3_DQ14	17
PS_DDR_DQ13_502_K1	K1	PS_DDR3_DQ11	17
PS_DDR_DQ14_502_J1	J1	PS_DDR3_DQ12	17
PS_DDR_DQ15_502_K3	K3	PS_DDR3_DQ15	17
PS_DDR_A14_502_G4	G4	PS_DDR3_A14	16,17,18,19
PS_DDR_A13_502_F4	F4	PS_DDR3_A13	16,17,18,19
PS_DDR_A12_502_H4	H4	PS_DDR3_A12	16,17,18,19
PS_DDR_A11_502_G5	G5	PS_DDR3_A11	16,17,18,19
PS_DDR_A10_502_J3	J3	PS_DDR3_A10	16,17,18,19
PS_DDR_A9_502_H5	H5	PS_DDR3_A9	16,17,18,19
PS_DDR_A8_502_J5	J5	PS_DDR3_A8	16,17,18,19
PS_DDR_A7_502_J6	J6	PS_DDR3_A7	16,17,18,19
PS_DDR_A6_502_J7	J7	PS_DDR3_A6	16,17,18,19
PS_DDR_A5_502_K5	K5	PS_DDR3_A5	16,17,18,19
PS_DDR_A4_502_K6	K6	PS_DDR3_A4	16,17,18,19
PS_DDR_A3_502_L4	L4	PS_DDR3_A3	16,17,18,19
PS_DDR_VRN_502_M7	M7	PS_VRN	9
PS_DDR_VRP_502_N7	N7	PS_VRP	9
PS_DDR_CKP_502_N4	N4	PS_DDR3_CLK_P	16,17,18,19
PS_DDR_CKN_502_N5	N5	PS_DDR3_CLK_N	16,17,18,19
PS_DDR_A2_502_K4	K4	PS_DDR3_A2	16,17,18,19
PS_DDR_A1_502_M5	M5	PS_DDR3_A1	16,17,18,19
PS_DDR_A0_502_M4	M4	PS_DDR3_A0	16,17,18,19
PS_DDR_BA2_502_M6	M6	PS_DDR3_BA2	16,17,18,19
PS_DDR_BA1_502_L6	L6	PS_DDR3_BA1	16,17,18,19
PS_DDR_BA0_502_L7	L7	PS_DDR3_BA0	16,17,18,19
PS_DDR_ODT_502_P5	P5	PS_DDR3_ODT	16,17,18,19
PS_DDR_CS_B_502_P6	P6	PS_DDR3_CS_B	16,17,18,19
PS_DDR_CKE_502_V3	V3	PS_DDR3_CKE	16,17,18,19
PS_DDR_WE_B_502_R4	R4	PS_DDR3_WE_B	16,17,18,19
PS_DDR_CAS_B_502_P3	P3	PS_DDR3_CAS_B	16,17,18,19
PS_DDR_RAS_B_502_R5	R5	PS_DDR3_RAS_B	16,17,18,19
PS_DDR_DQ16_502_M1	M1	PS_DDR3_DQ16	18
PS_DDR_DQ17_502_T3	T3	PS_DDR3_DQ21	18
PS_DDR_DQ18_502_N3	N3	PS_DDR3_DQ22	18
PS_DDR_DQ19_502_T1	T1	PS_DDR3_DQ19	18
PS_DDR_DM2_502_P1	P1	PS_DDR3_DM2	18
PS_DDR_DQS_P2_502_N2	N2	PS_DDR3_DQS2_P	18
PS_DDR_DQS_N2_502_P2	P2	PS_DDR3_DQS2_N	18
PS_DDR_DQ20_502_R3	R3	PS_DDR3_DQ18	18
PS_DDR_DQ21_502_T2	T2	PS_DDR3_DQ17	18
PS_DDR_DQ22_502_M2	M2	PS_DDR3_DQ20	18
PS_DDR_DQ23_502_R1	R1	PS_DDR3_DQ23	18
PS_DDR_DQ24_502_AA3	AA3	PS_DDR3_DQ27	19
PS_DDR_DQ25_502_U1	U1	PS_DDR3_DQ24	19
PS_DDR_DQ26_502_AA1	AA1	PS_DDR3_DQ29	19
PS_DDR_DQ27_502_U2	U2	PS_DDR3_DQ26	19
PS_DDR_DM3_502_AA2	AA2	PS_DDR3_DM3	19
PS_DDR_DQS_P3_502_V2	V2	PS_DDR3_DQS3_P	19
PS_DDR_DQS_N3_502_W2	W2	PS_DDR3_DQS3_N	19
PS_DDR_DQ28_502_W1	W1	PS_DDR3_DQ31	19
PS_DDR_DQ29_502_Y3	Y3	PS_DDR3_DQ30	19
PS_DDR_DQ30_502_W3	W3	PS_DDR3_DQ28	19
PS_DDR_DQ31_502_Y1	Y1	PS_DDR3_DQ25	19
PS_DDR_VREF0_502_H7	H7		
PS_DDR_VREF1_502_P7	P7		

E2	VCCO_DDR_502_E2	VCC1V5_PS
F5	VCCO_DDR_502_F5	
H1	VCCO_DDR_502_H1	
J4	VCCO_DDR_502_J4	
K7	VCCO_DDR_502_K7	
M3	VCCO_DDR_502_M3	
N6	VCCO_DDR_502_N6	
R2	VCCO_DDR_502_R2	
V1	VCCO_DDR_502_V1	

U1

VTTVREF_PS

C194
1
2
0.01UF
25V
X7R

GND

VTTVREF_PS

C193
1
2
0.01UF
25V
X7R

GND

VCC1V5_PS

R63
1
2
80.6
1/10W
1%

PS_VRN 9
PS_VRP 9

R62
1
2
80.6
1/10W
1%

GND

Zynq Bank 502

TRIPLE CROWN

Title: Zynq Bank 502

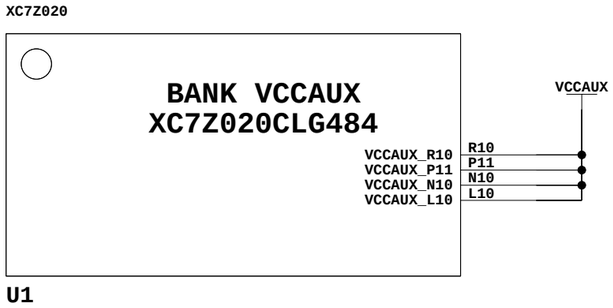
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	9 of 35	Drawn By	TG

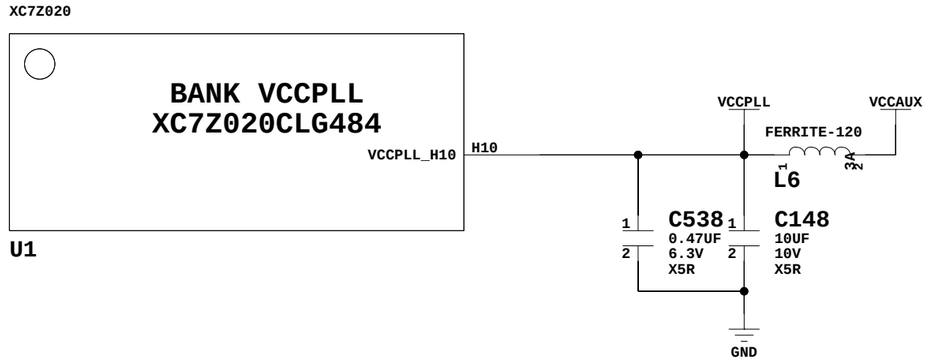
Increase width of VCCPLL route to
as wide as possible (target is > 20 mils)

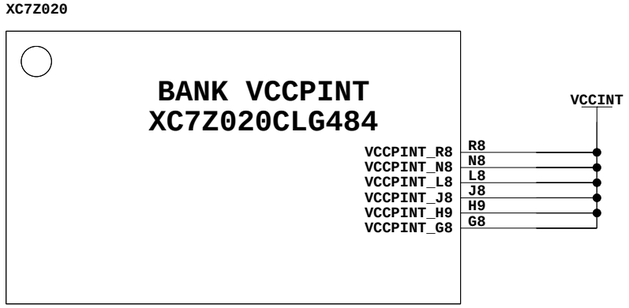
Reduce the length of VCCPLL route as much as possible

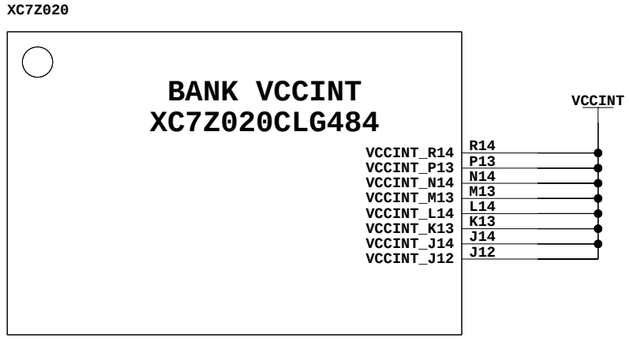
Place C538 inside the VIA field to provide
as short as possible connection to VCCPLL (H10) and GND

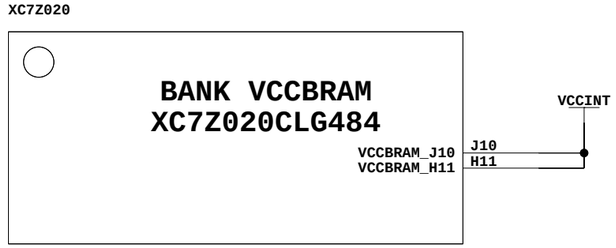
Place C539 inside the open space cross adjacent to H10
for the short possible connection to VCCPLL









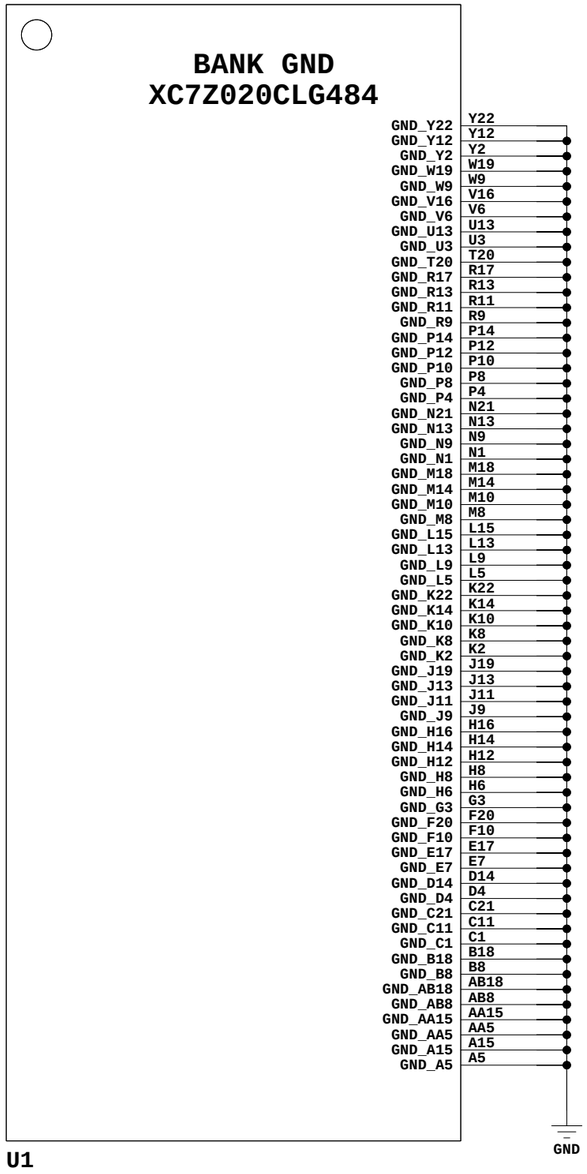


Zynq Power Pins

TRIPLE CROWN

Title: Zynq Power Pins			
Date:	10/11/2024:01:11	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	10 of 35	Drawn By	TG

XC7Z020



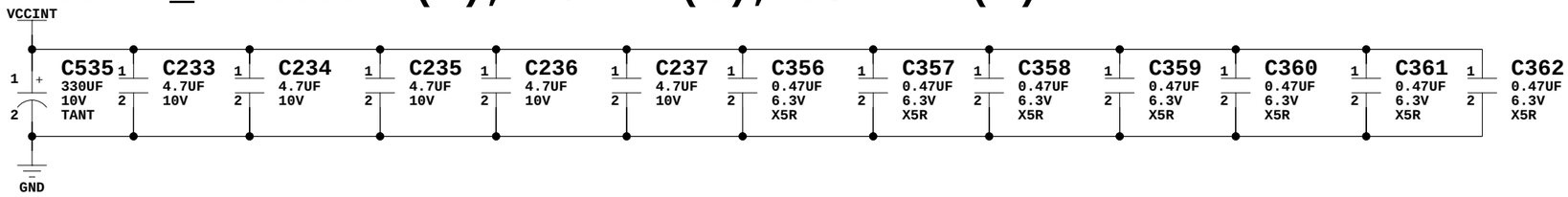
Zynq GND

TRIPLE CROWN

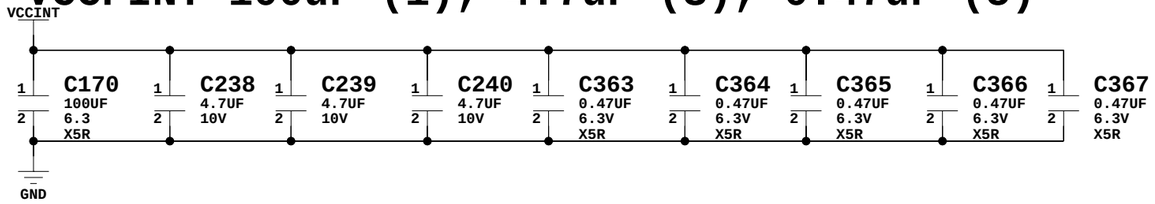
Title:	Zynq GND		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	
Sheet	11 of 35	Drawn By	TG

BYPASS CAPACITORS

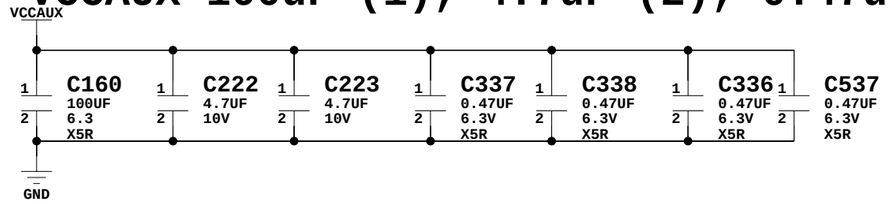
VCCINT_PL 330uF (1), 4.7uF (5), 0.47uF (7)



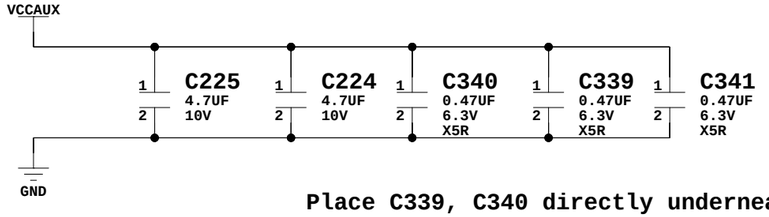
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



VCCAUX 100uF (1), 4.7uF (2), 0.47uF (4)

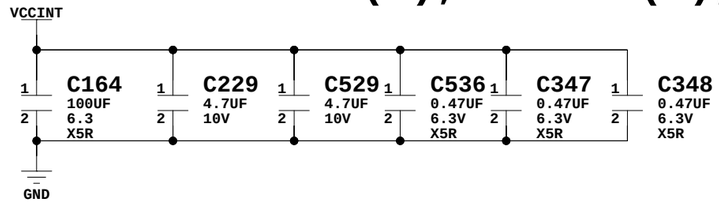


VCCPAUX 100uF (0), 4.7uF (2), 0.47uF (3)

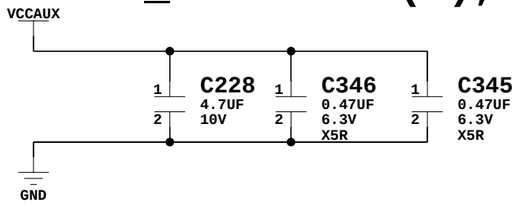


Place C339, C340 directly underneath the FPGA
as short as possible connection to VCCPAUX and GND

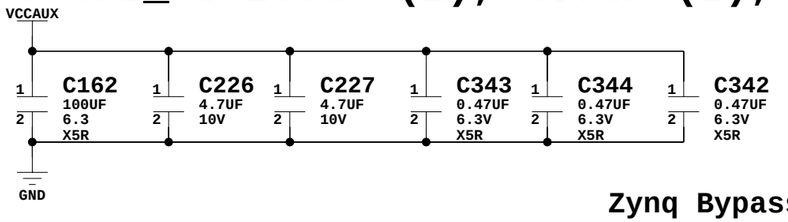
VCCBRAM 100uF (1), 4.7uF (2), 0.47uF (3)



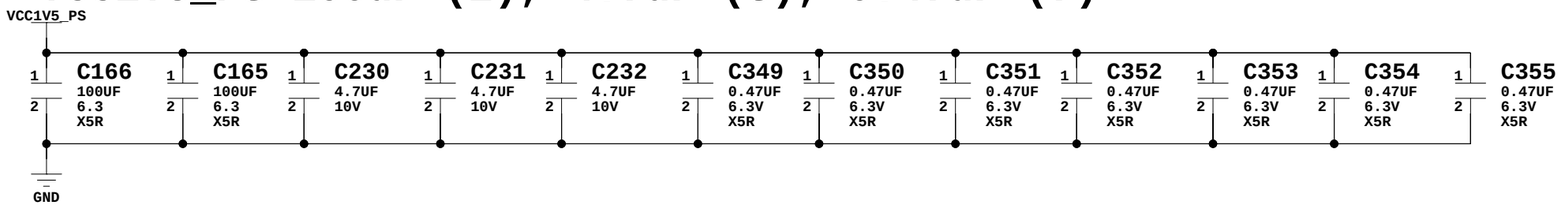
VCCP0_PS 100uF (0), 4.7uF (1), 0.47uF (2)



VCCP1_PS 100uF (1), 4.7uF (2), 0.47uF (3)



VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)

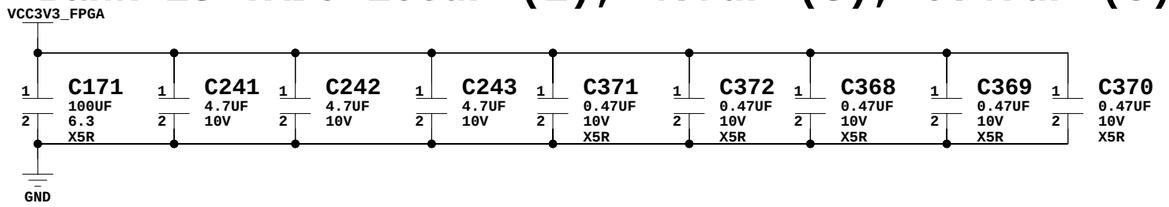


Zynq Bypass Capacitors

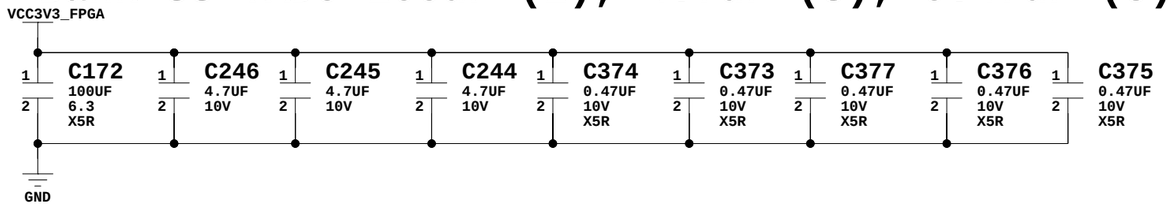
TRIPLE CROWN

Title:	Zynq Bypass Capacitors		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	12 of 35	Drawn By	TG

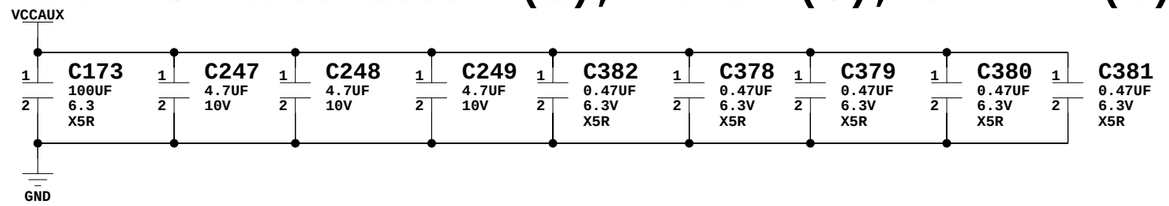
Bank 13 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



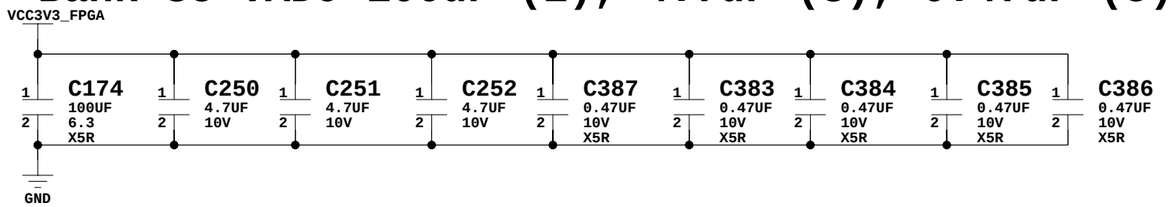
Bank 33 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 34 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 35 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)

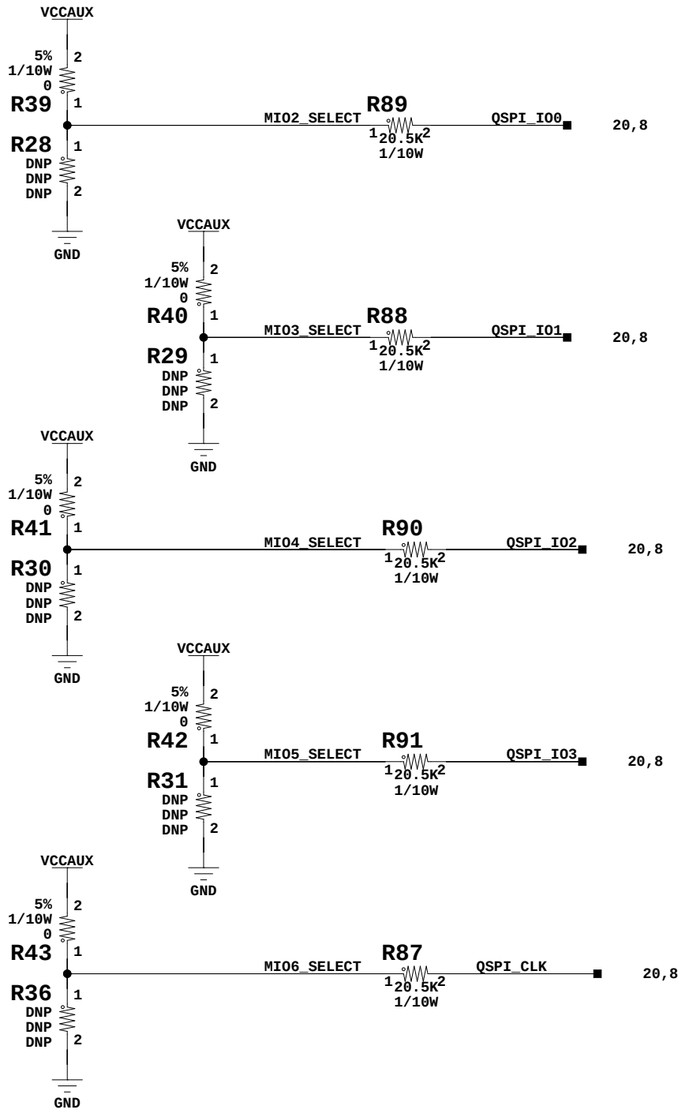


Zynq Bypass Capacitors

TRIPLE CROWN

Title:	Zynq Bypass Capacitors		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	13 of 35	Drawn By	TG

MIO[6:2] SELECTION HEADERS



Zynq Config Pins

TRIPLE CROWN

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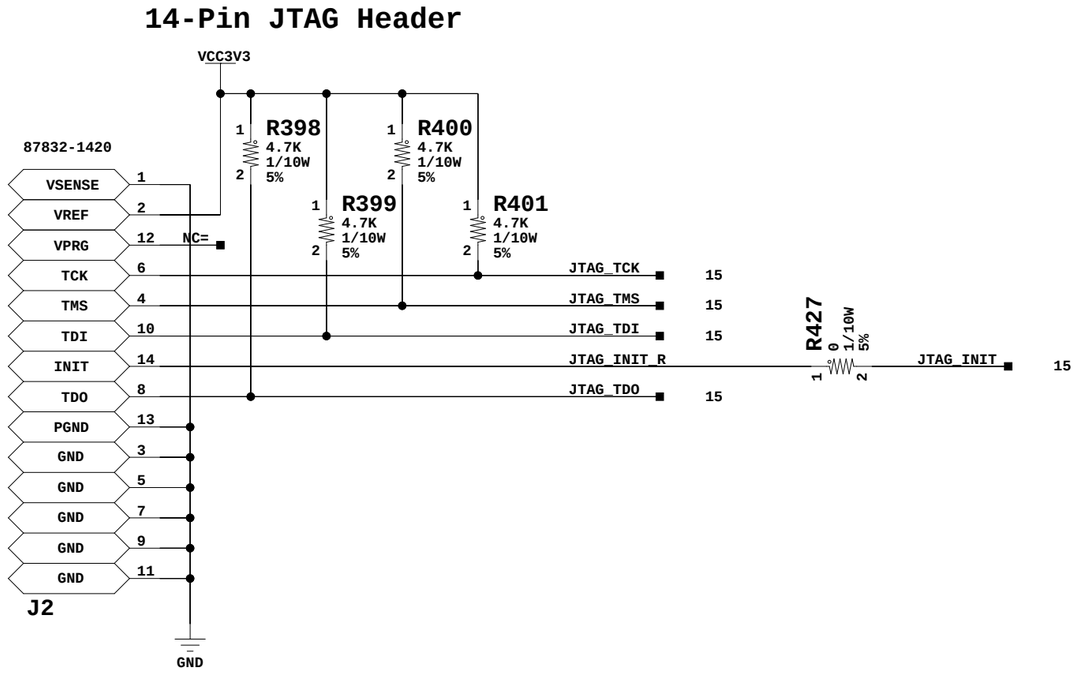
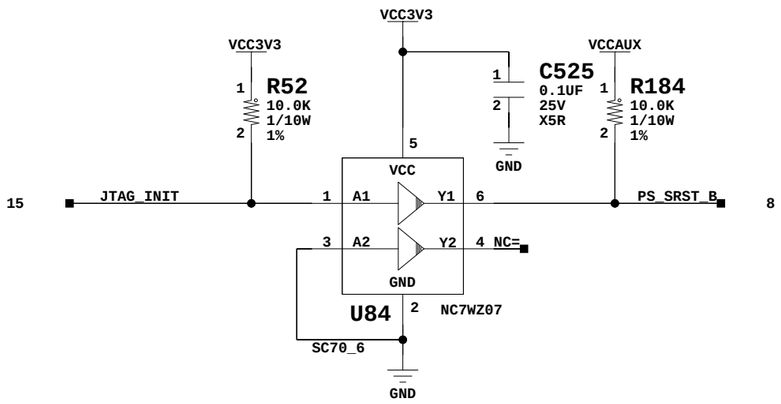
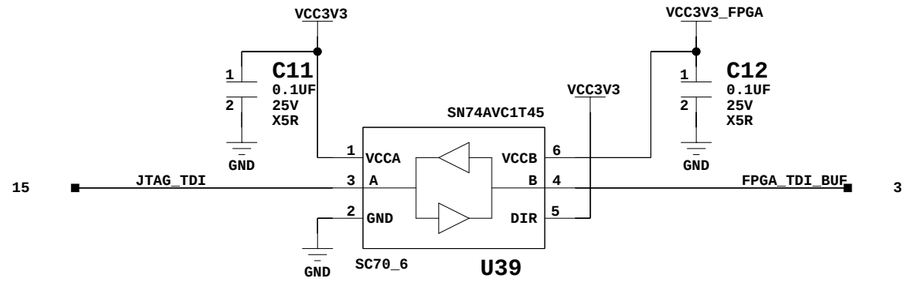
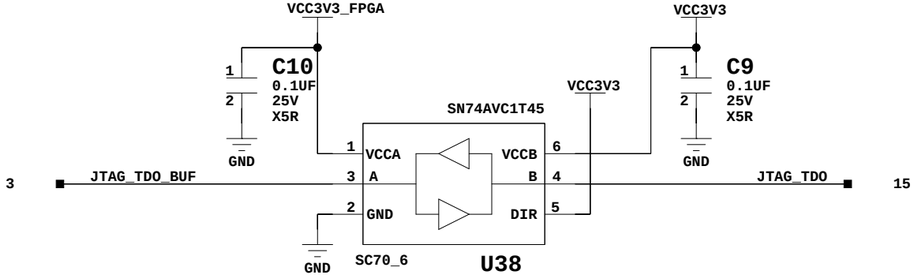
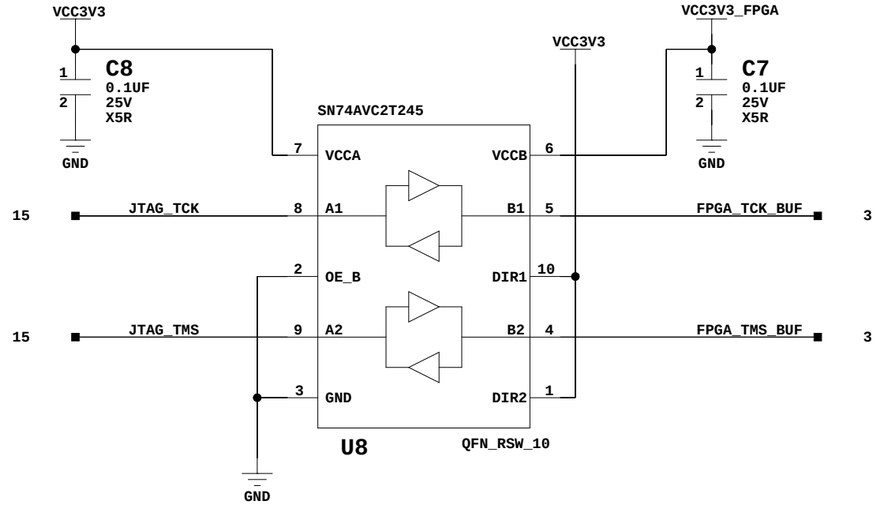
Sheet Size: B		Rev:	02
Sheet	14 of 35	Drawn By	TG











JTAG Buffers, JTAG Hdr

TRIPLE CROWN	
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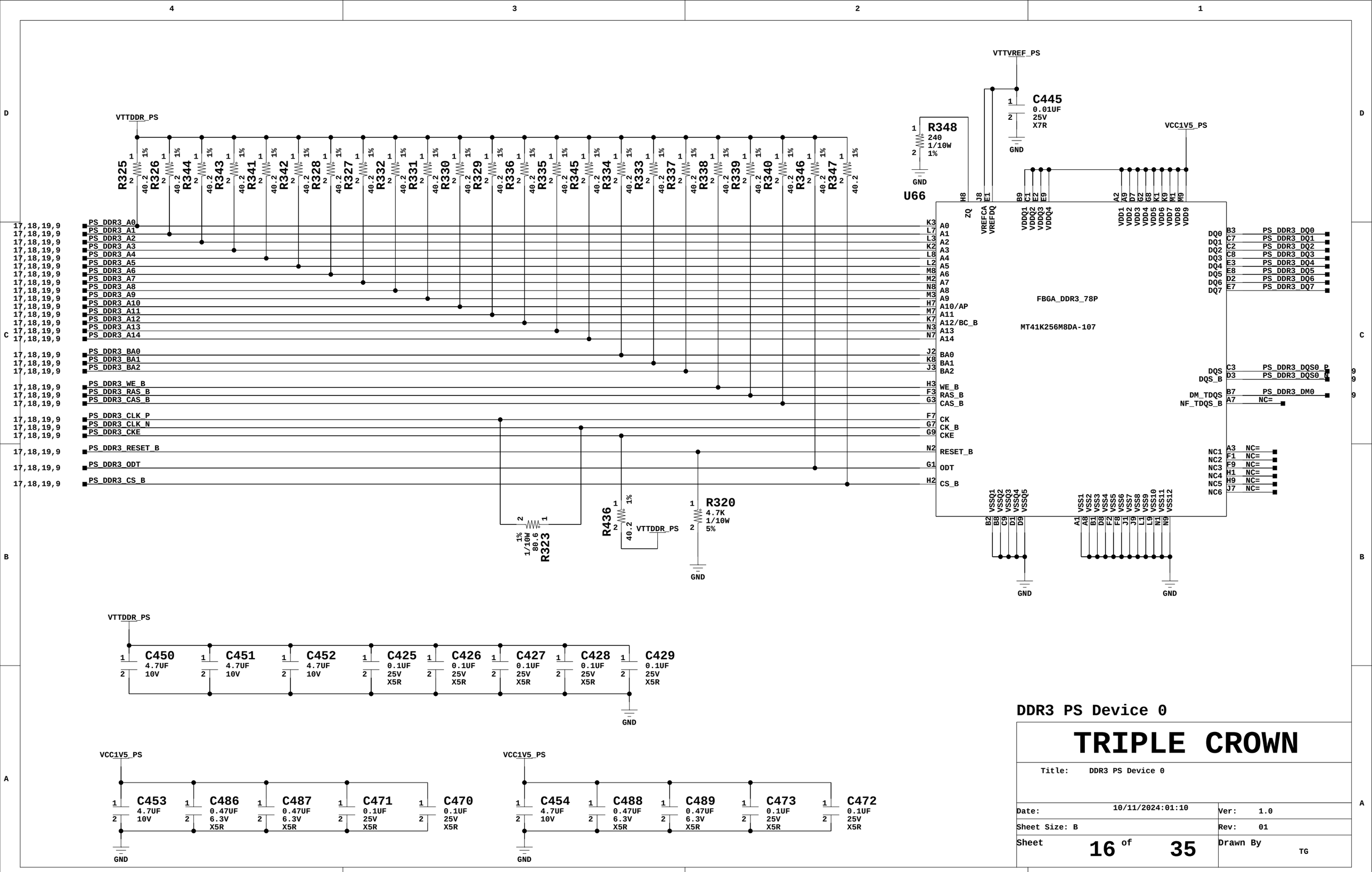
Date: 10/11/2024:01:10	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 15 of 35	Drawn By TG



DDR3 PS Device 0

TRIPLE CROWN

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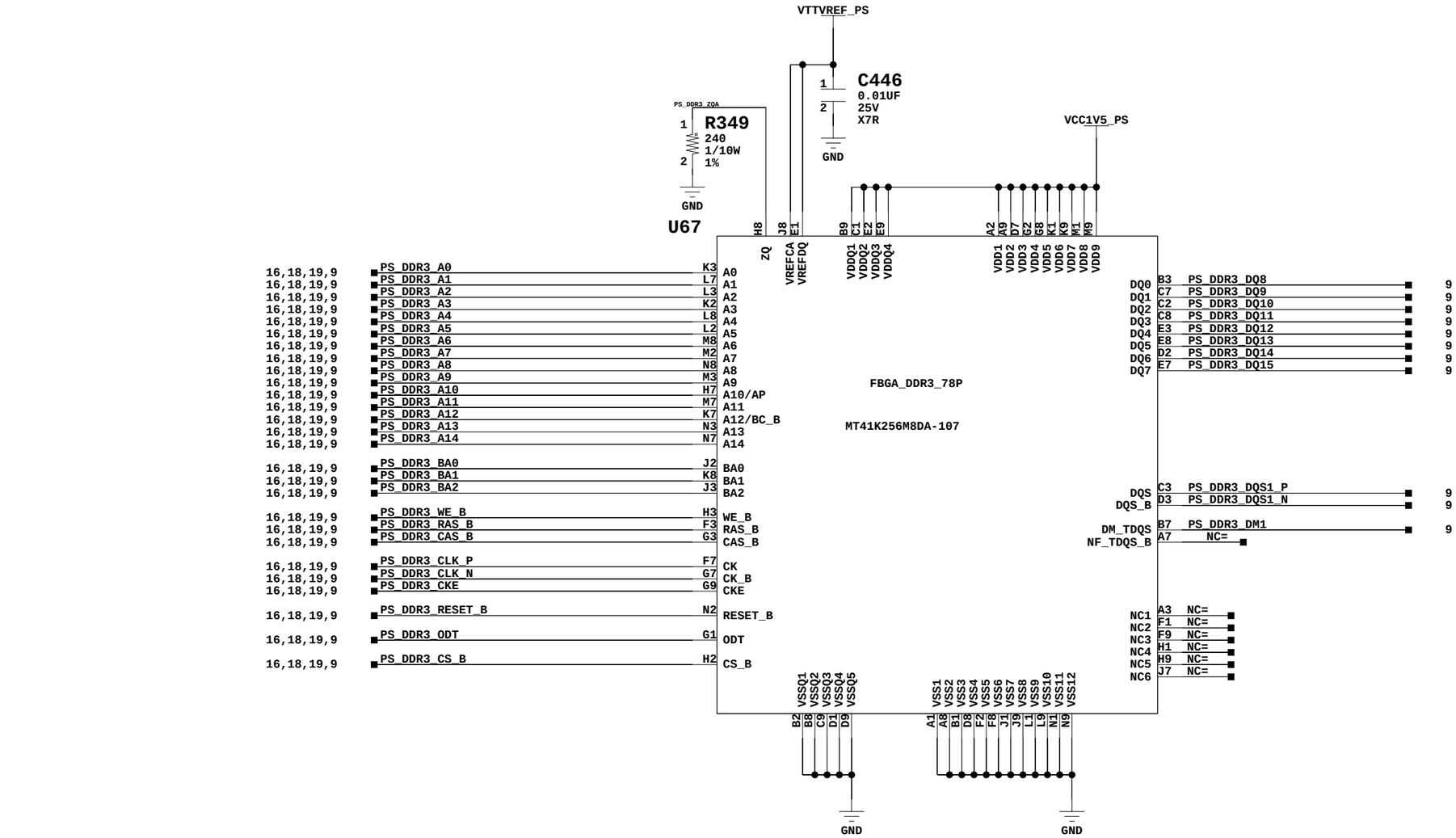
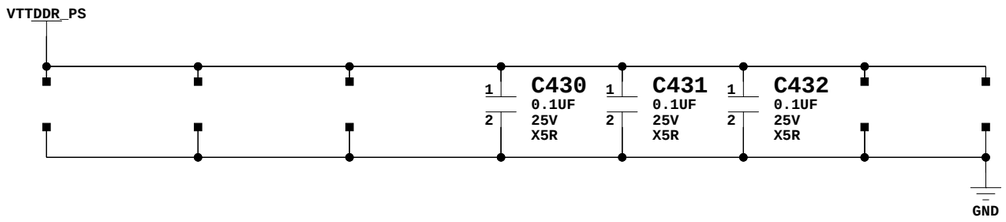
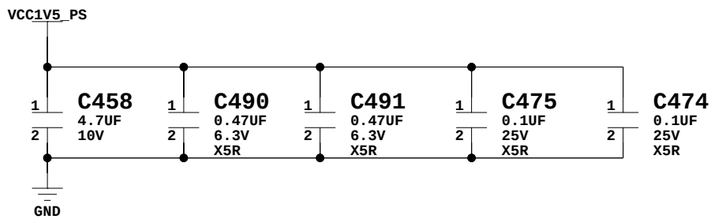
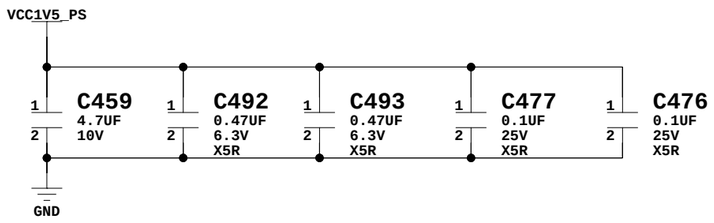
Sheet Size: B		Rev:	01
Sheet	16 of 35	Drawn By	TG









DDR3 PS Device 1

TRIPLE CROWN

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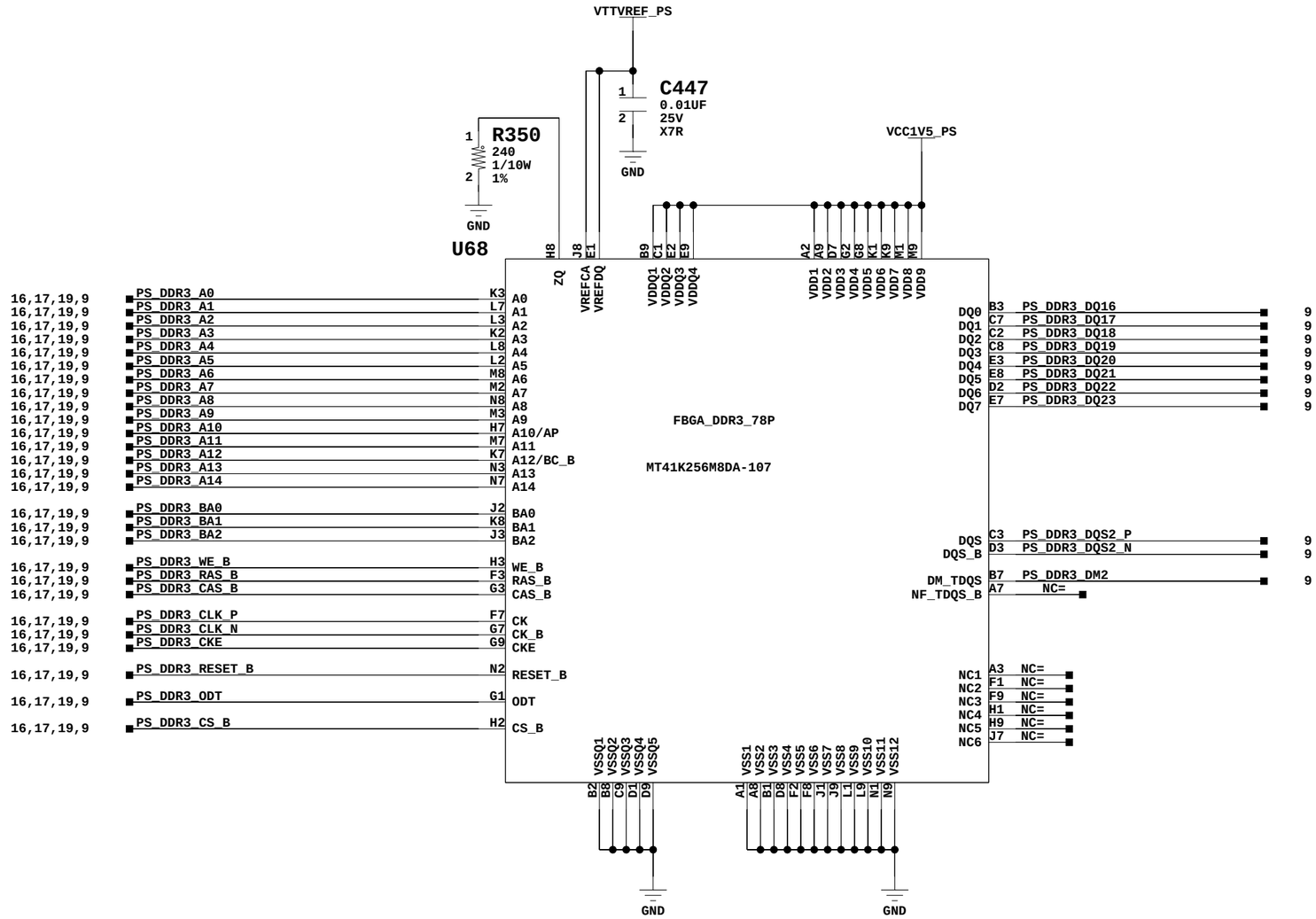
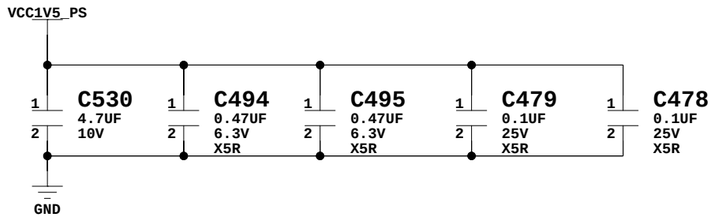
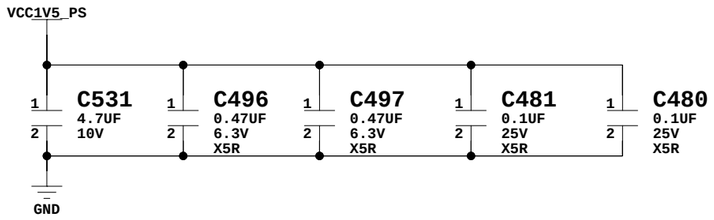
Sheet Size: B		Rev:	01
Sheet	17 of 35	Drawn By	TG







DDR3 PS Device 2

TRIPLE CROWN

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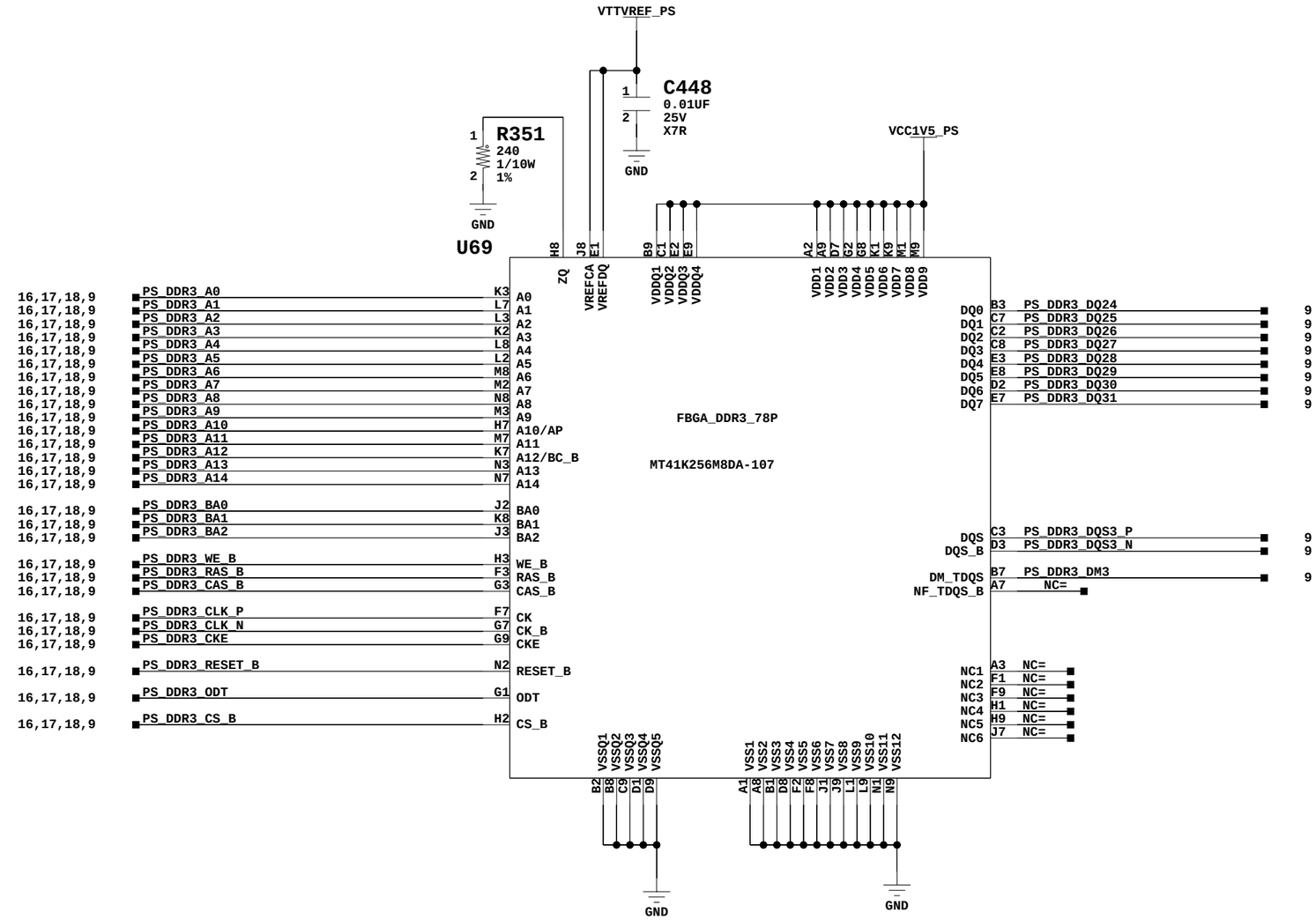
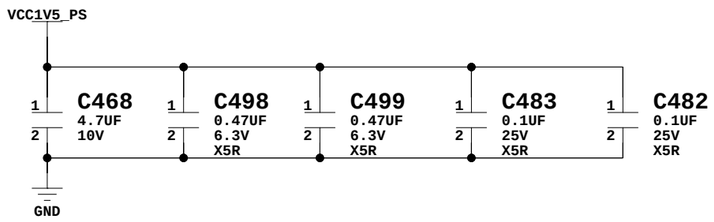
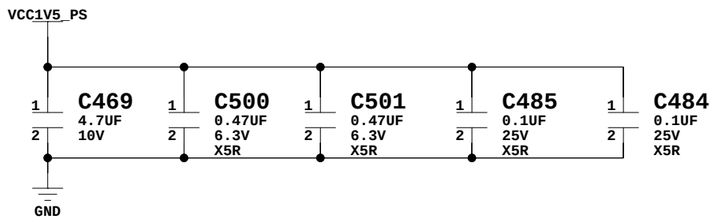
Sheet	18 of 35	Drawn By	TG







DDR3 PS Device 3

TRIPLE CROWN

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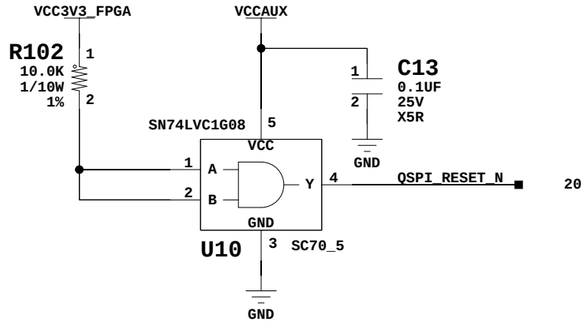
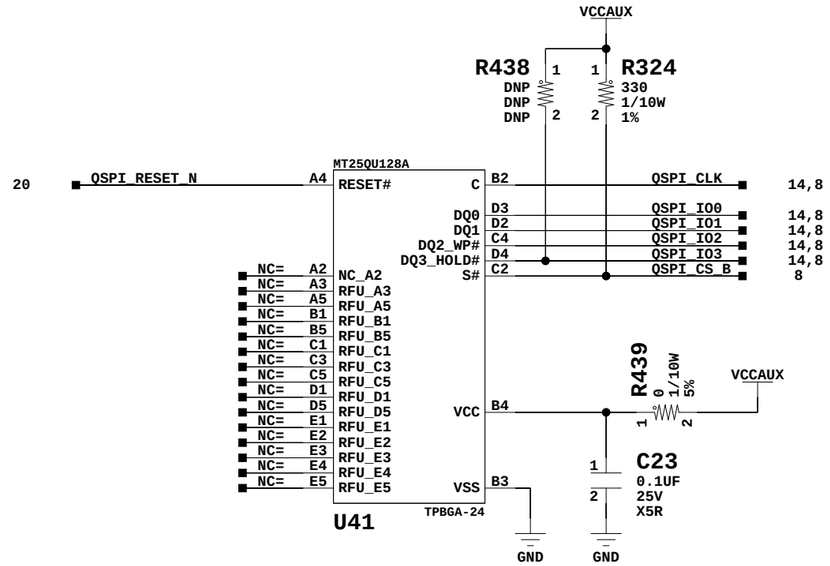
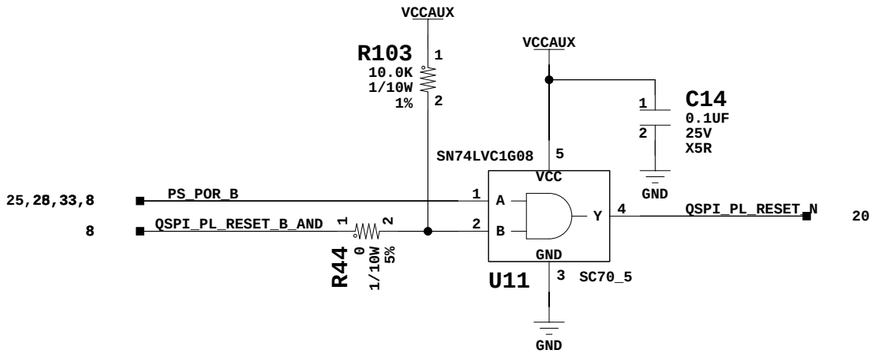
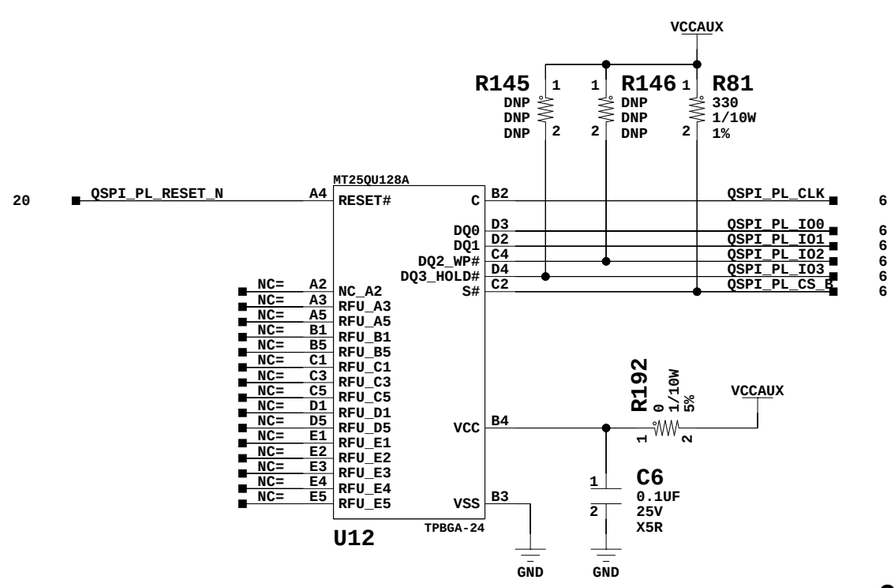
Sheet Size: B		Rev:	01
Sheet	19 of 35	Drawn By	TG





PS Quad SPI





PL Quad SPI

Quad SPI

TRIPLE CROWN

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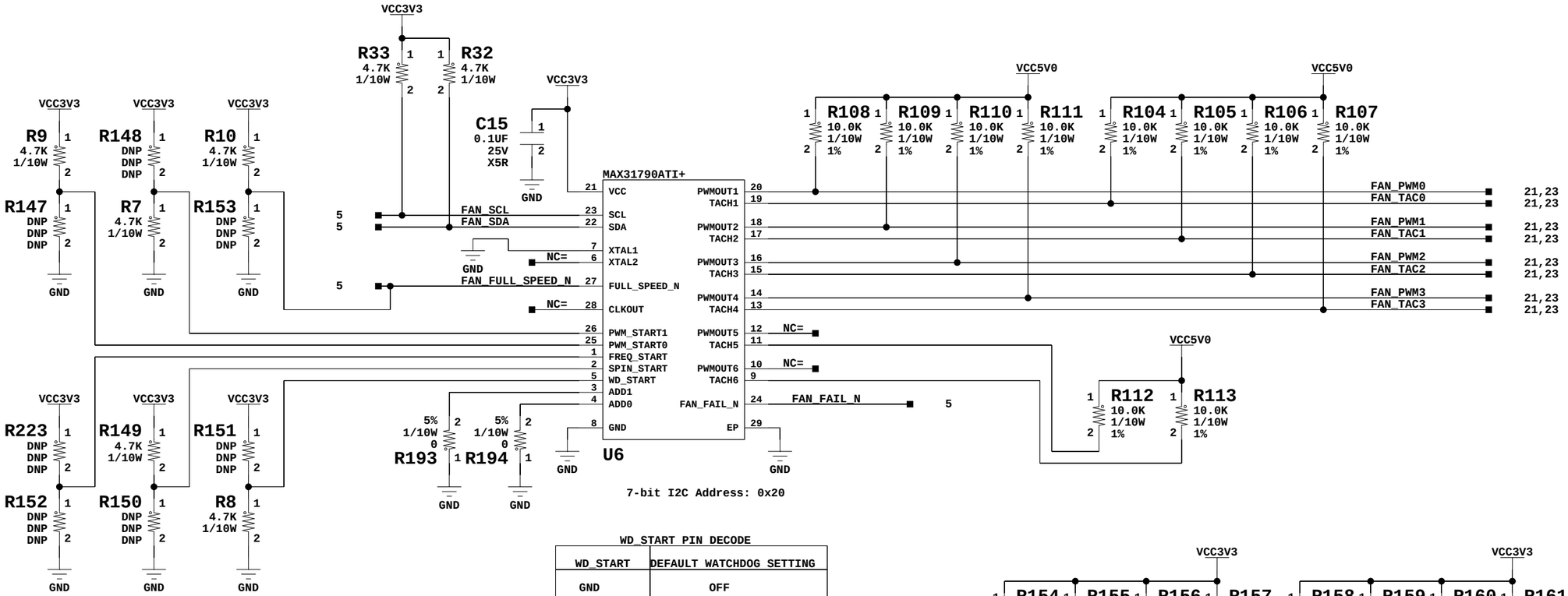
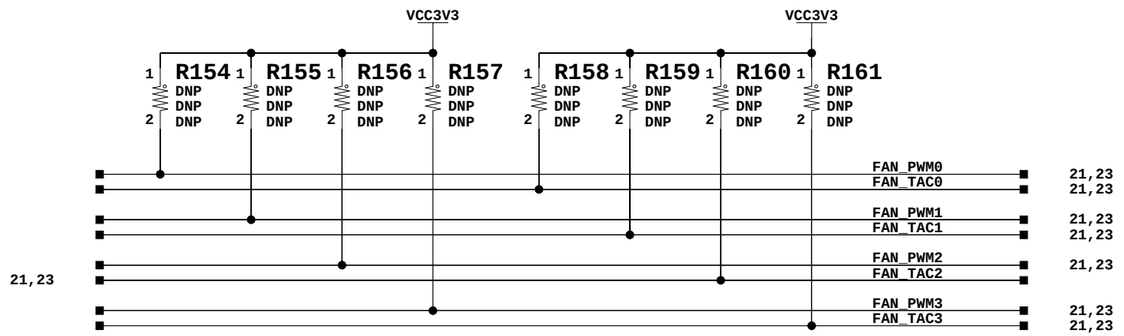
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	20 of 35	Drawn By	TG





WD_START PIN DECODE

WD_START	DEFAULT WATCHDOG SETTING
GND	OFF
VCC	ON

FREQ_START PIN DECODE

FREQ_START	FAN DEFAULT DRIVE SETTING
GND	30 Hz
VCC	25 KHz
UNCONNECTED	1.47 KHz

PWM_START PINS DECODE

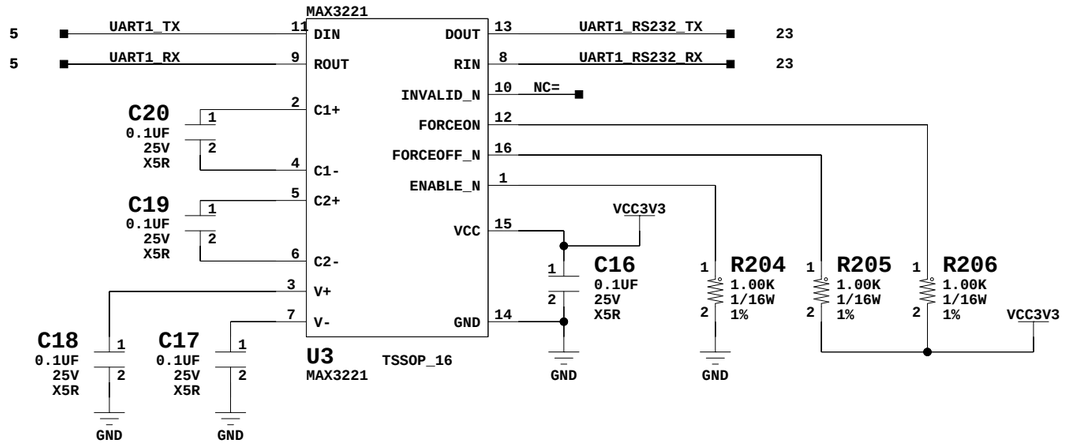
PWM_START0	PWM_START1	PWM DUTY CYCLE (%)
GND	GND	0
GND	UNCONNECTED	30
GND	VCC	40
UNCONNECTED	GND	50
UNCONNECTED	VCC	60
VCC	GND	75
VCC	VCC	100

Fan Control and Sense

TRIPLE CROWN

Title: Fan Control and Sense

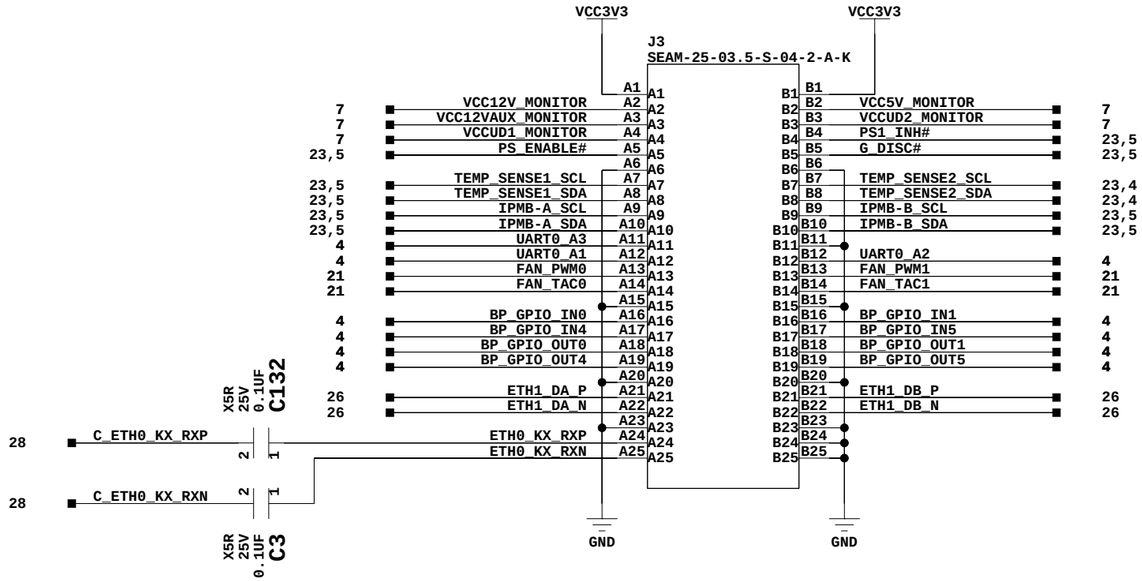
Date: 10/11/2024:01:10	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 21 of 35	Drawn By TG

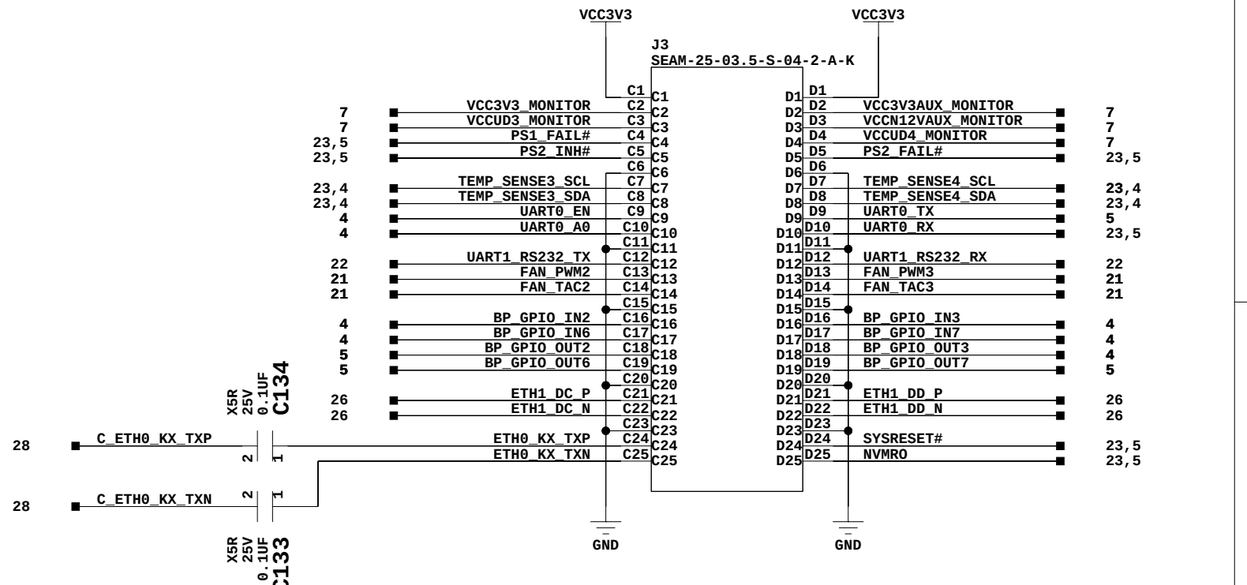


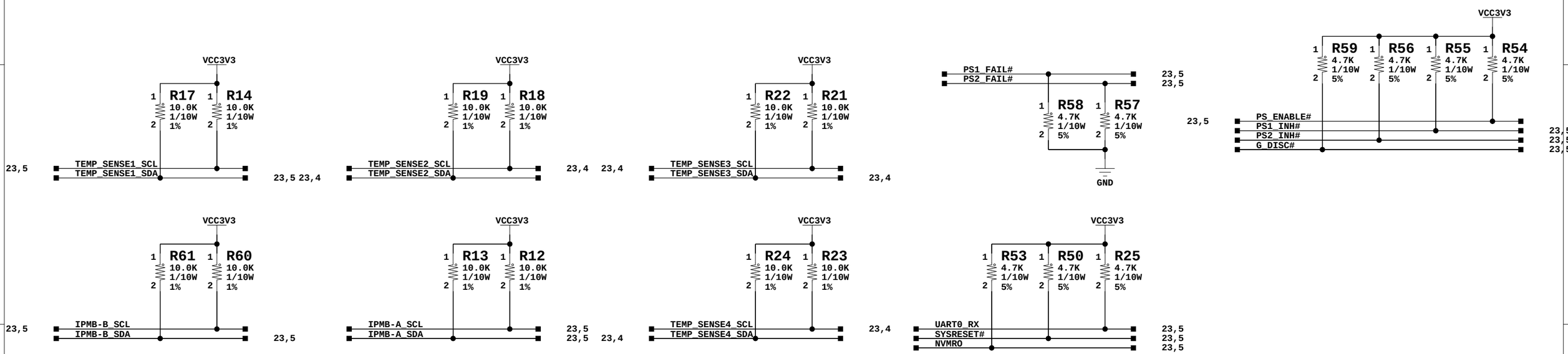
RS-232 UART

TRIPLE CROWN

Title:	RS-232 UART		
Date:	10/11/2024:01:10	Ver:	1.1
Sheet Size: B		Rev:	02
Sheet	22 of 35	Drawn By	BF







I/O CONNECTOR

TRIPLE CROWN

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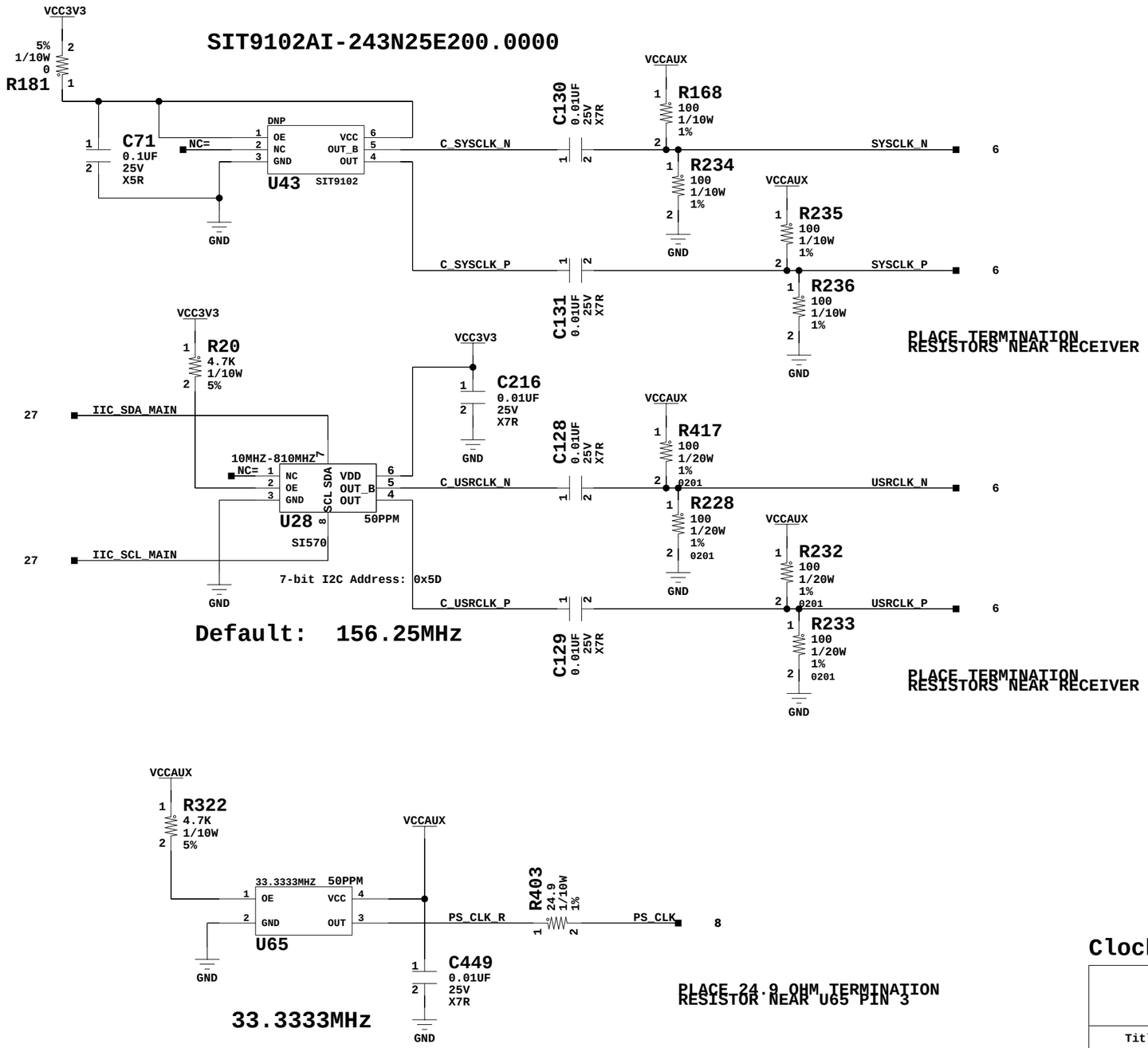
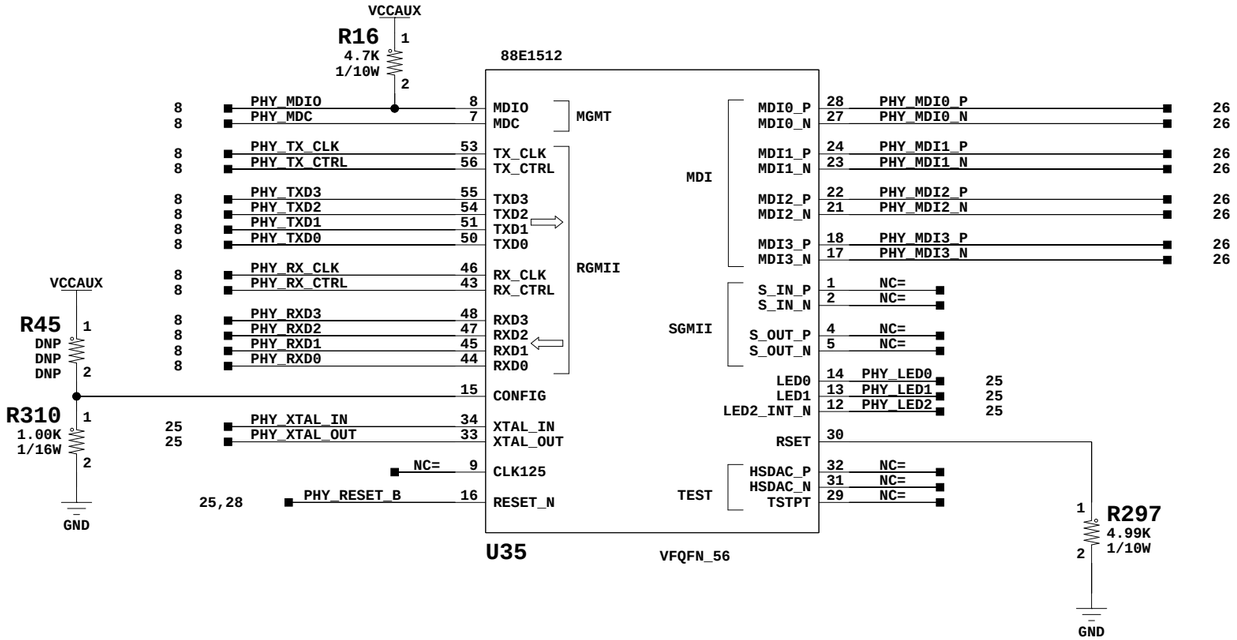
Date:	10/11/2024:01:10	Ver:	1.1
Sheet Size: B		Rev:	02
Sheet	23 of 35	Drawn By	BF

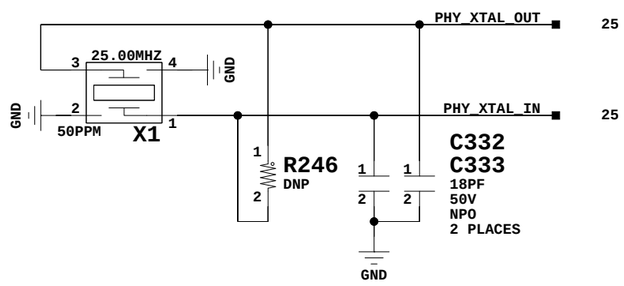


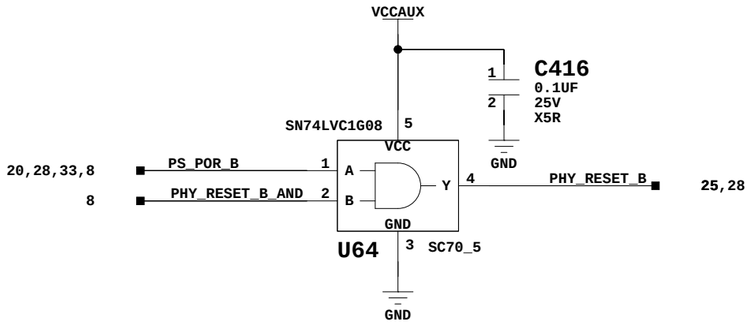
Clocks

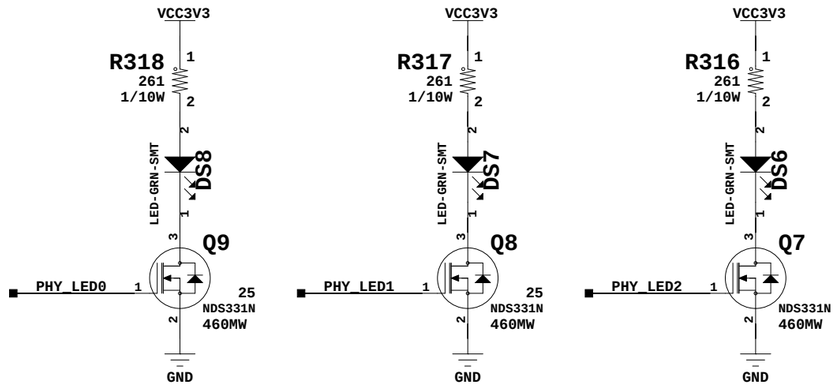
TRIPLE CROWN

Title: Clocks			
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	24 of 35	Drawn By	TG









SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

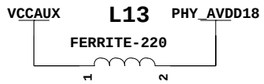
TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESITORS ON HSDAC_P AND HSDAC_N.

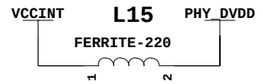
GEM / MDIO

TRIPLE CROWN

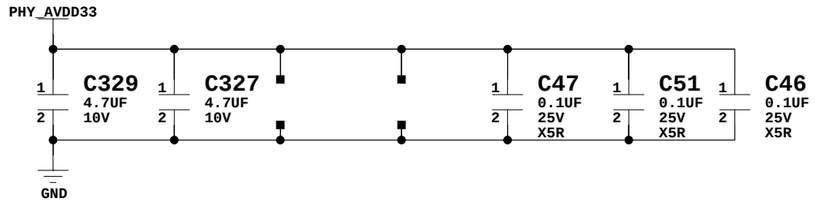
Title:	GEM / MDIO		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	25 of 35	Drawn By	TG

GEM / MDIO - POWER & DECOUPLING

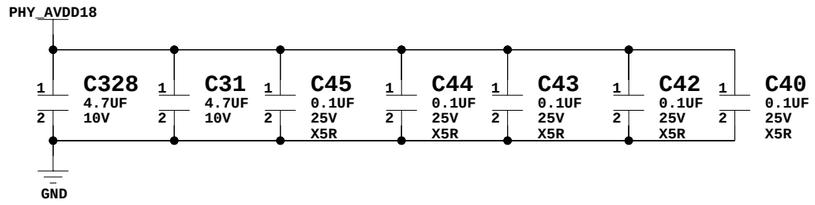




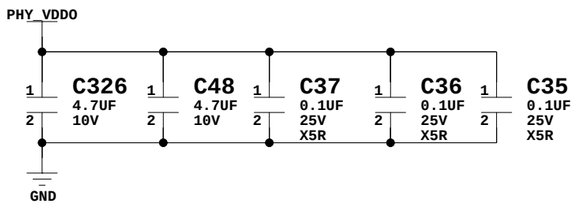
AVDD33



AVDD18



VDDO



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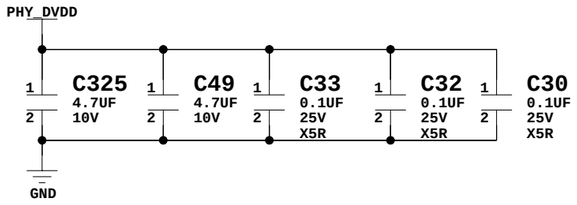

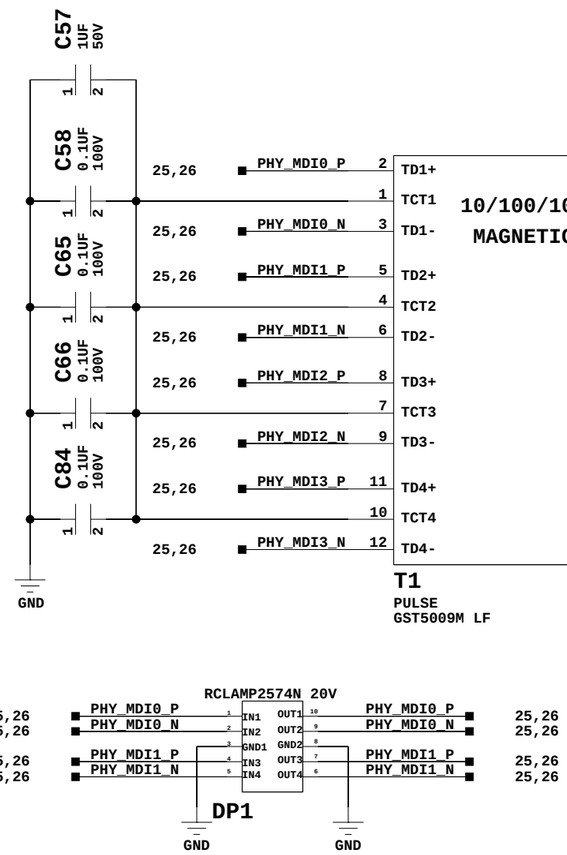

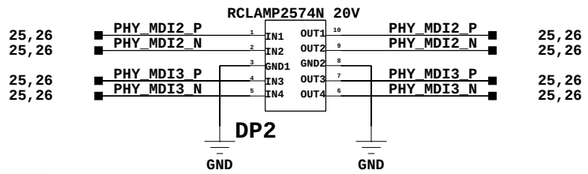

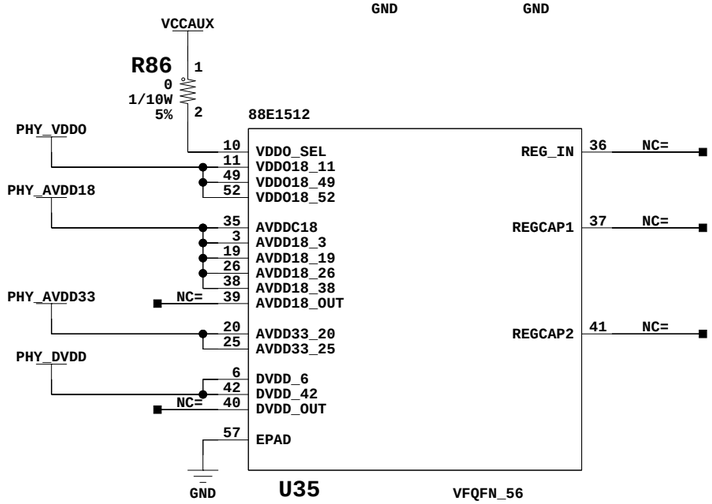

Chassis GND Accessible on PCB?

GEM / MDIO

TRIPLE CROWN

Title: GEM / MDIO			
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
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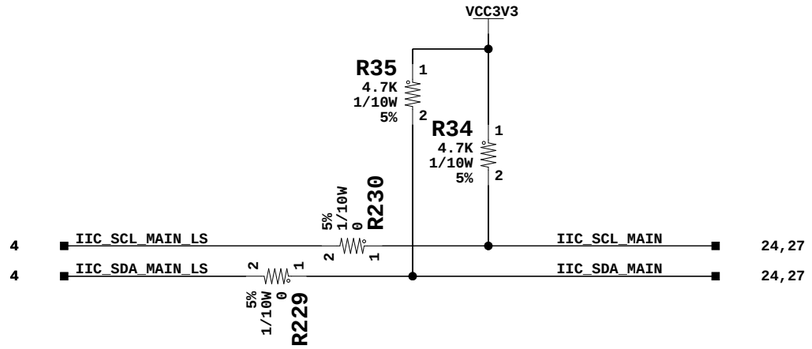

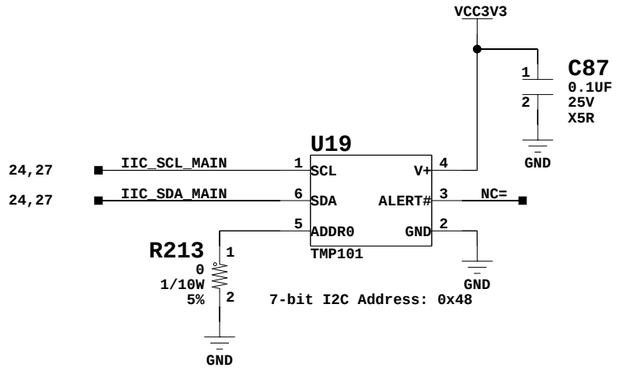

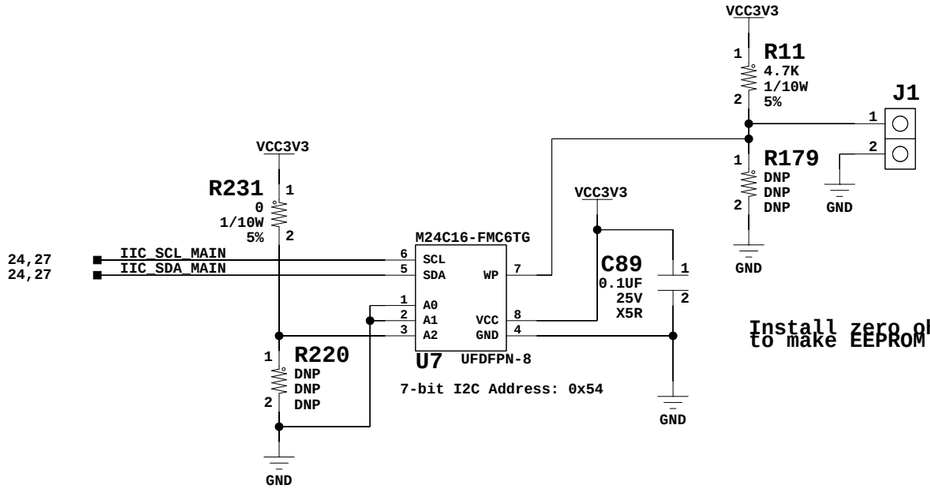

Install zero ohm resistor at location R179
to make EEPROM permanently writable

EEPROM, TEMPERATURE SENSOR

TRIPLE CROWN

Title: EEPROM, TEMPERATURE SENSOR			
Date:	10/11/2024:01:10	Ver:	1.1
Sheet Size: B		Rev:	02
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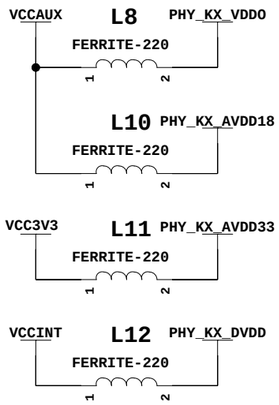
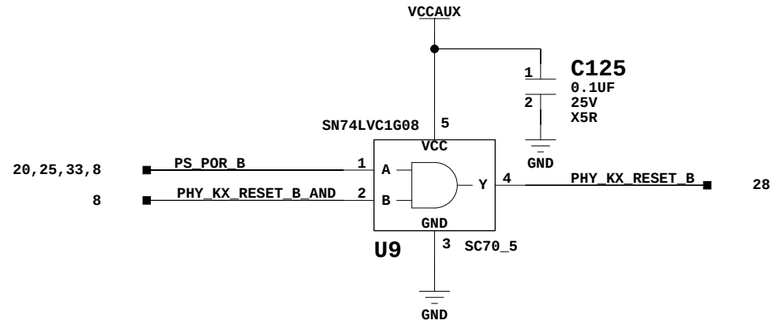
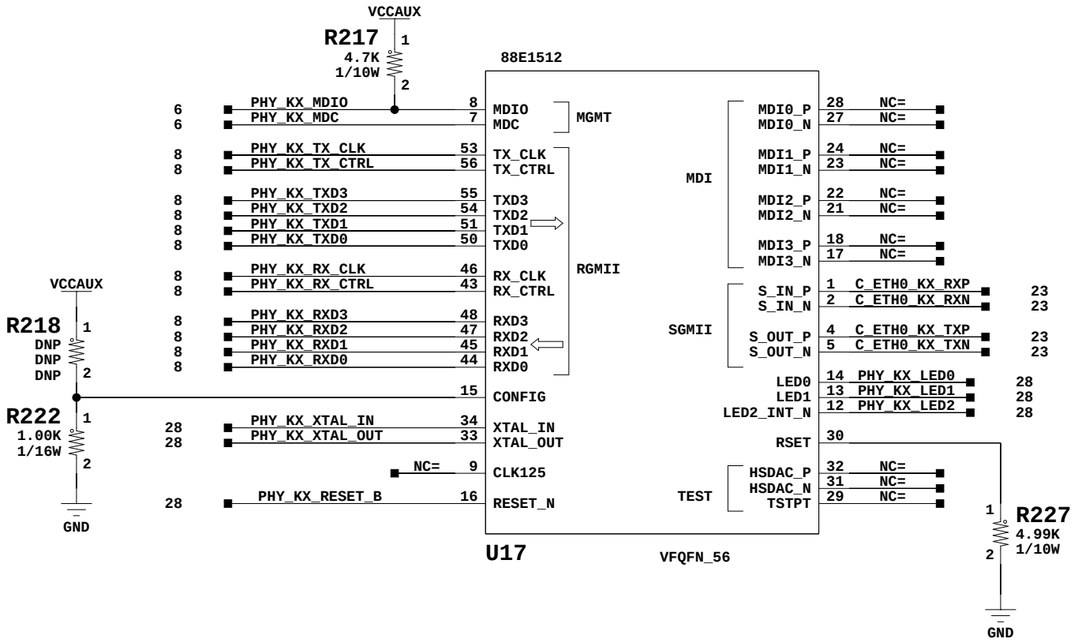
POWER & DECOUPLING

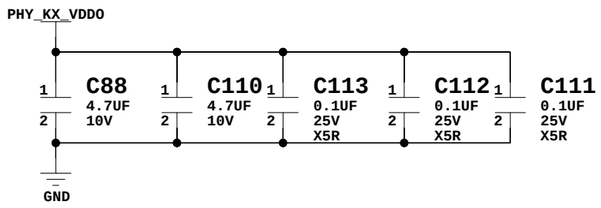




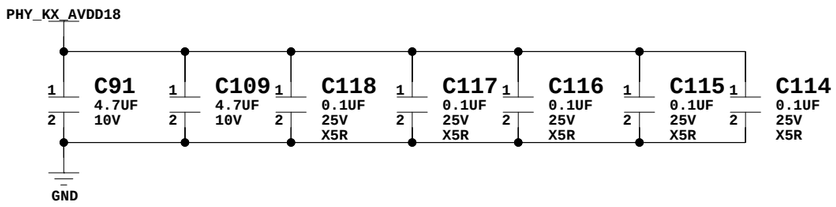
ADD SEPARATE FPGA RESET CONTROL?



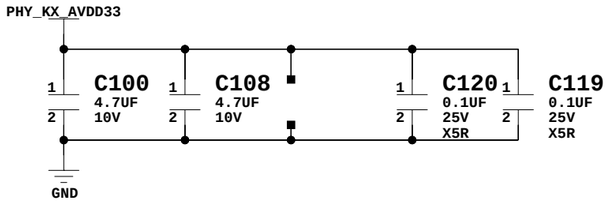
VDDO



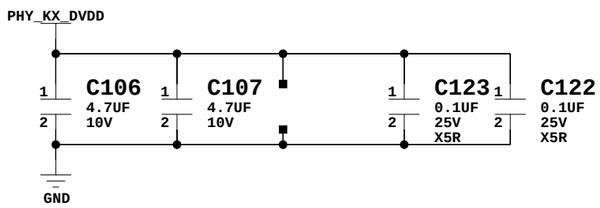
AVDD18

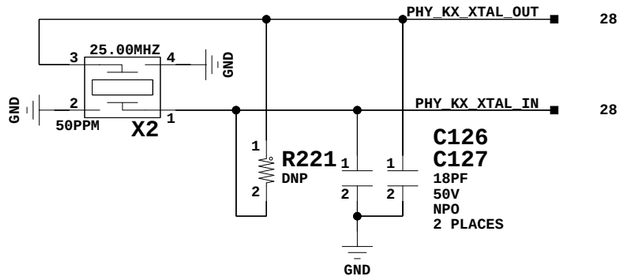


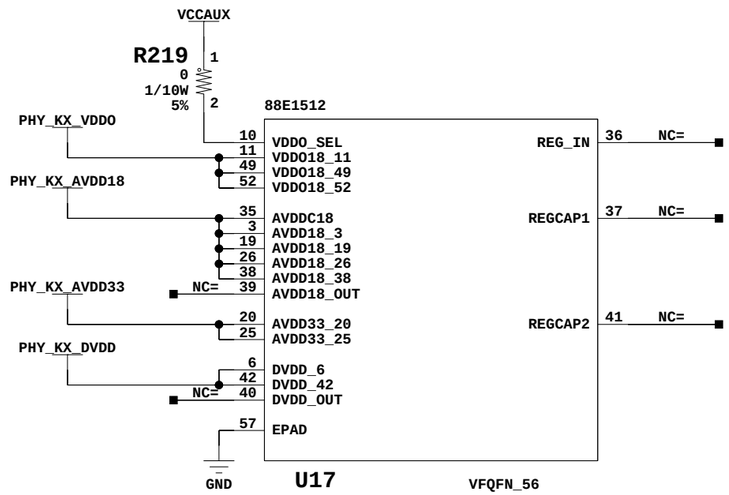
AVDD33

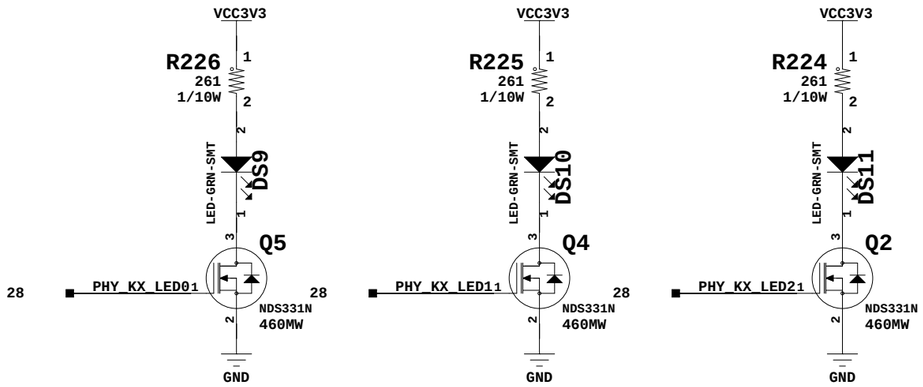


DVDD





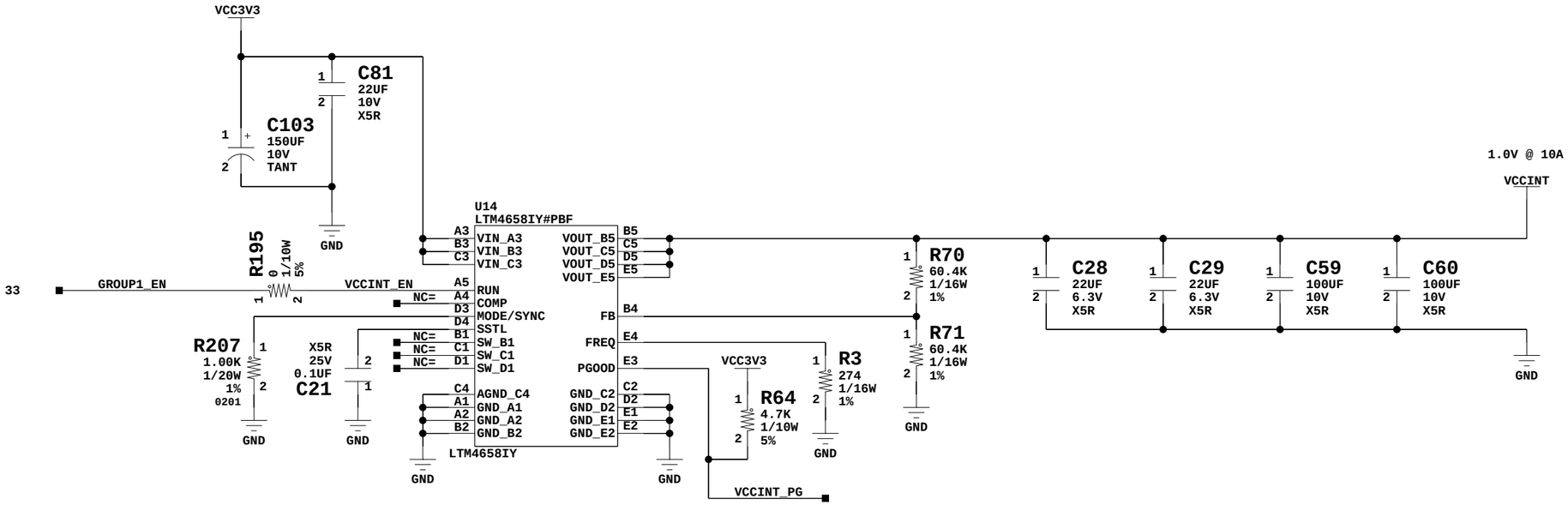




1000BASE-KX Ethernet

TRIPLE CROWN

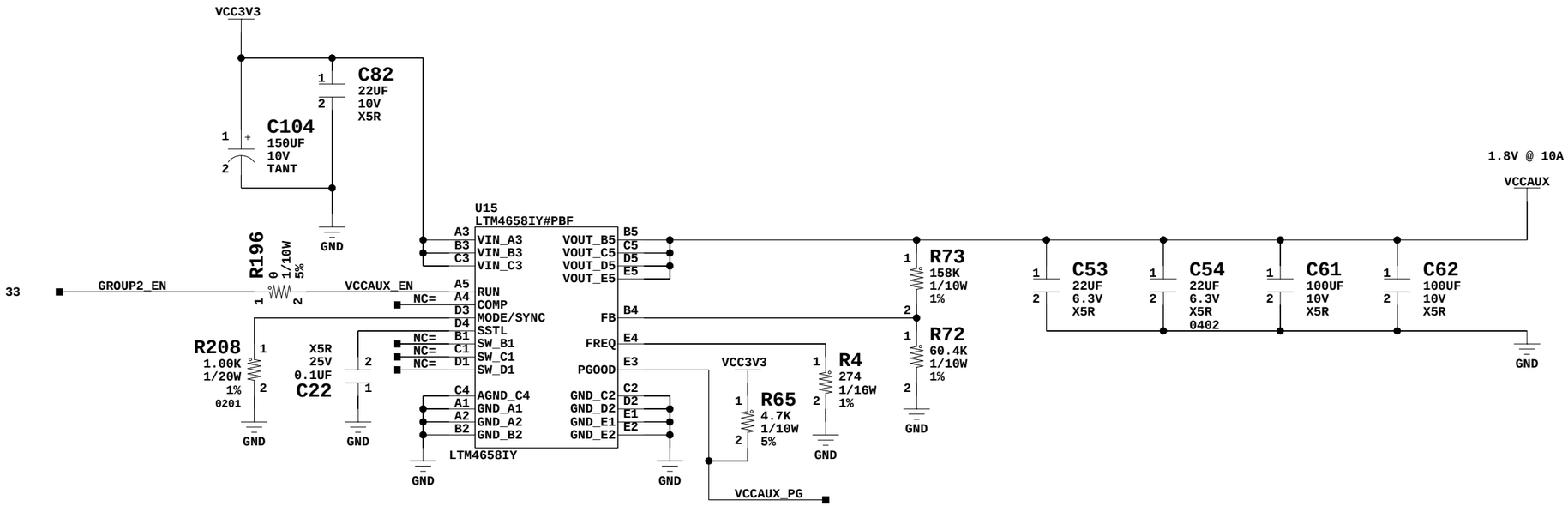
Title:	1000BASE-KX Ethernet		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	28 of 35	Drawn By	TG



1.0V 10A Power Regulator

TRIPLE CROWN

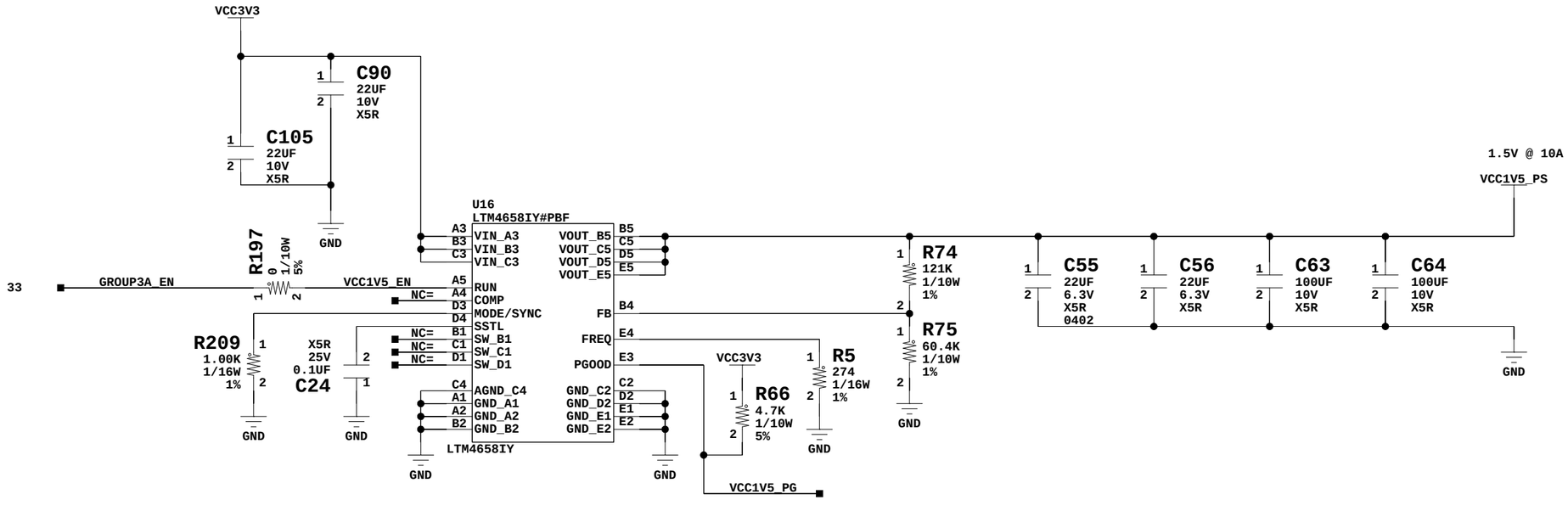
Title:	1.0V 10A Power Regulator		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	29 of 35	Drawn By	TG



1.8V 10A Power Regulator

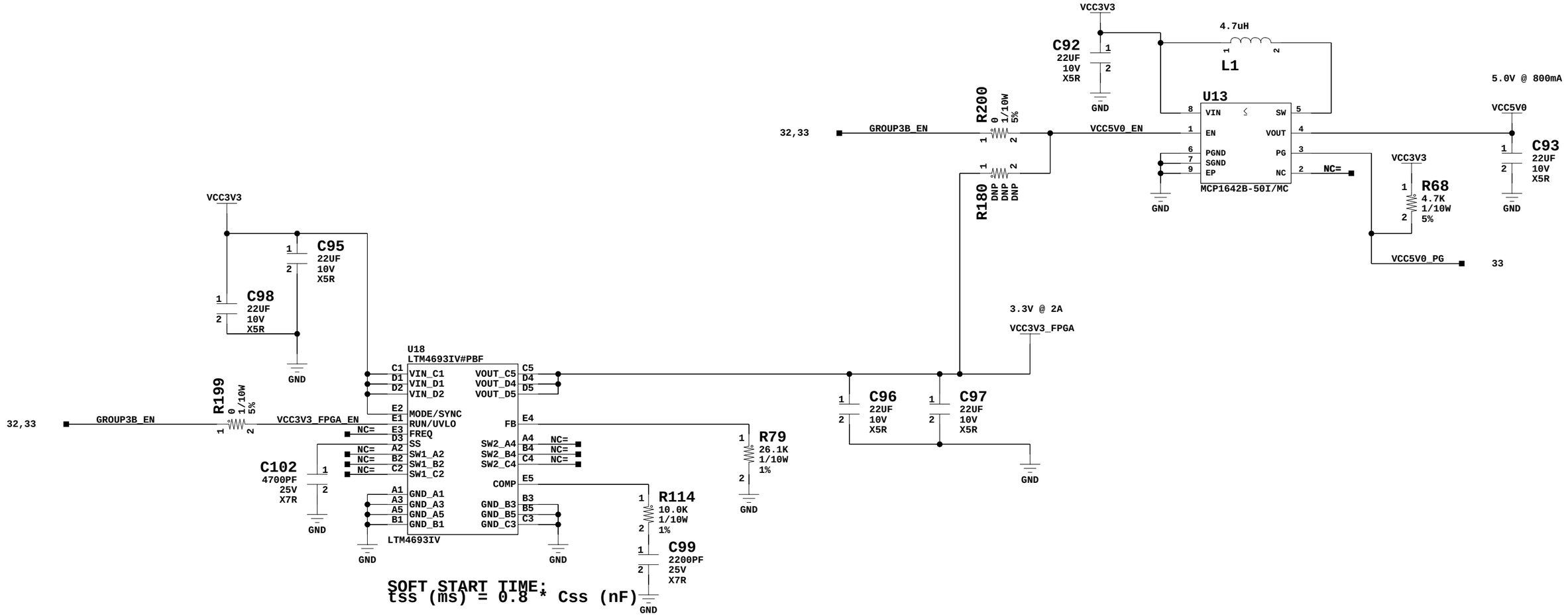
TRIPLE CROWN

Title:	1.8V 10A Power Regulator		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	30 of 35	Drawn By	TG



1.5V 10A Power Regulator

TRIPLE CROWN			
Title: 1.5V 10A Power Regulator			
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	31 of 35	Drawn By	TG



3.3V, 5V Power Regulators

TRIPLE CROWN

Title:	3.3V and 5V Power Regulators		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
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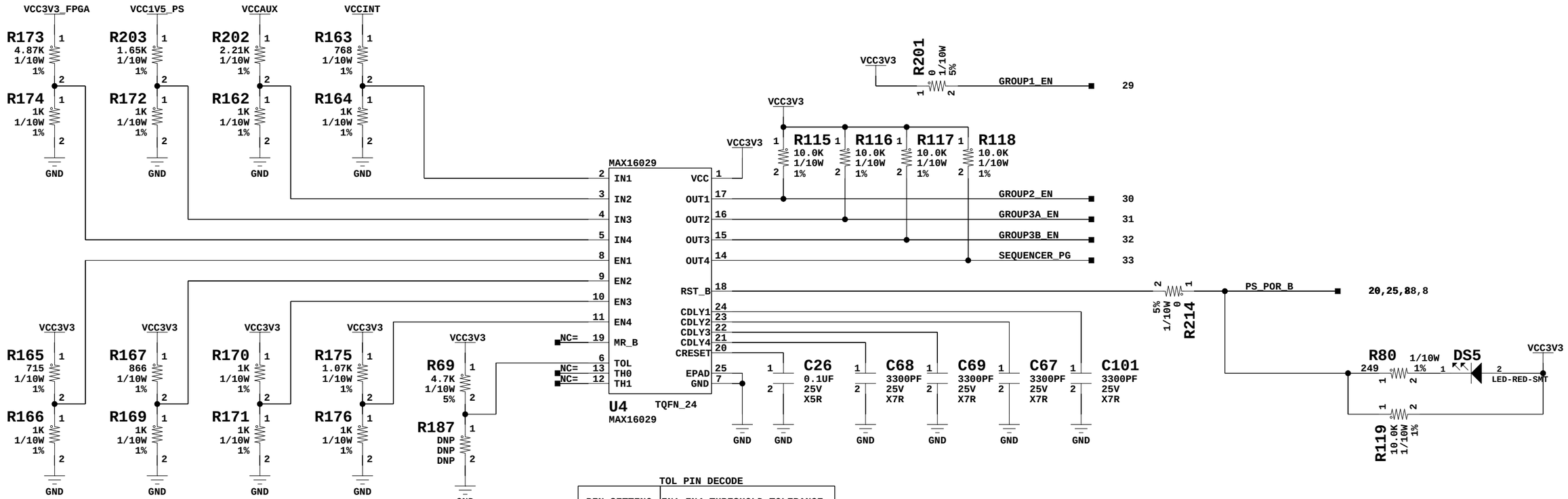
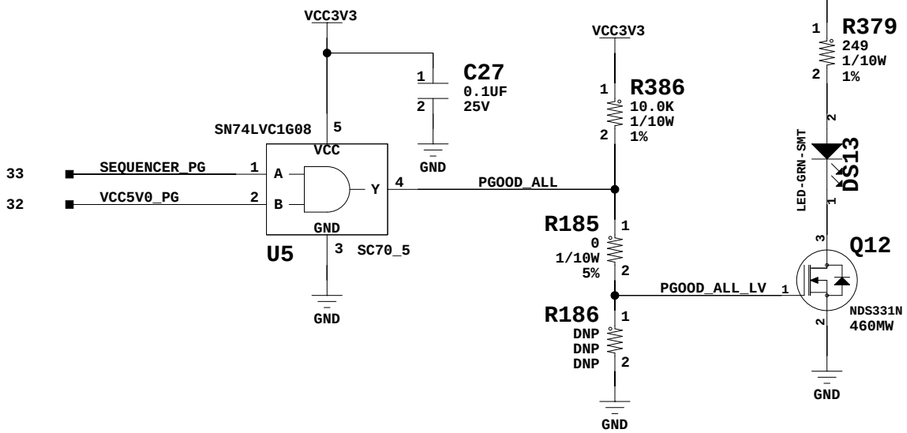
Power Sequence Order
1: VccINT (1.0v)
2: VccAUX (1.8v), VCCPLL (1.8V)
3: VCC1V5 (1.5V), VCC3.3V_FPGA (3.3V), VCC5V0 (5V)



TOL PIN DECODE	
PIN SETTING	IN1-IN4 THRESHOLD TOLERANCE
GND	5% BELOW NOMINAL
VCC	10% BELOW NOMINAL



OUT delay = 4,000,000 * CDLY + 35 * 10^-6 seconds
Note: CDLY in Farads

OUT delay calcuation:
CDLY = 2.7nF : OUT delay = 19ms
CDLY = 3.3nF : OUT delay = 13ms
CDLY = 2.2nF : OUT delay = 9ms
CDLY = 1.0nF : OUT delay = 4ms
CDLY = 0.24 nF : OUT delay = 1ms

OUT delay settings:
C101 = 3.3nF, OUT1 delay = 13ms
C67 = 3.3nF, OUT2 delay = 13ms
C69 = 3.3nF, OUT3 delay = 13ms
C68 = 3.3nF, OUT4 delay = 13ms

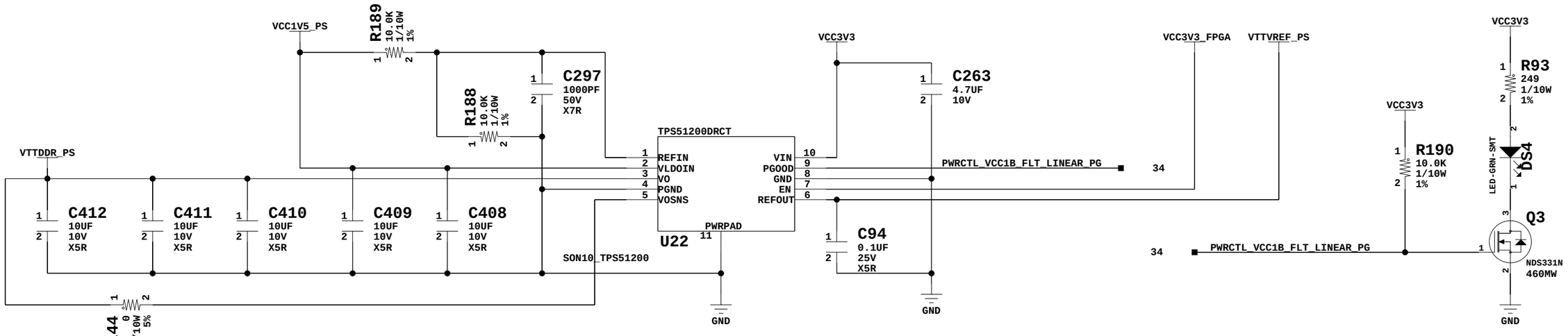
RST_B delay = 1,000,000 * CRESET + 35 * 10^-6 seconds
Note: CRESET in Farads

RST_B delay setting:
C26 = 0.1uF, RST_B delay = 100 ms

Power Sequencer

TRIPLE CROWN

Title:	Power Sequencer		
Date:	10/11/2024:01:10	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	33 of 35	Drawn By	TG



Place R144 close to DDR3 device that is farthest from TPS51200DRCT

Linear Power Supplies

TRIPLE CROWN

Title:	Linear Power Supplies		
Date:	10/11/2024:01:10	Ver:	1.0
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Update P/Ns for Mechanical Parts

MS01

STANDOFF_0P625

MN1

NUT_SS_4-40

MS1

MACHINE_SCREW_4-40

MH_136_250

MH4 — 1 — CHASSIS-2_GND

C34 (1–2): 0.01UF, 25V, X7R

GND

MS02

STANDOFF_0P625

MN2

NUT_SS_4-40

MS2

MACHINE_SCREW_4-40

MH_136_250

MH3 — 1 — CHASSIS-1_GND

C38 (1–2): 0.01UF, 25V, X7R

GND

MS03

STANDOFF_0P625

MN3

NUT_SS_4-40

MS3

MACHINE_SCREW_4-40

MH_136_250

MH2 — 1 — CHASSIS-1_GND

C39 (1–2): 0.01UF, 25V, X7R

GND

MS04

STANDOFF_0P625

MN4

NUT_SS_4-40

MS4

MACHINE_SCREW_4-40

MH_136_250

MH1 — 1 — CHASSIS-1_GND

C41 (1–2): 0.01UF, 25V, X7R

GND

MS05

STANDOFF_0P625

MN5

NUT_SS_4-40

MS5

MACHINE_SCREW_4-40

MH_136_250

MH8 — 1 — CHASSIS-2_GND

C50 (1–2): 0.01UF, 25V, X7R

GND

MS06

STANDOFF_0P625

MN6

NUT_SS_4-40

MS6

MACHINE_SCREW_4-40

MH_136_250

MH7 — 1 — CHASSIS-2_GND

C52 (1–2): 0.01UF, 25V, X7R

GND

MS07

STANDOFF_0P625

MN7

NUT_SS_4-40

MS12

MACHINE_SCREW_4-40

MH_136_250

MH6 — 1 — CHASSIS-1_GND

C121 (1–2): 0.01UF, 25V, X7R

GND

MS08

STANDOFF_0P625

MN8

NUT_SS_4-40

MS13

MACHINE_SCREW_4-40

MH_136_250

MH5 — 1 — CHASSIS-2_GND

C124 (1–2): 0.01UF, 25V, X7R

GND

Mechanical Components

TRIPLE CROWN

Title: Mechanical Components

Date: 10/11/2024:01:11	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 35 of 35	Drawn By TG