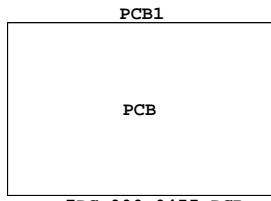
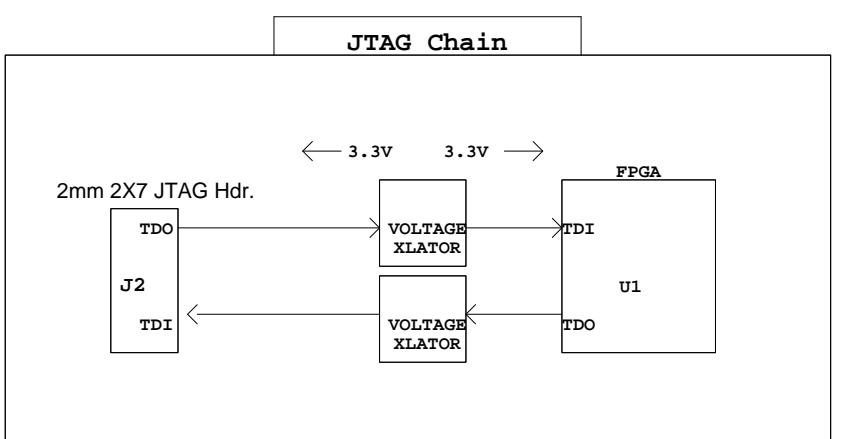
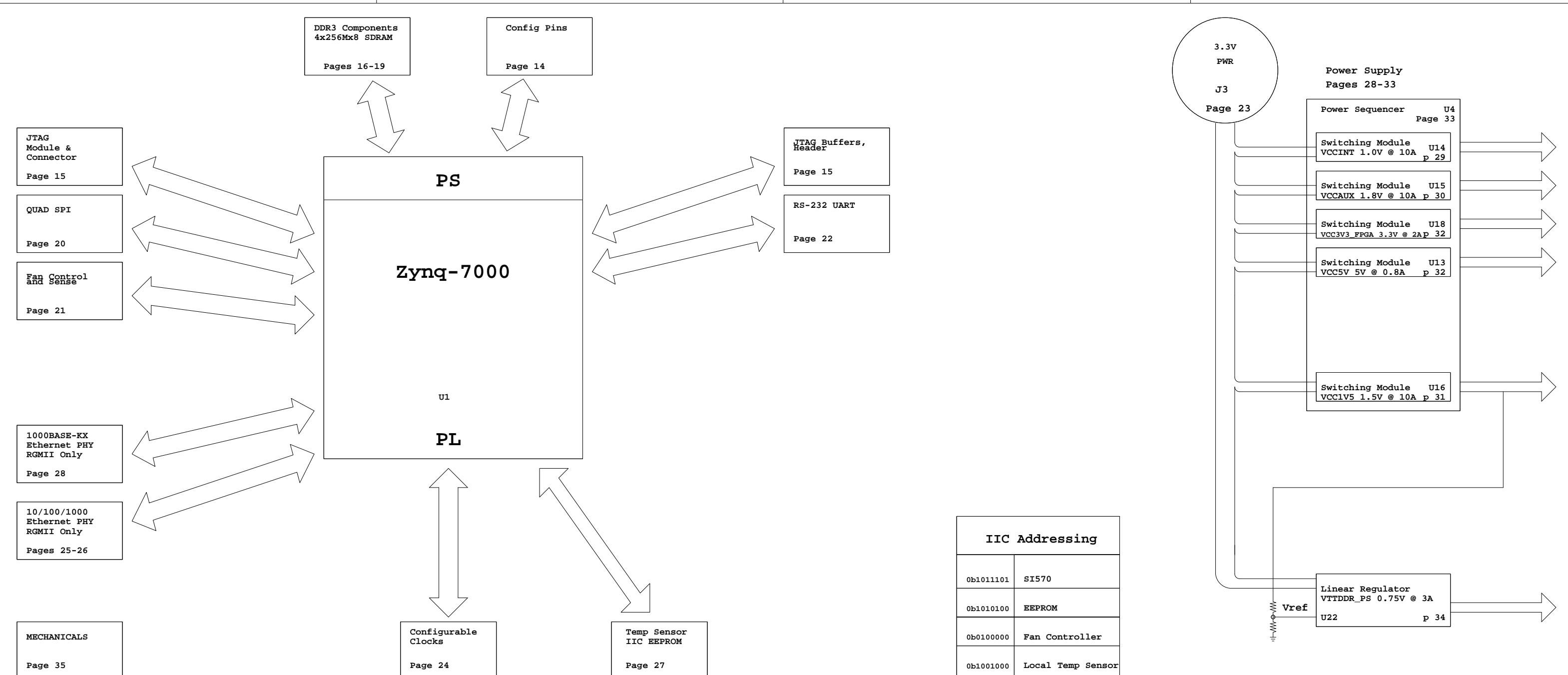


LCR CHASSIS MANAGER



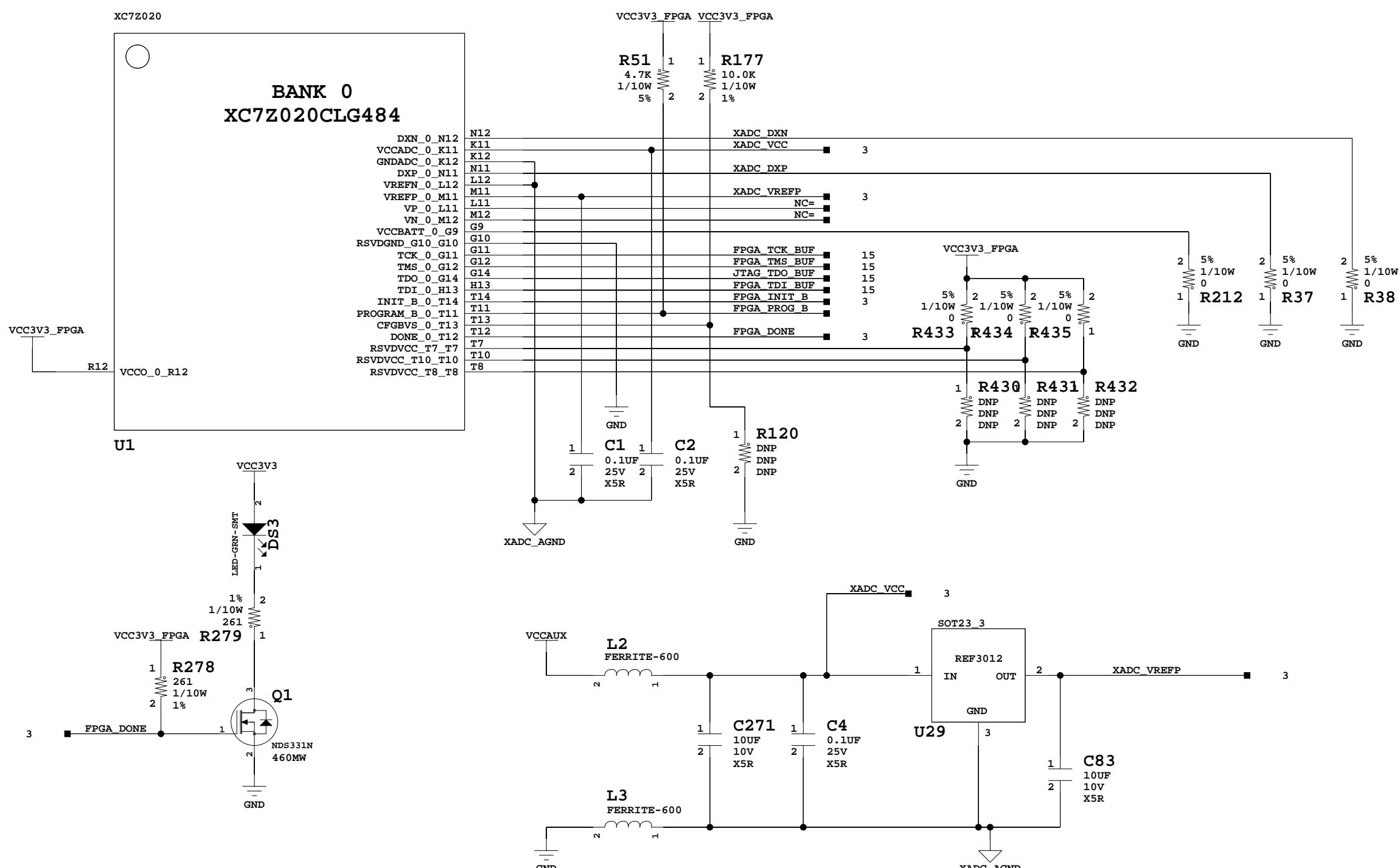
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Date:	02/07/2024:22:15	Ver: 1.0
Sheet Size:	B	Rev: 01
Sheet	1 of 35	Drawn By TG

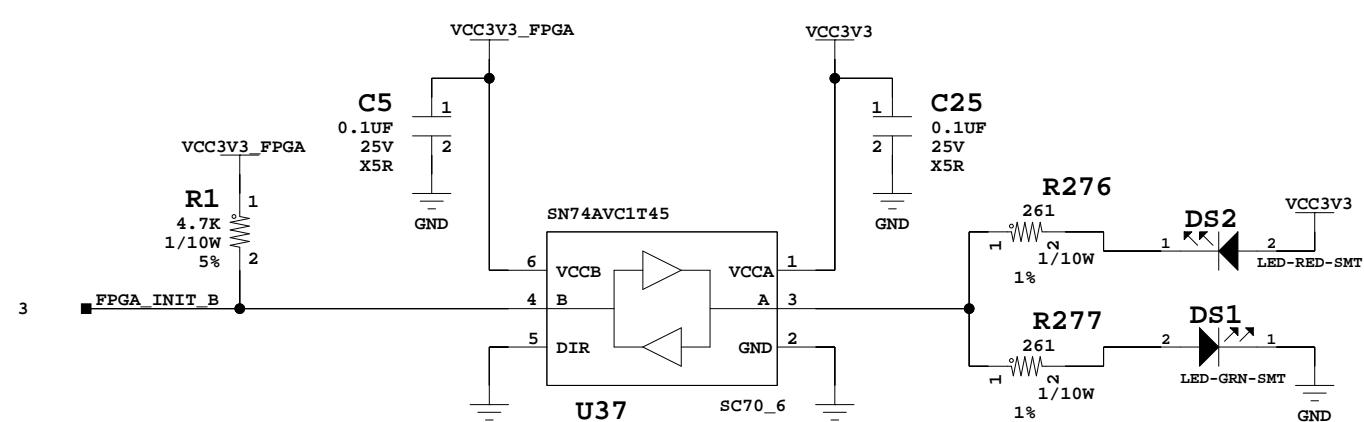


TRIPLE CROWN

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Date:	02/07/2024:22:15
Sheet Size:	B
Sheet	2 of 35 Drawn By TG



XADC Reference



Zynq Bank 0

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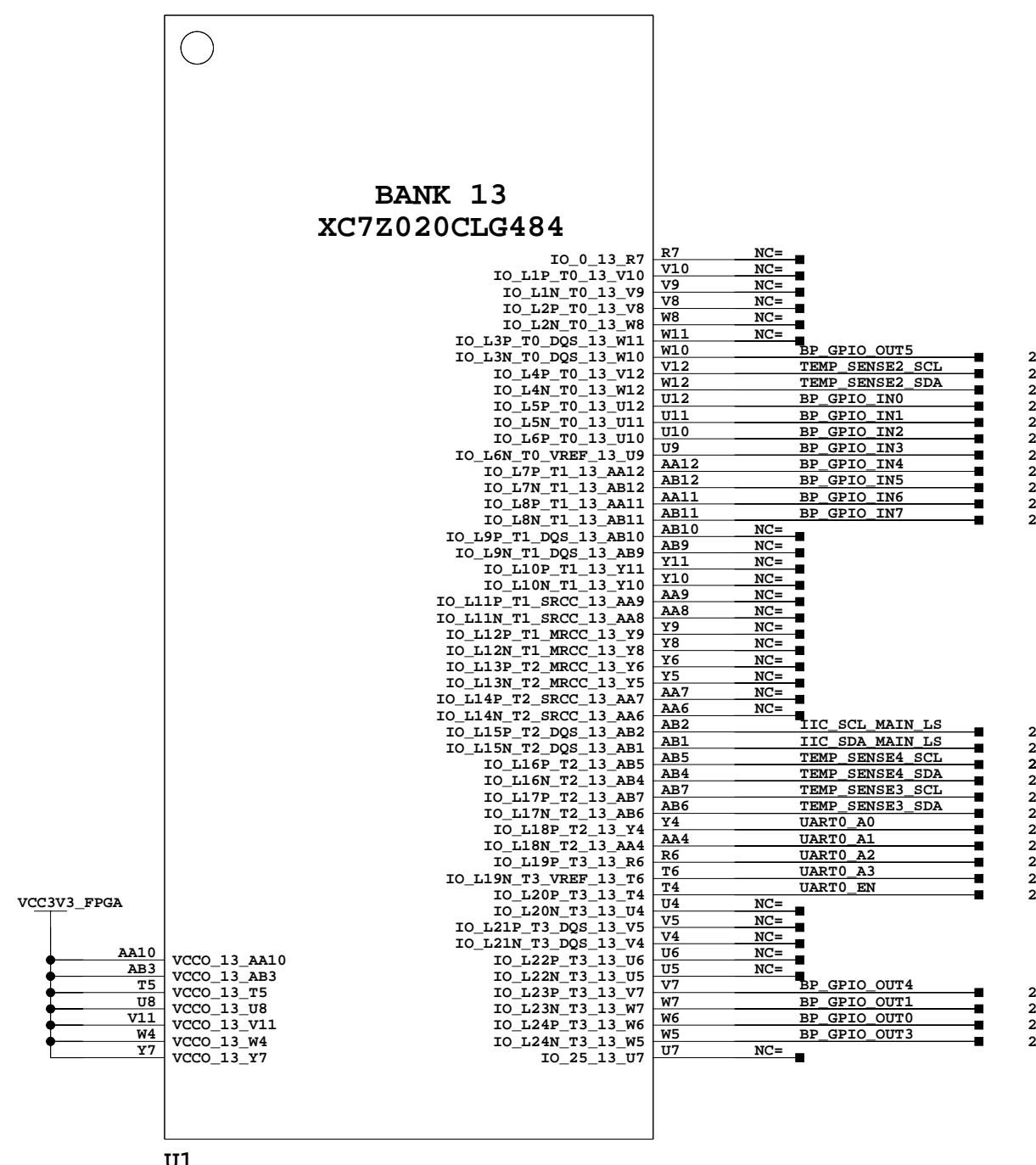
Rev: 01

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**Zynq Bank 13****TRIPLE CROWN**

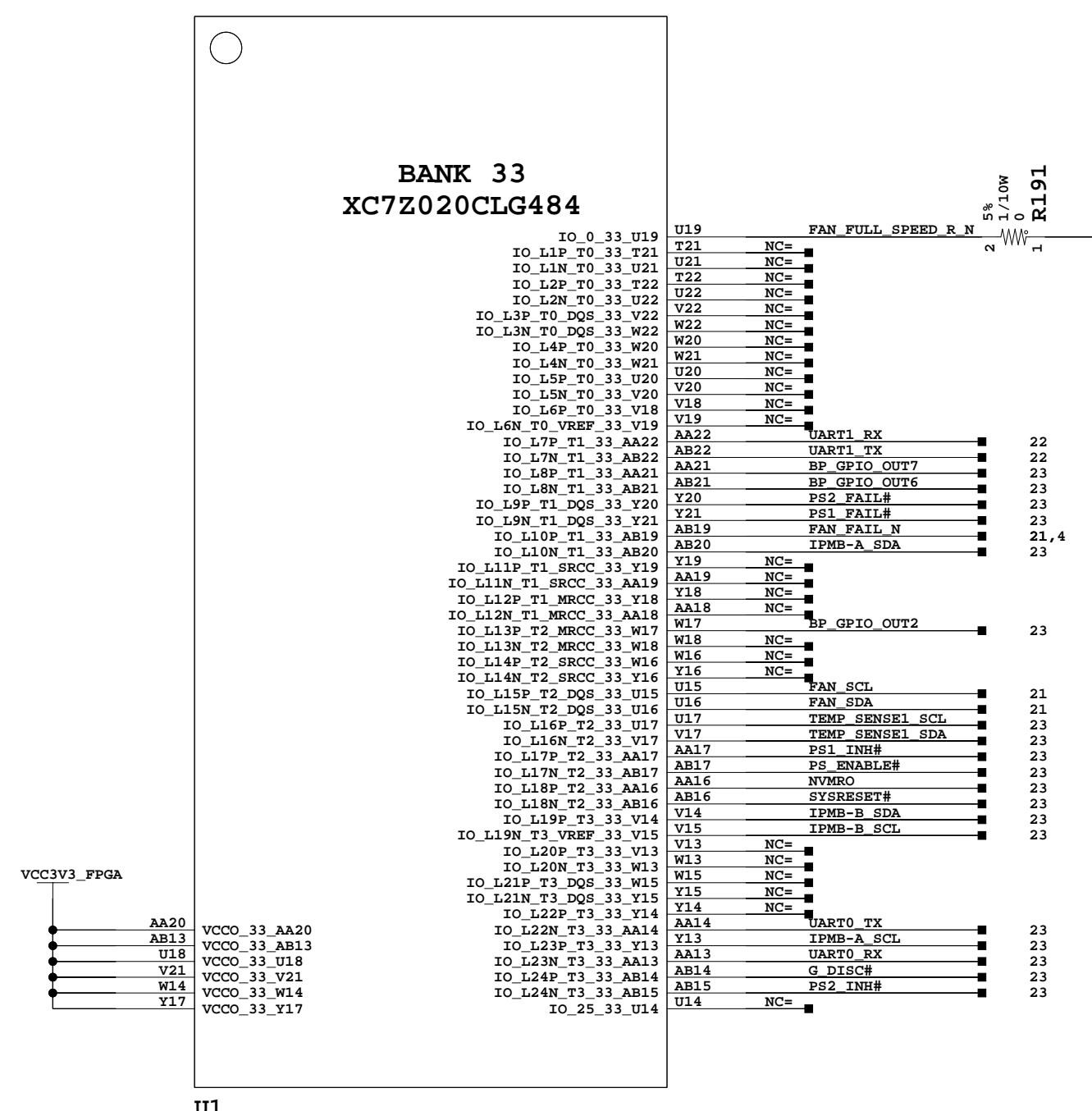
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Date: 02/07/2024:22:15 Ver: 1.0

Sheet Size: B Rev: 01

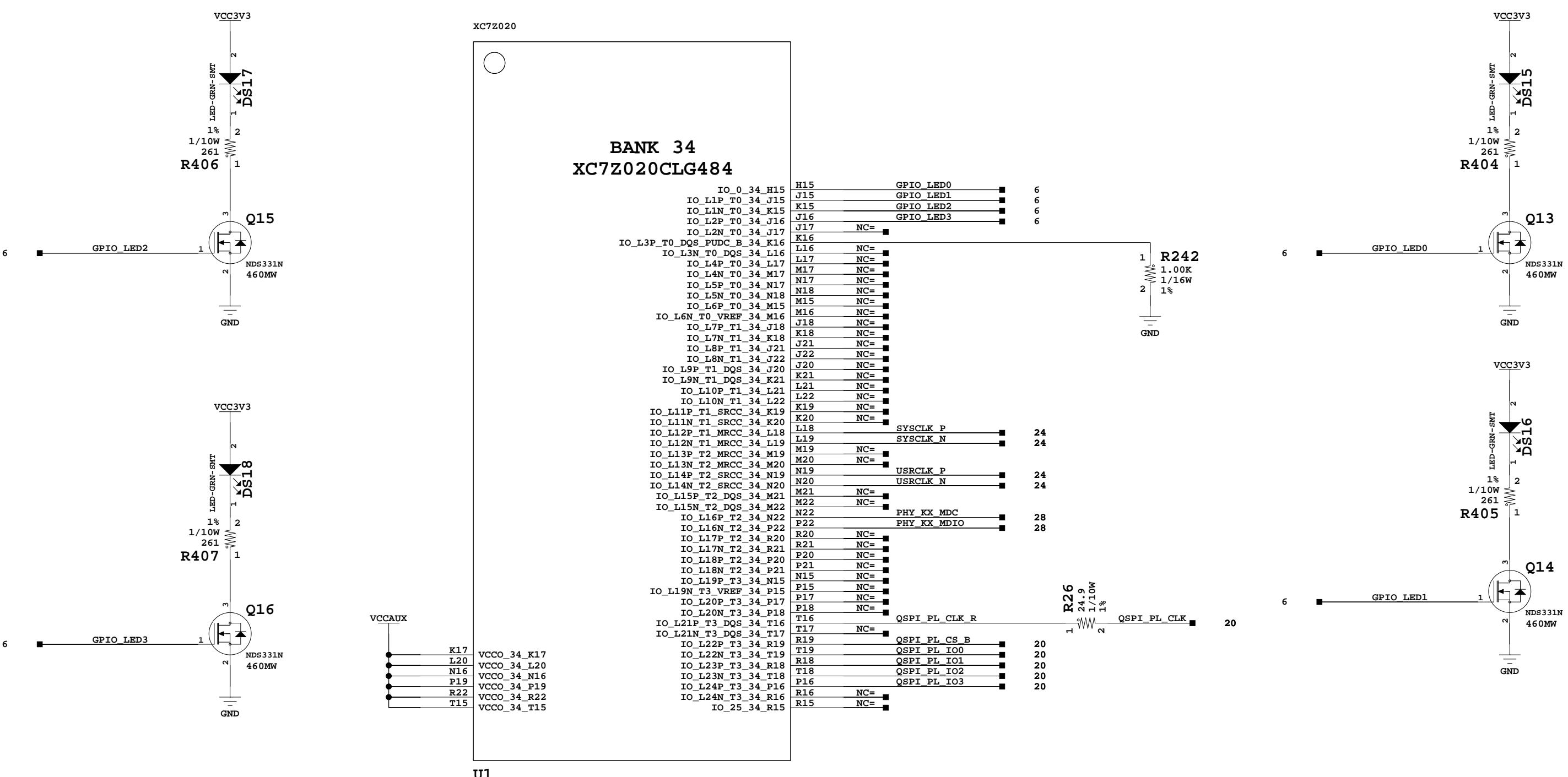
Sheet 4 of 35 Drawn By TG

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**Zynq Bank 33****TRIPLE CROWN**

Title: Zynq Bank 33

Date:	02/07/2024:22:15	Ver:	1.0
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Zynq Bank 34

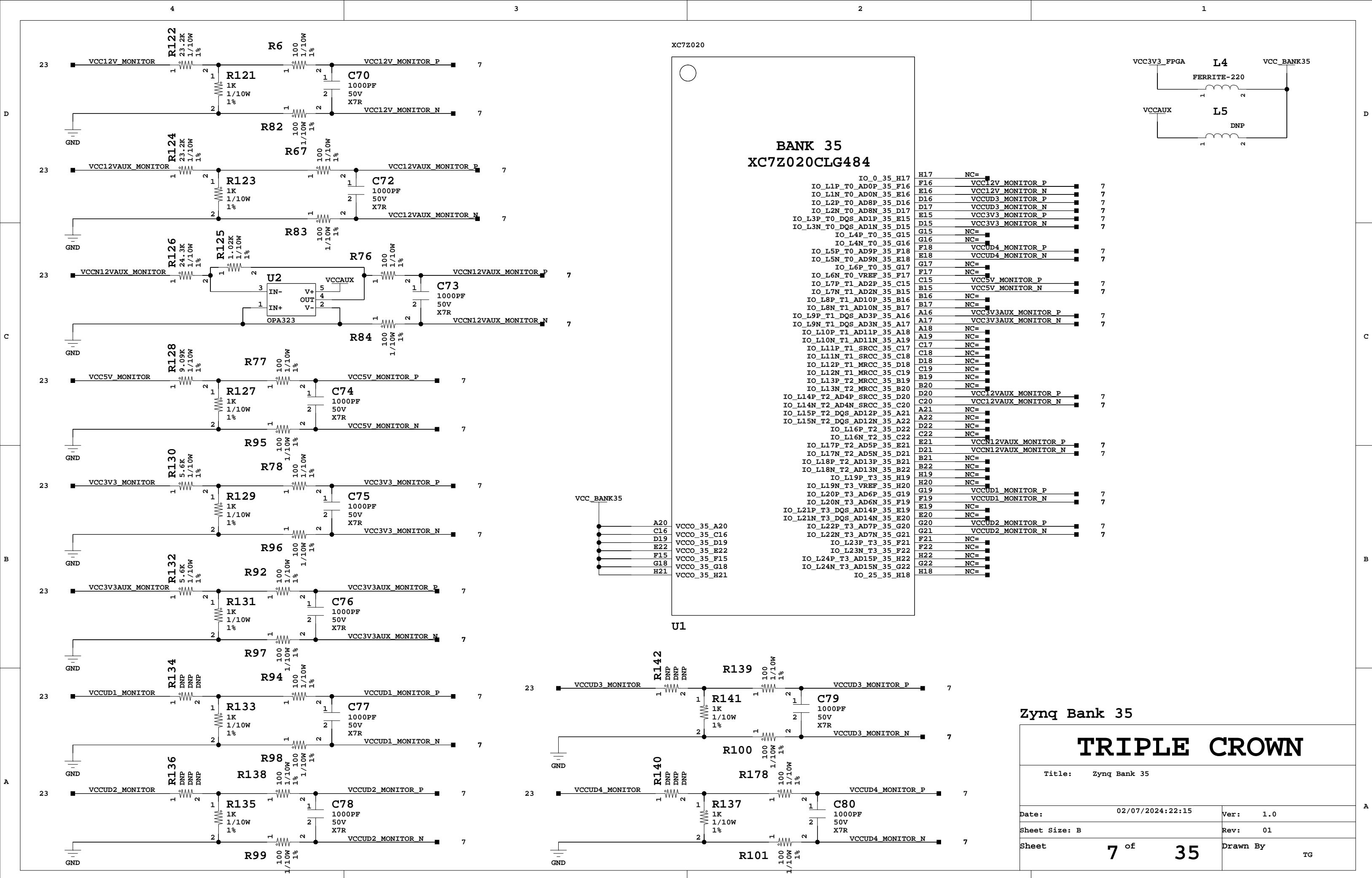
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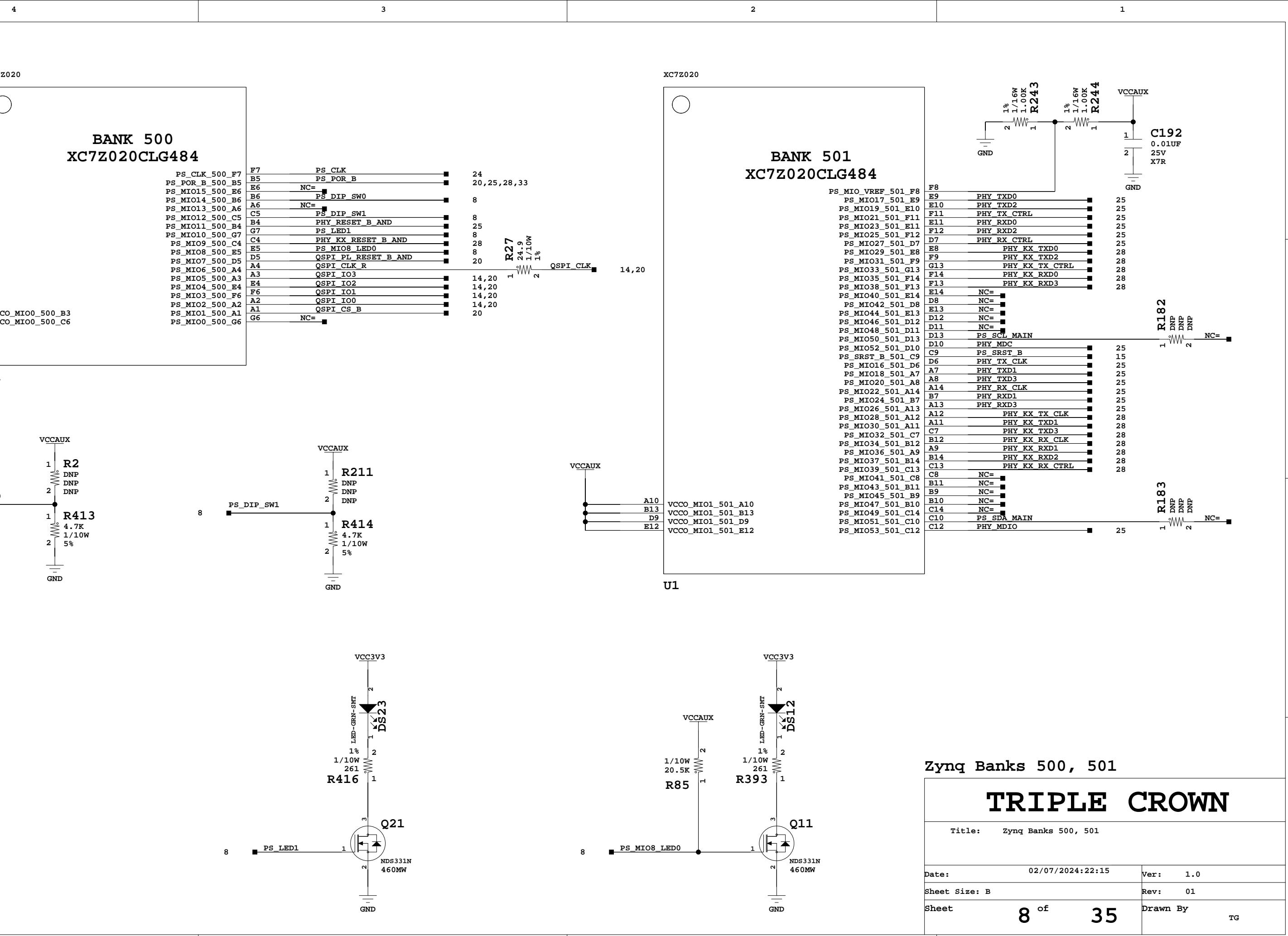
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Date: 02/07/2024:22:15 Ver: 1.0

Sheet Size: B Rev: 01

Sheet 6 of 35 Drawn By TG





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BANK 502

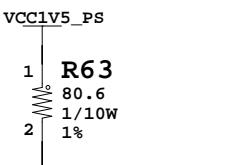
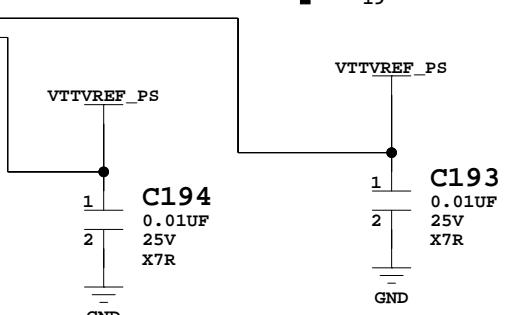
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PS_DDR_DRST_B_502_F3	F3	PS_DDR3_RESET_B	16,17,18,19
PS_DDR_DQ0_502_D1	D1	PS_DDR3_DQ3	16
PS_DDR_DQ1_502_C3	C3	PS_DDR3_DQ1	16
PS_DDR_DQ2_502_B2	B2	PS_DDR3_DQ6	16
PS_DDR_DQ3_502_D3	D3	PS_DDR3_DQ7	16
PS_DDR_DM0_502_B1	B1	PS_DDR3_DM0	16
PS_DDR_DQS_P0_502_C2	C2	PS_DDR3_DQS0_P	16
PS_DDR_DQS_N0_502_D2	D2	PS_DDR3_DQS0_N	16
PS_DDR_DQ4_502_E3	E3	PS_DDR3_DQ0	16
PS_DDR_DQ5_502_E1	E1	PS_DDR3_DQ5	16
PS_DDR_DQ6_502_F2	F2	PS_DDR3_DQ2	16
PS_DDR_DQ7_502_F1	F1	PS_DDR3_DQ4	16
PS_DDR_DQ8_502_G2	G2	PS_DDR3_DQ8	17
PS_DDR_DQ9_502_G1	G1	PS_DDR3_DQ10	17
PS_DDR_DQ10_502_L1	L1	PS_DDR3_DQ9	17
PS_DDR_DQ11_502_L2	L2	PS_DDR3_DQ13	17
PS_DDR_DM1_502_H3	H3	PS_DDR3_DM1	17
PS_DDR_DQS_P1_502_H2	H2	PS_DDR3_DQS1_P	17
PS_DDR_DQS_N1_502_J2	J2	PS_DDR3_DQS1_N	17
PS_DDR_DQ12_502_L3	L3	PS_DDR3_DQ12	17
PS_DDR_DQ13_502_K1	K1	PS_DDR3_DQ11	17
PS_DDR_DQ14_502_J1	J1	PS_DDR3_DQ14	17
PS_DDR_DQ15_502_K3	K3	PS_DDR3_DQ15	17
PS_DDR_A14_502_G4	G4	PS_DDR3_A14	
PS_DDR_A13_502_F4	F4	PS_DDR3_A13	16,17,18,19
PS_DDR_A12_502_H4	H4	PS_DDR3_A12	16,17,18,19
PS_DDR_A11_502_G5	G5	PS_DDR3_A11	16,17,18,19
PS_DDR_A10_502_J3	J3	PS_DDR3_A10	16,17,18,19
PS_DDR_A9_502_H5	H5	PS_DDR3_A9	16,17,18,19
PS_DDR_A8_502_J5	J5	PS_DDR3_A8	16,17,18,19
PS_DDR_A7_502_J6	J6	PS_DDR3_A7	16,17,18,19
PS_DDR_A6_502_J7	J7	PS_DDR3_A6	16,17,18,19
PS_DDR_A5_502_K5	K5	PS_DDR3_A5	16,17,18,19
PS_DDR_A4_502_K6	K6	PS_DDR3_A4	16,17,18,19
PS_DDR_A3_502_L4	L4	PS_DDR3_A3	16,17,18,19
PS_DDR_VRN_502_M7	M7	PS_VRN	9
PS_DDR_VRP_502_N7	N7	PS_VRP	9
PS_DDR_CKF_502_N4	N4	PS_DDR3_CLK_P	16,17,18,19
PS_DDR_CKN_502_N5	N5	PS_DDR3_CLK_N	16,17,18,19
PS_DDR_A2_502_K4	K4	PS_DDR3_A2	16,17,18,19
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PS_DDR_A0_502_M4	M4	PS_DDR3_A0	16,17,18,19
PS_DDR_BA2_502_M6	M6	PS_DDR3_BA2	16,17,18,19
PS_DDR_BA1_502_L6	L6	PS_DDR3_BA1	16,17,18,19
PS_DDR_BA0_502_L7	L7	PS_DDR3_BA0	16,17,18,19
PS_DDR_ODT_502_P5	P5	PS_DDR3_ODT	16,17,18,19
PS_DDR_CS_B_502_P6	P6	PS_DDR3_CS_B	16,17,18,19
PS_DDR_CKE_502_V3	V3	PS_DDR3_CKE	16,17,18,19
PS_DDR_WE_B_502_R4	R4	PS_DDR3_WE_B	16,17,18,19
PS_DDR_CAS_B_502_P3	P3	PS_DDR3_CAS_B	16,17,18,19
PS_DDR_RAS_B_502_R5	R5	PS_DDR3_RAS_B	16,17,18,19
PS_DDR_DQ16_502_M1	M1	PS_DDR3_DQ16	18
PS_DDR_DQ17_502_T3	T3	PS_DDR3_DQ17	18
PS_DDR_DQ18_502_N3	N3	PS_DDR3_DQ18	18
PS_DDR_DQ19_502_T1	T1	PS_DDR3_DQ19	18
PS_DDR_DM2_502_P1	P1	PS_DDR3_DM2	18
PS_DDR_DQS_P2_502_N2	N2	PS_DDR3_DQS2_P	18
PS_DDR_DQS_N2_502_P2	P2	PS_DDR3_DQS2_N	18
PS_DDR_DQ20_502_R3	R3	PS_DDR3_DQ20	18
PS_DDR_DQ21_502_T2	T2	PS_DDR3_DQ21	18
PS_DDR_DQ22_502_M2	M2	PS_DDR3_DQ22	18
PS_DDR_DQ23_502_R1	R1	PS_DDR3_DQ23	18
PS_DDR_DQ24_502_AA3	AA3	PS_DDR3_DQ27	19
PS_DDR_DQ25_502_U1	U1	PS_DDR3_DQ24	19
PS_DDR_DQ26_502_AA1	AA1	PS_DDR3_DQ25	19
PS_DDR_DQ27_502_U2	U2	PS_DDR3_DQ26	19
PS_DDR_DM3_502_AA2	AA2	PS_DDR3_DM3	19
PS_DDR_DQ28_502_W1	V2	PS_DDR3_DQS3_P	19
PS_DDR_DQ29_502_Y3	W2	PS_DDR3_DQS3_N	19
PS_DDR_DQ30_502_W3	W1	PS_DDR3_DQ28	19
PS_DDR_DQ31_502_Y1	Y3	PS_DDR3_DQ29	19
PS_DDR_VREF_502_H7	W3	PS_DDR3_DQ30	19
PS_DDR_VREF1_502_P7	Y1	PS_DDR3_DQ31	19
	H7		
	P7		

VCC1V5_PS

E2 VCCO_DDR_502_E2
 F5 VCCO_DDR_502_F5
 H1 VCCO_DDR_502_H1
 J4 VCCO_DDR_502_J4
 K7 VCCO_DDR_502_K7
 M3 VCCO_DDR_502_M3
 N6 VCCO_DDR_502_N6
 R2 VCCO_DDR_502_R2
 V1 VCCO_DDR_502_V1

U1



Zynq Bank 502

TRIPLE CROWN

Title: Zynq Bank 502

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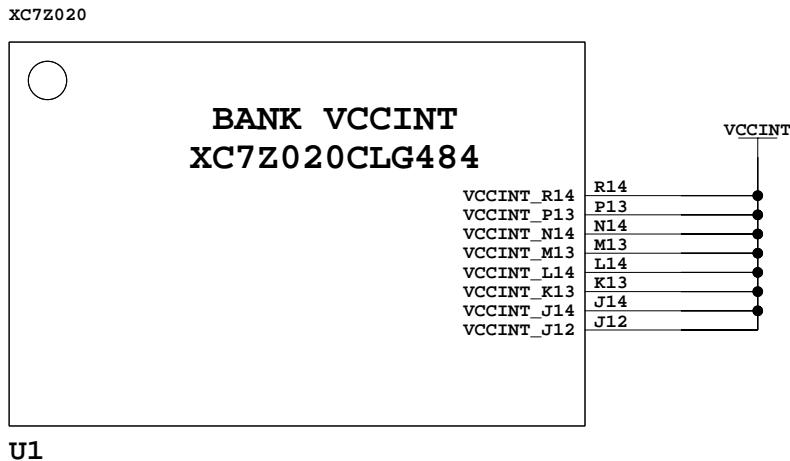
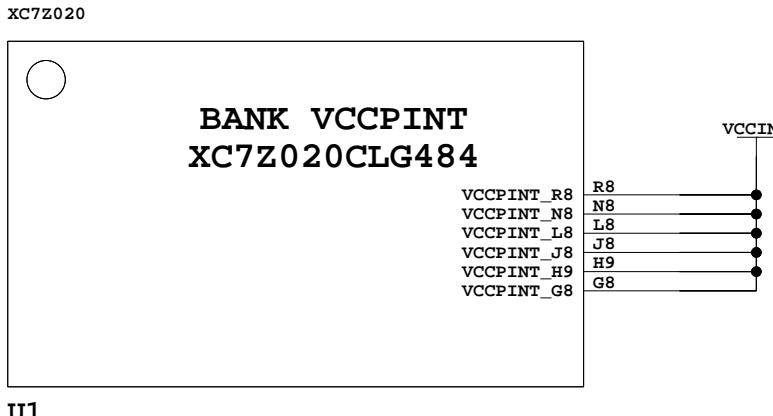
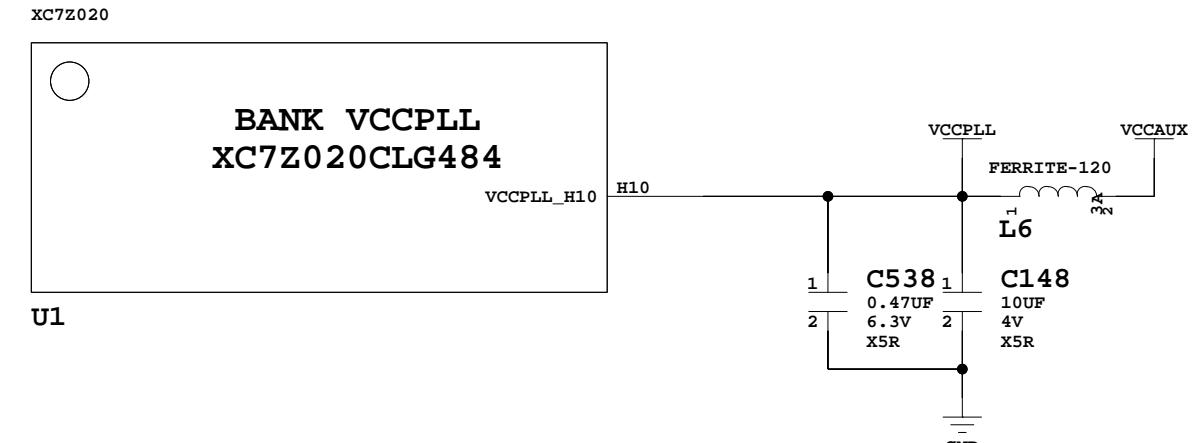
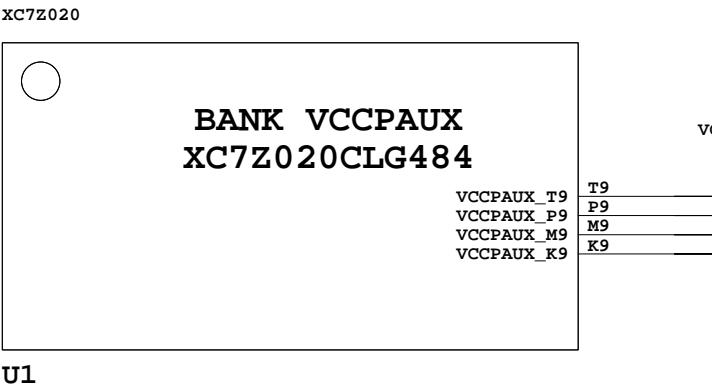
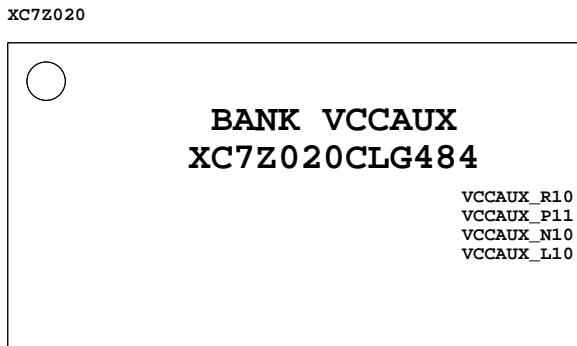
TG

Increase width of VCCPLL route to
as wide as possible (target is > 20 mils)

Reduce the length of VCCPLL route as much as possible

Place C538 inside the VIA field to provide
as short as possible connection to VCCPLL (H10) and GND

Place C539 inside the open space cross adjacent to H10
for the short possible connection to VCCPLL



Zynq Power Pins

TRIPLE CROWN

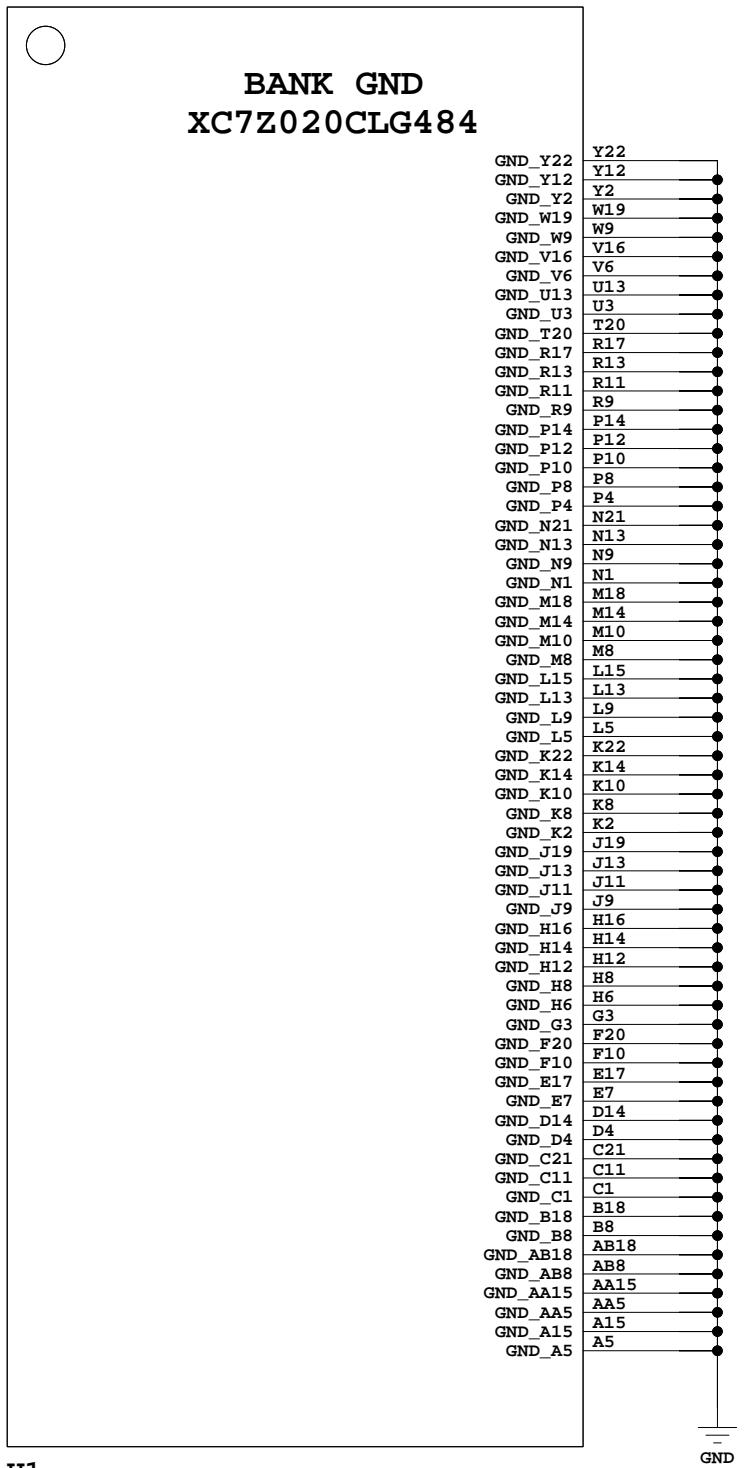
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Date: 02/07/2024:22:15 Ver: 1.0

Sheet Size: B Rev: 01

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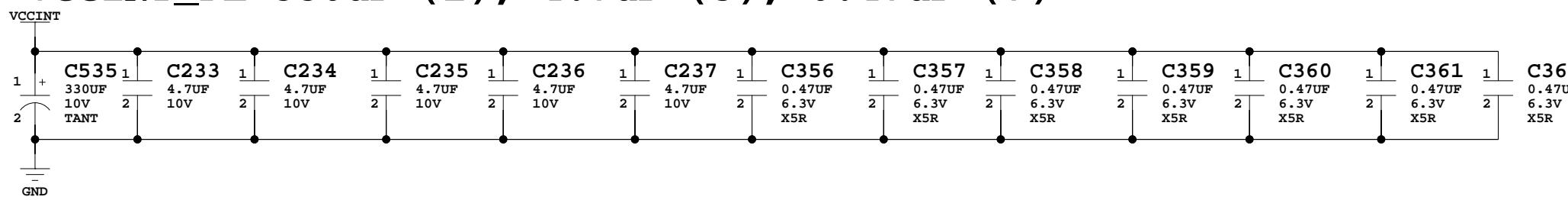
**Zynq GND****TRIPLE CROWN**

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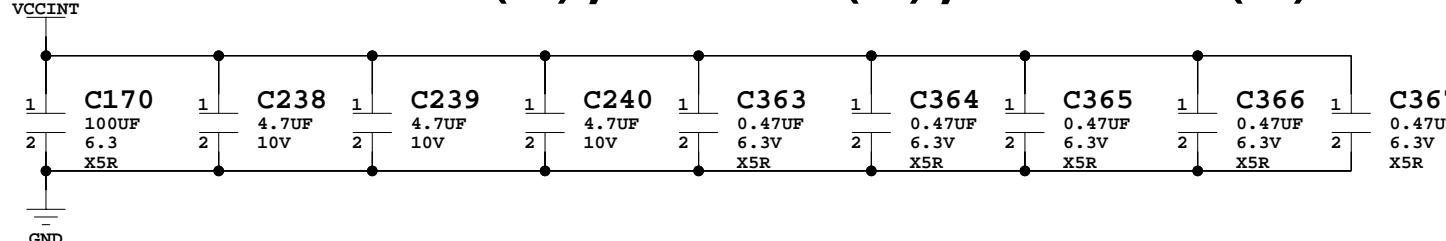
Date:	02/07/2024:22:15	Ver:	1.0
Sheet Size:	B	Rev:	
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BYPASS CAPACITORS

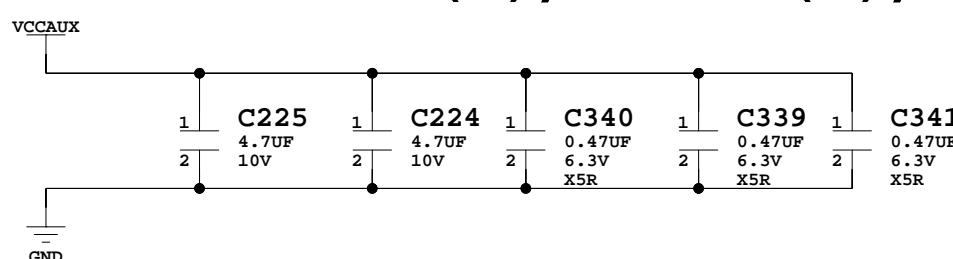
VCCINT_PL 330uF (1), 4.7uF (5), 0.47uF (7)



VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)

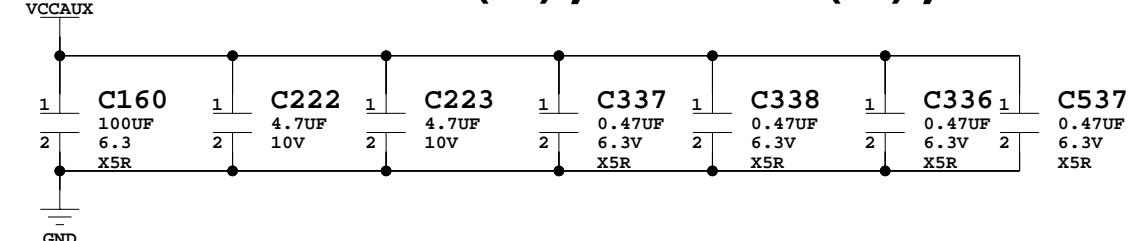


VCCPAUX 100uF (0), 4.7uF (2), 0.47uF (3)

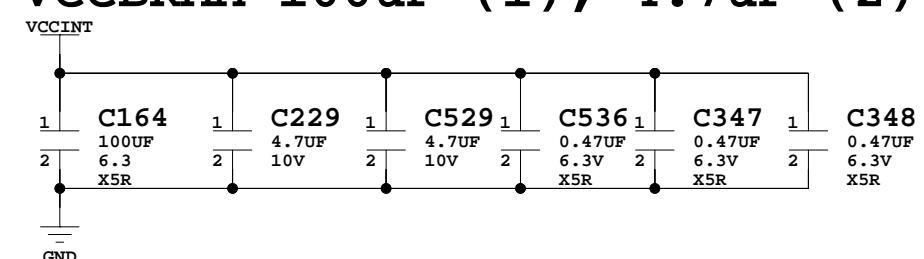


Place C339, C340 directly underneath the FPGA as short as possible connection to VCCPAUX and GND

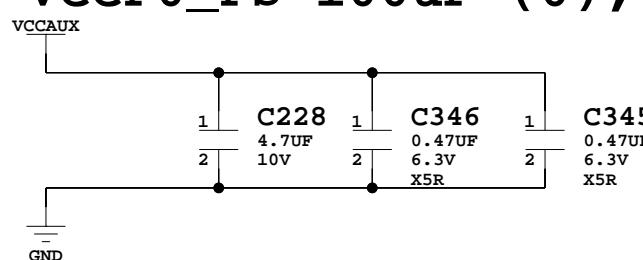
VCCAUX 100uF (1), 4.7uF (2), 0.47uF (4)



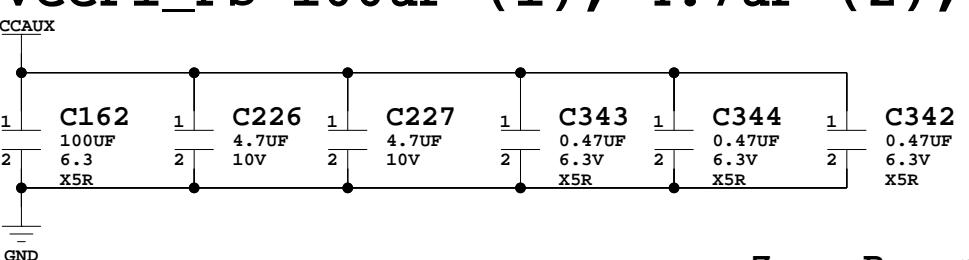
VCCBRAM 100 μ F (1) - 4,7 μ F (2) - 0,47 μ F (3)



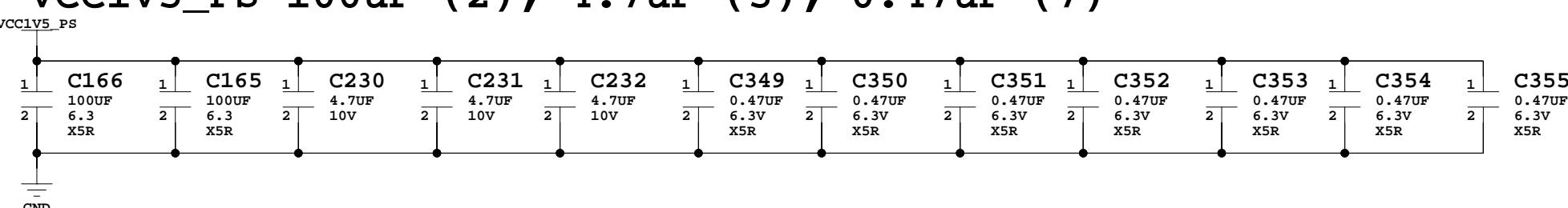
VCCP0 PS 100uF (0), 4.7uF (1), 0.47uF (2)



VCCP1 PS 100uF (1), 4.7uF (2), 0.47uF (3)



VCC1V5 PS 100uF (2), 4.7uF (3), 0.47uF (7)



Zyng Bypass Capacitors

TRIPLE CROWN

Title: Zyng Bypass Capacitors

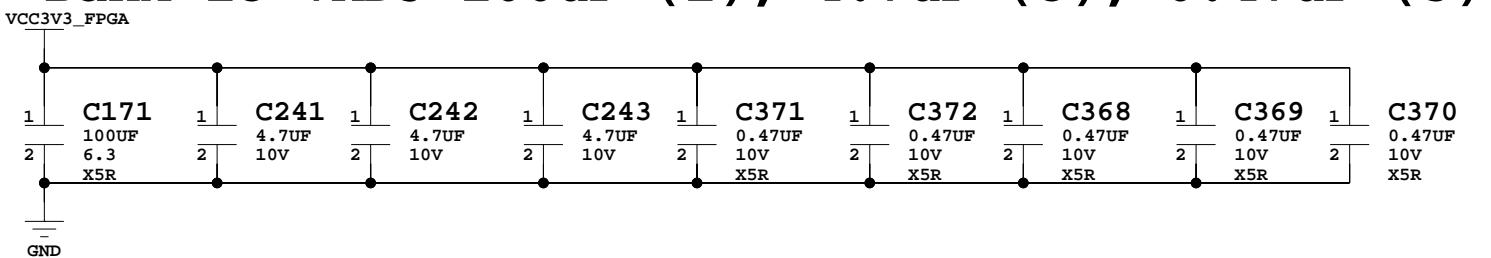
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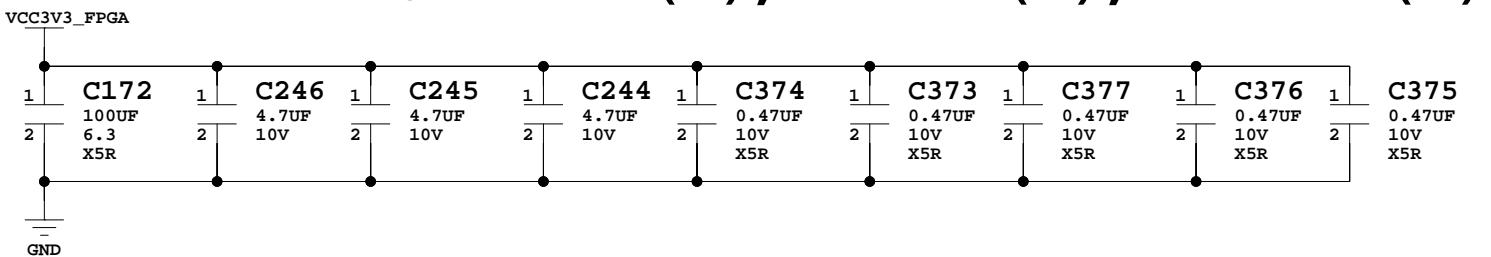
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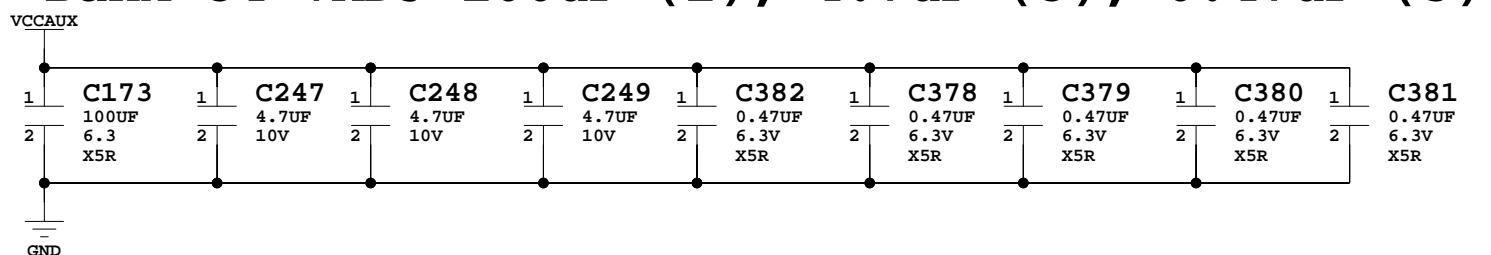
Bank 13 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



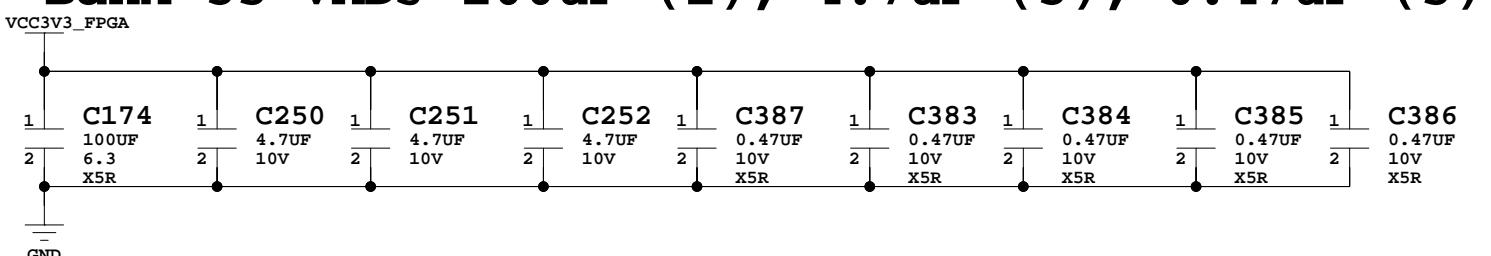
Bank 33 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 34 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 35 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Zynq Bypass Capacitors

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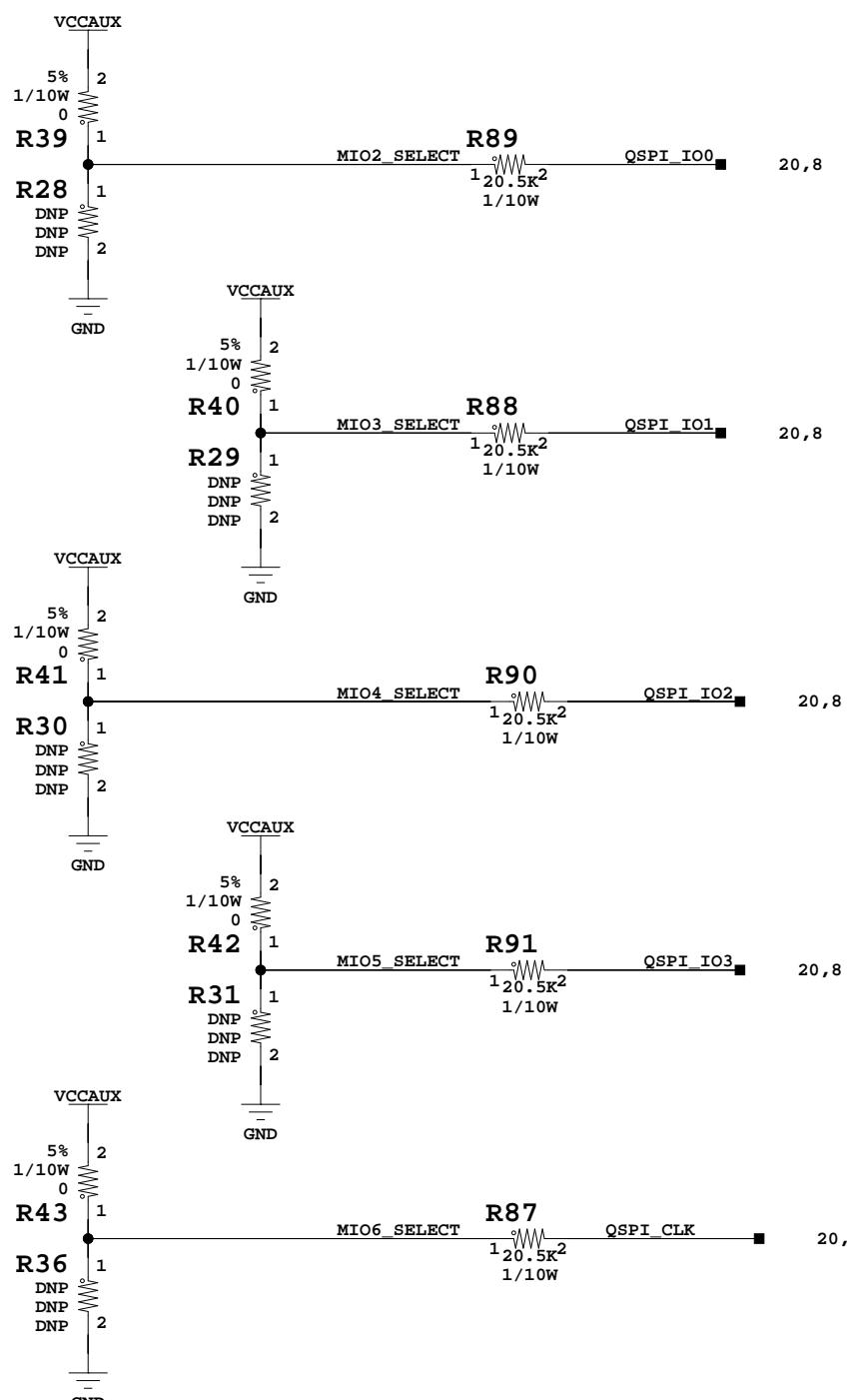
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MIO[6:2] SELECTION HEADERS

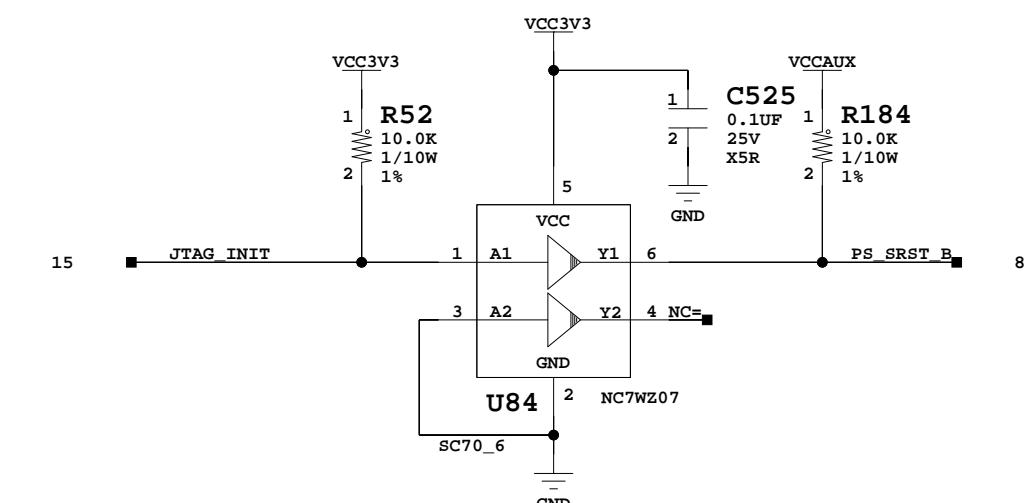
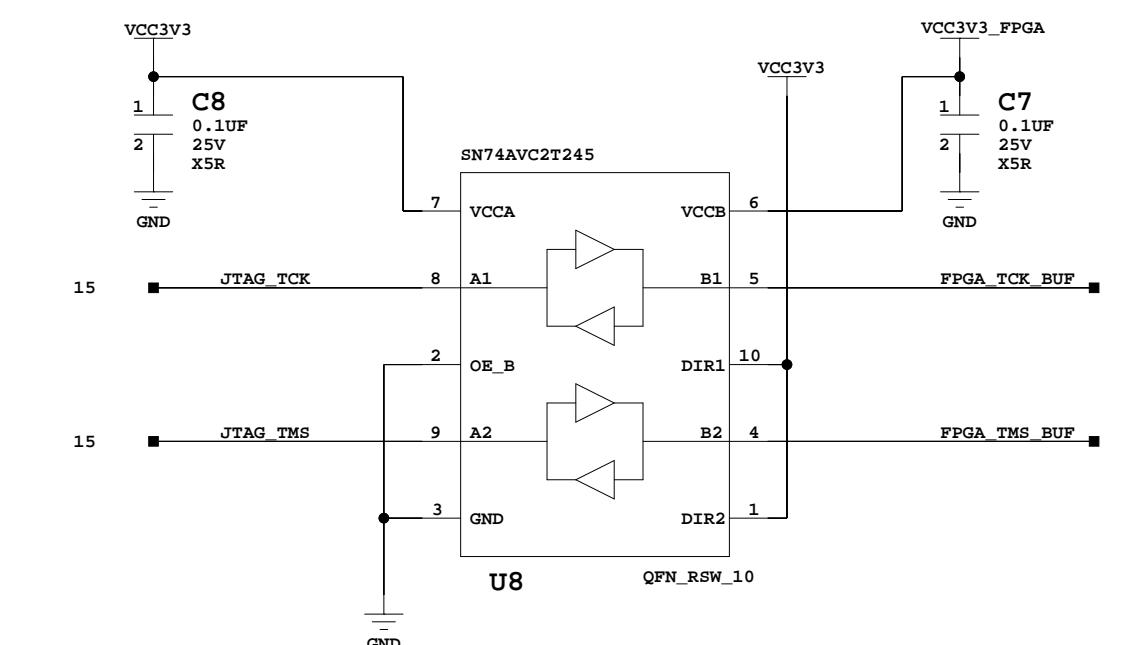
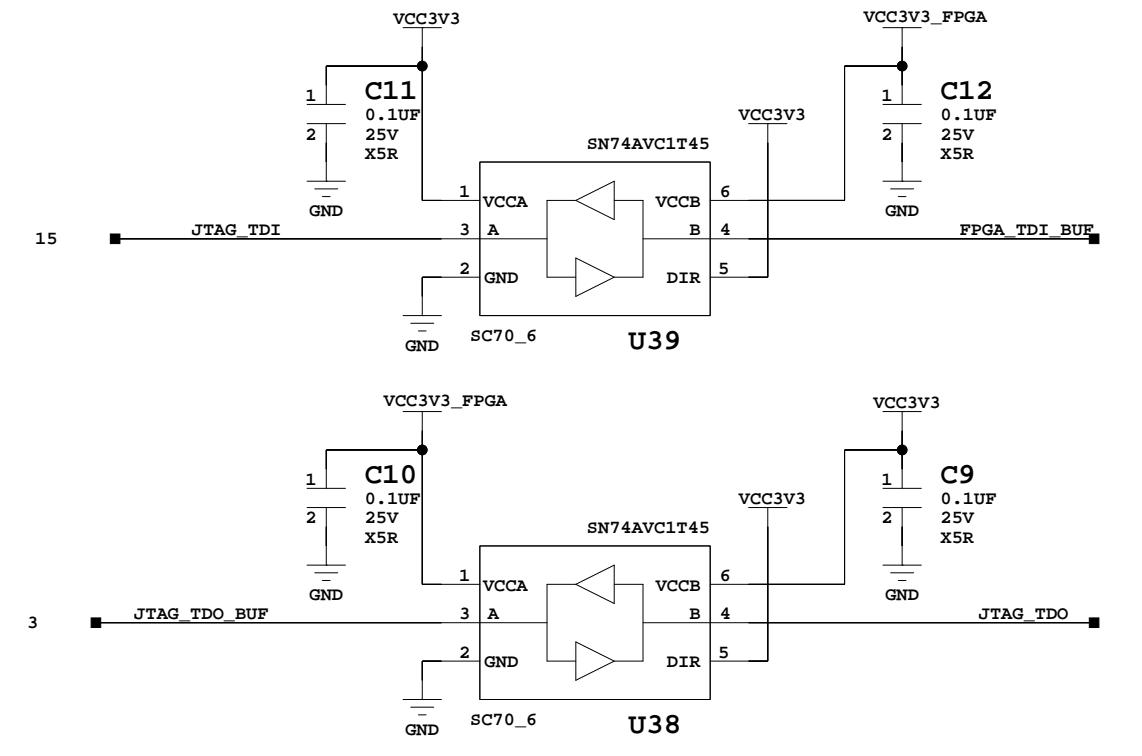
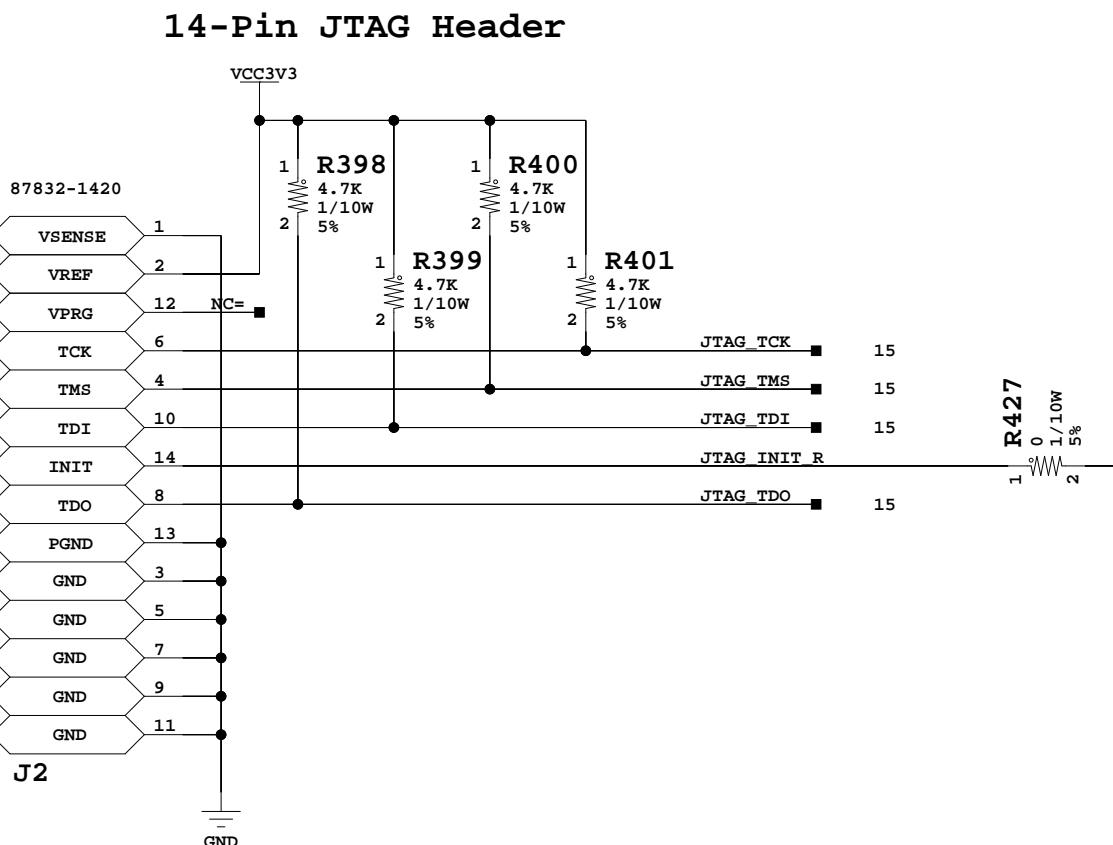


Zynq Config Pins

TRIPLE CROWN

Title: Zynq Config Pins

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JTAG Buffers, JTAG Hdr

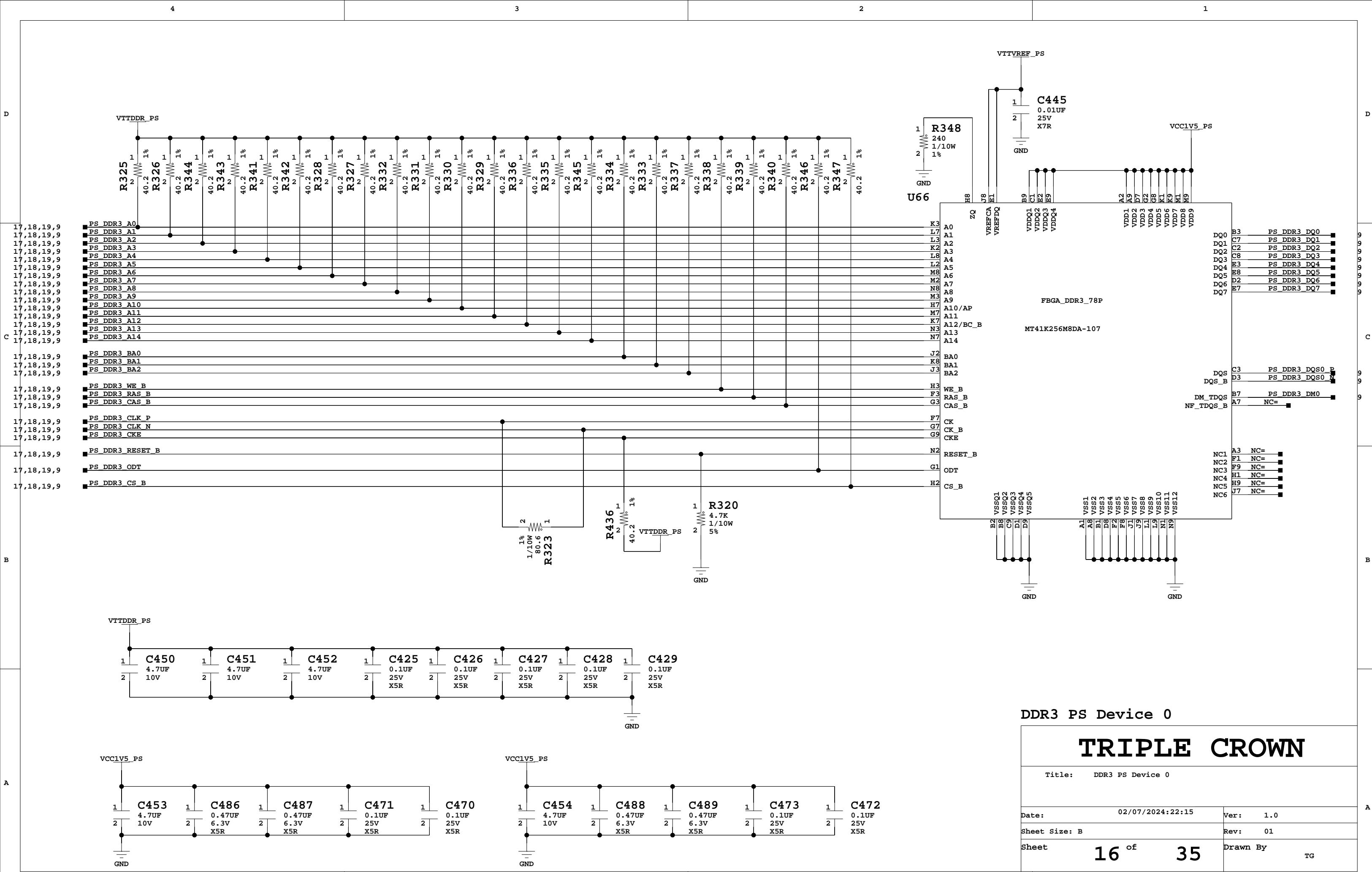
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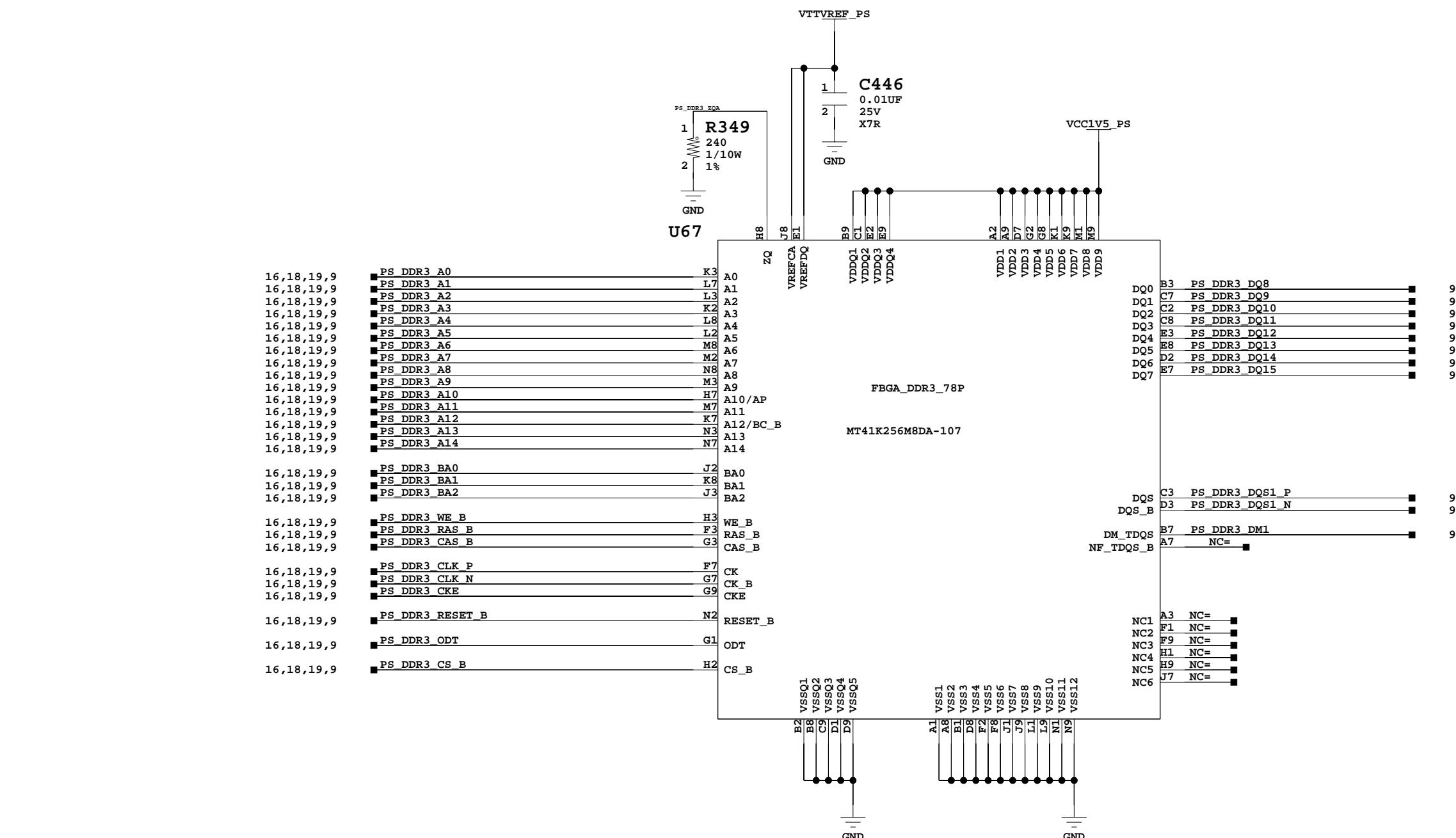
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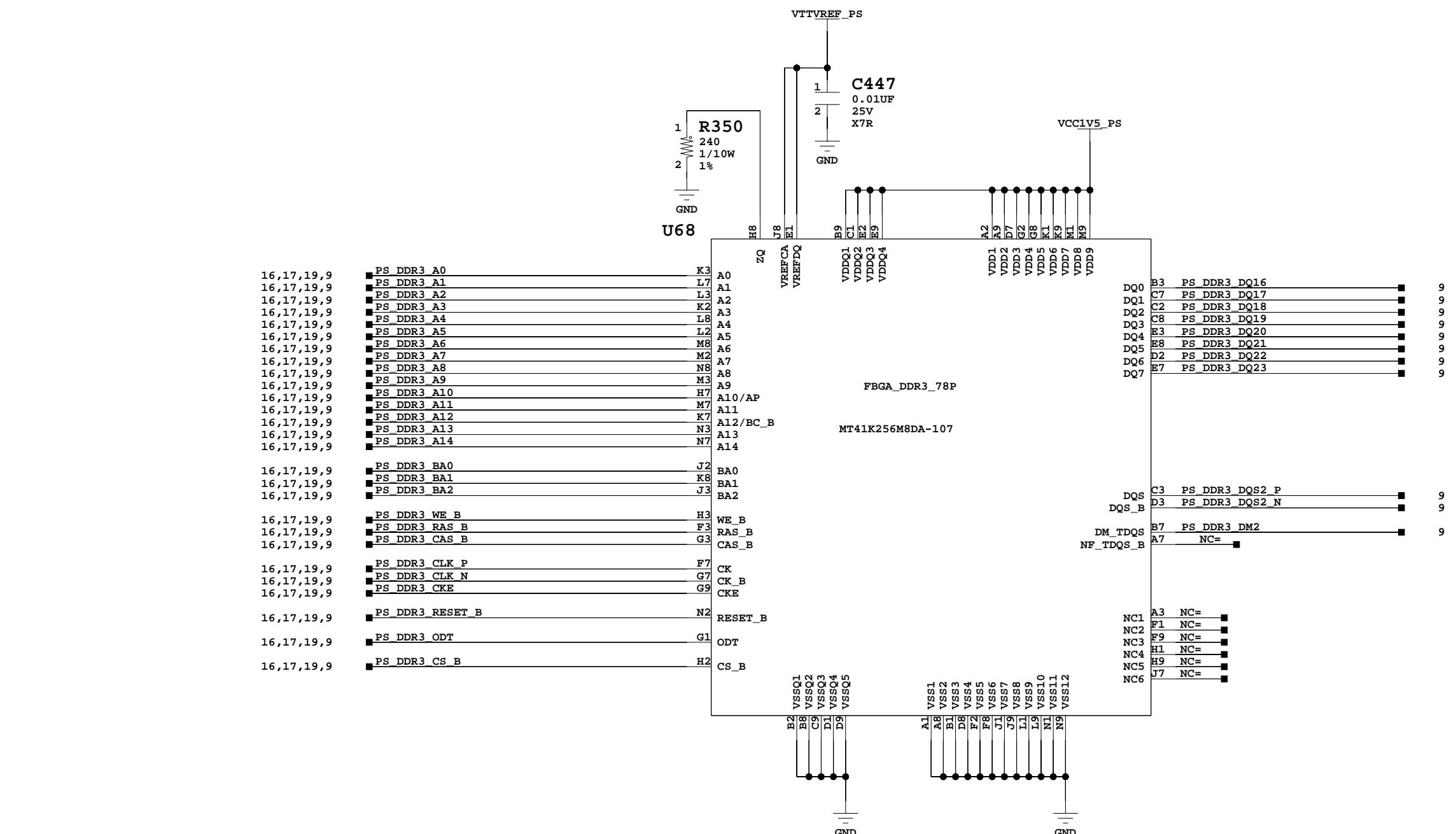
Date: 02/07/2024:22:15 Ver: 1.0

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DDR3 PS Device 2

TRIPLE CROWN

Title: DDR3 PS Device 2

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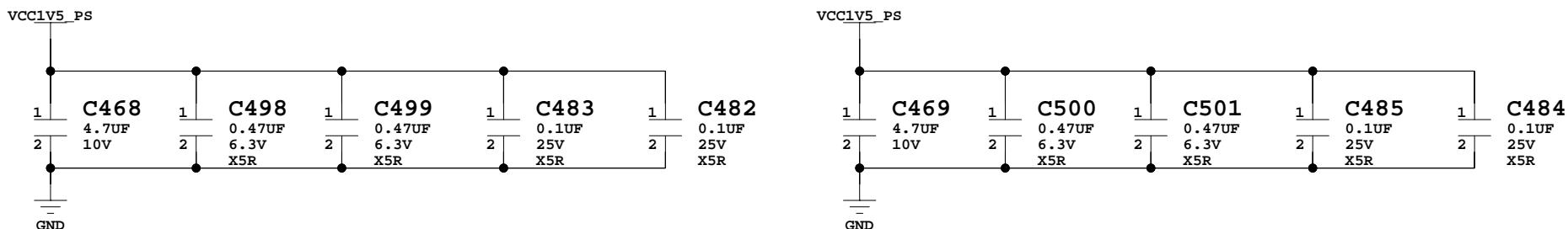
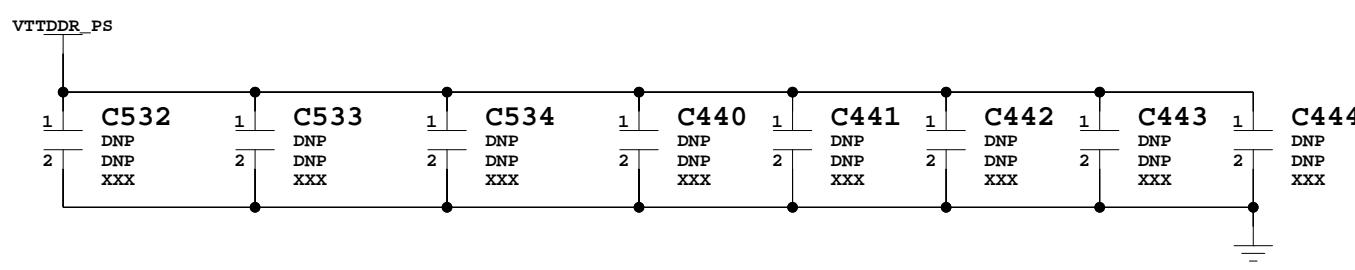
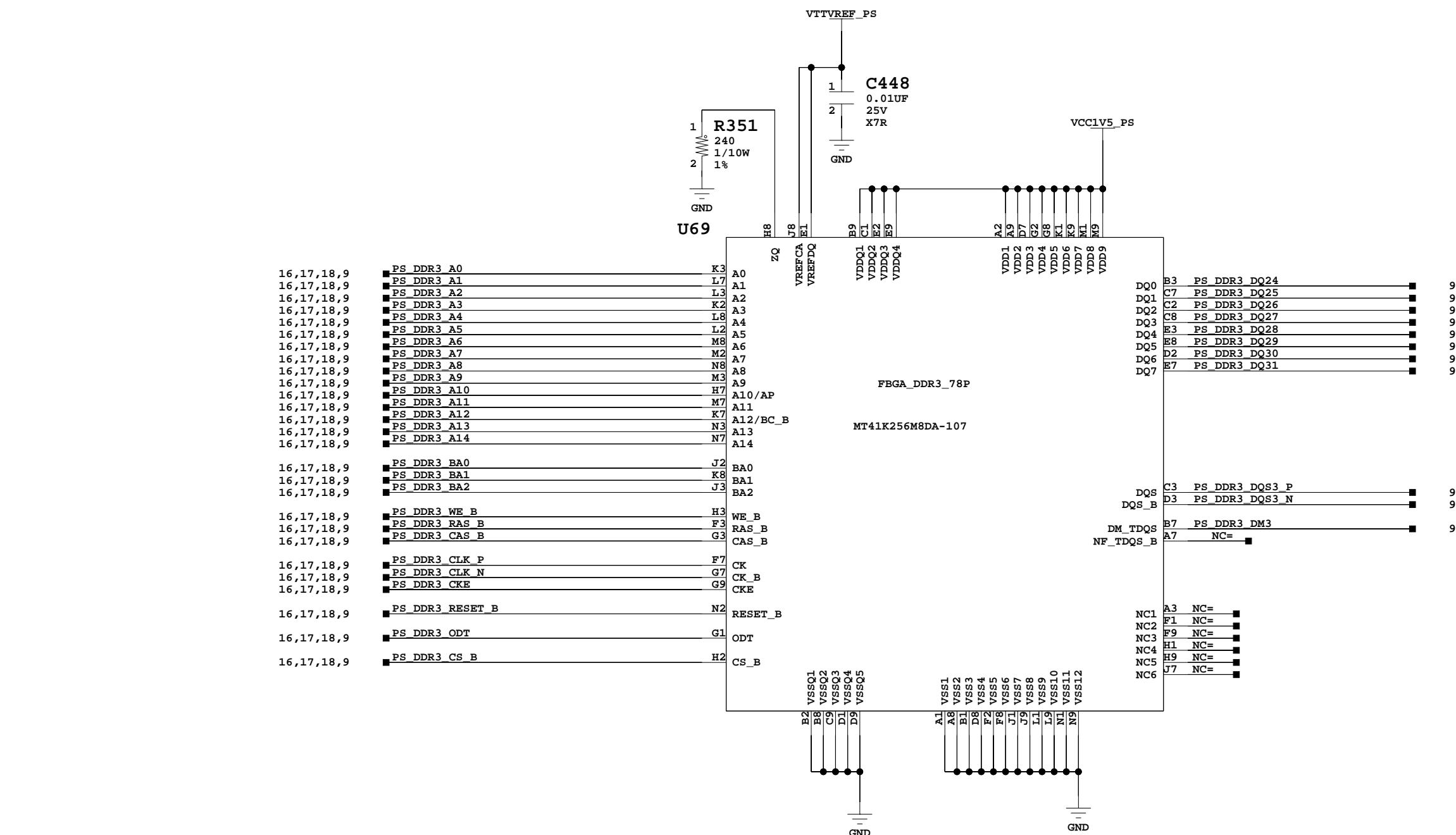
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DDR3 PS Device 3

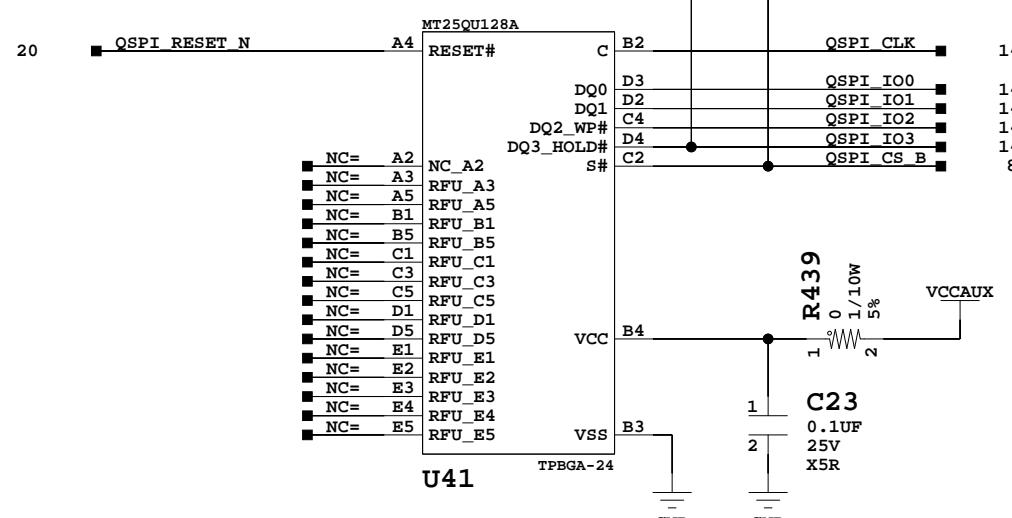
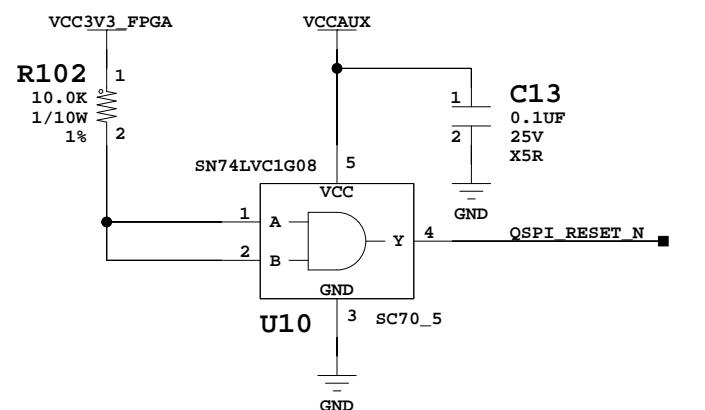
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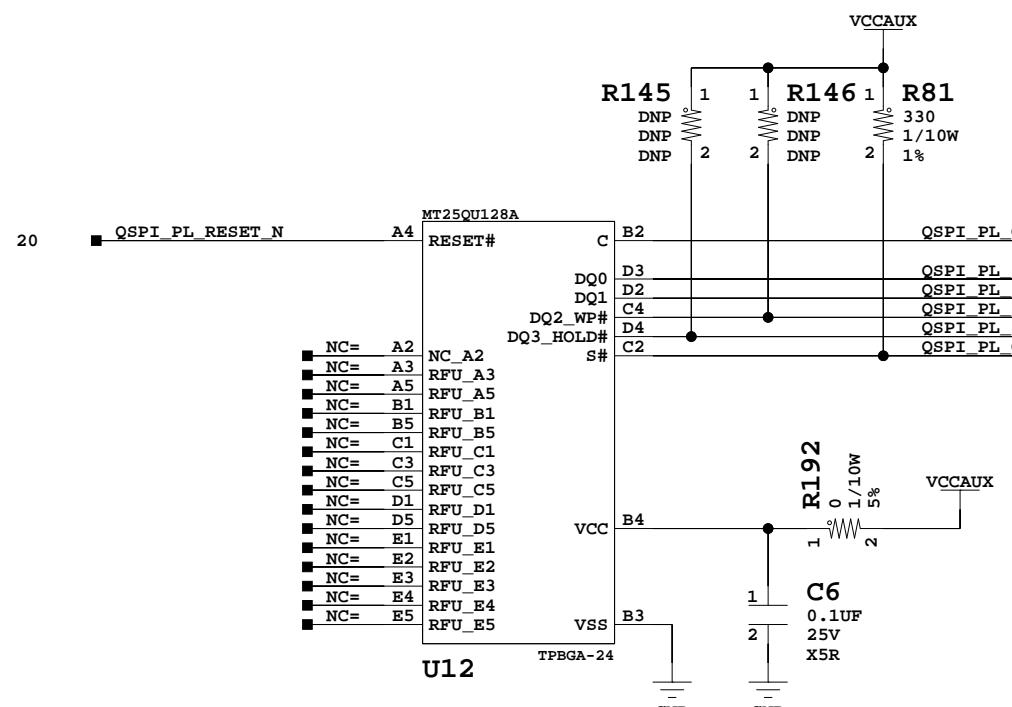
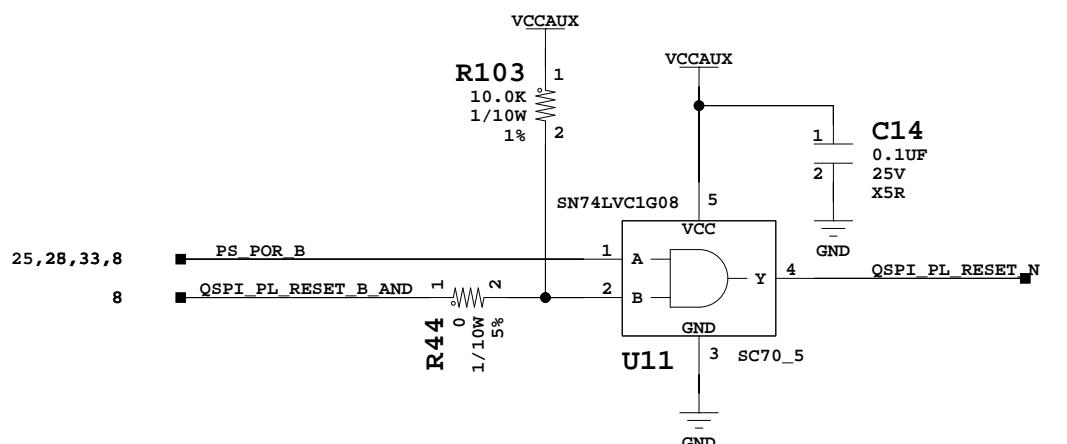
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PS Quad SPI

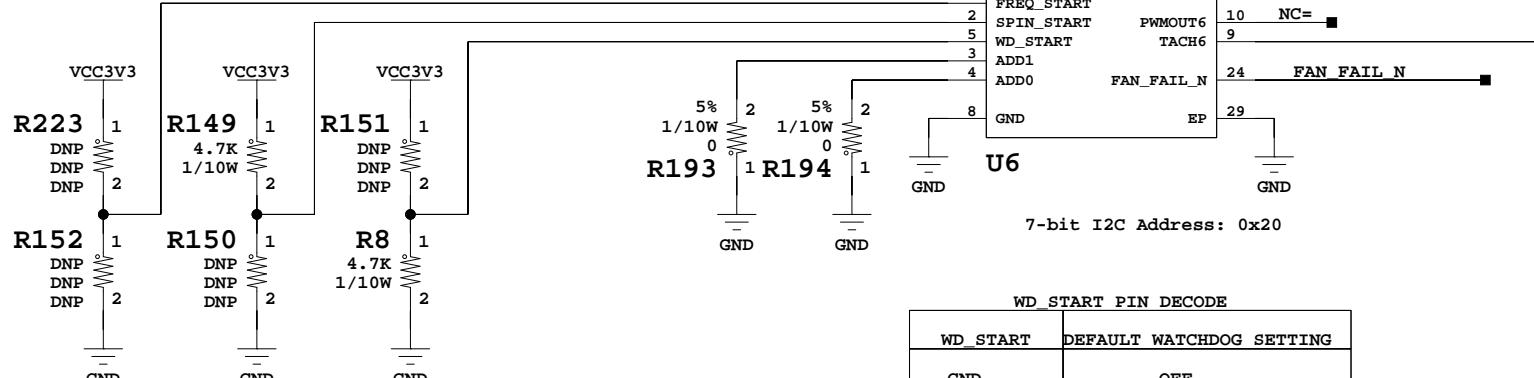
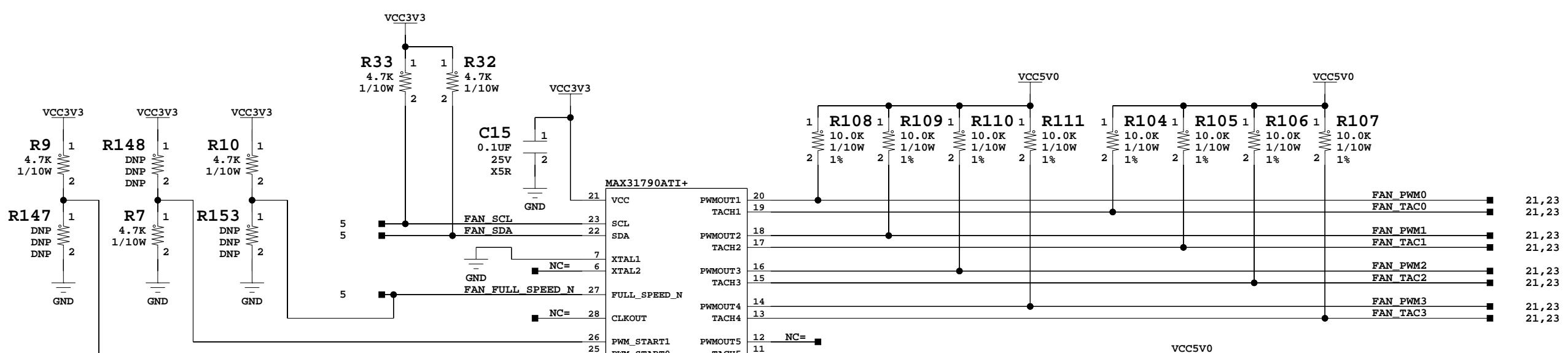


PL Quad SPI

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Title: Quad SPI

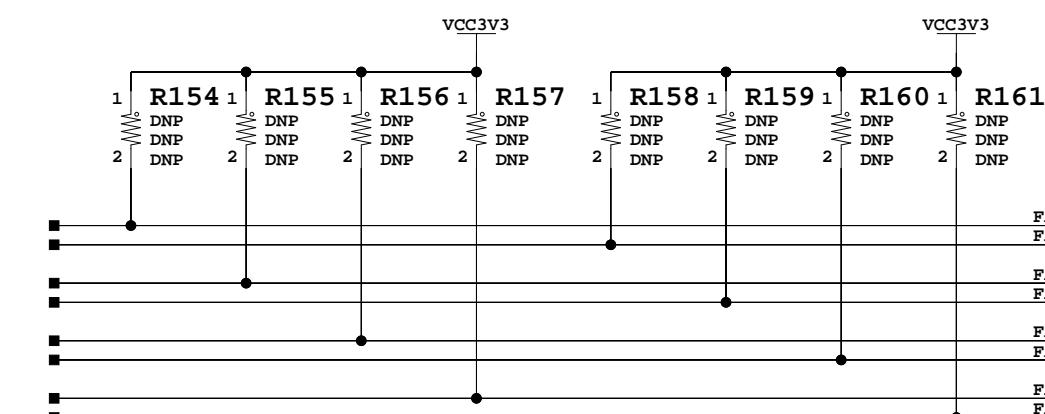
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WD_START	DEFAULT WATCHDOG SETTING
GND	OFF
VCC	ON

FREQ_START	FAN DEFAULT DRIVE SETTING
GND	30 Hz
VCC	25 kHz
UNCONNECTED	1.47 kHz

PWM_START0	PWM_START1	PWM DUTY CYCLE (%)
GND	GND	0
GND	UNCONNECTED	30
GND	VCC	40
UNCONNECTED	GND	50
UNCONNECTED	VCC	60
VCC	GND	75
VCC	VCC	100



Fan Control and Sense

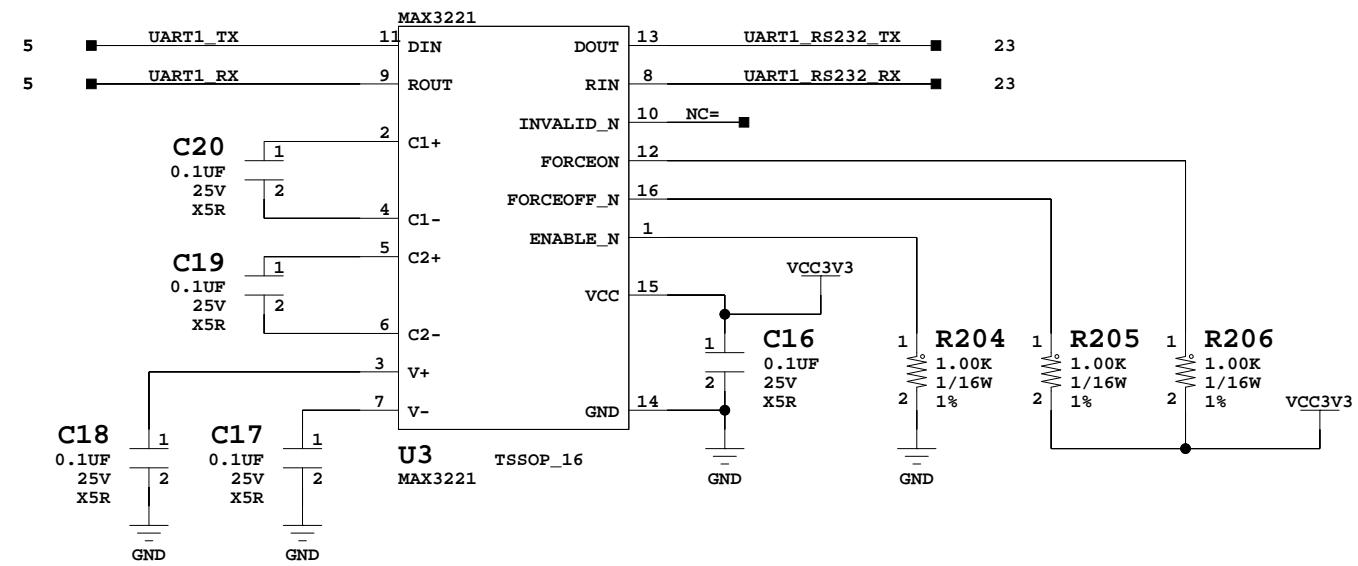
TRIPLE CROWN

Title: Fan Control and Sense

Date: 02/07/2024:22:15 Ver: 1.0

Sheet Size: B Rev: 01

Sheet 21 of 35 Drawn By TG



RS-232 UART

TRIPLE CROWN

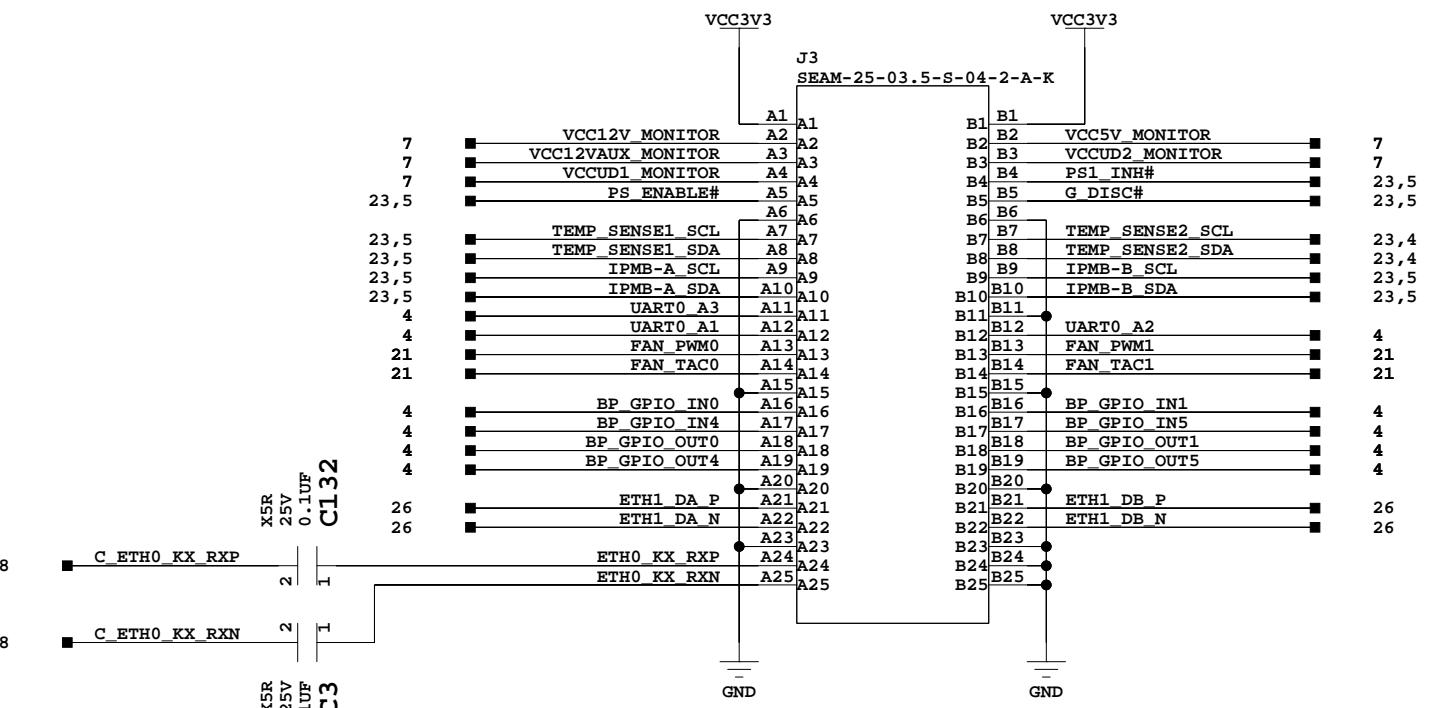
Title: RS-232 UART

Date: 02/07/2024:22:15 Ver: 1.1

Sheet Size: B Rev: 02

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D

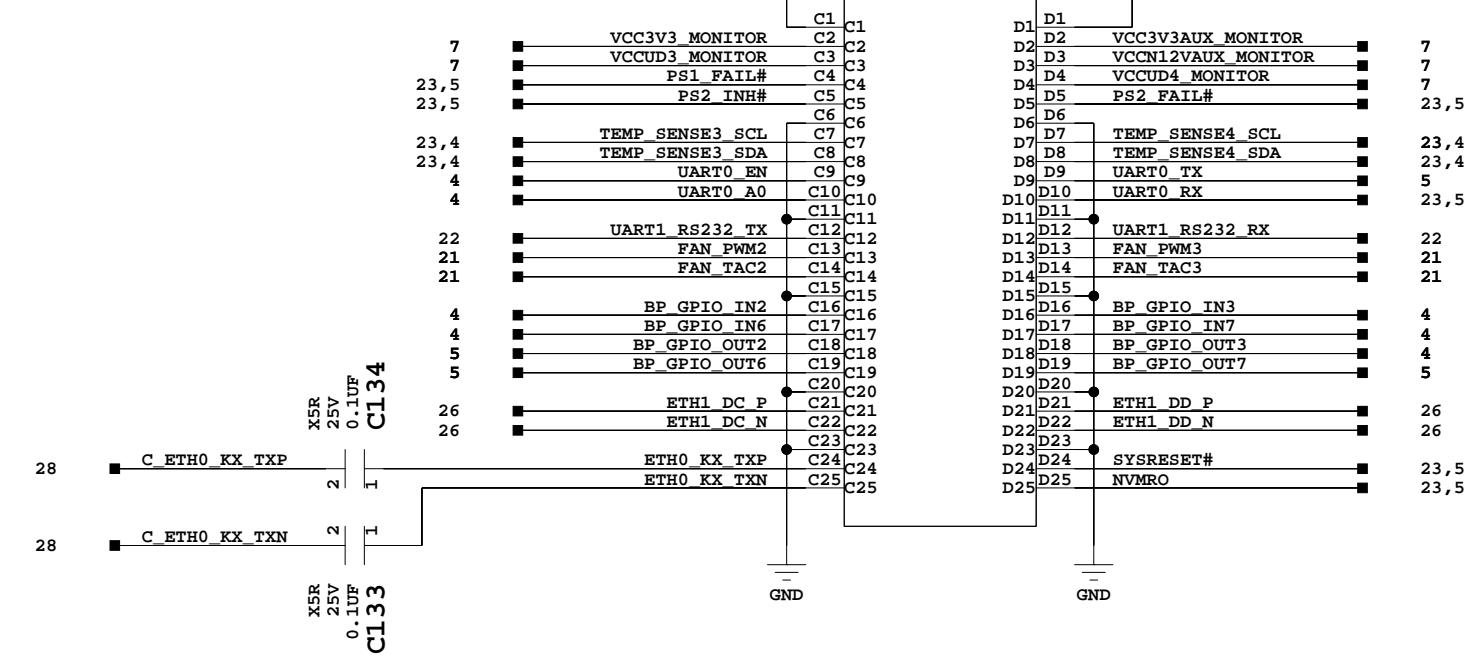


C

B

A

D

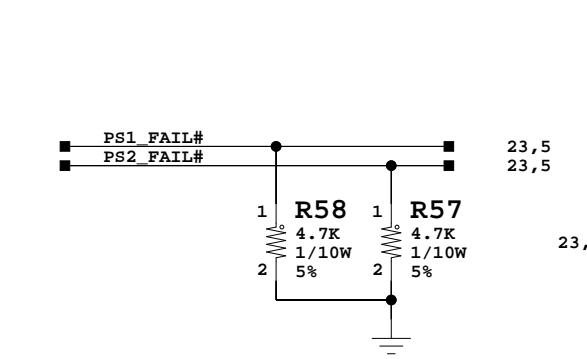


C

B

A

D



B

A

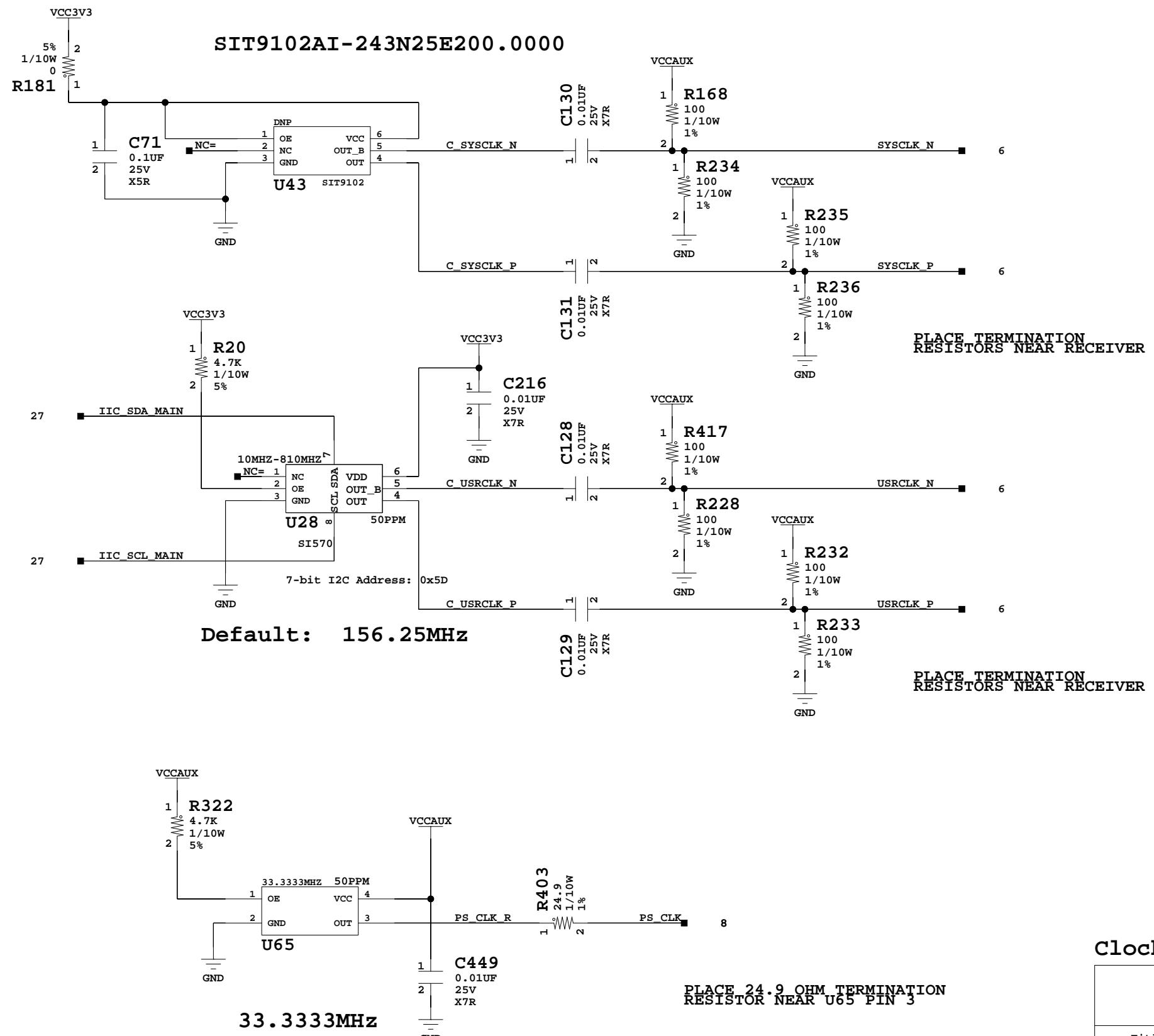
I/O CONNECTOR**TRIPLE CROWN**

Title: I/O Connector

Date: 09/07/2024:15:38 Ver: 1.1

Sheet Size: B Rev: 02

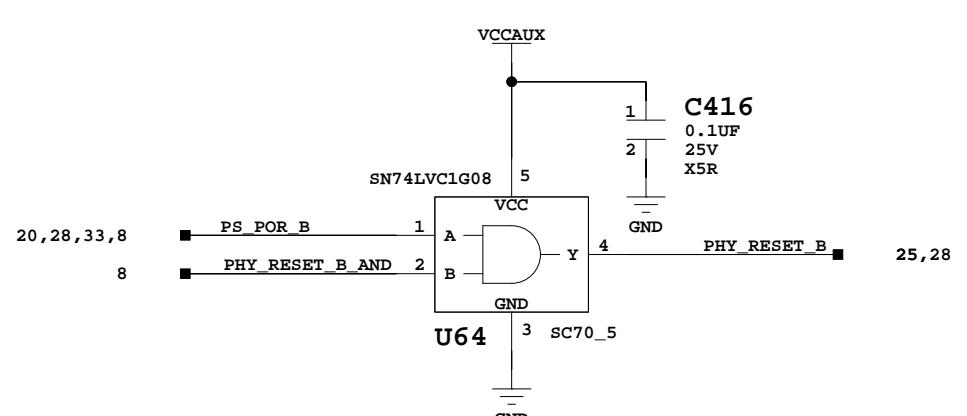
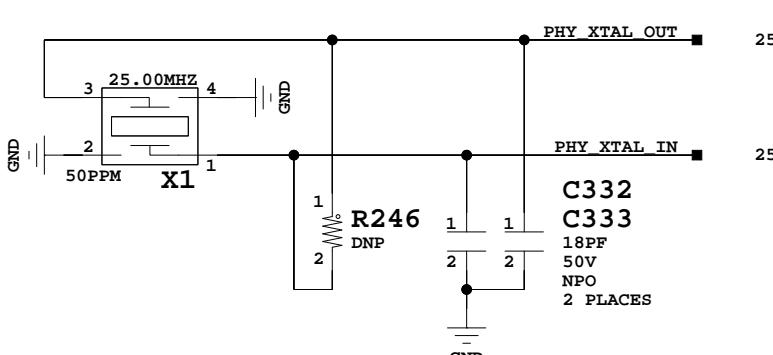
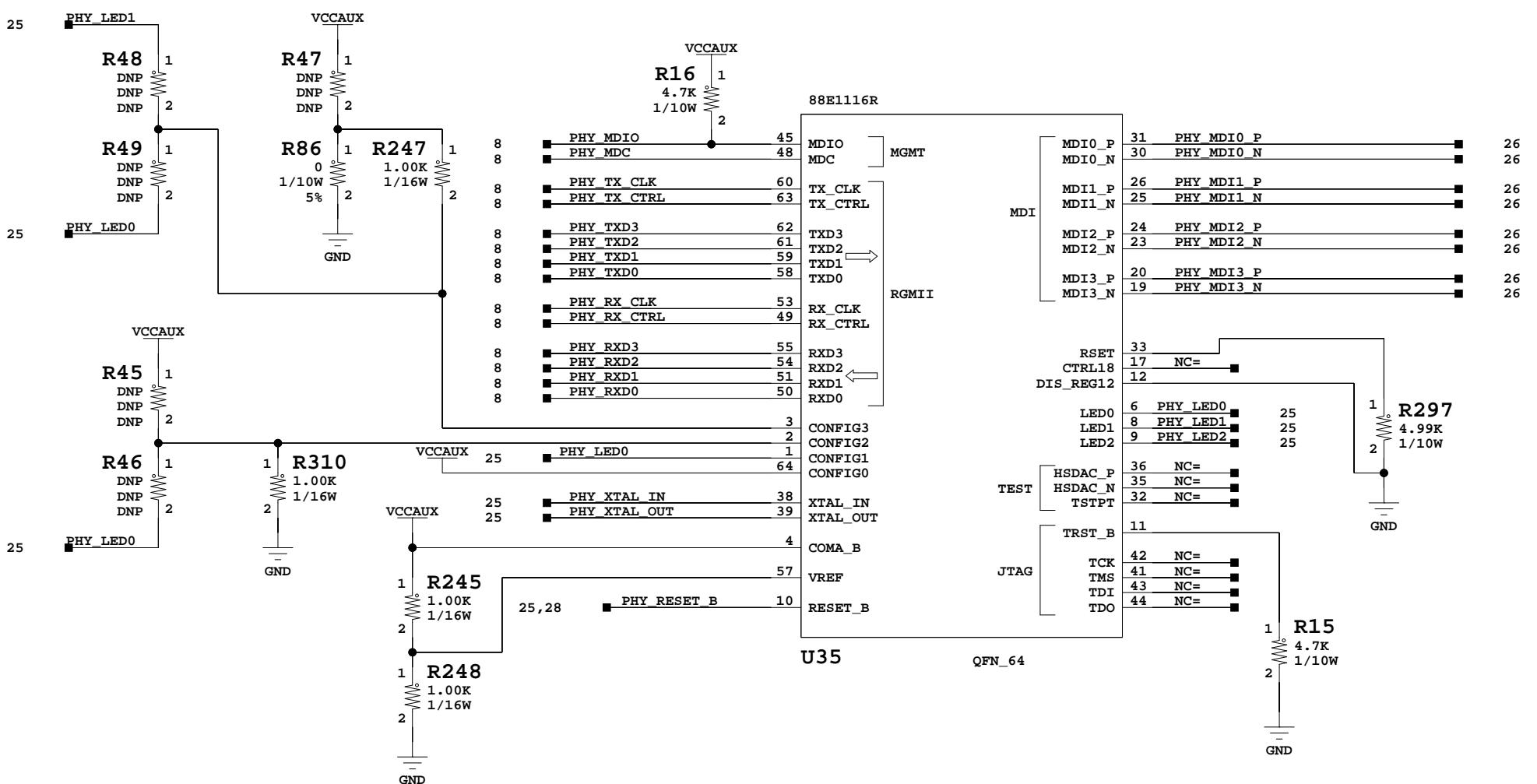
Sheet 23 of 35 Drawn By BF

**Clocks****TRIPLE CROWN**

Title: Clocks

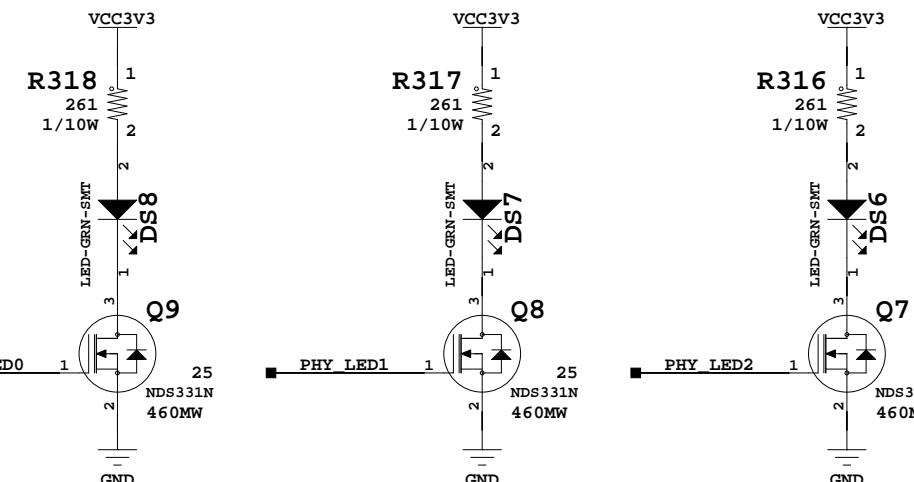
Date:	02/07/2024:22:15	Ver:	1.0
Sheet Size:	B	Rev:	01
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CONFIGURATION MAPPING		
PIN	SETTING	CONFIGURATION
CONFIG0	VCCO_MIO1	PHYAD[1]=1 PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0 PHYAD[2]=1
CONFIG2	GND	ENA_XC=0 PHYAD[4]=0
	EPHY_LED0	ENA_XC=0 PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1 PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0 RGMII_RX=0
	EPHY_LED0	RGMII_TX=0 RGMII_RX=1
	EPHY_LED1	RGMII_TX=1 RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1 RGMII_RX=1



SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.



GEM / MDIO

Title: GEM / MDIO

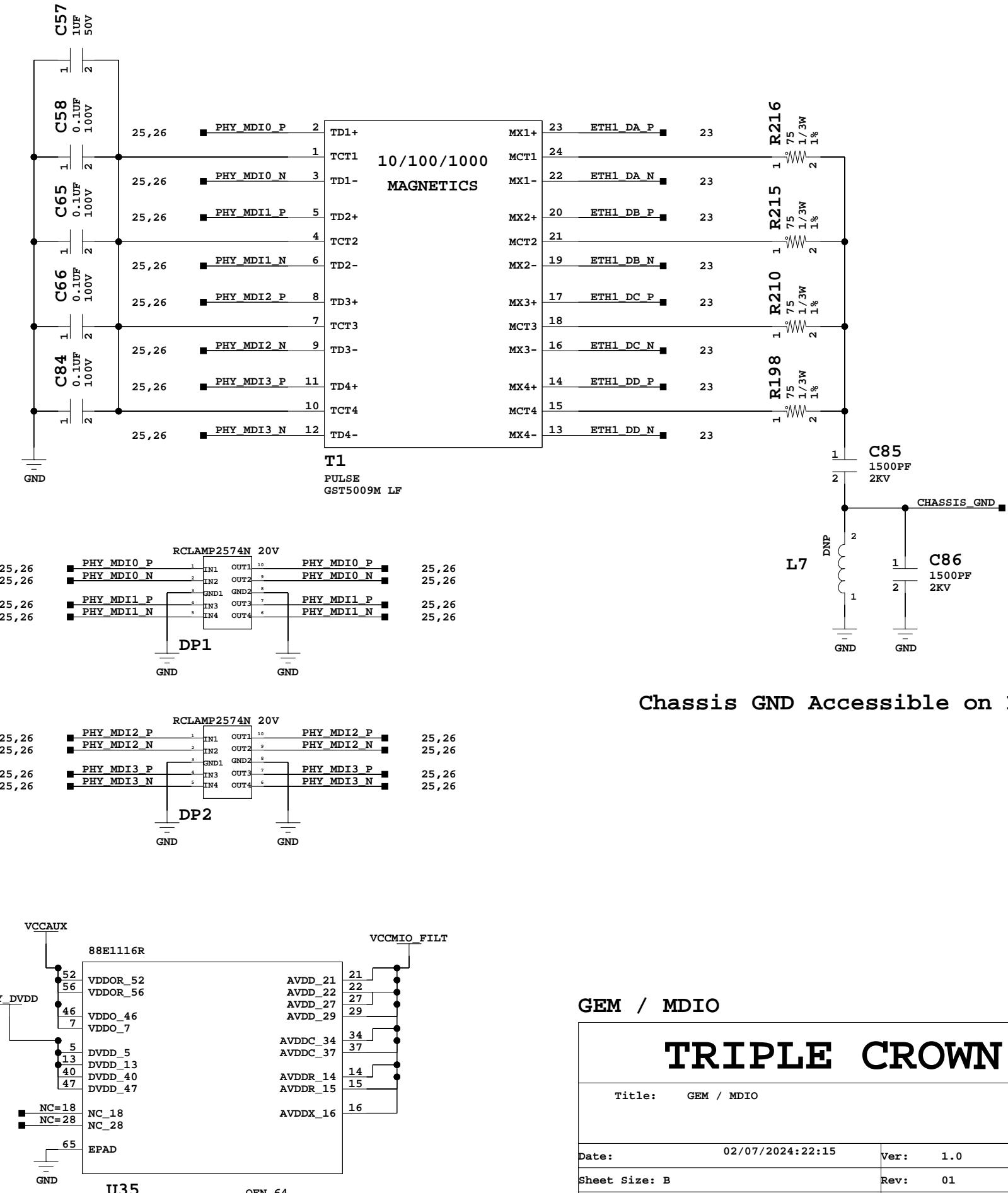
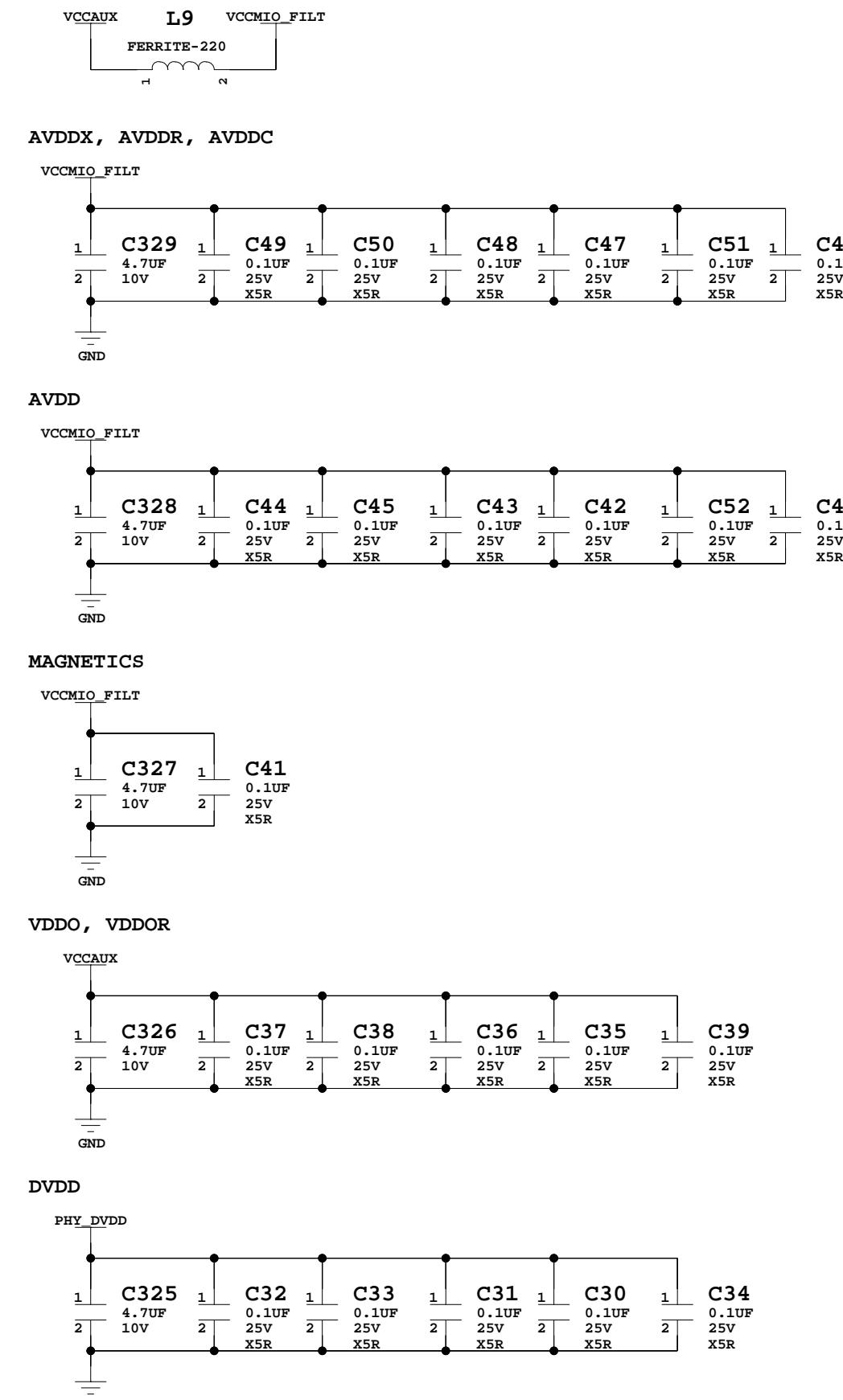
Date: 02/07/2024:22:15 Ver: 1.0

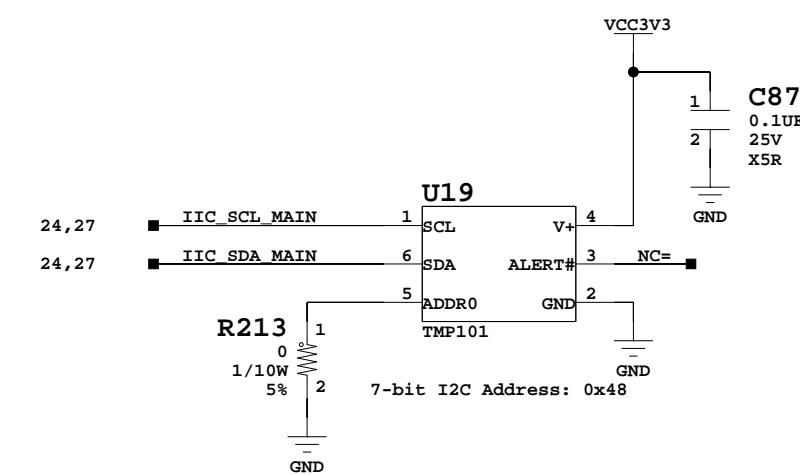
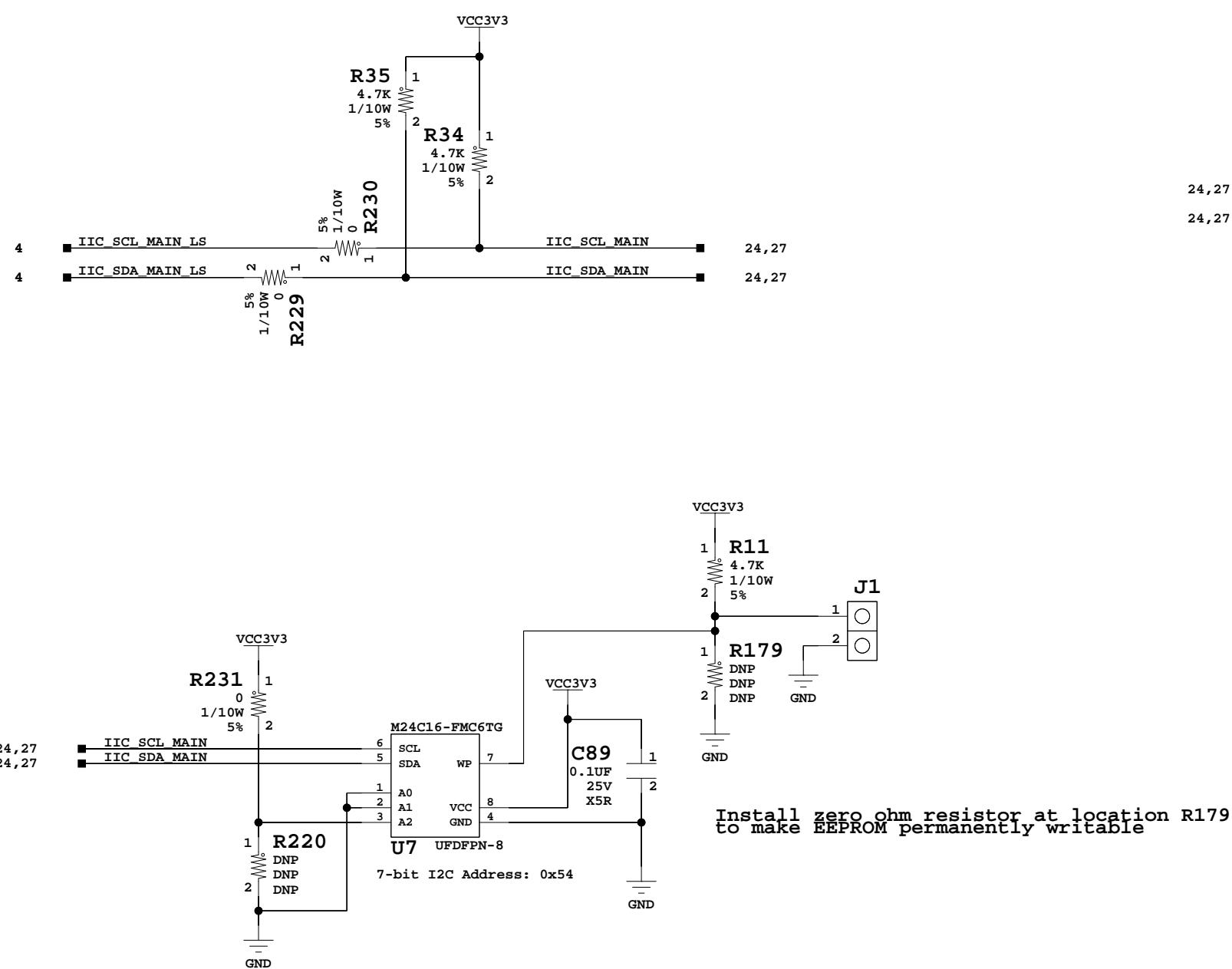
Sheet Size: B Rev: 01

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TRIPLE CROWN

GEM / MDIO - POWER & DECOUPLING





EEPROM, TEMPERATURE SENSOR

TRIPLE CROWN

Title: EEPROM, TEMPERATURE SENSOR

Date: 02/07/2024:22:15 Ver: 1.1

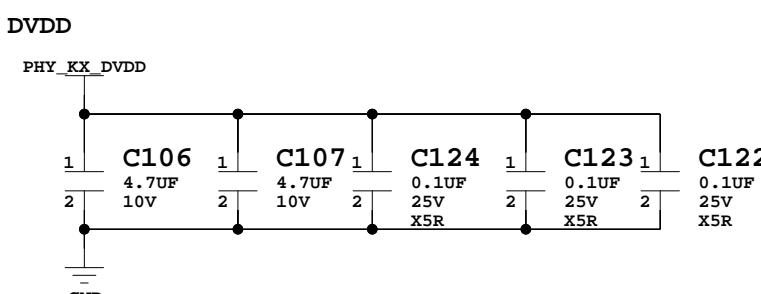
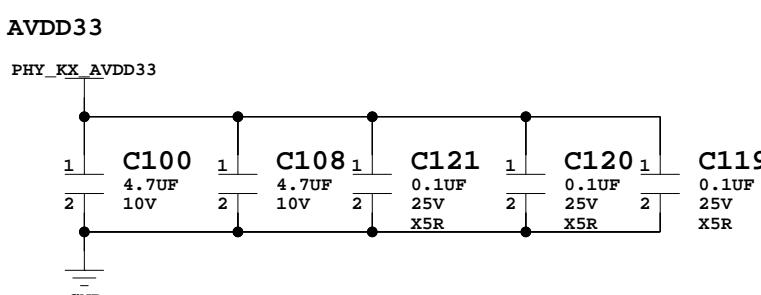
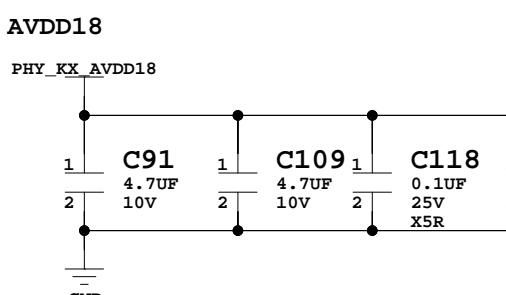
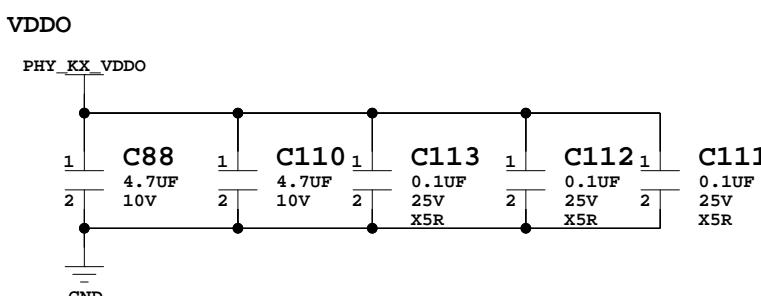
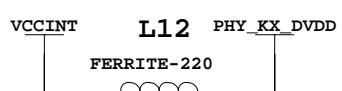
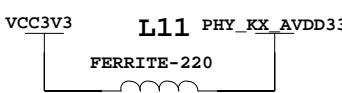
Sheet Size: B Rev: 02

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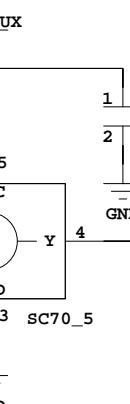
POWER & DECOUPLING



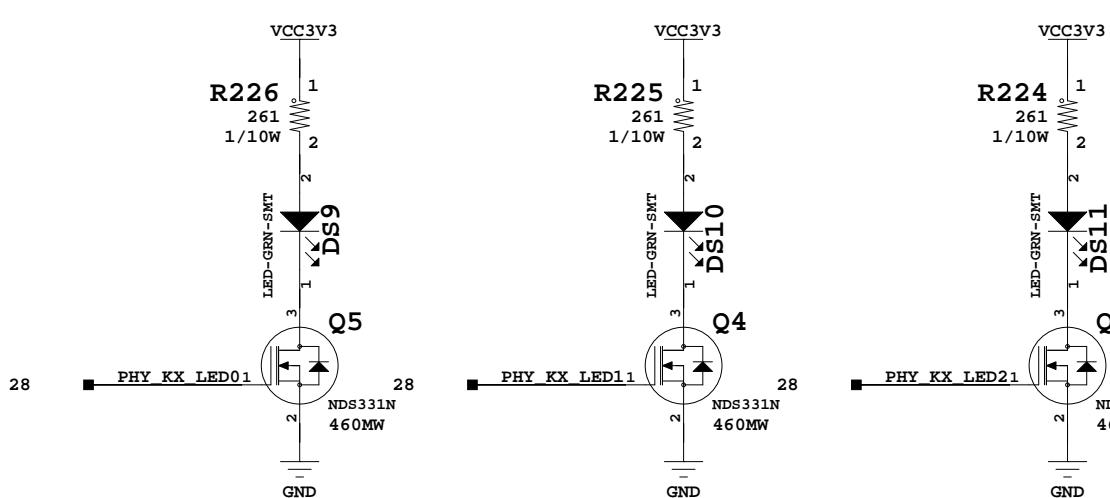
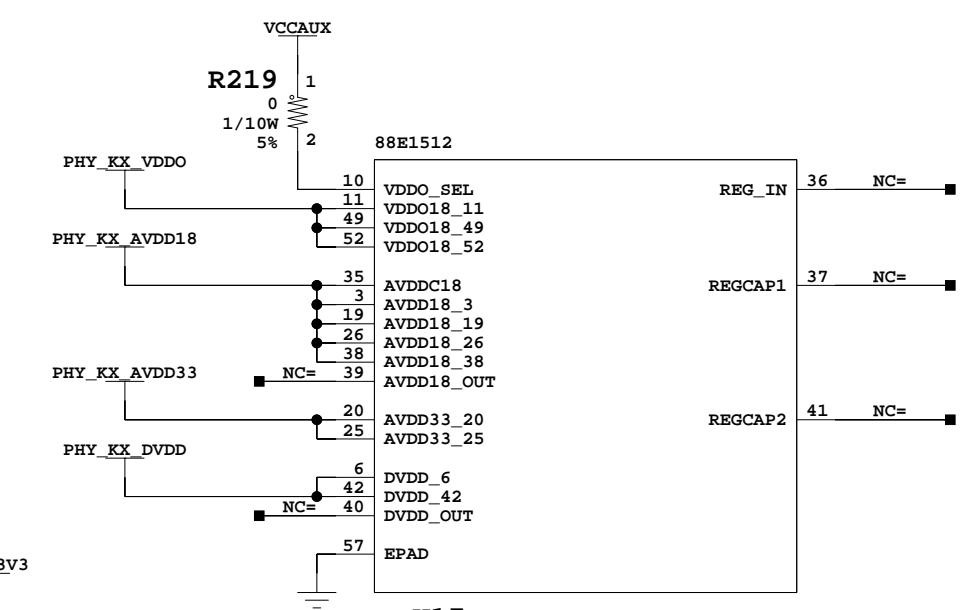
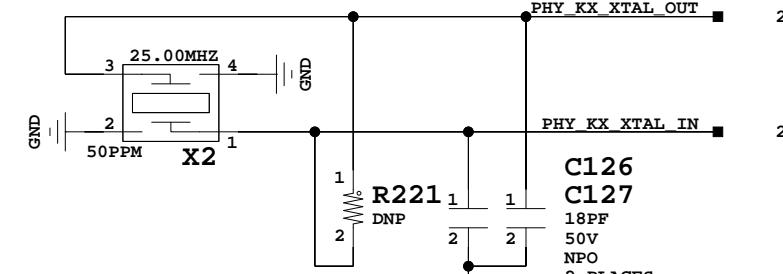
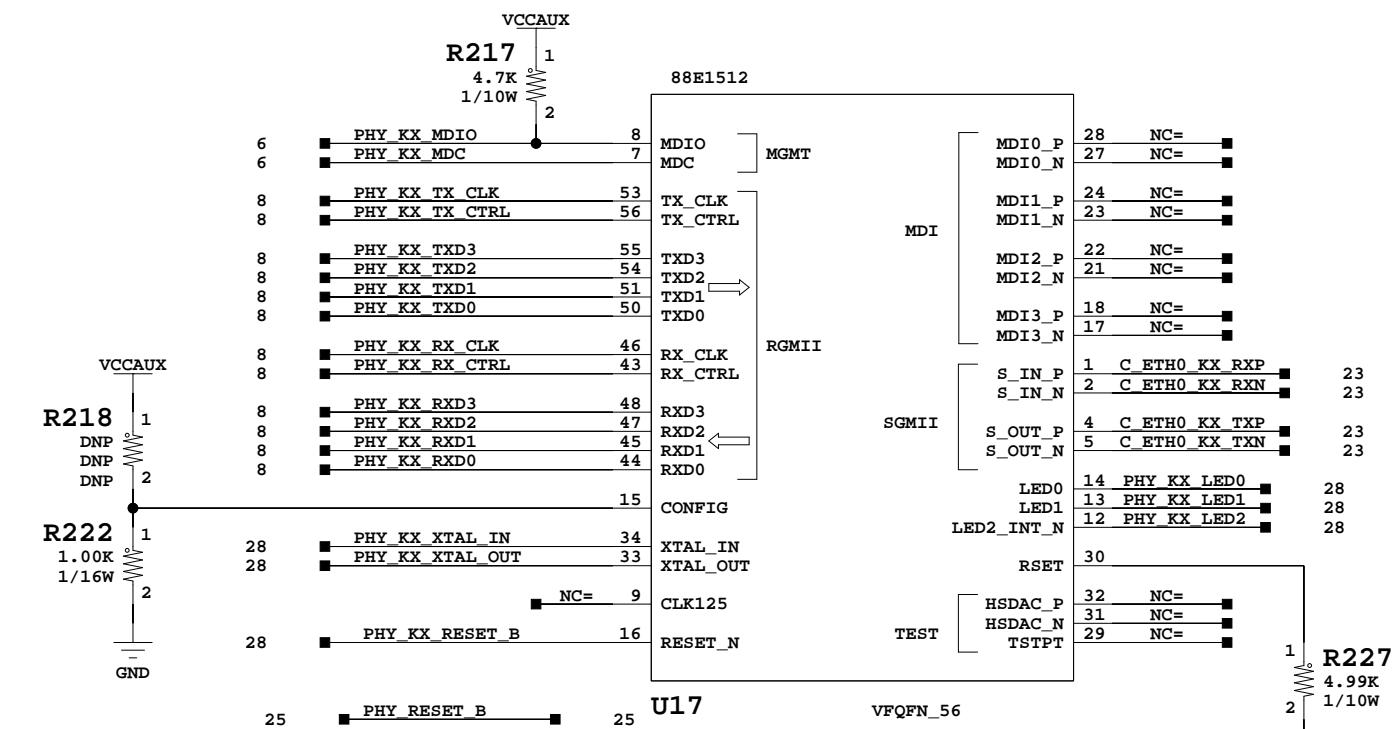
20,25,33,8 8 SN74LVC1G08 5 VCC
PS POR_B 1 A
PHY_KX_RESET_B_AND 2 B
GND Y 4 PHY_KX_RESET_B 28



ADD SEPARATE FPGA RESET CONTROL?



U9 SC70-5



1000BASE-KX Ethernet

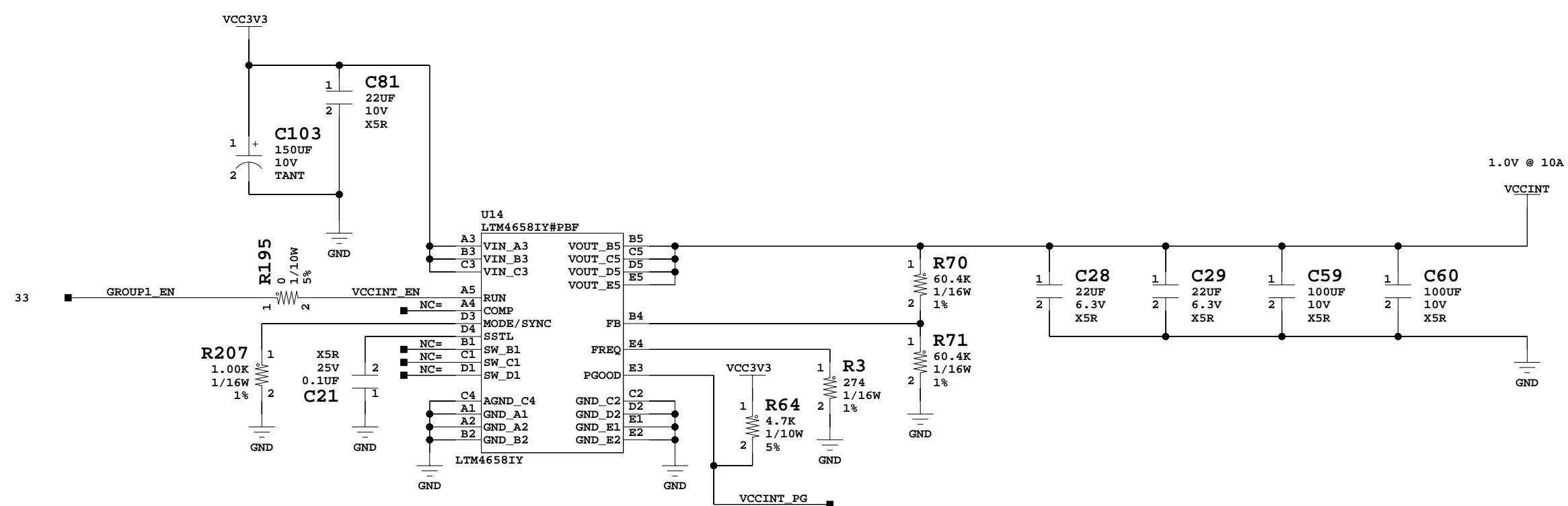
TRIPLE CROWN

Title: 1000BASE-KX Ethernet

Date: 09/07/2024:15:29 Ver: 1.0

Sheet Size: B Rev: 01

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1.0V 10A Power Regulator

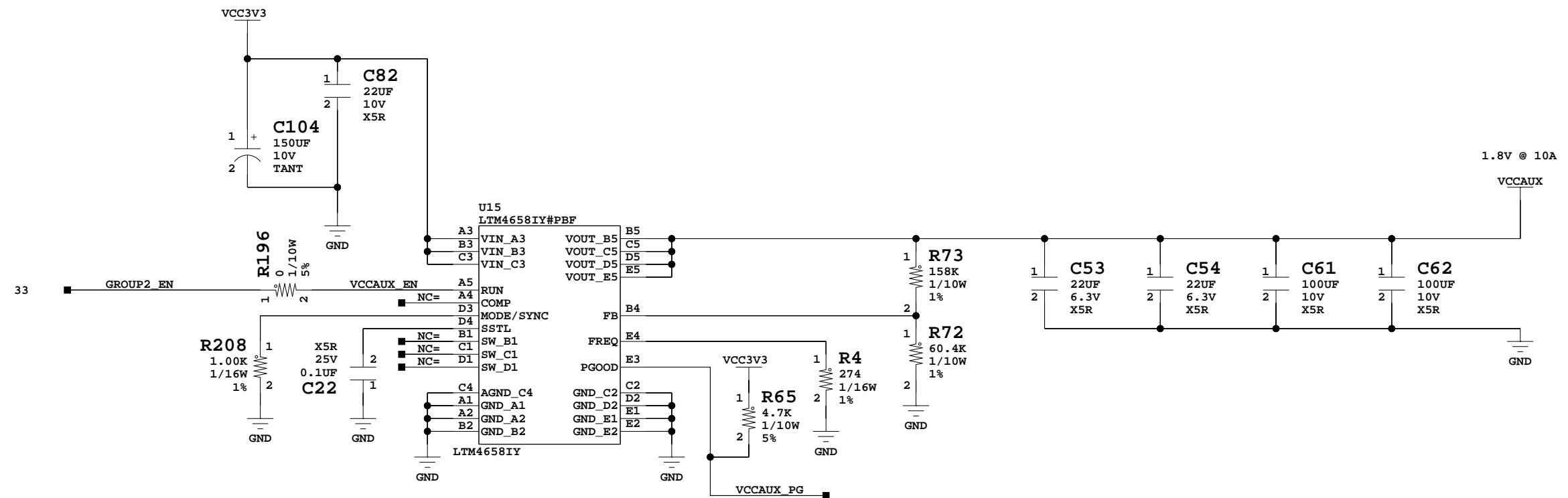
TRIPLE CROWN

Title: 1.0V 10A Power Regulator

Date:	02/07/2024:22:15	Ver:	1.0
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Sheet Size:	B	Rev:	01
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Sheet	29 of 35	Drawn By	TG
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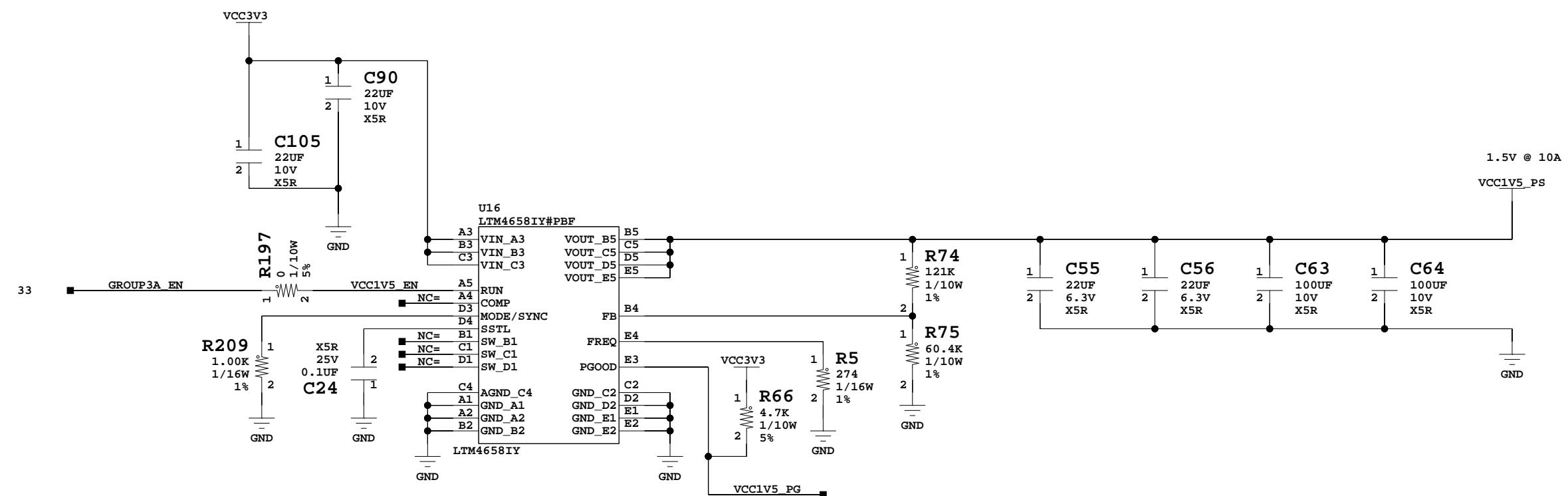


1.8V 10A Power Regulator

TRIPLE CROWN

Title: 1.8V 10A Power Regulator

Date:	02/07/2024:22:15	Ver:	1.0
Sheet Size:	B	Rev:	01
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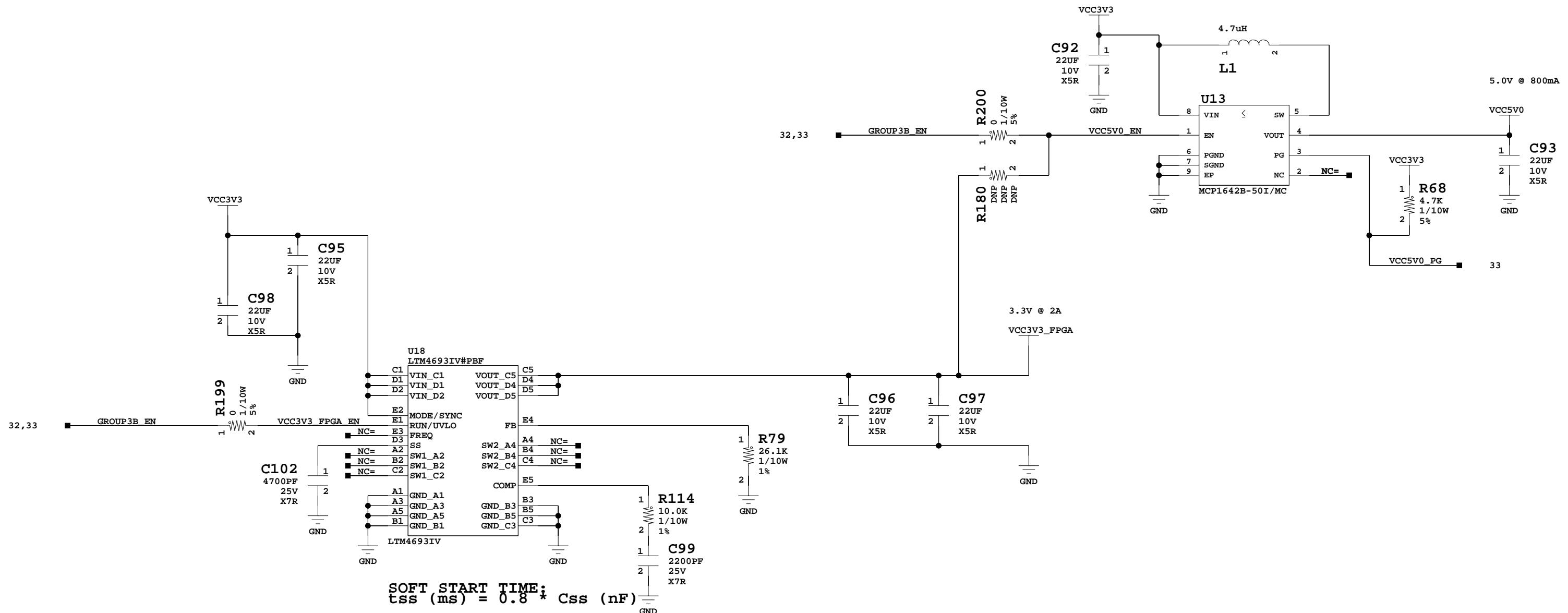


1.5V 10A Power Regulator

TRIPLE CROWN

Title: 1.5V 10A Power Regulator

Date:	02/07/2024:22:15	Ver:	1.0
Sheet Size:	B	Rev:	01
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3.3V, 5V Power Regulators

TRIPLE CROWN

Title: 3.3V and 5V Power Regulators

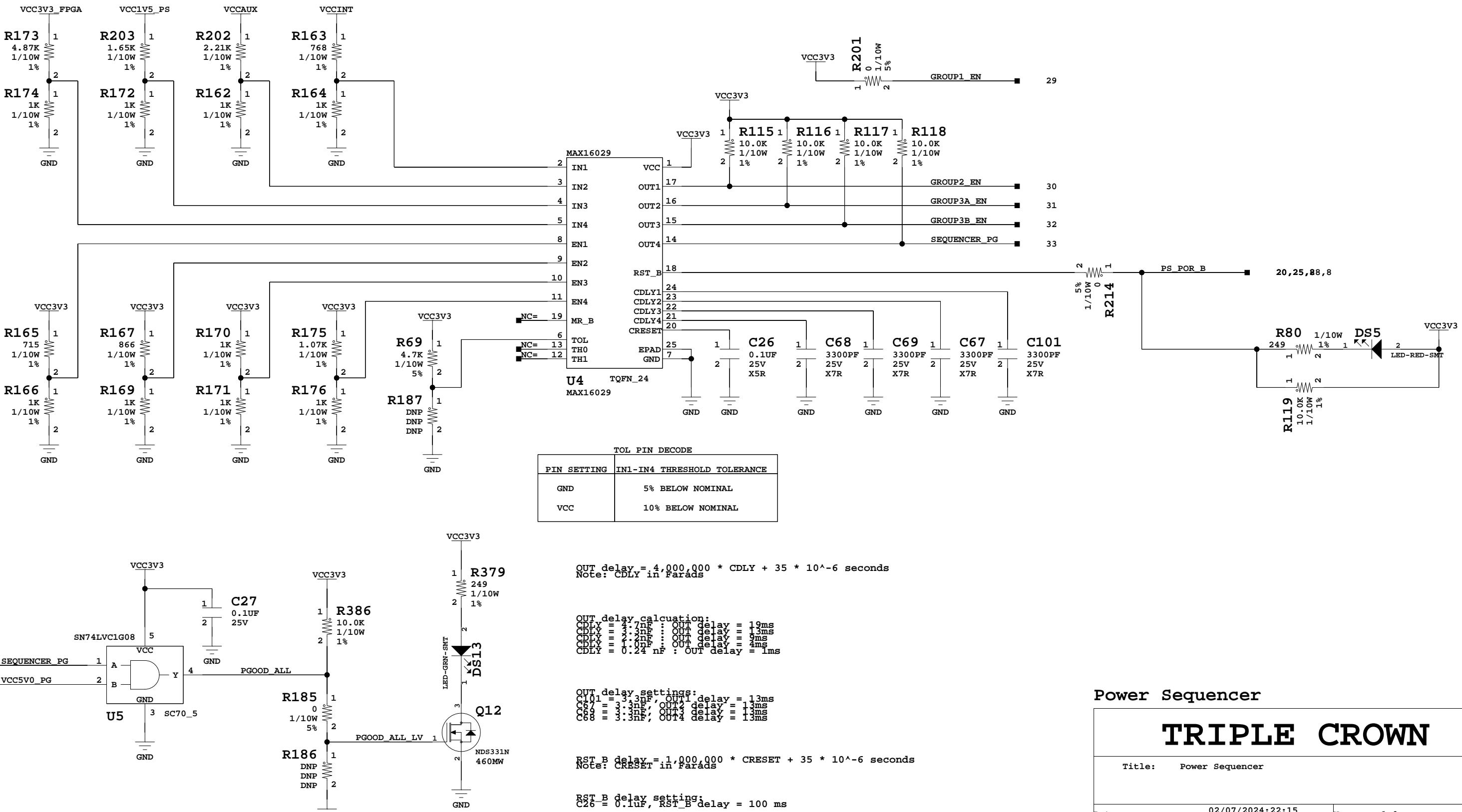
Date: 02/07/2024:22:15	Ver: 1.0
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Power Sequence Order

1. VCCINT (1.0V)
2. VCCAUX (1.8V); VCCPLL (1.8V)
3. VCC1V5 (1.5V); VCC3.3V_FPGA (3.3V), VCC5V0 (5V)



Power Sequencer

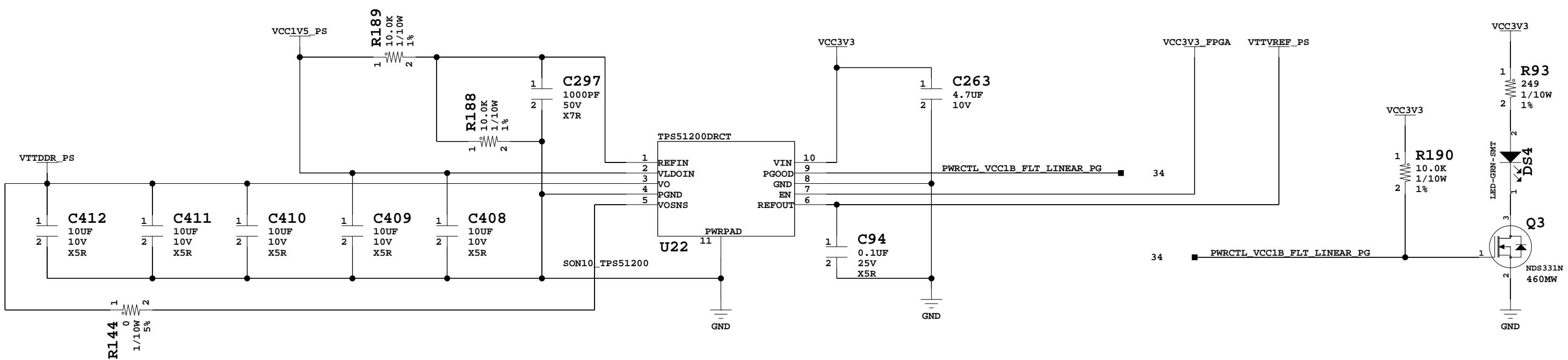
TRIPLE CROWN

Title: Power Sequencer

Date: 02/07/2024:22:15 Ver: 1.0

Sheet Size: B Rev: 01

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Place R144 close to DDR3 device that is farthest from TPS51200DRCT

Linear Power Supplies

TRIPLE CROWN

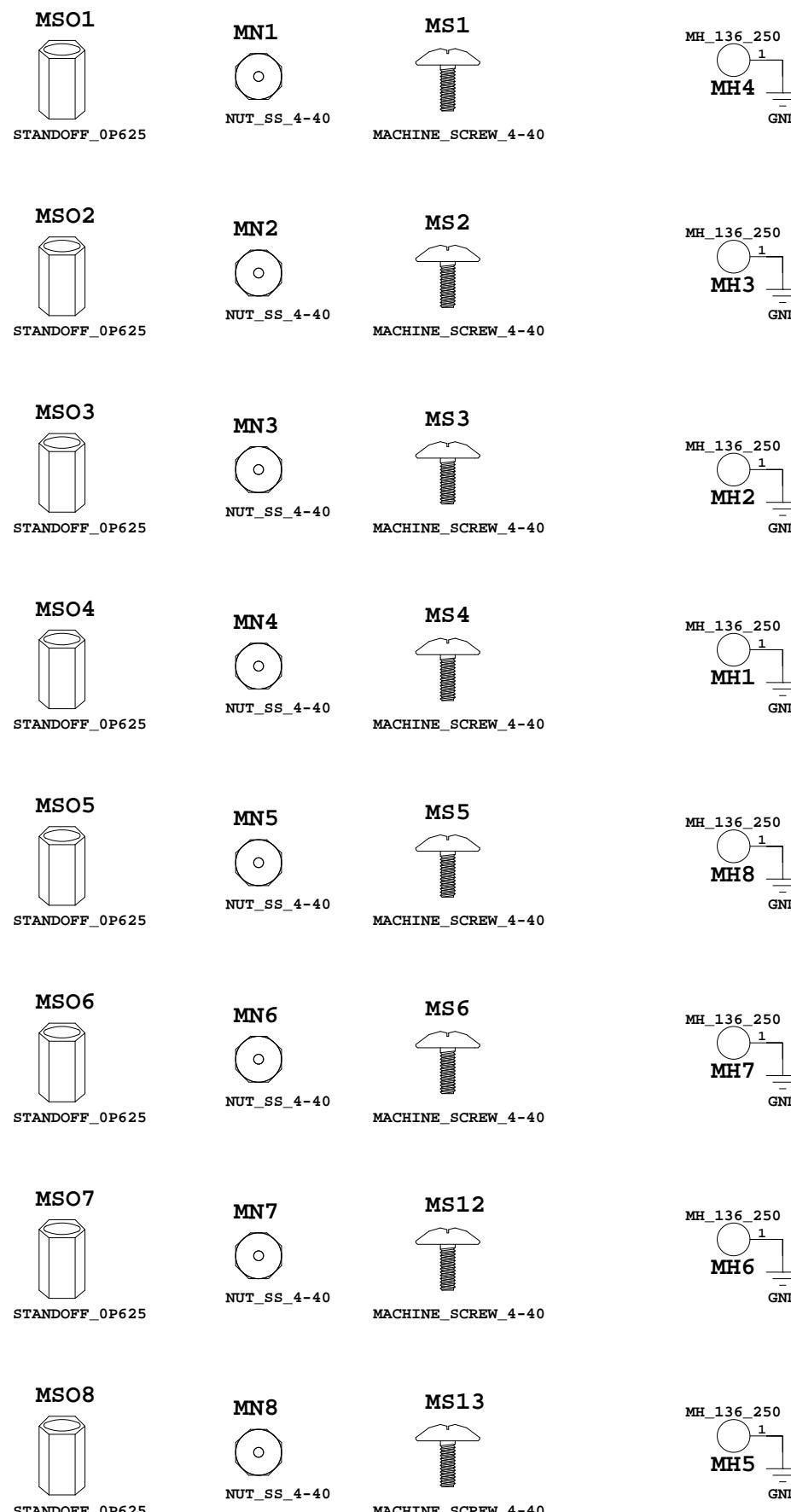
Title: Linear Power Supplies

Date: 02/07/2024:22:15	Ver: 1.0
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Sheet Size: B	Rev: 01
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**Update P/Ns
for
Mechanical Parts**



Mechanical Components

TRIPLE CROWN

Title: Mechanical Components

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Sheet Size:	B	Rev:	01
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