

# Chapter6: Memory unit

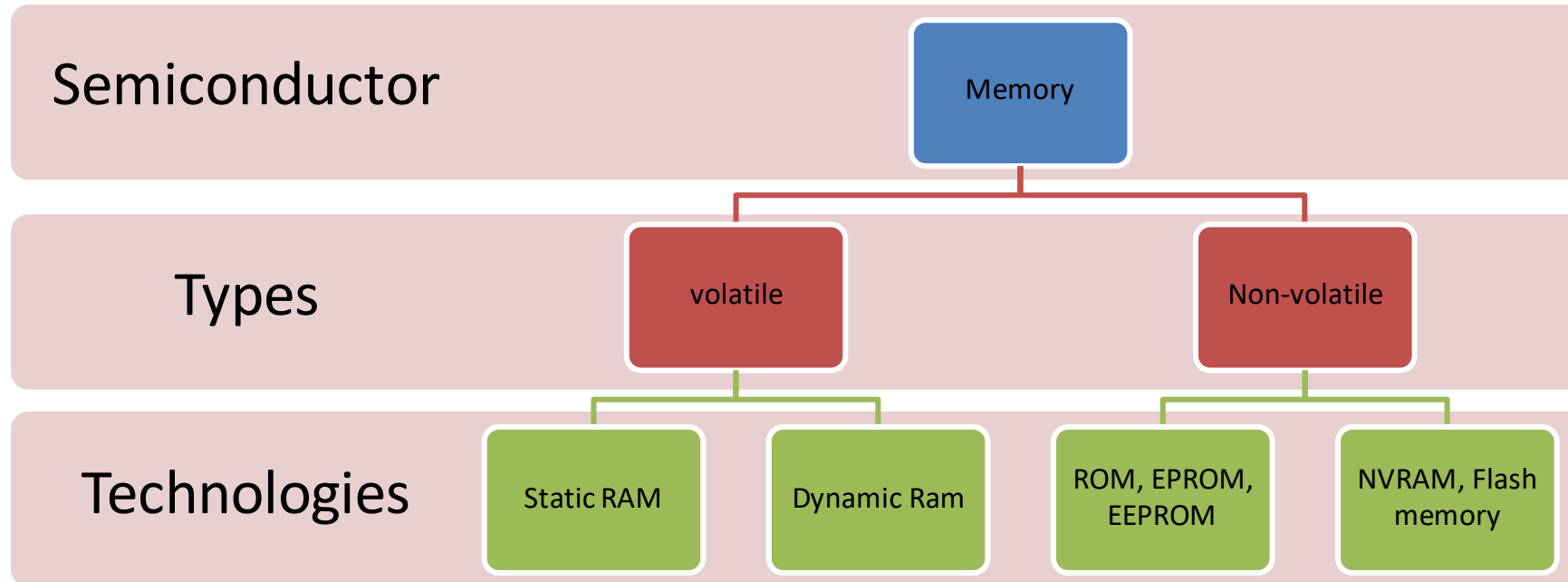
Asst.Prof.Dr.Supakit Nootyaskool



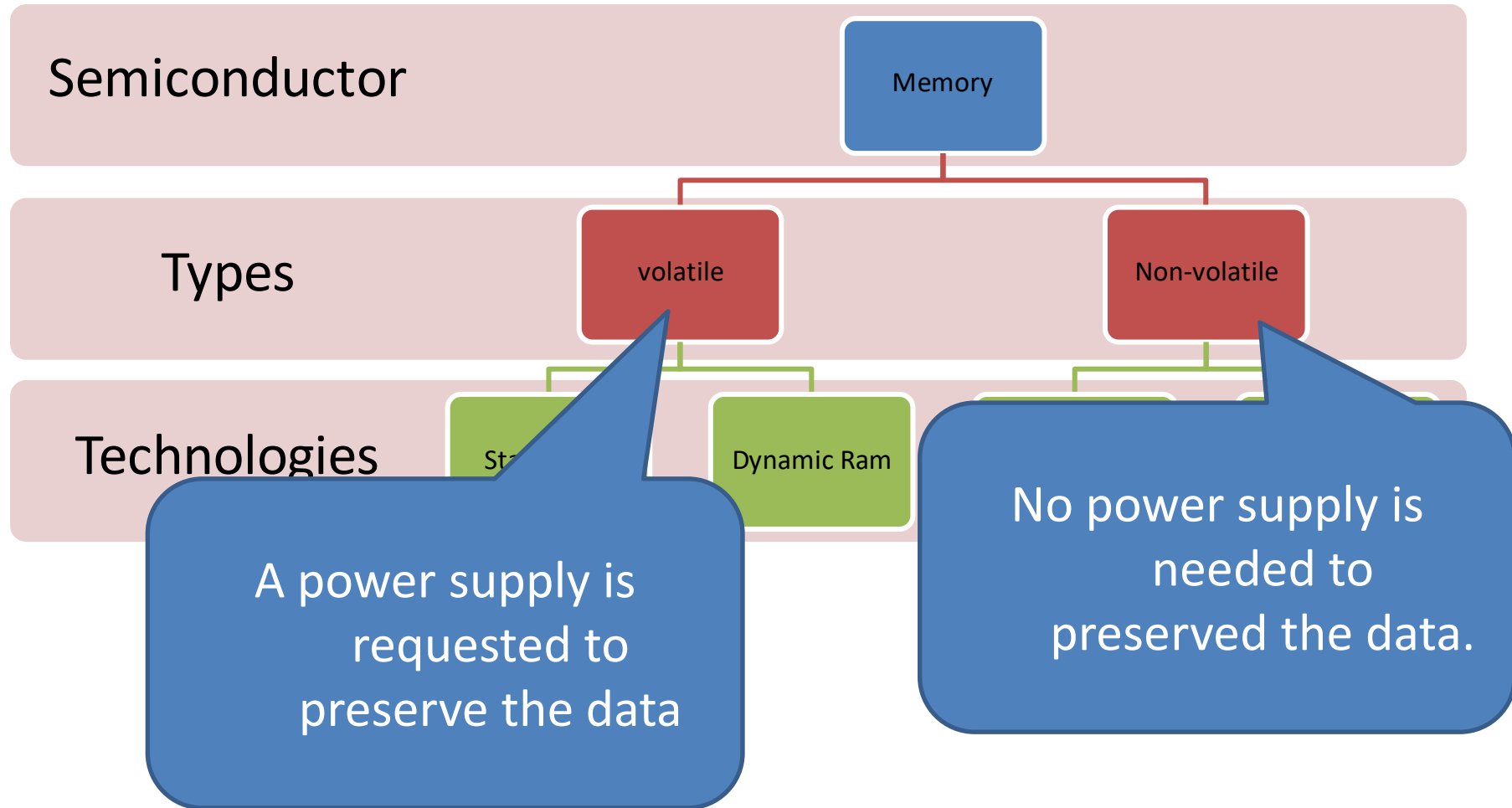
# Objective

- To understand components inside a memory.
- To explain the difference structure of static and dynamic memory.
- To explain the process of reading or writing through the management of the address bus, data bus, and control signals.

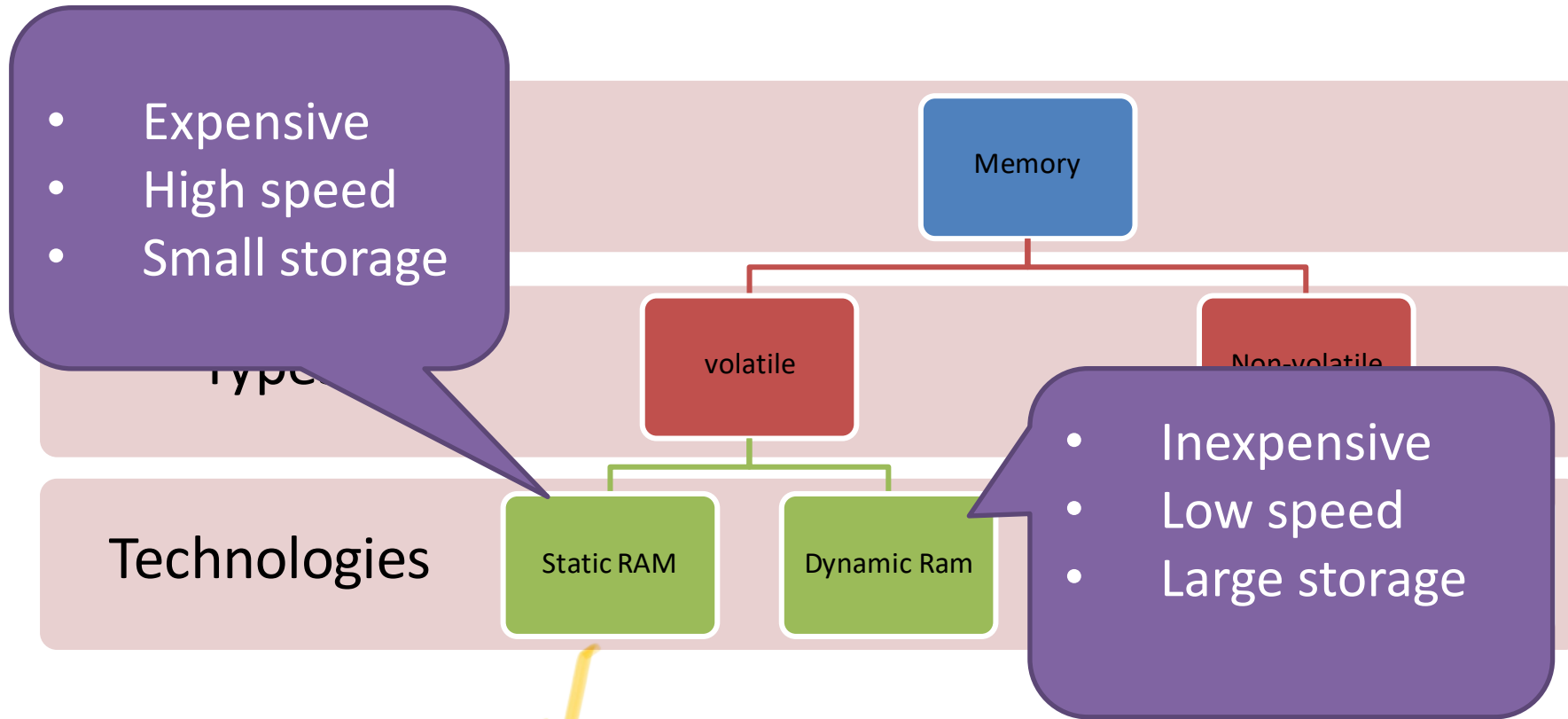
# Memory types



# Memory types





# Memory types

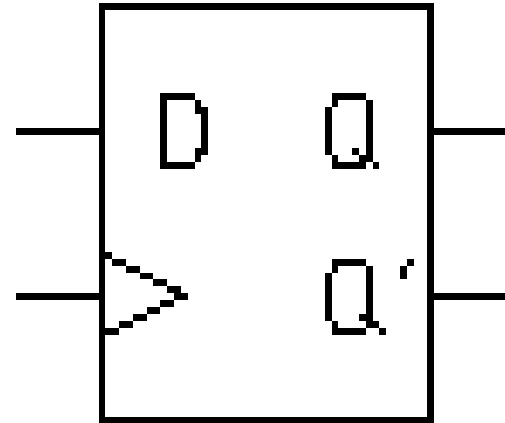


Static RAM is a flip-flop

# Static RAM (SRAM)

- SRAM created from D flip-flop.

D	Clk	Q
0		0
1		1

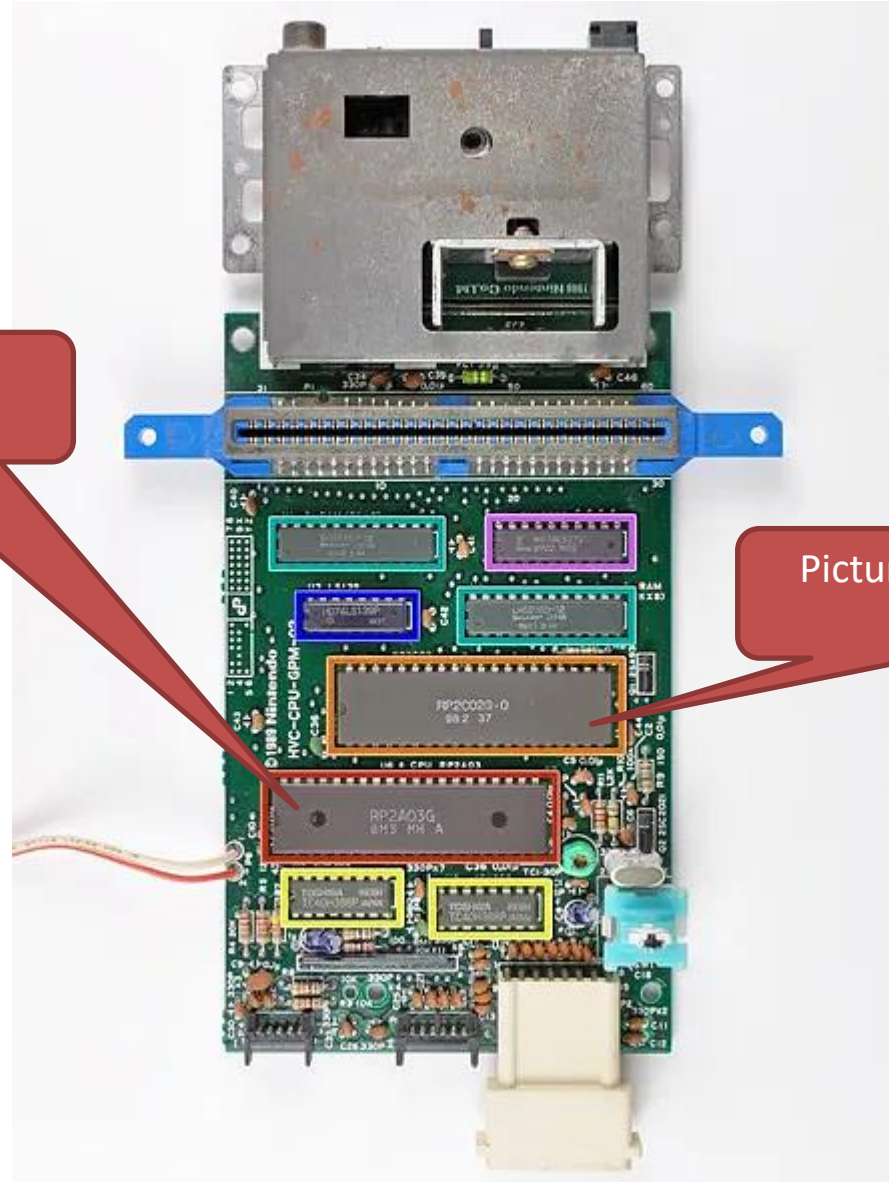
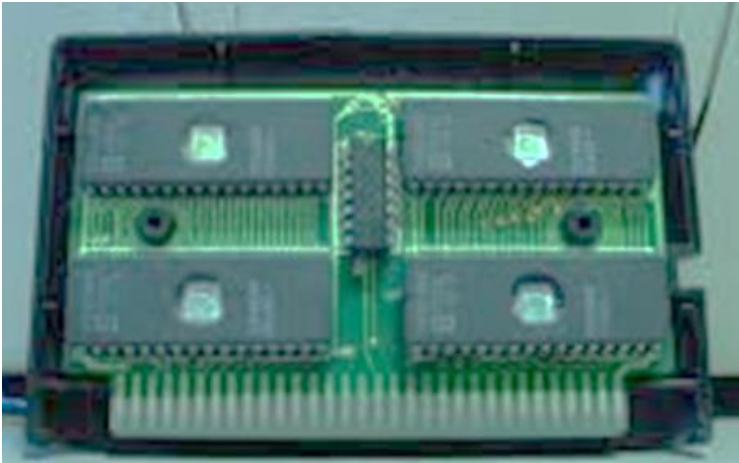


# SRAM and DRAM in Video GAME



8-bit CPU

EPROM



Picture processing  
Unit

# Character representation in ASCII code “A”

41H = 01000001

A

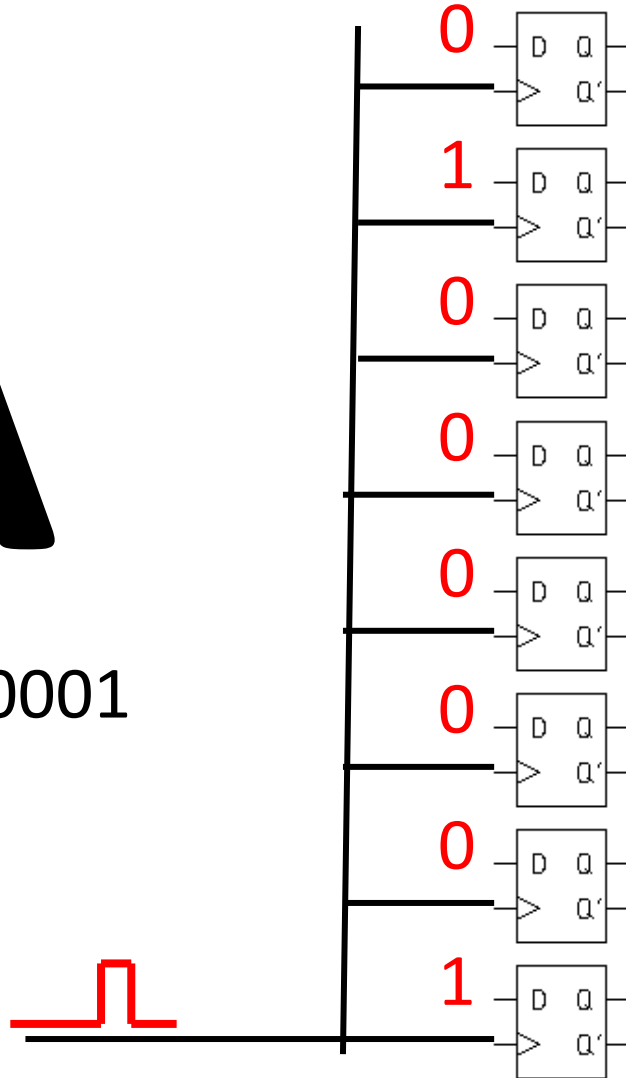
Column → Row↓	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	\$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
10	LF	SUB	*	:	J	Z	j	z
11	VT	ESC	+	;	K	[	k	{
12	FF	FS	,	<	L	\	l	
13	CR	GS	-	=	M	]	m	}
14	SO	RS	.	>	N	^	n	~
15	SI	US	/	?	O	_	o	DEL



# Static RAM keeps “A”

A

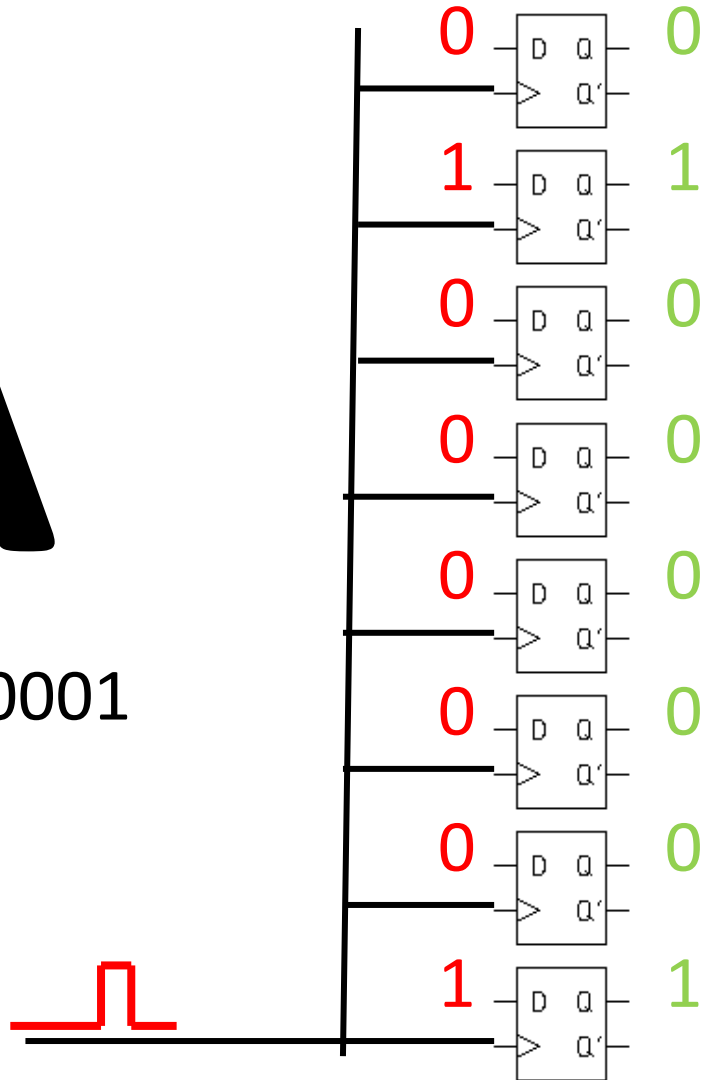
41 = 01000001



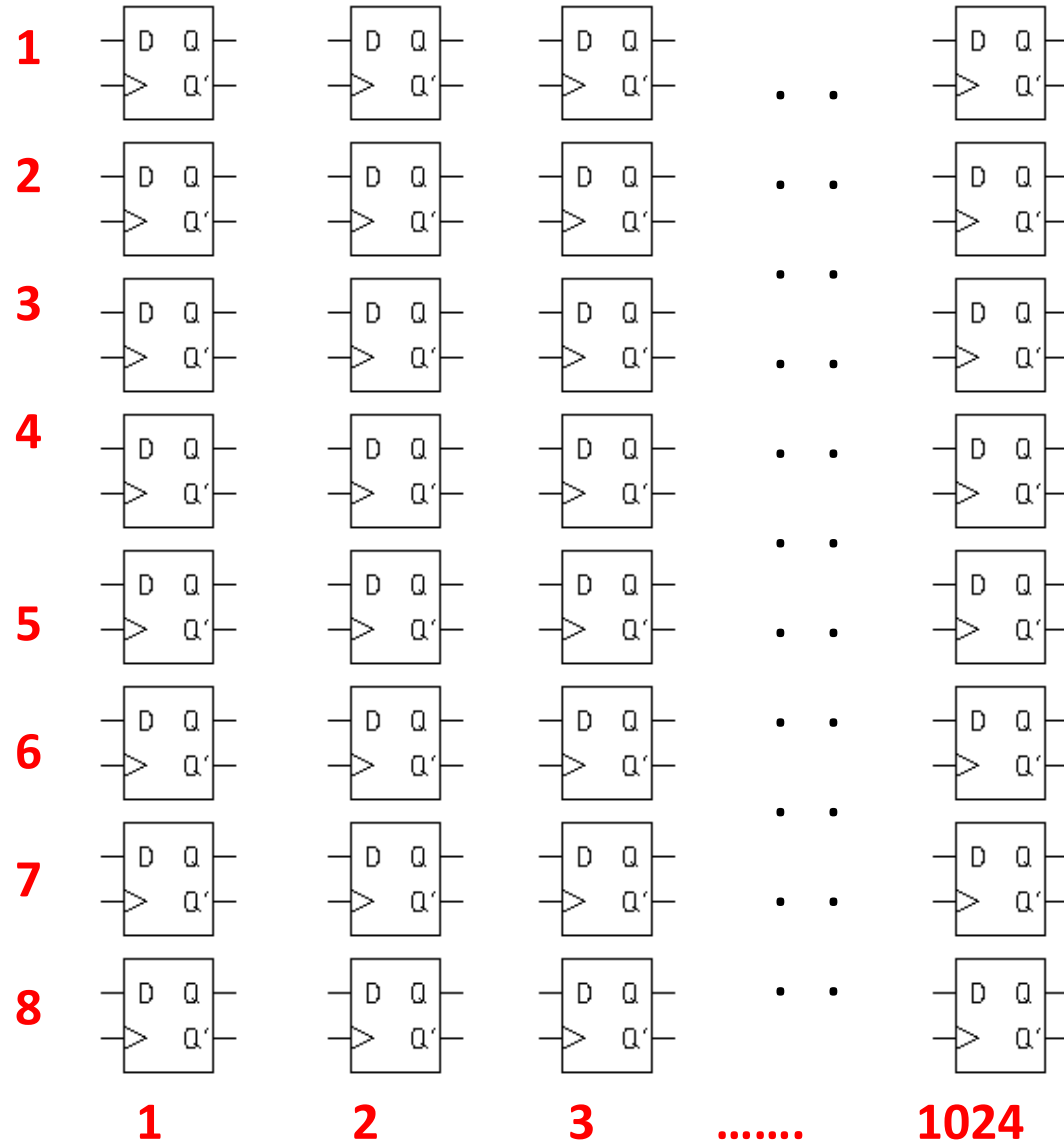
# Static RAM keeps “A”

A

41 = 01000001



# Static RAM



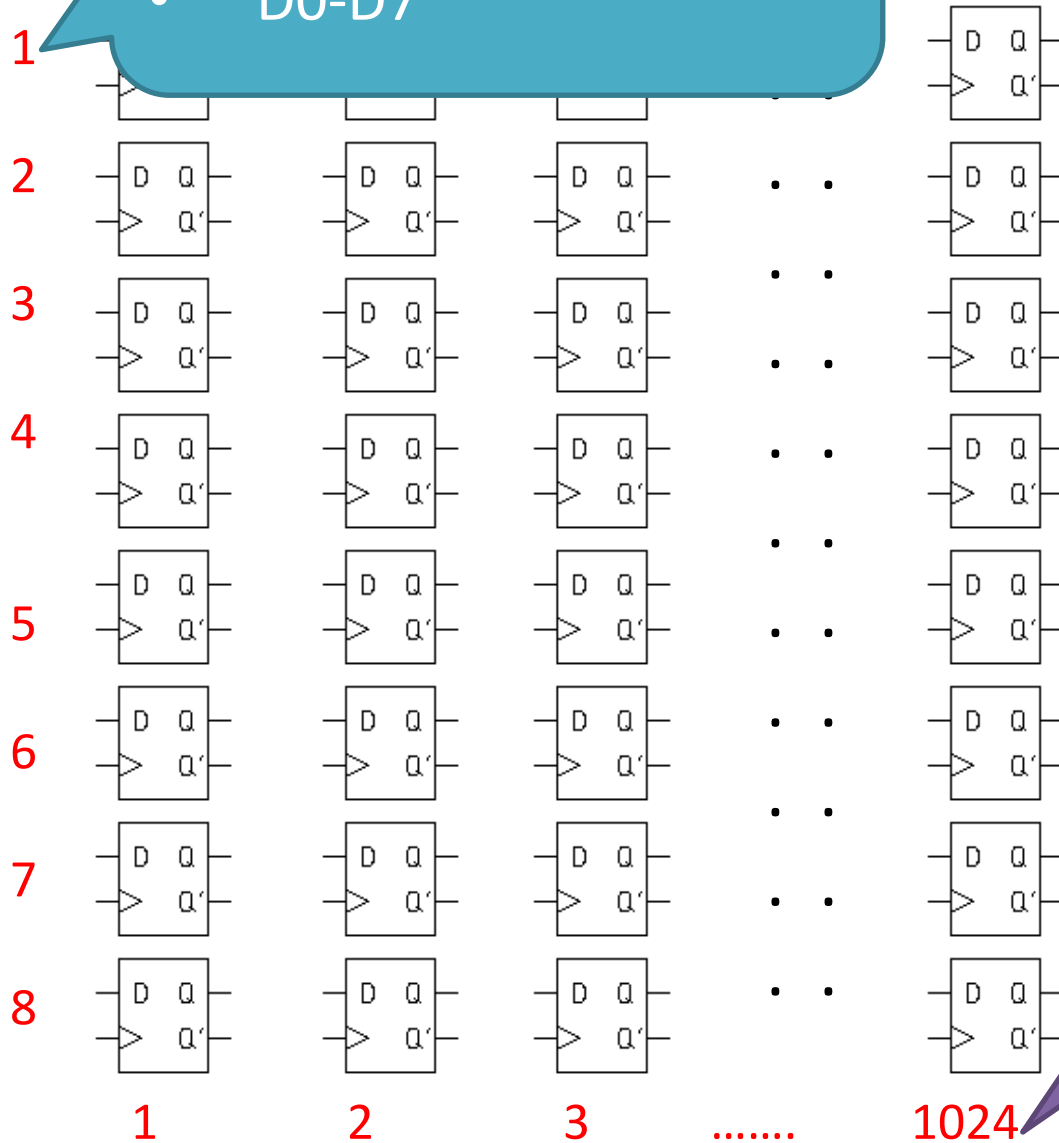
Memory Size

$$8 \times 1024 = 8192 \approx 8K \text{ bit}$$

9 KB

# SRAM

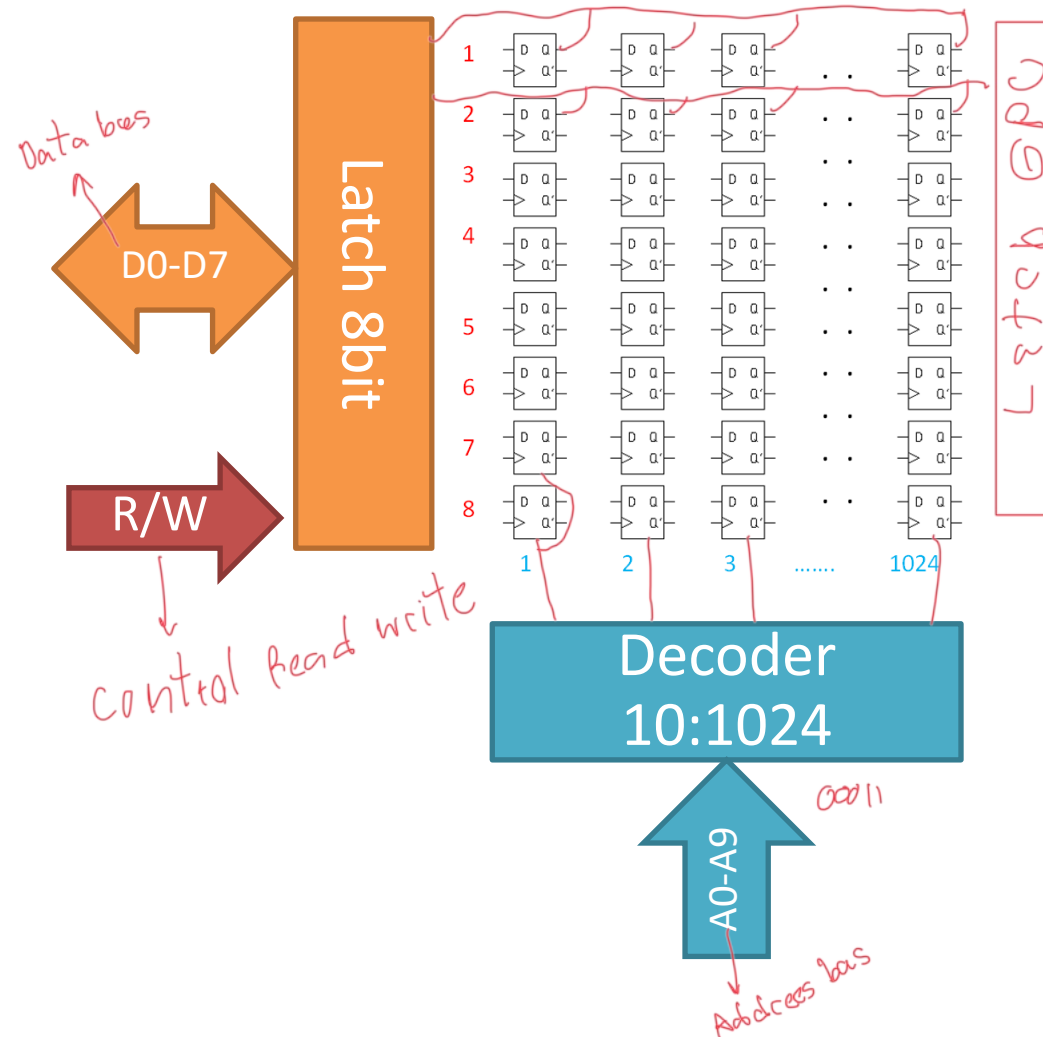
- Data
- 8Bit
- D0-D7



- Address
- 1024 Address =  $2^{10}$
- 1 2 4 8 16 32 64 128 256  
512 = 10Lines (A0-A9)

# Static RAM

Decoder GPU

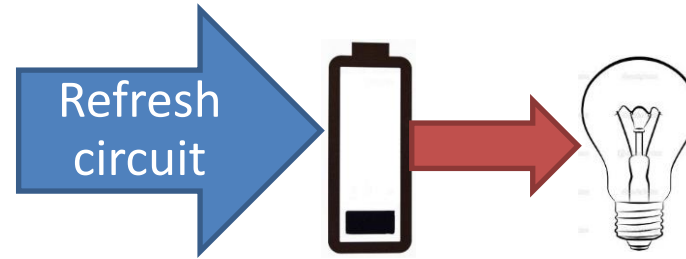


A memory chip has 3 group of pins:

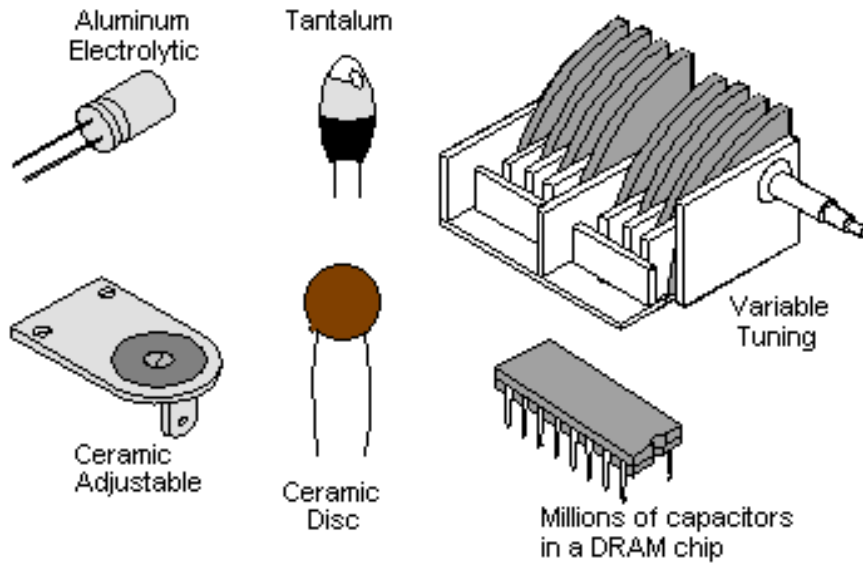
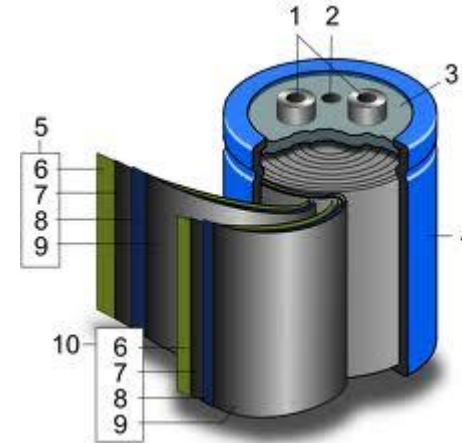
1. The data bus is bi-directional.
2. The address bus functions as an input.
3. Control signals includes read, write, and chip enable.

# Concept of Dynamic RAM

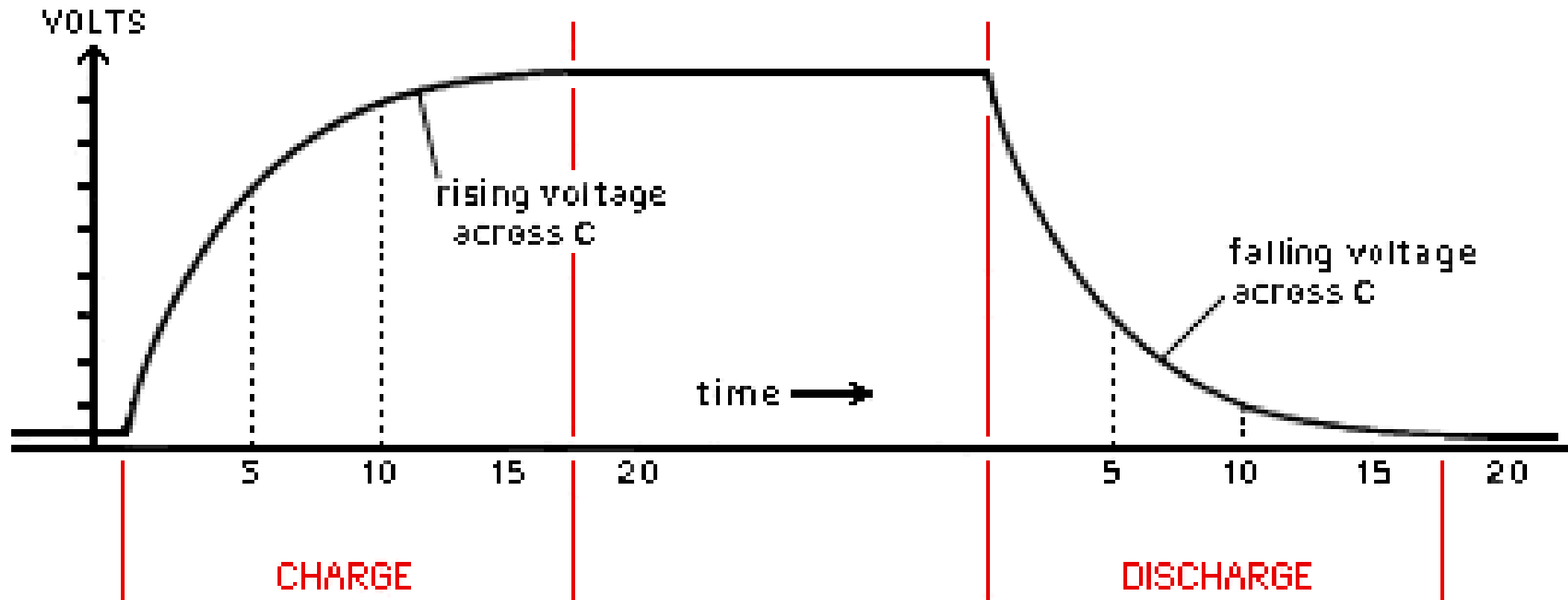
វិធីសាស្ត្រ ចំណាំ ឥតប្រសិទ្ធភាព



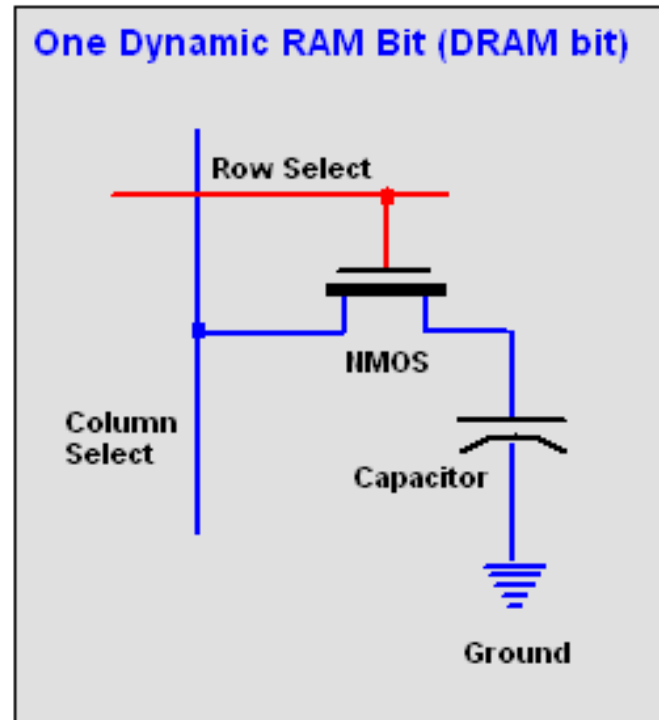
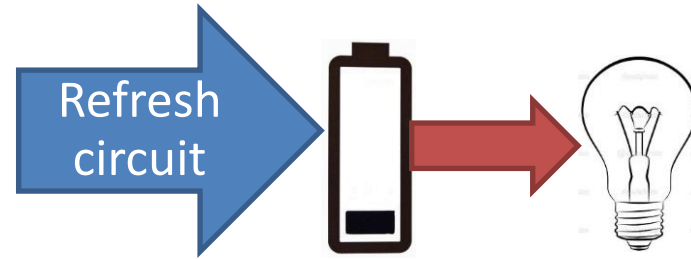
From Computer Desktop Encyclopedia  
© 2004 The Computer Language Co. Inc.



# Charge/Discharge Capacitor

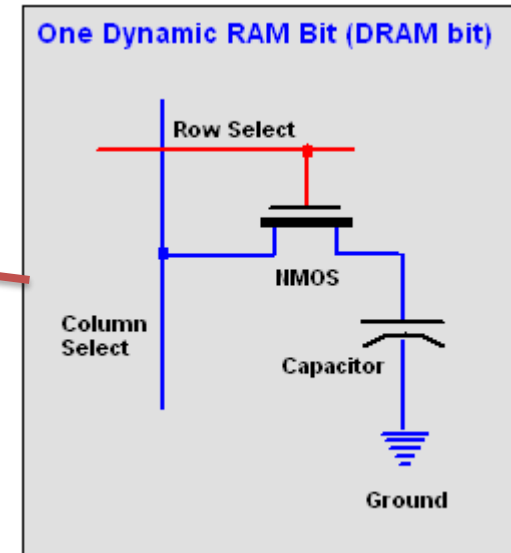
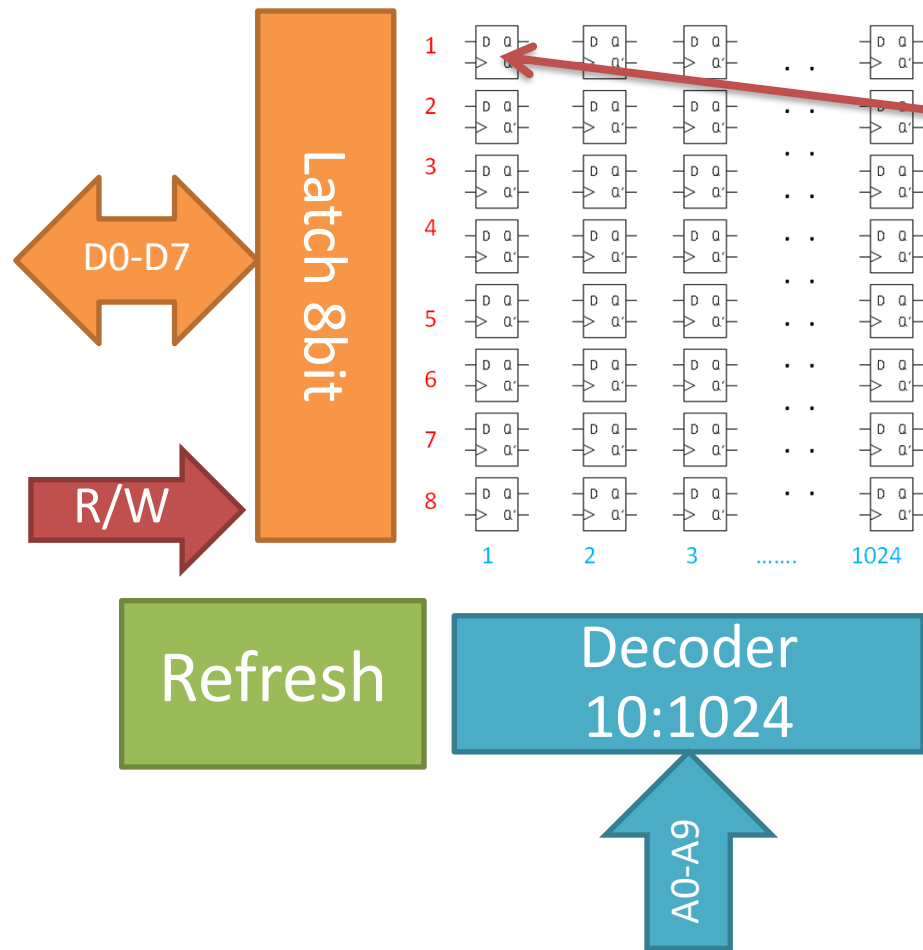


# DRAM

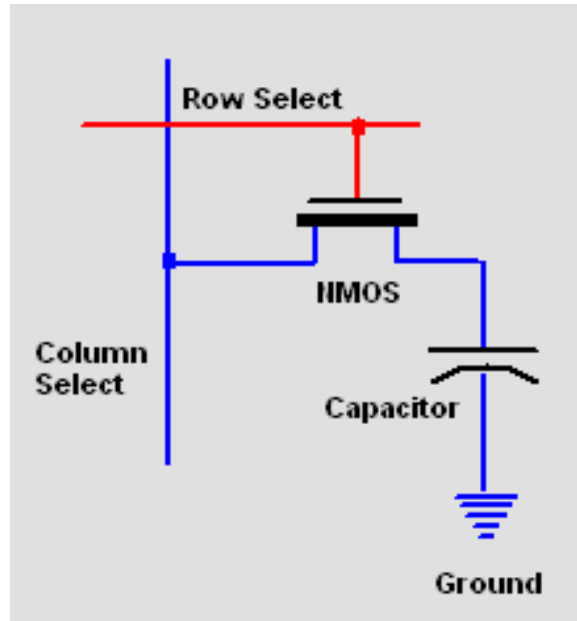




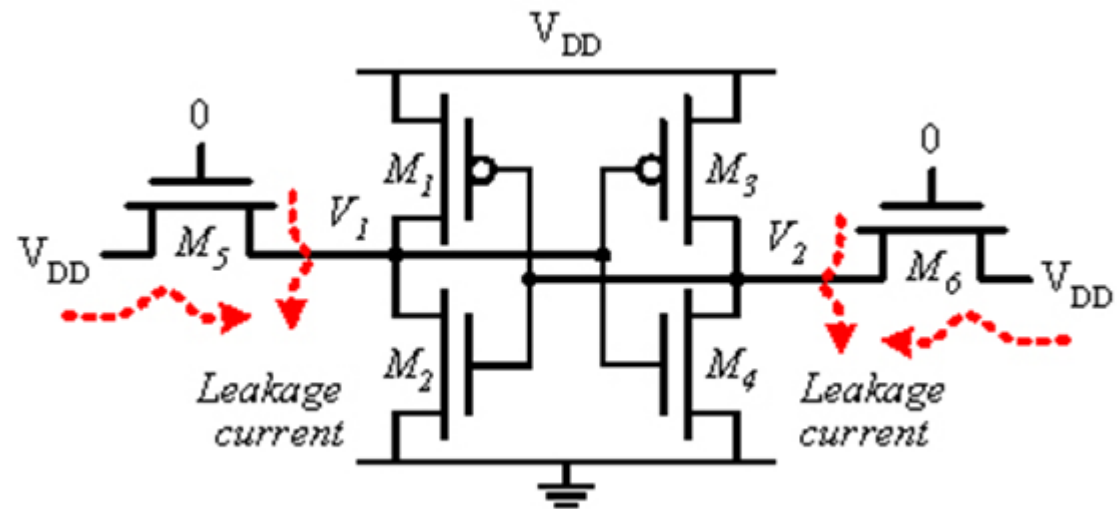
# DRAM



# Comparing structure of memory devices in 1 bit



Dynamic RAM



Static RAM

# Other types

Memory technologies for speed access improvement include:

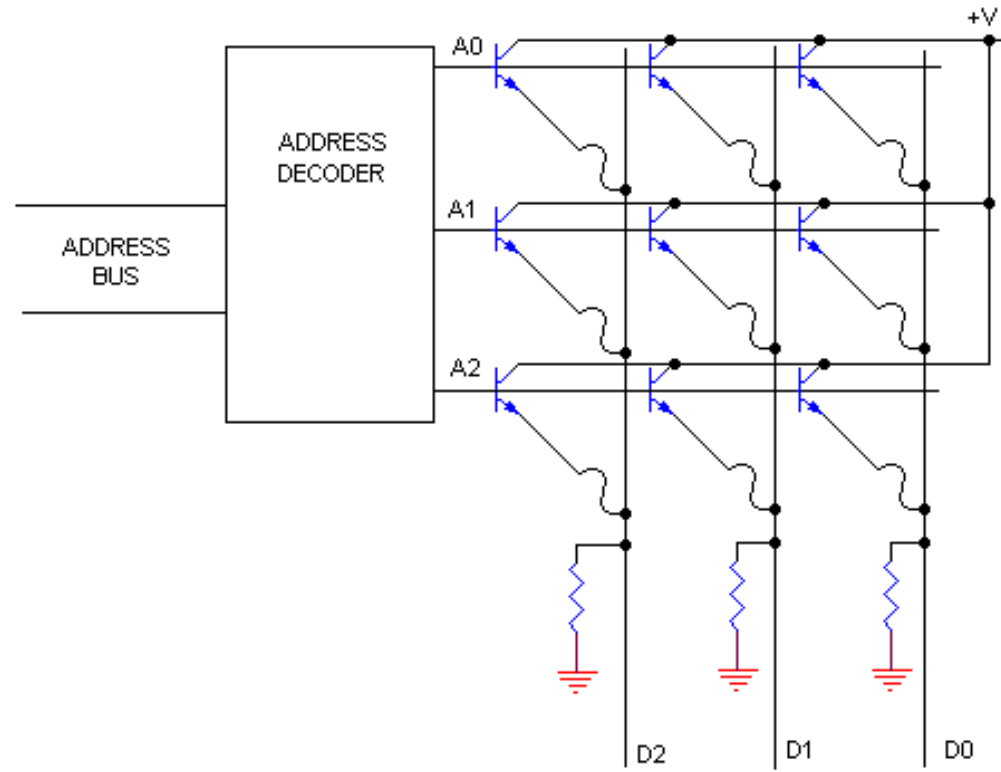
1. EDO DRAM (Extended Data-Out DRAM)
2. SDRAM (Synchronous DRAM)
3. DDR SDRAM (Double Data Rate SDRAM)
4. RDRAM (Rambus DRAM)

Additionally, memory with multiple data buses includes:

1. VRAM (Video RAM)
2. SGRAM (Synchronous Graphics RAM)

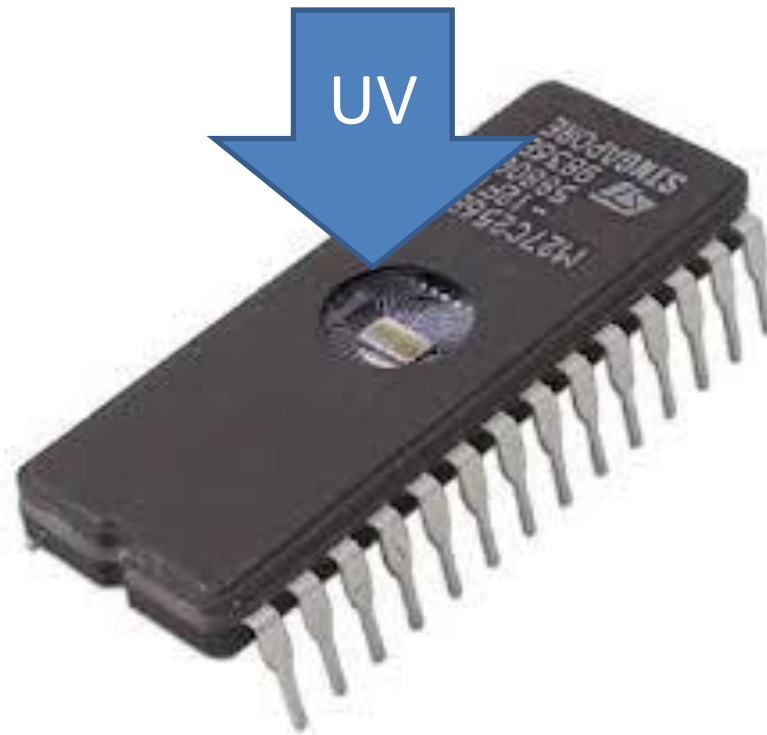
# ROM

- PROM (Programmable read only memory)



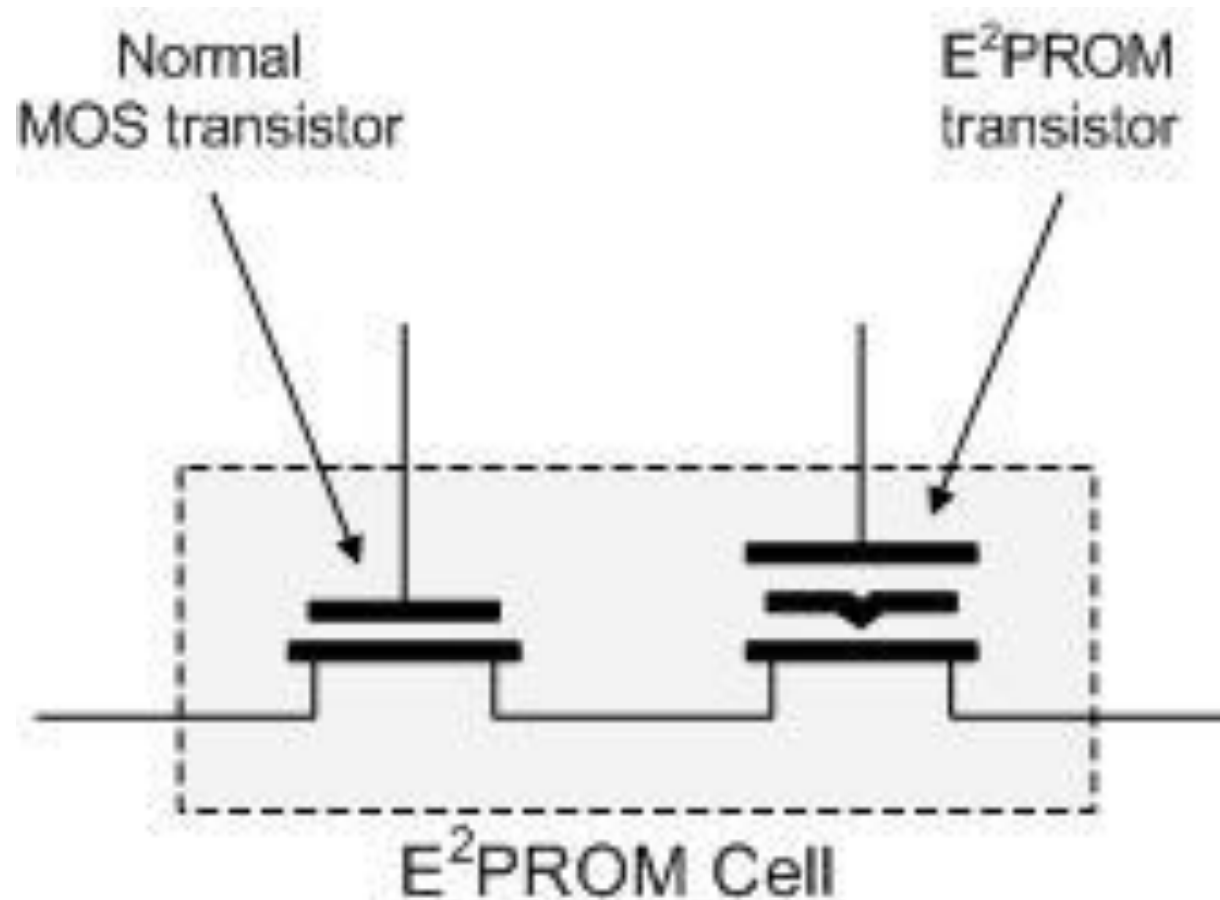
# Read Only Memory (ROM)

- EPROM (Erasable PROM)



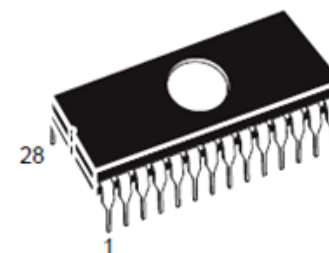
# ROM

- Electrical EPROM (Erasable PROM)



NMOS 64K (8K x 8) UV EPROM

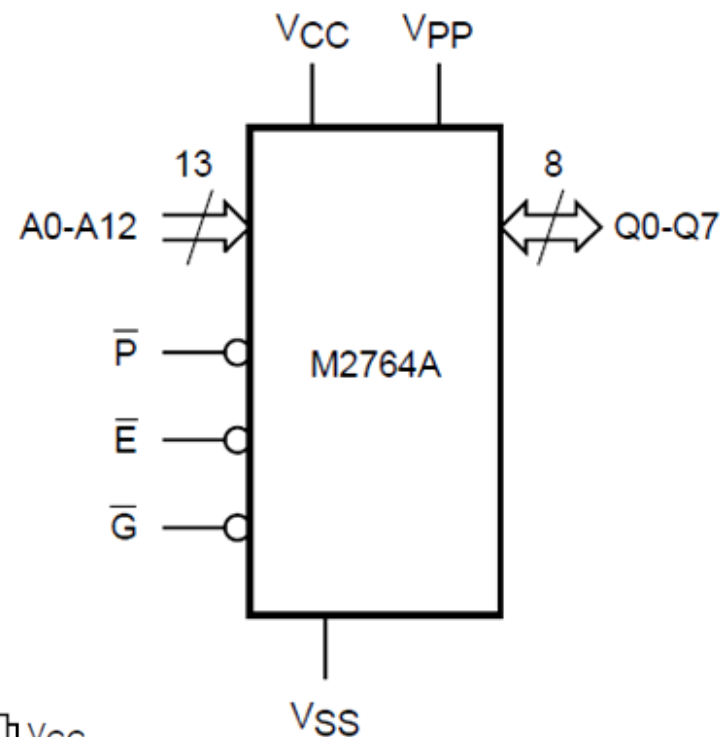
- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



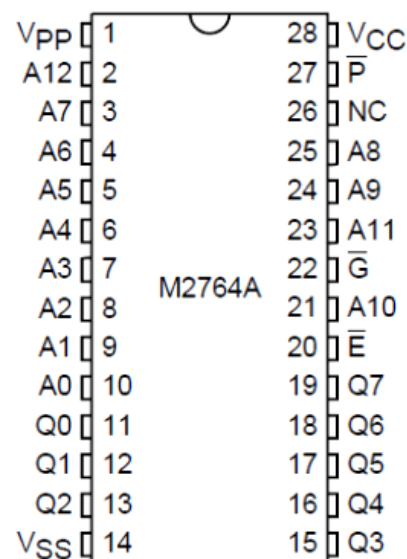
FDIP28W (F)

**Table 1. Signal Names**

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V <sub>PP</sub>	Program Supply
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground



AI00776B

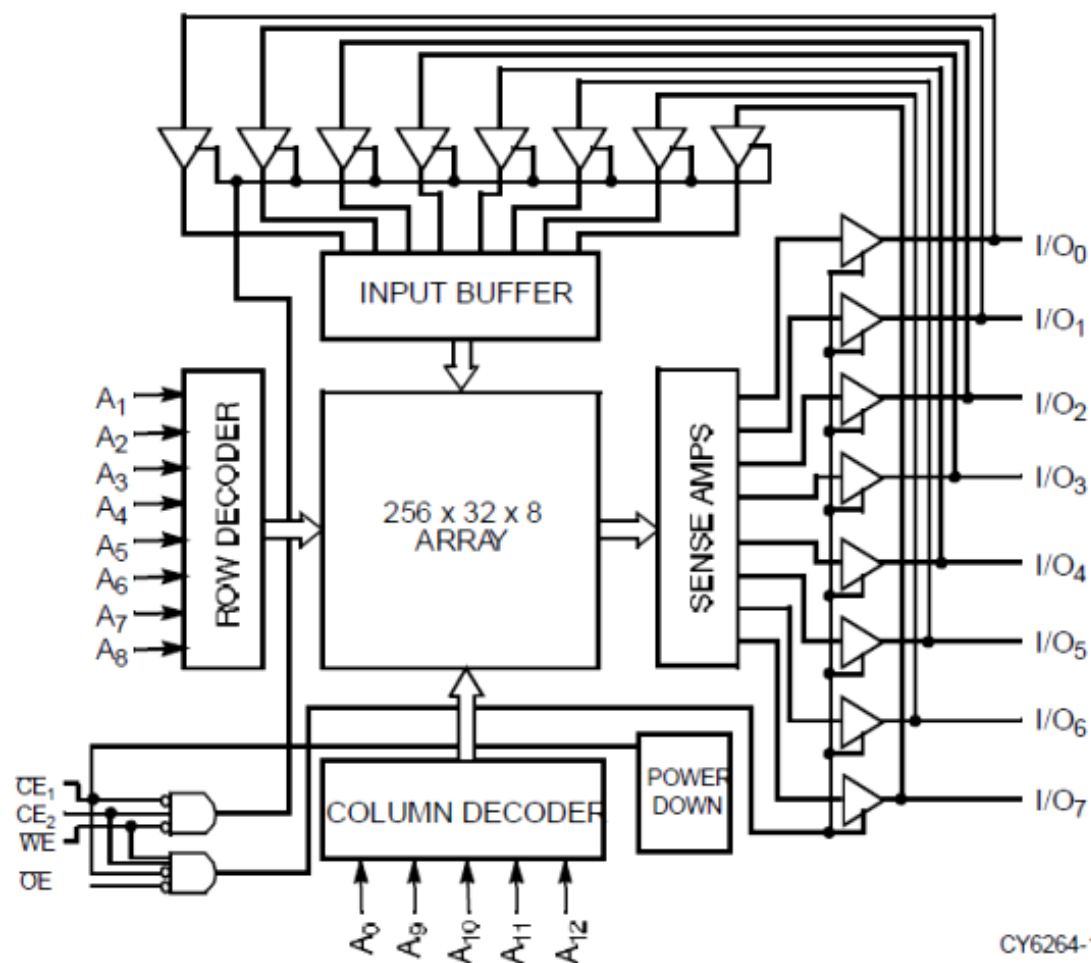


AI00777



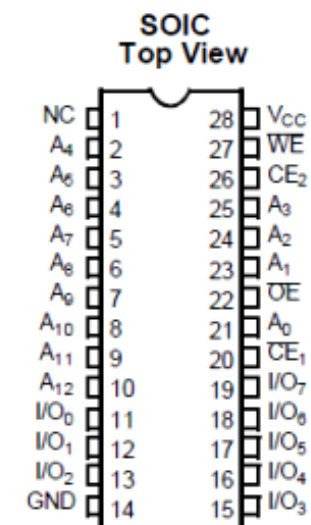
## 8K x 8 Static RAM

Logic Block Diagram



CY6264-1

Pin Configuration



CY6264-2

# Summary