I declare that this piece of work, which is the basis for recognition of achieving learning outcomes in the Digital Circuits (EDC1) course, was completed on my own.

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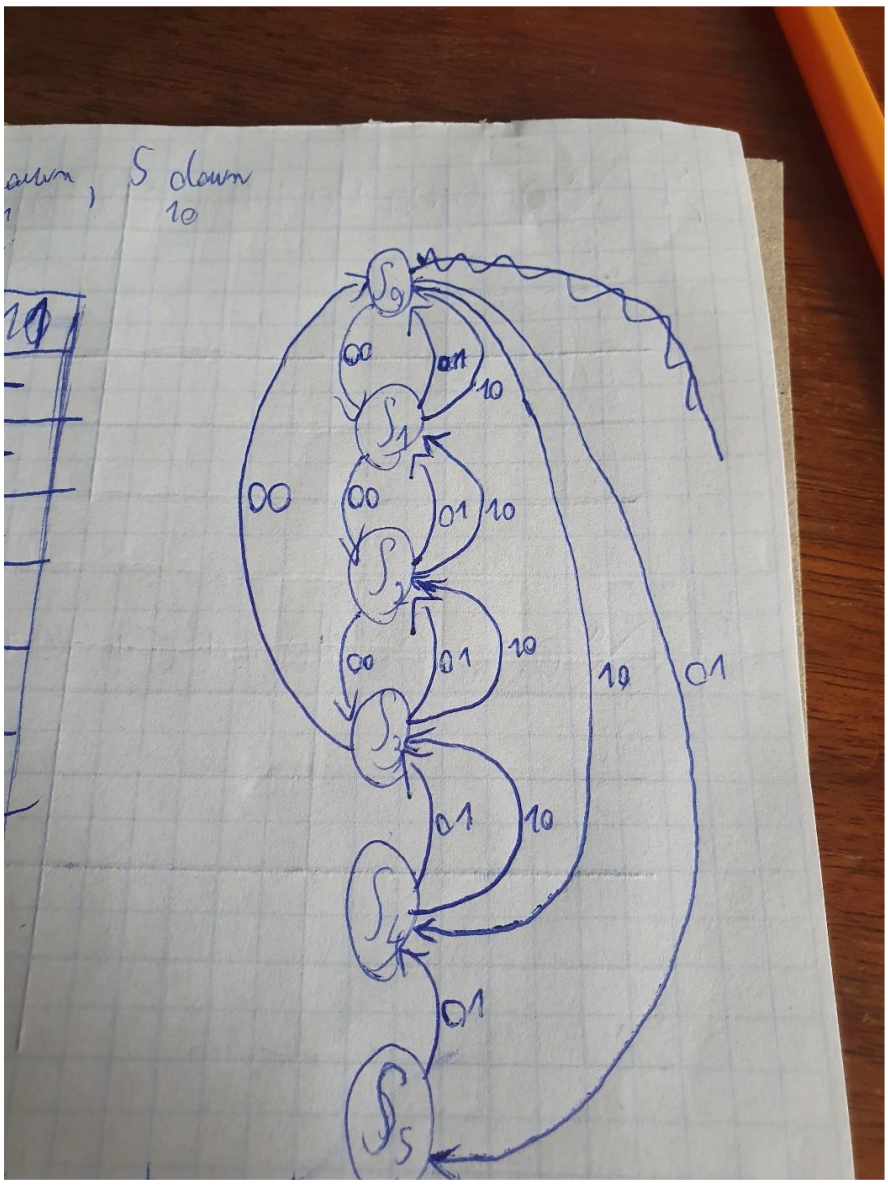
EDC1 – Lab2 report

On this laboratory the task was to design a JK counter that counts with individually given setup for some ab = 00, 01, 10
My setup was: 00: 4 up, 01: 6 down, 10: 5 down.

Theoretical design

First, I did a diagram and state transition tables on paper:



…uanb Balwch 4 up 00, 6 down 01, 5 down 10

…tation

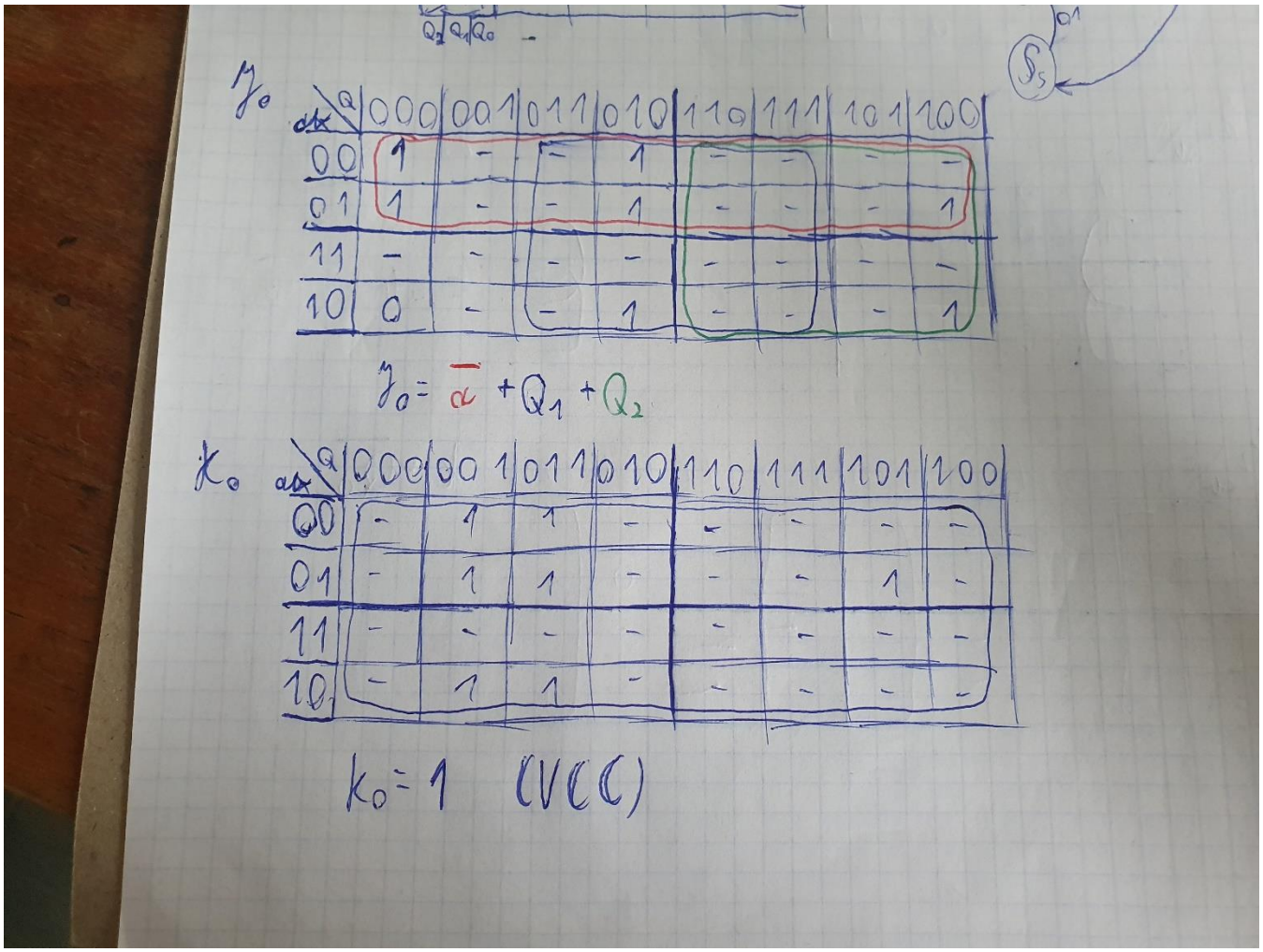
	Q \ a b	00	01	10	11
S_0	000	001	101	100	–
S_1	001	010	000	000	–
S_2	010	011	001	001	–
S_3	011	000	010	010	–
S_4	100	–	011	011	–
S_5	101	–	100	–	–
	~~110~~	–	–	–	–
	~~111~~	–	–	–	–

$Q_2 | Q_1 | Q_0$

From that, I started making JK Karnaugh maps. I've used JK state transition table and then transcoded the values into the K-maps. This is the JK state transition table:

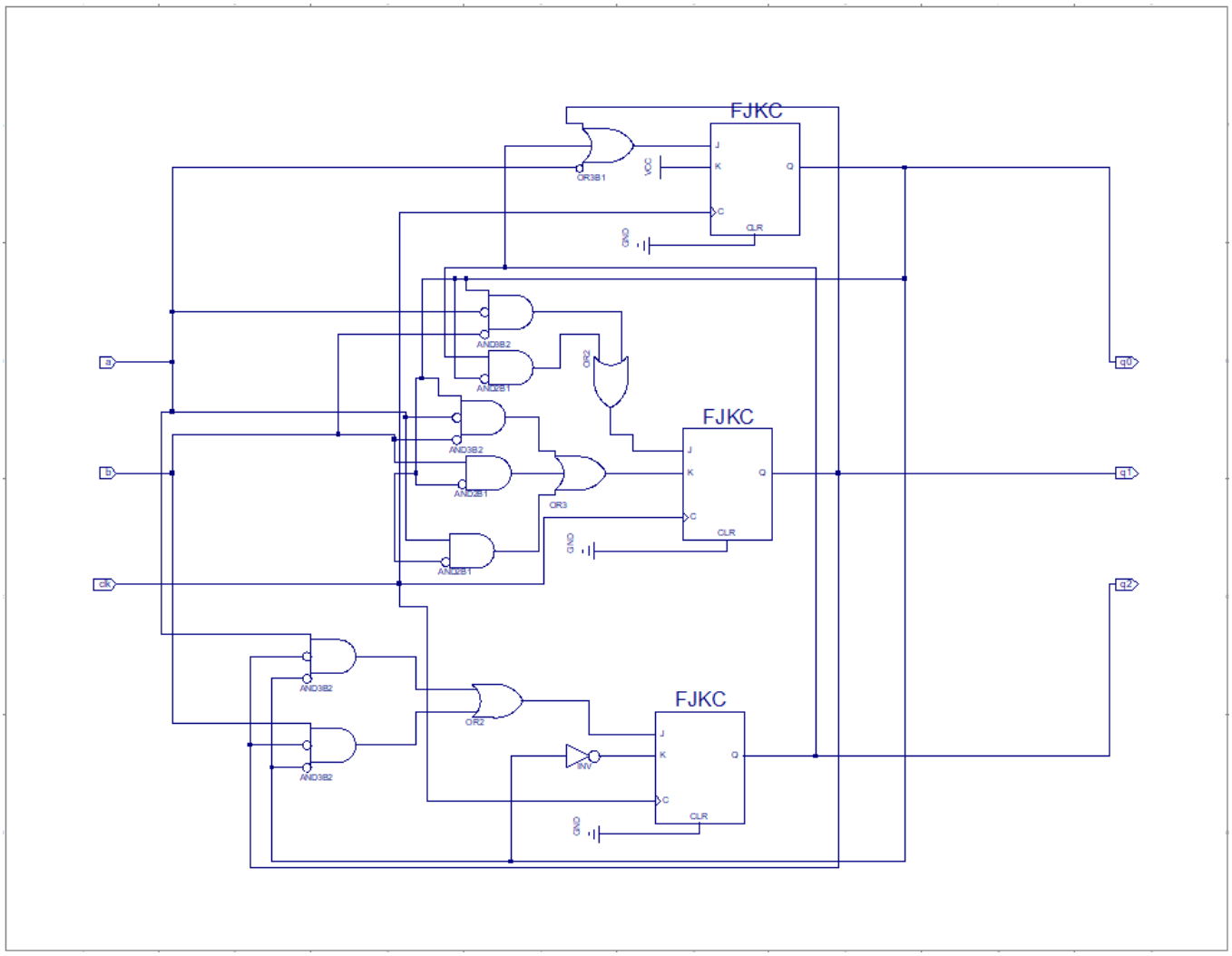
Present	Next	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

And these are the solved JK K-maps (obtained from transcoding) for the logic circuit:



(note: incorrect simplification has been discarded and is crossed out with red line)

After that, I put the circuit in Xilinx ISE. I got all the needed J0, K0, J1 etc. values. I create a schematic will all necessary connections, devices etc.:



Schematic file was provided in the .zip file sent at the end of laboratory (as well with testbench)

After making the schematic, I did a simple vhdl testbench file. Here is a snippet of the code:

```
SIGNAL q2  :     STD_LOGIC;
   SIGNAL q1     :     STD_LOGIC;
   SIGNAL q0     :     STD_LOGIC;
   SIGNAL clk    :     STD_LOGIC := '0';
   SIGNAL b      :     STD_LOGIC;
   SIGNAL a      :     STD_LOGIC;
[…]
```

```
   clk <= not clk after 15 ns;
tb : PROCESS
BEGIN
        a <= '0';
        b <= '0';
        WAIT FOR 225 ns;
        a <= '0';
        b <= '1';
        WAIT FOR 370 ns;
        a <= '1';
        b <= '0';
   WAIT; -- will wait forever
END PROCESS;
```

I timed the waits so that the modes when switched don't overlap with previous counting modes (see simulation screenshot).

Here is the obtained simulation from the VHDL testbench file. Note that work (colouring, virtual BUS, radix conversion) has been done to the output waveforms so that the simulation results can be read easier and clear:

From the simulation results, it can be seen that the behaviour shown in the simulation matches with the behaviour defined by the laboratory task. For 00 the counter counts 0,1,2,3 (4 up), for 01: 0,5,4,3,2,1 (6 down), and for 10: 0,4,3,2,1 (5 down). The laboratory was done successfully.