Max Score = 15 points

CS 250 2018 Spring Homework 04 SOLUTION & GRADING GUIDE

This assignment is due at 11:59:00 pm Thursday, February 15, 2018.

Upload your typewritten answer document in either PDF or Word format to Blackboard. Download from Blackboard to be sure that your upload was successful. Your last upload that is not marked "LATE" by Blackboard is the upload that will be graded. There is no "grace" period for late uploads.

1. If the bit string 0xC0E80000 stored in computer memory is interpreted according to the IEEE 754 floating point format for single precision, what is the equivalent base 10 number in normalized scientific format?

   Show each step of the conversion process starting with the machine stored bit string (display in groups of 4 bits with spaces); the three bit string fields s|E|M separated by spaces and including the hidden bit, the decimal value of the actual exponent, the value in base 2 scientific number format, the binary point shift necessary for conversion, the conversion to base 10, and the final normalization of the base 10 scientific format number.

   Answer: Writing out the bit string represented by 0xC0E80000 we have 0b1100 0000 1110 1000 0000 0000 0000 0000. Separating this into the fields of the format, 0b 1 10000001 **1.**110 1000 0000 0000 0000 0000 where the boldface font shows the hidden 1. Interpreting this bit string gives sign = 1 meaning a negative number; biased exponent = 10000001 = 129, so actual exponent = 129 - 127 = 2; and the significant mantissa bits (bits that affect the value represented) are 1.1101. So, we have
   -1.1101×2^{2} $= -111.01 \times 2^{0}$; ÷ by 2^{2} multiplied mantissa by 2^{2} so value unchanged.
   $= -7.25 \times 10^{0}$; 111. = 7. and $0.01 = 1 \times 2^{-1} = 0.25$ and $2^{0} = 10^{0}$.
   $= -7.25 \times 10^{0}$; result is in decimal scientific normalized form

2. **[3 points; 1 point for showing 11.125×2^{0} intermediate step; 1 point for showing 1.011001×2^{3} intermediate step; and 1 point for the final answer bit string in hexadecimal notation; all shown in bold]** Convert 1.1125×10^{1} to its corresponding bit string for the IEEE floating point format in single precision and write that result in hexadecimal notation.

   Show each step of the process: adjust to zero exponent in base 10; convert integer and fractional part to base 2 and exponent radix to 2; normalize mantissa binary point; determine sign, biased exponent, and mantissa fields of IEEE format; write out the bit string showing the three fields s|E|M with a space separating each field; re-write bit string in groups of 4 bits; write bit string in hexadecimal notation.

   Answer: Adjust the given 1.1125×10^{1} to have a zero exponent.
   1.1125×10^{1} $= 11.125 \times 10^{0}$; reduce exponent to 0, mantissa x10, no change
   $= \mathbf{1011.001 \times 2^{0}}$; convert to base 2 representation
   $= \mathbf{1.011001 \times 2^{3}}$; divide mantissa by 8, add 3 to exponent
   IEEE format components are: sign = 0, biased exponent = 3 + 127 = 130 = 10000010, and mantissa after hidden bit is removed = 0110 0100 0000 0000 0000 000. Thus, the bit string

is
0 10000010 01100100000000000000000 and then grouped by every 4 bits is
0100 0001 0011 0010 0000 0000 0000 0000 which in hexadecimal notation is
0x41320000.

3. **[6 points; 2for the answer to each part as shown in bold]** A computer has 16 registers that can supply operand bit strings to the computational circuits of the processor. For this computer all operands are 32 bits in size. Answer the following questions about a multiplexer that provides a path for data (bit strings) in the registers to reach the computational circuits (arithmetic/logic unit) of the processor.
   a. How many address bits are needed to have a multiplexer select one of the registers to provide an operand bit string?
   Answer: $16 = 2^4$ therefore **4 address bits** are needed to enable the mux to point to each register.

   b. How many input data buses does this multiplexer have?
   Answer: 16

   c. How many data input wires does this multiplexer have?
   Answer: 16 buses x 32 wires/bus = 2^4 buses x 2^5 wires = 2^9 wires = **512 data input wires**.

4. What is the name of the signal that tells a register that it is time to pay attention to its inputs?
Answer: The clock.

5. **[3 points, 2 points for Von Neumann, 1 point for Harvard]** What are the two principal computer organizational designs and how do they differ in memory organization and flexibility?
Answer: The two principal organizations are the Harvard Architecture and the Von Neumann Architecture. The architectures differ in memory organization. The Harvard design has two memory units, one for program instructions and one for program data. The Von Neumann design has a unified memory unit that stores both program instructions and program data. Because the Von Neumann architecture unifies all memory, it offers total flexibility to use memory to store program instructions or program data in whatever ratio is desired.

6. **[3 points for two or more issues]** The set of operations that a processor provides represents a tradeoff among what sorts of issues?
Answer: Issues such as cost of the processor hardware, convenience for a programmer, and engineering considerations such as power consumption.