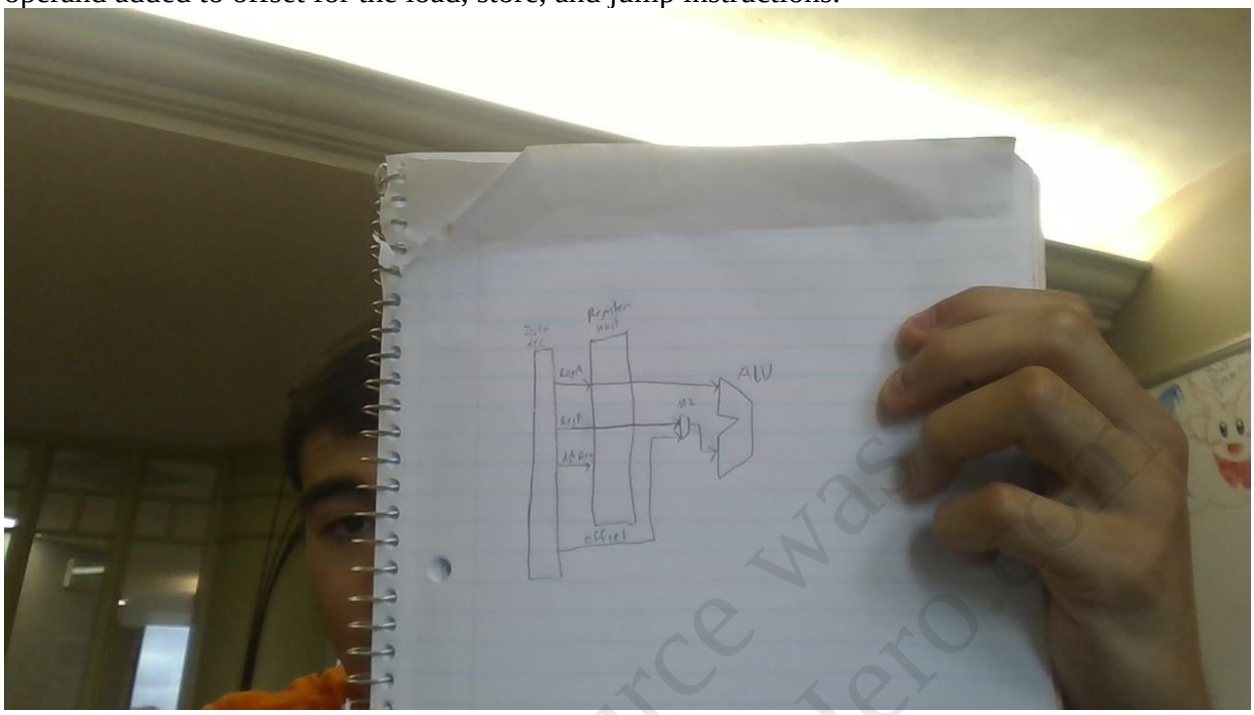
CS 250 Fall 2017 Homework 05
Due 11:58pm Thursday, Oct. 05, 2017
Submit your typewritten file in PDF format to Blackboard.

1. Refer to textbook Figure 5.9.
    a. Name an instruction that strongly implies that a register can hold a binary string that is interpreted as a 2's complement integer. **ADD**
    b. Name an instruction that shows a register can also hold a meaningless binary string. **MOVE FROM COPROCESSOR**
    c. Name an instruction that overrides the work of the circuit in Figure 6.4. **JUMP**
    d. Name the instruction that corresponds to the C language code *if(a == b){ }*. Assume that the values of a and b are held in registers. **BRANCH EQUAL**
    e. How many bits are necessary for the opcode field for the instructions in Figure 5.9? **5 BITS = 32 INSTRUCTIONS**

2. Modify Figure 6.2 to support a re-design of the processor of Chapter 6 with 32 general purpose registers. What significant negative impact does this change have on the expressiveness of the ISA?
Instead of 3 operands have 2 operands, which greatly increases how many instructions are needed in order to do certain tasks.

3. Consult Figure 6.3 and show each bit of the instruction **load r7, 43(r15)**.
00010|1111|0101|0111|000000000101011
4. Why is the instruction from Chapter 6, **jump 40000(r15),** invalid?
THE OFFSET ONLY HAS A MAX VALUE OF 32768 IN UNSIGNED INTEGER. 40000 > 2^15
5. Is Figure 6.9 of a Von Neumann architecture? Why or why not?
No because Von Neumann does not include instruction memory

6. Redraw enough of Figure 6.9 to clearly show a version of the circuit that uses reg B as the operand added to offset for the load, store, and jump instructions.



7. A schematic at the level of abstraction of Figure 6.9 omits many details. If the processor is changed so that every instruction is 64 bits, what trivial change must be made to the figure?
Add 8 bits to the program counter instead of 4
8. Make a table showing for each instruction in Figure 6.2 which input (upper or lower (closer to the figure caption)) for each multiplexer, M1, M2, and M3, in Figure 6.9 must be selected. If either multiplexer input is a correct selection, then enter X in that cell of the table.

	M1	M2	M3
Add	Lower	Upper	Lower
Load	Lower	X	Upper
Store	Lower	Upper	X
Jump	Upper	Lower	Lower

9. Here follows a schematic for the circuitry inside the register unit in textbook Figure 6.9. The triangular devices labeled BUF are buffers, circuits that allow signals to pass un-inverted when a buffer is selected, otherwise a buffer behaves as an open switch. Label this schematic with the following information.
    a. reg A inputs
    b. reg B inputs
    c. dst reg inputs
    d. reg A outputs
    e. reg B outputs
    f. except for the 4-to-16 decoder inputs, indicate how many wires each “wire” in the schematic actually represents using slash/number notation.

g. Two of the decoders have an unlabeled input; add a likely label for these two inputs