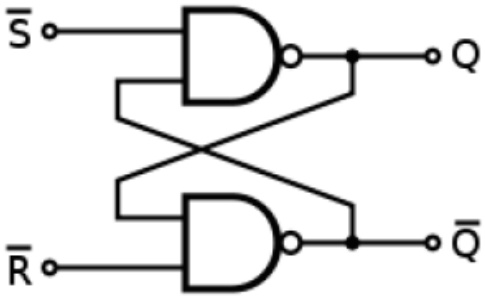
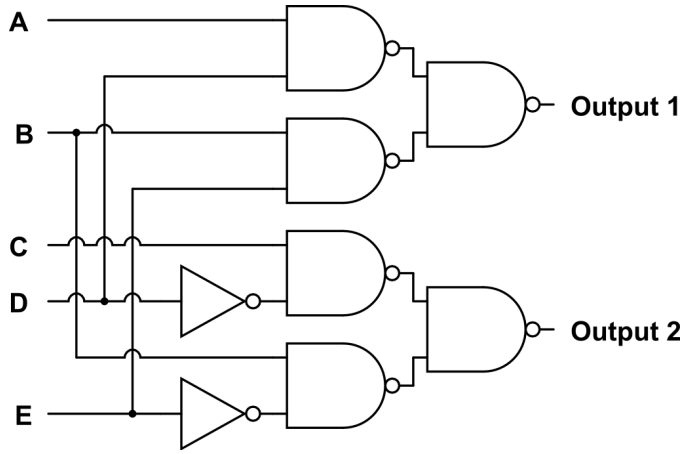
>>>> Reference Page – you may separate this page from the other pages <<<<

S'R' Latch Characteristic Table

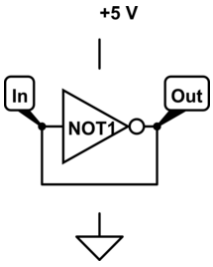
S'	R'	Q(t)	Q(t+1)
1	1	X	Q(t)
0	1	X	1 (set)
1	0	X	0 (reset)
0	0	X	Not allowed



Circuit A:



Circuit B:



The exam is closed book and notes and no calculators.

The TAs and I will not answer questions during the exam, so do not ask.

Correct answers to multiple choice questions earn 3 points.
Correct answers to free response questions earn 3 points, and partial credit is available.

Questions may refer to S'R' Characteristic Table, S'R' circuit, Circuit A, and Circuit B, all of which can be found on the Reference Page.

Enter this data on your bubble sheet now.

Instructor:	Adams
Course:	CS250
Signature:	<your signature>
Test:	M1
Date:	Feb. 6
Name:	<your name>
Student ID:	<your 10-digit ID number.

Step #1: Verify that your exam document contains 5 pages plus 1 Reference Page.

Answer the multiple choice questions on the bubble sheet.

1. I will neither give nor receive aid on this exam.
   A True
   B False

2. The bit string held in a register circuit depends on the history of the circuit.
   A True
   B False
   Answer: A. True. A register is a form of memory circuit and, thus, the bit string that it contains is a function of historic circuit inputs.

3. There is one best number representation format.
   A True
   B False
   C Insufficient information is given to allow making a decision between true or false.
   Answer: B. False. Different representations have different strengths and weaknesses and thus satisfy different sets of criteria. No one scheme can be best in all situations.

4. What is the propagation delay for Circuit A on the Reference Page?
   A 1 gate delay
   B 8 gate delays
   C 2 gate delays
   D 3 gate delays
   E None of the above
   Answer: D. The longest path through the circuit is from inputs D or E to Output2 through 3 gates.

5. The result of a function is true only when both of its two inputs are true. What logic gate can compute this function and deliver the result as an active low logic signal?
   A NAND
   B NOR
   C AND
   D OR
   E None of the above gates can perform as specified
   Answer: A. When both inputs of a NAND gate are asserted as logic 1, then the gate output is a logic 0.

6. A computer can perform addition on the set of integers.
   A True

B False

Answer: B. False, because of the finitude of hardware.

7. Which is the least abstract?
   A ASCII character
   B Bit
   C Source code
   D A zero volts logic signal
   E A C language struct

   Answer: D. A zero volts logic signal is a physical measurement of the electrical condition of a wire, which may represent a bit at a higher level of abstraction, which in turn may be part of an ASCII character, that is itself part of a struct, that, finally appears in source code.

8. For the S'R' latch, to ensure that Q(t+1) = 0 regardless of the value of Q(t), then ensure that
   A S'=0 and R'=0 at time t
   B S'=1 and R'=1 at time t
   C S'=0 and R'=1 at time t
   D S'=1 and R'=0 at time t
   E None of the above

   Answer: D. To be sure that Q(t+1) = 0 regardless of the value of Q(t), then the latch must be reset, which requires inputs of S'=1 and R'=0 at time t.

9. How many latches are needed to store the 8 digits of 0x01ABCD01?
   A 8
   B 16
   C 20
   D 26
   E None of the above

   Answer: E. Each hex digit is compact notation for 4 bits, so there are 32 bits denoted, which requires 32 latches, one latch per bit.

10. How many kilobytes is 2^{23} bits?
    A 2^5
    B 1024
    C 8192
    D 2^{20}
    E $2^{23}/8000$

    Answer: B. To convert bits to bytes, divide by the ratio 8 bits per byte. Thus, 2^{23} bits divided by 8 bits/byte gives 2^{23-3} bytes = 2^{20} bytes. To convert bytes to kilobytes divide by 2^{10} bytes per kilobyte. Thus, 2^{20} bytes / $2^{10\ bytes}$ / kilobyte = 2^{10} kilobytes. Finally, 2^{10} = 1024.

11. How many ones are in the bit string 0x78AE?

A 9
B 3
C 7
D 13
E None of the above
Answer: A. The bits string is 0111 1000 1010 1110 and contains 9 ones.

12. What is the bit string of the packed BCD representation for decimal integer 14?
A 1110
B 00001110
C 00011110
D 01001000
E 00010100
Answer: E. 00010100 partitioned into two 4-bit "nybbles" is 0001 0100, and each nibble represents the decimal digits 1 and 4, respectively as unsigned integers.

13. Which one of the three Boolean algebra operations is a universal logic gate?
A NOT
B AND
C OR
D All of the above gates are universal
E None of the above is correct
Answer: E. None of the individual Boolean algebra operations of NOT, AND, and OR corresponds to a universal logic gate that alone can implement any Boolean expression.

14. The following table describes a computer memory storing a 32-bit number representation.

Memory location address	Memory contents
0x00000000	0x80
0x00000001	0xF3
0x00000002	0xC0
0x00000003	0x00

If the memory uses big endian storage, what is the value of the most significant byte?
A 0x80
B 0x00
C 0x8
D 0x0
E None of the above
Answer: A. With big ending the "big," most significant byte, the byte containing the most significant bit, comes first. The first address is the one with the lowest address number. A byte requires two hex digits for its notation.

15. You do not know the values of the address bits input to a decoder, but they are not changing. The decoder outputs are active high. Two of the decoder outputs are connected to the inputs of a 2-input AND gate, but you do not know which two decoder outputs. The logic level voltages in the circuit are +5 volts and 0 volts.

    After waiting longer than the worst case propagation delay of this circuit, what voltage is there between the AND gate output and ground?

    A +5 volts
    B 0 volts
    C The voltage would be changing
    D There is insufficient information to determine the voltage
    E None of the above is correct

    Answer: B. The decoder points to only one output at a time and is of active-high design. Therefore, the voltage levels present at the two AND gate inputs cannot both be +5 volts. Therefore, the output of the AND gate will be at 0 volts.

16. Which adder circuit type operates the slowest assuming that all gate delays are equal and all wire lengths are equal.

    A 1's complement
    B 2's complement
    C 1's and 2's complement are equally fast
    D 1's complement is faster than 2's complement for some (addend, augend) pairs
    E None of the above answers is correct

    Answer: A. 1's complement requires end around carry, doubling propagation delay, but 2's complement does not.

17. The sum of three bits requires exactly two bits to represent.

    A True
    B False

    Answer: A. The sum of all possible combinations of three bits must be accommodated in the representation. There are four possible outcomes that can be written in decimal numbers as 0, 1, 2 and 3. Two is the precise number of bits needed to represent four results.

18. A byte can represent or encode

    A An unsigned integer
    B The outcomes from 8 tosses of a coin
    C One of 99 values
    D The names of the TAs of my CS250 lab section
    E All of the above

    Answer: E. A byte can take on 256 different patterns. Each of these patterns can be assigned a meaning. The cases in answers A, B, C, and D all have 256 or fewer members of the set of things to be identified. Therefore, one byte is sufficient to represent an item uniquely in each case.

19. A bit string represents a sequence of 7-bit ASCII characters. This same bit string must also represent
    A A 2's complement integer
    B A collection of single-precision IEEE floating point numbers
    C A series of decimal digits in packed BCD format
    D Any of the three above possibilities
    E None of the above
    Answer: A. Of the representation formats 2's complement integer, single-precision IEEE floating point, and packed BCD, only 2's complement representation is meaningful for a bit string of any length, and in particular, for a string of length 7c bits, where c is the number of ASCII characters in the given sequence.

20. Processors implement a fetch-execute cycle.
    A True
    B False
    Answer: A. This is how a processor automate software.

21. A computer can use the same circuit for unsigned and 2's complement integer arithmetic.
    A True
    B False
    Answer: A.

22. Sign extension can change the value of an unsigned integer.
    A True
    B False
    Answer: A. For some unsigned integers, the MSB is 1. Extending this bit will change the integer value represented.

23. The control system of a computer is found within which computer organization subsystem?
    A Input/Output
    B Memory
    C Processor
    D Data path
    E None of the above
    Answer: C. The control subsystem is the part of the processor that manages the fetch-execute cycle.