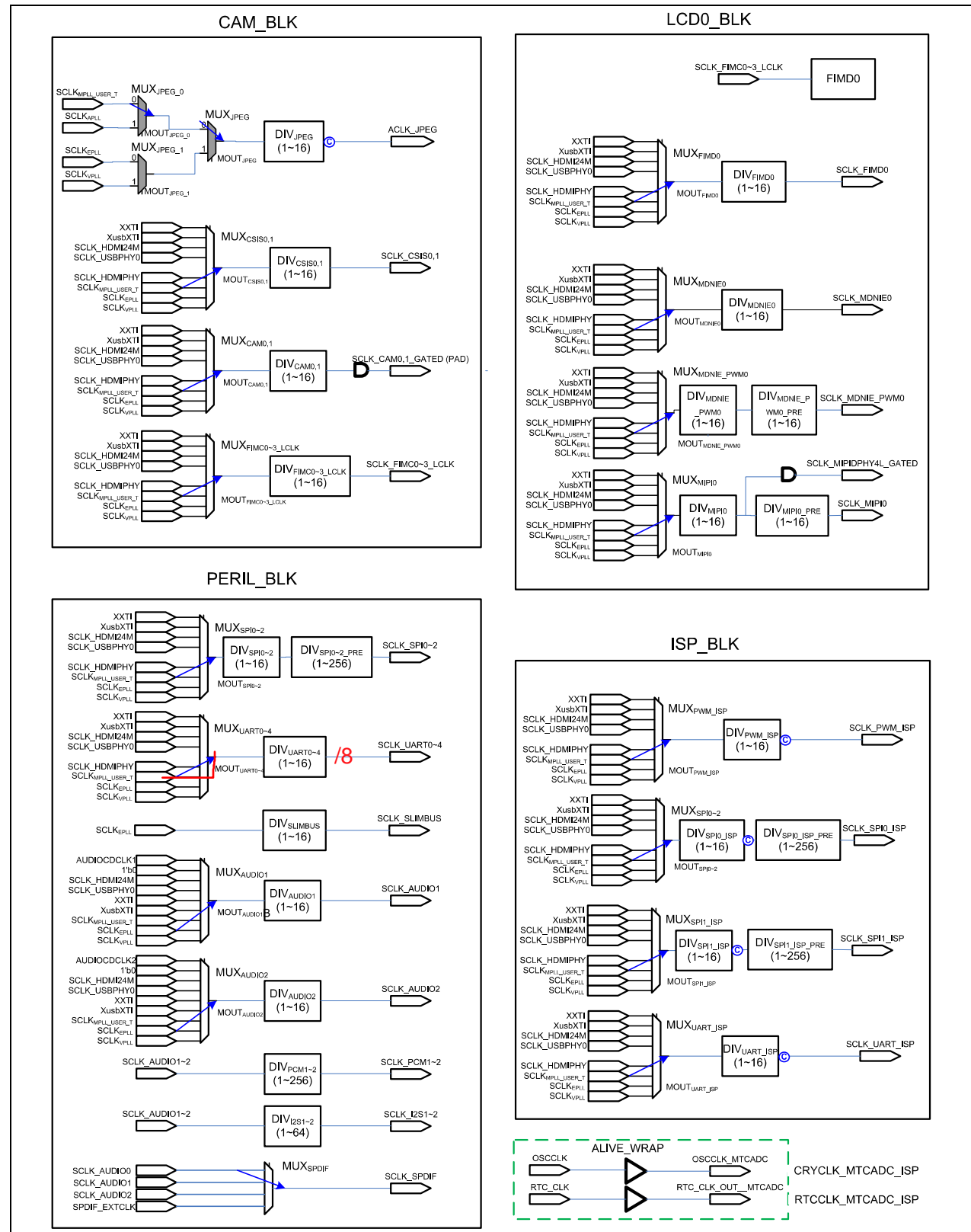


Figure 7-2 Exynos 4412 Clock Generation Circuit (CPU, BUS, DRAM, ISP Clocks)



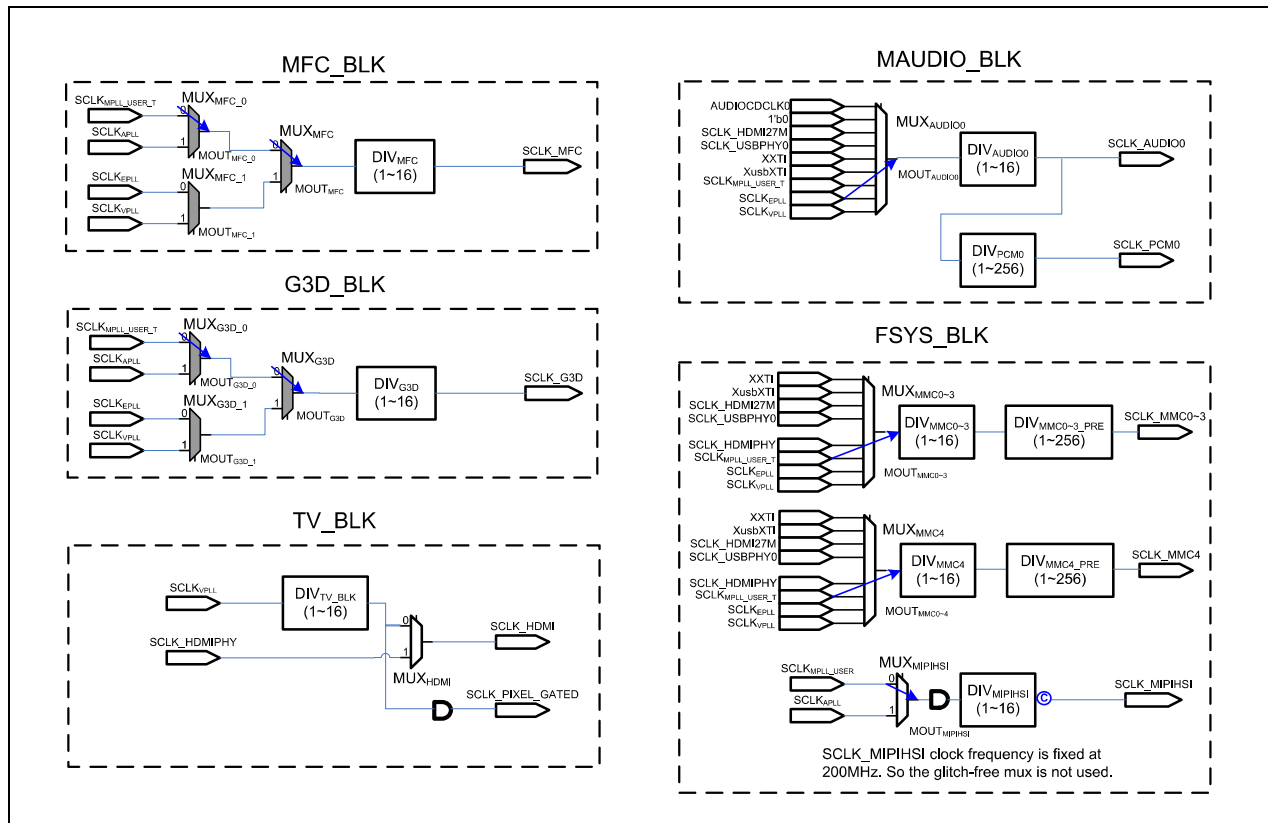


Figure 7-3 Exynos 4412 Clock Generation Circuit (Special Clocks)

NOTE: The SCLKuser_mpll In [Figure 7-3](#) means SCLKuser_mpll_T.

Caution: In [Figure 7-2](#) and [Figure 7-3](#), the MUX's with grey color are glitch-free. For glitch-free clock MUX, ensure that all clock sources are running while changing the clock selection. For clock dividers, ensure that input clock is running while changing the divider value.