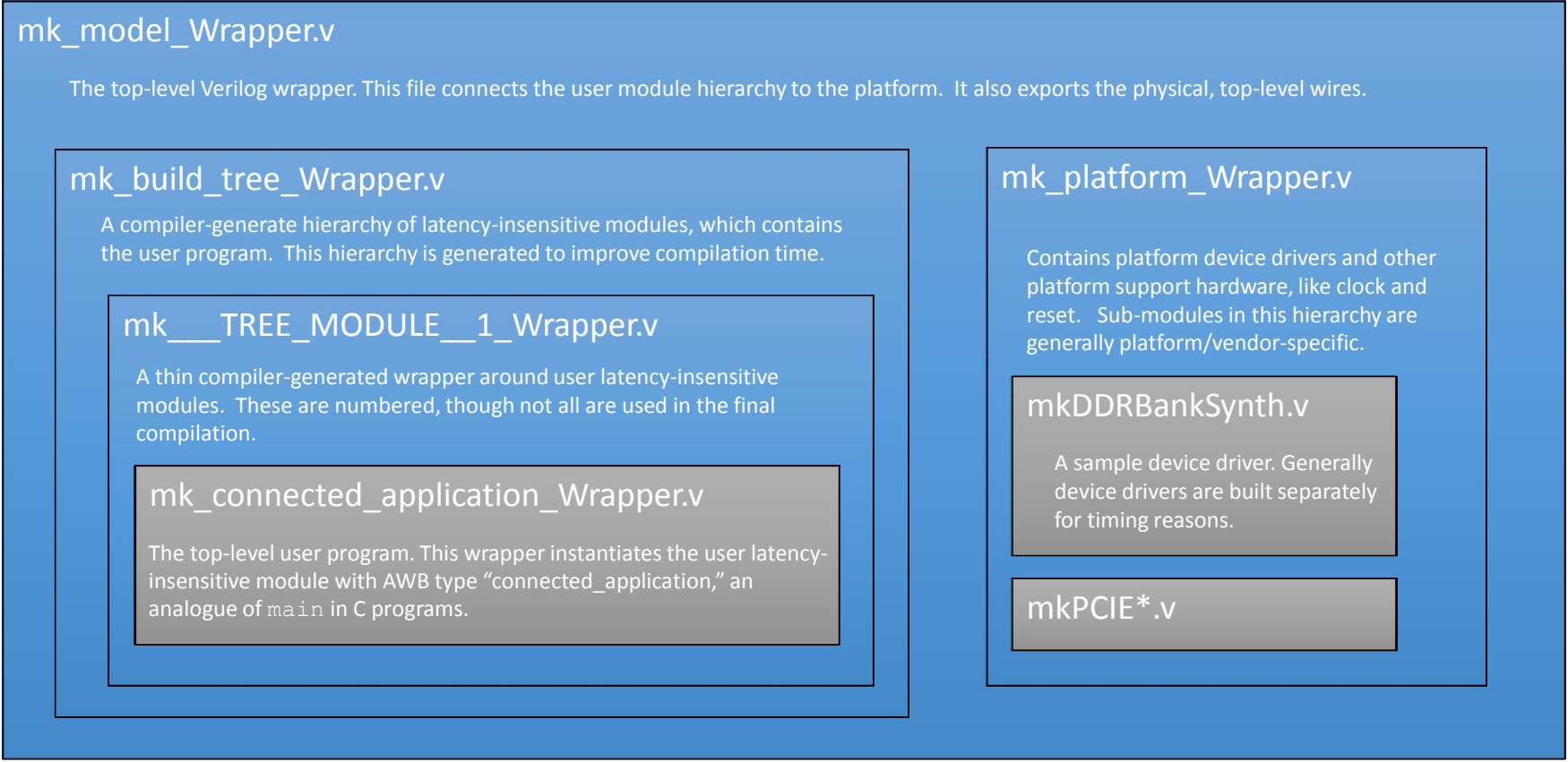
mk_model_Wrapper.v
The top-level Verilog wrapper. This file connects the user module hierarchy to the platform. It also exports the physical, top-level wires.
mk_build_tree_Wrapper.v
A compiler-generate hierarchy of latency-insensitive modules, which contains the user program. This hierarchy is generated to improve compilation time.
mk___TREE_MODULE__1_Wrapper.v
A thin compiler-generated wrapper around user latency-insensitive modules. These are numbered, though not all are used in the final compilation.
mk_connected_application_Wrapper.v
The top-level user program. This wrapper instantiates the user latency-insensitive module with AWB type "connected_application," an analogue of main in C programs.
mk_platform_Wrapper.v
Contains platform device drivers and other platform support hardware, like clock and reset. Sub-modules in this hierarchy are generally platform/vendor-specific.
mkDDRBankSynth.v
A sample device driver. Generally device drivers are built separately for timing reasons.
mkPCIE*.v