# Electronic Circuits Design

## *Lecture – 8*

- *Digital Voltage Transfer Characteristics*
- *Complementary CMOS Gates*

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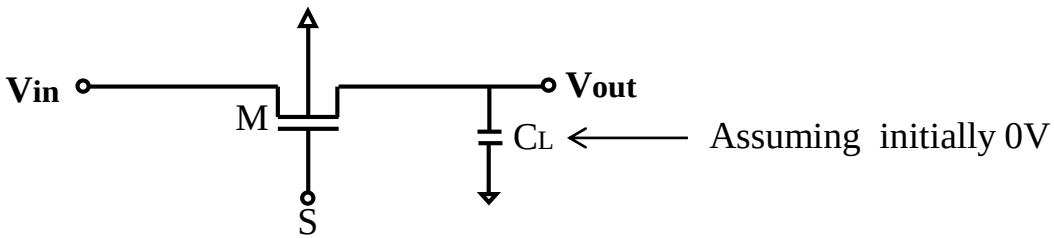
# MOSFET Voltage Transfer Characteristics

# n-MOS Pass Transistor



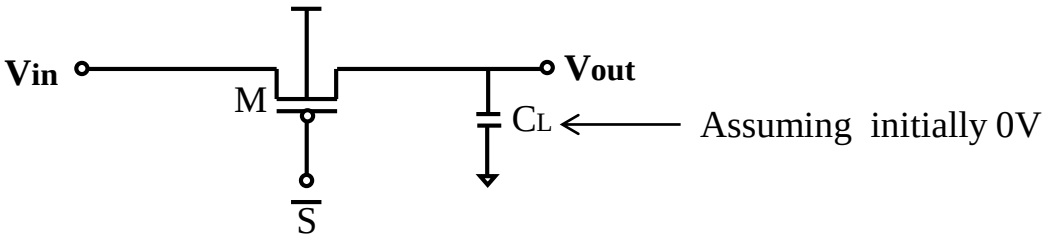

- S = $V_{SS}$ ; M is turn off, Vout = floating
- S = $V_{DD}$ ; M is turn on

  Vin = $V_{DD}$ ⇒ Vout = $V_{DD} - V_{THN}$ ← poor transmission of "1"

  ➔ Transistor would turn itself off

Then, Vin = $V_{SS}$ ⇒ Vout = Vss ← good transmission of "0"

# p-MOS Pass Transistor




- $\overline{S} = V_{DD}$ ; M is turn off, Vout = floating
- $\overline{S} = V_{SS}$ ; M is turn on

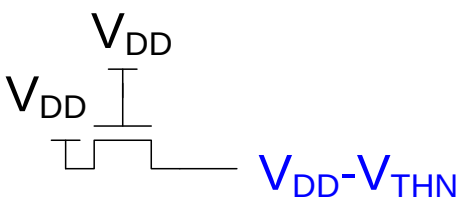
$V_{in} = V_{DD} \Rightarrow V_{out} = V_{DD}$ ← good transmission of "1"

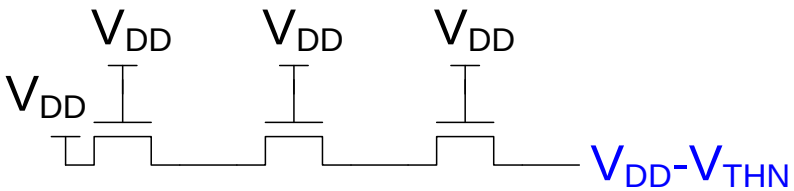
Then, $V_{in} = V_{SS} \Rightarrow V_{out} = |V_{THP}|$ ← poor transmission of "0"

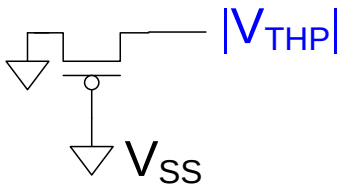
➔ Transistor would turn itself off

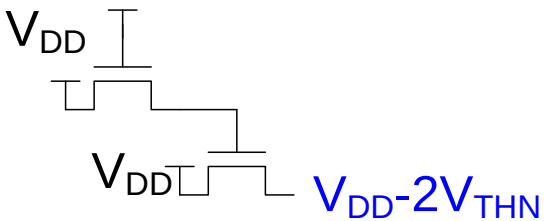
# Pass Transistor Circuits

- Assuming that sources of n-MOS and p-MOS are initially 0V and $V_{DD}$, respectively

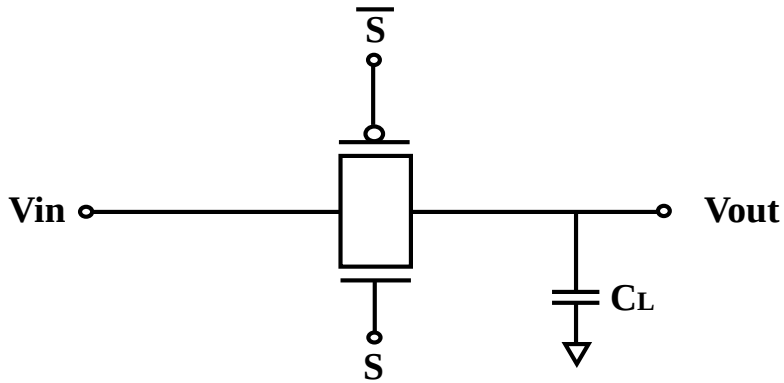


# Transmission Gate




- p-MOS body is tied to $V_{DD}$
- n-MOS body is tied to $V_{SS}$

- Function Table

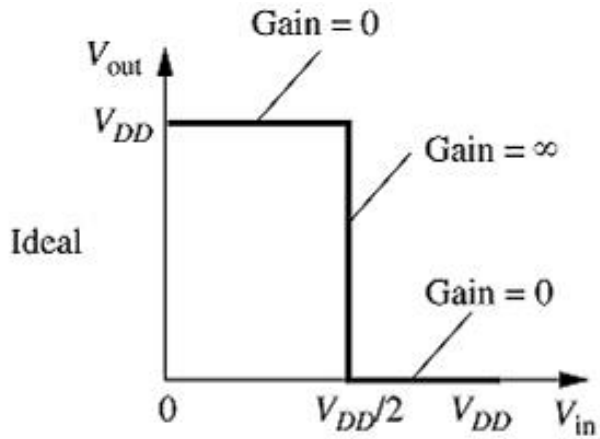
| | Vout |
|---|---|
| $S = 0$<br>$\overline{S} = 1$ | Z (floating) |
| $S = 1$<br>$\overline{S} = 0$ | Vin |

⇒ **good transmission for both of "0" & "1"**

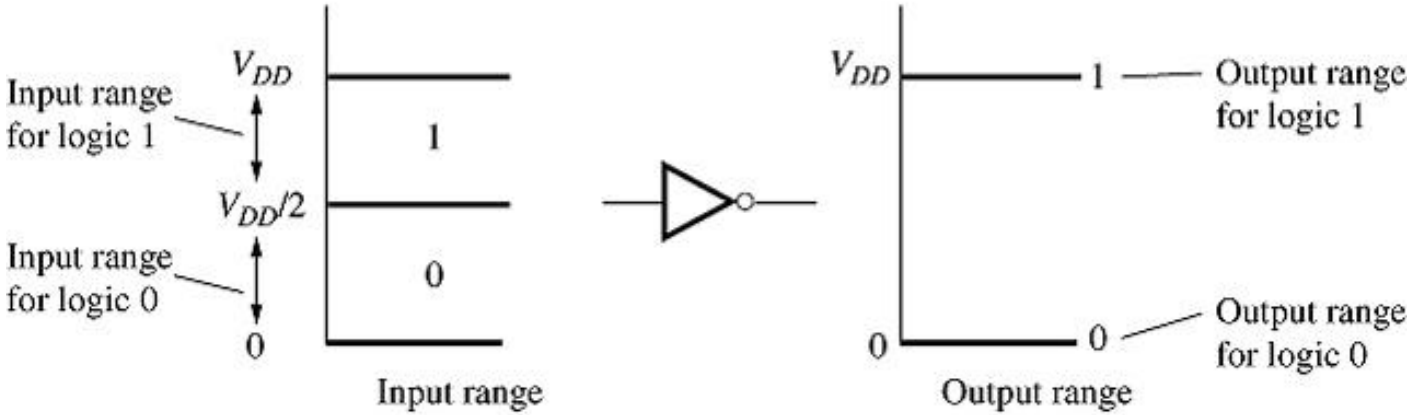
# Digital Inverter

- *Logic Level and Noise Margin*
- *CMOS Inverter*
- *Other Types of MOS Inverter*

# Ideal VTC of Inverter

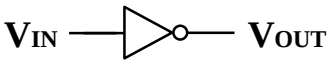


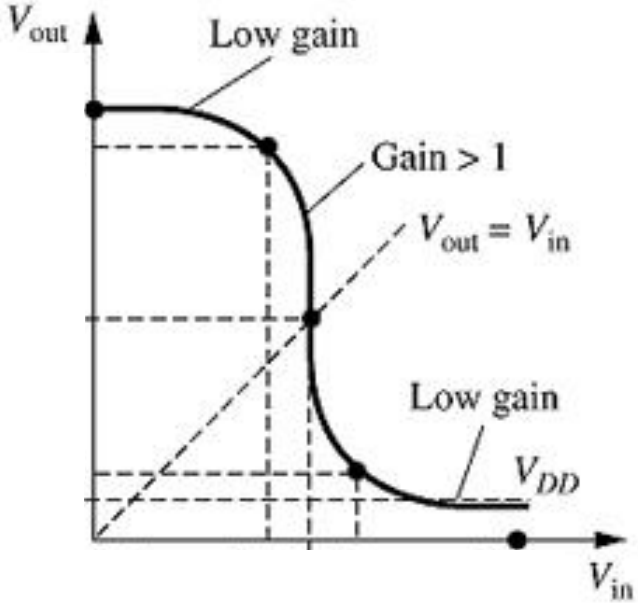

(a)




(b)

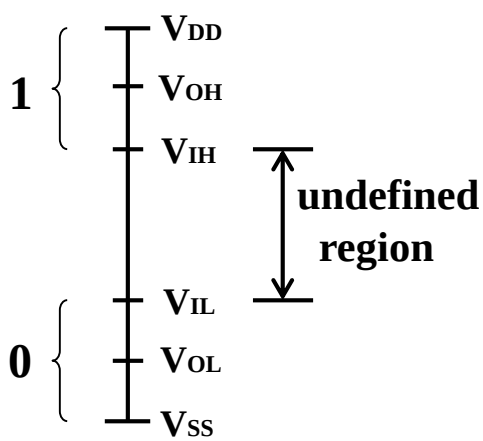
# Practical VTC of Inverter

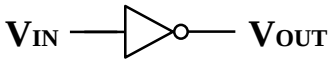


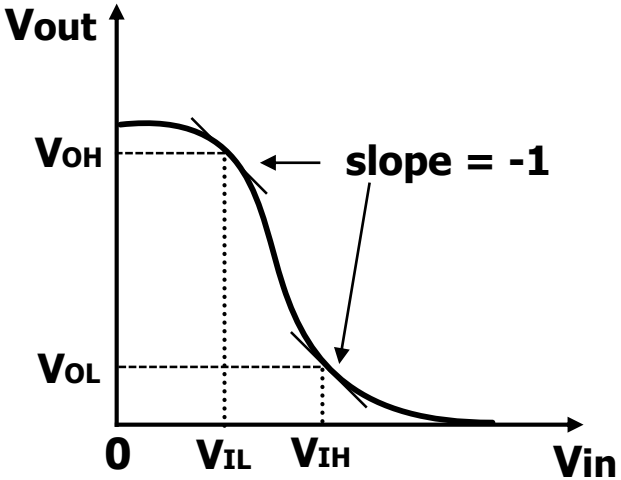



# Logic Level vs Voltage Domain

- $V_{IL}$ : maximum low input voltage
- $V_{IH}$ : minimum high input voltage
- $V_{OH}$ : minimum high output voltage
- $V_{OL}$ : maximum low output voltage

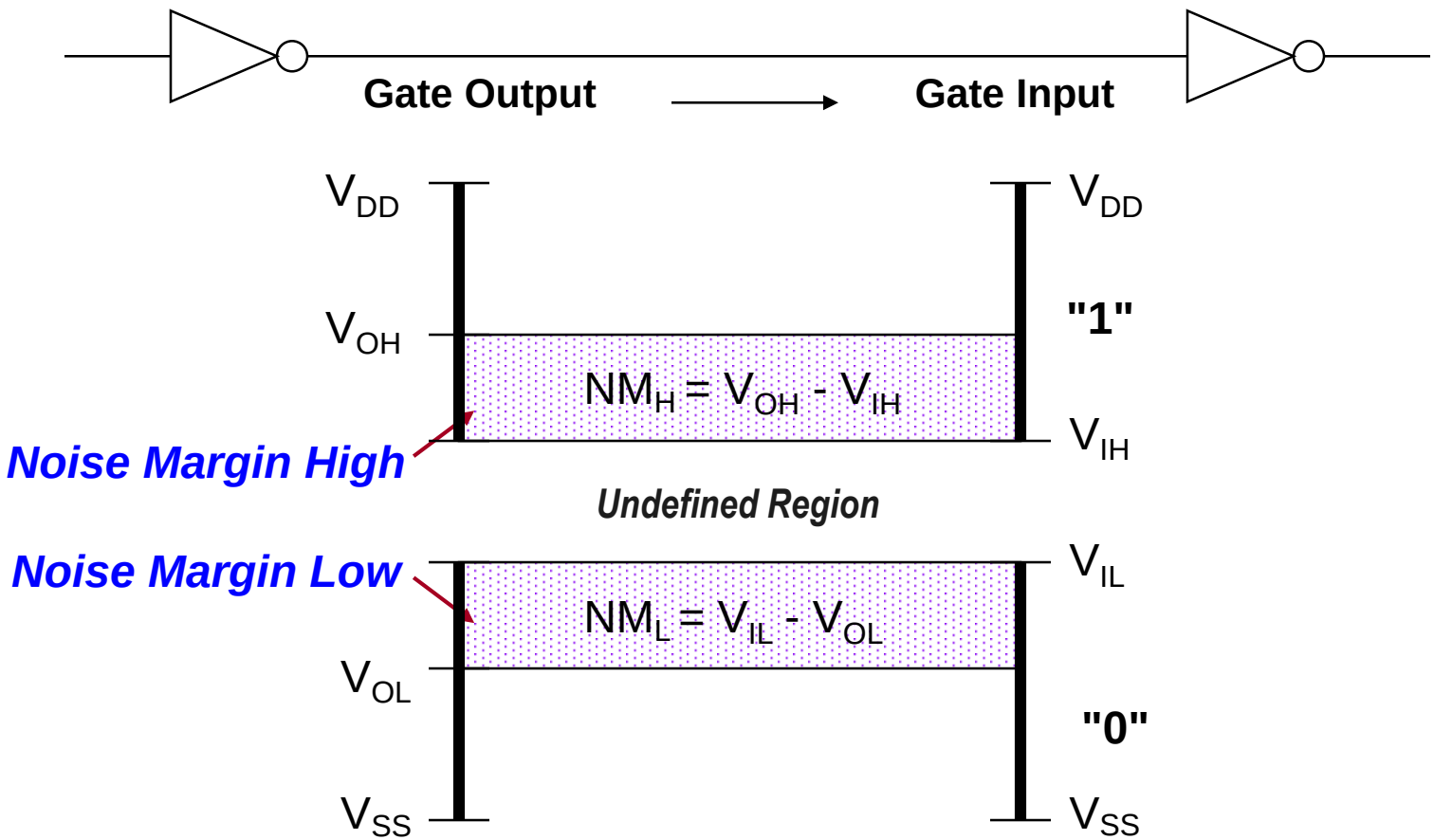


# Noise Margin

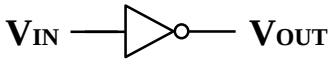
- Noise margin: allowable noise voltage on input of gate so that the output will not be corrupted

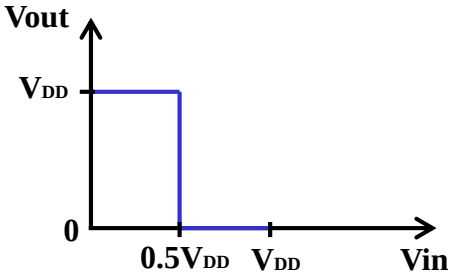


# Noise Margin (continued)

- Noise margin should be > 0 and as large as possible.
- Desirable : $V_{OH} \rightarrow V_{DD}$, $V_{OL} \rightarrow V_{SS}$

$$V_{IH} = V_{IL} \rightarrow (V_{DD} - V_{SS})/2$$



# CMOS Inverter

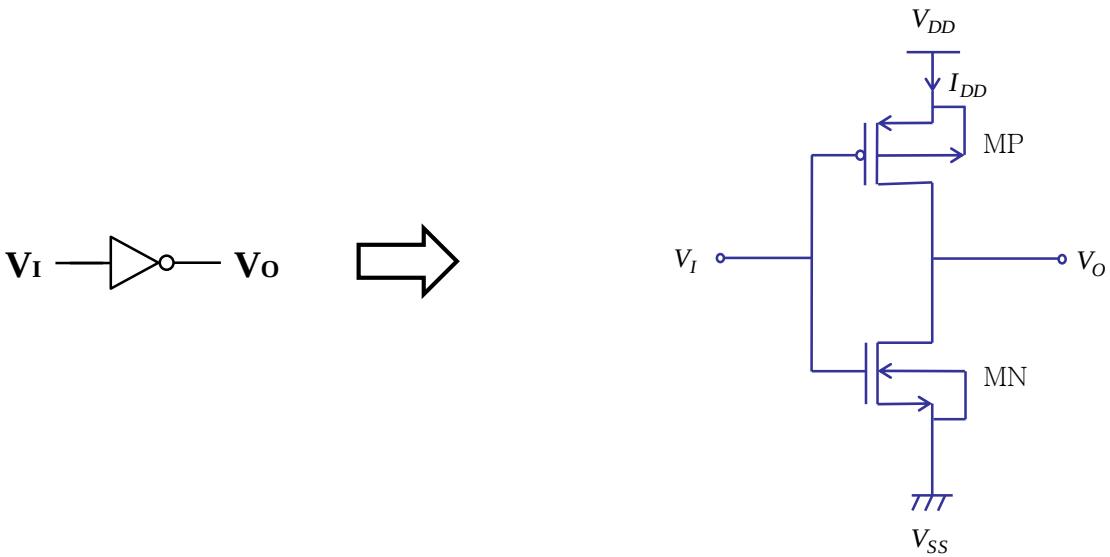



그림 2.1.1 CMOS inverter 회로

# DC Transfer Characteristics

- Logic threshold voltage (or gate threshold voltage) : $V_{LT} \equiv V_I$ when $V_O = V_I$

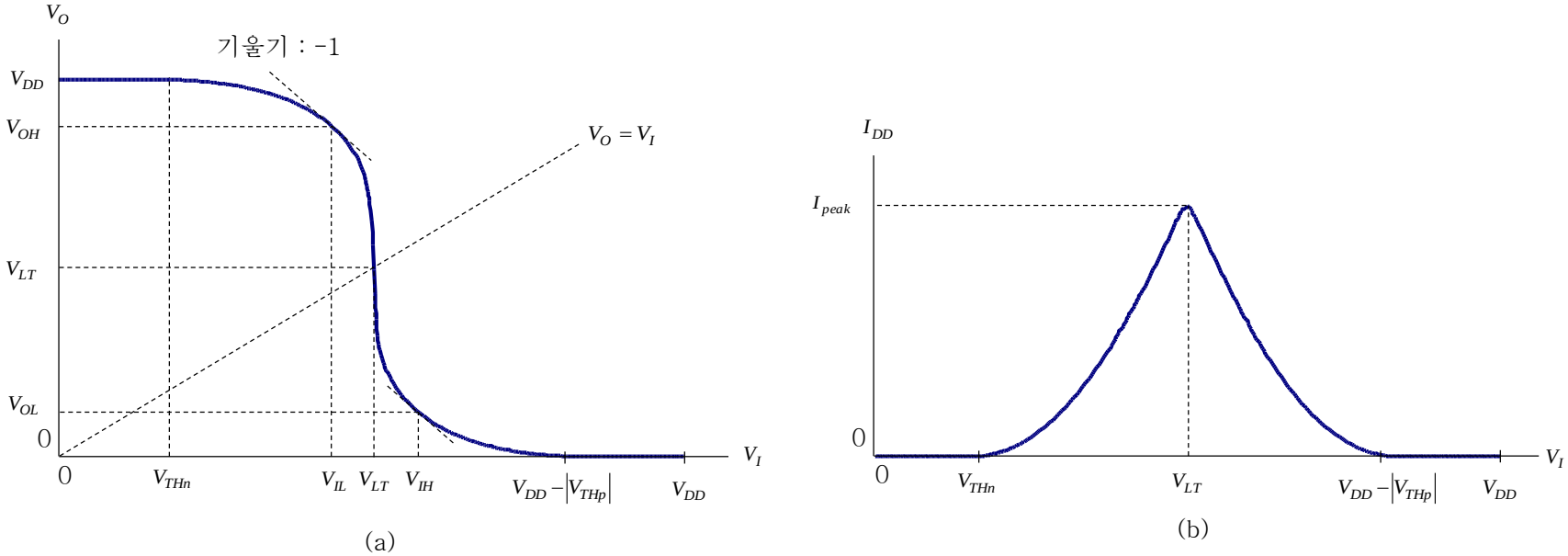



**그림 2.1.2** CMOS 인버터(inverter)의 DC 전달 특성: (a) 출력 전압, (b) 전류

# VTC: Case -1 & 2

1) $0 \leqq V_I < V_{THn}$ 인 경우

$$V_O = V_{DD}$$

$$I_{DD} = 0$$

2) $V_{THn} \leqq V_I < V_{LT}$ 인 경우 (neglecting the channel length modulation)

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot (V_I - V_{THn})^2 = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \cdot (V_{DD} - V_I - |V_{THp}| - 0.5(V_{DD} - V_O)) \cdot (V_{DD} - V_O)$$

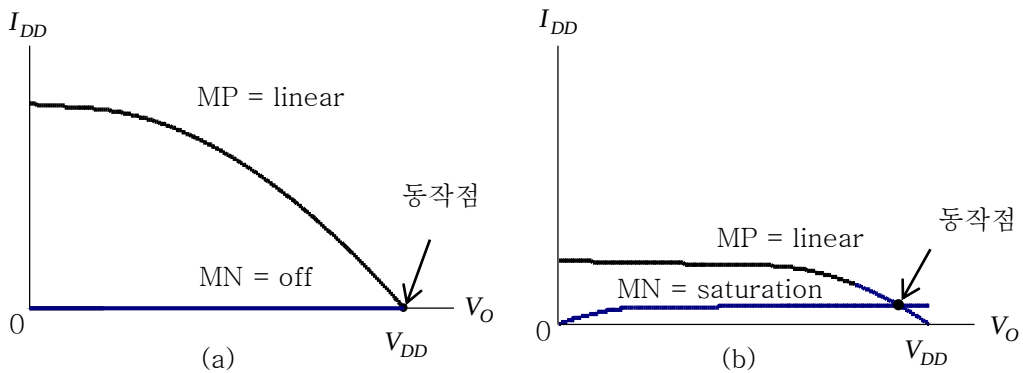



그림 2.1.3 (a) $0 \leqq V_I < V_{THn}$ 일 때의 동작점 결정 (b) $V_{THn} \leqq V_I < V_{LT}$ 일 때의 동작점 결정

# VTC: Case - 2

2) $V_{THn} \leqq V_I < V_{LT}$ 인 경우

==>

$$V_O = V_I + |V_{THp}| + \sqrt{(V_{DD} - V_I - |V_{THp}|)^2 - \beta \cdot (V_I - V_{THn})^2}$$

**where** $\beta = \dfrac{\mu_n C_{ox} (W/L)_n}{\mu_p C_{ox} (W/L)_p}$

$= \beta_N / \beta_P$

$$I_{DD} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n \cdot (V_I - V_{THn})^2$$

If $\beta_N = \beta_P$, $V_{THn} = -V_{THp} = V_{TH}$,

$$V_O = V_I + V_{TH} + \sqrt{(V_{DD} - 2V_{TH}) \cdot (V_{DD} - 2V_I)}$$

# VTC: Case - 2 (continued)

2) $V_{THn} \leqq V_I < V_{LT}$ 인 경우

- We define $V_{IL} \equiv V_I$ when $dV_O/dV_I = -1$, $V_{OH} \equiv V_O$ when $V_I = V_{IL}$

**==>**

$$V_{IL} = \frac{\sqrt{\beta}}{\beta - 1}\cdot\left(\sqrt{\beta} - \frac{2}{\sqrt{\beta+3}}\right)\cdot V_{THn} + \frac{\sqrt{\beta}}{\beta - 1}\cdot\left(\frac{2}{\sqrt{\beta+3}} - \frac{1}{\sqrt{\beta}}\right)\cdot\left(V_{DD} - \left|V_{THp}\right|\right)$$

$$= V_{THn} + \frac{2\sqrt{\beta} - \sqrt{\beta+3}}{(\beta-1)\sqrt{\beta+3}}\cdot\left(V_{DD} - V_{THn} - \left|V_{THp}\right|\right) \quad (\beta \neq 1 \text{ 일 때})$$

$$V_{IL} = V_{THn} + \frac{3}{8}\cdot\left(V_{DD} - V_{THn} - \left|V_{THp}\right|\right) \quad (\beta = 1 \text{ 일 때})$$

$$V_{OH} = V_{THn} + \left|V_{THp}\right| + \frac{(\beta+1)\cdot\sqrt{\beta} - \sqrt{\beta+3}}{(\beta-1)\cdot\sqrt{\beta+3}}\cdot\left(V_{DD} - V_{THn} - \left|V_{THp}\right|\right) \quad (\beta \neq 1 \text{ 일 때})$$

$$V_{OH} = V_{THn} + \left|V_{THp}\right| + \frac{7}{8}\cdot\left(V_{DD} - V_{THn} - \left|V_{THp}\right|\right) \quad (\beta = 1 \text{ 일 때})$$

# VTC: Case - 3

3) $V_I \approx V_{LT}$ 인 경우

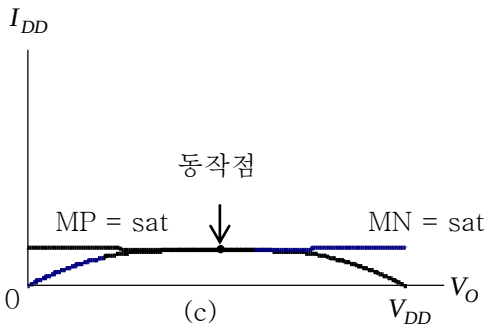



그림 2.1.3.(c) $V_I \approx V_{LT}$ 일 때의 동작점 결정

- Neglecting the channel length modulation, when $V_I = V_{LT}$

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot (V_{LT} - V_{THn})^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \cdot (V_{DD} - V_{LT} - |V_{THp}|)^2$$

# VTC: Case - 3 (continued)

3) $V_I \approx V_{LT}$ 인 경우

==>

$$V_{LT} = \frac{\sqrt{\mu_n (W/L)_n} \cdot V_{THn} + \sqrt{\mu_p (W/L)_p} \cdot (V_{DD} - |V_{THp}|)}{\sqrt{\mu_n (W/L)_n} + \sqrt{\mu_p (W/L)_p}}$$

$$= \frac{\sqrt{\beta} \cdot V_{THn} + (V_{DD} - |V_{THp}|)}{\sqrt{\beta} + 1}$$

If $\beta_N = \beta_P$, $V_{THn} = -V_{THp}$ ==> $V_{LT} = 0.5V_{DD}$

$$I_{DD} = I_{DD.peak} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot (V_{LT} - V_{THn})^2$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \cdot (V_{DD} - V_{LT} - |V_{THp}|)^2$$

# VTC: Case - 3 (continued)

3) $V_I \approx V_{LT}$ 인 경우

- **NOTE: When MN = MP = saturation, the voltage gain ≡ $dV_O/dV_I$ is maximum**

**==>**

$dV_O/dV_I = -\infty$ (if $\lambda = 0$)

$$\frac{\partial V_O}{\partial V_I} = -\frac{2}{\lambda(V_{DD}/2 - V_{TH})}$$ (if $\boldsymbol{\lambda \neq 0}$, $\beta_N = \beta_P$, $V_{THn} = -V_{THp} = V_{TH}$, $\boldsymbol{\lambda_p = \lambda_n = \lambda}$, $\boldsymbol{\lambda} V_{DD} << 2$)

- **Typically, for CMOS inverter, $|dV_O/dV_I| > 10$ in $V_I \approx V_{LT}$ region**

# VTC: Case - 4

4) $V_{LT} < V_I < V_{DD} - |V_{THp}|$ 인 경우 (neglecting the channel length modulation)

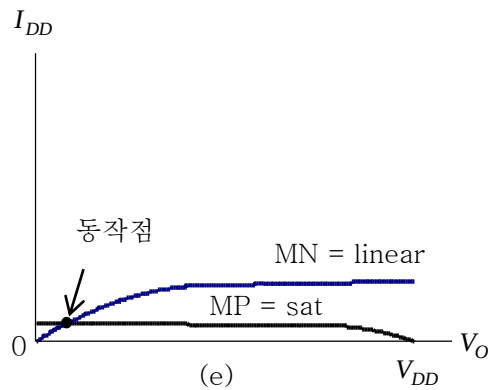



그림 2.1.3.(e) $V_{LT} < V_I < V_{DD} - |V_{THp}|$ 일 때의 동작점 결정

From a similar analysis with the case-2,

==>

$$V_O = V_I - V_{THn} - \sqrt{(V_I - V_{THn})^2 - \frac{1}{\beta}\cdot(V_{DD} - V_I - |V_{THp}|)^2}$$

$$I_{DD} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \cdot (V_{DD} - V_I - |V_{THp}|)^2$$

# VTC: Case - 4 (continued)

4) $V_{LT} < V_I < V_{DD} - |V_{THp}|$ 인 경우

- We define $V_{IH} \equiv V_I$ when $dV_O/dV_I = -1$, $V_{OL} \equiv V_O$ when $V_I = V_{IH}$

**==>**

$$V_{IH} = V_{THn} + \frac{2\beta - \sqrt{3\beta + 1}}{(\beta - 1)\cdot\sqrt{3\beta + 1}}\cdot(V_{DD} - V_{THn} - |V_{THp}|) \qquad (\beta \neq 1 \text{ 일 때})$$

$$V_{IH} = V_{THn} + \frac{5}{8}\cdot(V_{DD} - V_{THn} - |V_{THp}|) \qquad (\beta = 1 \text{ 일 때})$$

$$V_{OL} = \frac{\beta + 1 - \sqrt{3\beta + 1}}{(\beta - 1)\cdot\sqrt{3\beta + 1}}\cdot(V_{DD} - V_{THn} - |V_{THp}|) \qquad (\beta \neq 1 \text{ 일 때})$$

$$V_{OL} = \frac{1}{8}\cdot(V_{DD} - V_{THn} - |V_{THp}|) \qquad (\beta = 1 \text{ 일 때})$$

# VTC: Case - 5

5) $V_{DD} - |V_{THp}| \leqq V_I < V_{DD}$ 인 경우

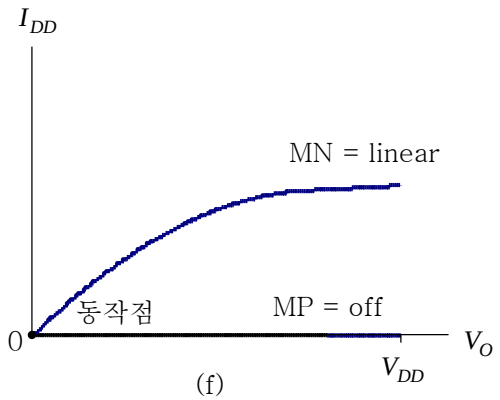



그림 2.1.3.(f) $V_{DD} - |V_{THp}| \leqq V_I < V_{DD}$ 일 때의 동작점 결정

==>

$V_O = 0$

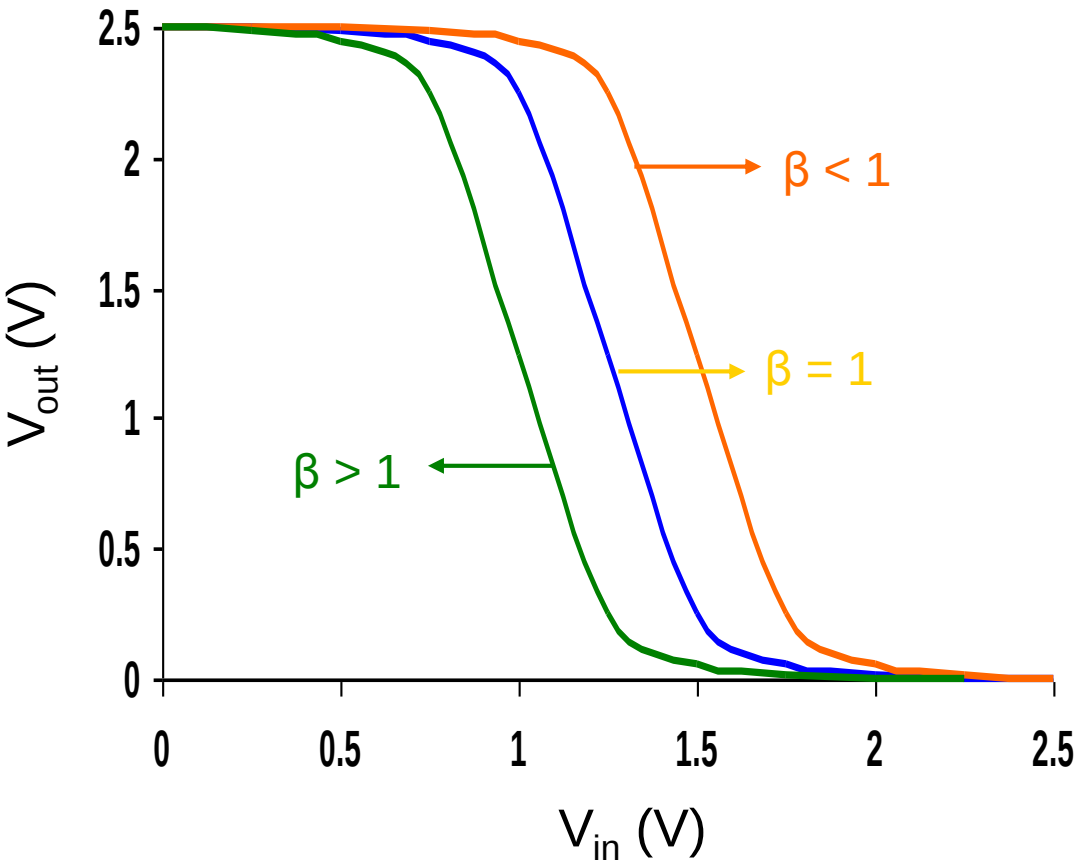
$I_{DD} = 0$

# Beta Ratio

- $\beta_N / \beta_P = 1$ is desirable since $V_{LT} = 0.5V_{DD}$
- If $\beta_N / \beta_P \neq 1$, switching point will move from $V_{DD}/2$

$$\beta = \frac{\mu_n C_{ox} (W/L)_n}{\mu_p C_{ox} (W/L)_p}$$

$$= \beta_N / \beta_P$$



# Effects of β

- $V_{DD}$ = 3.3 V, $V_{THn}$ = -$V_{THp}$ = 0.5 V

**표 2.1.2** $\beta = 1$일 때의 CMOS inverter DC 파라미터 값

| $V_{LT}$ | $V_{IL}$ | $V_{IH}$ | $V_{OL}$ | $V_{OH}$ | NML | NMH |
|---|---|---|---|---|---|---|
| 1.65 V | 1.3625 V | 1.9375 V | 0.2875 V | 3.0125 V | 1.075 V | 1.075 V |

# Effects of β (continued)

- $V_{DD}$ = 3.3 V, $V_{THn}$ = -$V_{THp}$ = 0.5 V

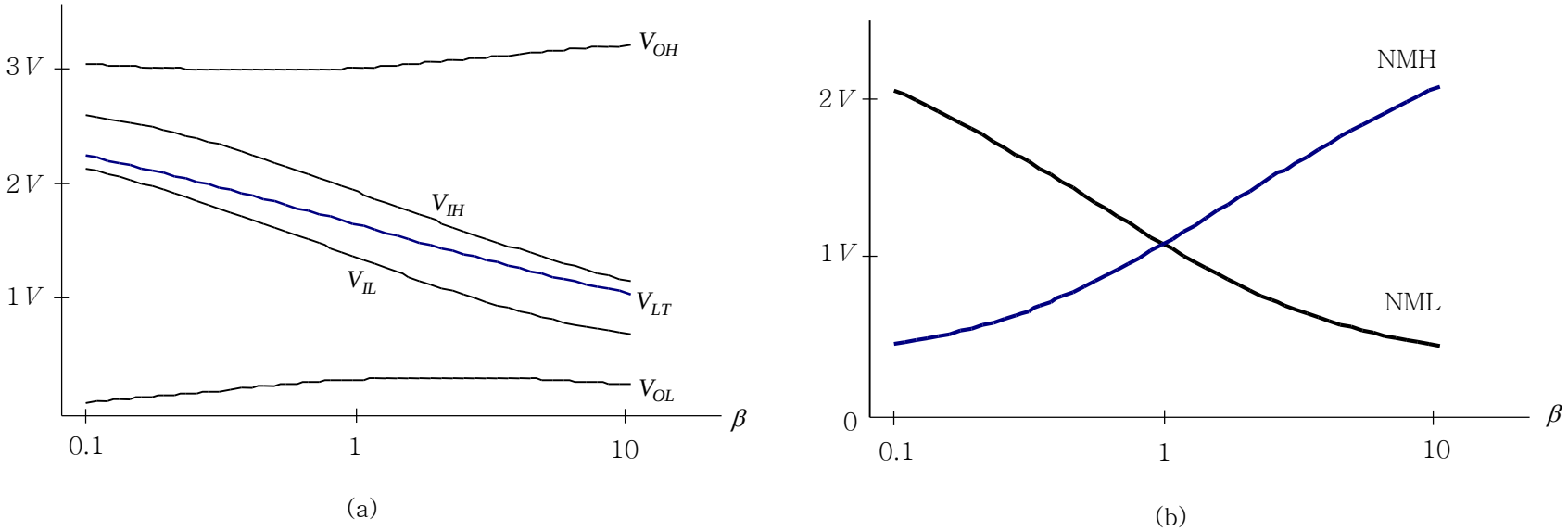



그림 2.1.4 $\beta$ 값 변화에 따른 DC 파라미터 값들의 변화

# Effects of $V_{DD}$

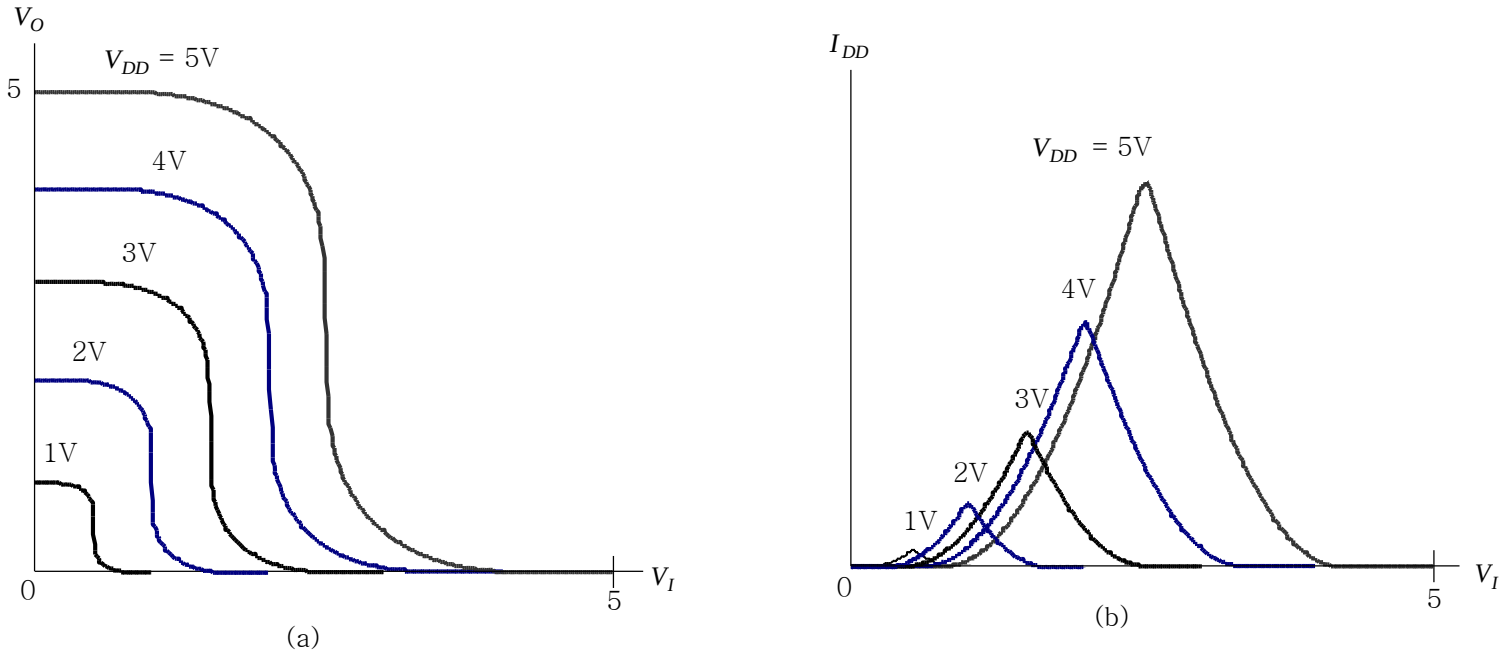
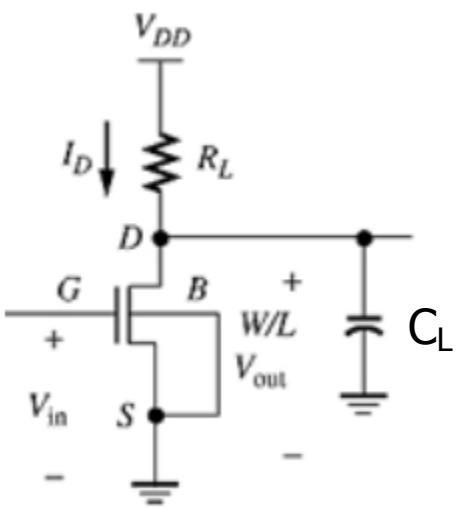


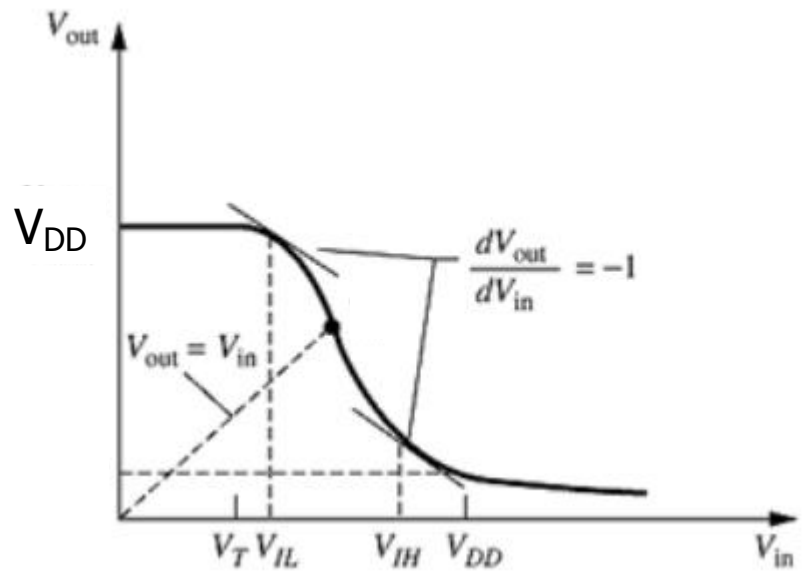

**그림 2.1.5** $V_{DD}$ 변화에 따른 CMOS inverter의 DC 전압 전달함수와 전류( $I_{DD}$ ) 변화
(a) 출력 전압, (b) 전류

# Features of CMOS Inverter

- No static current
  - Dynamic current only
  - Low power consumption
- Full swing from $V_{DD}$ to GND
  - Maximum noise margin
  - Immune to noise
- Minimum operating power supply
  - $V_{DD,MIN} > \text{Max}(V_{THN}, |V_{THP}|)$
- Ratioless logic

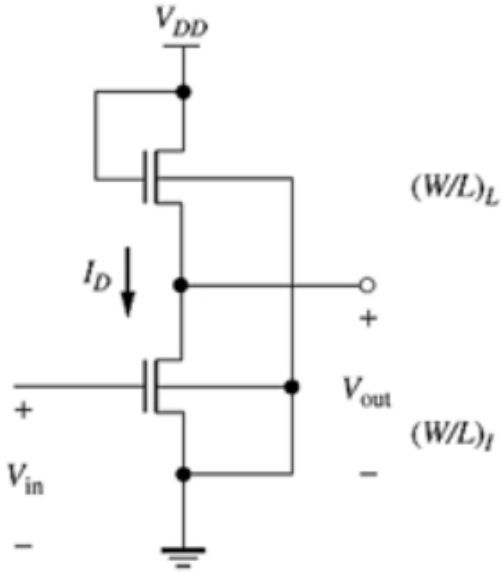
# Resistive Load Inverter

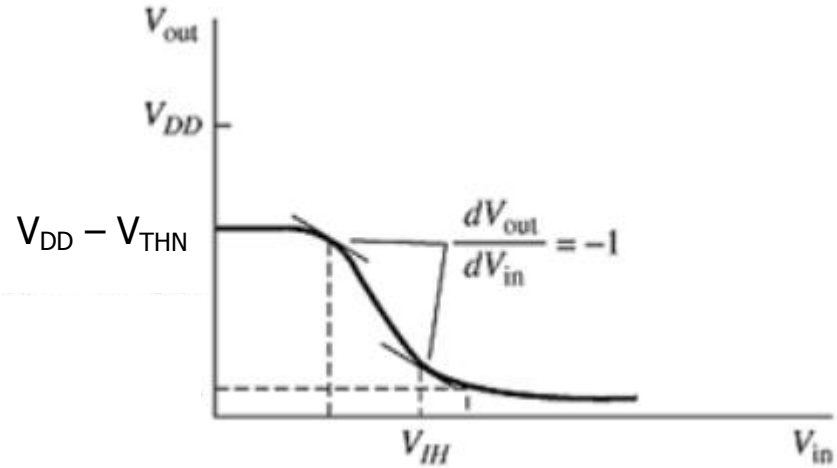



- VTC can be obtained by stating the current through the resistor and the drain current of the transistor are same.
- Ratioed logic
- Dissipates power continually when the input is high

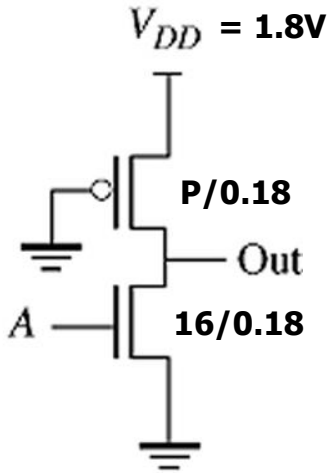
# Saturated Load Inverter

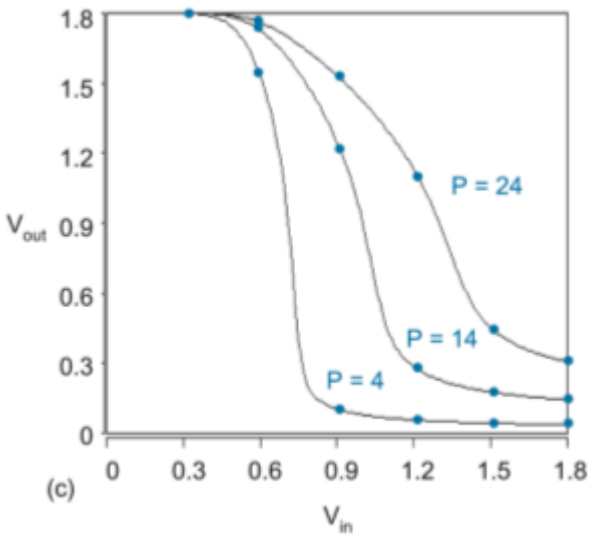



- **Ratioed logic**
  - ➔ **Logic operation depends on the size ratio of the two transistors**
- **Dissipates power continually when the input is high**

# Pseudo-nMOS Inverter

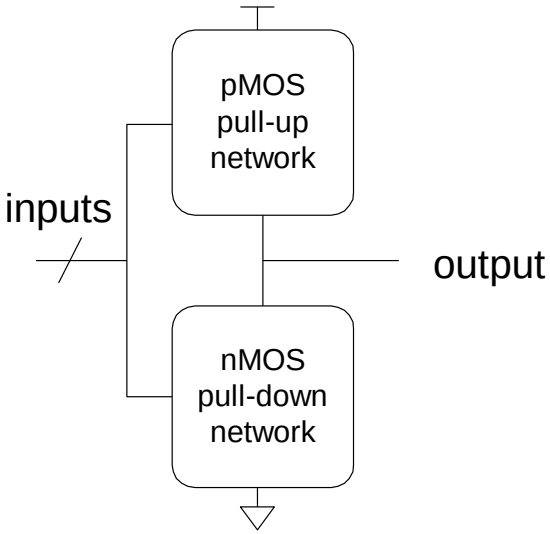



- When high fan-in gate is required, then pseudo-nMOS logic is a good candidate
- Ratioed logic
- Dissipates power continually when the input is high

# Complementary CMOS Gates

# Complementary CMOS Logic Gates



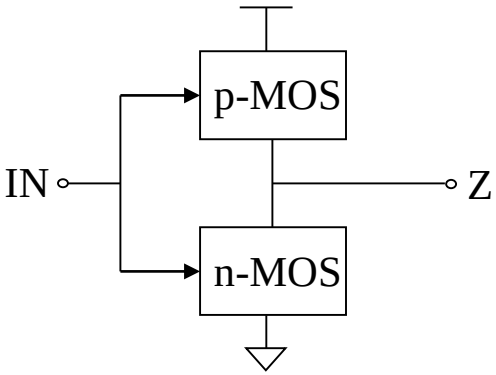

- A static CMOS logic is formed by combining series and parallel connection of p-MOS pull-up and n-MOS pull-down transistors.

⇨ Complementary Type !!

- best option in majority CMOS circuits

→ ~ 90% of all CMOS VLSI design

# Synthesis Procedure



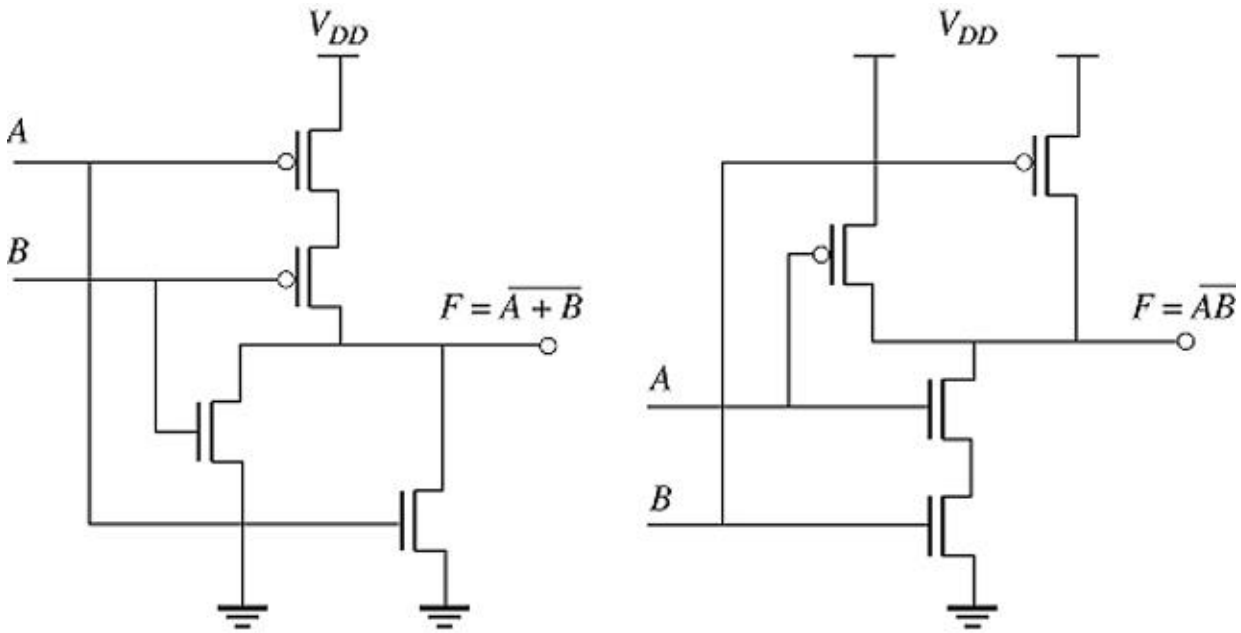

⇨ **When a logic function Z is given,**

i ) find a 0's function (Z') for n-MOS logic.
ii) make the function compact as much as possible.
iii) connect series / parallel combination such as AND = series / OR = parallel.
iv) connect one side of n-structure to Vss and the other to the output.
v ) find a 1's function (Z) for p-MOS logic by using De Morgan's theory from the 0's function.
vi) repeat ii) and iii).
vii) connect one end of p-structure to $V_{DD}$ and the other to the output.
viii) finally, combine both p-structure and n-structure.

# Inverter: F = A'

- Transistor Sizing: if $\mu_N = 2\mu_P$, $V_{THN} = -V_{THP}$, $L_{MIN} = 0.18\mu m$ to make $V_{LT} = 0.5V_{DD}$ ➔ $(W/L)_P = ?$, $(W/L)_N = ?$

# 2-Input NOR / NAND Gate




(a) 2-input NOR gate (b) 2-input NAND gate

- Transistor Sizing: if $\mu_N = 2\mu_P$, $V_{THN} = -V_{THP}$, $L_{MIN} = 0.18\mu m$
  to make $V_{LT} = 0.5V_{DD}$ in worst case ➔ $(W/L)_P$ = ?, $(W/L)_N$ = ?

# 4-Input NOR / NAND Gate

4-NOR: $F = (A+B+C+D)'$

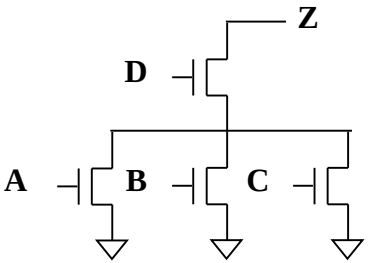
4-NAND: $F = (A \cdot B \cdot C \cdot D)'$

- Transistor Sizing: if $\mu_N = 2\mu_P$, $V_{THN} = -V_{THP}$, $L_{MIN} = 0.18\mu m$
  to make $V_{LT} = 0.5V_{DD}$ in worst case ➔ $(W/L)_P = ?$, $(W/L)_N = ?$

# Design Example: Z = [(A+B+C)·D]'

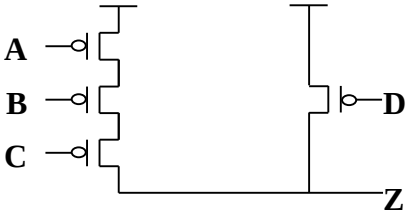
n-MOS logic :

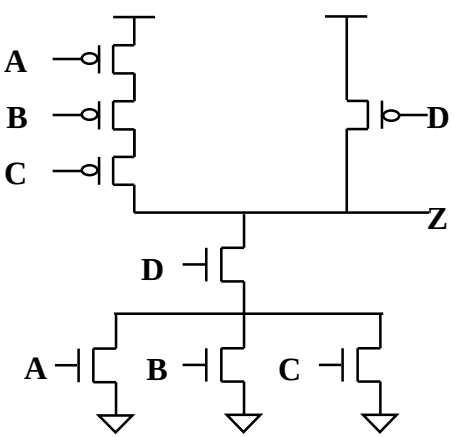
0's function = Z'
= (A+B+C)·D




p-MOS logic :

1's function = Z
= A'·B'·C'+D'



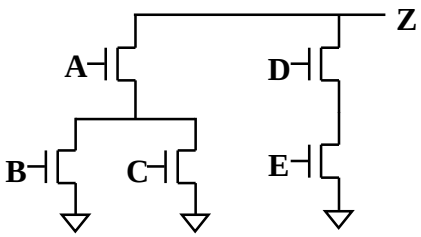




- Transistor Sizing: if $\mu_N = 2\mu_P$, $V_{THN} = -V_{THP}$, $L_{MIN} = 0.18\mu m$
  to make $V_{LT} = 0.5V_{DD}$ in worst case ➔ $(W/L)_P$ = ?, $(W/L)_N$ = ?

# Design Example: Z = [A(B+C)+D·E]'

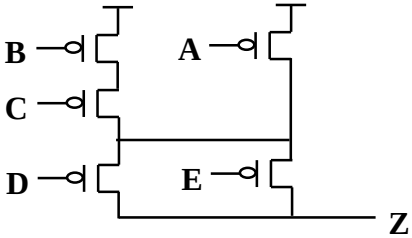
n-MOS logic :

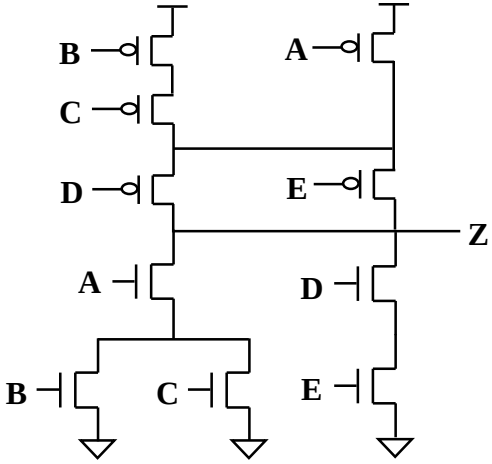
0's function = A(B+C)+D·E




p-MOS logic :

1's function = (A'+B'·C')(D'+E')




- Transistor Sizing: if $\mu_N = 2\mu_P$, $V_{THN} = -V_{THP}$, $L_{MIN} = 0.18\mu m$ to make $V_{LT} = 0.5V_{DD}$ in worst case ➔ $(W/L)_P$ = ?, $(W/L)_N$ = ?

# Features of Complementary CMOS Gate

- ✓ **In steady-state condition, no direct current path from $V_{DD}$ to $V_{SS}$**
- ✓ **High noise margin ($V_{OH} \approx V_{DD}$, $V_{OL} \approx V_{SS}$)**
- ✓ **Easy to design**
- ✓ **Easy to cascade**
- ✓ **Easy to implement circuit for low voltage application**
- ✓ **Generally requires a large circuit area**