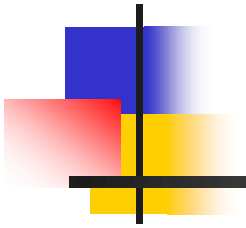

Electronic Circuits Design

Lecture – 13

- ***Positive-Edge Triggered D Flip-Flop using Transmission Gate***
- ***Counter***
- ***Shift Register***

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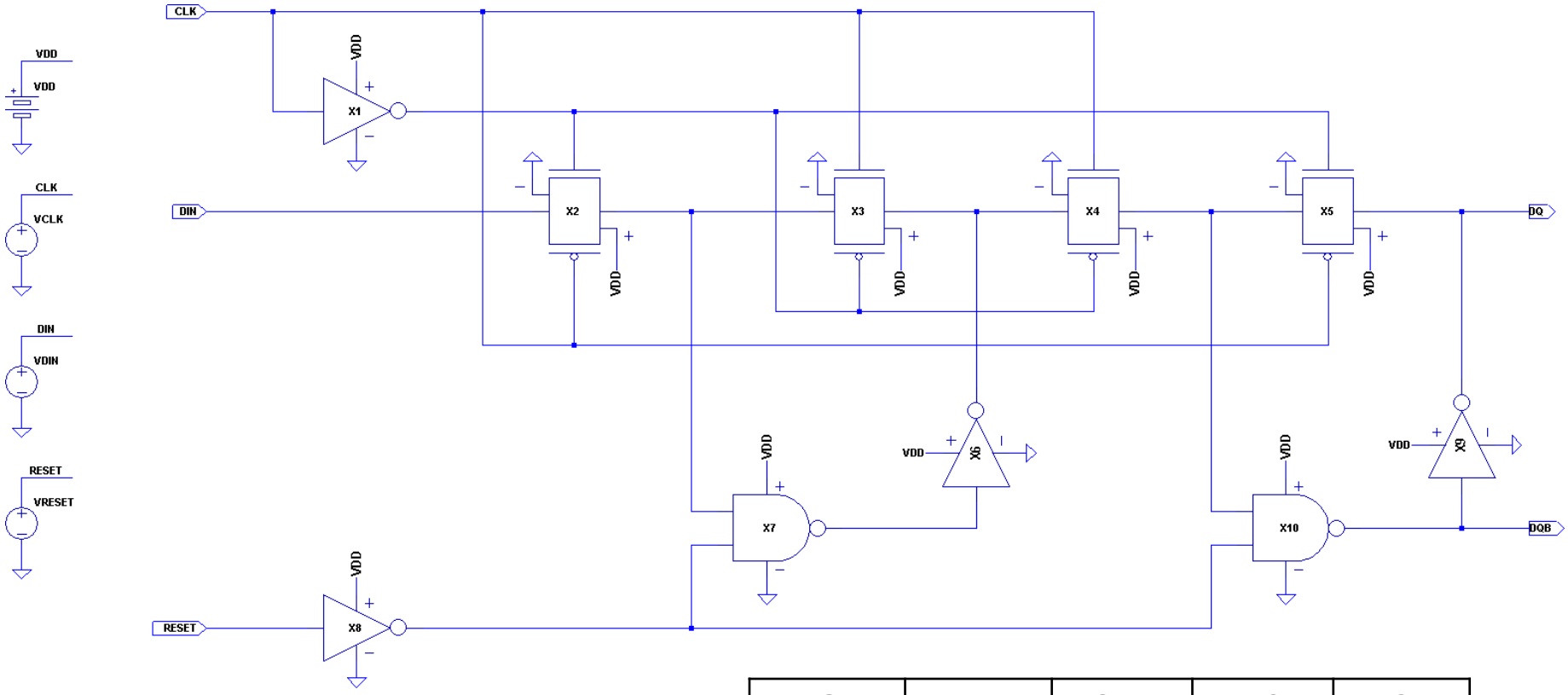
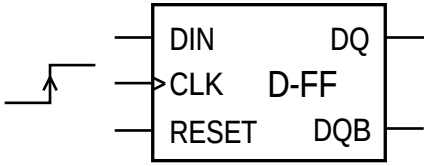
P-E Triggered D-FF using Transmission Gate





RESET	DIN	CLK	DQ	DQB
H	X	X	L	H
L	L	↑	L	H
L	H	↑	H	L

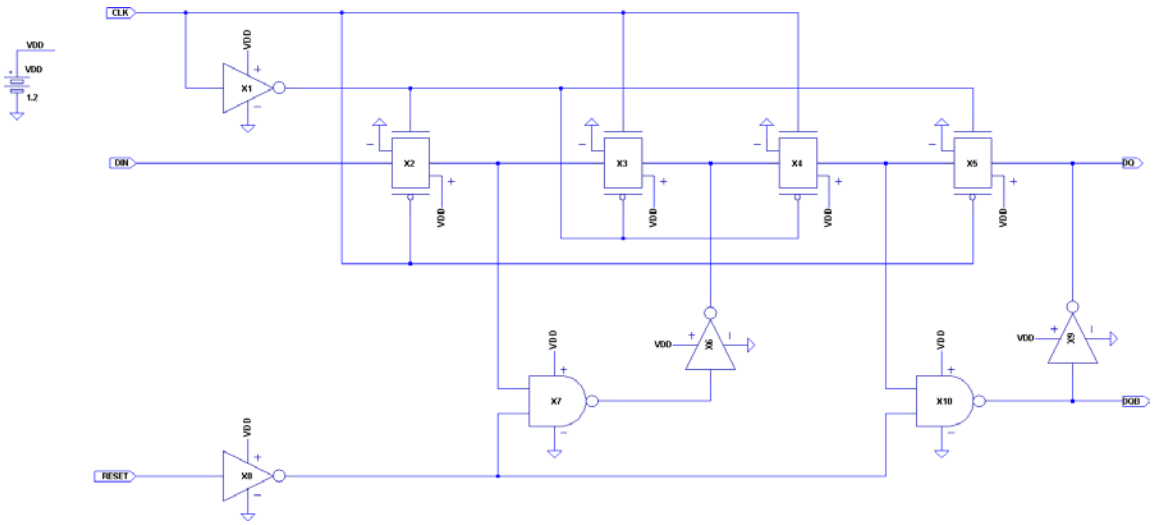
Lab-1: P-E Triggered D-FF using T-G

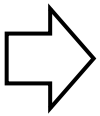
❖ **Simulation Condition**

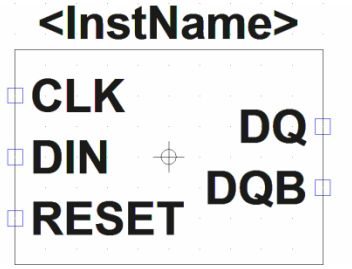
- **CMOS model parameter: MOSIS/TSMC_0.18µm**
- **VDD = 1.2 V**
- **Transmission gate (X2, X3, X4, X5): W_P/L_P = 1.5µm/0.18µm, W_N/L_N = 0.6µm/0.18µm**
- **2-input NAND (X7, X10): W_P/L_P = 1.5µm/0.18µm, W_N/L_N = 1.2µm/0.18µm**
- **Inverter (X1, X6, X8, X9): W_P/L_P = 1.5µm/0.18µm, W_N/L_N = 0.6µm/0.18µm**
- **VCLK = PULSE(0 1.2V 9.5ns 0.5ns 0.5ns 9.5ns 20ns)**
- **VDIN = PULSE(0 1.2V 4.5ns 0.5ns 0.5ns 19.5ns 40ns)**
- **VRESET = PULSE(1.2V 0 2.5ns 0.5ns 0.5ns 84.5ns 200ns)**
- **Transient analysis from 0 to 120 ns**

1) **Create the LTSpice schematic of the positive-edge triggered D flip-flop using transmission gate.**
2) **Obtain a plot of RESET, DIN, CLK, DQ and DQB versus time.**
3) **Verify the logic functionality.**
4) **Measure $T_{CLK\text{-}DQ}$ and $T_{CLK\text{-}DQB}$ respectively.**
5) **Make comments if you need.**

How to Make and Call Circuit Symbol ?





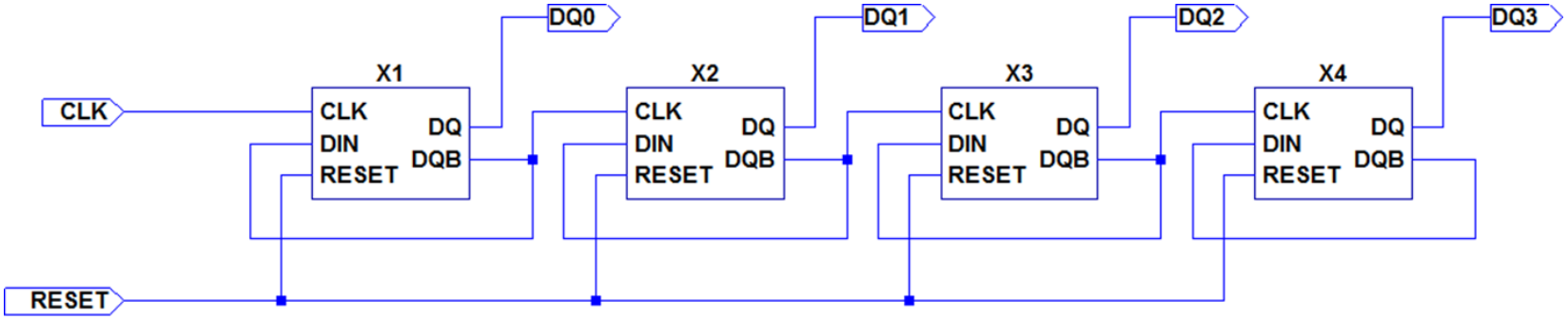


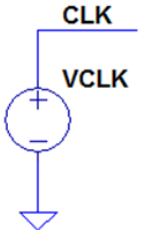
- **Step 1:** In LTSpice schematic, delete the control signal sources and any SPICE directive text. But leave the power supply.

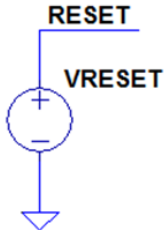
- **Step 2:** Left click on “Hierarchy” and select “Open this Sheet’s Symbol”, then click “Yes”. This will make the circuit symbol.

- **Step 3:** To call the symbol, left click on the component symbol in the schematic editor toolbar. Search directory structure for desired circuit element. Left click on OK. Move the mouse to the position you want to place it. Left click to place it.

Divide-by-16 Counter







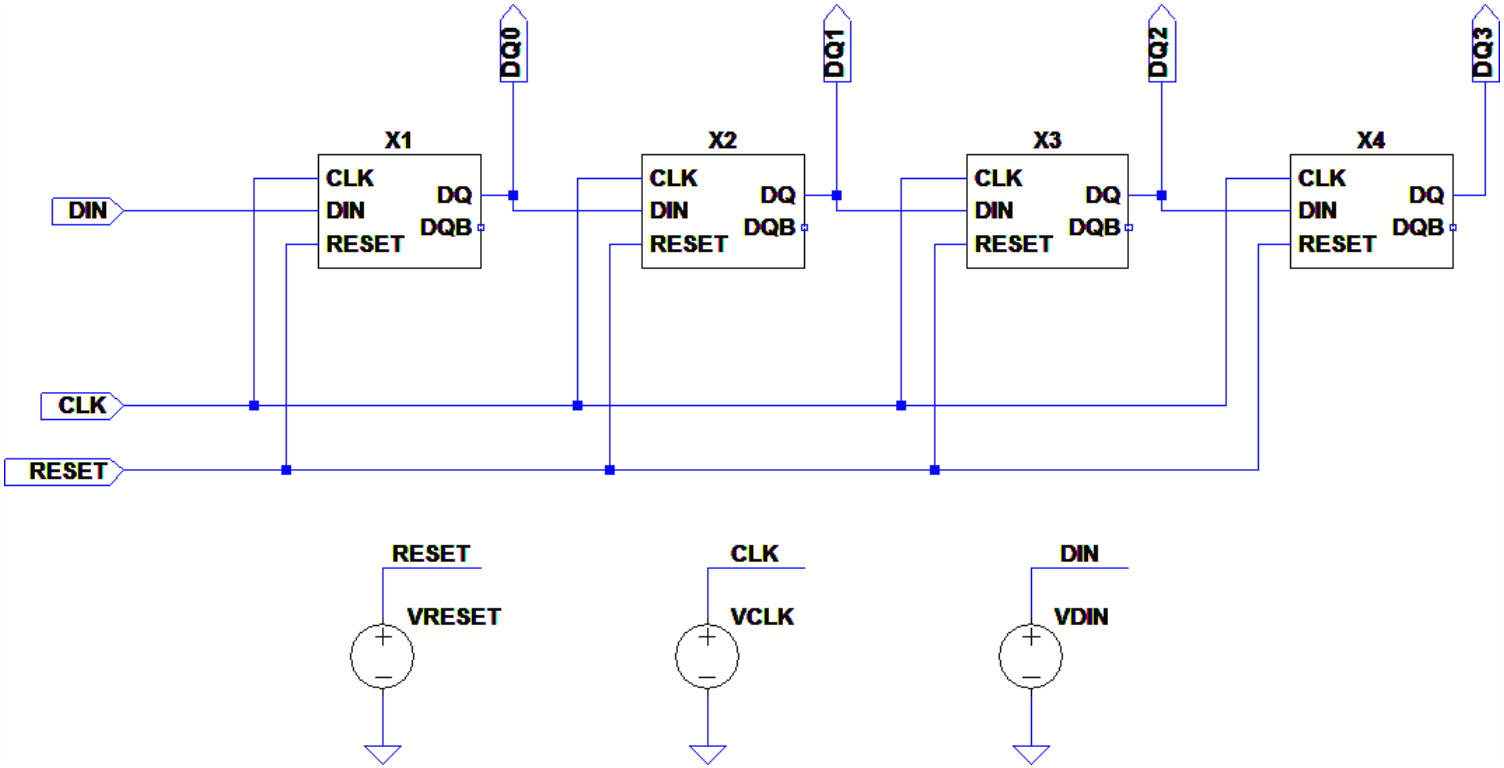
RESET	CLK	DQ3	DQ2	DQ1	DQ0
H	X	L	L	L	L
L	1↑	L	L	L	H
L	2↑	L	L	H	L
L	3↑	L	L	H	H
:	:	:	:	:	:
L	15↑	H	H	H	H

Lab-2: Divide-by-16 Counter

- **Simulation Condition**
  - **CMOS model parameter: MOSIS/TSMC_0.18µm**
  - **VDD = 1.2 V**
  - **VCLK = PULSE(0 1.2V 24.5ns 0.5ns 0.5ns 9.5ns 20ns)**
  - **VRESET = PULSE(1.2V 0 4.5ns 0.5ns 0.5ns 654.5ns 795ns)**
  - **Transient analysis from 0 to 700 ns**

1) **Create the LTSpice schematic of the divide-by-16 counter using D-FF symbol of Lab-1.**
2) **Obtain a plot of RESET, CLK, DQ0, DQ1, DQ2 and DQ3 versus time.**
3) **Verify the logic functionality.**
4) **Change the clock frequency to 500MHz such as VCLK = PULSE(0 1.2V 6ns 0.05ns 0.05ns 0.95ns 2ns), then obtain a plot of RESET, CLK, DQ0, DQ1, DQ2 and DQ3 versus time. Does the counter function properly ?**
5) **Make comments if you need.**

Serial-In Parallel-Out Shift Register



Lab-3: Serial-In Parallel-Out Shift Register

❖ **Simulation Condition**

- **CMOS model parameter: MOSIS/TSMC_0.18µm**
- **VDD = 1.2 V**
- **VRESET = PULSE(1.2V 0 4.5ns 0.5ns 0.5ns 374.5ns 482ns)**
- **VCLK = PULSE(0 1.2V 24.5ns 0.5ns 0.5ns 9.5ns 20ns)**
- **VDIN = PULSE(0 1.2V 19.5ns 0.5ns 0.5ns 29.5ns 120ns)**
- **Transient analysis from 0 to 450 ns**

1) **Create the LTSpice schematic of the serial-in parallel-out 4-bit shift register using D-FF symbol of Lab-1.**
2) **Obtain a plot of RESET, DIN, CLK, DQ0, DQ1, DQ2 and DQ3 versus time.**
3) **Verify the logic functionality.**
4) **Change the clock frequency to 1GHz such as VCLK = PULSE(0 1.2V 12ns 0.05ns 0.05ns 0.45ns 1ns), then obtain a plot of RESET, DIN, CLK, DQ0, DQ1, DQ2 and DQ3 versus time. Does the shift register function properly ?**
5) **Make comments if you need.**