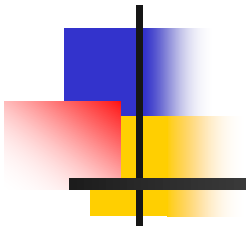


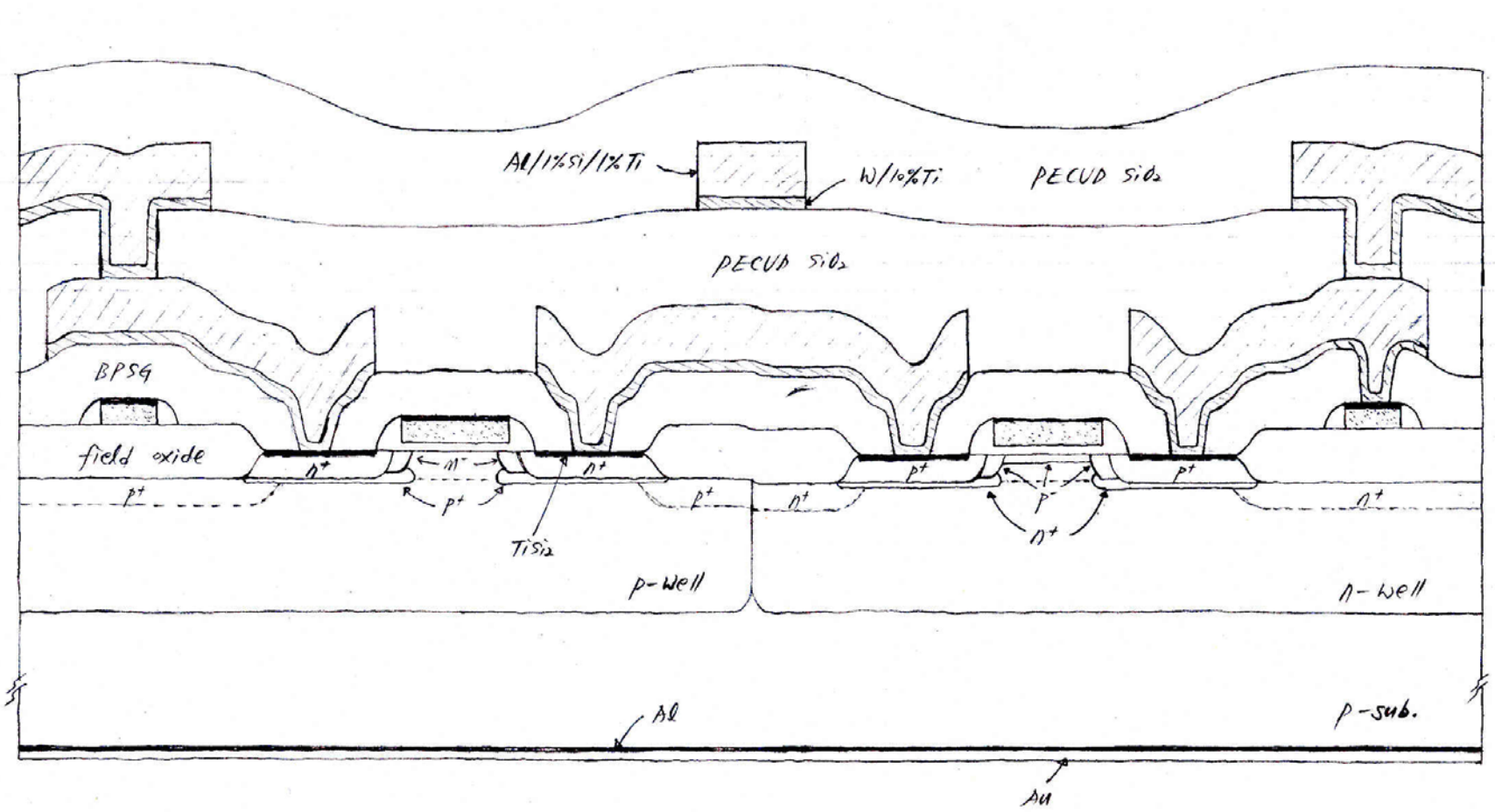
Electronic Circuits Design

Lecture – 1

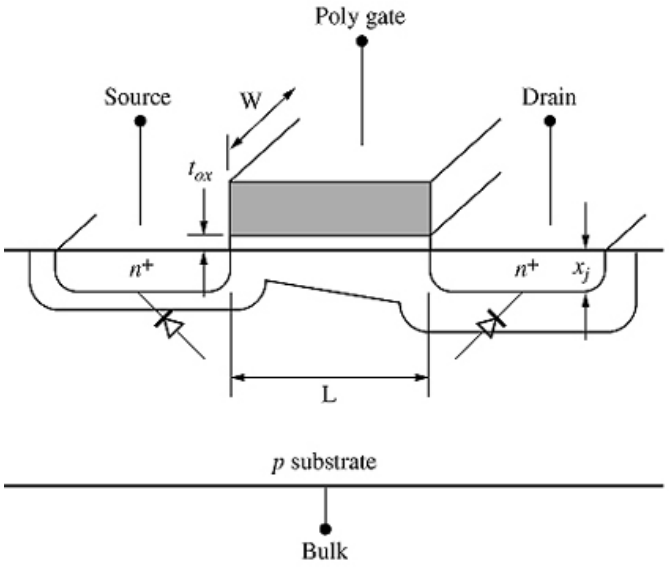
- ***MOS I-V Characteristics***
- ***MOS C-V Characteristics***

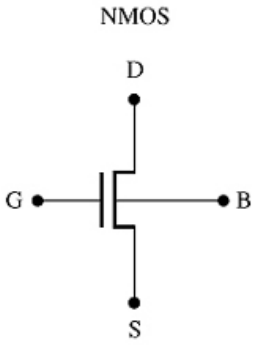
Yeonbae Chung
School of Electronics Engineering
Kyungpook National University

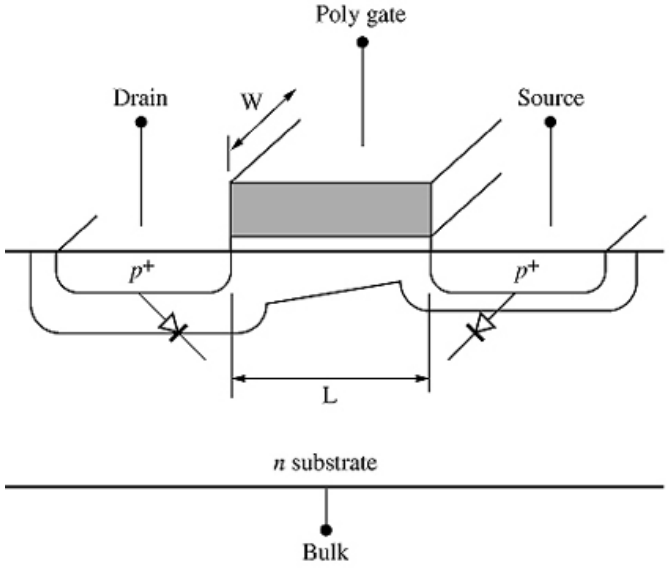
CMOS Cross Sectional View

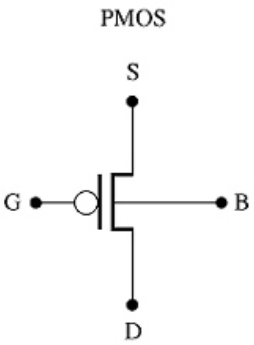


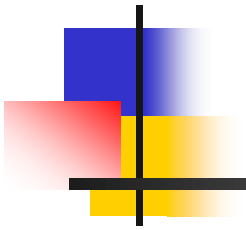
Symbol of n-MOS and p-MOS







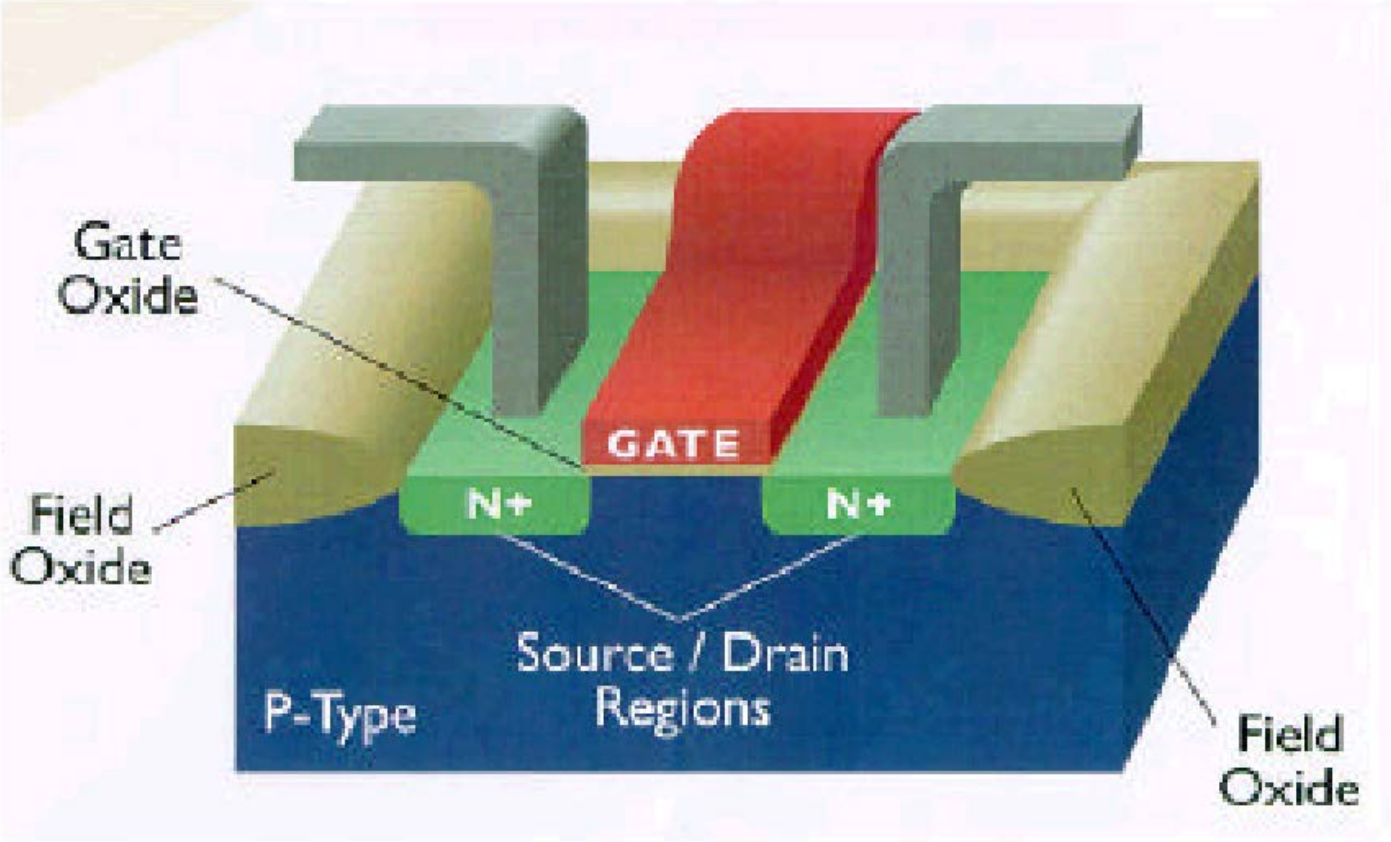




MOSFET I-V Characteristics

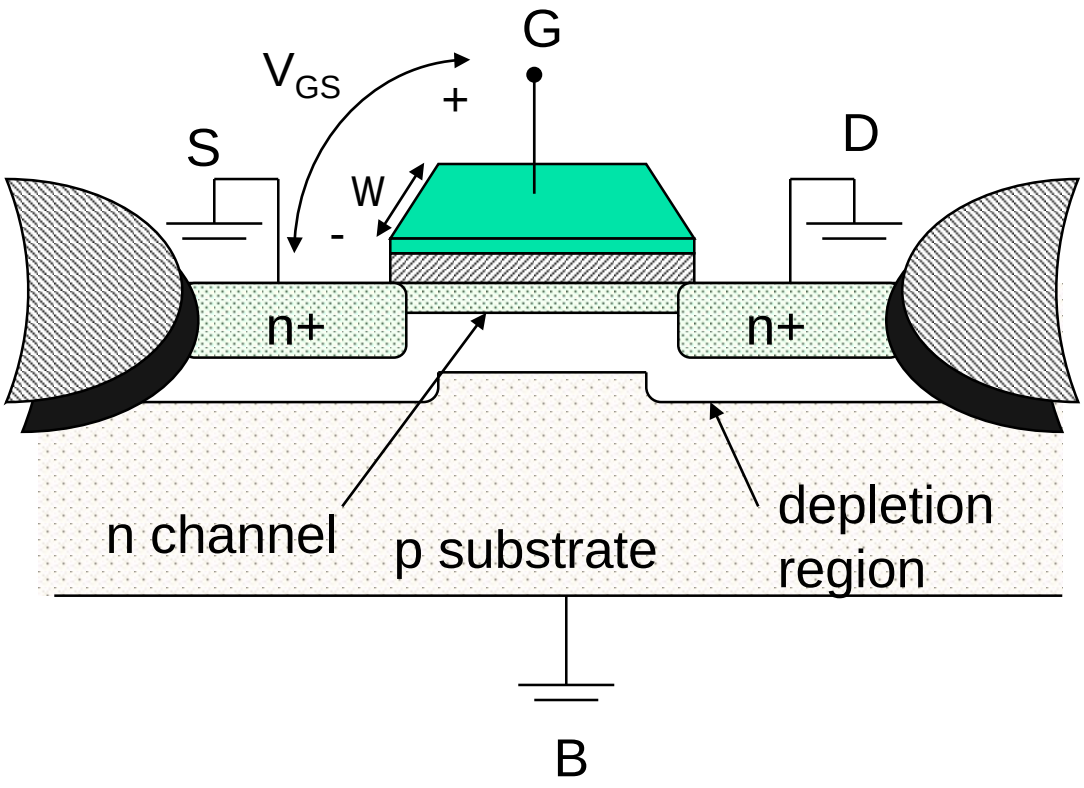
n-MOSFET

- We are focusing on n-MOSFET at first



Threshold Voltage: Concept

- The value of V_{GS} where strong inversion occurs is called the threshold voltage, V_{TH}



Threshold Voltage

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

where

- V_{TH0} is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process: difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.
- V_{SB} is the source-to-body voltage
- $\phi_F = V_T \ln(N_A/n_i)$ is the Fermi potential ($V_T = kT/q = 26mV$ at 300K is the thermal voltage; N_A is the body doping concentration; $n_i \approx 1.5 \times 10^{10}$ cm^{-3} at 300K is the intrinsic carrier concentration in pure silicon)
- $\gamma = \sqrt{(2q\varepsilon_{si}N_A)}/C_{ox}$ is the body-effect coefficient (impact of changes in V_{BS}); $\varepsilon_{si}=1.053 \times 10^{-10}$F/m is the permittivity of silicon, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance with $\varepsilon_{ox}=3.5 \times 10^{-11}$F/m

Linear Region

$\rightarrow V_{GD} > V_{TH}$

- When $V_{GS} \geq V_{TH}$, $V_{DS} < V_{GS}-V_{TH}$

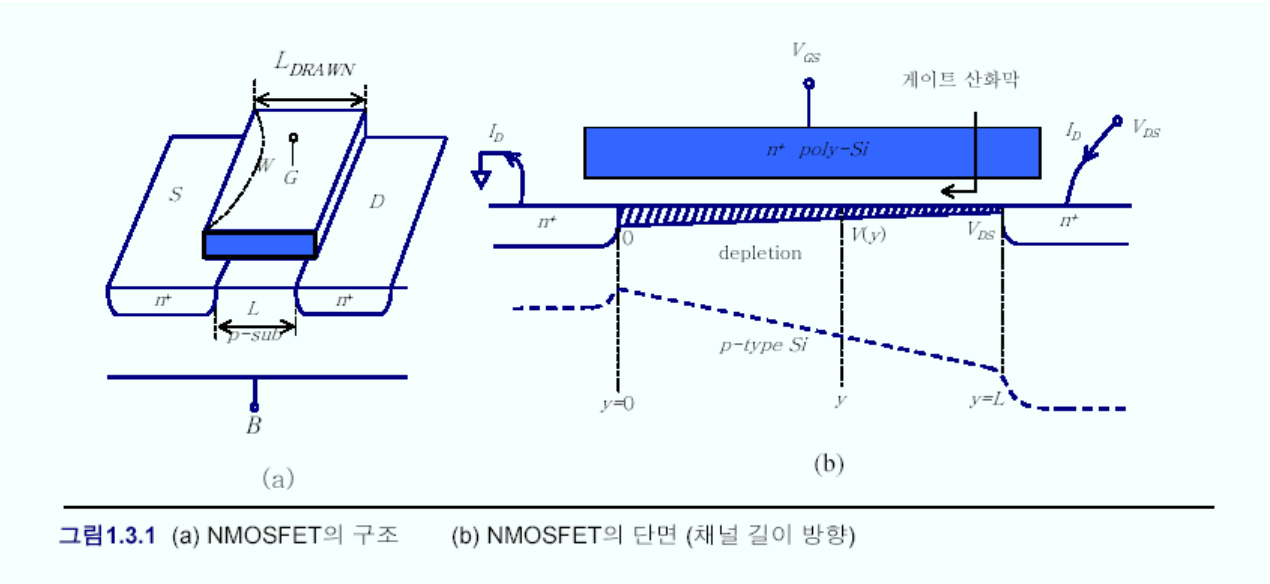


그림1.3.1 (a) NMOSFET의 구조 (b) NMOSFET의 단면 (채널 길이 방향)

$$I_D = \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH} - \frac{1}{2}V_{DS})V_{DS}$$

Saturation Region

- When $V_{GS} \geq V_{TH}$, $V_{DS} \geq V_{GS}-V_{TH}$ ($V_{GD} \leq V_{TH}$)

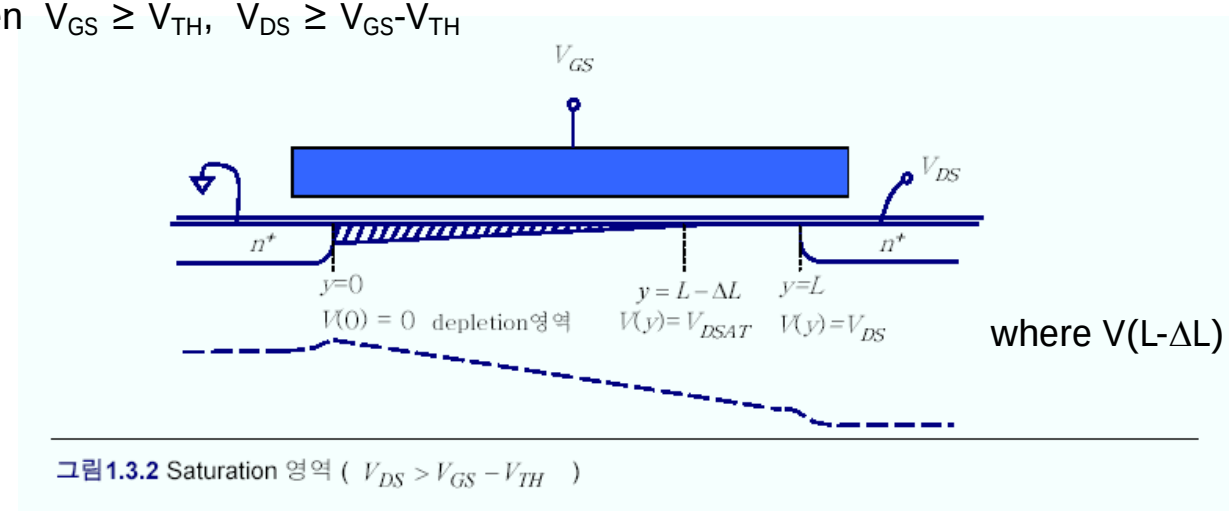


그림1.3.2 Saturation 영역 ($V_{DS} > V_{GS} - V_{TH}$)

where $V(L-\Delta L) \equiv V_{DSAT} = V_{GS} - V_{TH}$

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L-\Delta L}(V_{GS}-V_{TH})^2$$

channel length modulation

Channel Length Modulation in Spice Model

From p-n$^+$ step junction

$$\Delta L \approx \sqrt{\frac{2\varepsilon_{si}}{qN_A}\cdot(V_{DS}-V_{DSAT})}$$

where $V_{DSAT} = V_{GS} - V_{TH}$

$$\approx \lambda L V_{DS}$$

When $\Delta L/L << 1$,

$$\frac{1}{L-\Delta L} = \frac{1}{L}\cdot\frac{1}{1-\frac{\Delta L}{L}} \approx \frac{1}{L}\cdot\left(1+\frac{\Delta L}{L}\right) = \frac{1}{L}\cdot(1+\lambda V_{DS})$$

I-V Equation in SPICE Model Level-1

- Linear Region ($V_{GS} \geq V_{TH}$, $V_{DS} < V_{GS}-V_{TH}$)

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\right)V_{DS} \cdot (1 + \lambda V_{DS})$$

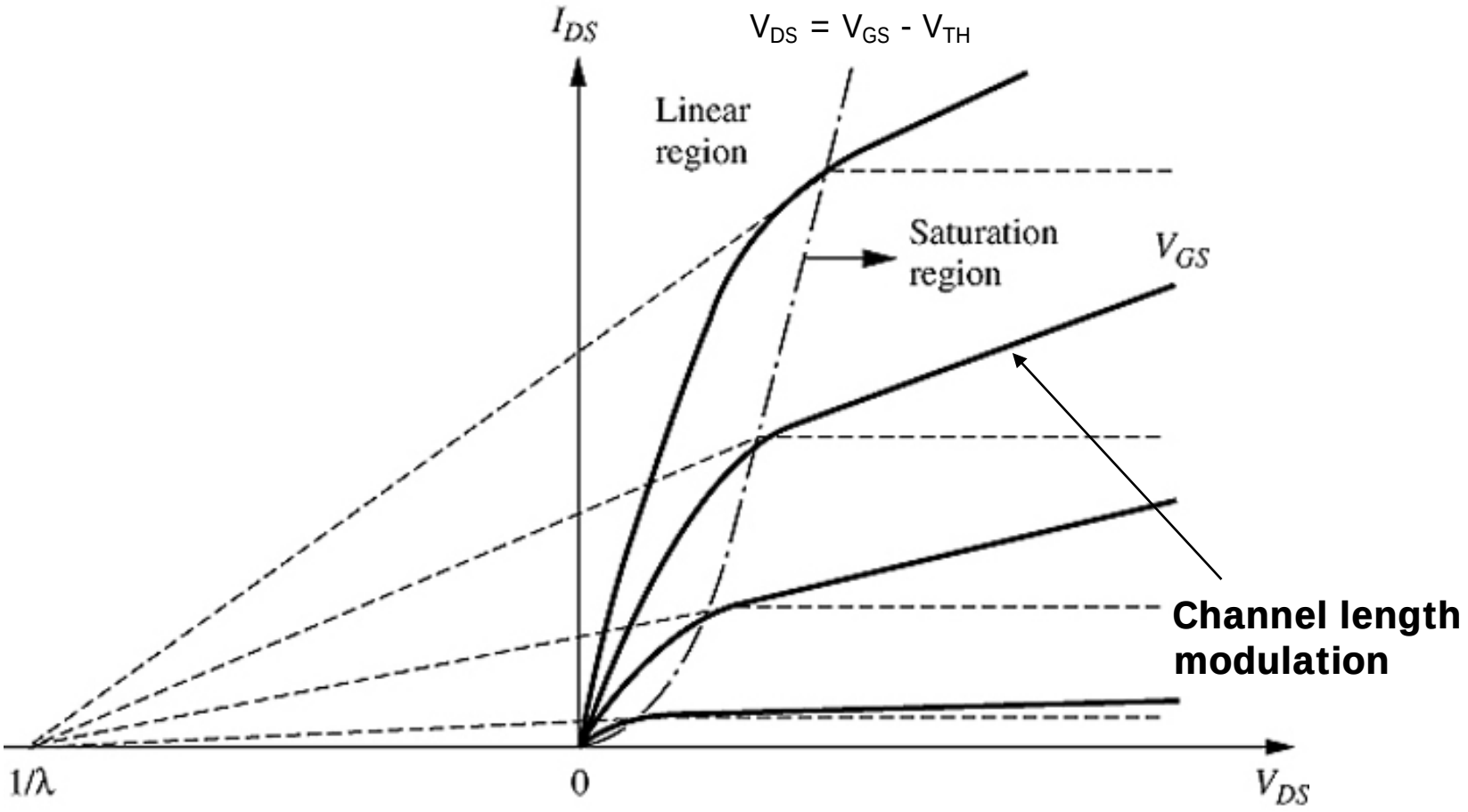
- Saturation Region ($V_{GS} \geq V_{TH}$, $V_{DS} \geq V_{GS}-V_{TH}$)

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS})$$

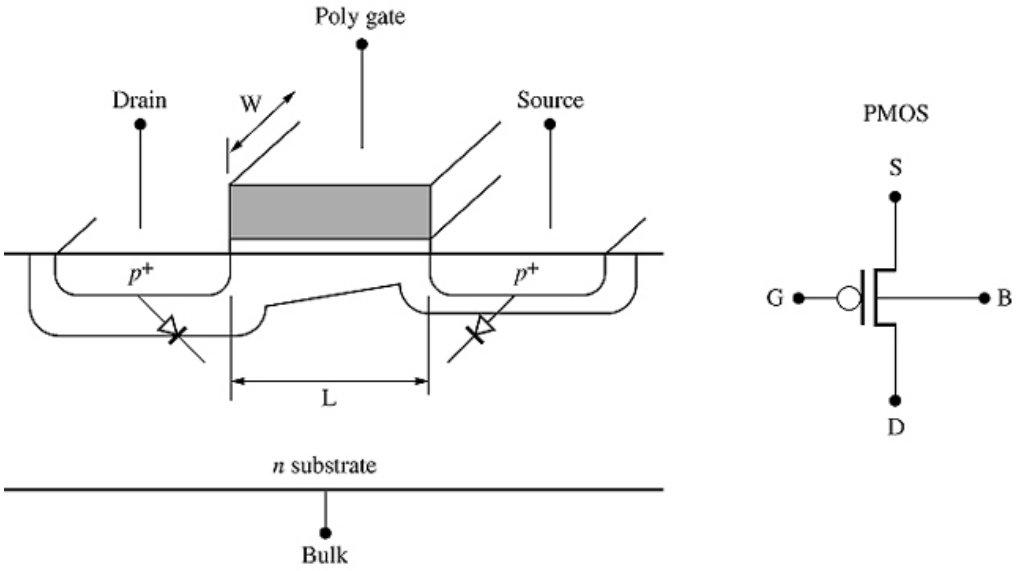
- Cutoff Region ($V_{GS} < V_{TH}$)

$$I_D = 0$$

I-V Relationship



p-MOSFET I-V



- All dopings and voltages are inverted for p-MOS
- Mobility μ_p is determined by holes
  - Typically 2-3 times lower than that of electrons μ_n
  - μ_n = 340 cm^2/V·s, μ_p = 130 cm^2/V·s in AMI 0.35 µm process
- Thus PMOS must be wider W to provide same current
  - Typically, assume $\mu_n / \mu_p = 2.5$

I-V Equation in p-MOSFET

- Linear Region ($V_{SG} \geq |V_{THP}|$, $V_{SD} < V_{SG} - |V_{THP}|$)

$$I_D = \mu_P C_{OX} \frac{W}{L}(V_{SG} - |V_{THP}| - \frac{1}{2}V_{SD})V_{SD}(1 + |\lambda_P| V_{SD})$$

- Saturation Region ($V_{SG} \geq |V_{THP}|$, $V_{SD} \geq V_{SG} - |V_{THP}|$)

$$I_D = \frac{1}{2}\mu_P C_{OX} \frac{W}{L}(V_{SG} - |V_{THP}|)^2(1 + |\lambda_P| V_{SD})$$

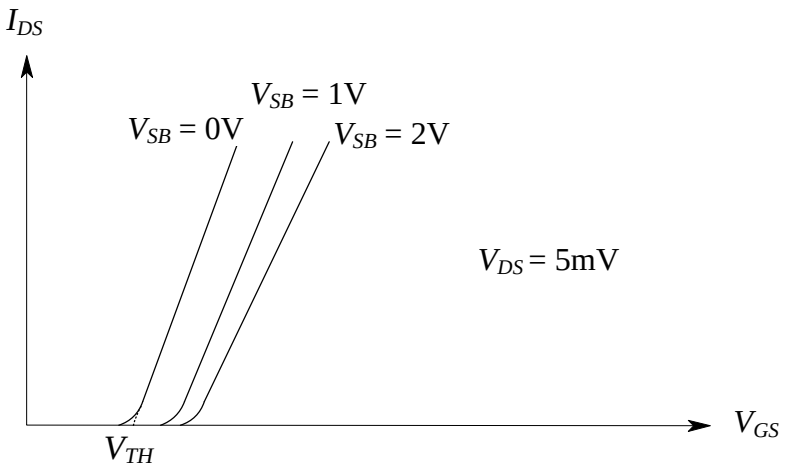
- Cutoff Region ($V_{SG} < |V_{THP}|$)

$$I_D = 0$$

Body Effect

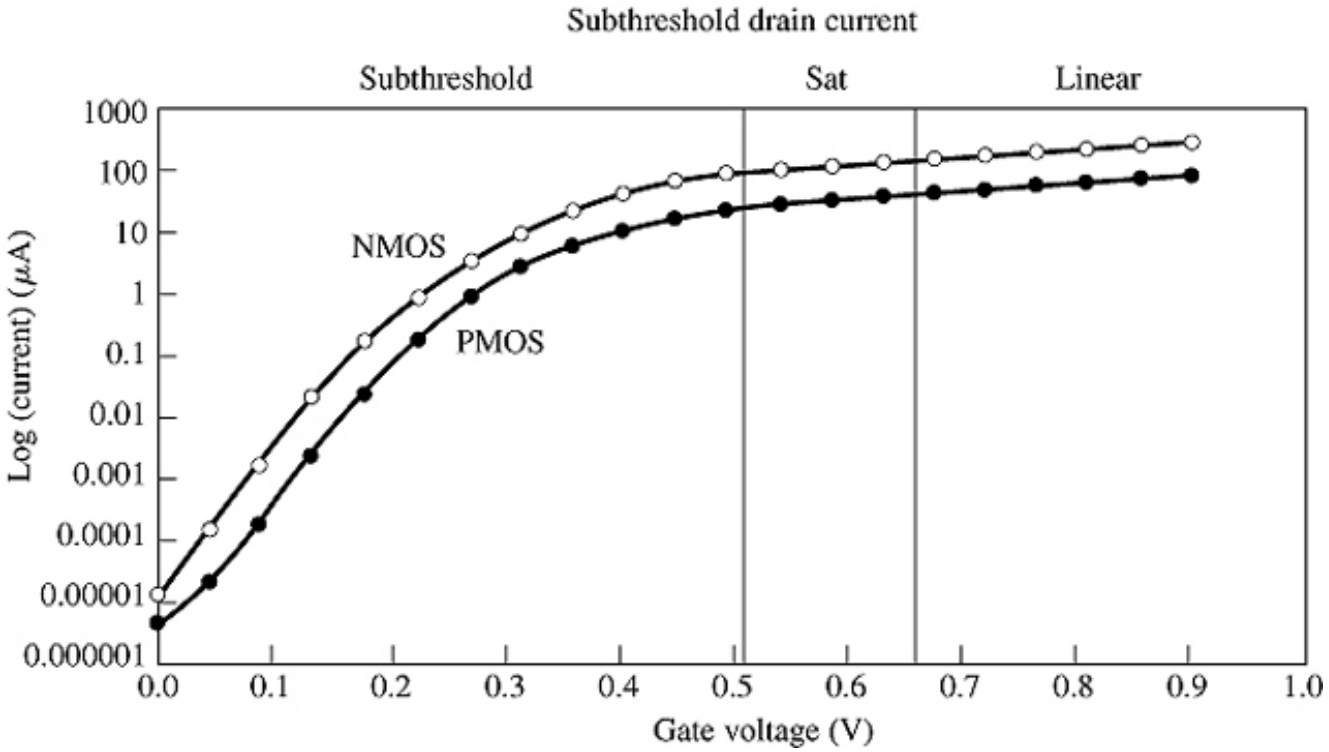
- V_{TH}: Gate voltage necessary to invert channel
- V_{TH} increases if source-to-body voltage increases because source is connected to the channel
- Increase in V_{TH} with V_{SB} is called the *body effect*

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

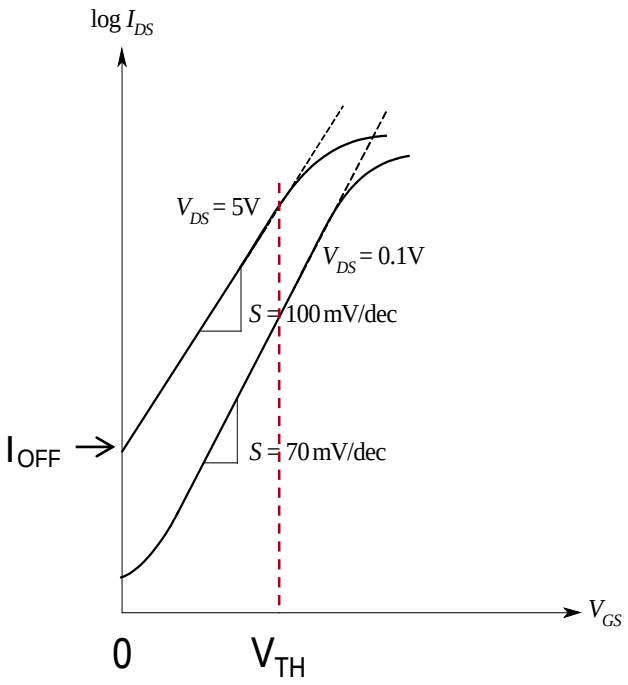


Subthreshold Conduction

- For $V_{GS} < V_{TH}$, the drain current is not zero
  - There is subthreshold conduction
  - Leakage component: critical in VLSI containing millions of transistors
  - Main source of static power consumption in CMOS VLSI



Subthreshold Current



- For $V_{GS} < V_{TH}$,

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \frac{\gamma \cdot V_T^{\,2}}{2\sqrt{2\phi_F + V_{SB}}} \cdot \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \cdot \left(1 - e^{-\frac{V_{DS}}{V_T}}\right)$$

<--- diffusion current; similar to bipolar transistor

$$V_T = \frac{kT}{q}$$; thermal voltage

$$n = 1 + \frac{C_D}{C_{ox}} + \frac{q \cdot NFS}{Cox}$$

where C_D = channel depletion capacitance per unit area
NFS = surface state density

- For $V_{DS} >> V_T$ and $V_{GS} = 0$,

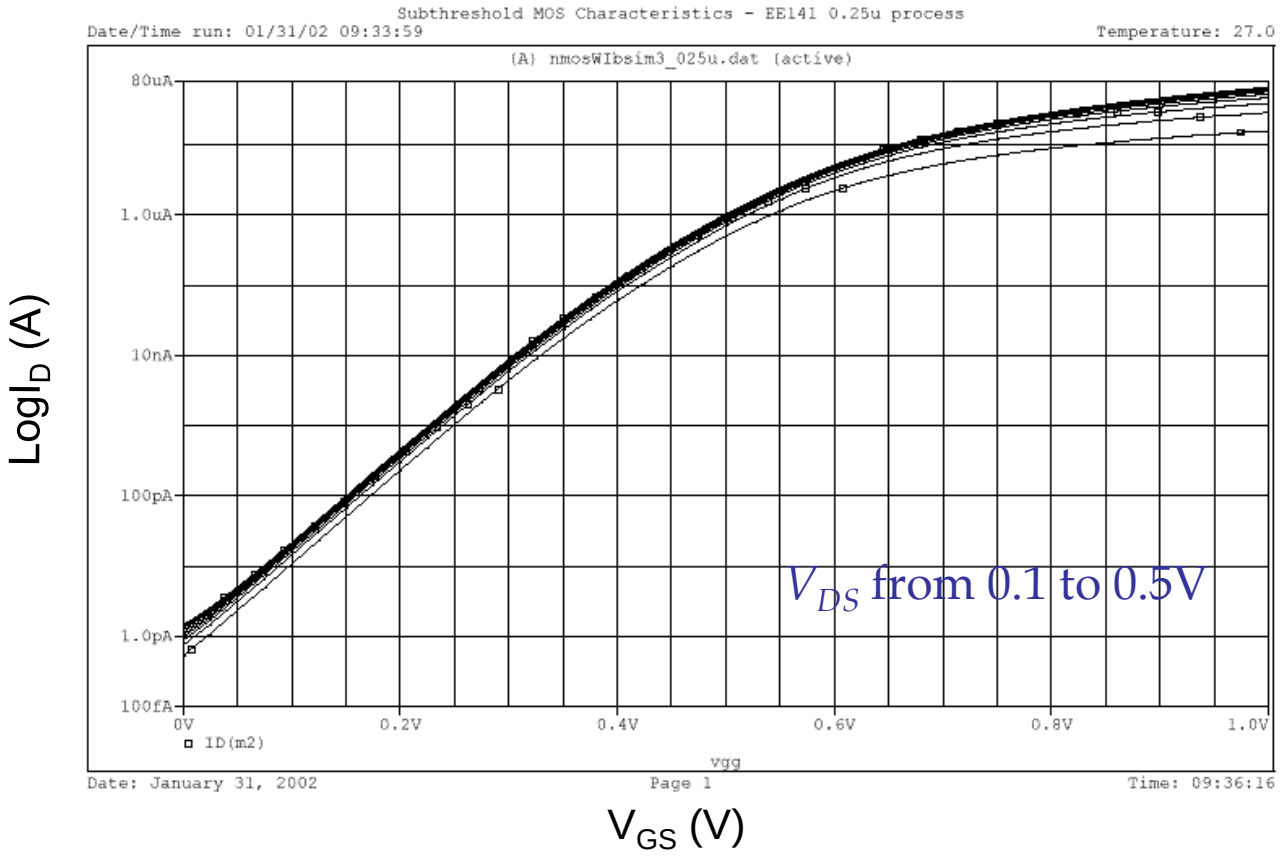
$$I_{D.OFF} = \mu_n C_{ox} \frac{W}{L} \cdot \frac{\gamma \cdot V_T^{\,2}}{2\sqrt{2\phi_F + V_{SB}}} \cdot \exp\left(\frac{-V_{TH}}{nV_T}\right)$$

$= f(V_{SB}, V_{TH})$

- Subthreshold swing:
  S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

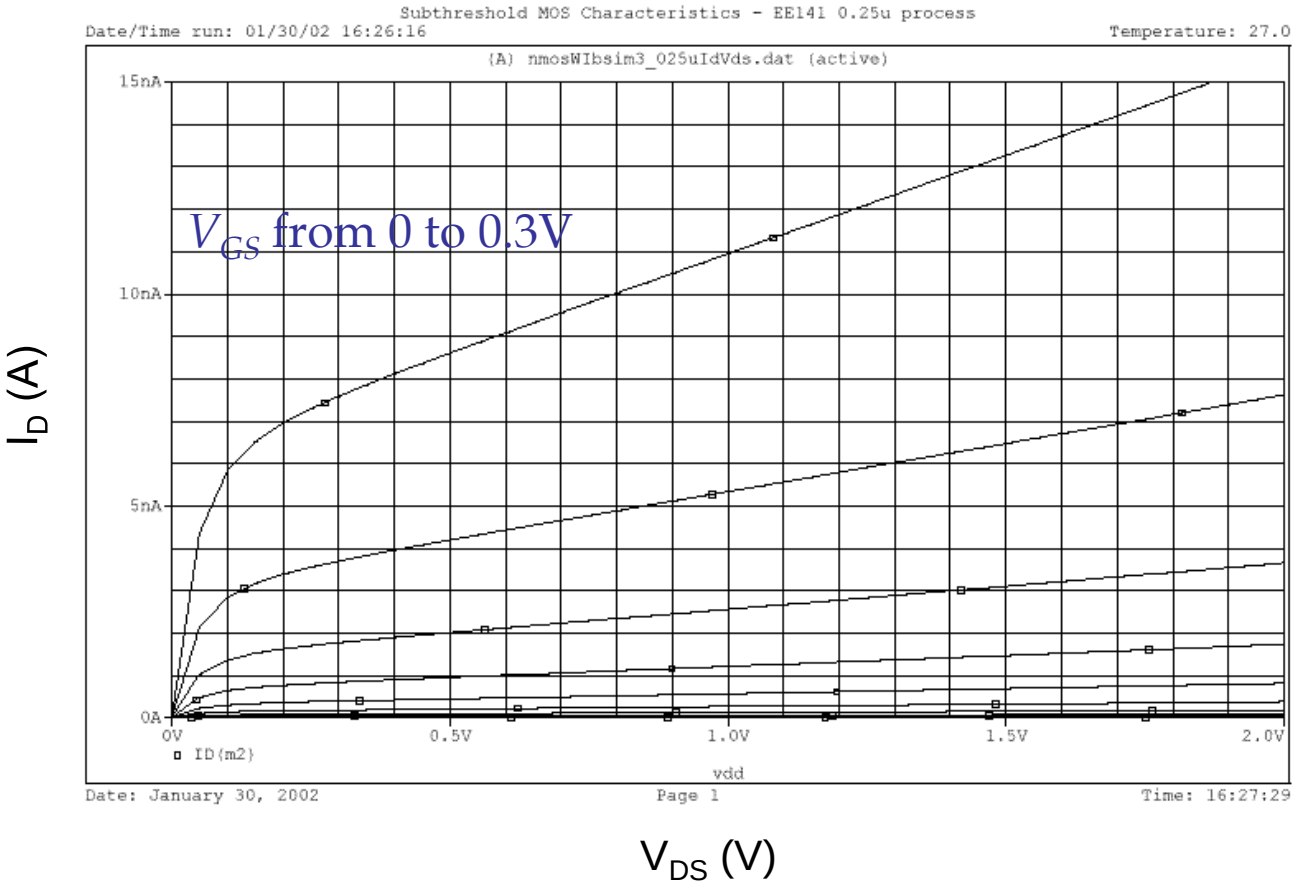
Practical Subthreshold I_D vs V_{GS}

- 0.25 μm CMOS technology



Practical Subthreshold I_D vs V_{DS}

- 0.25 μm CMOS technology

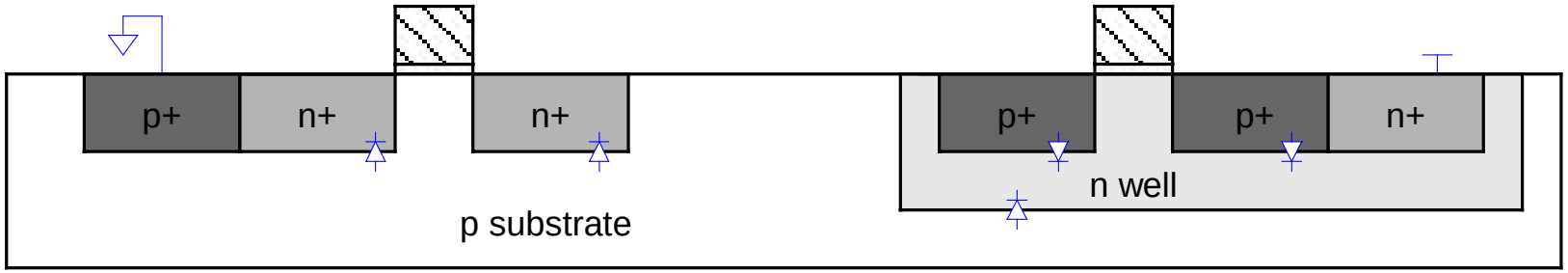


Junction Leakage

- Reverse-biased p-n junctions have some leakage

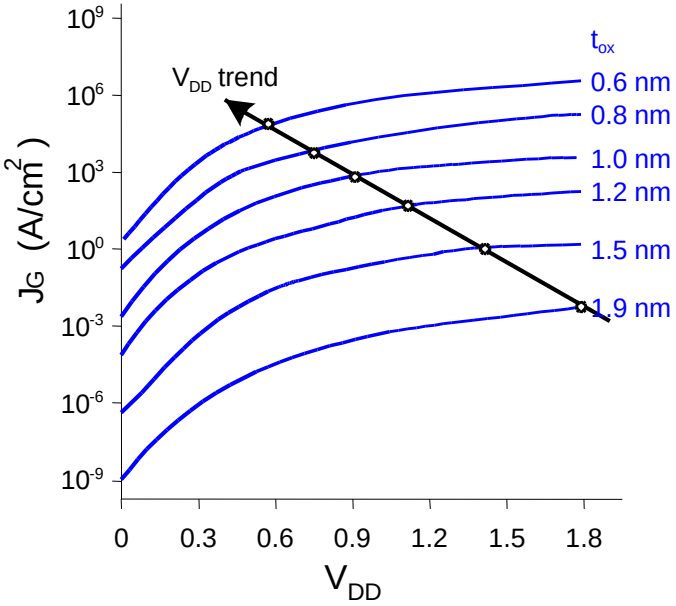
$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- I_s depends on doping level, area and perimeter of diffusion regions
  - Typically < 1 fA/μm^2



Gate Leakage

- Carriers may tunnel thorough very thin gate oxides
- Predicted tunneling current



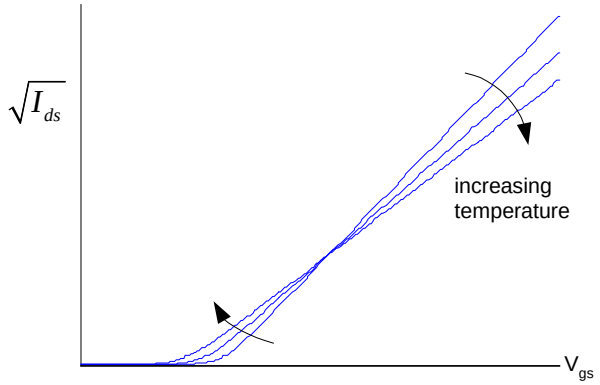
- Negligible for old CMOS process
- May soon be critically important

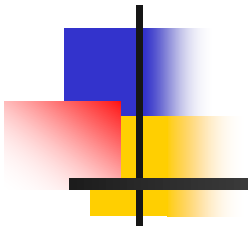
Leakage Sources

- Subthreshold conduction
  - Transistor OFF current
- Junction leakage
  - Reverse-biased p-n junction diode current
- Gate leakage
  - Tunneling through ultrathin gate dielectric
- Subthreshold leakage is the biggest source in modern transistors

Temperature Dependence

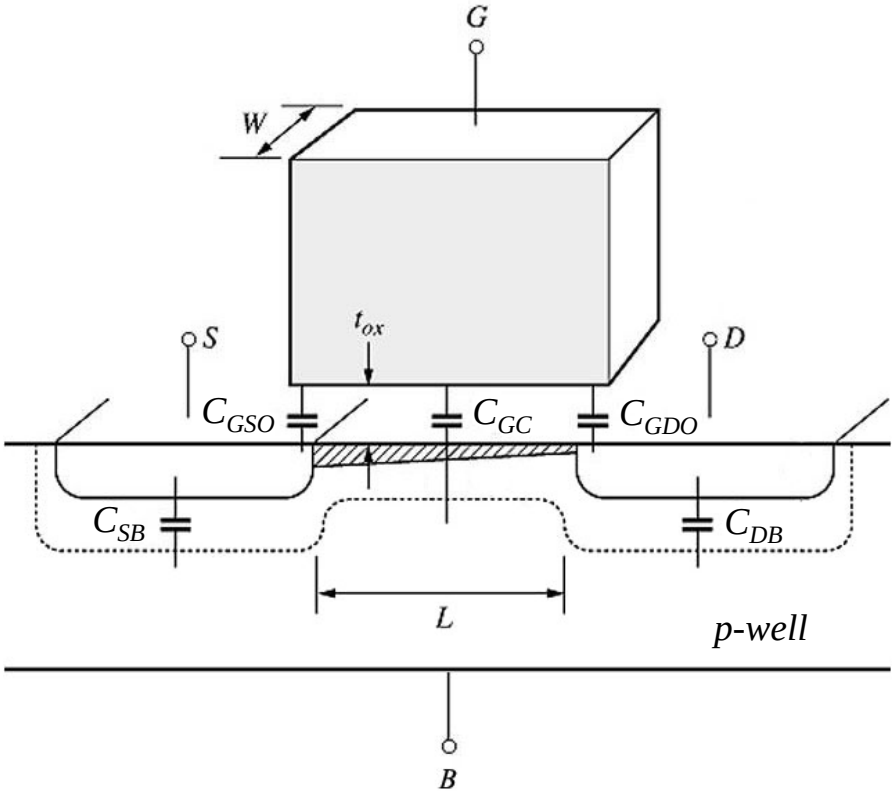
- Increasing temperature
  - Reduces mobility
  - Reduces V_{TH} **<--- due to diffusion current**
- I_{ON} decreases with temperature
- I_{OFF} increases with temperature





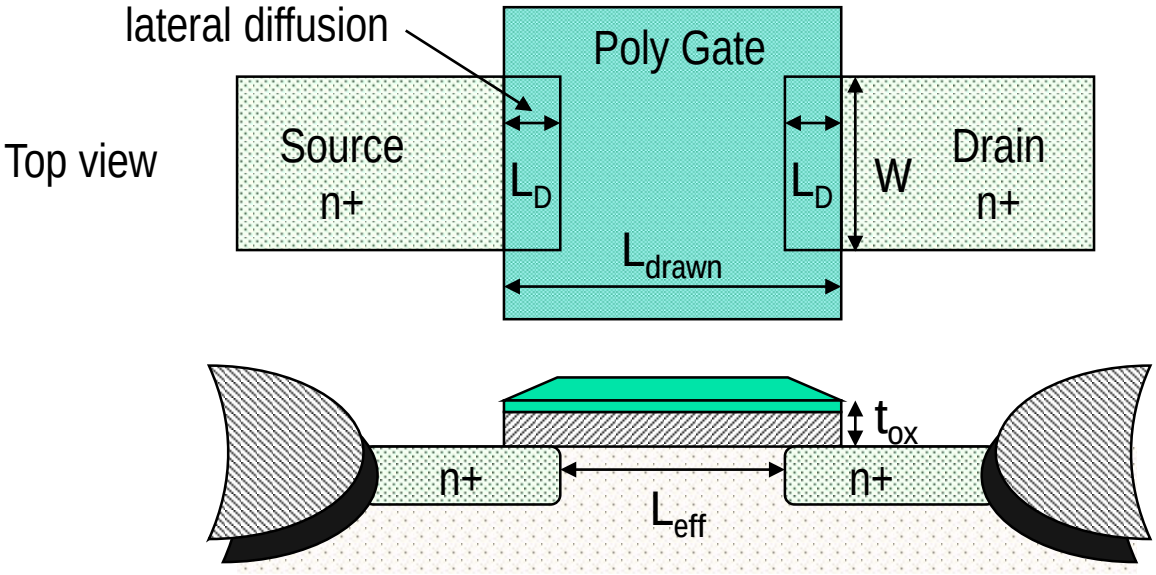
MOSFET C-V Characteristics

Parasitic Capacitances in MOS Transistor



- **Any two conductors separated by an insulator have capacitance**
  - **Overlap capacitances due to lateral diffusion**
  - **Gate-to-channel capacitance due to thin gate oxide**
  - **Source and drain capacitances due to reverse-biased pn junction**

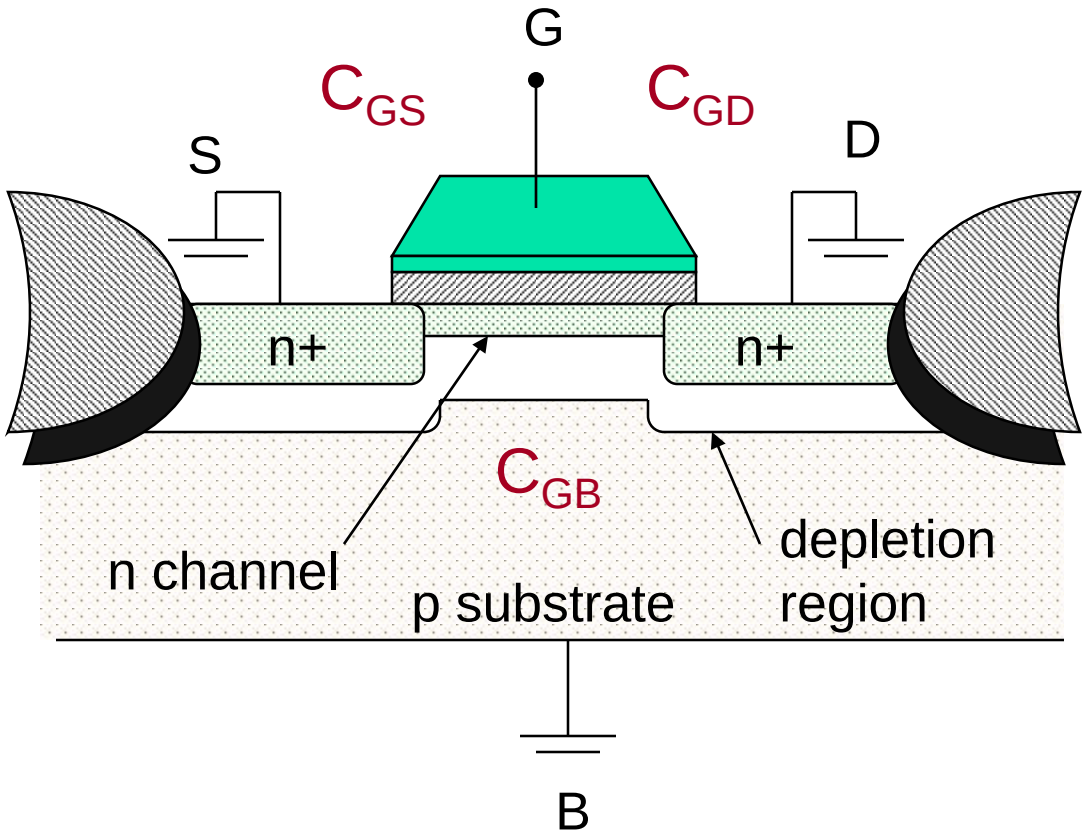
Overlap Capacitances



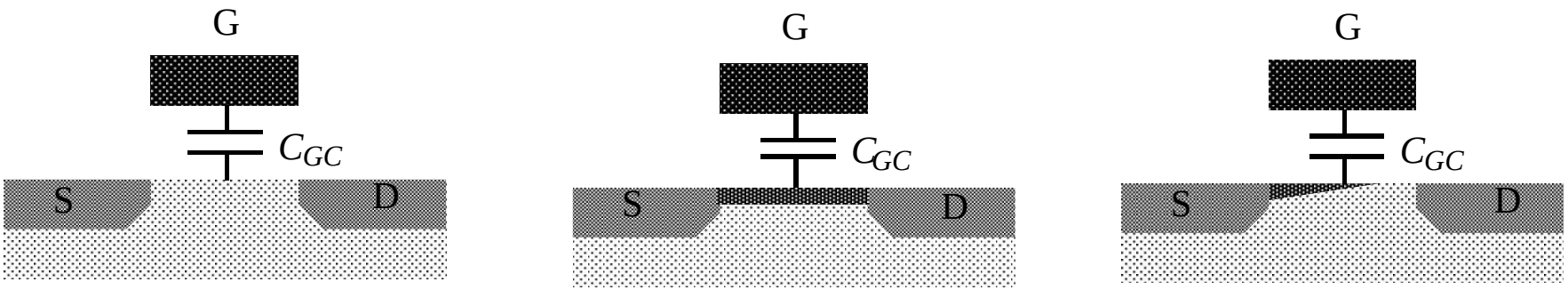
Overlap capacitance: $C_{GSO} = C_{GDO} = C_{OX} L_D W$

Gate-to-Channel Capacitance

- **The gate-to-channel capacitance depend upon the operating region and the terminal voltages**

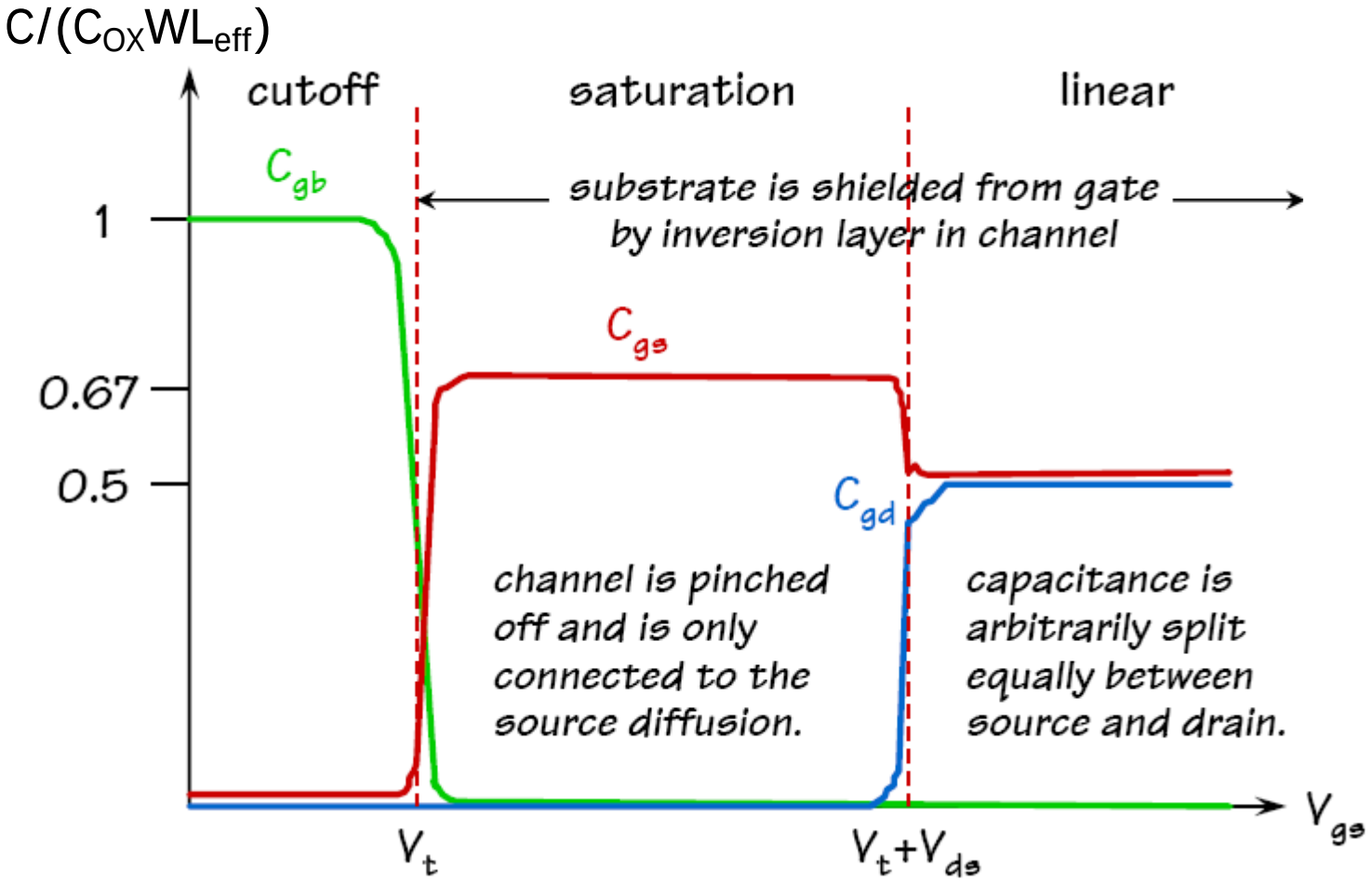


Distribution of Gate-to-Channel Capacitance



Operation Region	C_{GB}	C_{GS}	C_{GD}
Cutoff	$C_{OX}WL_{eff}$	0	0
Linear	0	$C_{OX}WL_{eff}/2$	$C_{OX}WL_{eff}/2$
Saturation	0	$(2/3)C_{OX}WL_{eff}$	0

Gate-to-Channel Capacitance



Junction Capacitance

- **The source-body and drain-body capacitances are from the reverse-biased source-body and drain-body p-n junctions.**

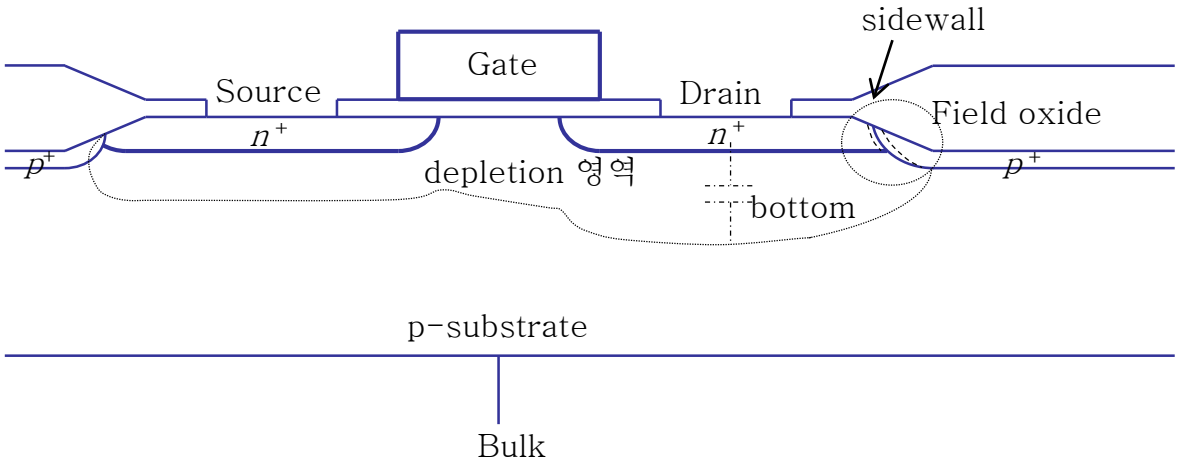
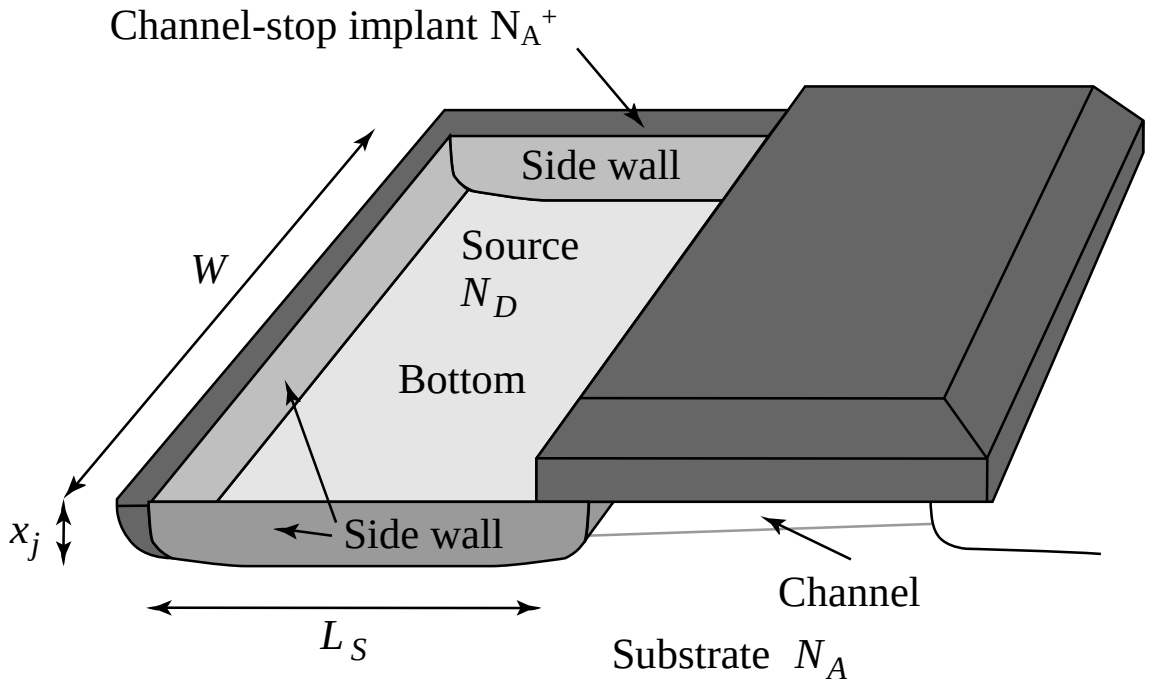


그림 2.3.3 드레인-벌크 접합의 bottom쪽과 sidewall쪽 커패시턴스

Source Junction Capacitance

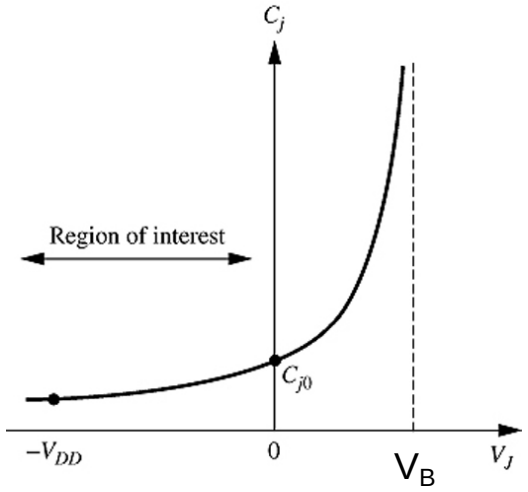


$$C_{junc} = C_{bottom} + C_{sw} = C_{JA} \times AREA + C_{JSW} \times PERIMETER$$
$$= C_{JA} L_S W + C_{JSW} (2L_S + W)$$

MOS Source/Drain Capacitance

$$C_{JA} = C_{JAO}\left(1 - \frac{V_J}{V_B}\right)^{-M_J}$$

$$C_{JSW} = C_{JSWO}\left(1 - \frac{V_J}{V_B}\right)^{-M_{JSW}}$$



C_{JAO} = zero-bias area capacitance [fF/μm^2]
C_{JSWO} = zero-bias perimeter capacitance [fF/μm]
V_J = applied junction voltage (typically < 0)
V_B = built-in potential (~ 0.6V)
M_J = grading coefficient of area junction
M_{JSW} = grading coefficient of sidewall perimeter junction } (0.3~0.5)

CDB and CSB in Spice Model

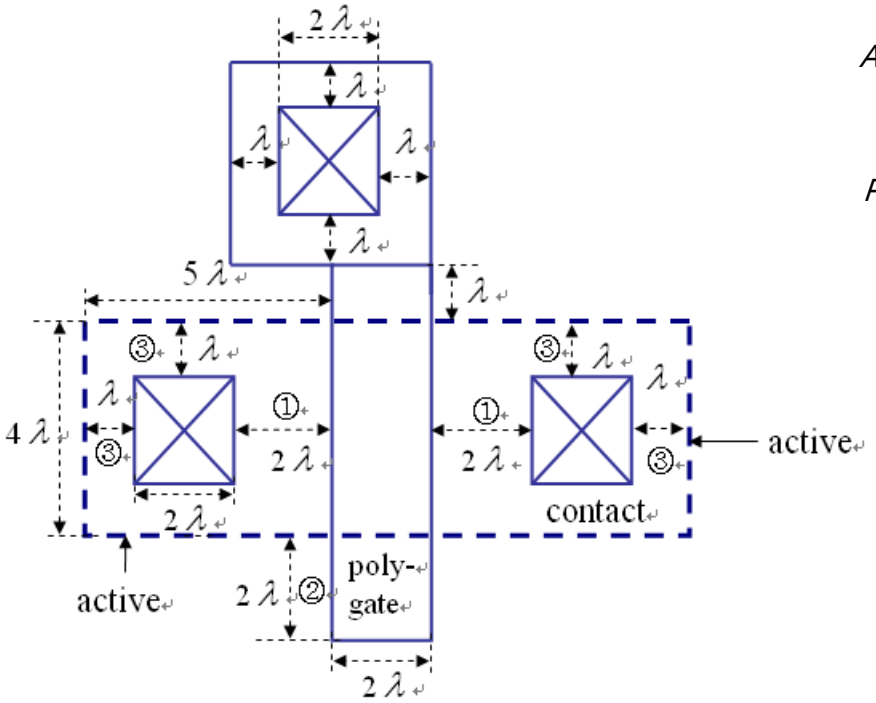


그림 2.3.2 최소크기 트랜지스터의 레이아웃 (λ = 0.2 μm)

$$AS = AD = W \times 5\lambda = 4\lambda \times 5\lambda = 20\lambda^2 = 0.8 \times 10^{-12}\, m^2$$

$$PS = PD = W + 2 \times 5\lambda = 4\lambda + 10\lambda = 14\lambda = 2.8\,\mu m$$

$$C_{DB} = AD \cdot \frac{CJ}{\left(1 - \frac{V_{BD}}{PB}\right)^{MJ}} + PD \cdot \frac{CJSW}{\left(1 - \frac{V_{BD}}{PB}\right)^{MJSW}}$$

$$C_{SB} = AS \cdot \frac{CJ}{\left(1 - \frac{V_{BS}}{PB}\right)^{MJ}} + PS \cdot \frac{CJSW}{\left(1 - \frac{V_{BS}}{PB}\right)^{MJSW}}$$

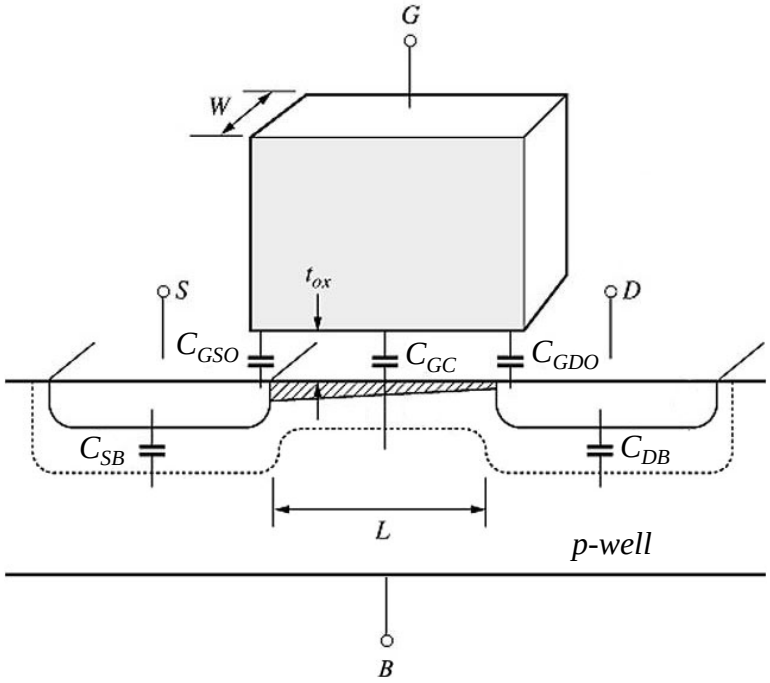
CJ = zero-potential bottom junction capacitance

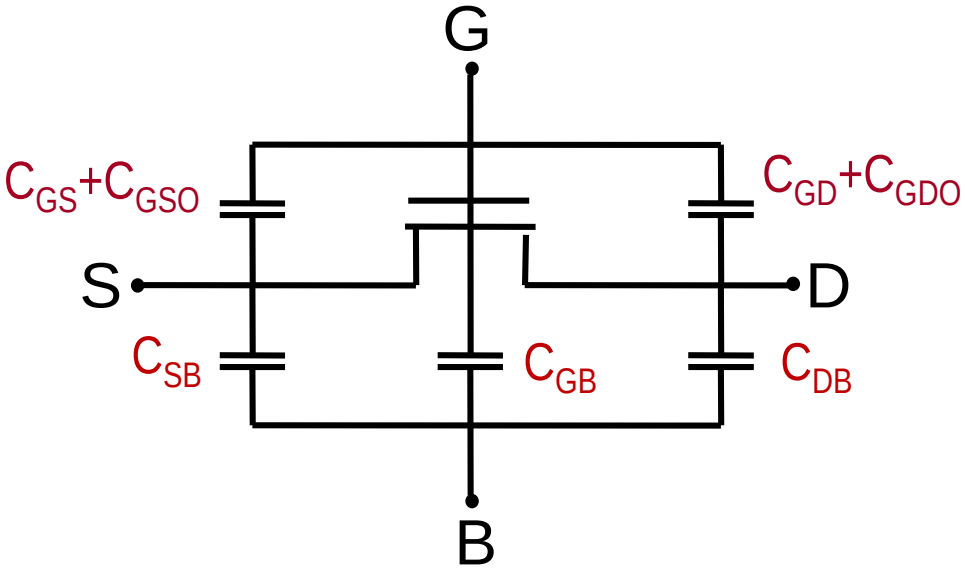
CJSW = zero-potential sidewall junction capacitance

PB = built-in potential

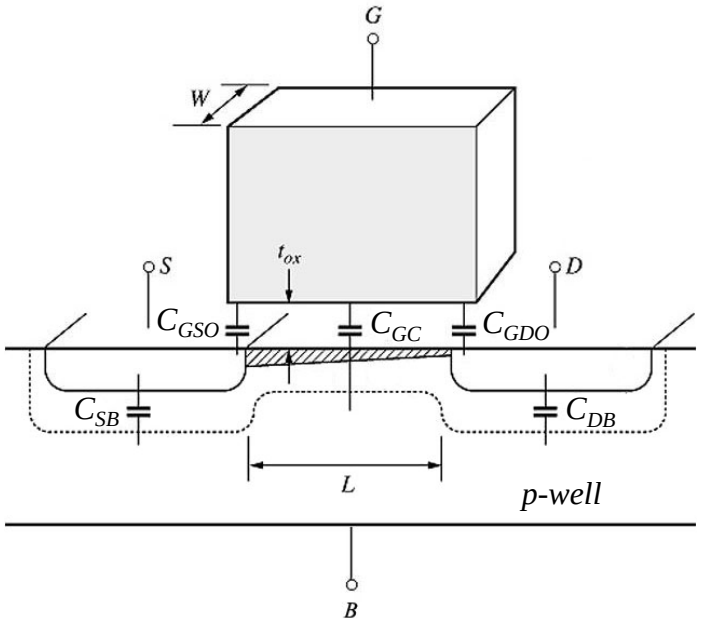
MJ, MJSW = grading coefficient

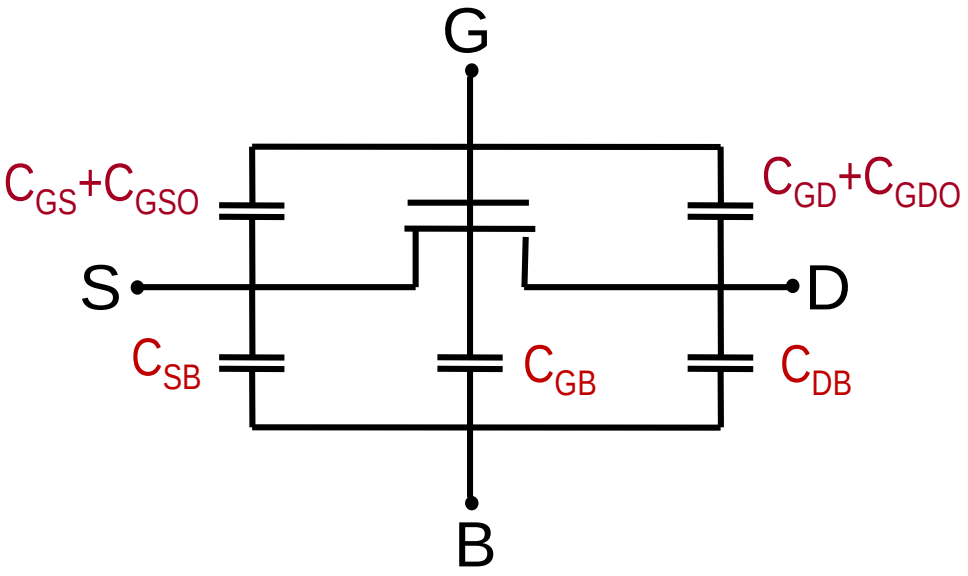
MOSFET Capacitance Model





Simple Hand Calculation





Typically, for simple hand calculation in digital circuits, we approximate regardless of transistor operating mode:

- $C_{GATE} = C_{GD}+C_{GS}+C_{GB}+C_{GDO}+C_{GSO} \simeq C_{OX} \cdot W \cdot L$
- $C_{SB} = C_{DB} \simeq C_{JAO} \times W \cdot L_S + C_{JSWO} \times (W+2L_S)$

Hand Calculation Example

	C_{ox} (fF/μm²)	C_{jao} (fF/μm²)	m_j	ϕ_b (V)	C_{jswo} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	10	2	0.5	0.9	0.28	0.44	0.9
PMOS	10	1.9	0.48	0.9	0.22	0.32	0.9

Example: an NMOS with L = 0.25 μm, W = 0.5 μm, L_S = 0.65 μm

- $C_{GATE} \simeq C_{OX} \cdot W \cdot L = 1.25$ fF
- $C_{SB} = C_{DB} \simeq C_{JAO} \times W \cdot L_S + C_{JSWO} \times (W+2L_S) = 1.154$ fF