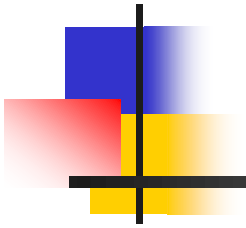

Electronic Circuits Design

Lecture – 12

- *Decoder*
- *Multiplexer*
- *Flip-Flop*

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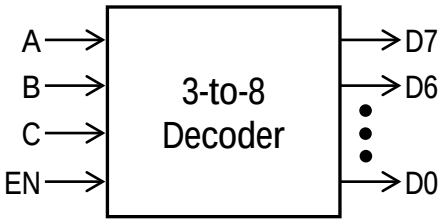
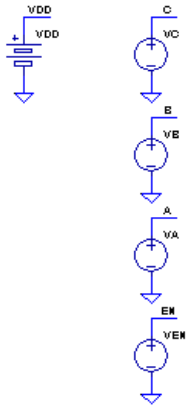
MSB (A, B, C) LSB

EN	A	B	C	D0	D1	D2	• • •	D7
0	X	X	X	0	0	0		0
1	0	0	0	1	0	0		0
1	0	0	1	0	1	0		0
1	0	1	0	0	0	1		0
1	1	1	1	0	0	0		1



3-to-8 Decoder



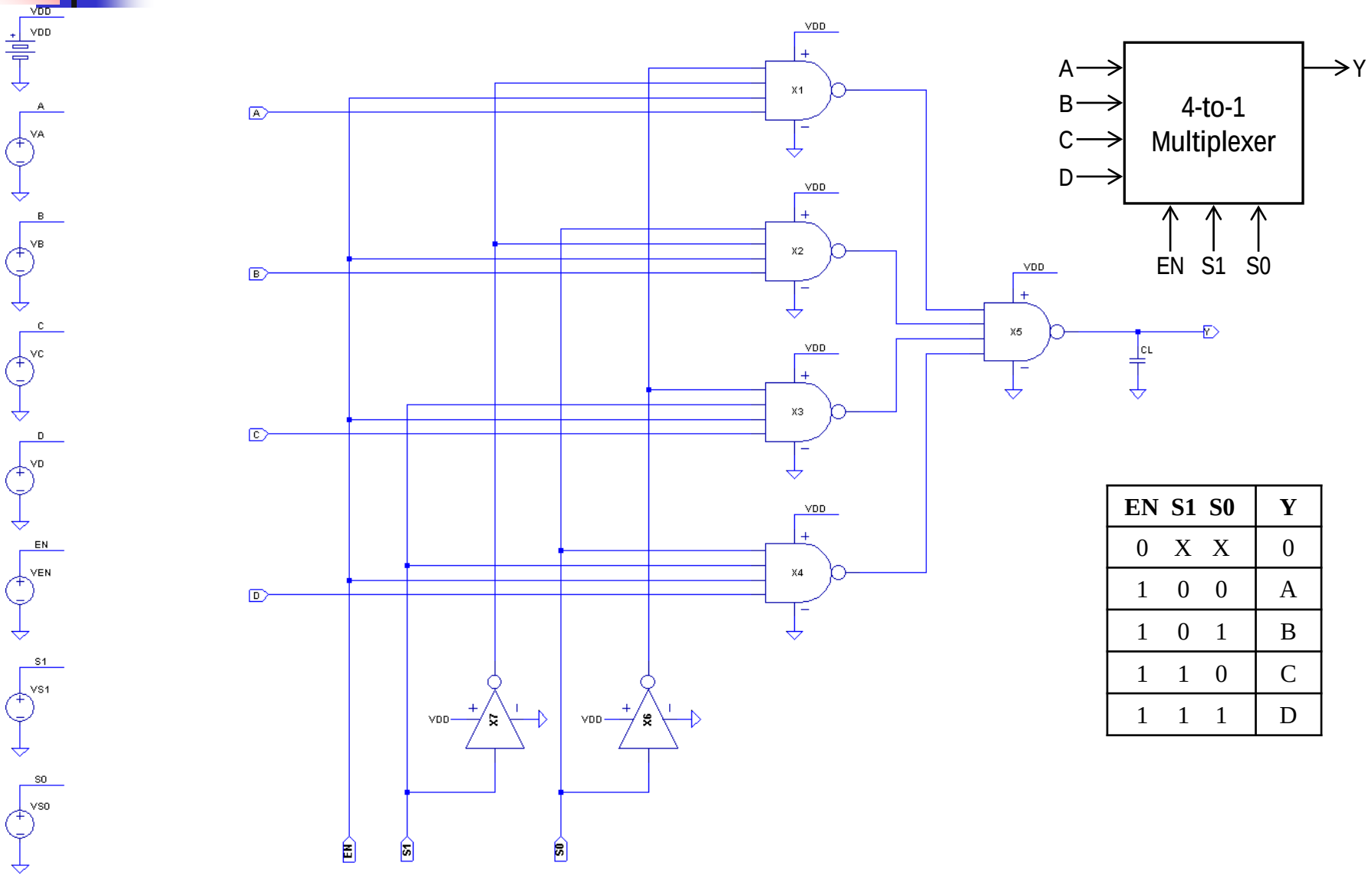
Lab-1: 3-to-8 Decoder

❖ **Simulation Condition**

- **CMOS model parameter: MOSIS/TSMC_0.18µm ($L_P = L_N = 0.18\mu m$)**
- **VDD = 1.8 V, CL0 = CL1 = CL2 = · · · = CL7 = 200fF**
- **VC = PULSE(0 1.8V 4.5ns 0.5ns 0.5ns 4.5ns 10ns)**
- **VB = PULSE(0 1.8V 9.5ns 0.5ns 0.5ns 9.5ns 20ns)**
- **VA = PULSE(0 1.8V 19.5ns 0.5ns 0.5ns 19.5ns 40ns)**
- **VEN = PULSE(0 1.8V 39.5ns 0.5ns 0.5ns 39.5ns 80ns)**
- **Transient analysis from 0 to 200 ns**

1) **Create the LTSpice schematic of the 3-to-8 decoder.**
2) **Assuming $\mu_N = 2.5\mu_P$, determine transistor sizes of each gate to provide t_{pLH} and t_{pHL} less than 300 ps.**
3) **Obtain a plot of A, B, C, EN, D0, D1, D2, D3, D4, D5, D6 and D7 versus time.**
4) **Measure the average active power consumed by the decoder.**
5) **Change the supply voltage to 0.9 V, then obtain the average active power consumed by the decoder. What percent is it reduced compared to VDD = 1.8 V ?**

4-to-1 Multiplexer



EN	S1	S0	Y
0	X	X	0
1	0	0	A
1	0	1	B
1	1	0	C
1	1	1	D

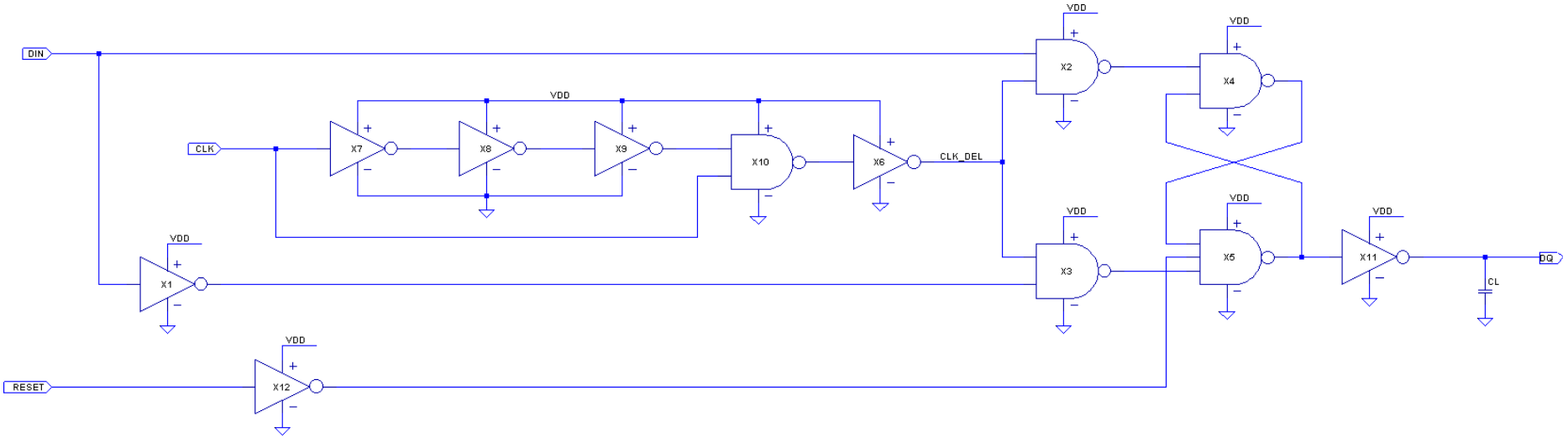
Lab-2: 4-to-1 Multiplexer

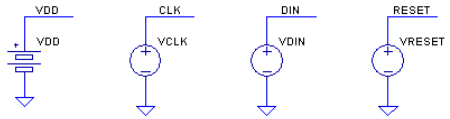
❖ **Simulation Condition**

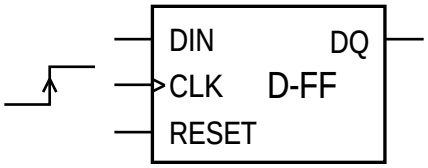
- **CMOS model parameter: MOSIS/TSMC_0.18µm ($L_P = L_N = 0.18\mu m$)**
- **VDD = 1.2 V, CL = 50fF**
- **VA = PULSE(0 1.2V 2ns 0.5ns 0.5ns 2ns 5ns)**
- **VB = PULSE(0 1.2V 4.5ns 0.5ns 0.5ns 4.5ns 10ns)**
- **VC = PULSE(0 1.2V 9.5ns 0.5ns 0.5ns 9.5ns 20ns)**
- **VD = PULSE(0 1.2V 19.5ns 0.5ns 0.5ns 19.5ns 40ns)**
- **VEN = PWL(0 0V 161.25ns 0V 161.75ns 1.2V 481.75ns 1.2V 482.25ns 0V)**
- **VS1 = PULSE(0 1.2V 79.5ns 0.5ns 0.5ns 79.5ns 160ns)**
- **VS0 = PULSE(0 1.2V 39.5ns 0.5ns 0.5ns 39.5ns 80ns)**
- **Transient analysis from 0 to 640 ns**

1) **Create the LTSpice schematic of the 4-to-1 multiplexer.**
2) **Assuming $\mu_N = 2.5\mu_P$, determine transistor sizes of each gate to provide t_{pLH} and t_{pHL} less than 300 ps.**
3) **Obtain a plot of A, B, C, D, EN, S1, S0 and Y versus time.**
4) **Verify the logic functionality.**

Positive-Edge Triggered D Flip-Flop

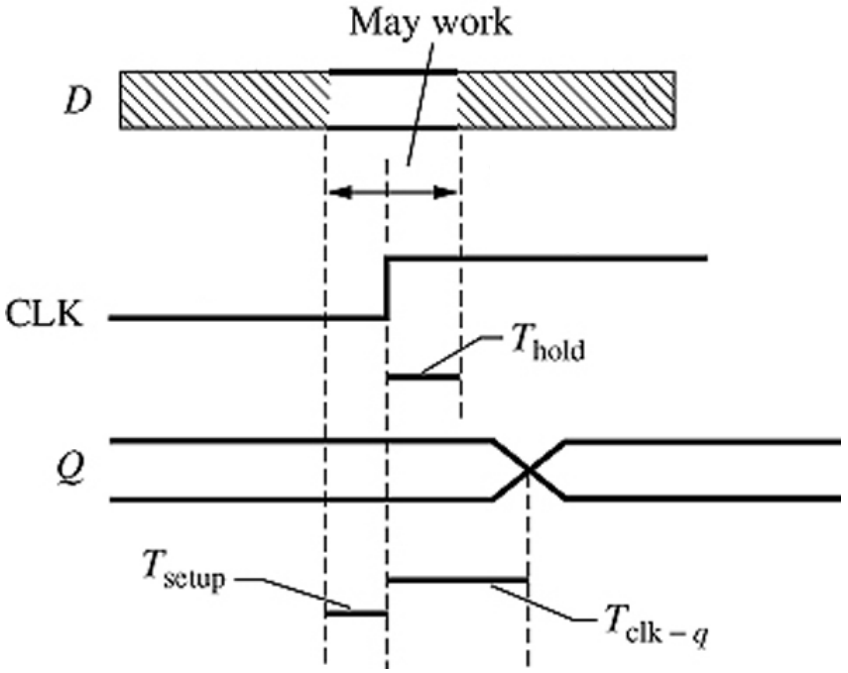






RESET	DIN	CLK	DQ
H	X	X	L
L	L	↑	L
L	H	↑	H

Flip-Flop Timing Parameters



- T_{setup}: the length of time that the incoming data must be stable before the clock arrives for proper operation
- T_{hold}: the length of time that the data must remain stable after the clock arrives for proper operation
- T_{CLK-Q}: the delay time from CLK to Q transition

Lab-3: Positive-Edge Triggered D Flip-Flop

- **Simulation Condition**
  - **CMOS model parameter: MOSIS/TSMC_0.18µm**
  - **VDD = 1.8 V, CL = 100fF**
  - **Inverter chain (X7, X8, X9): W_P/L_P = 3.8µm/0.5µm, W_N/L_N = 1µm/0.5µm**
  - **Inverter (X1, X6, X11, X12): W_P/L_P = 1.5µm/0.18µm, W_N/L_N = 0.6µm/0.18µm**
  - **2-input NAND (X2, X3, X4, X10): W_P/L_P = 1.5µm/0.18µm, W_N/L_N = 1.2µm/0.18µm**
  - **3-input NAND (X5): W_P/L_P = 1.5µm/0.18µm, W_N/L_N = 1.8µm/0.18µm**
  - **VCLK = PULSE(0 1.8V 6.5ns 0.5ns 0.5ns 4.5ns 10ns)**
  - **VDIN = PULSE(0 1.8V 4.5ns 0.5ns 0.5ns 8.5ns 20ns)**
  - **VRESET = PULSE(1.8V 0 2.5ns 0.5ns 0.5ns 47.5ns 100ns)**
  - **Transient analysis from 0 to 80 ns**

1) **Create the LTSpice schematic of the positive-edge triggered D flip-flop.**
2) **Obtain a plot of RESET, DIN, CLK, CLK_DEL and DQ versus time.**
3) **Verify the logic functionality.**
4) **Measure T_{CLK-Q}.**
5) **Make comments if you need.**