Electronic Circuits Design

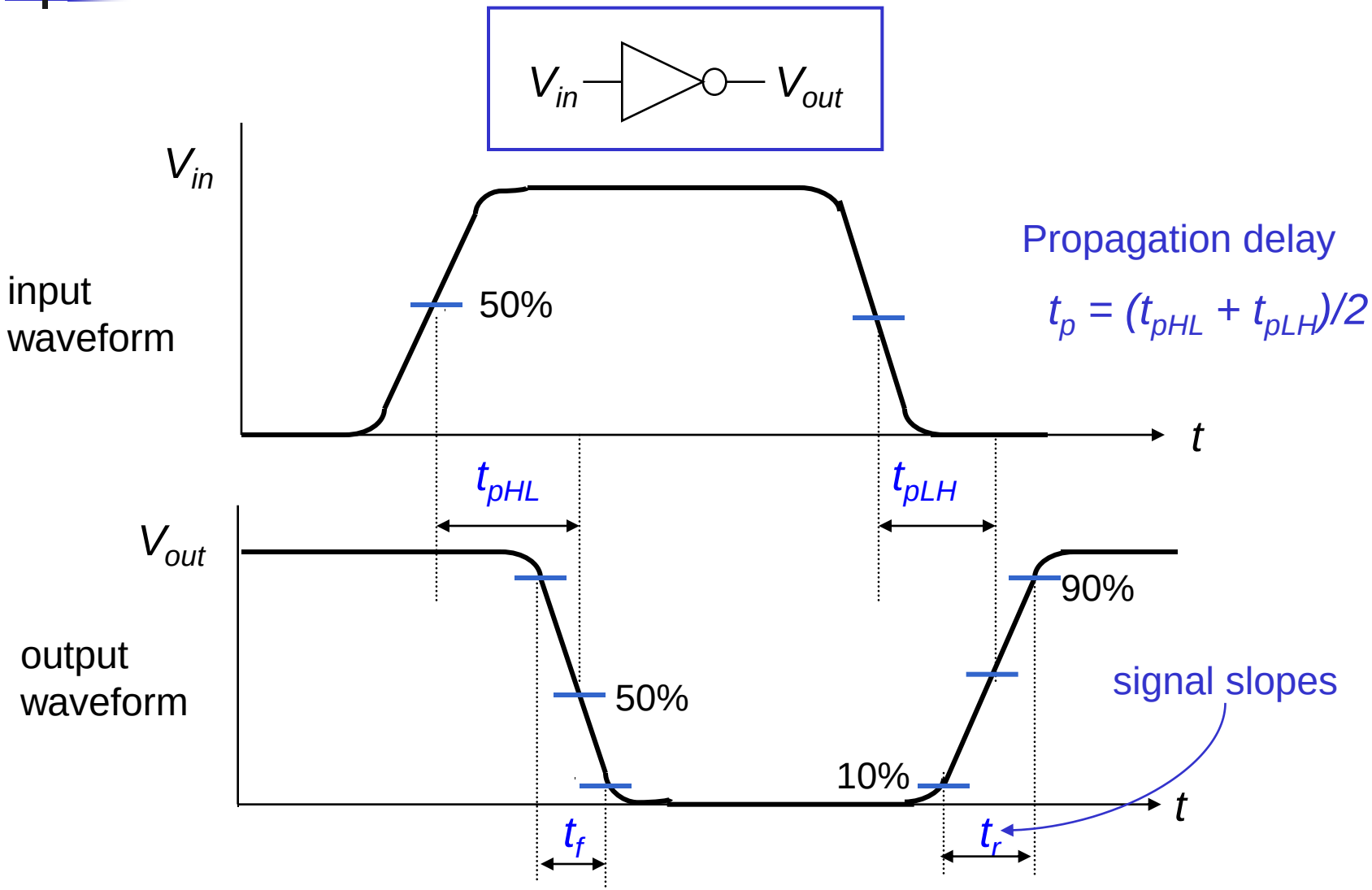
Lecture – 9

- ***Digital Circuit Characterization***
  - ***Delay Estimation***
  - ***Power Dissipation***

Yeonbae Chung
School of Electronics Engineering
Kyungpook National University

Delay Estimation

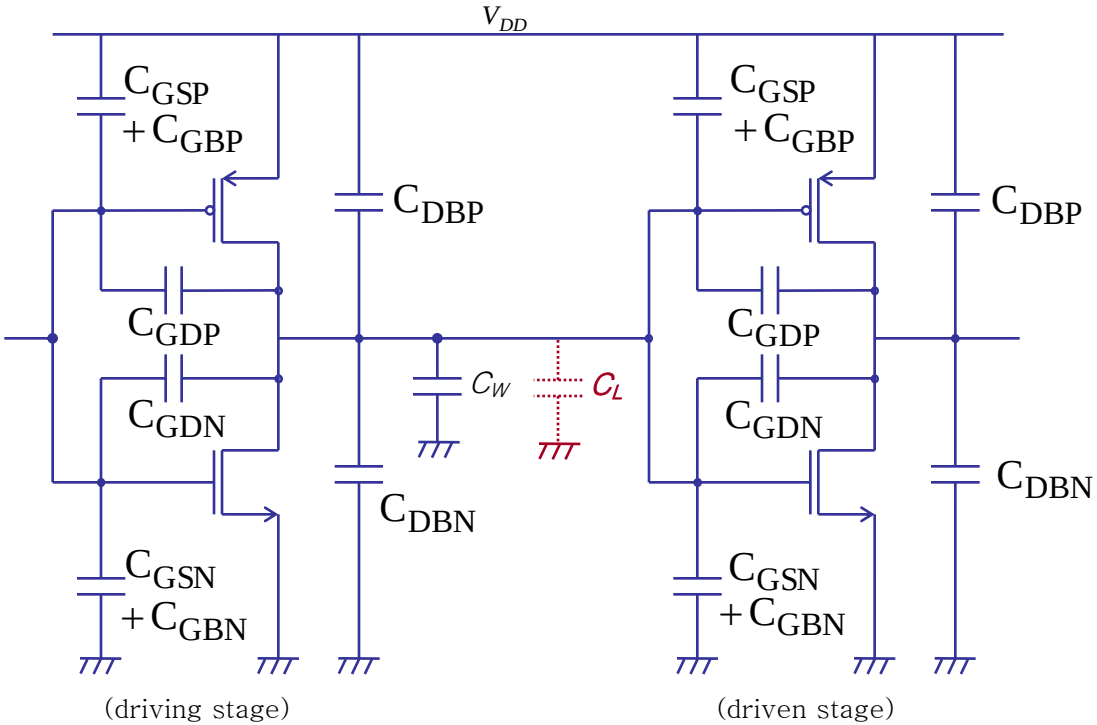
Delay Definitions



Delay Definitions (continued)

- **t_{pLH}**: rising propagation delay
  - From input to rising output crossing $V_{DD}/2$
- **t_{pHL}**: falling propagation delay
  - From input to falling output crossing $V_{DD}/2$
- **t_p**: average propagation delay
  - $t_p = (t_{pHL} + t_{pLH})/2$
- **t_r**: rise time
  - From output crossing 0.1 V_{DD} to 0.9 V_{DD}
- **t_f**: fall time
  - From output crossing 0.9 V_{DD} to 0.1 V_{DD}

Load Capacitances



CMOS inverter string (fanout = 1)

- $C_L = C_{L,driving} + C_{L,driven} + C_W$

Simple Calculation of Load Capacitances

- $C_{L,driving} \approx C_{DBP} + C_{DBN}$

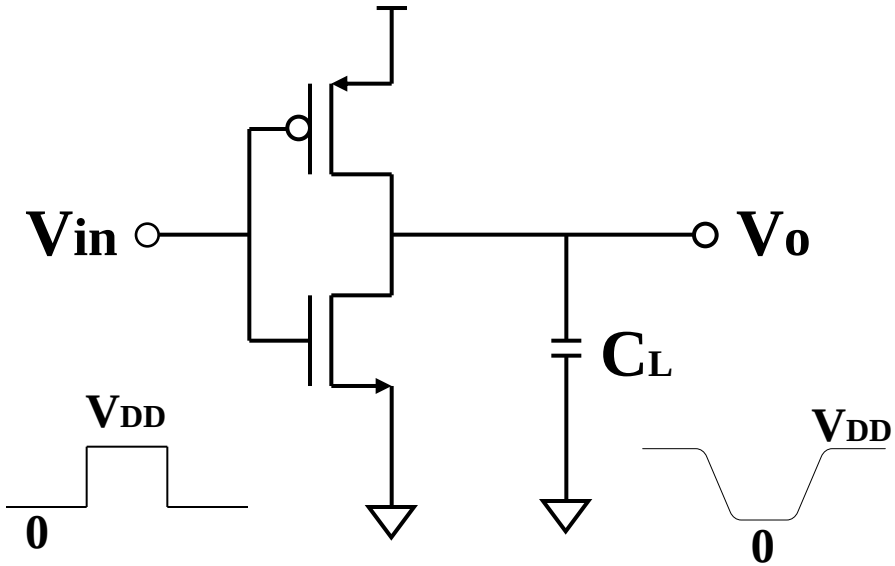
  $\approx C_{DJP}(V=0) + C_{DJN}(V=0)$

- $C_{L,driven} \approx C_{GP} + C_{GN}$

  $\approx C_{OX}W_PL_P + C_{OX}W_NL_N$

- $C_W \leftarrow$ typically negligible except long signal wire

Delay of CMOS Inverter



Suppose that

- Apply step voltage of input
- Think capacitive load (C_L) only
- $\beta_N = \mu_n C_{ox}\left(\frac{W_n}{L_n}\right)$
- $\beta_P = \mu_p C_{ox}\left(\frac{W_p}{L_p}\right)$

High-to-Low Transition

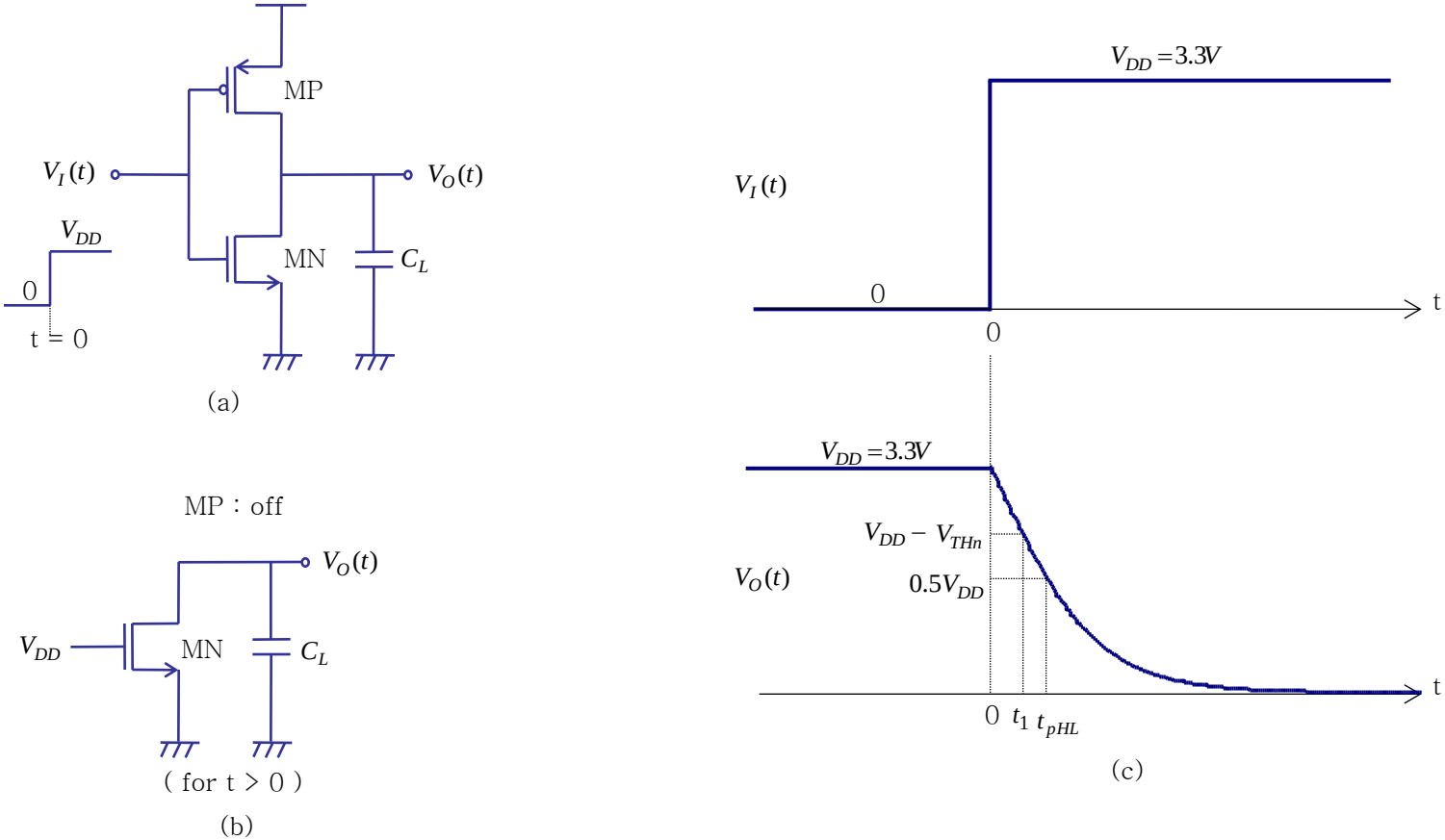


그림 2.2.1 CMOS inverter의 high-to-low 과도특성

(a) CMOS inverter 회로 (b) t > 0일 때 $V_I(t) = V_{DD}$인 회로 (c) $V_I(t)$ 와 $V_O(t)$ 의 파형

High-to-Low Transition (continued)

- when $0 < t \leq t_1$: MN in saturation

- when $t_1 < t$: MN in linear

Low-to-High Transition

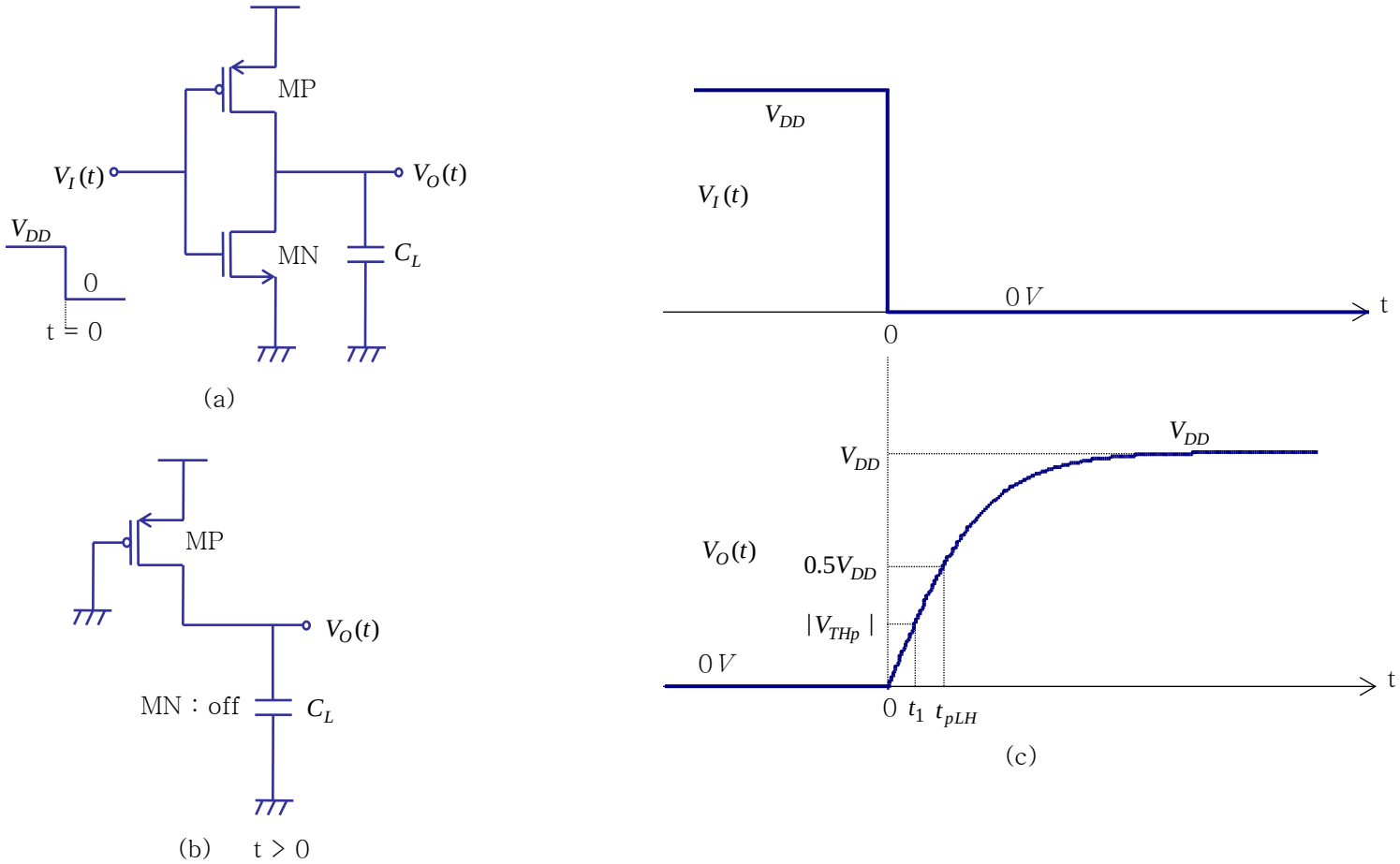


그림 2.2.2 CMOS inverter의 low-to-high 과도특성

(a) CMOS inverter 회로 (b) t > 0일 때 $V_I(t) = 0$ 인 (c) $V_I(t)$와 $V_O(t)$의 파형

Low-to-High Transition (continued)

- when $0 < t \leq t_1$: MP in saturation

- when $t_1 < t$: MP in linear

Propagation Delay, Rising / Falling Time

$$t_{pHL} = \frac{1.6C_L}{\beta_N \cdot V_{DD}} \qquad t_{pLH} = \frac{1.6C_L}{\beta_P \cdot V_{DD}}$$

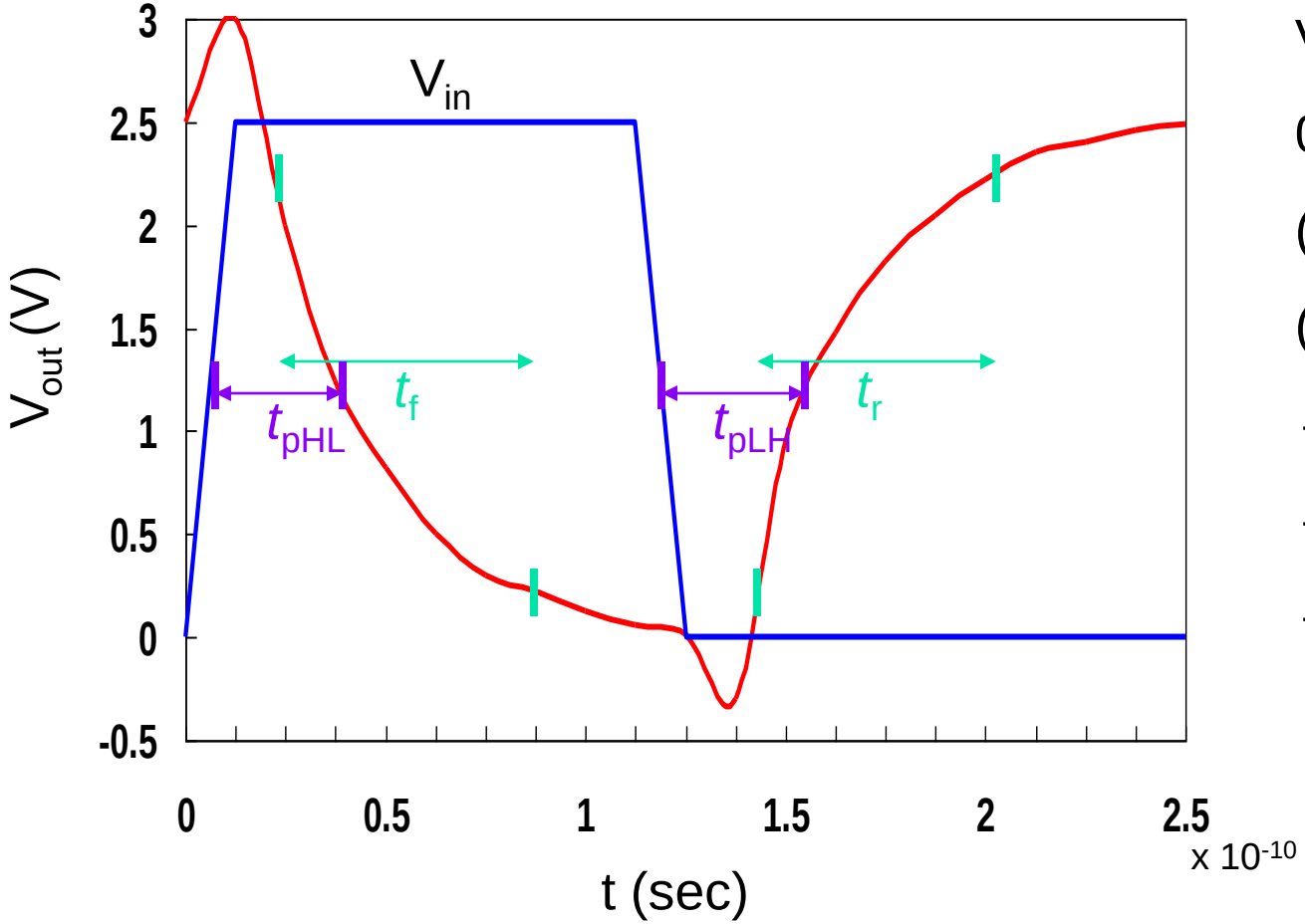
- $t_p = (t_{pHL} + t_{pLH})/2$

  $= 0.8(1/\beta_N + 1/\beta_P)C_L/V_{DD}$

- From similar analysis with the above, and assuming $V_{THN} = -V_{THP} = 0.2V_{DD}$

  - $t_r \approx 3.7C_L/(\beta_P V_{DD})$
  - $t_f \approx 3.7C_L/(\beta_N V_{DD})$

Inverter Transient Response



V_{DD} = 2.5V

0.25μm

$(W/L)_n$ = 1.5

$(W/L)_p$ = 3.5

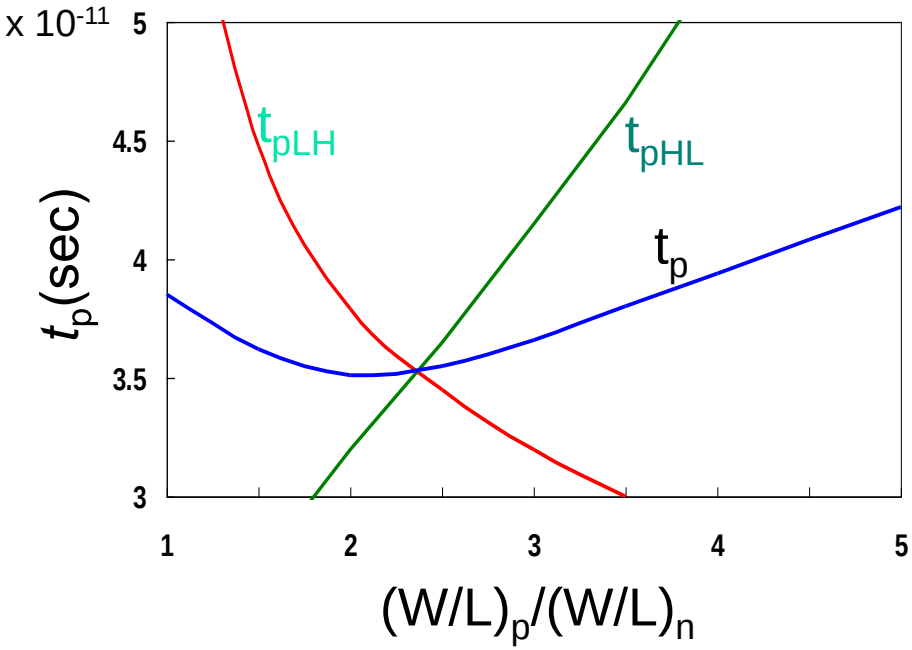
t_{pHL} = 36 psec

t_{pLH} = 29 psec

t_p = 32.5 psec

PMOS / NMOS Ratio

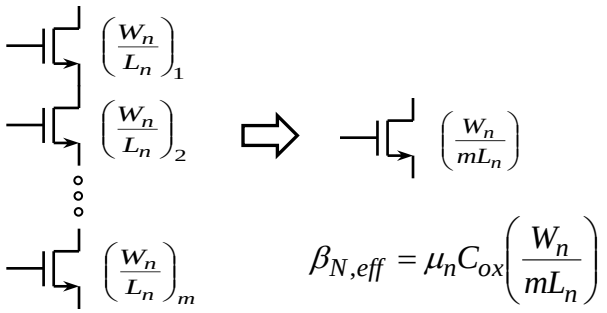
- Need the PMOS and NMOS to be sized so that the β ratio matches (ratio of 2 to 3)
  - symmetrical VTC
  - equal high-to-low and low-to-high propagation delays



$(W/L)_p/(W/L)_n$ of 2.4 gives symmetrical response when $\mu_N = 2.4\mu_P$

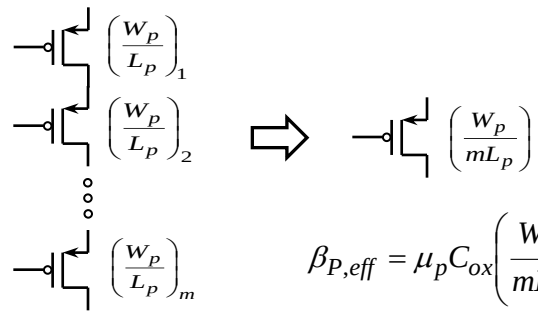
Effective β in Series Connection

- When m NMOS's or PMOS's of same W/L are in series and simultaneously turned-on



$$\beta_{N,eff} = \mu_n C_{ox}\left(\frac{W_n}{mL_n}\right)$$

$$\beta_{N,1} = \beta_{N,2} = \beta_{N,m} = \mu_n C_{ox}\left(\frac{W_n}{L_n}\right)$$

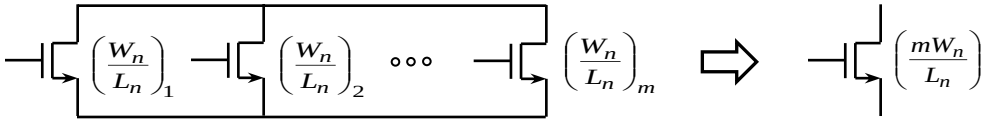


$$\beta_{P,eff} = \mu_p C_{ox}\left(\frac{W_p}{mL_p}\right)$$

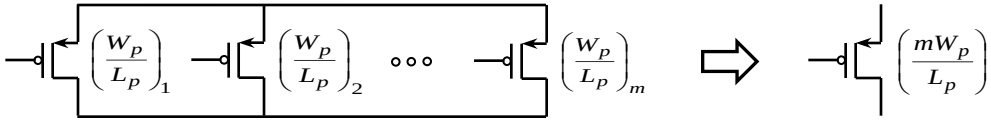
$$\beta_{P,1} = \beta_{P,2} = \beta_{P,m} = \mu_p C_{ox}\left(\frac{W_p}{L_p}\right)$$

Effective β in Parallel Connection

- When m NMOS's or PMOS's of same W/L are in parallel and simultaneously turned-on

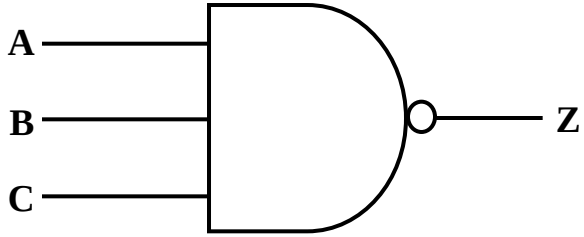


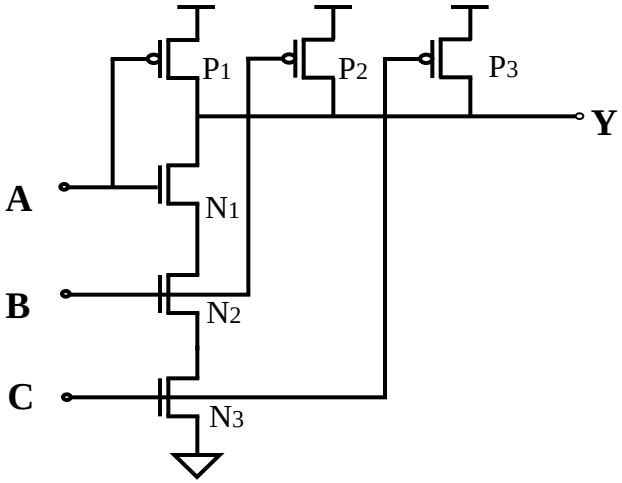
$$\beta_{N,1} = \beta_{N,2} = \beta_{N,m} = \mu_n C_{ox}\left(\frac{W_n}{L_n}\right) \qquad \beta_{N,eff} = \mu_n C_{ox}\left(\frac{mW_n}{L_n}\right)$$



$$\beta_{P,1} = \beta_{P,2} = \beta_{P,m} = \mu_p C_{ox}\left(\frac{W_p}{L_p}\right) \qquad \beta_{P,eff} = \mu_p C_{ox}\left(\frac{mW_p}{L_p}\right)$$

Delay of NAND Gate





$\beta_{Peff} = \beta_P$ if only one P-MOS turns on to raise the output.

$$\beta_{Neff} = \frac{1}{\frac{1}{\beta_{N1}} + \frac{1}{\beta_{N2}} + \frac{1}{\beta_{N3}}}$$ ← summation of series conductance

If $\beta_{N1} = \beta_{N2} = \beta_{N3} = \beta_N$

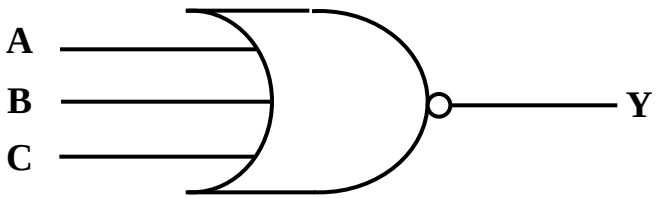
$$\beta_{Neff} = \frac{1}{3}\beta_N$$

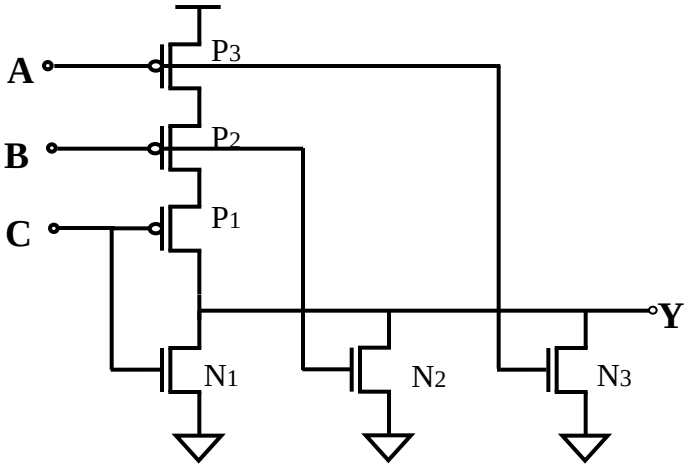
Therefore,

$$t_r = \frac{3.7C_L}{\beta_P \cdot V_{DD}}$$

$$t_f = \frac{3.7C_L}{\beta_{Neff} \cdot V_{DD}} = 3 \times \frac{3.7C_L}{\beta_N \cdot V_{DD}}$$

Delay of NOR Gate





$$\beta_{Peff} = \frac{1}{\frac{1}{\beta_{P1}} + \frac{1}{\beta_{P2}} + \frac{1}{\beta_{P3}}}$$

$\beta_{Neff} = \beta_N$ If only one n-MOS turns on to pull-down the output.

If $\beta_{P1} = \beta_{P2} = \beta_{P3} = \beta_P$

$$\beta_{Peff} = \frac{1}{3}\beta_P$$

Therefore,

$$t_r = \frac{3.7C_L}{\beta_{Peff} \cdot V_{DD}} = 3 \times \frac{3.7C_L}{\beta_P \cdot V_{DD}}$$

$$t_f = \frac{3.7C_L}{\beta_N \cdot V_{DD}}$$

Delay of General CMOS Gate

- When m n-MOS's with same W/L are in series and simultaneously turned-on

$$L_{N,eff} = mL_N \Rightarrow \beta_{N,eff} = \frac{1}{m}\beta_N \Rightarrow t_{f,eff} = mt_f$$

- When m n-MOS's with same W/L are in parallel and simultaneously turned-on

$$W_{N,eff} = mW_N \Rightarrow \beta_{N,eff} = m\beta_N \Rightarrow t_{f,eff} = \frac{1}{m}t_f$$

- When k p-MOS's with same W/L are in series and simultaneously turned-on

$$L_{P,eff} = kL_P \Rightarrow \beta_{P,eff} = \frac{1}{k}\beta_P \Rightarrow t_{r,eff} = kt_r$$

- When k p-MOS's with same W/L are in parallel and simultaneously turned-on

$$W_{P,eff} = kW_P \Rightarrow \beta_{P,eff} = k\beta_P \Rightarrow t_{r,eff} = \frac{1}{k}t_r$$

Design for Speed

$$t_r = \frac{3.7C_L}{\beta_P \cdot V_{DD}} \qquad t_f = \frac{3.7C_L}{\beta_N \cdot V_{DD}} \qquad t_{pLH} = \frac{1.6C_L}{\beta_P \cdot V_{DD}} \qquad t_{pHL} = \frac{1.6C_L}{\beta_N \cdot V_{DD}}$$

- **Reduce C_L**
  - **reduce fanout**
- **Increase W/L ratio of the transistor**
  - **the most powerful and effective performance optimization tool in the hands of the designer**
- **Increase V_{DD}**
  - **can trade-off power dissipation for performance**
  - **increasing V_{DD} above a certain level yields only very minimal improvements**
  - **reliability concerns enforce a firm upper bound on V_{DD}**

Power Dissipation

- *Active Power Dissipation*
- *Standby Power Dissipation*

Power and Energy

- **Power is drawn from a voltage source attached to the V_{DD} pin of a chip.**

- **Instantaneous Power:** $$P(t) = i_{DD}(t)V_{DD}$$

- **Energy:** $$E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$$

- **Average Power:** $$P_{\text{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$$

Power Dissipation in CMOS Gate

- **Dynamic Power Dissipation**

  ==> Charging and discharging parasitic load capacitors

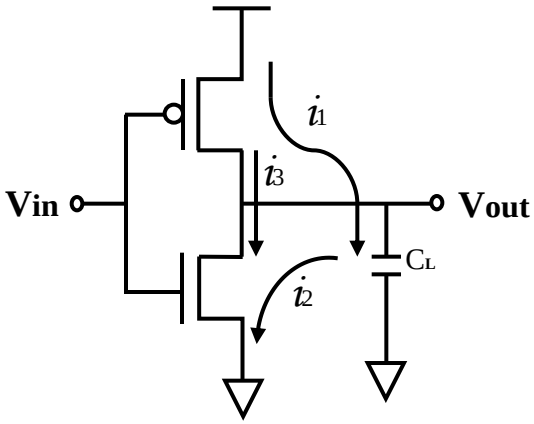
- **Short Circuit Power Dissipation**

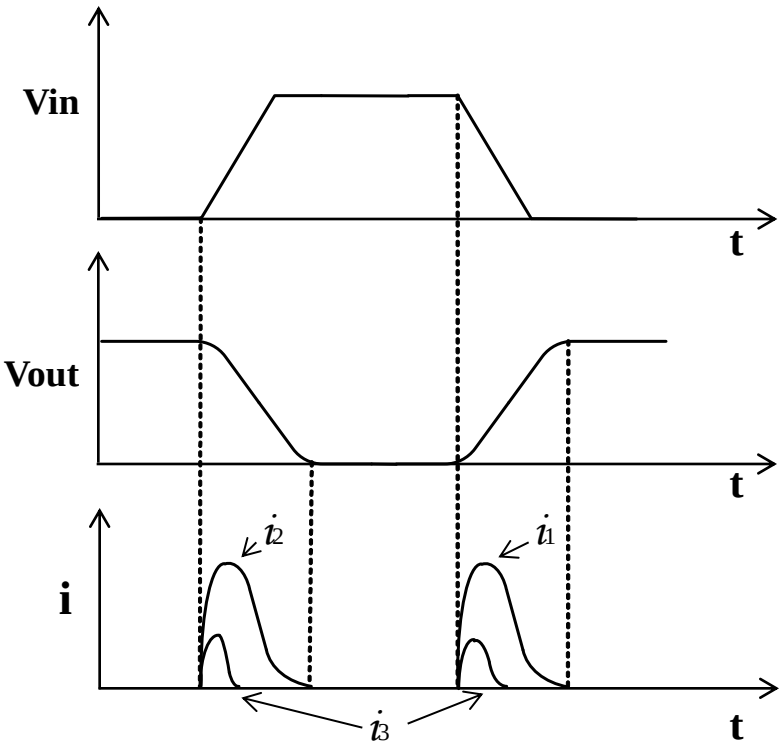
  ==> Short circuit path between supply rails during switching

- **Standby Power Dissipation**

  ==> Leaking p-n junction, gate oxide leakage,
  and transistor subthreshold current

Active Power Dissipation



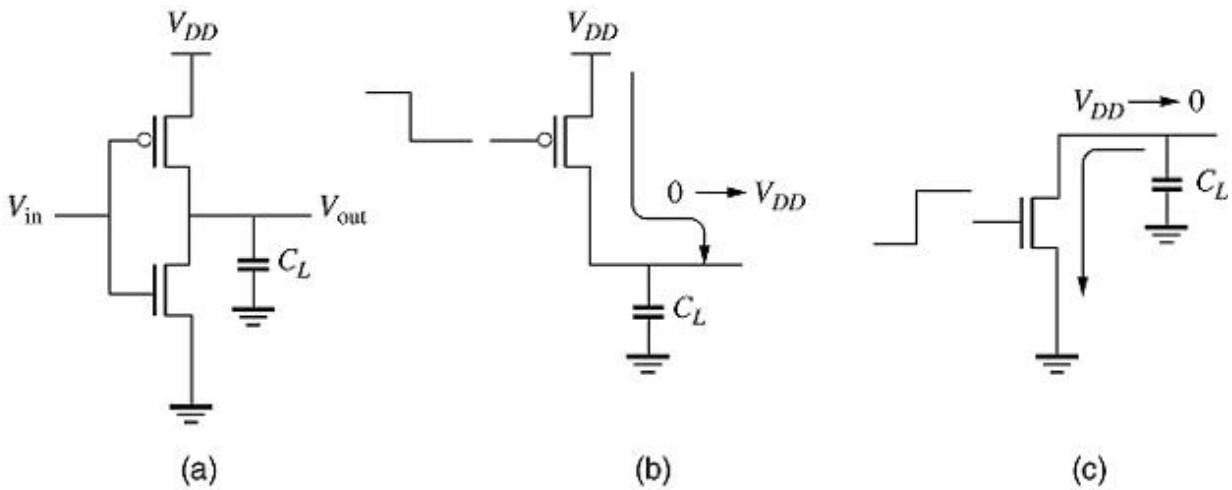


- i_1 & i_2 ; charge and discharge current of C_L → i_L
- i_3 ; short circuit current during switching → i_{sc}

Typically, $i_L >> i_{sc}$

- Slow rising and falling will increase i_{sc}

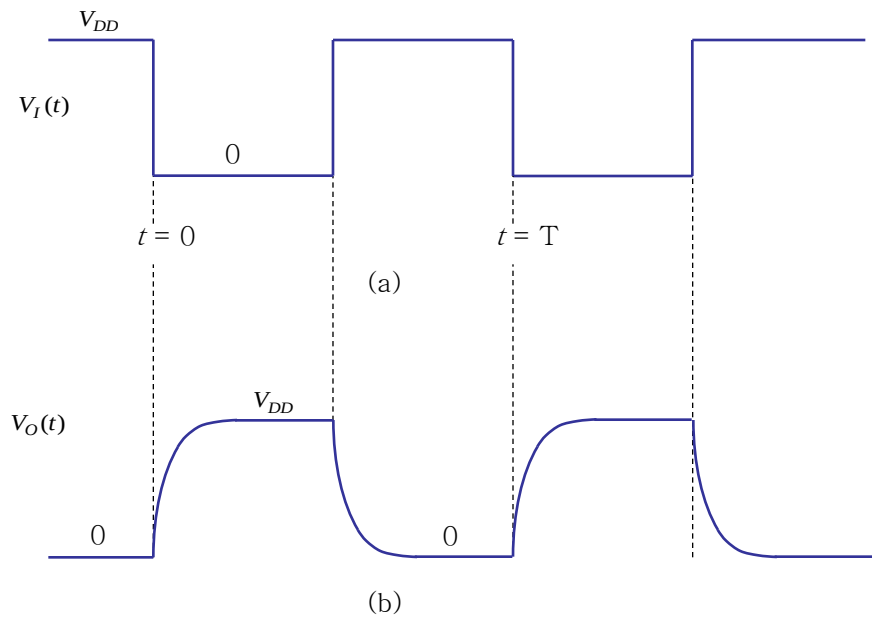
Dynamic Power



Total charge supplied by V_{DD} and drained to GND during T : $Q = C_L \times V_{DD}$

Average current : $I_{avg} = Q/T = C_L \times V_{DD} \times f$

Average Dynamic Power Dissipation



When $V_I(t)$ is a clock waveform with period T

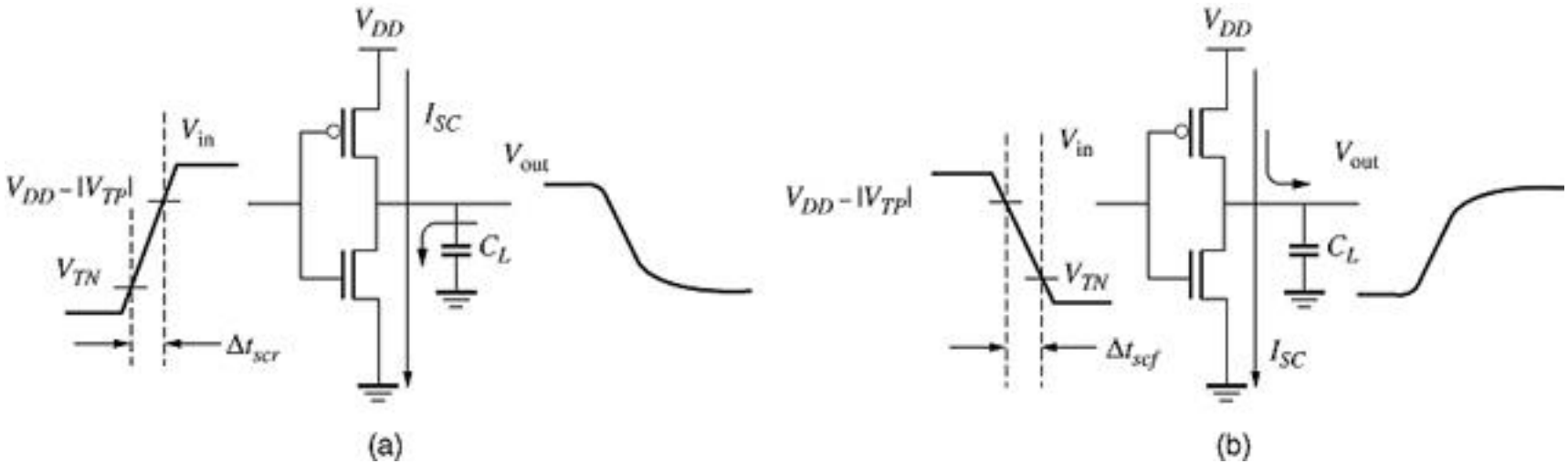
$$\Longrightarrow \quad P_D = \frac{C_L V_{DD}^2}{T} = f\, C_L V_{DD}^2$$

NOTE ;

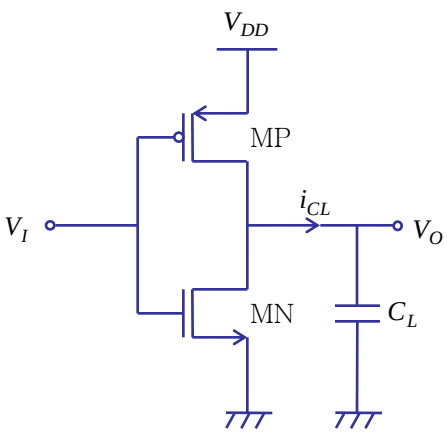
- $P_D \propto C_L, f, V_{DD}^2$
- P_D is not dependent on actual rise and fall time.

Short Circuit Power

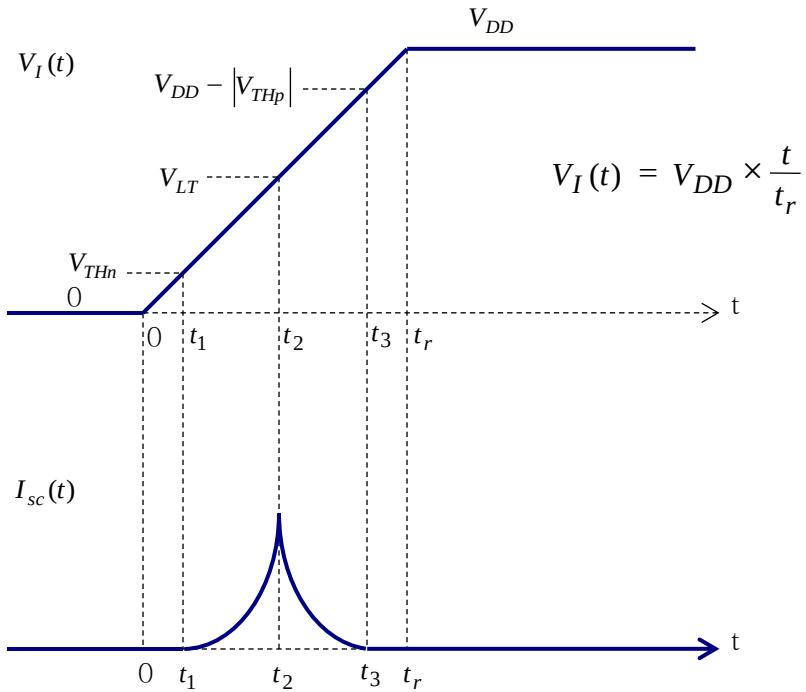
- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a "short circuit" current from V_{DD} to GND
- Typically, less than 10% of dynamic power if rise/fall times are comparable for input and output



Short Circuit Current



(a)



(b)

Short Circuit Power Dissipation

Assuming $\beta_N = \beta_P$, $V_{THn} = -V_{THp}$, $I_{SC} >> I_{CL}$ ==>

$$I_{sc}(t) = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot (V_I(t) - V_{THn})^2$$ <== MN in saturation for ($t_1 < t < t_2$)

$$I_{sc}(t) = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \cdot (V_{DD} - |V_{THp}| - V_I(t))^2$$ <== MP in saturation for ($t_2 < t < t_3$)

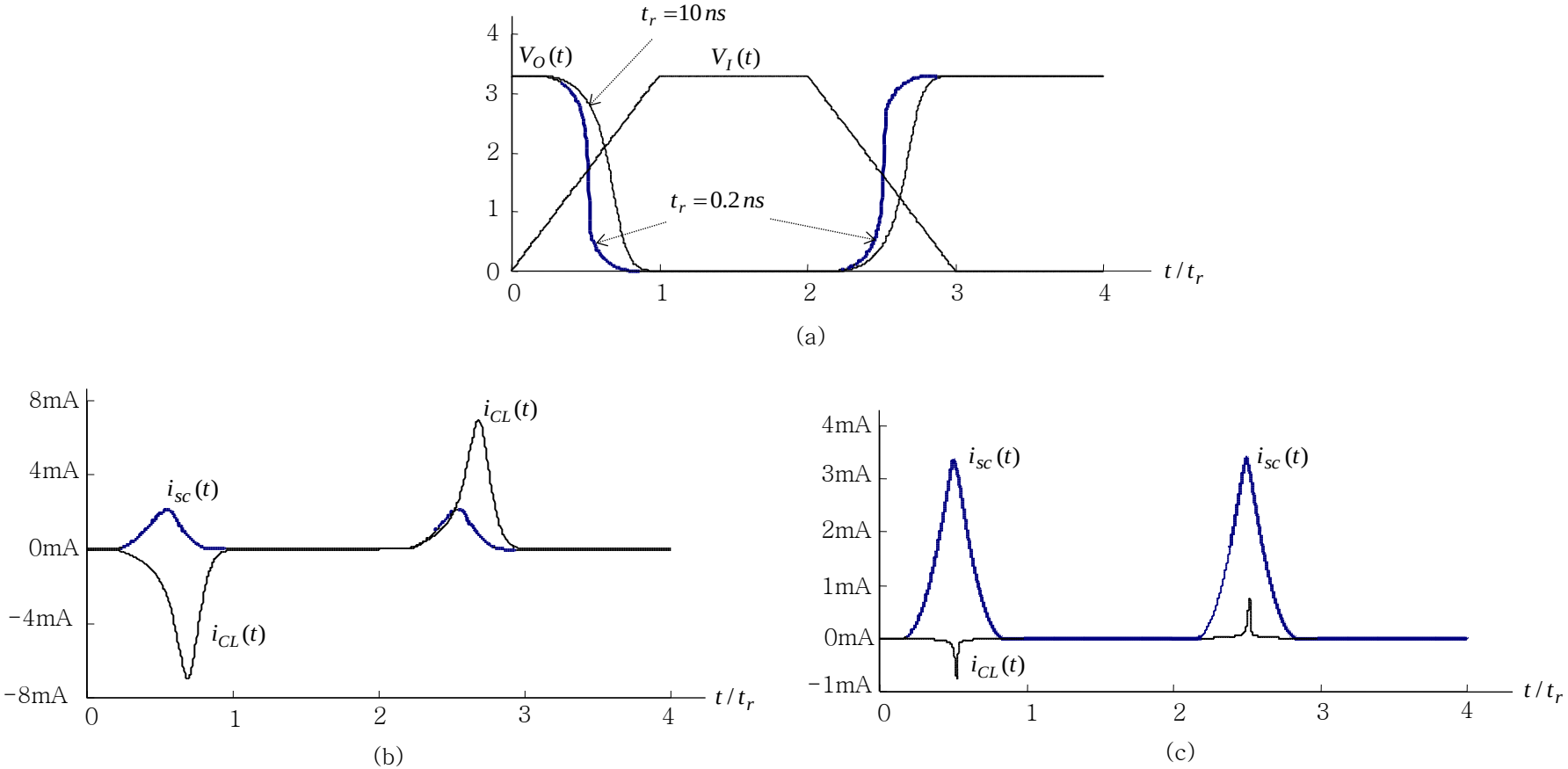
$$E_{rise} = V_{DD} \cdot \int_0^{t_r} I_{sc}(t)\,dt = V_{DD} \cdot 2 \times \int_{t_1}^{t_2} \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot (V_I(t) - V_{THn})^2\,dt$$

$$= V_{DD} \cdot \mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot \frac{t_r}{V_{DD}} \cdot \int_{V_{THn}}^{\frac{1}{2}V_{DD}} (V_I(t) - V_{THn})^2\,dV_I = \frac{1}{3} \cdot \mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot \left(\frac{V_{DD}}{2} - V_{THn}\right)^3 \cdot t_r$$

$$E_{sc} = E_{rise} + E_{fall} = \frac{2}{3} \cdot \mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot \left(\frac{V_{DD}}{2} - V_{THn}\right)^3 \cdot t_r$$ <== assuming $t_r = t_f$

$$P_{sc} = \frac{E_{sc}}{T} = \frac{2}{3} \cdot \mu_n C_{ox}\left(\frac{W}{L}\right)_n \cdot \left(\frac{V_{DD}}{2} - V_{THn}\right)^3 \cdot t_r \cdot f$$

Simulation Example



CMOS inverter transient according to rise time

(a) $V_I(t)$ & $V_O(t)$ (b) when $t_r = t_f = 0.2ns$ (c) when $t_r = t_f = 10\,ns$

Reducing Short Circuit Power

- **To reduce short-circuit power, the rise and fall times of the input signal should be as small as possible.**

- **One good optimum solution is to make the input and output signal edge rates sharp and about equal.**

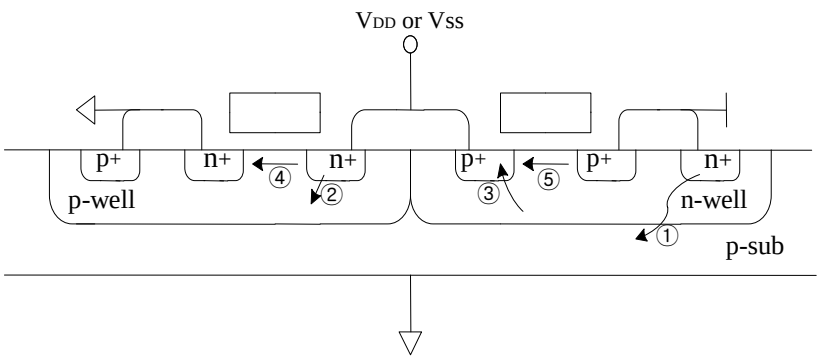
Standby Power Dissipation

- Considering the complementary CMOS logic, either p-MOS or n-MOS is always off during steady-state.

  ⇒ No DC current path from V_{DD} to Vss

  ⇒ $I_{static} \cong 0$ ⇒ $P_s = V_{DD} \times I_{static} \cong 0$

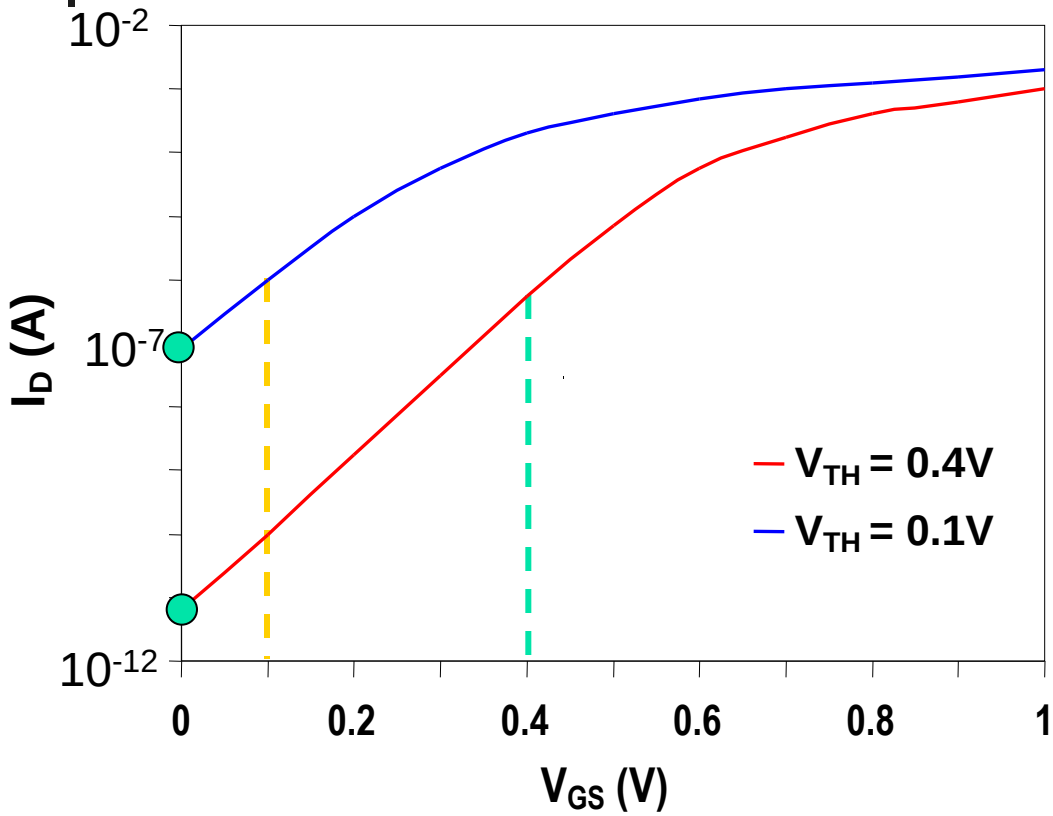
- But there is a small static power dissipation due to reverse-biased junction leakage and transistor subthreshold current.



- Reverse-biased junction leakage : ①, ②, ③
- Subthreshold leakage : ④, ⑤

$$P_{static} = I_{leak} \times V_{DD} = \left(I_{subthreshold} + I_{juncton}\right) \times V_{DD} \text{ for CMOS}$$

Subthreshold Leakage

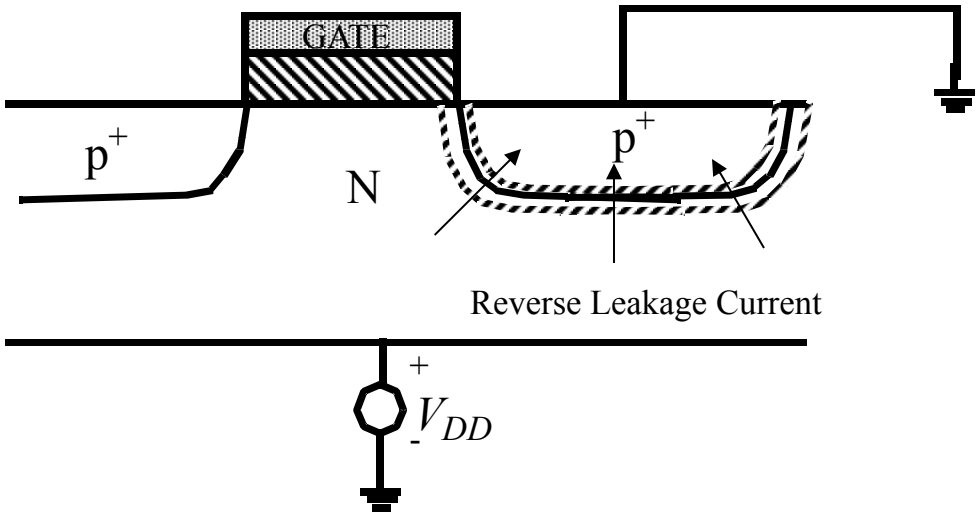


- Continued scaling of supply voltage and the subsequent scaling of threshold voltage will make subthreshold conduction a dominate component of DC power dissipation.

- For $V_{DS} >> kT/q$ and $V_{GS} = 0$,

$$I_{D,OFF} = \mu_n C_{ox} \frac{W}{L} \cdot \frac{\gamma \cdot V_T^{\,2}}{2\sqrt{2\phi_F + V_{SB}}} \cdot \exp\left(\frac{-V_{TH}}{nV_T}\right)$$

Junction Leakage



- NMOS junction leakage in SPICE

$$I_{DB.leak} = (JS \cdot AD + JSW \cdot PD) \cdot (1 - e^{\frac{V_{BD}}{V_T}})$$

$$I_{SB.leak} = (JS \cdot AS + JSW \cdot PS) \cdot (1 - e^{\frac{V_{BS}}{V_T}})$$

Standby Power Dissipation

- Critical in low-power battery-operated portable devices
- Sources of static power dissipation
  - Subthreshold leakage
  - Junction leakage
  - Gate oxide leakage
  - DC current flow in ratioed logic such as pseudo-nMOS logic

Power Equations

$$P = C_L V_{DD}^2 f + 2/3\beta_n (V_{DD}/2 - V_{THn})^3 t_r f + V_{DD} I_{leakage}$$

Dynamic power (~90% today and decreasing relatively)

Short-circuit power (~8% today and decreasing absolutely)

Leakage power (~2% today and increasing)

Low Power Design

- Reduce voltage (prime choice !!)
  - Recent years have seen an acceleration in supply voltage reduction (5.0 V, 3.3/3.0 V, 2.5/2.2 V, 1.8 V, 1.5 V, 1.2 V, …)
  - Design at very low voltages still open question (0.3-0.5 V by 2020 !)
- Reduce switching activity
- Reduce physical capacitances: small junction, short wire
- Reduce static power
  - Use selectively ratioed circuits
  - Use selectively low V_{TH} devices
  - Leakage reduction: stacked devices, body bias, low temperature