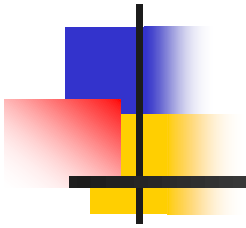

Electronic Circuits Design

Lecture – 10

- *Lab-1: Pass Transistor Circuits*
- *Lab-2: CMOS Inverter*
- *Lab-3: Complementary CMOS Gate*

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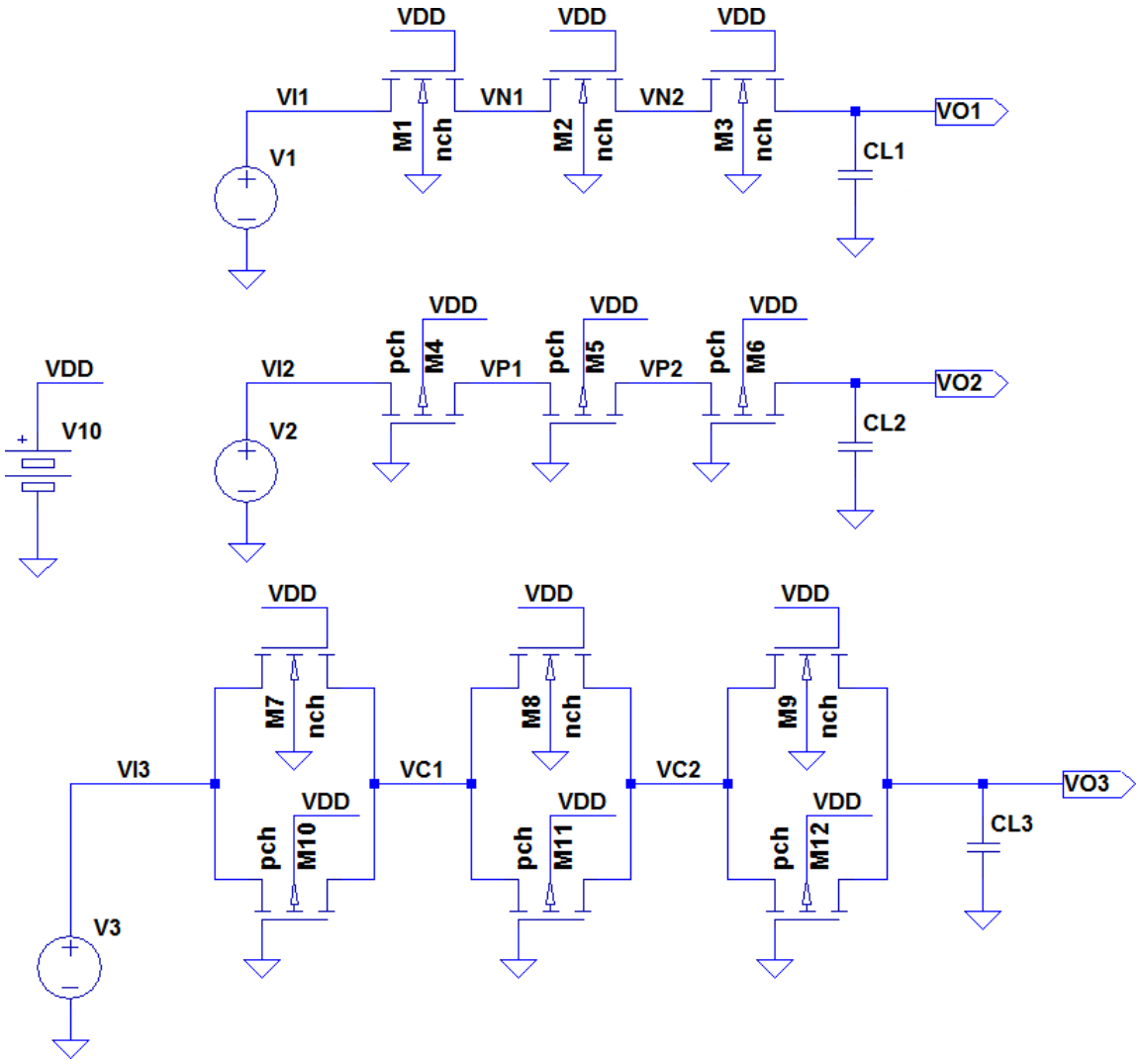
Lab-1: Pass Transistor Circuits



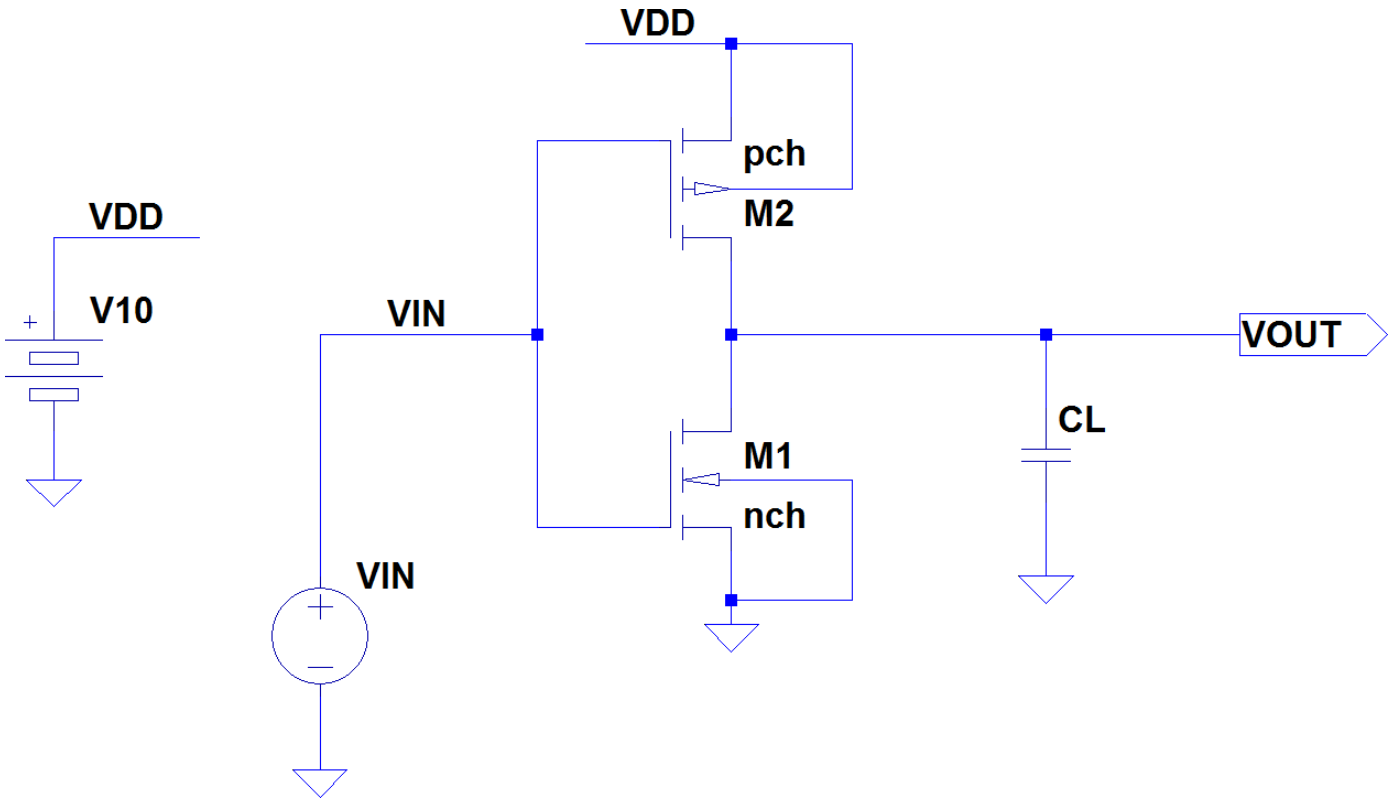
Lab-1: Pass Transistor Circuits

❖ **Simulation Condition**

- **CMOS model parameter: MOSIS/TSMC_0.18µm**
- **VDD = 1.8 V**
- **W_N/L_N = 4µm/0.18µm, W_P/L_P = 10µm/0.18µm**
- **CL1 = CL2 = 50 fF, CL3 = 800 fF**
- **V1 = V3 = PULSE(0 1.8V 19ns 1ns 1ns 39ns 80ns),**
  V2 = PULSE(1.8V 0V 19ns 1ns 1ns 39ns 80ns)
- **Transient analysis from 0 to 240 ns**

1) **Create the LTSpice schematic of the pass transistor circuits.**
2) **Obtain a plot of (VI1, VN1, VN2, VO1), (VI2, VP1, VP2, VO2) and (VI3, VC1, VC2, VO3) versus time.**
3) **Estimate the values of V_{THN} and V_{THP} respectively, reflecting the body effect.**
4) **Make comments if you need.**

Lab-2: CMOS Inverter



Lab-2: CMOS Inverter

❖ **Simulation Condition**

- **CMOS model parameter: MOSIS/TSMC_0.18µm**
- **VDD = 1.8 V**
- **W_N/L_N = 5µm/0.18µm, L_P = 0.18µm**
- **CL = 500 fF**

1) **Create the LTSpice schematic of the CMOS inverter.**
2) **Obtain the DC voltage transfer curve (VIN = DC sweep from 0 V to VDD) to provide V_{LT} = 0.5VDD. What is the size of W_P ?**
3) **From the VTC result of 2), estimate the values of V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L and NM_H.**
4) **Let VIN = PULSE(0 1.8V 4.5ns 0.5ns 0.5ns 9.5ns 20ns). From transient simulation results from 0 to 40ns, measure t_r, t_f, t_{pLH}, t_{pHL} and average active power consumed by the inverter.**
5) **Make comments if you need.**

Lab-3: Complementary CMOS Gate

1) **Create the LTSpice schematic of a complementary CMOS gate that provides a logic function of F = [A(B+C)+D]'.**
2) **Determine p-MOS channel width W_P to drive the output symmetrically for the worst rising and falling, supposing that i) all p-MOS transistors have the same W_P/L_P in the gate; ii) all n-MOS transistors have the same W_N/L_N in the gate; iii) W_N = 4 μm and $L_P = L_N$ = 0.18 μm; iv) $\mu_N = 2.5\mu_P$ and $V_{THN} = -V_{THP}$.**
3) **Following the simulation specifications in the below, obtain a plot of VA, VB, VC, VD and VF versus time. Verify the logic functionality.**

   - **CMOS model parameter: MOSIS/TSMC_0.18μm**
   - **VDD = 1.8 V**
   - **VA = PULSE(0 1.8V 4.5ns 0.5ns 0.5ns 4.5ns 10ns)**
   - **VB = PULSE(0 1.8V 9.5ns 0.5ns 0.5ns 9.5ns 20ns)**
   - **VC = PULSE(0 1.8V 19.5ns 0.5ns 0.5ns 19.5ns 40ns)**
   - **VD = PULSE(0 1.8V 39.5ns 0.5ns 0.5ns 39.5ns 80ns)**
   - **Transient analysis 0 to 160 ns**

4) **Make comments if you need.**