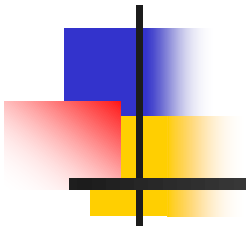

Electronic Circuits Design

Lecture – 7

- ***Digital-to-Analog Converter***

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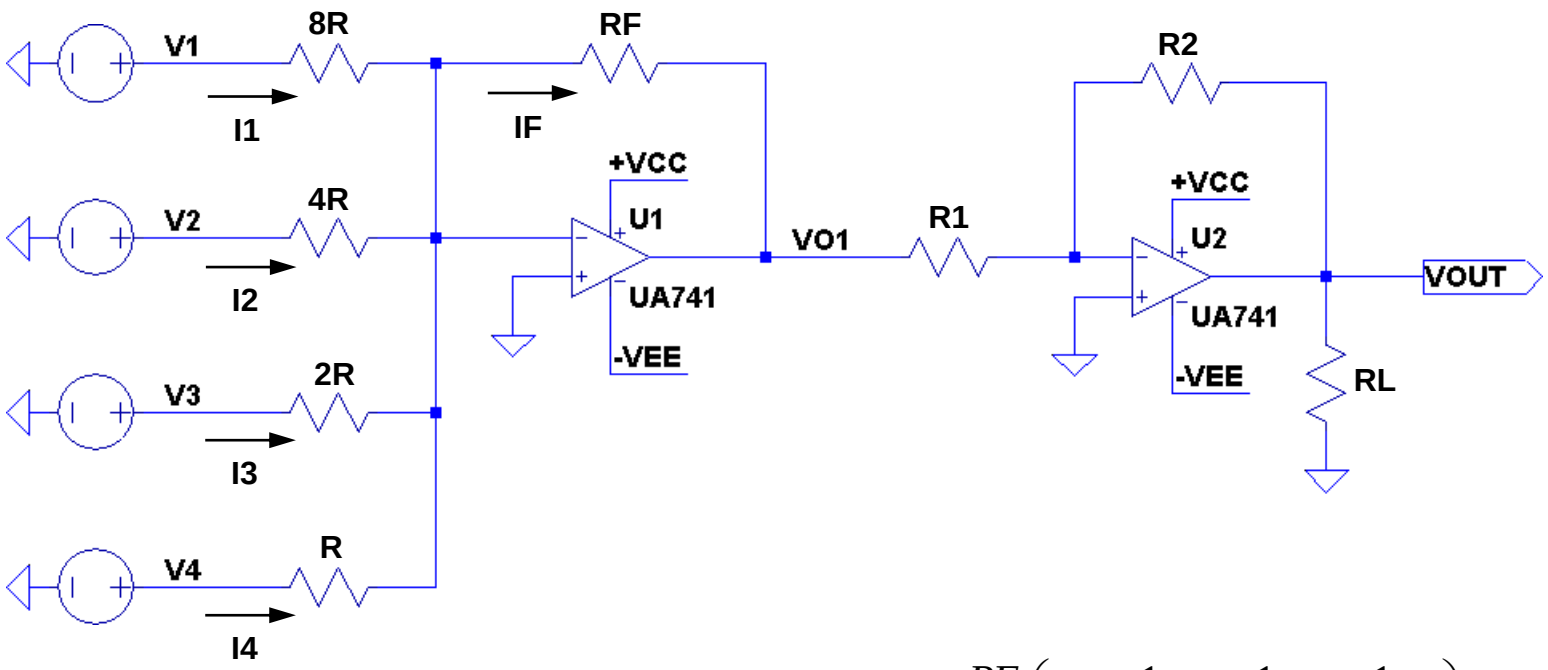
Binary-Weighted Resistor DAC



$$VO1 = -\frac{RF}{R}\left(V4 + \frac{1}{2}V3 + \frac{1}{4}V2 + \frac{1}{8}V1\right)$$

- V4, V3, V2, V1: binary digital signal
- V4 = MSB, V1 = LSB

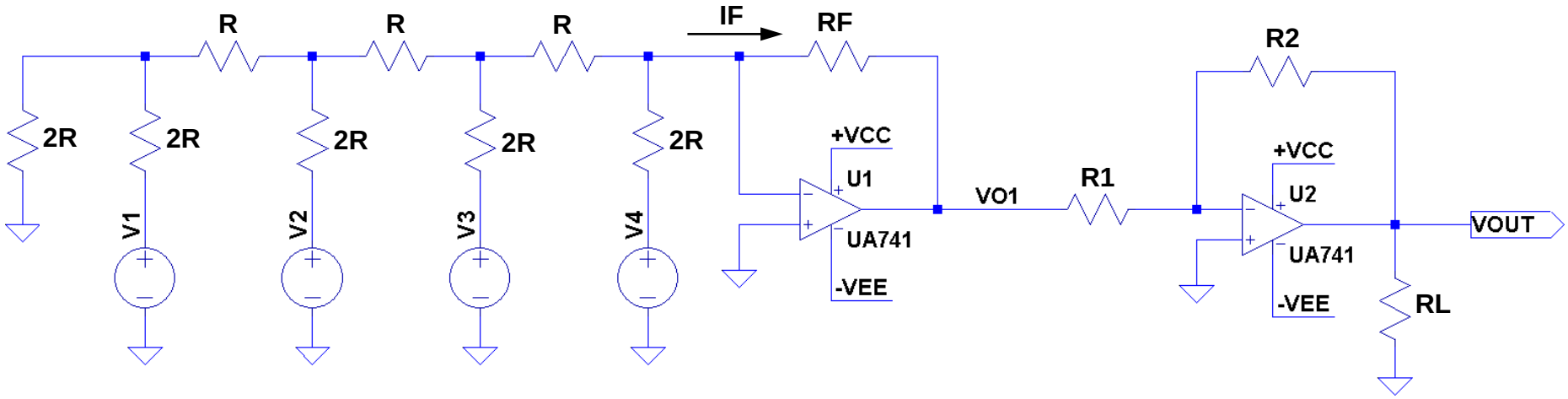
$$VOUT = \frac{R2}{R1}\left(\frac{RF}{R}\right)\left(V4 + \frac{1}{2}V3 + \frac{1}{4}V2 + \frac{1}{8}V1\right)$$

Lab-1: Binary-Weighted Resistor DAC

- **Simulation Condition**
  - **Op Amp: μA741**
  - **RL = 5 kΩ**
  - **+VCC = 15 V, -VEE = -15 V**
  - **V4 = PULSE(0 1.8V 1ms 1ns 1ns 1ms 2ms)**
  - **V3 = PULSE(0 1.8V 0.5ms 1ns 1ns 0.5ms 1ms)**
  - **V2 = PULSE(0 1.8V 0.25ms 1ns 1ns 0.25ms 0.5ms)**
  - **V1 = PULSE(0 1.8V 0.125ms 1ns 1ns 0.125ms 0.25ms)**
  - **Transient analysis 0 to 10 ms**

1) **Design the 4-bit binary-weighted resistor DAC with a bit resolution of 0.3 V, and obtain a plot of V1, V2, V3, V4 and VOUT versus time.**
2) **Design the 4-bit binary-weighted resistor DAC with the largest bit resolution, and obtain a plot of V1, V2, V3, V4 and VOUT versus time.**
3) **Make a comment on your design if you need.**

R-2R Resistor DAC



- V4, V3, V2, V1: binary digital signal
- V4 = MSB, V1 = LSB

- From the superposition's principle and Thevenin's theory;

$$IF = \frac{V4}{2R} + \frac{V3}{4R} + \frac{V2}{8R} + \frac{V1}{16R}$$

$$VO1 = -IF \times RF = -\frac{RF}{2R}\left(V4 + \frac{1}{2}V3 + \frac{1}{4}V2 + \frac{1}{8}V1\right)$$

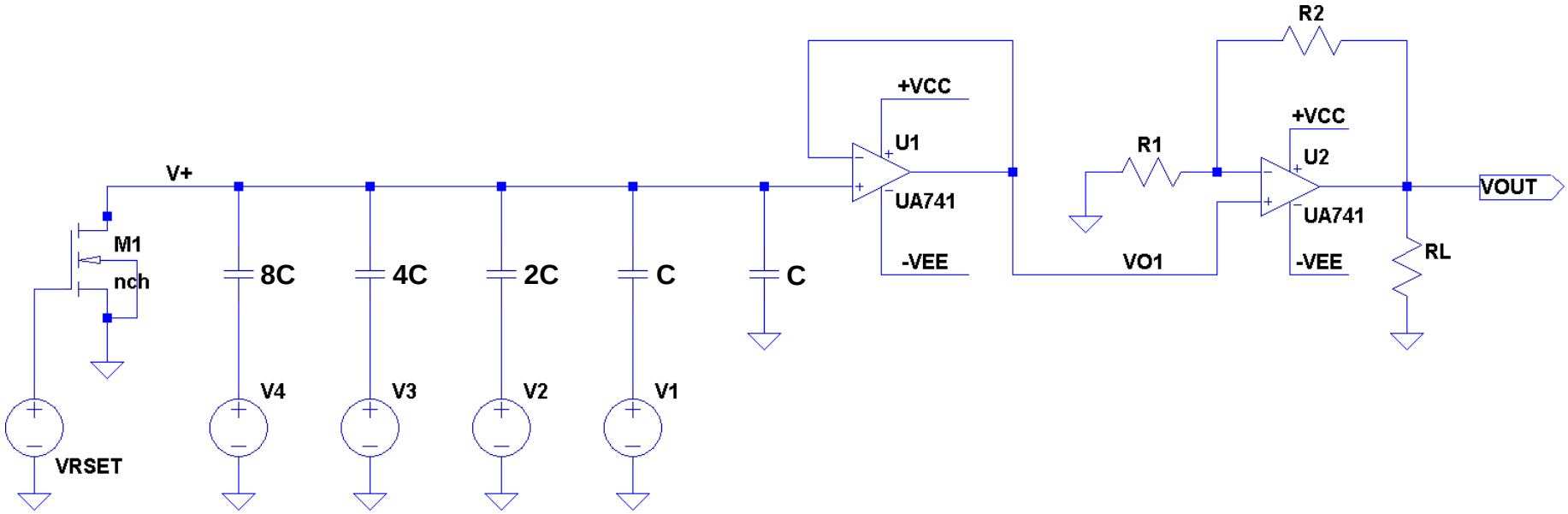
$$VOUT = \frac{R2}{R1}\left(\frac{RF}{2R}\right)\left(V4 + \frac{1}{2}V3 + \frac{1}{4}V2 + \frac{1}{8}V1\right)$$

Lab-2: R-2R Resistor DAC

- **Simulation Condition**
  - **Op Amp: μA741**
  - **RL = 5 kΩ, +VCC = 15 V, -VEE = -15 V**
  - **V4 = PULSE(0 1.2V 500us 1ns 1ns 500us 1000us)**
  - **V3 = PULSE(0 1.2V 250us 1ns 1ns 250us 500us)**
  - **V2 = PULSE(0 1.2V 125us 1ns 1ns 125us 250us)**
  - **V1 = PULSE(0 1.2V 62.5us 1ns 1ns 62.5us 125us)**
  - **Transient analysis 0 to 5 ms**

1) **Design the 4-bit R-2R resistor DAC with a bit resolution of 0.4 V, and obtain a plot of V1, V2, V3, V4 and VOUT versus time.**
2) **Change the LSB digital input V1 to (DC) 0 V, then obtain a plot of V1, V2, V3, V4 and VOUT versus time. How does the DAC work? Make a comment on your results.**
3) **Change the MSB digital input V4 to (DC) 0 V, then obtain a plot of V1, V2, V3, V4 and VOUT versus time. How does the DAC work? Make a comment on your results.**

Charge Scaling DAC



- V4, V3, V2, V1: binary digital signal
- V4 = MSB, V1 = LSB

- When the NMOS is off ;

$$VO1 = V+ = \frac{V4}{2} + \frac{V3}{4} + \frac{V2}{8} + \frac{V1}{16}$$

$$VOUT = \left(1 + \frac{R2}{R1}\right)\left(\frac{1}{2}\right)\left(V4 + \frac{1}{2}V3 + \frac{1}{4}V2 + \frac{1}{8}V1\right)$$

Lab-3: Charge Scaling DAC

❖ **Simulation Condition**

- **Op Amp: µA741**
- **NMOS: W/L = 50µm/0.18µm**
- **RL = 5 kΩ**
- **+VCC = 15 V, -VEE = -15 V**
- **V4 = PULSE(0 1.8V 1ms 1ns 1ns 1ms 2ms)**
- **V3 = PULSE(0 1.8V 0.5ms 1ns 1ns 0.5ms 1ms)**
- **V2 = PULSE(0 1.8V 0.25ms 1ns 1ns 0.25ms 0.5ms)**
- **V1 = PULSE(0 1.8V 0.125ms 1ns 1ns 0.125ms 0.25ms)**
- **VRSET = PULSE(0 1.8V 0.02ms 1ns 1ns 0.05ms 2ms)**
- **Transient analysis 0 to 10 ms**

1) **Design the 4-bit charge scaling DAC with a bit resolution of 0.5 V, and obtain a plot of V1, V2, V3, V4, VRSET, VO1 and VOUT versus time.**
2) **Make a comment on your design if you need.**