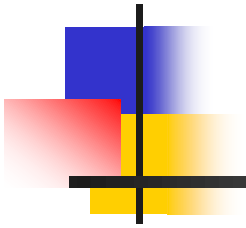
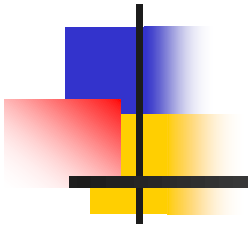


Electronic Circuits Design

Lecture – 11

- ***Delay-Based CMOS Gates***
- ***How to Add / Use Standard Gate Symbols in LTSpice***
- ***Lab Design***

Yeonbae Chung
School of Electronics Engineering
Kyungpook National University

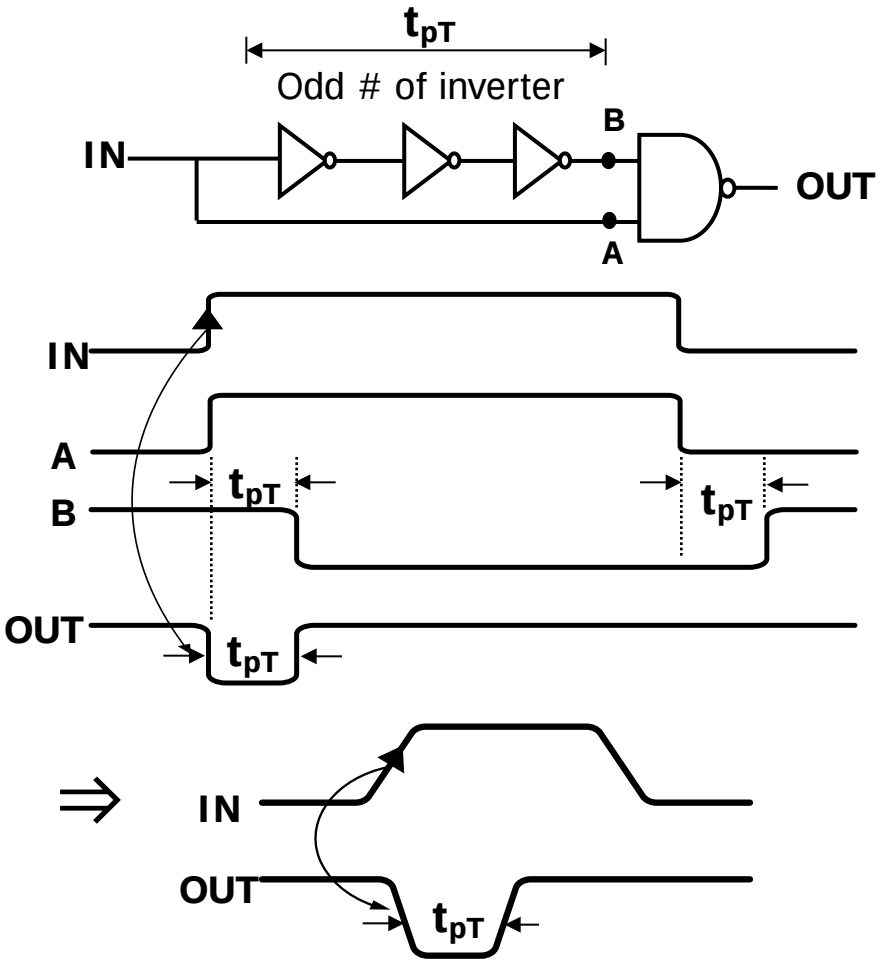


Delay-Based CMOS Gates

Delay-Based CMOS Gates

- CMOS gate utilizing a kind of delay circuit
  - Pulse Generator
  - Delayed Signal Generator
- Used for Sequential Circuits
  - Clock
  - Sequencing Circuit Element

Pulse Generator



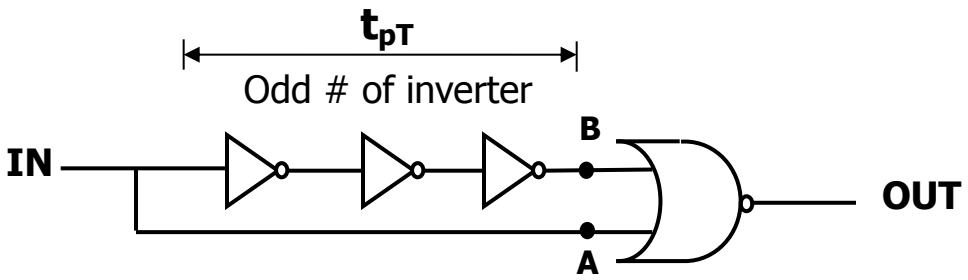
$$t_{pT} \simeq \sum_{i=1}^{n} t_{pi}$$

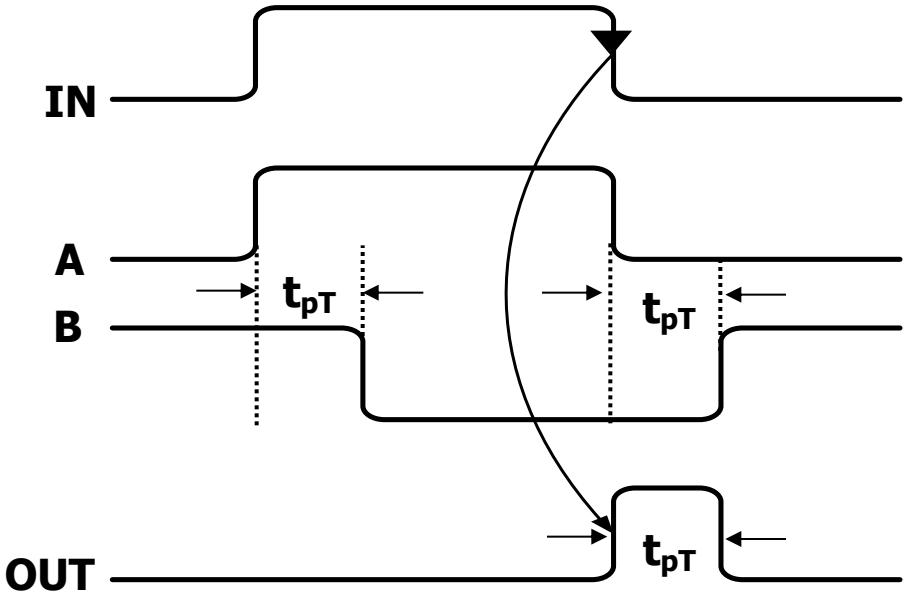
where $t_{pi} = (t_{pHLi} + t_{pLHi})/2$

$= 0.8(1/\beta_{Ni} + 1/\beta_{Pi})C_{Li}/V_{DD}$

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

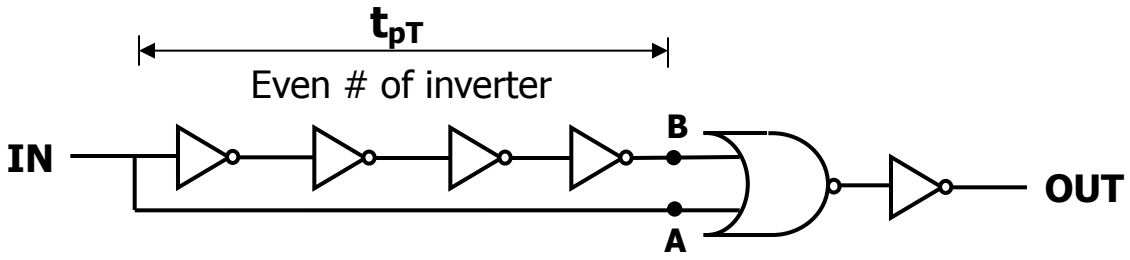
Pulse Generator

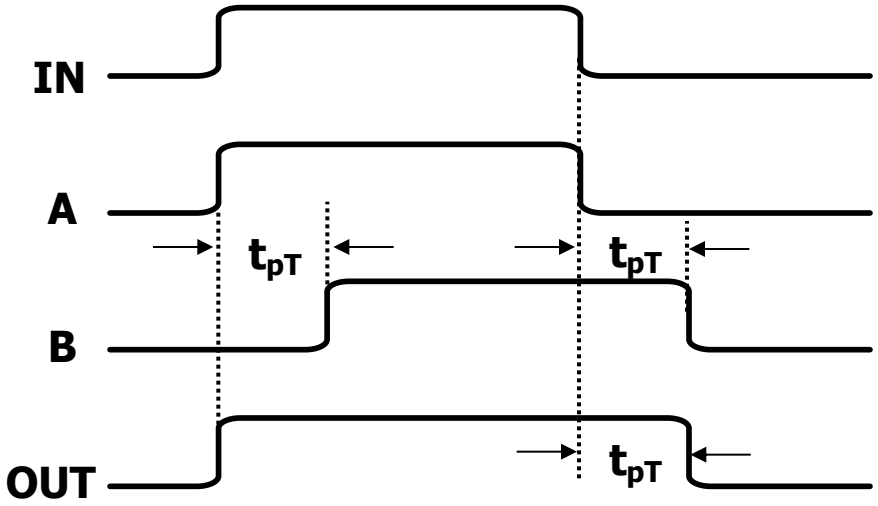




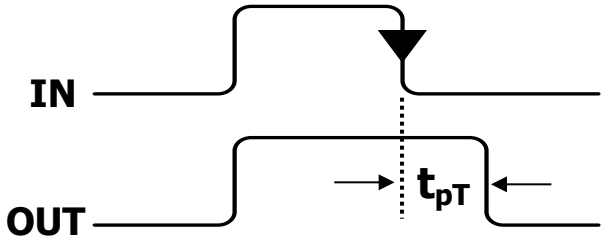
A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Delayed Signal Generator

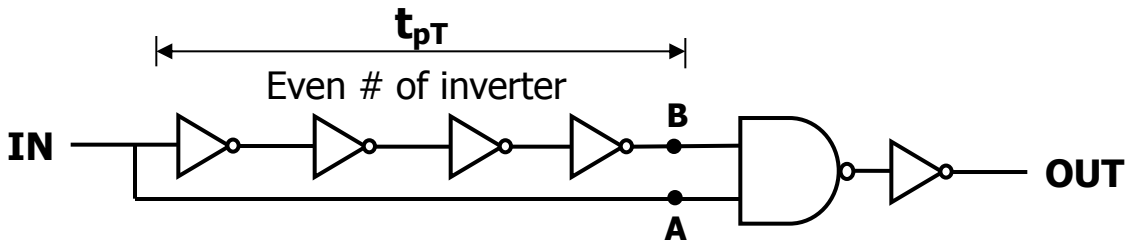


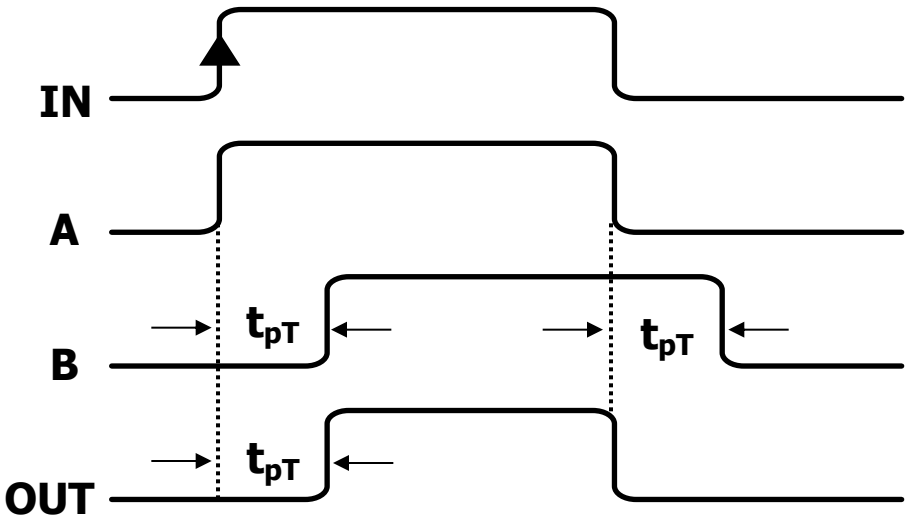


A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

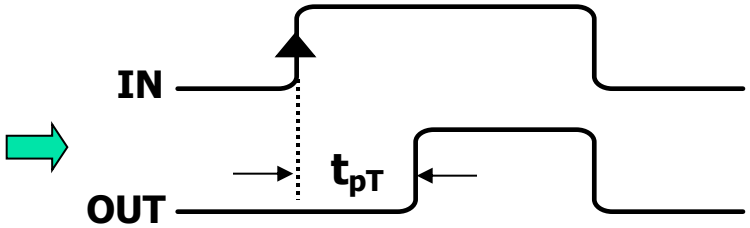


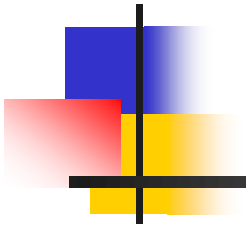
Delayed Signal Generator





A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1





How to Add / Use Standard Gate Symbols

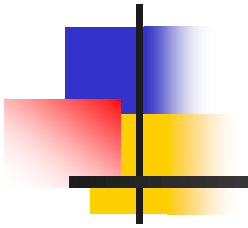
How to Add / Use Standard Gate Symbol ?

❖ **Standard CMOS Gates: inv, nand2, nand3, nand4, nor2, nor3, nor4, trans**

- Step 1: Copy the "standard_gate" subcircuit file to LTSpice user directory (D:₩ybchung).

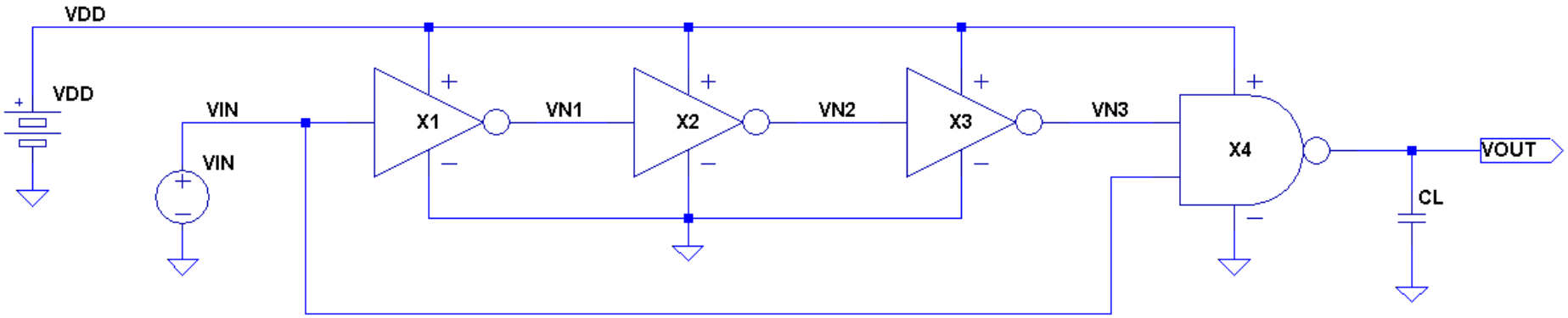
- Step 2: In LTSpice, insert "standard gate (inv, nand2, … or trans)" component. Right click on the symbol and add the values of transistor size in PARAMS (Ex: wp=5u lp=0.18u wn=2u ln=0.18u).

- Step 3: Add SPICE directive to the schematic.
".inc C:₩Program Files₩LTC₩LTspiceIV₩cmos_model₩cmos180_level49"



Lab Design

Lab-1: Pulse Generator



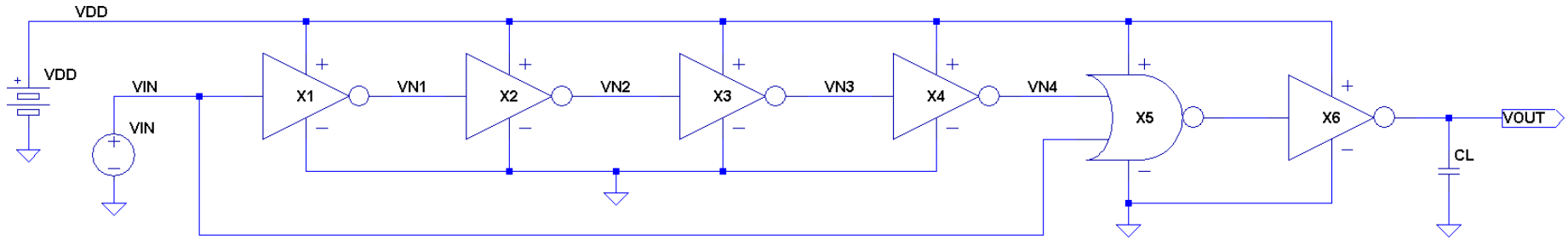
Lab-1: Pulse Generator

❖ **Simulation Condition**

- **CMOS model parameter: MOSIS/TSMC_0.18µm**
  (0.3µm ≤ W ≤ 50µm, 0.18µm ≤ L ≤ 20µm)
- **VDD = 1.8 V, CL = 200 fF**
- **2-input NAND (X4): W_P/L_P = 7.5µm/0.18µm, W_N/L_N = 6µm/0.18µm**
- **VIN = PULSE(0 1.8V 9.5ns 0.5ns 0.5ns 9.5ns 20ns)**
- **Transient analysis from 0 to 45 ns**

1) **Create the LTSpice schematic of the pulse generator.**
2) **Determine transistor sizes of the inverter chain (X1, X2, X3) to provide a pulse width of 2 ns.**
3) **Obtain a plot of VIN, VN1, VN2, VN3 and VOUT versus time.**
4) **Change the supply voltage into 1.2 V, then obtain a plot of VIN, VN1, VN2, VN3 and VOUT versus time. What is value of the pulse width ?**
5) **Make comments if you need.**

Lab-2: Delayed Signal Generator



Lab-2: Delayed Signal Generator

❖ **Simulation Condition**

- **CMOS model parameter: MOSIS/TSMC_0.18µm**
  (0.3µm ≤ W ≤ 50µm, 0.18µm ≤ L ≤ 20µm)
- **VDD = 1.8 V, CL = 200 fF**
- **2-input NOR (X5): W_P/L_P = 5µm/0.18µm, W_N/L_N = 1µm/0.18µm**
- **Driving INV (X6): W_P/L_P = 5µm/0.18µm, W_N/L_N = 2µm/0.18µm**
- **VIN = PULSE(0 1.8V 9.5ns 0.5ns 0.5ns 9.5ns 20ns)**
- **Transient analysis from 0 to 45 ns**

1) **Create the LTSpice schematic of the delayed signal generator.**
2) **Determine transistor sizes of the inverter chain (X1, X2, X3, X4) to provide a delayed signal width of 2 ns.**
3) **Obtain a plot of VIN, VN1, VN2, VN3, VN4 and VOUT versus time.**
4) **Measure the standby power consumed by the circuit when VIN = 0 V (DC) and 1.8 V (DC) respectively.**
5) **Make comments if you need.**