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Flexible and Stackable Non-Volatile Resistive Memory for High Integration

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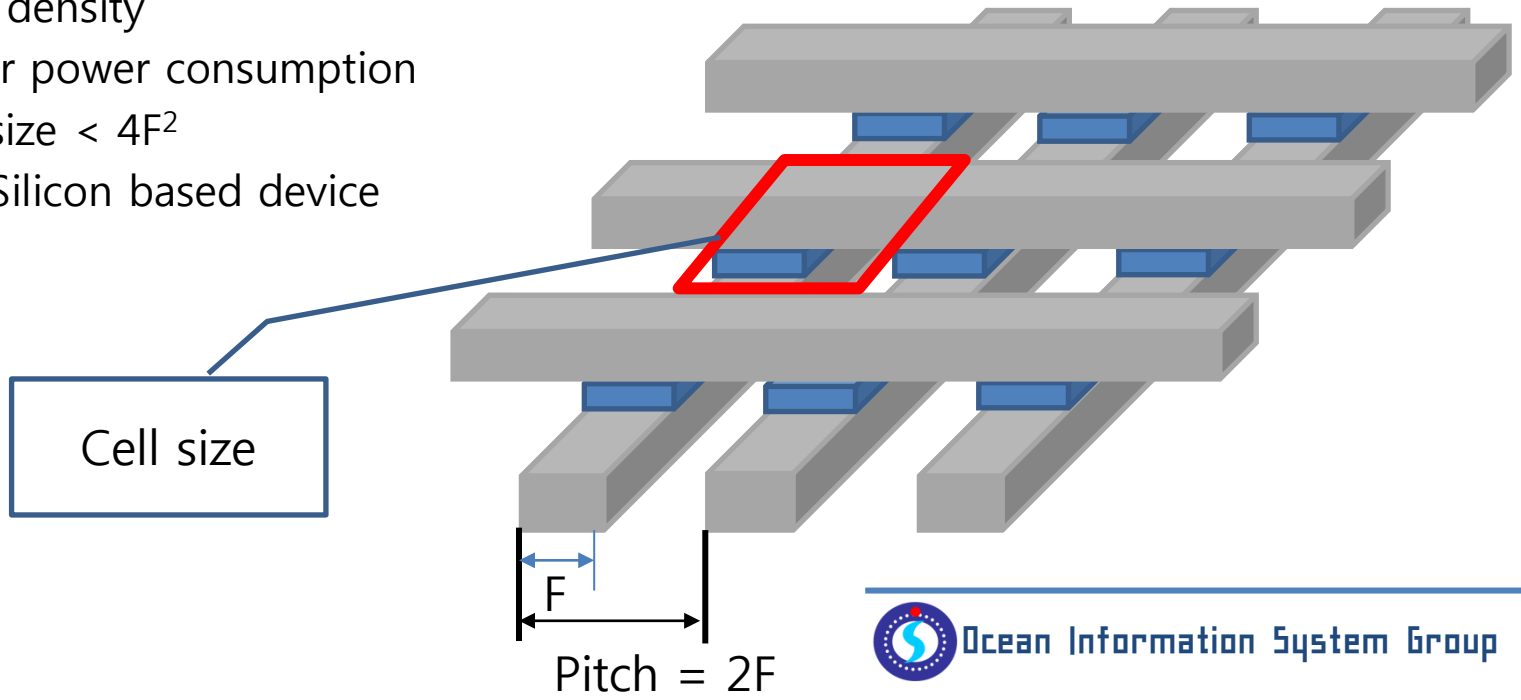
Resistive memory: Crossbar array

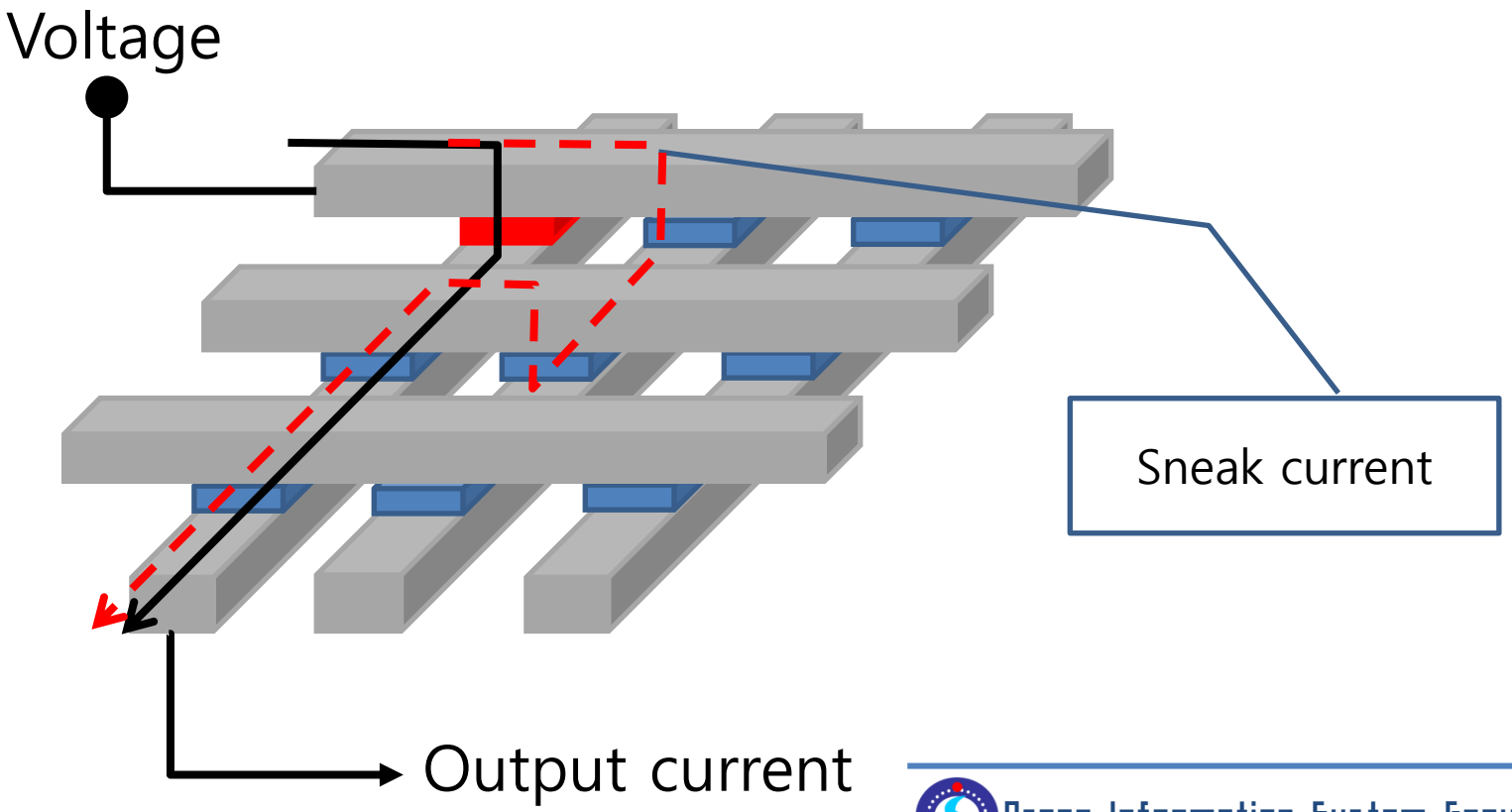
- Scaling limitation of the CMOS technology:
  - 2008 International Technology Roadmap for Semiconductors: "Beyond CMOS" ➔ "New switches"
  - N.Z. Haron, S. Hamdioui, Why is CMOS scaling coming to an END?, Design and Test Workshop, IDT 3rd International, 2008 pp. 98-103.

- HP group: proposed memristor
  - High density
  - Lower power consumption
  - Cell size < $4F^2$
  - Not Silicon based device



Resistive memory: Sneak current problem

- Sneak current: make big problems in terms of the data reading/ writing errors and an extra power consumption in read and write cycles in Linn, E.; Rosezin, R.; Kugeler, C.; Waser, R. Nat. Mater. 2010, 9, 403–406.



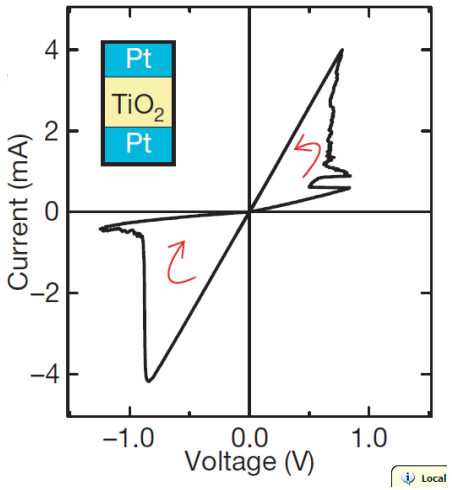
Memristor:

- Element was proposed by Leon Chua (UC Berkeley) in 1971.

MEMRISTOR

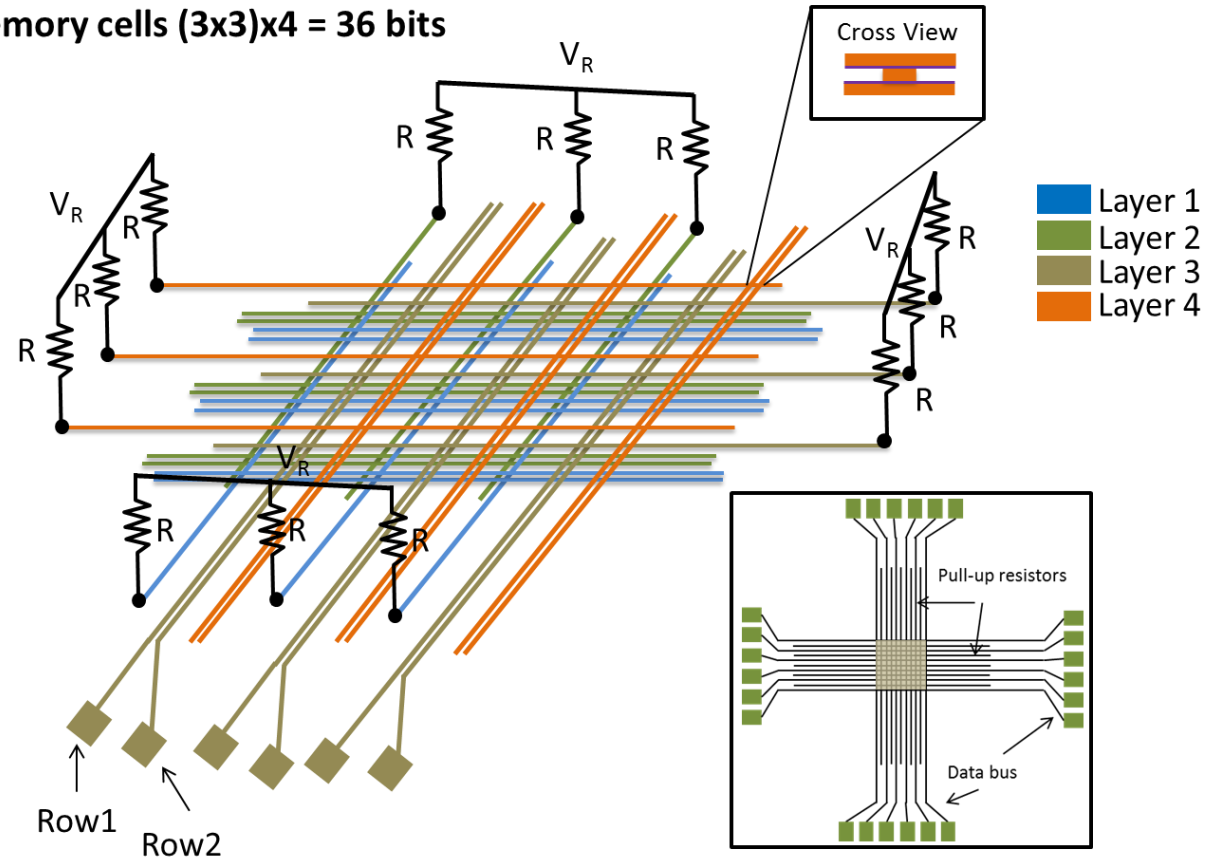
$$d\varphi = M\ dq$$

- R. Stanley Williams (HP Laboratories) found the Memristor in D. B. Strukov, et al., vol 453, 1 May 2008, doi:10.1038/nature06932.



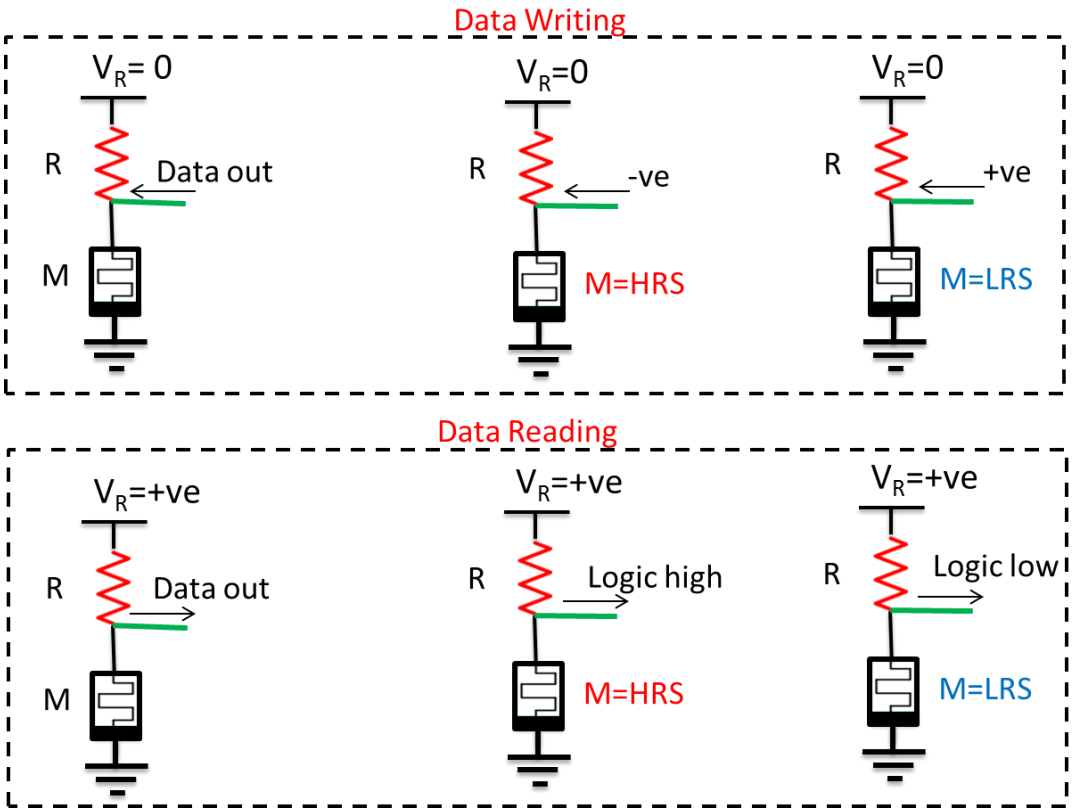
The goal

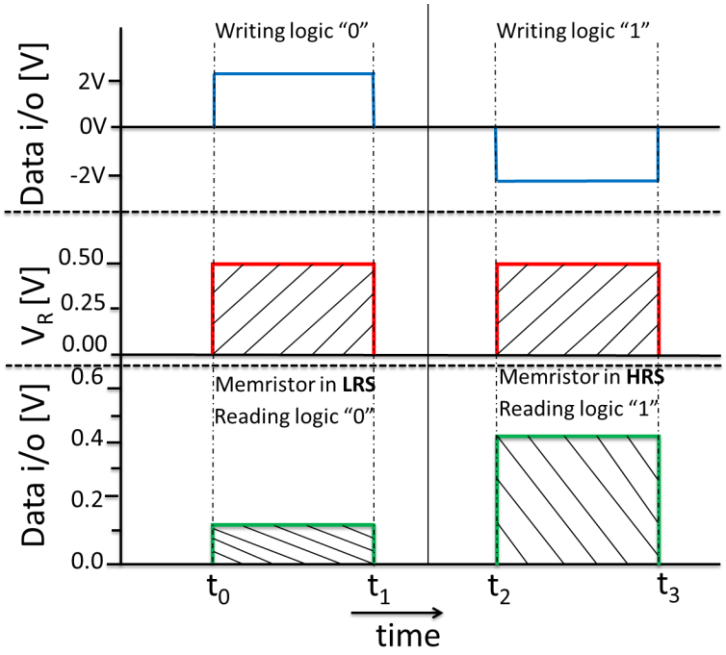
- We propose a novel flexible and stackable resistive random access memory (ReRAM) array with multi-layered crossbar structures fabricated on a PET flexible substrate through EHD system.



How to read and write data

- Voltage division principal to read/write data:

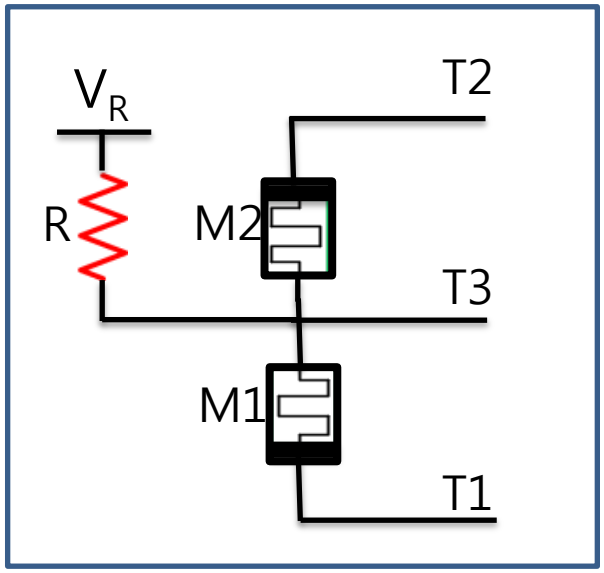


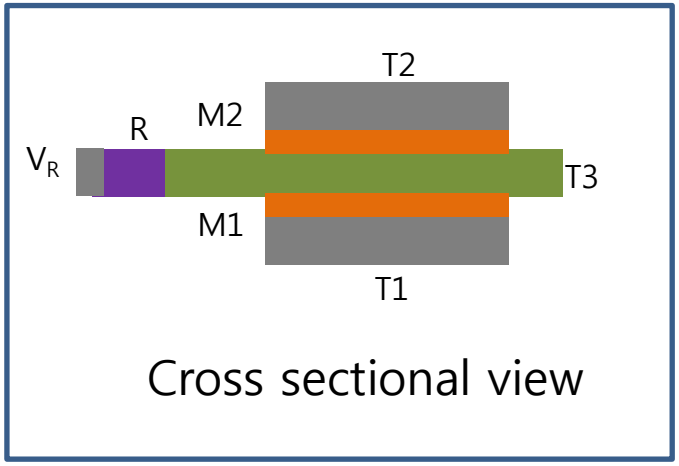


Ali, S., Bae, J., Choi, K. H., Lee, C. H., Doh, Y. H., Shin, S., and Kobayashi, N. P., "Organic non-volatile memory cell based on resistive elements through electro-hydrodynamic technique," Organic Electronics 17, 121-128 (2015).

Basic memory cell

- Our basic memory cell and operation:





M1 operation

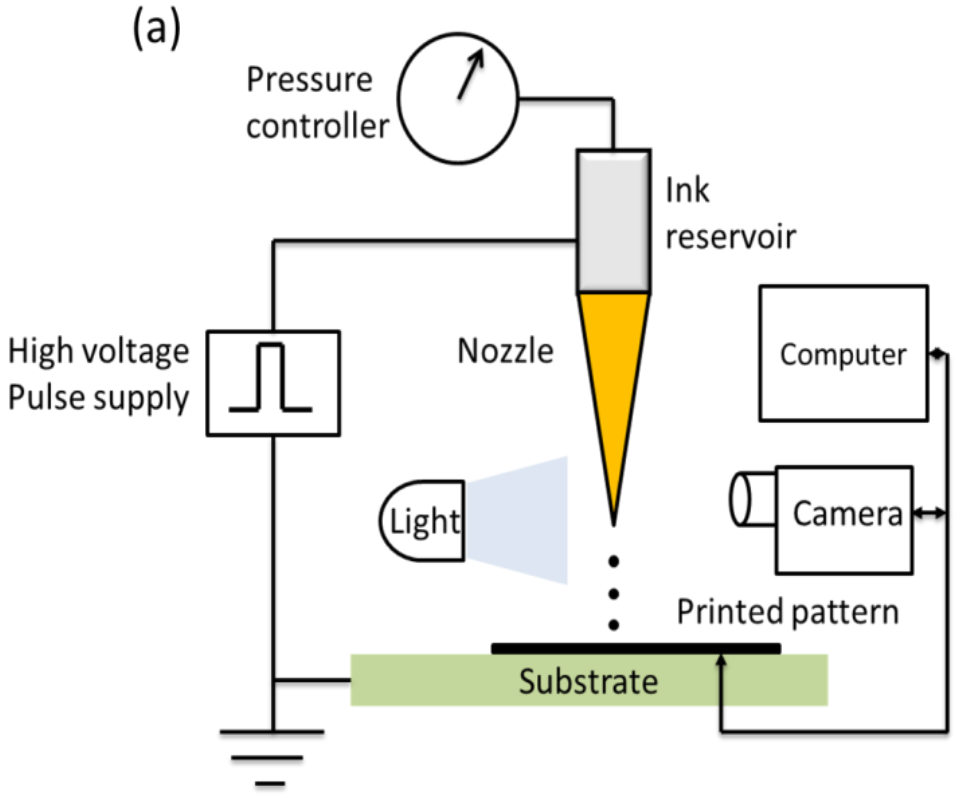
Operation	T_1	T2	T3
Write "0"	Ground	Open	2
Write "1"	Ground	Open	-2
Read logic 0/1	Ground	0=0.1V 1=0.9V	1V

M2 operation

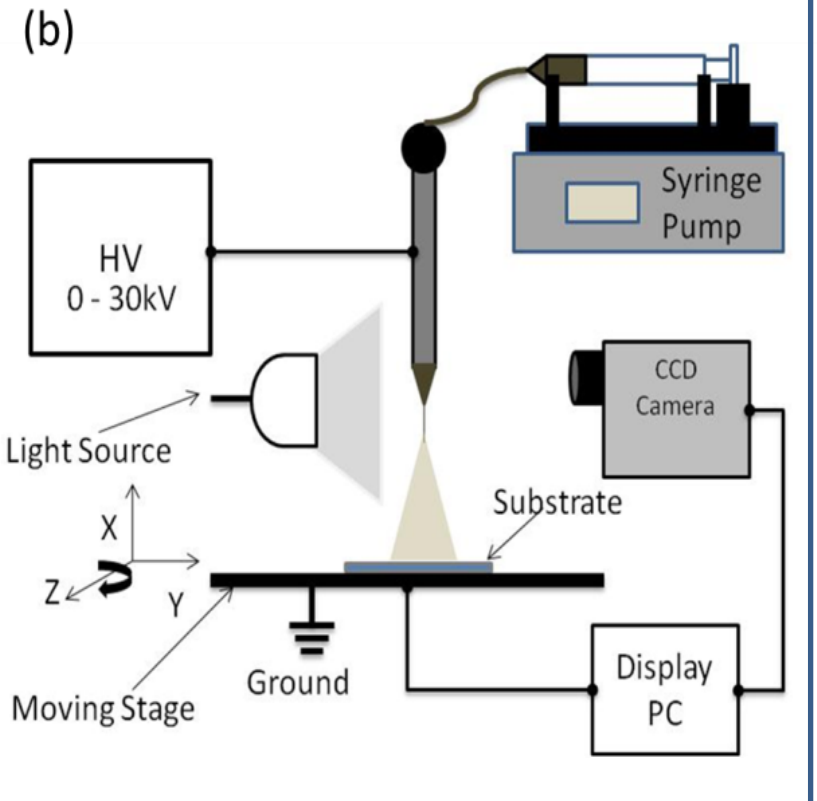
Operation	T_1	T2	T3
Write "0"	Open	Ground	-2
Write "1"	Open	Ground	2
Read logic 0/1	Ground	0=0.1V 1=0.9V	1V

Fabrication

- Deposition layer and crossbar:



Drop on Demand EHD: deposit printed pattern

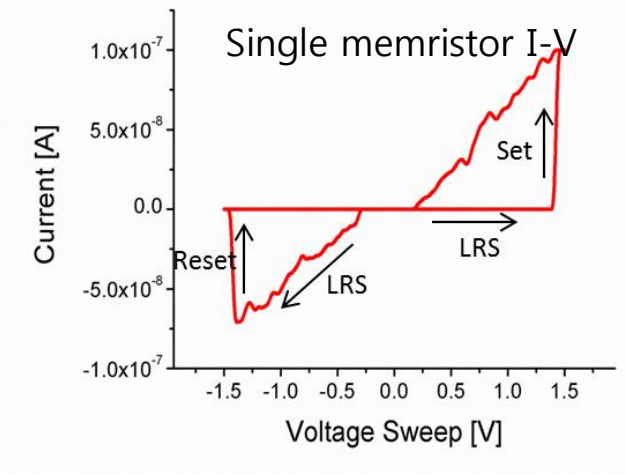


ESD: deposit thin film

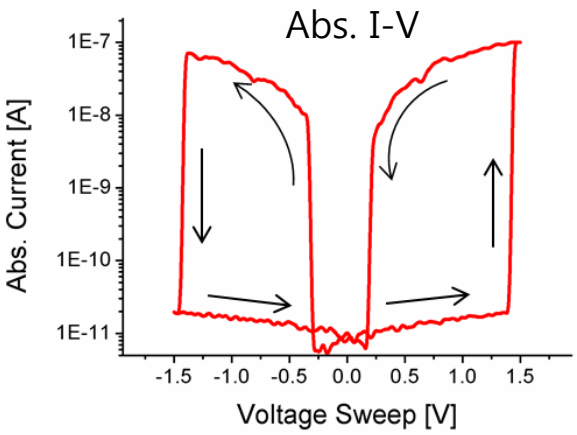
Memristor

- We fabricated the memristor based on PVP (poly(4-vinylphenol)):

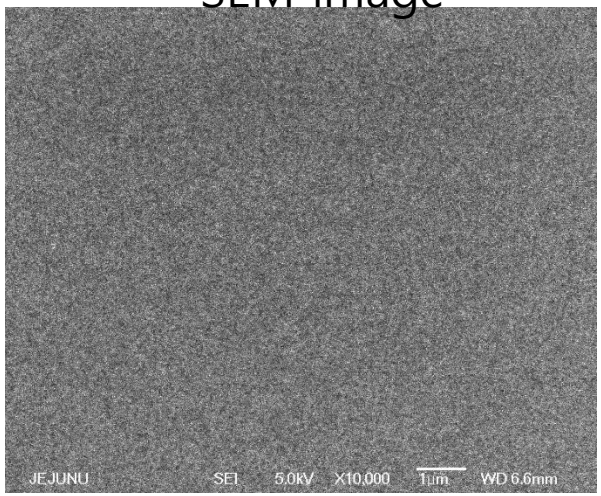
MIM structure



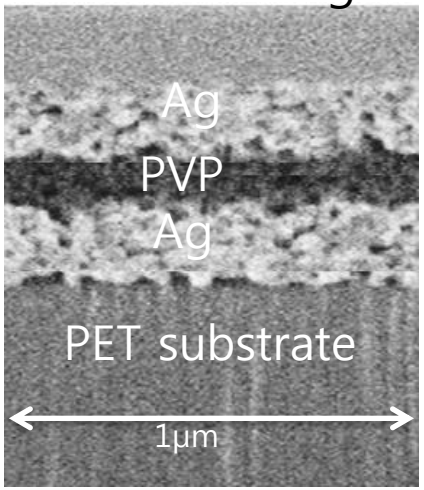
OFF/ON = ~ 4330 read @1V



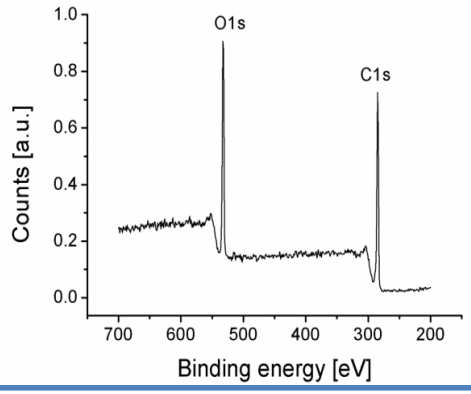
SEM image



FIB image



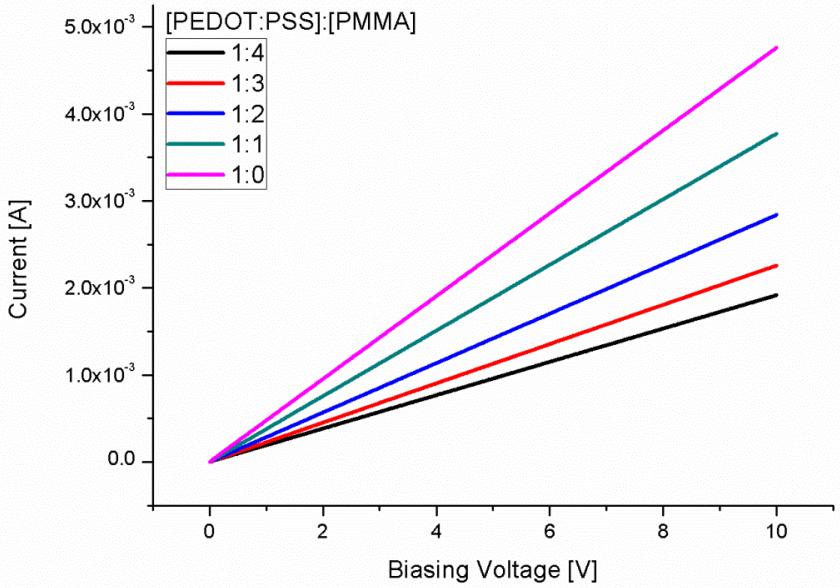
XPS of PVP

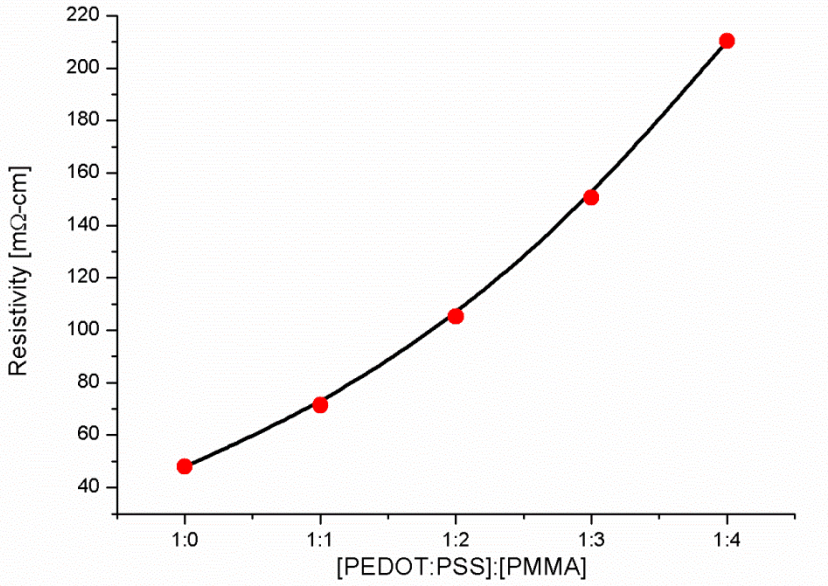


HRS: 66.66 GΩ, LRS: 14.28 GΩ

Pull-up resistor

- Pull-up resistor based on MEH:PPV and PMMA: 20 MΩ

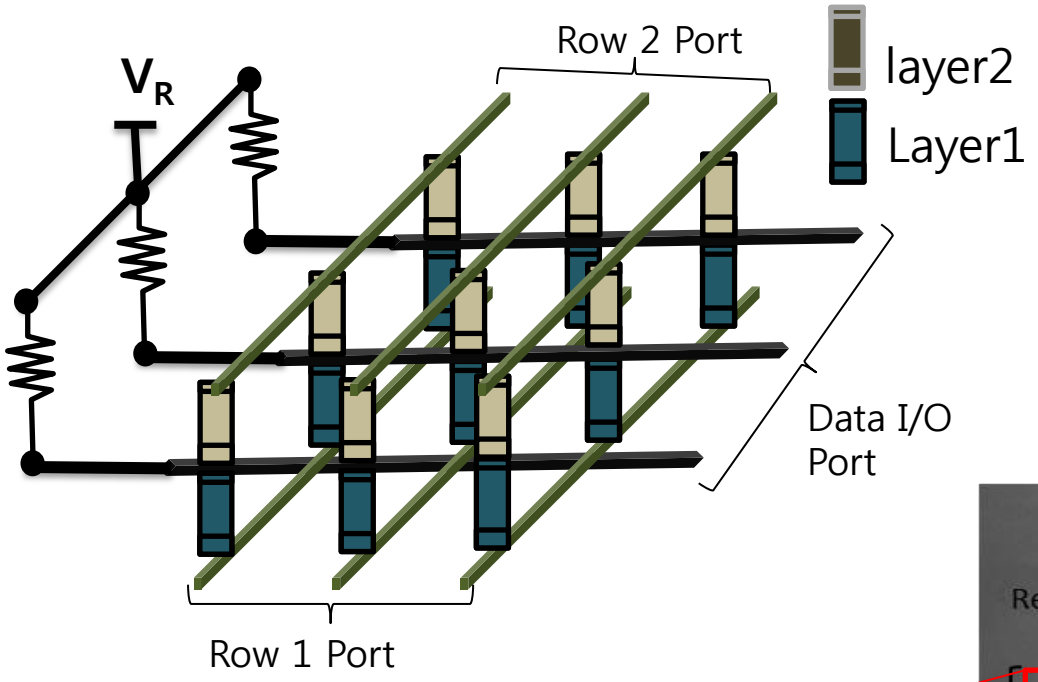


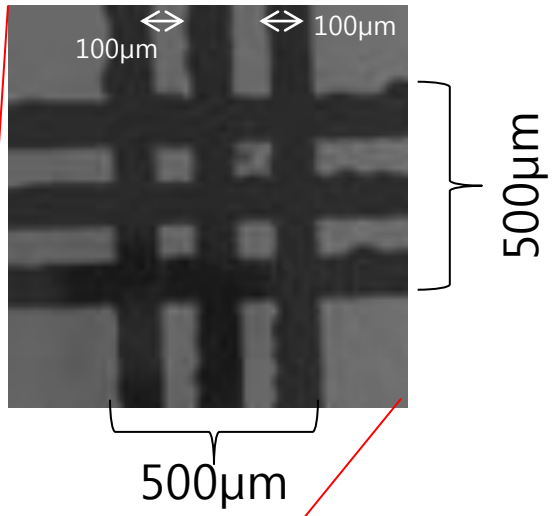


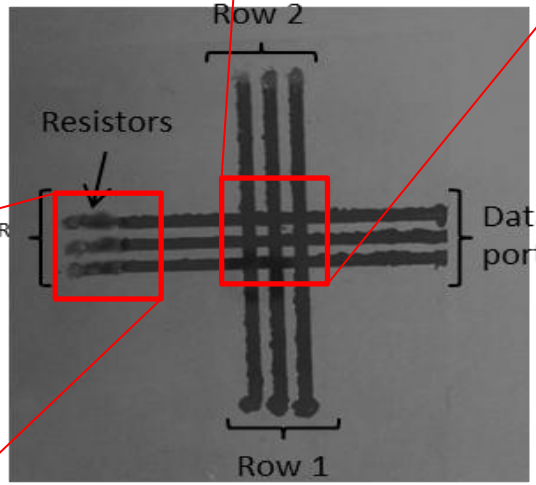
Ali, S., Bae, J., and Lee, C. H., "Design of versatile printed organic resistor based on resistivity (ρ) Control," Appl. Phys. A 119, 1499-1506 (2015).

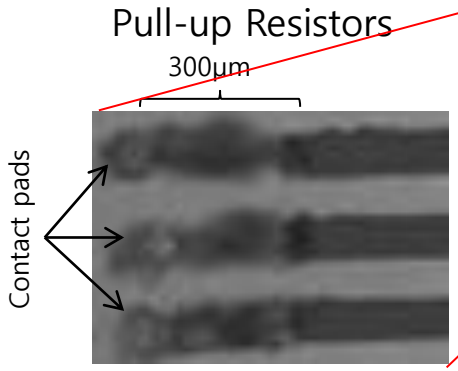
Fabricated two layered 3×3 memory

- The fabricated device:



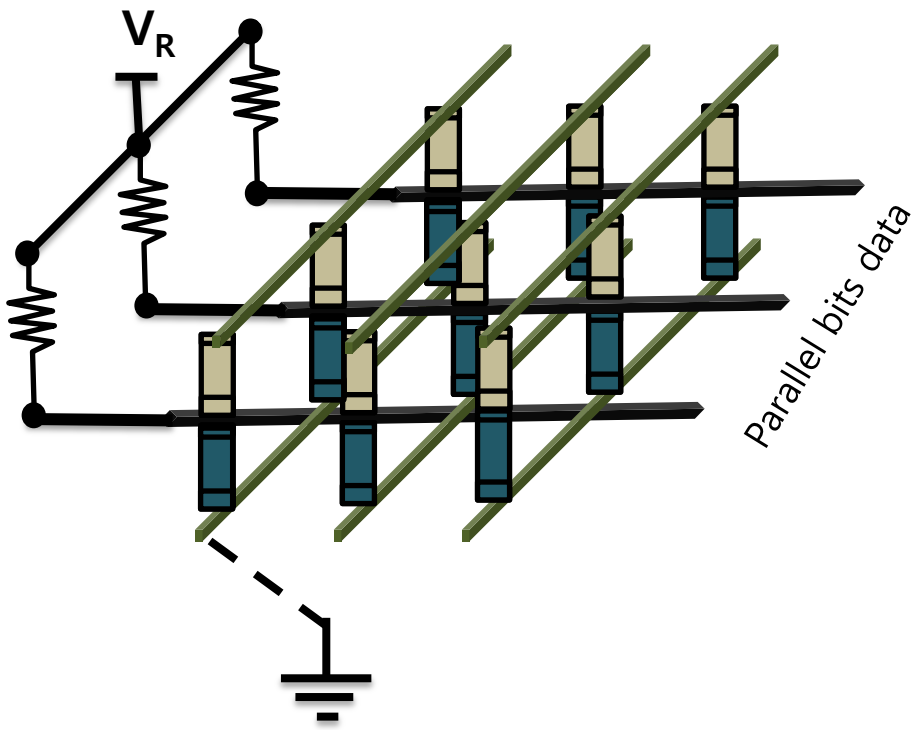




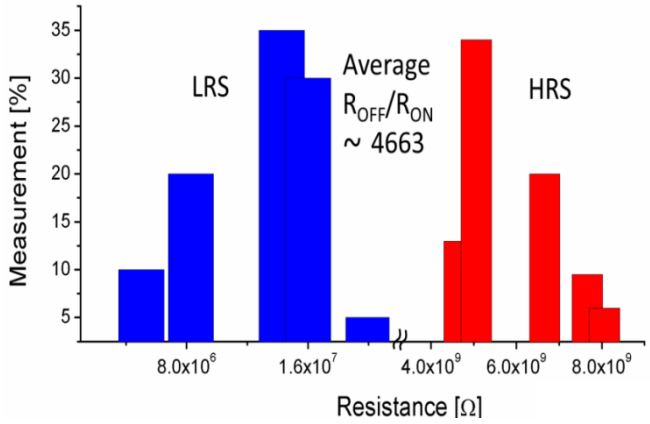


Read data

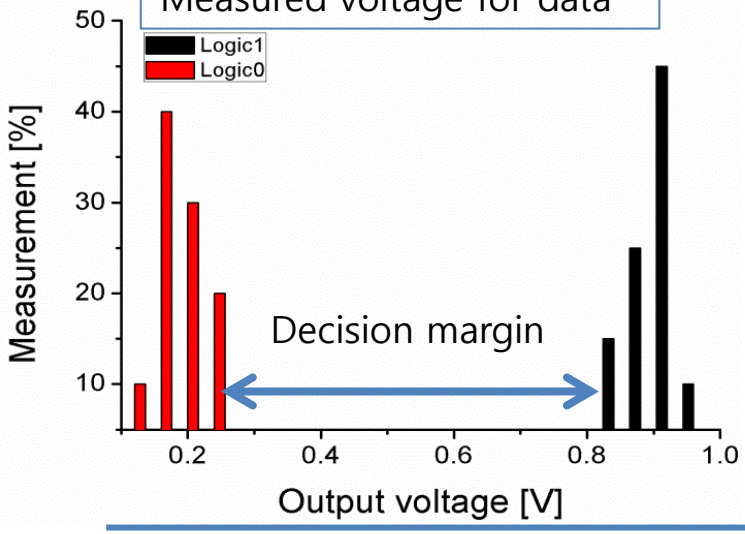
- The fabricated device:



Measured memristor resistance



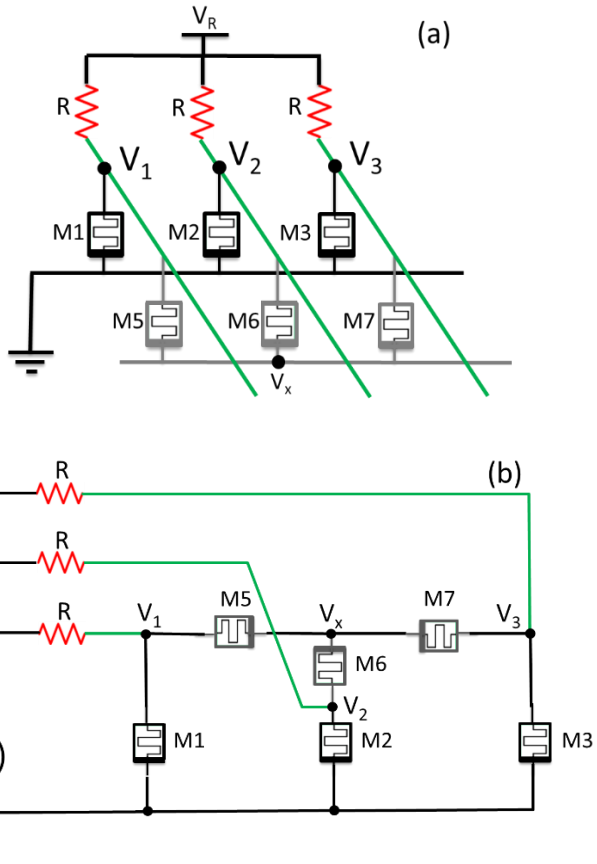
Measured voltage for data



It has a higher decision margin, but it has a problem
In occasions of a worst case by sneak current.

Reading problem with sneak current

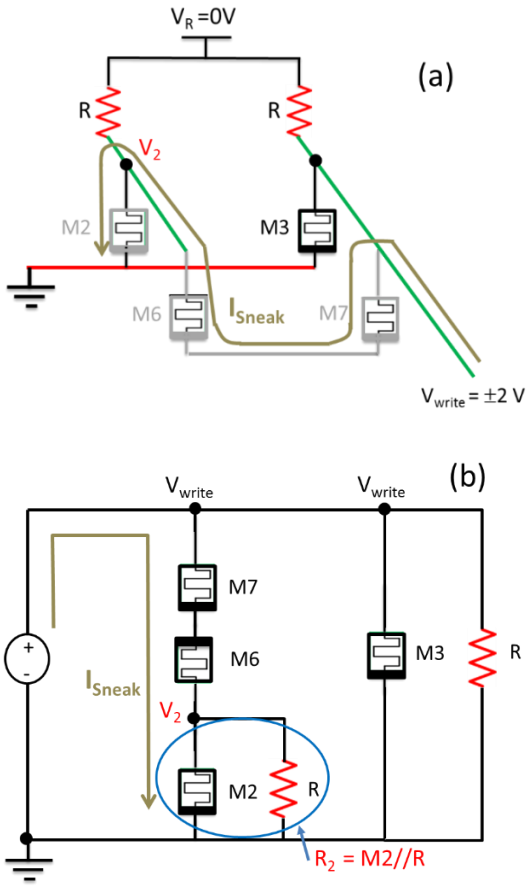
- Memory circuit with sneak current:



(a) A 2×3 memory array during data reading cycle. (b) Equivalent resistive circuit.

Writing problem with sneak current

- Memory circuit with sneak current:



If $\left|V_2 = \frac{R_2 V_{write}}{M6 + M7 + R_2}\right|$ > |Voltage of state switch|,

M2 is changed by the sneak current.

However, the proposed circuit avoid this problem

Due to $|V_2|$ < |Voltage of state switch|.

Here, R_2 is sufficiently decreased by R because R

Is smaller than M.

a) A 2×2 memory array during data writing cycle of the proposed structure. (b) Equivalent resistive circuit.

Conclusions

- We have proposed stackable memory based on materials PVP for memristor and MEH:PPV and PMMA for pull up resistor through EHD technology.
- We have fabricated two layered 3×3 memory.
- The resistance of the fabricated memristor is about HRS = 66.66 GΩ and LRS = 14.28 GΩ.
- The resistance of the fabricated memristor is 20 MΩ.
- The proposed device was obtained zero detection error, experimentally.
- The sneak current problem:
  - Read cycle: occurred several problem, but we can reduced this problem by choosing resistances of memristors and pull up resistors.
  - Write cycle: avoid the problem by the pull up resistors.

Thank you for your attention!