

Memristors

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History of VLSI



1956 Nobel Prize, Physics
(J. Bardeen, W. Shockley,
and W. Brattain)

Dec. 16, 1947



Dec. 16, 1947

- Shockley's semiconductor device concept (1945)
- Bardeen and Brattain's point-junction transistor (1947)
- Shockley's junction (sandwich) transistor (1950)
- Kahng and Attala's MOSFET (1960)

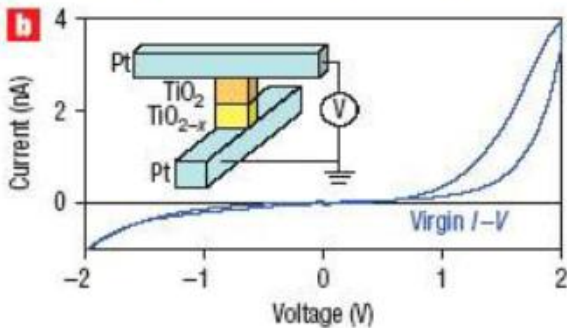
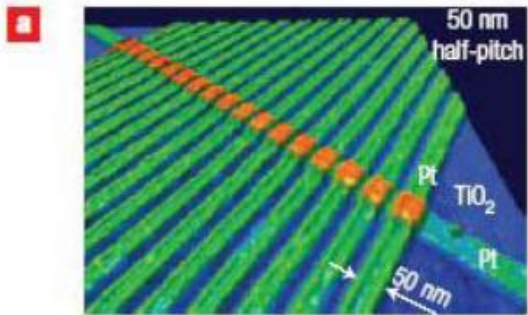
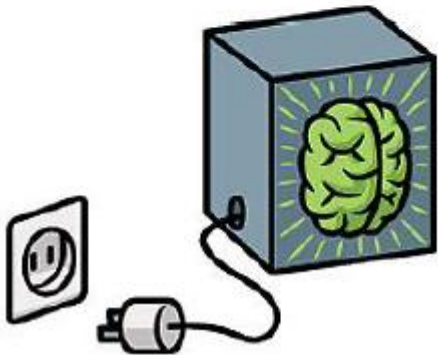
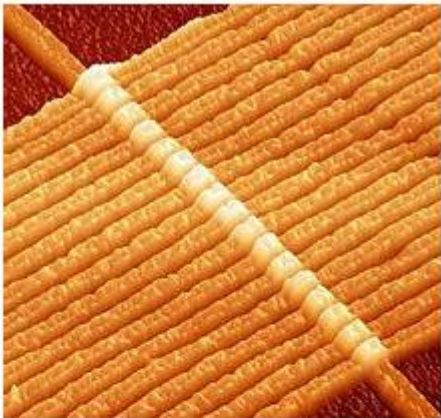
2000 Nobel Prize, Physics
(Jack Kilby)



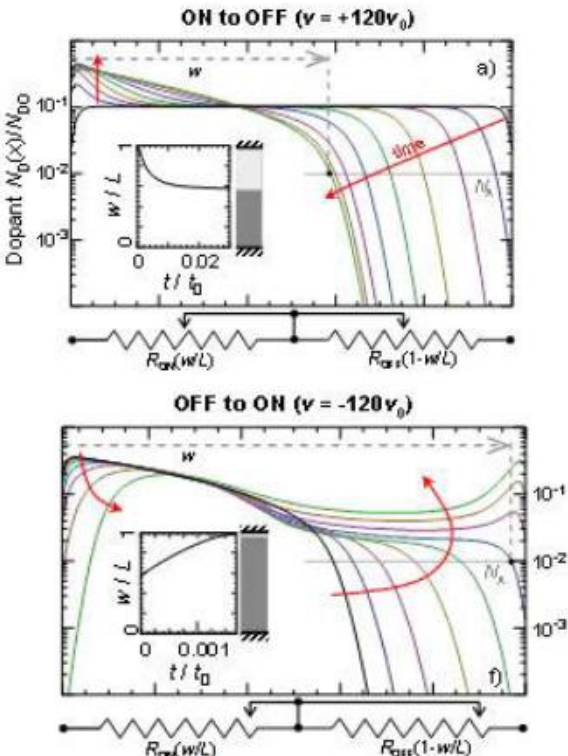
Germanium, 1T, 1C, 3R, Oscillator,
0.04 inch X 0.06 inch (Sept. 12, 1958)



2008: Memristive device invented by HP



J. Yang, D. Pickett, X. Li, Ohlberg, D. Stewart, R. S. Williams, *Nature Nanotech.* (2008)



D. Strukov, J. Borghetti, R. S. Williams, *Small* (2008)



The missing link in constitutive relations

$V = R I$ (Resistor)

$Q = C V$ (Capacitor)

$\Phi = L I$ (Inductor)

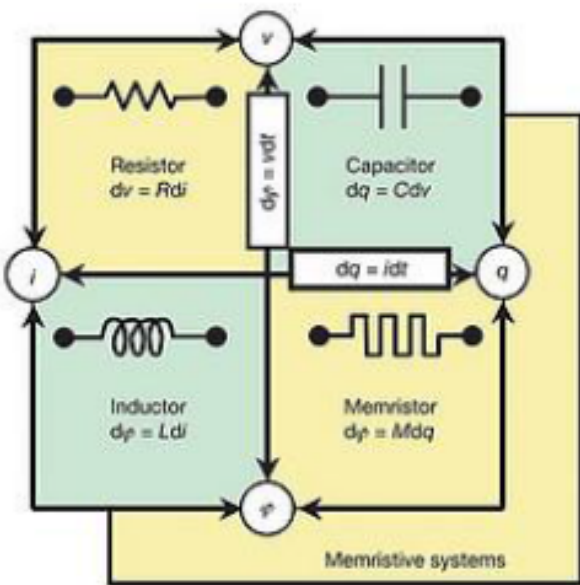
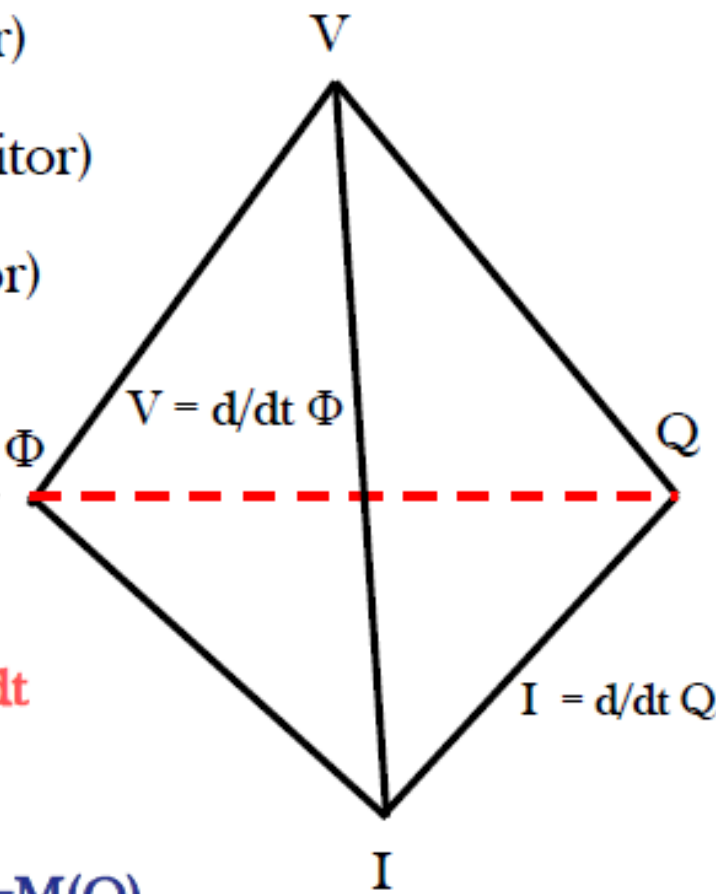
$\Phi = f(Q)$

$d\Phi / dt = df(Q) / dt$

$= df(Q) / dQ \cdot dQ / dt$

$V = M I$

Memristance $M = M(Q)$



Who are generalization of memristors



Memristor (1971 Chua)

$$\phi = f(q)$$

with property of
 $V = M(x) i$
 $dx/dt = i$

Memristive Device (1976 Chua and Kang)

$$V = R(\underline{x}, i, t) i$$
$$d\underline{x}/dt = \underline{f}(\underline{x}, i, t)$$

X is a much broader state variable.
When $\underline{f}(\underline{x}, i, t) = i$, $R(\underline{x}, i, t) = M(x)$,
then a memristor property.

Example:

- Thermistor
- Fluorescent Lamp
- Ionic channels in Hodgkin-Huxley model

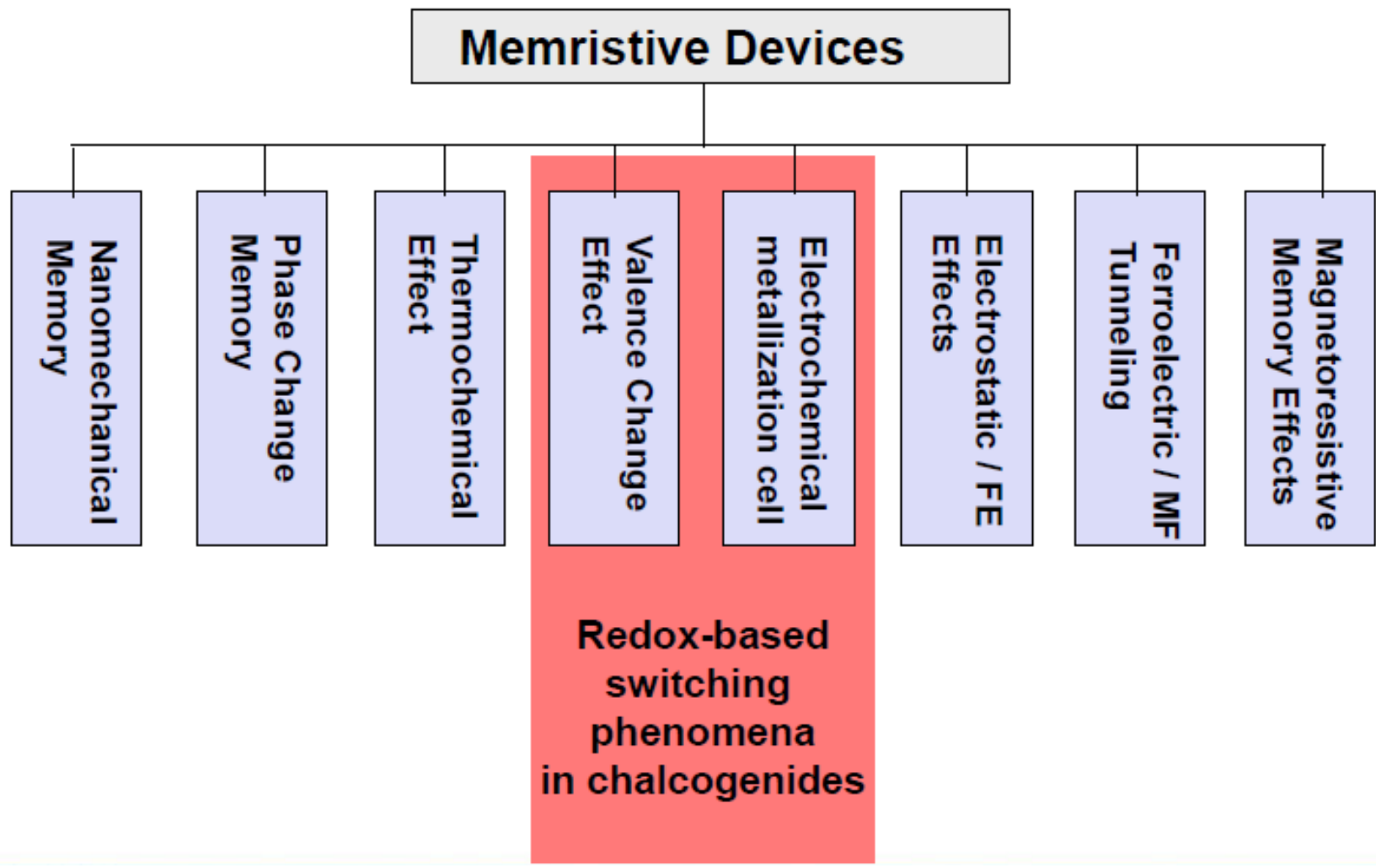
**Recently, "Memristor" and "Memristive Device"
have been used interchangeably**

Ref. L. O. Chua, Memristor-The Missing Circuit Element, IEEE Trans. On Circuit Theory, CT-18 (5):505-517, 1971

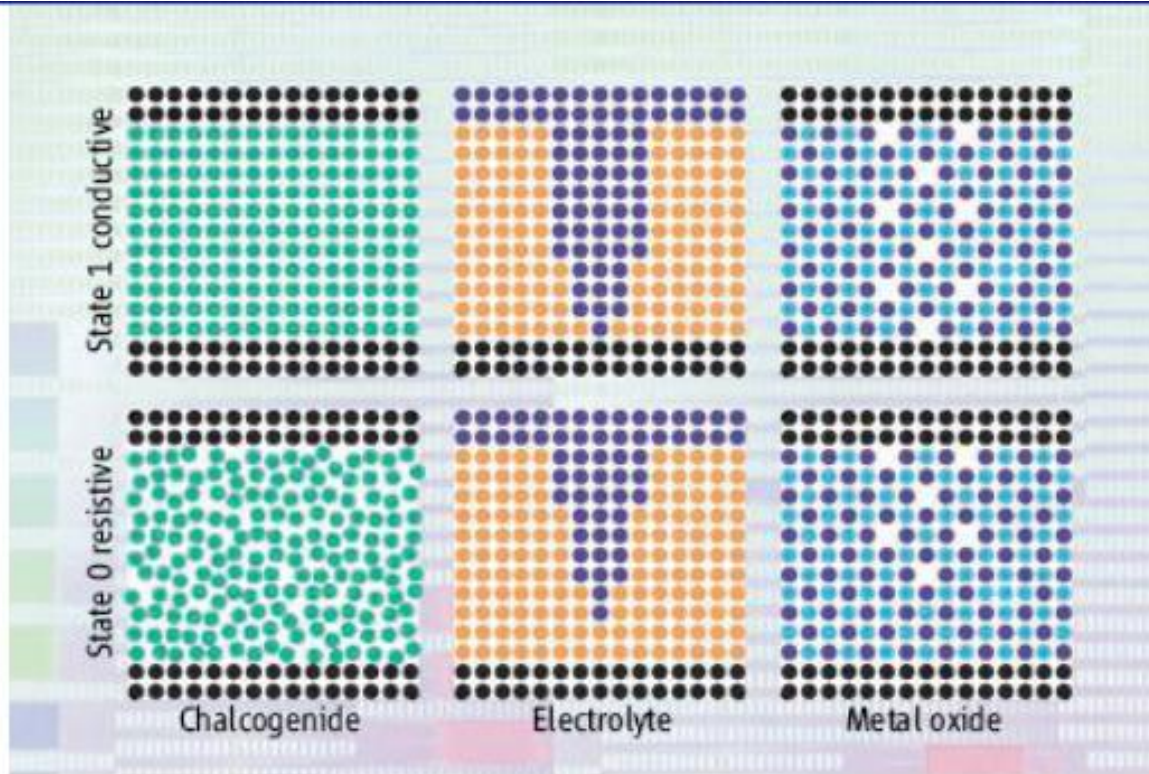
L. O. Chua and S. M. Kang, Memristive Devices and Systems, Proceedings of the IEEE, vol. 64, pp. 209-223, Feb. 1976



Classification of the mechanism of memristor



Resistive switching materials

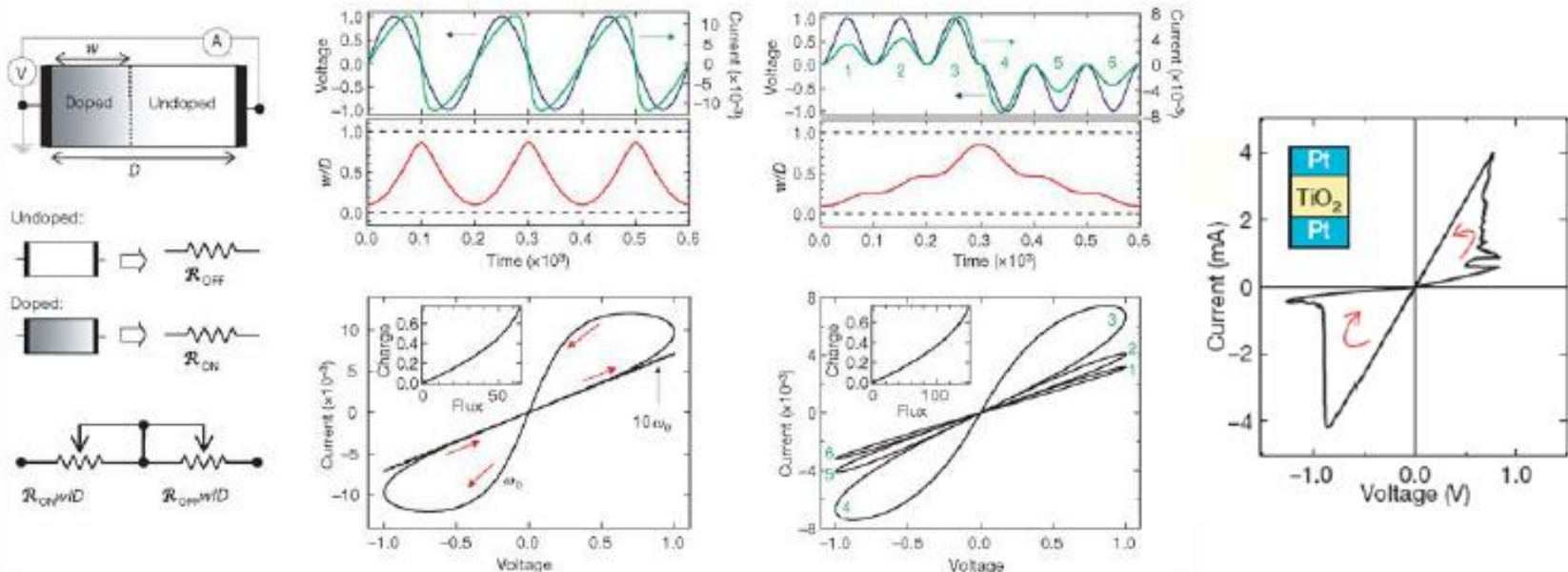


(Left) **Phase change** between a crystalline and an amorphous $\text{Ge}_2\text{Sb}_2\text{Te}_5$ chalcogenide.
=> **Phase-Change RAM (PCRAM)**, on the brink of mass-production

(Middle) Creation and annihilation of a **metallic Ag protrusion** in a GeSe solid electrolyte.

(Right) Creation and disruption of a pattern of **missing oxygen atoms** in a SrTiO_3 transition-metal oxide. => **RRAM (Resistive RAM) or Memristor**, early stage in research

- Nanotechnology Enabled Memristive Devices
 - Typically formed in nano crossbar structures
 - Capable of ultra dense integration
 - Compatible with CMOS process
 - Enables hybrid CMOS/Nanodevices integration



$$V = \left[R_{on} \frac{W}{D} + R_{off} \left(1 - \frac{W}{D} \right) \right] i$$

$$\frac{dw}{dt} = \mu \frac{R_{on}}{D} i$$

with a boundary condition $0 \leq \frac{w}{D} \leq 1$

- A more accurate model should reflect non-constant memristance values when memristor is in high resistance and low resistance modes and their mode switching

Bipolar resistive switching in transition metal oxides

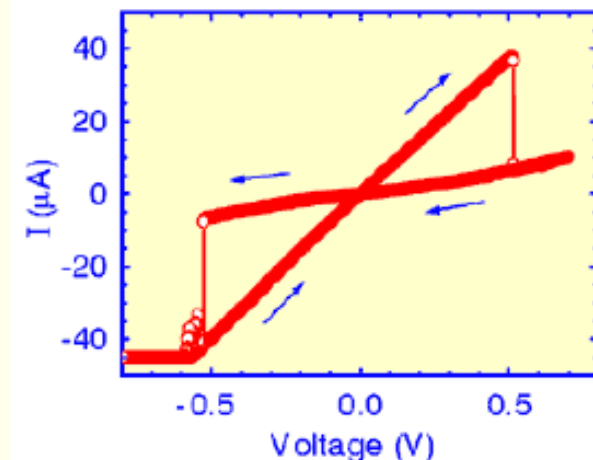
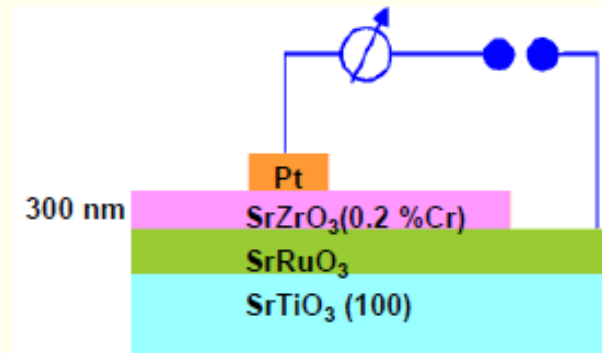


Examples

- Capacitor-like structure with
- ▶ Cr-doped SrZrO_3 thin films
 - ▶ PCMO thin films
 - ▶ $(\text{Ba}, \text{Sr})\text{TiO}_3$ thin films
 - ▶ TiO_2 thin films
 - ▶ SrTiO_3 single crystals as resistive element

Characteristics

after forming process: reversible bipolar switching between stable impedance states



A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel and D. Widmer, *Appl. Phys. Lett.* 77, 139 (2000).



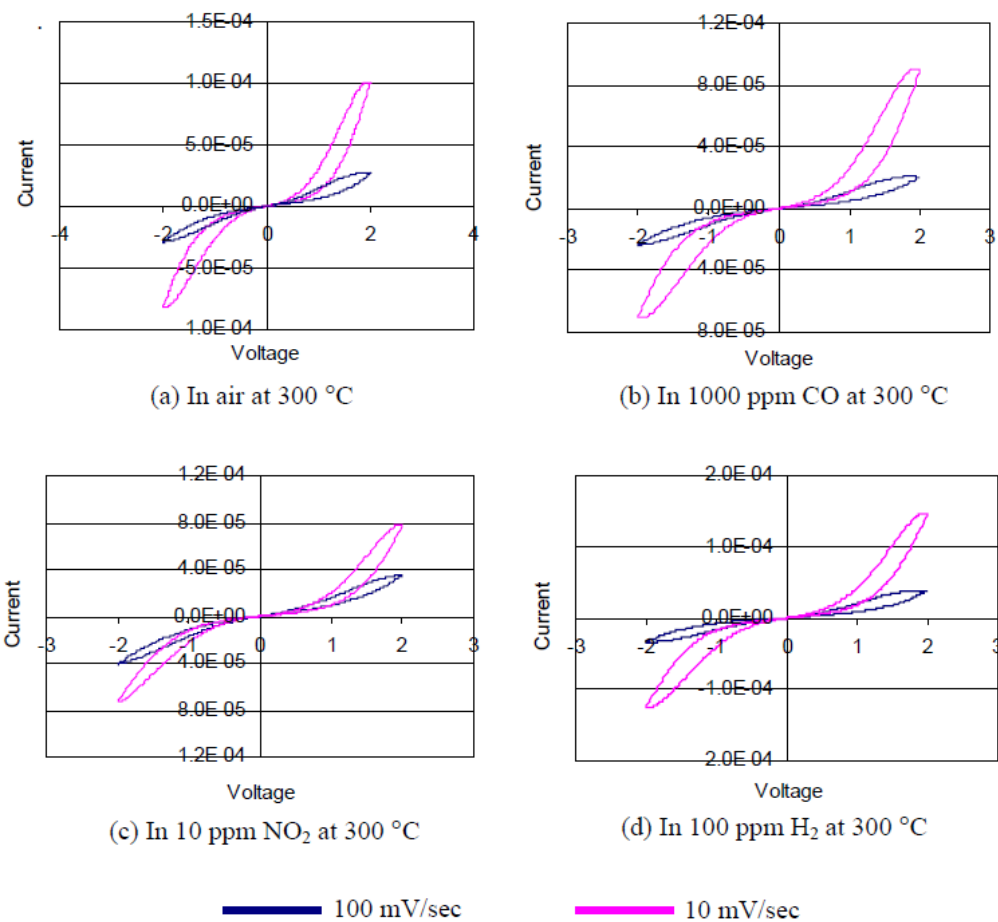
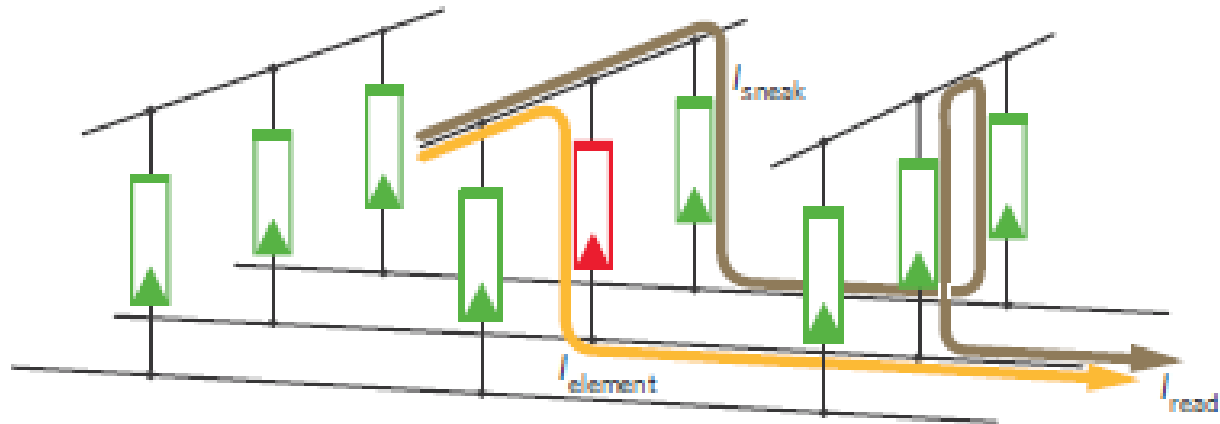


Figure 4.18 Current-voltage (I-V) curves of ZnO (Ar:O₂ = 7:3) micro array sensor measured at 300°C. I-V characteristics were observed from 0V to -2V, 0V, 2V to 0V with different sweep rates of 100 mV/sec and 10 mV/sec.



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Complementary resistive switches for passive nanocrossbar memories

Eike Linn^{1,2}, Roland Rosezin^{2,3}, Carsten Kügeler^{2,3} and Rainer Waser^{1,2,3}★

Memristor memory array (2)

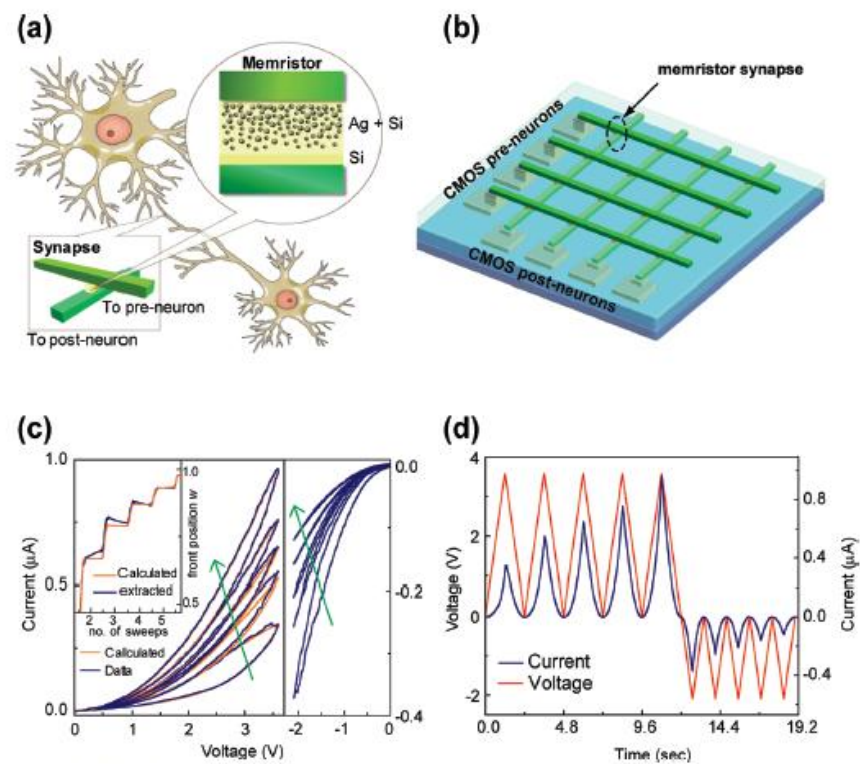


FIGURE 1. Nanoscale memristor characteristics and its application as a synapse. (a) Schematic illustration of the concept of using memristors as synapses between neurons. The insets show the schematics of the two-terminal device geometry and the layered structure of the memristor. (b) Schematic of a neuromorphic with CMOS neurons and memristor synapses in a crossbar configuration. (c) Measured (blue lines) and calculated (orange lines) I - V characteristics of the memristor. Inset: calculated (orange lines) and extracted (blue lines) values of the normalized Ag front position w during positive DC sweeps. (d) The current and voltage data versus time for the device in (c) highlighting the change in current in sequential voltage sweeps.

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Nanoscale Memristor Device as Synapse in Neuromorphic Systems

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Department of Electrical Engineering and Computer Science, University of Michigan, Michigan 48109



Memristor memory array (3)

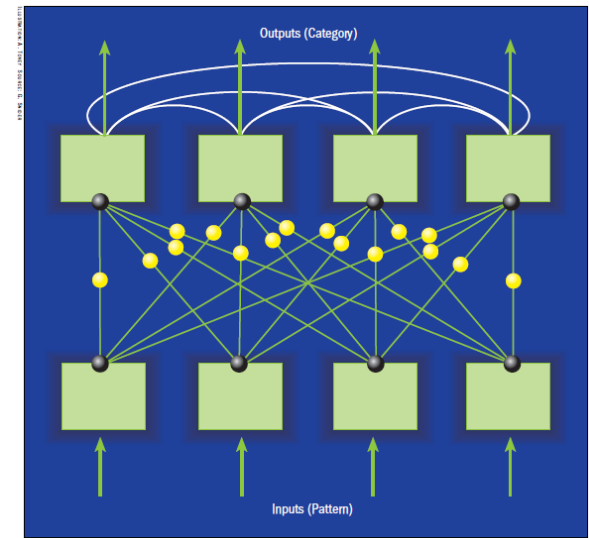


Figure 1. Winner-take-all competitive network.

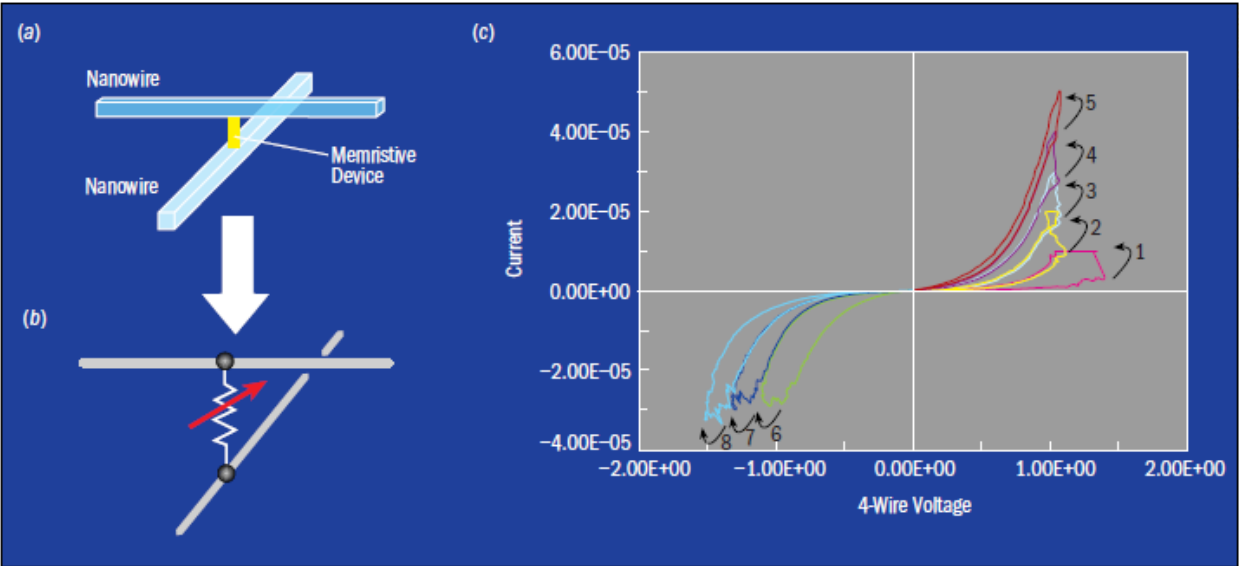


Figure 2. Dynamical behavior of nanojunctions from experiments. Current-voltage curves are numbered sequentially and offset vertically for clarity. Positive voltage sweeps (1–5) are hysteresis loops of increasing conductivity; negative voltage sweeps (6–8) are hysteresis loops of decreasing conductivity.

