A Simple Hybrid 3-Level Buck-Boost DC-DC Converter with Efficient PWM Regulation Scheme

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***Abstract*—This paper describes a 3-level buck-boost converter with an output voltage range up to double the input voltage. The proposed converter can be used for applications that require stepping up/down the input voltage depending on the operating conditions like solar power harvesting. The converter has a hybrid structure between inductor-based converters and capacitor-based converters by utilizing a one flying capacitor and an inductor in the charge transfer process. The converter features smaller inductor size and current ripples as compared to the traditional buck-boost inductor-based converter while offering a high efficiency as compared to SC converters making it suitable for efficient on-chip integration. A prototype circuit has been designed on a 65nm technology using a 5-nH parasitic bondwire inductor. Simulation results show that the proposed converter features up to 20% improvement in the efficiency over a conventional 1:2 SC converter for a wide range of output voltage values.**

I. Introduction

Energy harvesting offers the opportunity to continuously power integrated circuits from the surrounding environment without the need for a battery replacement. However, the harvested power often generates varying low output voltages that are not sufficient to power integrated circuits. Therefore, boost or buck-boost converters are required to provide the desired supply voltages for integrated circuits. Boost (or buck-boost) converters can be realized using two approaches which can be inductor-based or capacitor-based. Inductor-based converters can offer higher power conversion efficiencies but have the disadvantage of utilizing large bulky inductors which cause challenges for on-chip integration. On the other hand, switched capacitor (SC) converters are easily integrable on-chip but suffer from several performance limitations.

SC converters are intrinsically lossy due to the charge sharing losses between the flying capacitors and the output capacitor. These losses are called slow switching limit (SSL) losses [6] and are given by:

$$P_{SSL} = I_L^2 \frac{M}{C_f F_{sw}}, \tag{1}$$

where M is a constant determined by the SC topology, F_{sw} is the switching frequency, C_f is the flying capacitor size and I_L is the load current. Therefore, these losses are a strong function in the switching frequency itself which is the common control parameter used to regulate the output voltage in SC converters.

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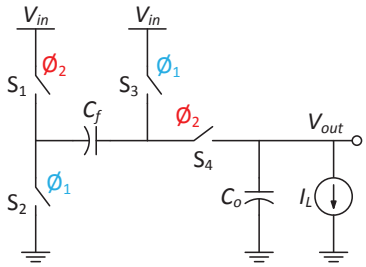

Fig. 1. Conventional switched capacitor 1:2 topology (voltage doubler).

For example, Fig. 1 shows the conventional 1:2 SC converter which has been used as a voltage doubler in many applications [2], [3], [4]. However, this converter lacks the support for efficient regulation of the output voltage. The output voltage is lowered by scaling down the switching frequency. Scaling down the switching frequency would result in additional losses according to (1) making the converter acts more like a linear regulator once deviating from the normal output voltage of the SC topology. Therefore, this regulation scheme of SC converters is considered a lossy regulation scheme. A way to solve this limitation is by using more conversion ratios, but this means adding more capacitors and switches to the SC topology resulting in more complexity and losses.

On the other hand, hybrid DC-DC converters, with both capacitors and inductors involved in the charge transfer process, offer the potential to solve the limitations of the conventional DC-DC converters. Capacitors have been added to inductor-based converters to enhance their performance like the 3-level buck converter [1]. Similarly, small inductors have been added to SC converters to overcome their limitations [5]. In this paper, a hybrid buck-boost DC-DC converter is proposed with an output voltage up to double the input voltage. The structure and the operation of the proposed converter are discussed in Section II. Power loss analysis of the converter is done in Section III. Simulation results are provided in Section IV where the performance of the proposed converter is compared with that of a conventional 1:2 SC converter. Conclusions are provided in Section V.

II. Circuit Structure and Operation

The proposed 3-level buck-boost converter consists of a one flying capacitor and four switches followed by an inductor and an output capacitor as shown in Fig. 2(a). With the help

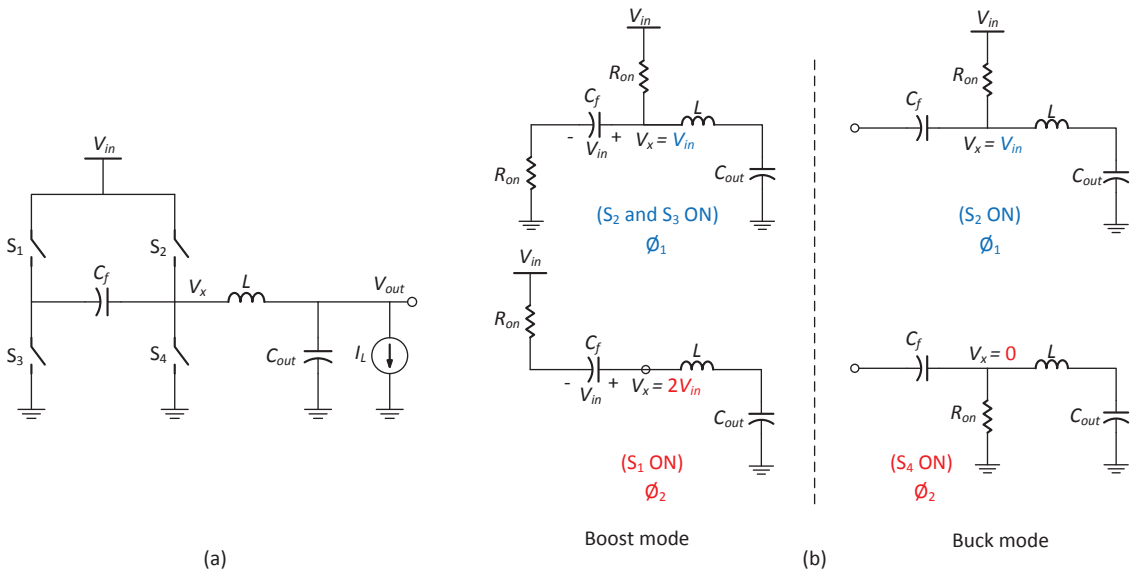

Fig. 2. The proposed 3-level buck-boost DC-DC converter: (a) the full circuit schematic and (b) the equivalent circuits in the two phases of each mode.

of the flying capacitor, three voltage levels can be produced at the inductor input (*i.e.*, V_x node) which are $2V_{in}$, V_{in} and zero. The inductor and the output capacitor work as a Low Pass Filter (LPF) that takes the average of the switching voltage waveform generated at the inductor input and produces a regulated output voltage. The converter can be configured to operate in one of two modes which are the boost-mode and the buck-mode.

In the boost-mode, the converter can theoretically provide an output voltage up to double the input voltage. However, the actual maximum output voltage is slightly below $2V_{in}$ due to the charging/discharging behavior of the flying capacitor and the losses exhibited in the converter. In this mode, there are two phases of operation. In the first phase (pre-charge phase), the flying capacitor is charged to V_{in} by turning on switches S_2 and S_3. In this case, the V_x node at the inductor input is connected to V_{in} as shown in Fig. 2(b). In the second phase (discharge phase), the flying capacitor is connected in series with the input source to produce a voltage level of $2V_{in}$ at the V_x node. Therefore, the V_x node changes its voltage level between V_{in} and $2V_{in}$ periodically when the converter is transitioning between the two phases as shown in Fig. 3(a). The LPF takes the average of this switching voltage waveform and produces a regulated output voltage. In this case, the output voltage is given by:

$$V_{out} = V_{in} + DV_{in} = (1 + D)V_{in}, \tag{2}$$

where D is the duty cycle of the V_x waveform. The output voltage can be tuned between V_{in} and $2V_{in}$ by adjusting the duty cycle which controls the relative duration between the two phases of the boost-mode of the converter.

In the buck-mode, the converter is configured to work as a conventional buck converter, as shown in Fig. 2(b), to produce an output voltage between V_{in} and zero. In this mode, the flying capacitor is left floating by permanently turning off switches S_1 and S_3. The V_x node is connected to either V_{in} or ground by turning on/off switches S_3 and S_4 alternatively like

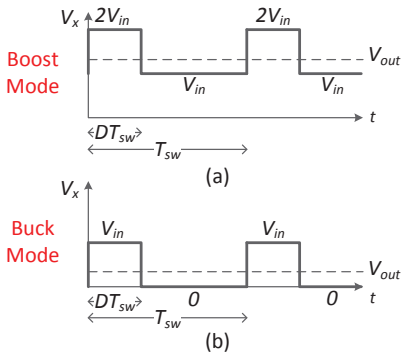

Fig. 3. Conventional switched capacitor 2:1 topology (voltage doubler).

a conventional buck converter. In this case, the output voltage is given by:

$$V_{out} = DV_{in}, \quad 0 < D < 1 \tag{3}$$

Table I summarizes the switch configurations in the two phases of each operation mode. The same circuit shown in Fig. 2(a) can be modified to work as a boost-only converter by removing the switch S2 as shown in Fig. 4.

TABLE I. SWITCH CONFIGURATIONS IN THE TWO PHASES OF EACH MODE

Mode	Phase	S_1	S_2	S_3	S_4	C_f
Boost	ϕ_1	OFF	ON	ON	OFF	↑
	ϕ_2	ON	OFF	OFF	OFF	↓
Buck	ϕ_1	OFF	ON	OFF	OFF	-
	ϕ_2	OFF	OFF	OFF	ON	-

III. CIRCUIT ANALYSIS

In the following part, the losses exhibited in the converter when working in the boost mode are calculated. Due to the charging/discharging behavior of the inductor, some ripples appear in the current flowing in the inductor as shown in Fig.

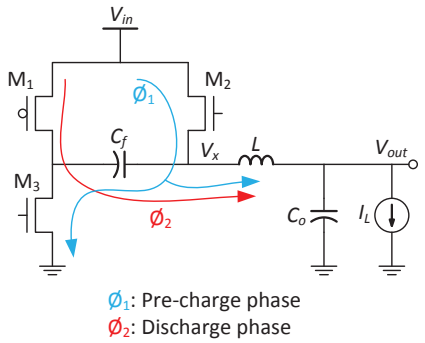

Fig. 4. A three-switches boost-only version of the DC-DC converter showing the two phases of operation.

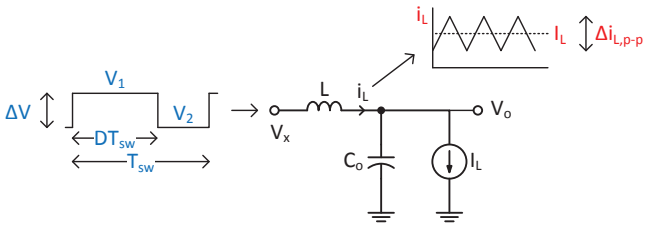

Fig. 5. Current ripples in an inductor due to a switching voltage waveform at its input.

5. These current ripples are a key parameter in determining the performance of the converter in terms of its power conversion efficiency and the output voltage ripples. A general relation for calculating these current ripples is derived here when the input to the inductor is a voltage waveform switching between two voltage levels and the output of the inductor is fixed at a constant voltage (i.e., V_{out}) as shown in Fig. 5. In this case, assuming the converter is operating in the continuous conduction mode (CCM), the peak-to-peak current ripples are given by:

$$\Delta I_{L,p-p} = \frac{\Delta V D(1-D)}{LF_{sw}}, \tag{4}$$

where ΔV is the difference between the two voltage levels of the switching voltage waveform, D is the duty cycle of the switching waveform and F_{sw} is the switching frequency. When the converter is operating in either the buck or the boost mode, the ΔV of the V_x waveform at the inductor input is equal to V_{in} as shown in Fig. 3. Hence, the inductor ripples in each mode is given by:

$$\Delta I_{L,p-p} = \frac{V_{in} D(1-D)}{LF_{sw}}. \tag{5}$$

Fig. 6 shows the normalized peak-to-peak current ripple for the 3-level buck/boost converter versus the voltage conversion ratio. The inductor ripple approaches its maximum at the middle of each operation mode ($i.e.$, when D = 0.5). As the current ripple increases, the RMS value of the current flowing in the parasitic resistances increases and hence the conduction loss of the converter increases. The conduction loss of the converter is given by:

$$P_{Cond} = (I_{L,DC}^2 + \frac{\Delta I_{L,p-p}^2}{12})(R_{on,switches} + R_{ind}), \tag{6}$$

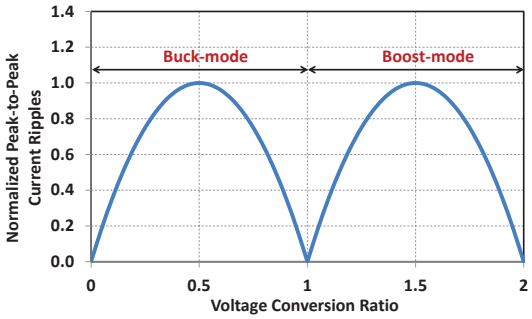

Fig. 6. Normalized peak-to-peak current ripple versus the voltage conversion ratio when operating in the continous conduction mode (CCM).

where $I_{L,DC}$ is the load current drawn by the load circuit, R_{ind} is the parasitic DC Resistance (DCR) of the inductor and $R_{on,switches}$ is the equivalent on-resistance of the MOSFET switches. In the first phase of the boost-mode, a small portion of the current is drawn from the input source to pre-charge the flying capacitor instead of going to the load as shown in Fig. 2(b). However, the conduction losses due to the this pre-charge current can be neglected assuming its value is small as compared to the main load current drawn by the load (I_L).

Increasing the switching frequency of the converter decreases the current ripple and hence the conduction losses but increases the switching losses. The switching loss due to the parasitic gate capacitance of MOSFET switches is given by:

$$P_{SW,Mos} = 3V_{sw}^2 W_{sw} C_{gate} F_{sw} \tag{7}$$

where V_{sw} is the voltage swing on the gate capacitance, C_{gate} is the gate capacitance per unit width (F/m) and W_{sw} is the total width of one switch. Assuming all switches have the same V_{sw} and W_{sw}, the factor of three represents the number of switches changing their states in a one switching period which is equal to three in the boost-mode as shown in table I. The switching loss due to the bottom-plate parasitic capacitance of the flying capacitor is given by:

$$P_{SW,Bott} = K_{bott} V_{in}^2 C_f F_{sw}, \tag{8}$$

where K_{bott} represents the percentage of the bottom-plate parasitic capacitance from the total flying capacitor size. The voltage swing on the bottom-plate capacitance in this topology is equal to V_{in}. The charge sharing losses existent in traditional SC converters are eliminated in this converter due to the existence of an inductor between the flying capacitor and the output capacitor [5]. The total losses exhibited in the converter in the boost-mode are then given by:

$$P_{losses,total} = P_{Cond} + P_{SW,Mos} + P_{SW,Bott} + P_{Others}. \tag{9}$$

Other losses can include the power dissipated in the controller and the driver circuitry of the switches. These losses are a function in the design parameters (e.g. flying capacitor size, switch width, switching frequency) as well as the operating point of the converter (V_{out}, I_L, V_{in}). Therefore, at each operating point of the converter, there are certain design parameters that give the maximum performance of the converter.

TABLE II. CONVERTER SPECIFICATIONS

Technology	TSMC 65nm
Input Voltage (V_{in})	1.2V
Output Voltage (V_o)	0.4V-2V
Inductor	5nH (Bondwire, DCR = 250mΩ)
Flying Capacitor (C_f)	200pF (5% bottom-plate parasitic cap)
Output Capacitor (C_o)	10nF (MOS Cap)
Switching Frequency (F_{sw})	500MHz
Load Current (I_L)	5-10mA

IV. SIMULATION RESULTS AND COMPARISONS

A test circuit of a fully integrated 3-level buck-boost converter has been designed and simulated on a 65nm technology with the specifications shown in Table II. Although the proposed converter utilizes an inductor which introduce challenges for on-chip integration, new techniques have recently appeared in the literature to overcome this problem like inductor realization using the parasitic inductance of the package bond-wires between pins and pads [7]. This technique has an overhead of utilizing two pads and one pin but offers inductors of good quality factors without an additional process complexity or area overhead. In this design, a 5-nH inductor with an DCR of 250mΩ has been used. Fig. 7 shows the power conversion efficiency versus the output voltage at different load currents.

Fig. 8 shows a comparison between the power conversion efficiency of the 3-level buck-boost converter and an optimized switched-capacitor voltage doubler. The SC converter was designed and optimized according to the technique mentioned in [6]. It can be noted that the 3-level buck-boost converter has a better regulation capability as compared to the SC converter, where the efficiency is roughly maintained above 75% over a wide range of output voltage values and load currents. In contrast, the efficiency of the 1:2 SC topology starts to degrade quickly once deviating from the nominal output value (i.e. $2V_{in}$). This phenomena occurred due to the inefficient regulation scheme of SC converters where the output voltage is regulated using the switching frequency instead of the duty cycle. The losses of the SC converter is a strong function in the switching frequency as indicated by (1) where as the switching frequency scales down, the losses increases substantially. On the contrary, the losses of the 3-level does not have that strong dependency on the duty cycle as indicated by (5) and (6). The 1:2 voltage doubler achieves a fairly higher output voltage than the 3-level buck-boost converter as their is a maximum duty cycle the converter can work at due to the required pre-charging time of the flying capacitor in the 3-level buck-boost converter. However, the 3-level buck-boost achieves a higher efficiency especially for lower output voltage values which proves the good regulation capabilities of the 3-level buck-boost converter.

V. CONCLUSION

A 3-level buck-boost DC-DC converter has been proposed where the circuit structure and the working principle are explained. The circuit is capable of providing three different voltage levels at the inductor input allowing the converter to operate in either a boost-mode or a buck-mode. The proposed converter has a better regulation scheme that is based on Pulse Width Modulation (PWM) techniques rather than the switching frequency used in SC converters. Simulation results of the 3-level buck-boost converter show it can offer a better performance as compared to the conventional 1:2 SC converter over a wide range of output voltage values.

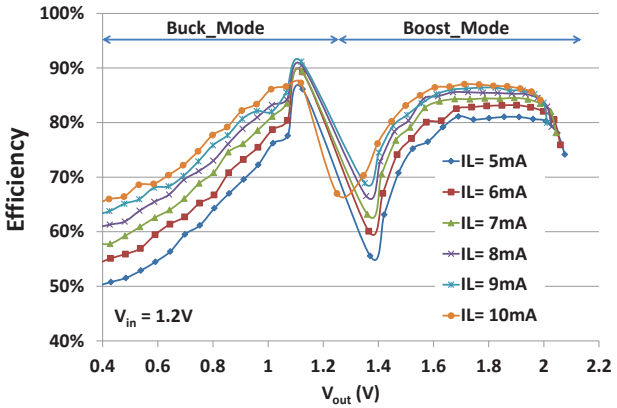

Fig. 7. Power conversion efficiency versus V_{out} for different load currents.

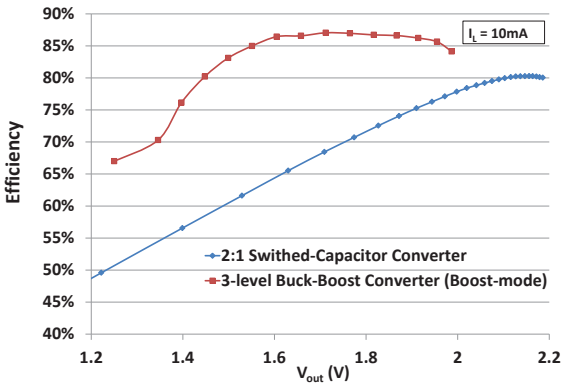

Fig. 8. Comparison between the power conversion efficiency of the 3-level buck-boost converter and an optimized 1:2 SC converter (C_f = 800pF, F_{sw} = 57MHz).

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