Bidirectional Three-Level DC-DC Converters: Sum-Difference Modeling and Control

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***Abstract*—This paper proposes a modeling and control approach for the three-level DC-DC converter. The converter is described in a sum and difference ($\Sigma\Delta$) framework. It is shown that the formulation is useful to model the inverter and derive design-specific equations. The Σ component is responsible for the inductor current, i.e. the power flow, and the Δ component is used to balance (or unbalance) the DC-link capacitor voltages. It is shown that there are cross-coupling terms between the Σ and Δ axes that can be compensated. The proposed model is validated using high fidelity simulations with a proportional-integral controller. Two- and three-level converter operation is shown and it is proven that the passive components can be reduced by 50% to 75% using three-level operation without affecting the control performance. The control is verified by introducing load current and DC voltage steps.**

I. Introduction

Bidirectional non-isolating DC-DC converters are a key technology for electrified transportation systems. They are particularly relevant for vehicles with more-electric drivetrains [1]–[3]. DC-DC converters are used to interface energy storage systems in electric vehicles (EV) and plug-in hybrid electric vehicles (HEV) and energy transformation units in fuel-cell vehicles [4]–[6]. The energy necessary for xEV traction can be provided by one or more electrical energy sources or storage mediums. Non-isolating DC-DC converters are necessary to interface different voltage levels and to control the power flow [7], [8]. An example are EVs with hybrid energy storage systems [9], [10], where a battery pack stores the energy for a suitable driving range and an ultracapacitor pack provides peak power and handles micro-cycling [8].

Numerous converters have been proposed and compared in literature [7], [11]–[13]. DC-DC converters for xEV are typically benchmarked with respect to efficiency. xEVs require a high efficiency over a wide range of operating points that are defined by city and highway driving cycles. A promising solution is the three-level DC-DC converter [14], [15] that is capable of operating at high efficiency over wide load and high voltage transformation ranges. In particular, this converter has been shown to be highly competitive when compared to the two-level and two-level inverterleaved converters [16].

This paper proposes a novel modeling and control approach for the three-level DC-DC converter. The converter is described in a sum and difference ($\Sigma\Delta$) framework. It is shown that the formulation is useful to model the inverter and derive design specific equations. Design equations are given for balanced operation and can be easily extended to unbalanced operation. The results are confirmed by simulation. The converter is operated in both two- and three-level operation. The latter introduces vertical interleaving to reduce passive components. It is proven that the passive components can be reduced by 50% to 75% using three-level operation. The same ratio holds when comparing the 2L DC-DC (conventional buck-boost converter) to the 3L DC-DC converter.

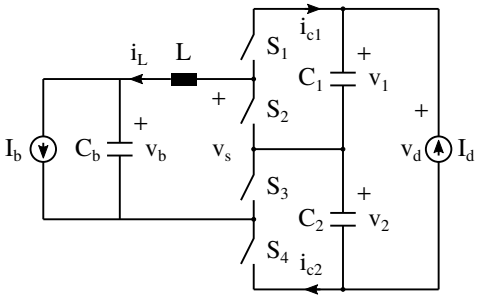

Fig. 1: Three-level DC-DC converter.

The $\Sigma\Delta$ framework is further used for control. It can be used in a fashion similar to the dq framework that is widely employed in motor drives [17]. The Σ component is responsible for current control, i.e. the power flow, whereas the Δ system is used to control the voltage sharing of the DC-link capacitors. It is shown that there are cross-coupling terms between the Σ and Δ axes and that they can be compensated. Compensation is optional and can be taken care of by a sufficiently fast feedback controller. The control is verified by introducing load current and DC voltage steps in high fidelity simulations.

II. Analysis

The bidirectional three-level boost converter has four useful switching states. One of the upper two switches (S_1 and S_2) needs to be off to avoid short-circuiting the voltage $v_1(t)$.

TABLE I: Switching states, capacitor currents and output voltages for the three-level converter.

S_1	S_2	S_3	S_4	$s(t)$	$[i_{c1},i_{c2}]'$	$v_s(t)$
off	on	on	off	$[0,0]'$	$[0,0]'$	0
on	off	on	off	$[1,0]'$	$[-i_L,0]'$	v_1
off	on	off	on	$[0,1]'$	$[0,-i_L]'$	v_2
on	off	off	on	$[1,1]'$	$[-i_L,-i_L]'$	v_1+v_2

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Likewise, one of the lower two switches (S_3 and S_4) needs to be off to avoid short-circuiting the voltage $v_2(t)$. Turning both S_1 and S_2 (or S_3 and S_4) off yields a voltage, $v_s(t)$, that depends on the sign of the current and is ignored in this text. The resulting useful switching states are shown in Table I and Fig. 2.

To simplify the modeling, we introduce the binary switching state $s(t) = [s_1(t),s_2(t)] \in \{0,1\}^2$ and capacitor voltage $v_{12}(t) = [v_1(t),v_2(t)]' \in \mathbb{R}^2_+$, where $v_d(t) = \mathbf{1}'v_{12}(t) = v_1(t) + v_2(t) \in \mathbb{R}_+$. Hence, the voltage that is applied to the inductor is $v_s(t) = v_{12}(t)'s(t) \in \mathbb{R}_+$. In practice, DC-DC converters are typically designed for *Pulse Width Modulation* (PWM). PWM translates a duty cycle $d = [d_1,d_2]' \in [0,1]^2$ into a switching sequence with time average

$$d = \frac{1}{T_{sw}} \int_{kT_{sw}}^{kT_{sw}+T_{sw}} s(t)\ dt, \tag{1}$$

where T_{sw} is the switching period. Similarly, the model can be rewritten using average modeling (neglecting second order components)

$$v_s = v'_{12}d = v_1d_1 + v_2d_2. \tag{2}$$

Furthermore, we introduce the sum and difference notation $d_{\Sigma\Delta} = [d_\Sigma,d_\Delta]' = \mathbf{T}d$ and $v_{\Sigma\Delta} = [v_\Sigma,v_\Delta]' = \mathbf{T}v_{12}$, where

$$\mathbf{T} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \tag{3}$$

and $v_\Sigma = v_d$. The updated notation yields

$$v_s = \left(\mathbf{T}^{-1}v_{\Sigma\Delta}\right)' \left(\mathbf{T}^{-1}d_{\Sigma\Delta}\right) \tag{4a}$$

$$= \frac{1}{2}v'_{\Sigma\Delta}d_{\Sigma\Delta} = \frac{1}{2}\left(v_dd_\Sigma + v_\Delta d_\Delta\right), \tag{4b}$$

and the (discrete-time) dynamic equation of the inductor current

$$i_L^+ = i_L + \frac{T_s}{L}v_s - \frac{T_s}{L}v_b \tag{5a}$$

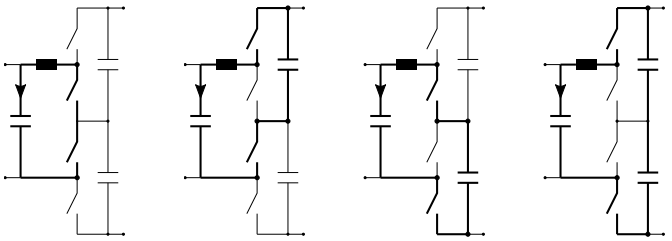
$$= i_L + \frac{T_s}{2L}\left(v_dd_\Sigma + v_\Delta d_\Delta\right) - \frac{T_s}{L}v_b, \tag{5b}$$

where the sampling period $T_s = T_{sw}$ for simplicity and $.^+$ denotes entities of the (discrete) sampling time instant $t + T_s$. The voltages on capacitors C_1 and C_2 vary as a function of the inductor current and duty cycle, per

$$v_{12}^+ = v_{12} - \frac{T_s}{C}i_Ld + \frac{T_s}{C}I_d, \tag{6}$$

where we assume $C_1 = C_2 = C$ for simplicity and I_d is the constant DC current. This equation states that $d_1 > 0$ and $d_2 > 0$ discharges the capacitors C_1 and C_2 with current i_L, respectively. The duty cycles $d_1 = 0$ and $d_2 = 0$ bypass i_L and do not affect the capacitor voltage. The equation is rewritten using the sum and difference notation as

$$v_{\Sigma\Delta}^+ = v_{\Sigma\Delta} - \frac{T_s}{C}i_Ld_{\Sigma\Delta} + \left[\frac{2T_s}{C}I_d,0\right]'. \tag{7}$$



(a) $s = [0,0]'$ (b) $s = [1,0]'$ (c) $s = [0,1]'$ (d) $s = [1,1]'$

Fig. 2: Conduction paths as a function of the switching state $s(t)$.

Adding the dynamic equation of the capacitor C_b, we obtain the full dynamics of the system in scalar notation:

$$i_L^+ = i_L + \frac{T_s}{2L}(v_dd_\Sigma + v_\Delta d_\Delta) - \frac{T_s}{L}v_b, \tag{8a}$$

$$v_\Delta^+ = v_\Delta - \frac{T_s}{C}i_Ld_\Delta, \tag{8b}$$

$$v_d^+ = v_d - \frac{T_s}{C}i_Ld_\Sigma + \frac{2T_s}{C}I_d, \tag{8c}$$

$$v_b^+ = v_b + \frac{T_s}{C_b}i_L - \frac{T_s}{C_b}I_b; \tag{8d}$$

or, in matrix form,

$$x^+ = \mathbf{A}x + \mathbf{B}(x)u + e, \tag{9}$$

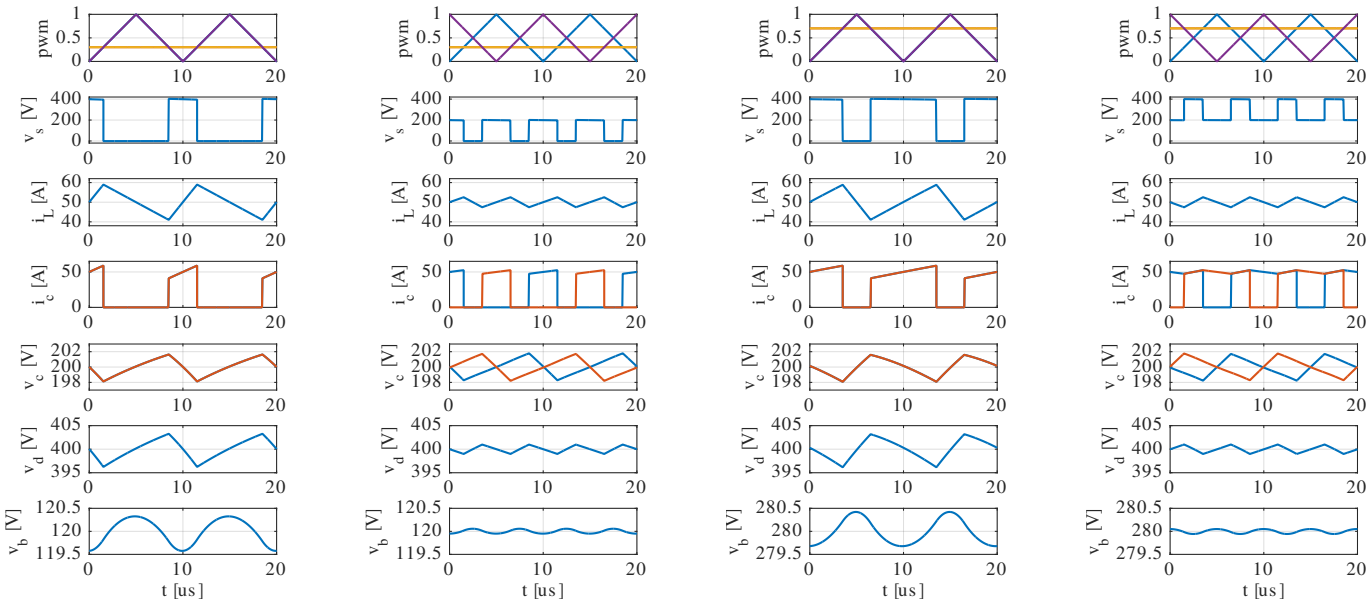
where $x = [i_L,v_\Delta,v_d,v_b]'$ is the state vector, $u = d_{\Sigma\Delta}$ is the input and e is the exogenous input. Their parameters are

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & 0 & \frac{-T_s}{L} \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ \frac{T_s}{C_b} & 0 & 0 & 1 \end{bmatrix}, \mathbf{B}(x) = \begin{bmatrix} \frac{T_s}{2L}v_d & \frac{T_s}{2L}v_\Delta \\ 0 & \frac{-T_s}{C}i_L \\ \frac{-T_s}{C}i_L & 0 \\ 0 & 0 \end{bmatrix}, e = \begin{bmatrix} 0 \\ 0 \\ \frac{2T_s}{C}I_d \\ \frac{-T_s}{C_b}I_b \end{bmatrix}.$$

The system (9) has a constant state parameter matrix and is affine in the input with a state-dependent parameter matrix.

The state-space system (8) defines the following control problems that need to be addressed to operate the three-level DC-DC converter

- *Power flow:* the converter transfers the power $p = v_bi_L$. Controlling the power translates into controlling i_L since v_b is approximately constant (by design or control).
- *Symmetric operation:* Converters are typically implemented with one type of semiconductor and capacitor. To minimize component stresses, the capacitor voltages should be symmetrical, which can be achieved by controlling v_Δ to zero.
- *Voltage stabilization:* Either v_b or v_{12} can be controlled via the power flow through the converter. The other voltage needs to be stabilized via the exogenous input (I_b or I_c) since the converter cannot store significant amounts of energy. Stabilization can be achieved through connection to a DC bus or energy storage system (battery or ultracapacitor).



(a) No interleaving, $d_1 = 0.3$. (b) Interleaving, $d_1 = 0.3$. (c) No interleaving, $d_1 = 0.7$. (d) Interleaving, $d_1 = 0.7$.

Fig. 3: High fidelity simulations, with and without interleaving, for $C_1 = C_2 = C_b = 30\mu$F, $L = 47\mu$H and $f_{sw} = 100$kHz.

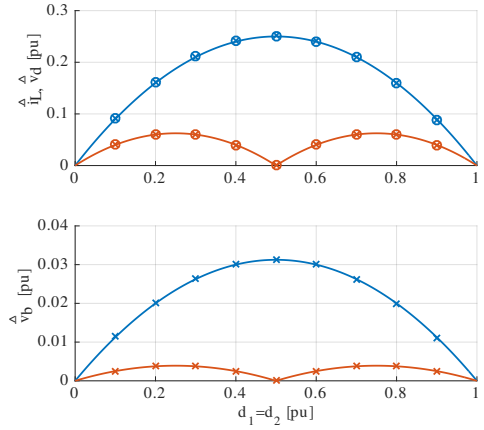


Fig. 4: Normalized current and voltage ripples. Continuous line: analytic functions (12), (13), (15), (16), (18) and (19); markers: current (○) and voltage (×) ripples obtained from high fidelity simulation with $C_1 = C_2 = C_b = 30\mu$F, $L = 47\mu$H and $f_{sw} = 100$kHz.

III. Modulation

The upper bridge (switches S_1 and S_2) is actuated by the duty cycle d_1 and the lower bridge (S_3 and S_4) by d_2 using dedicated PWM modules. Both bridges can be operated independently from one another and two modulation strategies are analyzed: two-level (2L) and three-level (3L) switching. The PWM carrier signals of the upper and lower bridge are in phase for 2L switching and phase shifted by 180° ($T_{sw}/2$) in 3L switching. Three-level switching can be interpreted as a vertical *interleaving* of the two bridges. Interleaving is generally considered to reduce current (voltage) ripples compared to 2L switching. An example is shown in Fig.3.

The switching ripples are analyzed in steady state conditions. Substituting $i_L^+ = i_L$ and $v_\Delta^+ = v_\Delta$ in (28) yields $v_s = v_b$ and $i_\Delta = 0$, i.e. $d_\Delta = 0$, and $d_1 = d_2 = d_\Sigma/2 = v_b/v_d$. We also assume symmetric operation, where $v_\Delta = 0$ and $v_1 = v_2 = v_d/2$. This operation yields symmetric voltage and current stresses on the upper and lower bridge and it can be shown that it yields minimum ripples. In these conditions, it can be shown that the (constant) input/output currents are $I_c = d_1 i_L$ and $I_b = i_L$.

Both 2L and 3L switching yield a characteristic switching pattern in the steady state that can be observed in Fig. 3. Two-level switching only applies the switching states $s(t) = [0,0]'$ and $s(t) = [1,1]'$ such that $v_s(t)$ switches between two voltage levels: $0V$ and v_d. In contrast, 3L switching applies all four switching states and $v_s(t) \in \{0V, v_d/2, v_d\}$. Dependent on the duty cycle, v_s switches between $0V$ and $v_d/2$ or $v_d/2$ and v_d. In addition, 3L switching effectively doubles the switching frequency for the passive components.

To quantify the effects of switching, we formally define the switching ripple as the peak-to-peak amplitude over T_{sw} in steady state conditions. The switching ripple of inductor current is defined as

$$\hat{i}_L = \max i_L(t) - \min i_L(t) \quad \forall t \in [kT_{sw}, (k+1)T_{sw}], \quad (10)$$

and the switching ripple of v_s and v_b are defined analogously. Switching ripples are calculated using the discrete version of the characteristic inductor and capacitor equations. The inductor current ripple results from

$$L\frac{\hat{i}_L}{\hat{T}} = |\hat{v}_L|, \quad (11)$$

where the voltage $\hat{v}_L$ is assumed to be approximately constant and applied for the period $\hat{T}$. For 2L switching, the normalized current ripple is

$$\hat{i}_{L,2L}(d_1) = \frac{L}{T_{sw} v_d} \hat{i}_L = d_1(1-d_1) \tag{12}$$

when considering the off period where $|\hat{v}_L| = v_b = d_1 v_d$ is applied for $\hat{T} = (1-d_1)T_{sw}$. With interleaving, the current ripple depends on the value of d_1 as follows:

$$\hat{i}_{L,3L}(d_1) = \begin{cases} |0.5 - d_1| d_1, & \text{if } 0 \le d_1 \le 0.5; \\ |0.5 - d_1|(1-d_1), & \text{if } 0.5 < d_1 \le 1. \end{cases} \tag{13}$$

For $d_1 \le 0.5$ the voltage $|\hat{v}_L| = d_1 v_d$ is applied during the off interval $|0.5 - d_1|T_{sw}$; for $d_1 \ge 0.5$, the voltage $|\hat{v}_L| = v_d - v_b = (1-d_1)v_d$ is applied during the on interval $|0.5-d_1|T_{sw}$.

The v_d voltage ripple is computed similar to $\hat{i}_L$. The treatment is based on the equation

$$\frac{C}{2} \frac{\hat{v}_d}{\hat{T}} = |\hat{i}_d|, \tag{14}$$

where $\hat{v}_d$ is the voltage ripple, $\hat{i}_d$ is the capacitor current that is assumed to be approximately constant over the period $\hat{T}$ that it is applied, and $C/2$ is the resulting capacitance of the series connected C_1 and C_2. Without interleaving, the normalized voltage ripple is

$$\hat{\hat{v}}_{d,2L}(d_1) = \frac{C}{2T_{sw} I_{LR}} \hat{v}_d = d_1(1-d_1) \tag{15}$$

when considering the off period where $|\hat{i}_d| = |I_b| = d_1 I_{LR}$ is applied for $\hat{T} = (1-d_1)T_{sw}$. The ripple is computed using the rated (average) inductor current I_{LR}, which yields the worst-case ripple. With interleaving, the voltage ripple is

$$\hat{\hat{v}}_{d,3L}(d_1) = \begin{cases} |0.5 - d_1| d_1, & \text{if } 0 \le d_1 \le 0.5; \\ |0.5 - d_1|(1-d_1), & \text{if } 0.5 < d_1 \le 1. \end{cases} \tag{16}$$

For $d_1 \le 0.5$ the current $|\hat{i}_c| = |I_b| = d_1 I_{LR}$ is applied during the off interval $|0.5 - d_1|T_{sw}$; for $d_1 \le 0.5$, the current $|\hat{i}_c| = I_{LR} - |I_b| = (1-d_1)I_{LR}$ is applied during the on interval $|0.5 - d_1|T_s$.

The computation of thevoltage ripple of v_b is based on the assumption that the inductor current ripple circulates in the capacitor. The charge, which varies with v_d, is obtained by integrating the triangular inductor current ripple in the positive half-period and is calculated as

$$\hat{Q}_b = C_b \hat{v}_b = \frac{1}{2} \frac{\hat{i}_L}{2} \hat{T}, \tag{17}$$

where $\hat{T}$ is the duration of the half-period. Without interleaving, we obtain the normalized voltage ripple

$$\hat{\hat{v}}_{b,2L}(d_1) = \frac{LC_b}{T_{sw}^2 v_d} \hat{v}_b = \frac{1}{8} \hat{i}_{L,2L}(d_1) = \frac{1}{8} d_1(1-d_1), \tag{18}$$

where $\hat{T} = T_{sw}/2$. With interleaving, $\hat{T} = T_{sw}/4$ and we obtain

$$\hat{\hat{v}}_{b,3L}(d_1) = \frac{\hat{i}_{L,3L}(d_1)}{16}. \tag{19}$$

The normalized switching ripple is provided by (12), (13), (15), (16), (18) and (19) and shown in Fig. 4 as continuous lines. The analytic equations are validated using a high fidelity MATLAB/Simulink model with Simscape/SPICE components applying (10) to the steady state waveforms for $d = 0.1, 0.2, \ldots, 0.9$. The results are shown in Fig. 4 as markers with current being circles ($\circ$) and voltages crosses ($\times$).

IV. Design

The switching ripples of the presented boost converter depend on the modulation technique. Three-level switching significantly reduces the current and voltage switching ripples compared to 2L switching. Hence, 3L switching can be used to reduce the passive components. This section presents design equations for 2L and 3L switching.

The maximum normalized ripple is obtained by deriving the analytic expression and setting it to zero. Using the 2L inductor current ripple as an example, we have

$$\frac{d}{d\, d_1} \left(\hat{\hat{i}}_{L,2L}(d_1) \right) = 1 - 2d_1 = 0 \;\Leftrightarrow\; d_{1,2L\max} = 0.5. \tag{20}$$

In the same fashion, $d_{1,3L\max} = 0.25$ for 3L switching. The same duty cycles are obtained for the maximum voltage ripples. The maximum 2L normalized ripples are obtained by substituting the duty cycles in (12), (15) and (18):

$$\hat{\hat{i}}_{L,2L\max} = \hat{\hat{v}}_{d,2L\max} = 250 \cdot 10^{-3}, \tag{21a}$$

$$\hat{\hat{v}}_{b,2L\max} = 31.2 \cdot 10^{-3}. \tag{21b}$$

The maximum 3L normalized ripples are obtained by substituting the duty cycles in (13), (16) and (19):

$$\hat{\hat{i}}_{L,3L\max} = \hat{\hat{v}}_{d,3L\max} = 62.5 \times 10^{-3}, \tag{22a}$$

$$\hat{\hat{v}}_{b,3L\max} = 3.9 \times 10^{-3}. \tag{22b}$$

Once the maximum normalized ripples are known, the design equations result directly from (12), (15) and (18). Transforming these equations, we obtain

$$L = \hat{\hat{i}}_{L,\max} \frac{v_d}{f_{sw} \hat{i}_{L\max}} \tag{23a}$$

$$C_1 = C_2 = C = \hat{\hat{v}}_{d,\max} \frac{2I_{LR}}{f_{sw} \hat{v}_{d\max}} \tag{23b}$$

$$C_b = \hat{\hat{v}}_{b,\max} \frac{v_d}{f_{sw}^2 L \hat{v}_{b\max}} \tag{23c}$$

where $f_{sw} = 1/T_{sw}$ is the switching frequency. The normalized ripples $\hat{\hat{i}}_{L,\max}$, $\hat{\hat{v}}_{d,\max}$ and $\hat{\hat{v}}_{b,\max}$ are either the normalized 2L switching ripples specified in (21) or the normalized 3L switching ripples specified in (22). The maximum peak-to-peak current ripple, $\hat{i}_{L,\max}$ is often chosen as 40% of I_{LR}. The maximum peak-to-peak voltage ripples $\hat{v}_{d,\max}$ and $\hat{v}_{b,\max}$ are typically specified design requirements.

The required inductance and capacitance values can be put into relation for a 2L and 3L design that use the same voltages (v_d and v_b), current (I_{LR}), inductor current ripple ($\hat{i}_{L,\max}$)

and switching frequency (f_{sw}). The inductance L ratio and capacitance C ratio is

$$\frac{L_{3L}}{L_{2L}} = \frac{\hat{\dot{i}}_{L,3Lmax}}{\hat{\dot{i}}_{L,2Lmax}} = \frac{C_{3L}}{C_{2L}} = \frac{\hat{v}_{d,3Lmax}}{\hat{v}_{d2L,max}} = \frac{1}{4} \tag{24}$$

and the capacitance C_b ratio is

$$\frac{C_{b,3L}}{C_{b,2L}} = \frac{\hat{v}_{b,3Lmax}}{\hat{v}_{b2L,max}} \frac{\hat{\dot{i}}_{L,2Lmax}}{\hat{\dot{i}}_{L3L,max}} = \frac{1}{2}. \tag{25}$$

Hence, 2L switching requires 4 times the inductance L and capacitance C compared to 3L switching. Although the inductance current ripple is the same, 3L switching requires half the capacitance C_b since the frequency of the current ripple is $2f_{sw}$ compared to just f_{sw} for 2L switching.

The impact of the filter parameter on volume can be estimated using scaling laws [18]. The inductor volume scales approximately according to

$$\frac{Y_L}{Y_L^*} = \left(\frac{E_L}{E_L^*}\right)^{\frac{3}{4}} = \left(\frac{0.5LI^2}{0.5L^*I^2}\right)^{\frac{3}{4}} = \left(\frac{L}{L^*}\right)^{\frac{3}{4}}, \tag{26}$$

where Y_L and E_L are the inductor volume and energy, respectively. The variables with superscript $.^*$ belong to a reference device using the same technology. The capacitor volume scales approximately according to

$$\frac{Y_C}{Y_C^*} = \frac{E_C}{E_C^*} = \frac{0.5CV^2}{0.5C^*V^2} = \frac{C}{C^*} \tag{27}$$

where Y_C and E_C are the capacitor volume and energy, respectively. Since the inductor (capacitor) works with the same current (voltage), the volume ratio can be computed based on the parameter values. Therefore, the inductor L volume can be reduced by a factor of about 2.8 using 3L switching compared to 2L switching. Similarly, the volume of C and C_b can be reduced by a factor of 4 and 2, respectively.

A 2L switching-based converter is compared to a (vertically interleaved) 3L switching-based converter with a reference design for each case. The design specifications and results are shown in Table II.

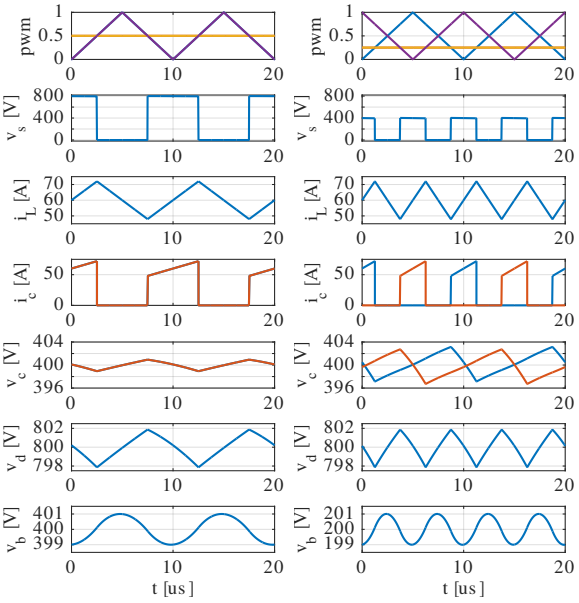
V. Control

A simple control approach is obtained by assuming that the DC voltages, v_d and v_b, are effectively constant with respect to sampling instants (controlled externally or due to a connected energy storage system). This assumption can be relaxed such that only one voltage is constant using a(n) (outer) voltage control loop. Ignoring (8c) and (8d), the state-space model is

$$i_L^+ = i_L + \frac{T_s}{L} v_s - \frac{T_s}{L} v_b, \tag{28a}$$

$$v_\Delta^+ = v_\Delta + \frac{T_s}{C} i_\Delta, \tag{28b}$$

where v_s is used to steer i_L and $i_\Delta = -i_L d_\Delta$ steers v_Δ. The dynamic equations are independent from one another and can be analyzed using common SISO tools, such as Bode plots.



(a) 2L. (b) 3L.

Fig. 5: Reference design (Table II) validation for worst-case duty cycles: $d = 0.5$ for 2L and $d = 0.25$ for 3L.

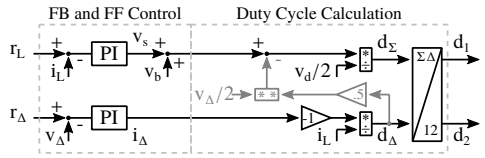
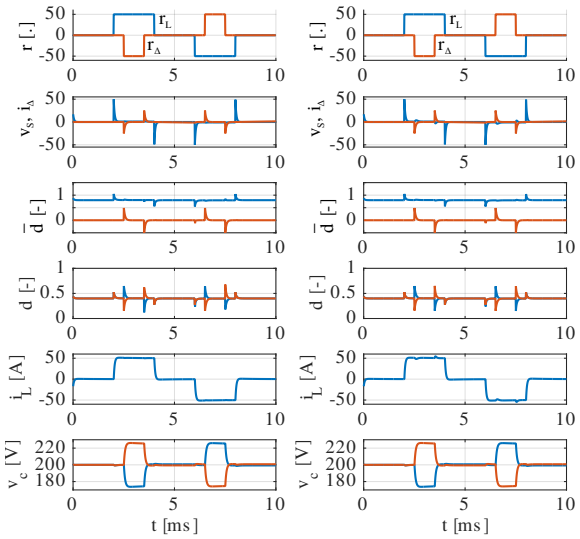


Fig. 6: Control block diagram with feedback (FB) and feedforward (FF) control and duty cycle calculation. The compensation of $v_\Delta d_\Delta/2$ (grey blocks) can be typically omitted.

TABLE II: Two- and three-level converter design.

Design Specification		
Voltage range v_d	400V . . . 800V	
Voltage range v_b	200V . . . 400V	
Rated current I_{LR}	60A	
Ripple amplitude $\hat{v}_{dmax}$	$1\% v_{dmin} = 4$V	
Ripple amplitude $\hat{v}_{bmax}$	$1\% v_{bmin} = 2$V	
Ripple amplitude $\hat{i}_{Lmax}$	$40\% I_{LR} = 24$A	
Switching frequency f_{sw}	100kHz	
Passive Design	**2L**	**3L**
Inductance L	83.3μH	20.8μH
Capacitance C	75.0μF	18.8μF
Capacitance C_b	15.0μF	7.5μF
Inductance ratio L_{3L}/L_{2L}	25.0%	
Capacitor ratio C_{3L}/C_{2L}	25.0%	
Capacitor ratio Cb_{3L}/Cb_{2L}	50.0%	
Estimated Volume Reduction		
Inductor volume ratio Y_{L3L}/Y_{L2L}	35.4%	
Capacitor volume ratio Y_{C3L}/Y_{C2L}	25.0%	
Capacitor volume ratio Y_{Cb3L}/Y_{Cb2L}	50.0%	



(a) With compensation of $\frac{v_\Delta d_\Delta}{2}$. (b) Without compensation.

Fig. 7: Control evaluation for $C_1 = C_2 = C_b = 30\mu$F, $L = 47\mu$H, $f_{sw} = 100$kHz, with inductor current reference r_L and difference voltage reference r_Δ.

The discrete-time transfer functions are

$$\mathrm{tf}_1(z) = \frac{i_L}{v_s} = \frac{T_s}{L}\frac{1}{z-1}; \quad \mathrm{tf}_2(z) = \frac{v_\Delta}{i_\Delta} = \frac{T_s}{C}\frac{1}{z-1}. \quad (29)$$

Power electronic systems are typically controlled using proportional-integral (PI) feedback (FB) control thanks to its simplicity of design and implementation. The PI controllers issue a v_s and i_Δ value. The integral action is used to avoid control biases, for example, due to actuation uncertainties (interlock times and on-voltage drop). However, the effect of v_b is large and may yield unacceptable transients, e.g. at startup. Hence, a feedforward term is added that compensates the effect of v_b as shown in the block diagram in Fig. 6.

The resulting control inputs $v_s + v_b$ and i_Δ cannot be actuated directly by PWM to the plant and need to be transformed into duty cycles. In the $\Sigma\Delta$ framework, we have

$$d_\Sigma = \frac{v_s + v_b - v_\Delta d_\Delta/2}{v_d/2}, \quad d_\Delta = -\frac{i_\Delta}{i_L}. \quad (30)$$

The resulting scheme (with grey blocks) is shown in Fig. 6. However, the term v_Δ is typically controlled to zero to ensure symmetric operation (equivalent voltage stress and losses on C_1, C_2 and the switches, etc.). If $v_\Delta \approx 0$, the effect of $v_\Delta d_\Delta/2$ is small and the computation can be simplified to

$$d_\Sigma = \frac{v_s + v_b}{v_d/2}, \quad d_\Delta = -\frac{i_\Delta}{i_L}. \quad (31)$$

Hence, the grey blocks in the block diagram in Fig. 6 can typically be omitted. To apply the duty cycles with PWM to the plant, $d_{\Sigma\Delta}$ is transformed into $d_{12} = \mathbf{T}^{-1} d_{\Sigma\Delta}$; or,

$$d_1 = \frac{d_\Sigma + d_\Delta}{2}, \quad d_2 = \frac{d_\Sigma - d_\Delta}{2}. \quad (32)$$

It is noted that the term i_L can be positive, negative or zero. If $i_L = 0$, v_Δ is constant and not controllable. Hence, the computation of d_Δ in (30)–or, (31)–has to be protected against division by zero. The control is shown in Fig. 7 using synchronous sampling.

VI. Conclusions

This paper presented a $\Sigma\Delta$ formulation of the three-level DC-DC converter. Three-level operation is shown to reduce switching ripples by 50% to 75%. Alternatively, the passive components can be reduced by the same amount to achieve a required switching ripple under the same operating conditions. The control can also be implemented in this framework and has been demonstrated with a proportional-integral controller.

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