Universidad Nacional Autónoma de México

Facultad de Ingeniería

T E S I S

QUE PARA OBTENER EL TÍTULO DE:

Ingeniero en Computación

P R E S E N T A :

Luis Esteban Serrano Bermúdez

TUTOR

Dr. ... Tutor

Ciudad Universitaria, Cd. Mx., 2020

Dedicatoria ...

Agradecimientos

Resumen

Índice general

Índice de figuras

Índice de tablas

Prólogo

Este proyecto se ha desarrollado con la finalidad de añadir una mejora a los medidores de energía previamente realizados en el Instituto de Ingeniería de la UNAM. La finalidad de esta mejora es agregar una función de lectura de datos de registros del medidor de energía ADE7880 para poder analizar una gran cantidad de datos en poco tiempo.

Capítulo 1

Introducción

1.1. Computadora

Una computadora esta conformada por hardware y software. La parte de Hardware consta de 4 componentes: el procesador, que funciona como el cerebro; la unidad de entrada, por la cual los programas y los datos son ingresados; la unidad de salida por donde son presentados los los resultados y la memoria que es en donde se almacena el software y los datos.

1.1.1. Procesador

El procesador, tambien llamada como la Unidad Central de Procesamiento se puede clasificar en tres partes:

- **Registros:** Es una locación de almacenamiento dentro de la CPU en la cual se mantienem los datos y las direcciones de memoria durante la ejecución de una instrucción. Accesar a los registros de datos es más rápido que acceder a los datos en la memoria externa. Estos registros varían dependiendo del modelo del procesador.

- **Unidad Lógica Aritmética:** Es la calculadora numérica y evaluadora lógica de operaciones. Aquí se reciben los datos provenientes de la memoria principal o de los registros, realiza una operación lógica y si es necesario reescribe el resultado de vuelta al registro o memoria.

- **Unidad de Control:** Contiene las instrucciones lógicas del hardware, esta se encarga de decodificar y monitorear la ejecución de las instrucciones. Tambien funciona como árbitro de varios de los servicios del CPU, los cuiales se encuentran sincronizados por un reloj de sistema.

1.1.2. Arquitecturas de Procesadores

Arquitectura Harvard

El término de Arquitectura Harvard se le conoce a aquellas configuraciones donde las instrucciones y los datos de entrada/salida se almacenan por separado en 2 memorias, este término se le conoce por la primer computadora digital automática el "*Harvard Mark I*"(1944) diseñado por IBM y la Universidad de Harvard[Cuéllar, 2008].

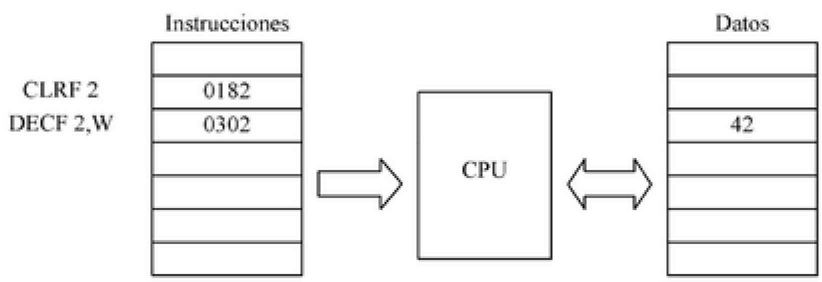


Figura 1.1: Arquietctura Harvard

La arquitectura Harvard duplica efectivamente el espacio accesible de memoria y la velocidad teórica de ejecución, ya que el procesador puede realizar las operaciones de lectura y escritura sobre los 2 buses a la vez y leer datos e instrucciones en el mismo ciclo[Caprile, 2012].

Arquitectura Von Neumann

Esta arquitectura usa la misma memoria para instrucciones como para datos, es decir, utiliza una memoria de lectura/escritura para estoa procesos. En esta arquitectura no hay diferencia entre datos e instrucciones, todos son números y solo depende del uso que se le asigne. Esto ha permitido el desarrollo de procesaores simples y relativamente eficientes.

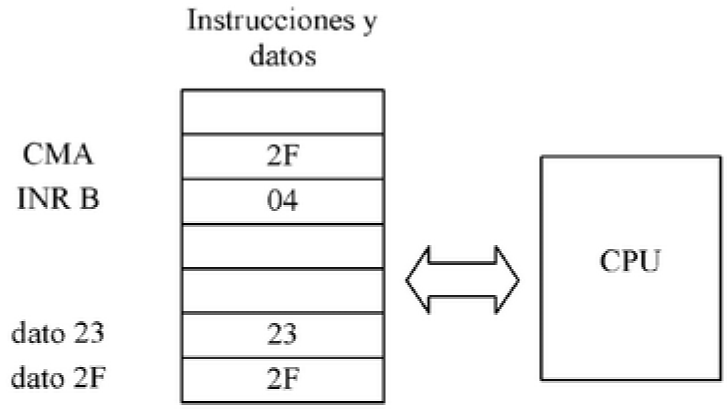


Figura 1.2: Arquietctura Von Neumann

En estos casos es común el tener un programa para tomar datos externos, almacenarlos como datos en la memoria y ejecutarlos como instrucciones.

Actualmente se tienen microprocesadores de ambas arquitecturas y depende de las necesidades de cada situación en la que se beneficiaá del uso de una u otra arquitectura.

Puertos

Los puertos son un conjunto de conexiones con las que el procesador puede interactuar con el mundo exterior a través de señales digitales.

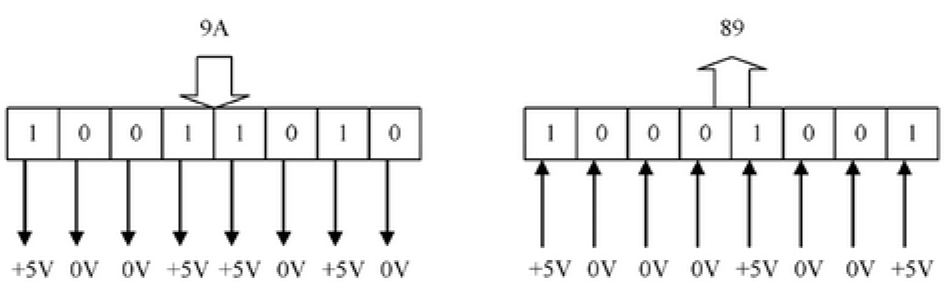


Figura 1.3: Puertos de Entrada y Salida

Un procesador considera a estos como locaciones de memoria que se escriben o leen datos. A un puerto que toma datos del exterior se le conoce como puertos de entrada (input) y si envía información al exterior entonces es de salida (output). Generalmente a estos puertos se les conoce como Puertos I/O.

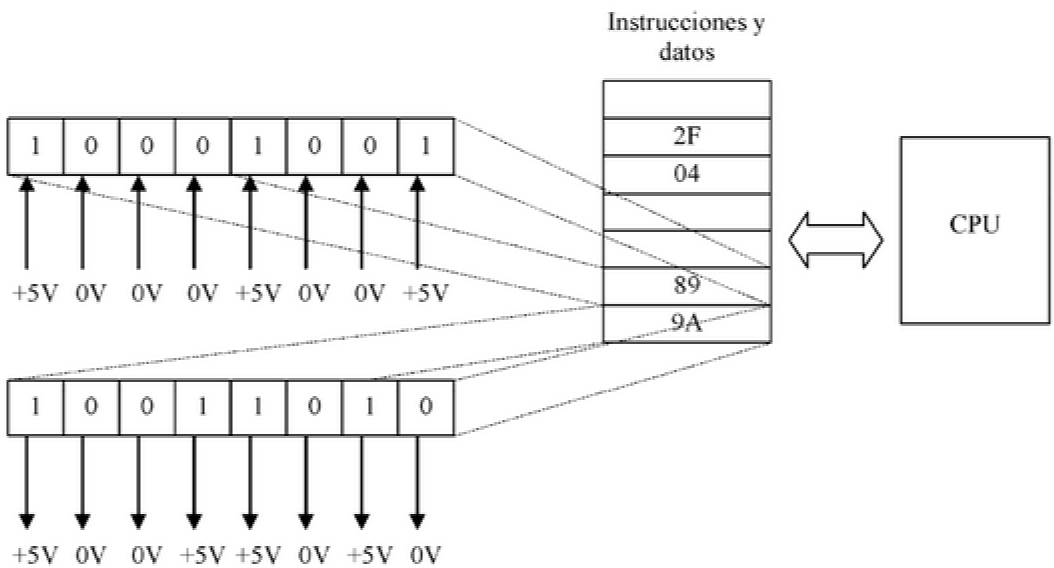


Figura 1.4: Interacción de puertos con la memoria y con el procesador

1.2. Microprocesador

El procesador en una computadora, esta comprendido de varios circuitos integrados, mientras que un microprocesador es un procesador empaquetado en un único circuito integrado. Una microcomputadora usa un microprocesador como su CPU[Valdes and Areny, 2007].

Los microprocesadores vienen en diferentes presentaciones, 4-Bits, 8-Bits, 16-bits, 32-Bits e incluso en 64-Bits aunque estos últimos no son demasiado comunes como los anteriores. El número de bits corresponde al número de digitos binarios que el microprocesador puede manipular en las operaciones.

El acceso de la memoria principal toma mucho más tiempo que el tiempo de reloj disponible por el CPU, por ello es que los microprocesadores de 32 y 64 Bits poseen una textitmemoria caché de alta velocidad.

1.3. Microcontrolador

Una microcomputadora se compone de 3 bloques fundamentales: CPU, Memoria y los puertos de entrada/salida. Estos se conectan entre si mediante grupos de lineas eléctricas denominados buses; los cuales pueden ser de direcciones, si transportan direcciones de memoria, o de datos, si en cambio transportan datos o instrucciones, o de control si estos conducen diversas señales de control.

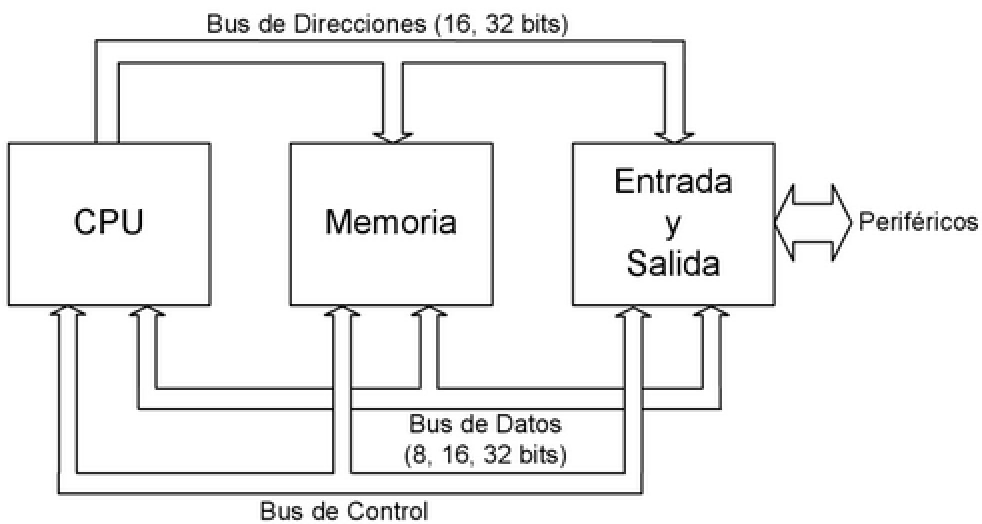


Figura 1.5: Esquema básico general de un microprocesador

El CPU es el encargado en traer las instrucciones alojadas en la memoria, interpretarlas y hacer que se ejecuten. En una micromputadora la CPU es el microprocesador por lo cual un Microcontrolador es una Microcomputadora fabricada en un Circuito Integrado.

Los microcontroladores son construidos fundamentalmente para aplicaciones puntuales en automoción, equipos de comunicaciones y telefonía, instrumentación electrónica, equipos médicos e industriales, electrodomésticos, etc. donde se deben realizar un pequeño número de tareas al menor costo posible. En estas el microcontrolador ejecuta un programa almacenado permenentemente en la memoria interactuando con datos almacenados temporalmente e interactua con el exterior a traves de las líneas de entrada/salida. El microcontrolador es parte de la aplicación(Controlador Embebido).

1.3.1. Elementos Principales

Además de la microcomputadora (CPU, memori y lineas de entrada/salida) los microcontroladores disponen de más componentes para poder realizar el funcionamiento requerido por las aplicaciones.

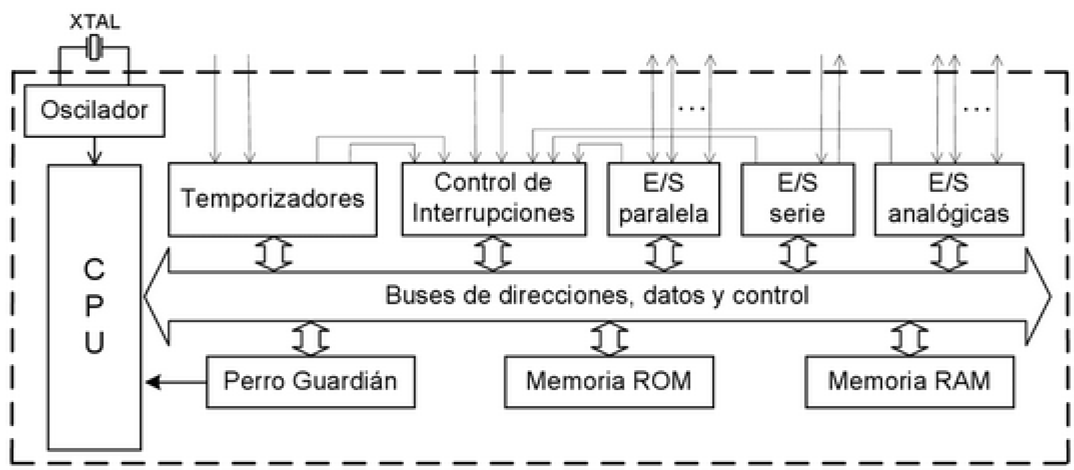


Figura 1.6: Esquema de bloques de un microprocesador

Oscilador

Para poder realizar las operaciones internas el microcontrolador depende de un oscilador que genera los impulsos que permiten la sincronización de todas ellas. En la mayoría de los microcontroladores se utiliza como oscilador a un cristal de cuarzo debido a la gran estabilidad de frecuencia que ofrecen estos cristales ya que de estos dependen la velocidad de ejecucion de las tareas.

Watchdog Timer (Perro Guardián)

Es un recurso disponible en la mayoría de los microcontroladores, consta de un oscilador (puede ser el principal) y de un contador binario de N-bits. La salida del contador va conectada al circuito *reset* del microcontrolador(1.7). El funcionamiento se define como un contador de pulsos que al llegar al desbordamiento reinicia el dispositivo, el fin de este bloque es que el programador evite el desbordamiento y por ende el reinicio del dispositivo, por ello se debe reiniciar el contador desde el programador. En cambio si existe un error en alguna parte del código que evita que se reinicie el contador del perro guardián este reiniciará el microcontrolador y será posible retomar el control y redirigir el programa por la ruta correcta.

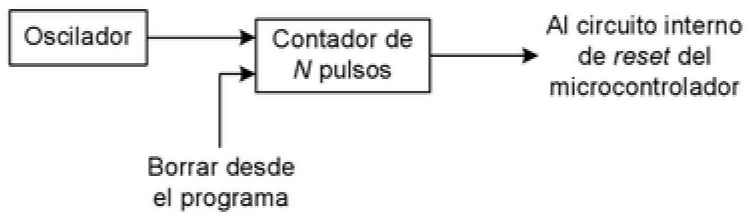


Figura 1.7: Bloque WatchDog Timer

Es importante que cuando no se limpie el contador WDT a tiempo, se realice la acción de *reset* ya que entonces significa que se ha encontrado un fallo en la secuencia de las instrucciones y para remediarlo se redirecciona a una direccion de memoria determinada y no una aleatoria como podría suceder en estos casos.

En algunos microcontroladores como los PIC se señaliza la causa del reset por medio de bits de un registro del microcontrolador con lo cual se puede remediar el origen del fallo.

Reset

El reset es una función con la cual se inician los microprocesadores y los microcontroladores. Esta acción se ejecuta cuando una señal de reset es aplicada de manera manual a una terminal en el CI con lo cual se pone el contador de programa (PC) a un valor predeterminado comunmente 0 haciendo que el microprocesador comienze a ejecutar las instrucciones a partir de esa posición.

En un microcomputador la señal de *reset* se genera e forma manual al pulsar un botón o al iniciar el sistema (*Reset* por encendido), sin embargo tambien pueden haber otras fuentes de *reset* como lo son por "Fallo de Alimentación.º por "Desbordamiento del WatchDog Timer".

El segundo caso, como se explicó anteriormente sucede cuando el contador WDT se desborda al no reiniciar el contador por lo que el microcontrolador ha perdido la secuencia de las instrucciones o ha entrado en un bucle demasiado largo. El primer caso sucede cuando el valor de voltaje cae por debajo del umbral de operación momentáneamente con lo que el capacitor se descarga parcialmente y se produce el reinicio del dispositivo.

Estado de Bajo Consumo

Una parte importante en los microcontroladores es la caracteristica de tener un bajo consumo de corriente ya que hay un gran número de aplicaciones que rquieren el uso de baterias como medio de alimentación por lo que un bajo consumo de corriente ayuda a una prolongada duración de la bateria.

El consumo de corriente en el circuito se sustenta en el uso de compuertas CMOS que al mantenerse en un nivel lógico estático el consumo es prácticamente 0 y solo aumenta cuando el oscilador aumenta la frecuencia de las conmutaciones de los estados de las compuertas lógicas.

Los microcontroladores comunmente se encuentran en este estado y únicamente se activan al ocurrir un evento externo, realizan una tarea y regresan a este estado por lo que se recomienda tener el microcontrolador con bajo consumo de corriente hasta que ocurra un evento que lo saque de ese letargo.

Memoria

La memoria en un microcontrolador es el lugar donde se almacenan el programa que se va a ejecutar y los datos y/o variables que va a utilizar. La memoria de datos es de lectura y escritura y los datos no permanecen en ella una vez que se suspende la alimentación al microcontrolador, es decir, la memoria es volátil (Memorias RAM estáticas). Algunos microcontroladores usan una memoria adicional externa de lectura y escritura no volátil como parte de la memoria de datos, para permitir almacenamiento de datos fijos, para este tipo de memorias se utilizan comunmente EEPROM.

- **RAM:** Esta es un tipo de memoria de lectura y escritura de alta velocidad. En la memoria RAM la información almacenada permanece estable indefinidamente mientras no se suprima la alimentación del microcontrolador.

- **ROM:** Si se usa memoria ROM ésta se graba durante la fabricación del dispositivo y no se puede alterar una vez almacenada, por ello el programa debe ser depurado. Los microcontroladores que utilizan este tipo de memorias son aquellos que se fabrican en grandes cantidades ya que su fabricación es bastante rentable gracias a su bajo costo.
- **EEPROM:** Las memorias EEPROM son memorias no volátiles de lectura y escritura, donde la escritura se realiza por medios eléctricos y se puede lograr individualmente sin la necesidad de un borrado previo, sin embargo a pesar de ser reprogramables cuentan con un número finito de veces.
- **FLASH:** En las memorias FLASH se pueden realizar las operaciones de lectura y escritura celda por celda, pero a diferencia de las anateriores se requiere primero borrar la información de la celda antes de escribir en ella y estas deben borarse por bloques de celdas colocando a 0. A menudo las operaciones de ecritura de información se debe realizar un proceso de lectura-borrado-escritura del bloque de celdas donde se desea escribir la información. Todas las operaciones de borrado, lectura y escritura se realizan con la misma tensión de voltaje

1.3.2. Arquitecturas CISC y RISC

CISC (Complex Instruction Set Computer) y RISC (Reduced Instruction Set Computer) son dos modelos de computadoras visto desde el repertorio de instrucciones que repercuten en el modelo de arquitectura de la CPU y como lo dice su nombre las computadoras CISC tiene una mayor cantidad de instrucciones miestras que el RISC posee una menor cantidad.

Las arquitecturas CISC predominaba en un inicio debido a la ambición de hacer los microprocesadores y microcontroladores los más potente posibles. Debido a la complejidad que fue aumentando lo hizo también la complejidad de la CPU y por ende se le debió dedicar un mayor espacio en el circuito integrado a la decodificadción y ejecución de las instrucciones.

Por el contrario las RISC tienen un repertorio corto de instrucciones sencillas que pueden realizar operaciones simples pero a alta velocidad. La complejidad del CPU disminuye, así que a frecuencia del oscilador puede aumentar y así mejorar la velocidad de ejecución de las operaciones. Esto támbien apoya en su fabricación siendo más sencillos y baratos de producir, por ello esta arquitectura ha sido la predominante en microcontroladores PIC.

1.4. PIC32MZ2048EFM100

Es un microcontrolador de 32-bits que permite la conectividad embebida con una unidad de Punto Flotante[PIC, 2019], esta familia de microcontroladores poseen una gran cantidad de puertos de comunicación lo que permite que sea una opción bastante adecuada para proyectos en los que se necesite el intercambio de información entre varios dispositivos.

La especificaciones del microcontrolador se pueden ver en la tabla.

En particular esta familia de microcontroladores posee perifericos que operan a una mayor frecuencia que los microcontroladores tipicos usados para los sistemas embebidos. Esto es posible gracias al microprocesador que posee la CPU el cual contiene varios bloques lógicos que trabajan en conjunto en paralelo, proviendo un alto rendimiento de procesamiento.

1.5. Medidor de Energía ADE7880

Este Circuito Integrado es un medidor de energía eléctrica trifasica de alta precisión, con interfaces de comunicación serial I^2C y SPI. Es adecuado para la medición de energía electrica activa, reactiva y aparente en varias configuraciones trifásicas, además posee registros de muestreo de formas de onda para todas las salidas del Convertidor Análogico Digital incluido en el CI[1].

[1] Circuito Integrado ADE7880 renombrado asi a partir de aqui para simplificar.

Nombre	**Valor**
Familia	PIC32MZEF
Velocidad Max CPU [MHz]	200
Tamaño de Memoria Programable [KB]	2048
SRAM [KB]	512
Auxiliary Flash [KB]	160
Crypto Engine	Yes
Range Temperatura [°C]	-40 to 125
Rango de Voltaje Operacional [V]	2.2 to 3.6
Direct Memory Access Channels	8
Canales SPI	6
Canales I2C	5
Interfaz CODEC (I2S,AC97)	Yes
Peripheral Pin Select / Pin Muxing	Yes
Ethernet	10/100 Base-TX Mac
Número de Puertos Ethernet	1
Número de Modulos USB	1
Interfaz USB	High Speed
Números de Modulos CAN	2
Tipo de Modulos CAN	CAN
Entrada ADC	40
Resolucion Max ADC (Bits)	12
Max Rango de Muestreo ADC [ksps]	18000
Entradas de Captura	9
Standalone Output Compare/Standard PWM	9
Max 16-bit Digital Timers	9
Parallel Port	PMP
Number of Comparators	2
Internal Oscillator	8 [MHz], 32 [kHz]
Hardware RTCC/RTC	Yes
Max I/O Pins	78
Pincount	100
Serial Quad Interface	Yes

Tabla 1.1: Especificaciones PIC32MZ2048EFM100

1.5.1. Gestion de Energía

Este CI posee 4 modos de energía determinados por el estado de los pines PM0 y PM1 estros proveen total control sobre el chip y gracias a que poseen resistencias pull-up internas se pueden copnectar facilmente al microcontrolador.

Los modos de operación son:

Modo de Energía	**PM1**	**PM0**
PSM0	0	1
PSM1	0	0
PSM2	1	0
PSM3	1	1

Tabla 1.2: Configuración de los pines PM para los modos de suministro de energía

- **PSM0 (Normal Power Mode):** Este es el modo de operación completamente funcional. Si el medidor de energía se encuentra en cualquiera de los otros modos y se cambia a este todos los regitros automáticamente son reiniciados a sus valores iniciales, con excepción del registro LPOILVL[2] y el registro CONFIG2[3].

  Cuando se realiza la transición de un modo de energía a otro el CI cambia el estado del pin $\overline{IRQ1}$ a bajo y el bit 15 (RSTDONE) en el registro STATUS1 a alto, especialmente este último es el que indica el fin de la transición ya que durante es 0.

- **PSM1 (Reduced Power Mode):** En este modo el CI mide los valores absolutos promedio de las 3 fases de corriente para almacenarlos en los registros $xIMAV$ [4]. Este modo es útil al usar una batería externa. Los puertos de comunicación serial estan activos y se puede utilizar para leer los registros $xIMAV$, sin embargo, a pesar de poder leer estos registros para los demás registros del CI no se garantizan que los valores sean correctos.

  Al entrar en este modo despues de haber estado en en el PSM0 entonces el cálculo de valor absoluto promedio inicia sin retrasos. Los registros $xIMAV$ son

[2] Registro del límite de sobrecorriente durante el modo PSM2.
[3] Registro de configuración de armónicos.
[4] *x:* Canal de corriente A. B, C.

accesibles en cualquier momento después de que el pin $\overline{IRQ1}$ ha cambiado a un valor de 0 (indicando el inicio del cómputo de valores absolutos promedio).

- **PSM2 (Low Power Mode):** Los puertos de comunicación no son funcionales en eeste modo, se reduce el consumo requerido para monitorear la corriente cuando no hay entrada de voltaje y la fuente de voltaje es provista por una bateria externa.

  Si el pin $\overline{IRQ0}$ está en un nivel lógico bajo al acabar el periodo de medición, entonces significa que todas las fases de corriente se meantuvieron por debajo del límite y, por lo tanto, no hay corriente fluyendo por el sistema, en este punto el microcontrolador externo pone el CI en modo de de espera. Si en cambio el pin $\overline{IRQ1}$ es el que se encuentra en bajo, entonces significa que por lo menos una entrada de corriente está por encima del límite definido y hay corriente fluyendo por el sistema a pesar de que no hay voltaje presente en los pines del CI. Esta situación se conoce como falta neutra, en este punto el microcontrolador externo coloca el CI en el modo PSM1. No es recomendable usar este modo si los registros de ganancia[5] son diferentes a 1 ó 2.

- **PSM3 (Sleep Mode):** En este modo la mayoría de los circuitos internos se encuentran apagados y el consumo de corriente se mantiene a su más bajo nivel. Los puertos I^2C, SPI Y HSDC no son funcionales, además los pines de $\overline{RESET}$, MOSI/SDA, SCLK/SCI y $\overline{SS}$/HSA deben permanecer en alto.

1.5.2. Procedimiento de Encendido

El ADE7880 posee un chip interno que monitorea la fuente de alimentación (VDD). En el encendido el dispositvo permanece inactivo hasta que VDD alcanza los 2.0[V]$\pm$10 %. Al sobrepasar este límite el monitor mantiene el dispositivo en inactivo por 26[ms] para permitir alcanzar el voltaje de 3.3[V]$\pm$10 % a la fuente de voltaje.

Los pines PM0 y PM1 tienen resistencias pull-up, pero es necesario el colocar PM1 en un nivel lógico bajo ya sea por hardware (colocando a tierra) ó a travez del

[5]PGA1[2:0].

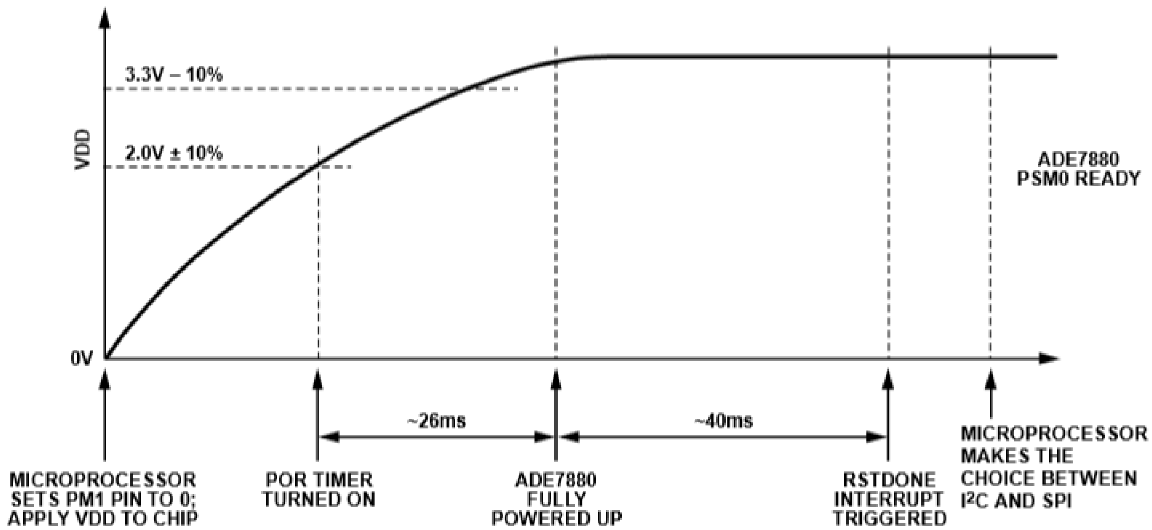


Figura 1.8: Procedimiento de encendido

microcontrolador antes de encender el chip, para asegurar que el dispositivo se inicie en PSM0. El tiempo de encendido es de al rededor de 40[ms] tiempo en el cual el pin de $\overline{RESET}$ debe permanecer en un nivel lógico alto.

Al iniciar en en modo PSM0 el puerto activo es el I^2C, si se desea cambiar el puerto de comunicación se tiene que alternar el pin $\overline{SS}$/HSA 3 veces de un nivel lógico de voltaje alto a un nivel de voltaje bajo. Cuando se decide usar un puerto de comunicación este debe bloquearse para evitar que durante la comunicación ó combio de modo de energía se alterne por el otro puerto y se pierda la comunicación. Para ello si el puerto activo es el I^2C se debe escribir un 1 el bit 1 (I2C_LOCK) del registro CONFIG2 en caso contrario si el puerto activo es el SPI entonces cualquier escritura al registro CONFIG2 bloqueará este puerto como el activo. En ambos casos el cambio por el otro puerto de comunicación no es posible hasta que se haga un reinicio de hardware o se apague y vuelva a encender el sistema.

Inicialmente el CI se encuentra en modo de reposo y, por lo tanto, no ejecuta ninguna instrucción, es en este punto donde todos los registros necesarios para la ejecución del programa deben iniciarse. Si el voltaje cae por debajo de los 2.0[V]$\pm$10 % este entra en estado inactivo y ninguna medición ó cómputo es ejecutada.

1.5.3. Hardware Reset

Este tipo de reset se logra al tener el CI en el modo PSM0 y colocando el pin de $\overline{RESET}$ en un nivel de voltaje bajo, en otros modos de energía el pin no tiene función. Si entonces el pin es alternado de alto-bajo-alto con 10[ms] de retraso entre cambio. Durante el proceso de reinicio el pin $\overline{IRQ1}$ permanece en 1, al termino del proceso este pin es colocado a 0 y todos los registros son devueltos a sus valores iniciales de fábrica.

El reinicio por Hardware devuelve el puerto I^2C como canal principal de comunicación.

1.5.4. Software Resest

Al igual que el reset por Hardware estaopción solo esta disponible durante el modo PSM0. Para iniciar el reset por Software se utiliza el bit 7 en el registro CONFIG, inicialmente este bit se encuentra en 0, y si es cambiado a 1 entonces entra en modo de Reset, el cual regresa a valores iniciales a la mayoria de los registros, la seleccion de puerto de comunicación se mantiene si se ha bloqueado de manera correcta. Los únicos valores que mantienen sus valores son CONFIG2 y LPOILVL.

1.5.5. Operación del ADE7880

Entradas analógicas

Se tienen 7 entradas analógicas que forman los canales de corriente y voltaje. Los canales de corriente constan de 4 pares de entradas IxP/IxN[6] diferenciales los cuales tienen un máximo de señal ± 0.5[V] e igual con respecto a la señal en AGND[7].

Todas las entradas poseen un Amplificador Programable de Ganancia (PGA por sus siglas en inglés) con una selección de 1, 2, 4, 8 ó 16. Las ganancias presentes en IA, IB e IC se colocan en un registro diferente a IN[8] para obtener una ganancia diferente

[6]x: Canales A, B, C y N respectivamente
[7]Referencia a tierra para el circuito analógico.
[8]Entrada analógica del canal de corriente neutral.

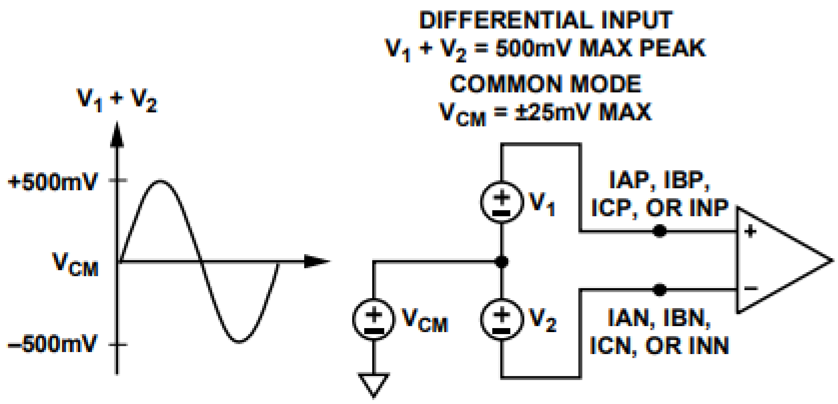


Figura 1.9: Esquema de entradas analógicas de corriente

a las 3 primeras.

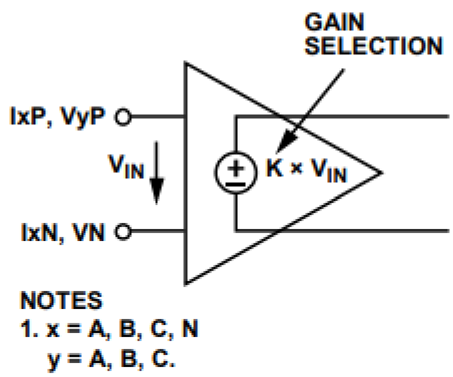


Figura 1.10: Esquema de los amplificadores de ganancia en las entradasa analógicas

El canal de voltaje tiene 3 entradas de voltaje de un sólo extremo, con una entrada máxima de ±0.5[V] con respecto a VN[9], de igual manera estas entradas tienen una entrada de señal máxima de ±0.5[V] con respecto a AGND.

Convertidor Analógico Digital

A las entradas de los canales de corriente y voltaje se tienen Convertidores Analógicos Digitales Σ-Δ, estos se encuentran activos en el modo PSM0, y en el PSM1 solo los que miden los canales de corriente se encuentran activos a excepcion del canal de corriente neutral. En los otros modos no estan activos ninguno de los ADC[10].

[9]Entrada analógica del canal de voltaje neutral.
[10]Convertidor Analógico Digital.

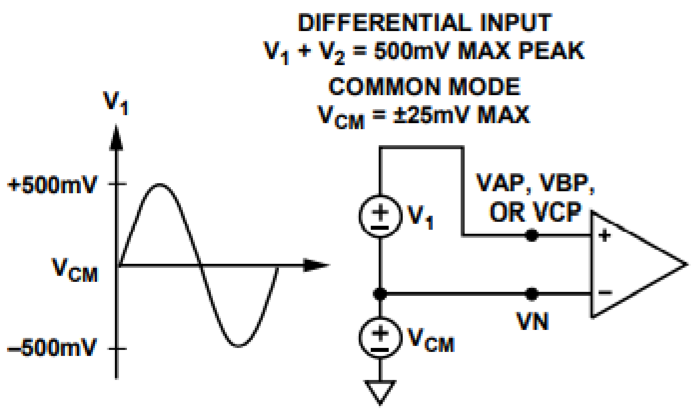


Figura 1.11: Esquema de entradas analógicas de voltaje

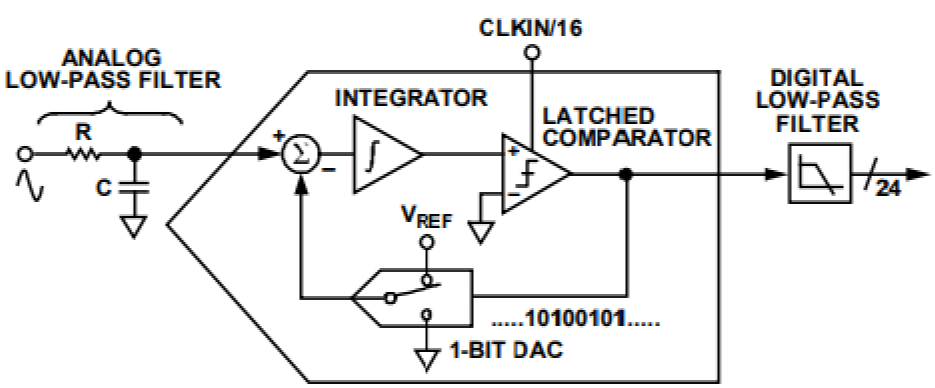


Figura 1.12: Convertidor Analógico Digital

El módulo Σ-Δ convierte la señal de entrada en un flujo en serie de "1z "0.ª un tiempo determinado por el reloj de muestreo (En el ADE7880 este reloj es de 1.024[MHz]). El DAC[11] de 1-bit en el bucle de retroalimentación es llevado por el flujo de datos en serie, entonces la la salida del DAC es sutraida de la señal de entrada. Si el bucle de ganancia es lo suficientemente alto el valor promedio de la salida del DAC puede aproximarse al nivel de la señal de entrada. El promedio es pasado entonces a un filtro digital pasa-bajas que produce una palabra de 24-bits proporcional al nivel de la señal de entrada.

Filtro Antialias

Este filtro se encuentra a la entrada del ADC y su función es la de prevenir el solapamiento que se presenta en todos los sistemas de muestreo.

Para sensores de corriente convencionales es recomendable usar filtros RC[12] con una frecuencia de corte de 5[kHz] para que la atenuación sea suficiente para eliminar los efectos de solapamiento para sensores de corriente convencionales.

Función de Transferencia de los ADC

Todos los ADC en el CI estan diseñados para producir el mismo nivel de señal de la salida en el código de 24-bits con signo a la salida. El código del ADC puede variar entre 0x800000 (-8,388,608) y 0x7FFFFF (8,388,607), esto es equivalente a una señal de entrada de ± 0.787[V], por lo tanto no debe excederse el rango nominal especificado de ± 0.5[V]. Las señales se muestrean a una velocidad de 8[kSPs][13].

1.5.6. Interfaces de Comunicación

El ADE7880 posee 3 puertos de comunicación serial SPI, I^2C Y HSDC, sin embargo por la configuración de los pines solo se pueden usar 2 tipos de configuraciones, una utilizando el puerto SPI únicamente y la segunda es usando los puertos I^2C Y HSDC.

[11] Convertidor Digital Analógico.
[12] RC: Resistor Capacitor.
[13] kSPs: Mil muestras por segundo (Kilo Samples per second).

Se incluyen un conjunto de 3 registros que permiten verificar la comunicación con el CI. Los regsitros LAST_OP (Address 0xEA01), LAST_ADD (Address 0xE9FE) and LAST_RWDATA se encargan de almacenar los datos, la dirección de registro y la naturaleza del acceso al registro (Lectura/Escritura) de la última comunicación exitosa respectivamente. El registro LAST_RWDATA tiene 3 diferentes direcciones dependiendo de la longitud del registro de la última comunicación.

Tipo de comunicación	**Dirección de registro**
Lectura/ Escritura de 8-Bit	0xE7FD
Lectura/ Escritura de 16-Bit	0xE9FF
Lectura/ Escritura de 32-Bit	0xE5FF

Tabla 1.3: Direcciones de los registros de última escritura (LAST_RWDATA)

Después de cada comunicación exitosa los registros se actualizan con la información de la operación, 0xCA si fue escritura y 0x35 si es escritura y el dato que se leyó o escribió. Las operciones no completadas no se reflejan en estos registros asi como cuando se leen estos registros.

SPI (Serial Peripheral Interface)

El SPI de este CI siempre es esclavo en la comunicación y consiste en 4 pines de comunicación SCLK, MOSI, MISO Y SSA.

El reloj para la transferencia de datos debe aplicarse al pin SCLK y todas las transferencias de datos se sincronizan con este reloj. El intercambio de información entrante en el CI se realiza en el pin MOSI en los flancos descendentes del reloj serial y el CI lo muestrea en los flancos ascendentes del reloj. Por el contrario la información saliente del CI se transfiere por el pin MISO en los flancos descendentes del reloj serial y el dispositivo maestro muestrea la información en los flancos ascendentes. El bit más significante de la palabra es intercambiado a la entrada. La másima frecuencia del reloj serial soportada por esta interfaz es de 2.5[MHz], el pin MISO se mantiene en alta impedancia mientras no hay intercambio de información.

EL pin $\overline{SS}$ es utilizado para seleccionar entra más de un dispositivo si es que los hay. Para poder utilizar el dispositivo y realizar la comunicación entre ete y el dispositivo maestro este pin debe llevarse a un voltaje lógico bajo y permanecer así mientras dure la comunicación. Al cambiar el nivel lógico de este pin aborta la transferencia y para iniciar una nueva este se debe volver a poner a un voltaje lógico bajo.

I^{2}C (Inter Integrated Circuits)

Este CI posee una interfaz I^{2}C para la comunicación, implementada completamente como un hadware esclavo. El pin de intercambio de información SDA se encuentra localizado en el pin 38 y se encuentra compartido con el pin MOSI del puerto SPI, de igual manera el reloj serial SCL se encuentra compartido con el reloj serial del puerto SPI en el pin 36. La máxima frecuencia soportada por el reloj serial es de 400[kHz].

La secuencia de transferencia del sistema I^{2}C consiste en el dispositivo maestro generando un condición de inicio para la transferencia cuando el bus se encuantra desocupado. El dispositivo maestro entonces transmite la direccion del dispositivo esclavo (0x70) y la dirección del regitro de la transferencia de datos en la transferencia de dirección inicial si el dispositivo esclavo reconoce entonces empieza la transferencia de datos. Esto continua hasta que el maestro emite una condición de parada y el bus queda de nuevo desocupado.

HSDC (High Speed Data Capture)

Debido a que para este proyecto es necesario el recopilar una gran cantidad de muestras a alta velocidad la documentación del Circuito Integrado ADE7880 recomienda, para la lectura de estos registros en específico, utilizar una interfaz propia de Analog Devices para este circuito llamada High Speed Data Capture (Captura de Datos a Alta Velocidad) por lo que es necesario configurar el microprocesador de manera que se pueda usar la comunicación I^{2}C como interfaz serial principal y la comunicación HSDC como secundaria usando el canal SPI del microcontrolador como esclavo, que recibirá toda la información de los registros de voltaje y corriente enviados por esta interfaz.

1.6. Entorno de Desarrollo MPLABX

Microchip provee un entorno de desarrollo y un compilador

1.6.1. Herramienta de configuración MPLAB Harmony

1.7. Firmware

1.7.1. Inicialización

La programación del proyecto se realiza por parte del entorno de desarrollo de Microchip MPLAB X, mientras que la conficuración de los puertos se realiza con la herramienta proporcionada por el mismo MPLAB Harmony debido a que la configuración manual sería demasiado complicada debido a la cantidad de puertos, pines y servicios disponibles por parte del microcontrolador. ya que esta es una actualización del módulo de medición de energía por lo que la inicialización esta parcialmente completa, sin embargo al realizar el cambio de canal de comunicación principal de SPI (1.13) a I2C(1.14) y HSDC(Este puerto utiliza la interfaz SPI del microcontrolador por lo que se reconectan los pines pero se deja la configuración) se cambió las configuraciones de estos canales. Todas las demás siguieron igual a como se tenían en la primer versión del módulo.

1.7.2. Configuración del puerto I^2C

Este puerto se activa al encender el dispositivo o al realizar un reinicio de hardware, entonces el puerto I^2C queda seleccionado como interfaz de comunicación. Para evitar que al hacer cambios en el nivel de voltaje del pin $\overline{SS}$/HSA se cambie a la interfaz de comunicación SPI, se debe bloquear el puerto I^2C para ello se debe poner a 1 el Bit 1 (I2C_LOCK) del registro CONFIG2, esto previene que al realizar cambios de voltaje en el pin $\overline{SS}$/HSA y el cambio a SPI no es posible hasta que se realize un reinicio de hardware o se reinicie todo el sistema.

Este registro se accesa como si fuera un registro de 8-Bits por lo que los 6 Bits

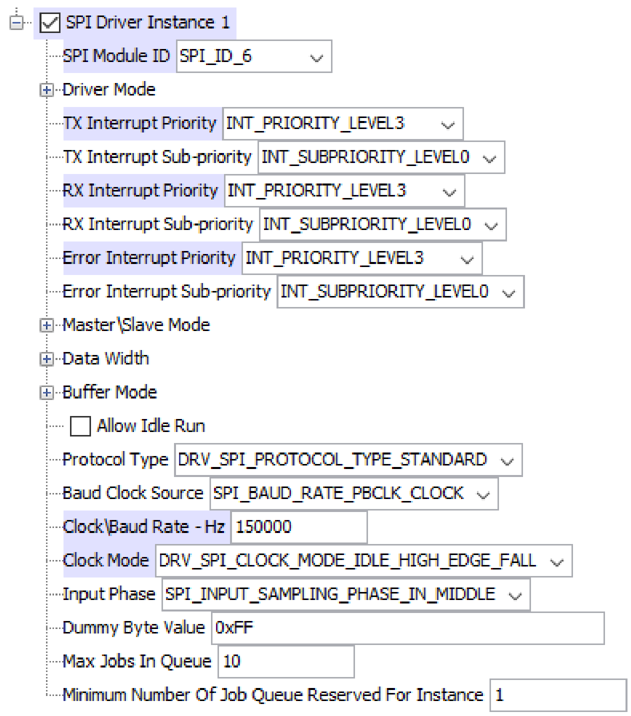


Figura 1.13: Configuración SPI del PIC32MZ

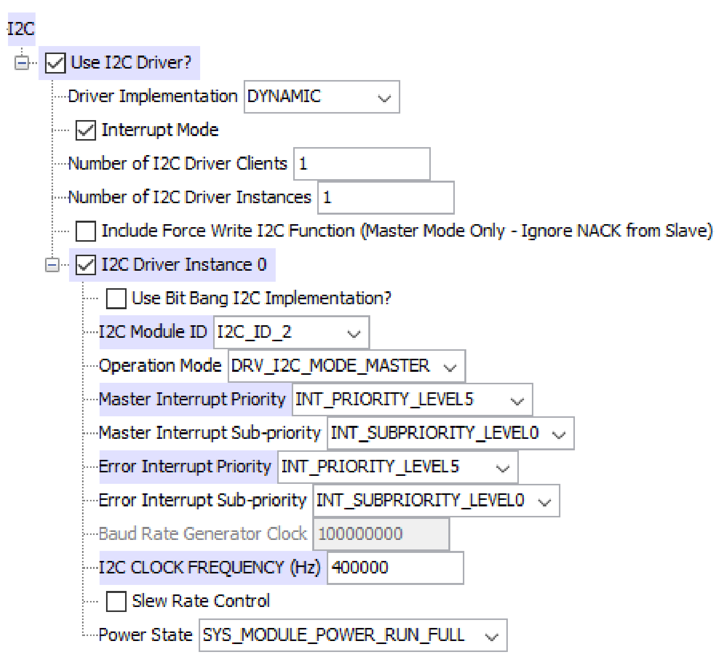


Figura 1.14: Configuración I2C del PIC32MZ

Bit	Mnemonico	Valor predeterminado
0	EXTREFEN	0
1	I2C_LOCK	1
7:2	Reservados	0

Tabla 1.4: Valores del registro CONFIG2 que se deben transmitir para bloquear el puerto I^2C

más significativos deben permanecer como 0. En este caso en particular se transmite 0x02 a la dirección de registro 0xEC01.

1.7.3. Configuración del puerto HSDC

Para configurar el puerto HSDC se debe escribir primero al registro HSDC_CFG [0xE706] a traves del puerto I^2C la configuración con la que se van a estar enviando los datos a traves del puerto HSDC. Ya que se configura el puerto se habilita colocando el bit 6 (HSDCEN) en el registro CONFIG [0xE618] a 1, con esto se activa la comunicación.

La configuracion que se ha decidido usar es tener el reloj a 8[MHz] con la transmision de registros en paquetes de 32-bits, no se agrega una brecha de 7 ciclos de reloj entre transmisiones y unicamente se transmitira el contenido de los registros de voltaje y corriente: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, e INWV, lo que permite que se realice la comunicación de manera más rápida. El pin de selccion de esclavo ($\overline{SS}$ ó Chip Select) se mantiene como activo en bajo.

Capítulo 2

Resultados

Como se explicó al principio el desarrollo de este proyecto se pensó como una mejora a los medidores de energía anteriormente fabricados por el Instituto de Ingeniería por lo que este, solo se centró únicamente en la lectura de muestras a alta velocidad por parte del microcontrolador.

2.1. Lectura de Datos Usando el Canal SPI

En un principio el sistema medidor de energía estaba pensado para realizar la comunicación entre el microprocesador y el medidor ADE7880 con interfaz SPI sin embargo al momento de realizar las primeras pruebas, los registros correspondientes a los canales de medición de voltaje y corriente, pasado un tiempo los valores que se recuperan de los registros pierden coherencia lo que hace que los resultados sean inutiles para su análisis.

La lectura de los registros se configuró para que el microprocesador lo realizara a la mayor velocidad posible utilizando un reloj de 150000[Hz] por el canal 6 SPI 1.13.

En la siguiente gráfica 2.1 se puede ver como la velocidad de comunicación es bastante rápida al leer los valores de registro a pesar de tener que leer el registro DREADY para asegurarse que los registros de voltaje y corriente esten listos se obtenían demasiado rápido, pero como se había mencinado estos valores no demostraban valores que puedan ser útiles.

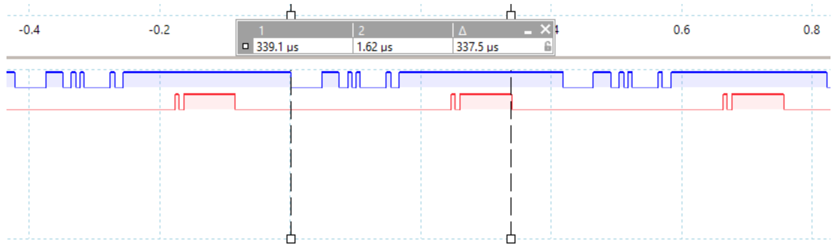


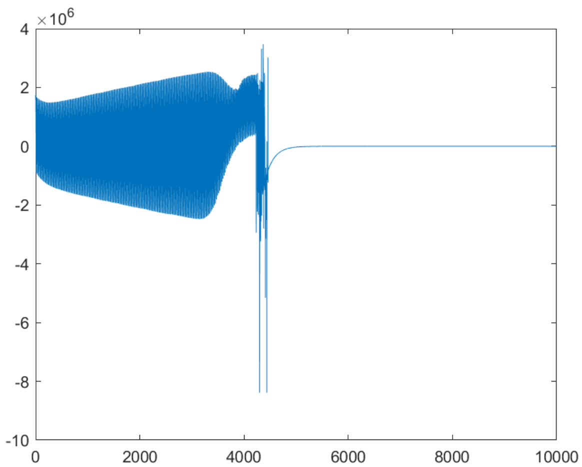
Figura 2.1: Comunicación SPI con los registros de voltaje y corriente

Como se pueden ver en las graficas de voltaje (Graficas 2.2) y corriente (Graficas 2.3) al usar el canal SPI para muestrear los registros de voltaje y corriente de los 3 canales estos entregaban valores que no reflejaban la energía que se suministraba y en algunos casos ni siquiera se actualizaban los valores que el dispositivo tiene inicialmente, ya que las pruebas que se hacían se realizaban con un simulador de voltaje y corriente controlado con lo cual era posible conocer el valor que se deseaba obtener.

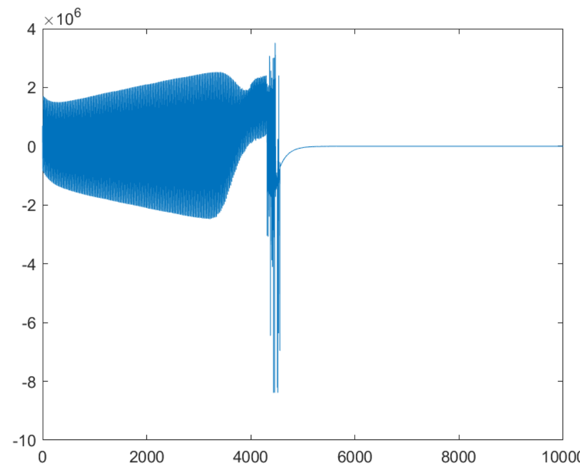
Después de realizar un par de pruebas más y obtener valores similares en todas las pruebas y siguiendo la recomendación que el manual del dispositivo para la lectura de esos registros se decidió cambiar el canal de comunicación de SPI por el HSDC con el cual se planea tener una lectura más rápida de los registros así como poder mantener la comunicación únicamente con los registros de voltaje y corriente de manera continua sin interaciones con los otros módulos del sistema de medición de energía.

2.2. Lectura de Datos usando el canal HSDC

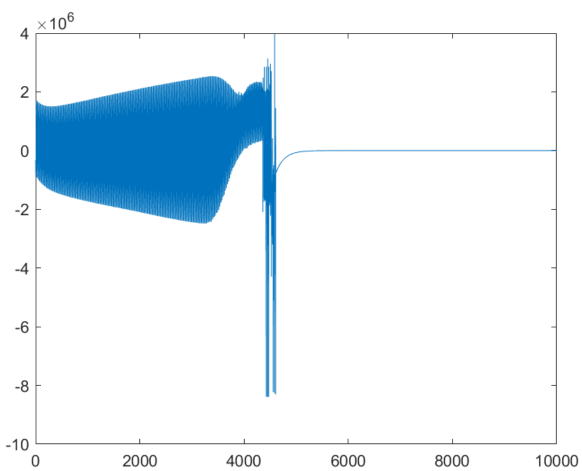
Las primeras pruebas que se realizaron usando este canal de comunicación inicia de manera correcta al configurar los valores necesarios en el registro correspondiente del ADE7880, se comprobó usando el osciloscopio que los paquetes de datos se envíen y reciban de manera correcta por el canal I2C para despues comprobar que el puerto HSDC realmente envíe información. Al iniciar el DSP se comprobó que el puerto HSDC enviaba la información proveniente de los registros de corriente y voltaje del medidor de energía.



(a) Canal de Voltaje A

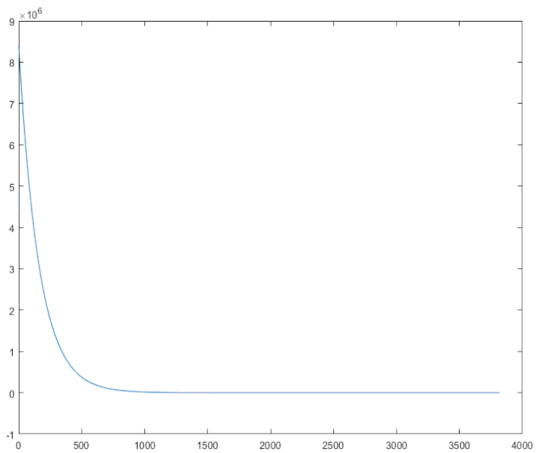


(b) Canal de Voltaje B

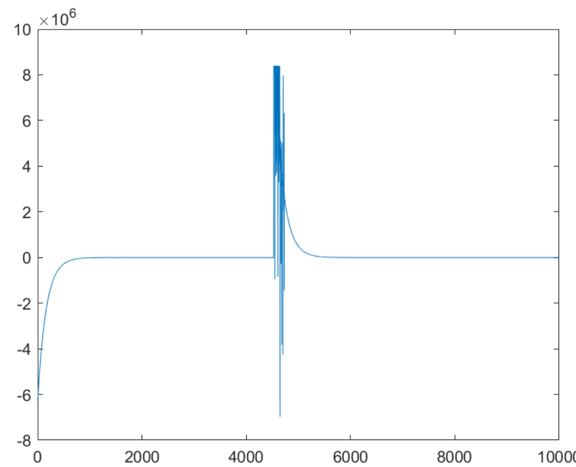


(c) Canal de Voltaje C

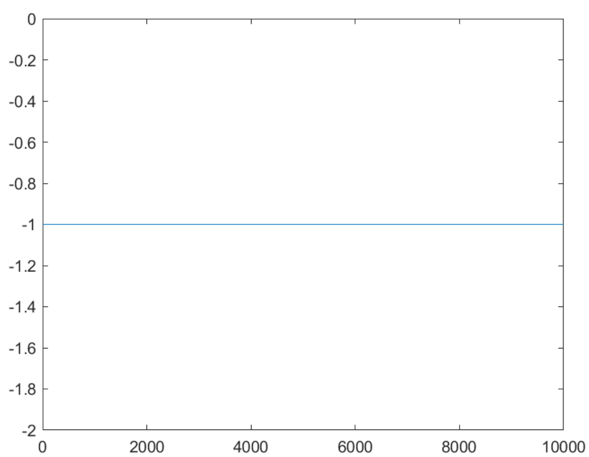
Figura 2.2: Gráficas de la primer prueba de los Canales de Voltaje



(a) Canal de Corriente A



(b) Canal de Corriente B



(c) Canal de Corriente C

Figura 2.3: Gráficas de la primer prueba de los Canales de Corriente

Capítulo 3

Conclusiones

Capítulo 4

Glosario

Frecuencia de corte (ωC) o también llamada frecuencia de esquina o frecuencia crítica. Es la frecuencia donde la respuesta en amplitud está 3 dB por abajo del valor de la banda de paso.

Bibliografía

[PIC, 2019] (2019). *PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family*. Microchip.

[Caprile, 2012] Caprile, S. (2012). *Desarrollo con microcontroladores ARM Cortex-M3*. Puntolibro.

[Cuéllar, 2008] Cuéllar, A. (2008). *Sistemas de Procesamiento Digital.* Delta Publicaciones.

[Valdes and Areny, 2007] Valdes, F. and Areny, R. (2007). *Microcontroladores Fundamentos y Aplicaciones con PIC*. Alfaomega. Marcombo. Marcombo.

Apéndice A

Hojas de Datos de la Familia PIC32MZ

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog

Operating Conditions

- 2.1V to 3.6V, -40ºC to +85ºC, DC to 252 MHz
- 2.1V to 3.6V, -40ºC to +125ºC, DC to 180 MHz

Core: 252 MHz (up to 415 DMIPS) M-Class

- 16 KB I-Cache, 4 KB D-Cache
- FPU for 32-bit and 64-bit floating point math
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating, and fractional math
  - IEEE 754-compliant
- Code-efficient (C and Assembly) architecture

Clock Management

- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timers (WDT) and Deadman Timer (DMT)
- Fast wake-up and start-up

Power Management

- Low-power modes (Sleep and Idle)
- Integrated Power-on Reset (POR) and Brown-out Reset (BOR)

Memory Interfaces

- 50 MHz External Bus Interface (EBI)
- 50 MHz Serial Quad Interface (SQI)

Audio and Graphics Interfaces

- Graphics interfaces: EBI or PMP
- Audio data communication: I^{2}S, LJ, and RJ
- Audio control interfaces: SPI and I^{2}C
- Audio master clock: Fractional clock frequencies with USB synchronization

High-Speed (HS) Communication Interfaces (with Dedicated DMA)

- USB 2.0-compliant Hi-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features

- Crypto Engine with RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
  - Peripheral and memory region access control

Direct Memory Access (DMA)

- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features

- 12-bit ADC module:
  - 18 Msps with up to six Sample and Hold (S&H) circuits (five dedicated and one shared)
  - Up to 48 analog inputs
  - Can operate during Sleep and Idle modes
  - Multiple trigger sources
  - Six Digital Comparators and six Digital Filters
- Two comparators with 32 programmable voltage references
- Temperature sensor with ±2ºC accuracy

Communication Interfaces

- Two CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
  - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as an additional SPI module (50 MHz)
- Five I^{2}C modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Timers/Output Compare/Input Capture

- Nine 16-bit or up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

Input/Output

- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, pull-downs, and slew rate controls
- External interrupts on all I/O pins
- PPS to enable function remap

Qualification and Class B Support

- AEC-Q100 REVH (Grade 1 -40ºC to +125ºC)
- Class B Safety Library, IEC 60730 (planned)
- Back-up internal oscillator

Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Software and Tools Support

- C/C++ compiler with native DSP/fractional and FPU support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™, and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micriμm® μC/OS™, and SEGGER embOS®

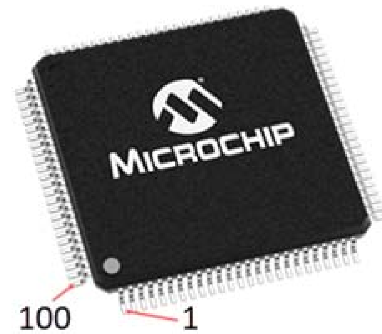
Packages

Type	QFN	TQFP				TFBGA		VTLA	LQFP
Pin Count	64	64	100		144	100	144	124	144
I/O Pins (up to)	53	53	78		120	78	120	98	120
Contact/Lead Pitch	0.50 mm	0.50 mm	0.40 mm	0.50 mm	0.40 mm	0.65 mm	0.50 mm	0.50 mm	0.50 mm
Dimensions	9x9x0.9 mm	10x10x1 mm	12x12x1 mm	14x14x1 mm	16x16x1 mm	7x7x1.2 mm	7x7x1.2 mm	9x9x0.9 mm	20x20x1.40 mm

TABLE 3: PIN NAMES FOR 100-PIN TQFP DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
1	AN23/AERXERR/RG15	36	VSS
2	EBIA5/AN34/PMA5/RA5	37	VDD
3	EBID5/AN17/RPE5/PMD5/RE5	38	TCK/EBIA19/AN29/RA1
4	EBID6/AN16/PMD6/RE6	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13
5	EBID7/AN15/PMD7/RE7	40	TDO/EBIA17/AN31/RPF12/RF12
6	EBIA6/AN22/RPC1/PMA6/RC1	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12
7	EBIA12/AN21/RPC2/PMA12/RC2	42	AN8/ERXD1/AECOL/RB13
8	EBIWE/AN20/RPC3/PMWR/RC3	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14
9	EBIOE/AN19/RPC4/PMRD/RC4	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	45	VSS
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	46	VDD
12	EBIA3/AN12/C2IND/ERXDV/ECRSDV/AERXDV/ AECRSDV/ RPG8/SCL4/PMA3/RG8	47	AN32/AETXD0/RPD14/RD14
13	VSS	48	AN33/AETXD1/RPD15/SCK6/RD15
14	VDD	49	OSC1/CLKI/RC12
15	MCLR	50	OSC2/CLKO/RC15
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/AERXCLK/ AER-EFCLK/RPG9/PMA2/RG9	51	VBUS
17	TMS/EBIA16/AN24/RA0	52	VUSB3V3
18	AN25/AERXD0/RPE8/RE8	53	VSS
19	AN26/AERXD1/RPE9/RE9	54	D-
20	AN45/C1INA/RPB5/RB5	55	D+
21	AN4/C1INB/RB4	56	RPF3/USBID/RF3
22	AN3/C2INA/RPB3/RB3	57	EBIRDY3/RPF2/SDA3/RF2
23	AN2/C2INB/RPB2/RB2	58	EBIRDY2/RPF8/SCL3/RF8
24	PGEC1/AN1/RPB1/RB1	59	EBICS0/SCL2/RA2
25	PGED1/AN0/RPB0/RB0	60	EBIRDY1/SDA2/RA3
26	PGEC2/AN46/RPB6/RB6	61	EBIA14/PMCS1/PMA14/RA4
27	PGED2/AN47/RPB7/RB7	62	VDD
28	VREF-/CVREF-/AN27/AERXD2/RA9	63	VSS
29	VREF+/CVREF+/AN28/AERXD3/RA10	64	EBIA9/RPF4/SDA5/PMA9/RF4
30	AVDD	65	EBIA8/RPF5/SCL5/PMA8/RF5
31	AVSS	66	AETXCLK/RPA14/SCL1/RA14
32	EBIA10/AN48/RPB8/PMA10/RB8	67	AETXEN/RPA15/SDA1/RA15
33	EBIA7/AN49/RPB9/PMA7/RB9	68	EBIA15/RPD9/PMCS2/PMA15/RD9
34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	69	RPD10/SCK4/RD10
35	AN6/ERXERR/AETXERR/RB11	70	EMDC/AEMDC/RPD11/RD11

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

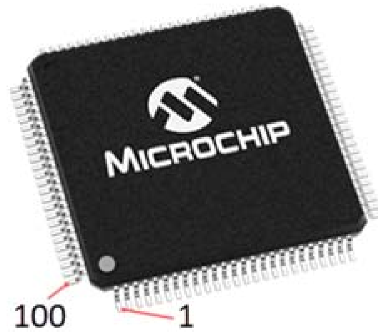
2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 3: PIN NAMES FOR 100-PIN TQFP DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
71	EMDIO/AEMDIO/RPD0/RTCC/INT0/RD0	86	EBID10/ETXD0/RPF1/PMD10/RF1
72	SOSCI/RPC13/RC13	87	EBID9/ETXERR/RPG1/PMD9/RG1
73	SOSCO/RPC14/T1CK/RC14	88	EBID8/RPG0/PMD8/RG0
74	VDD	89	TRCLK/SQICLK/RA6
75	VSS	90	TRD3/SQID3/RA7
76	RPD1/SCK1/RD1	91	EBID0/PMD0/RE0
77	EBID14/ETXEN/RPD2/PMD14/RD2	92	VSS
78	EBID15/ETXCLK/RPD3/PMD15/RD3	93	VDD
79	EBID12/ETXD2/RPD12/PMD12/RD12	94	EBID1/PMD1/RE1
80	EBID13/ETXD3/PMD13/RD13	95	TRD2/SQID2/RG14
81	SQICS0/RPD4/RD4	96	TRD1/SQID1/RG12
82	SQICS1/RPD5/RD5	97	TRD0/SQID0/RG13
83	VDD	98	EBID2/PMD2/RE2
84	VSS	99	EBID3/RPE3/PMD3/RE3
85	EBID11/ETXD1/RPF0/PMD11/RF0	100	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

© 2015-2019 Microchip Technology Inc.

1.0 DEVICE OVERVIEW

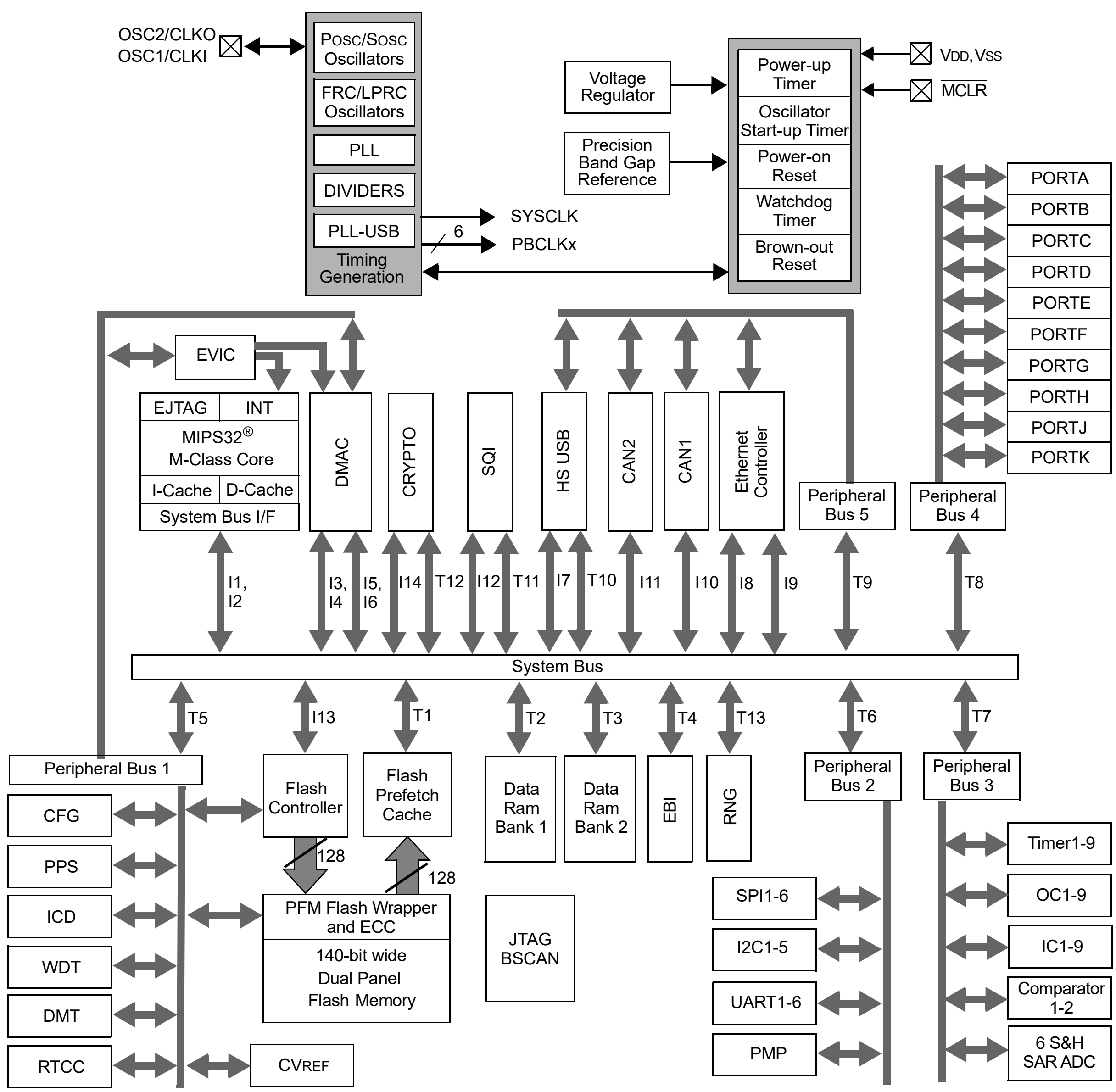
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This data sheet contains device-specific information for PIC32MZ EF devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EF family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 6).

FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MZ EF Family Features"** for the list of features by device.

© 2015-2019 Microchip Technology Inc.

19.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^{2}S)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

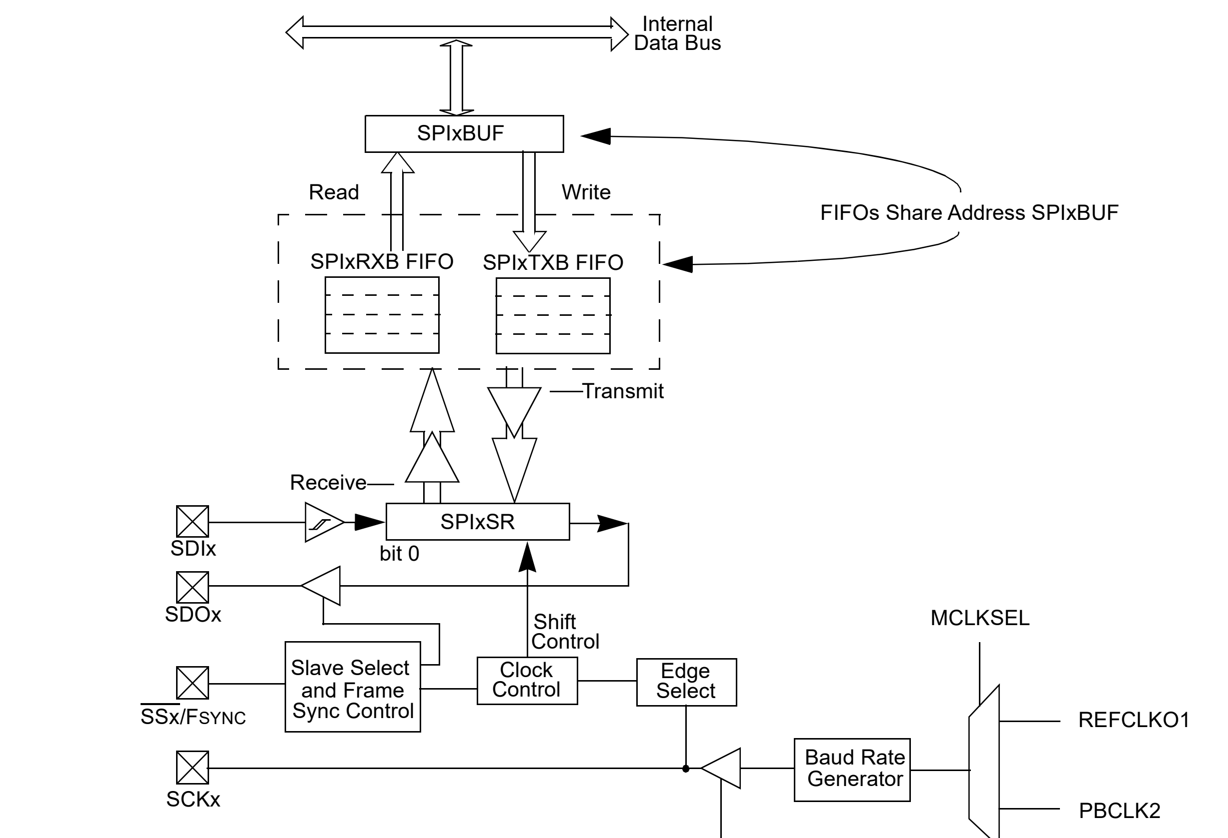
The SPI/I^{2}S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters, and so on.

The SPI/I^{2}S module is compatible with Motorola® SPI and SIOP interfaces.

The following are key features of the SPI module:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^{2}S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 19-1: SPI/I^{2}S MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

© 2015-2019 Microchip Technology Inc.

21.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note:	This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard.

Each I^2C module has a 2-pin interface:

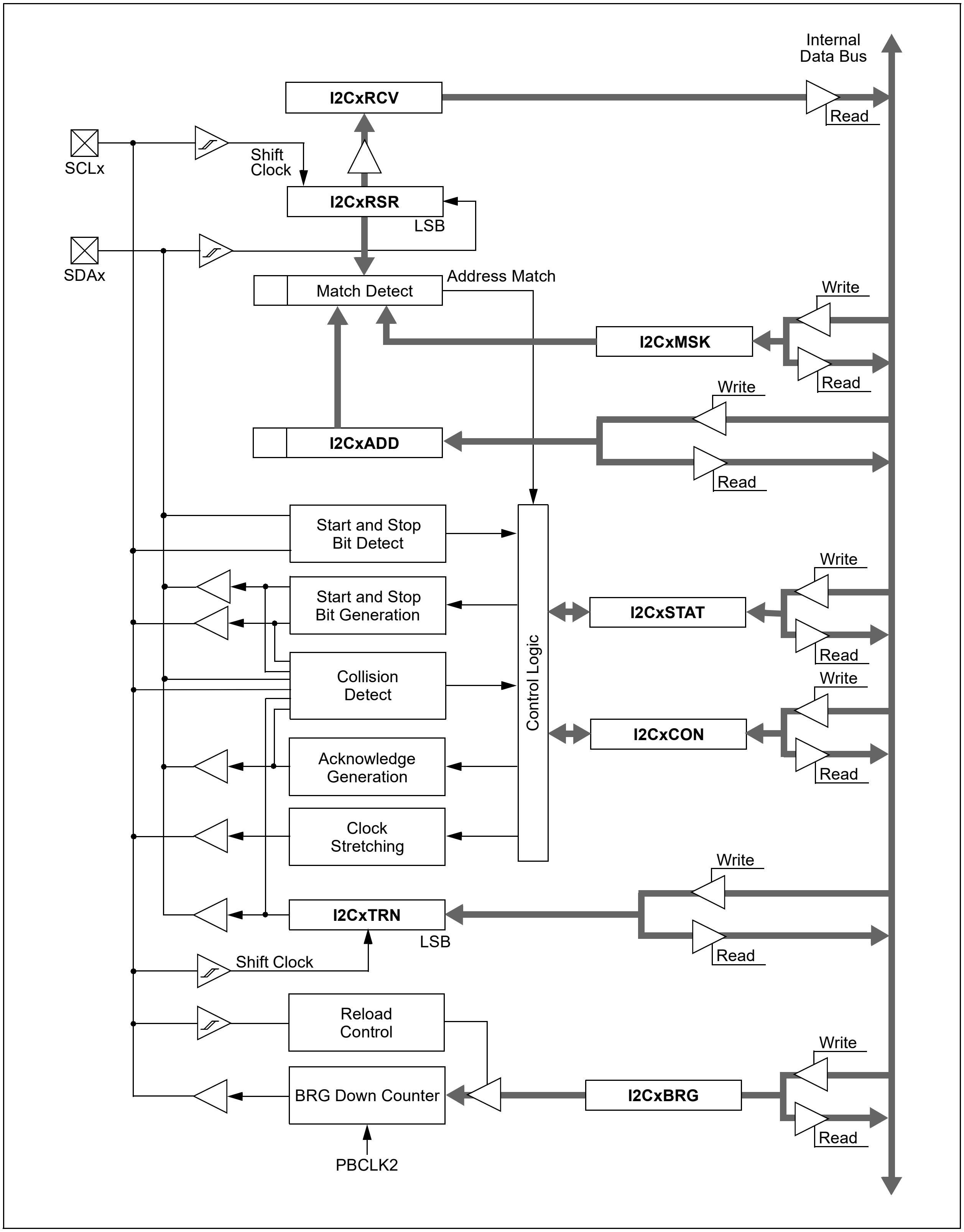
- SCLx pin is clock
- SDAx pin is data

Each I^2C module offers the following key features:

- I^2C interface supporting both master and slave operation
- I^2C Slave mode supports 7-bit and 10-bit addressing
- I^2C Master mode supports 7-bit and 10-bit addressing
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

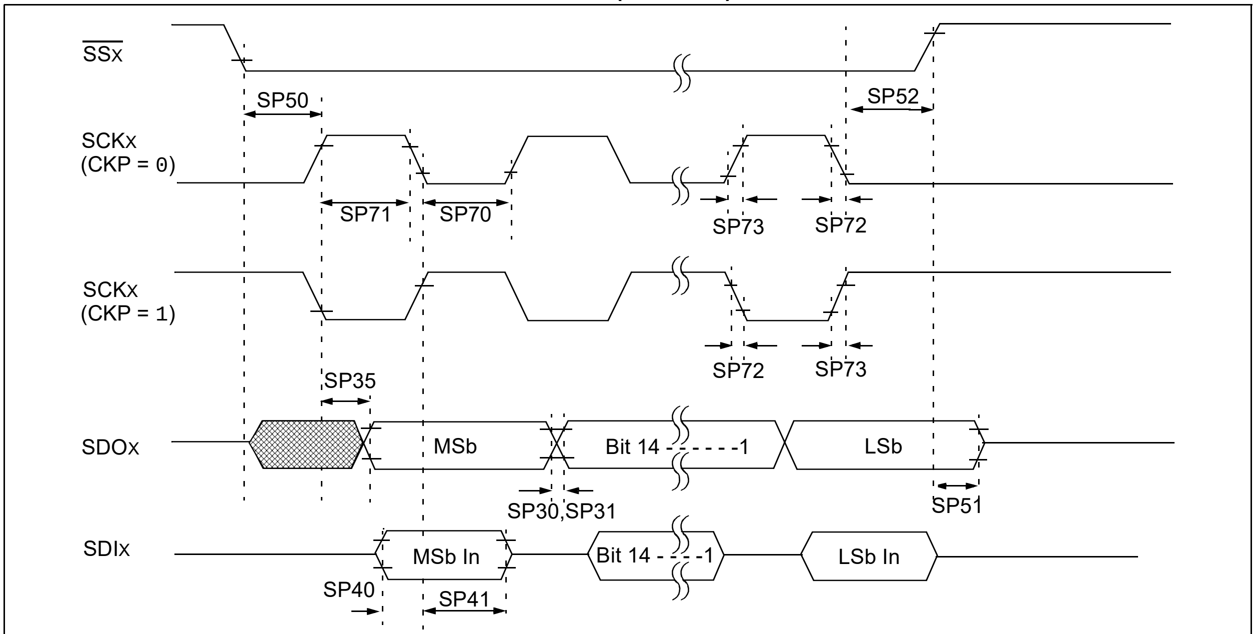
Figure 21-1 illustrates the I^2C module block diagram.

FIGURE 21-1: I^{2}C BLOCK DIAGRAM



© 2015-2019 Microchip Technology Inc.

FIGURE 37-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

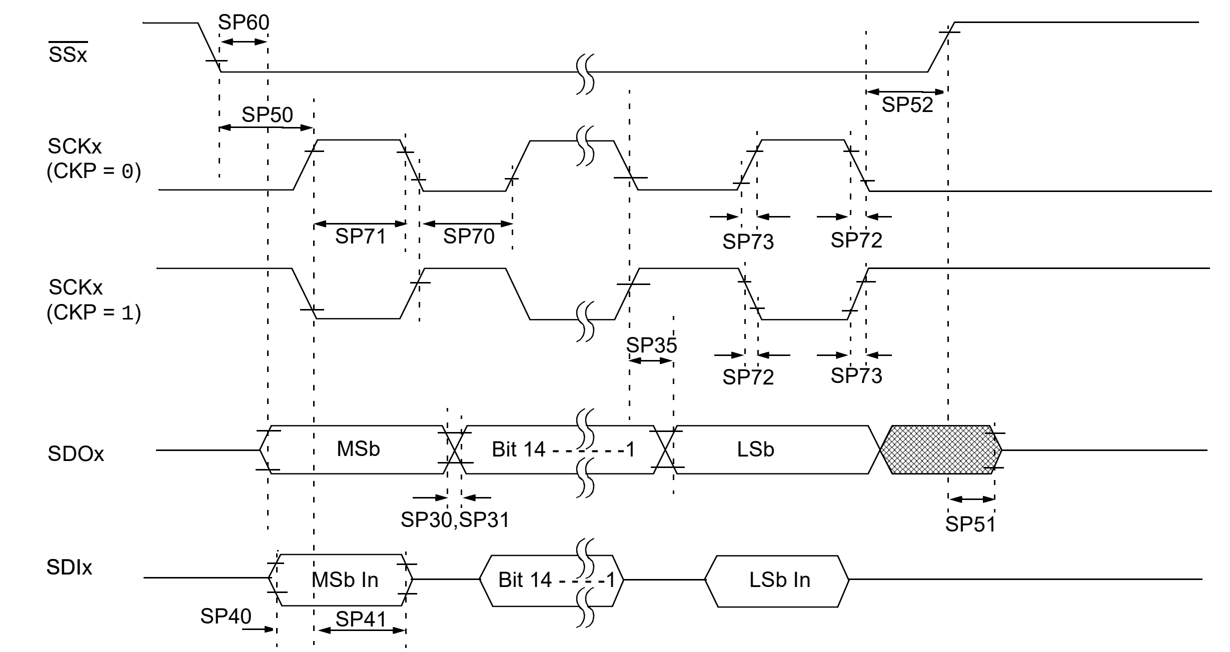
TABLE 37-32: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics(1)	Min.	Typ.(2)	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time **(Note 3)**	TSCK/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	TSCK/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance **(Note 3)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
3: The minimum clock period for SCKx is 20 ns.
4: Assumes 30 pF load on all SPIx pins.

© 2015-2019 Microchip Technology Inc.

FIGURE 37-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.7V
			—	—	15	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
3: The minimum clock period for SCKx is 20 ns.
4: Assumes 30 pF load on all SPIx pins.

© 2015-2019 Microchip Technology Inc.

TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

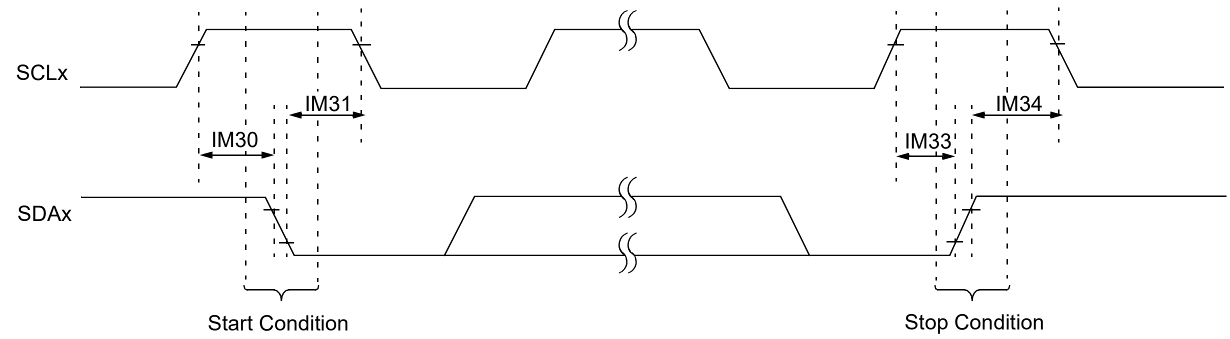
2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

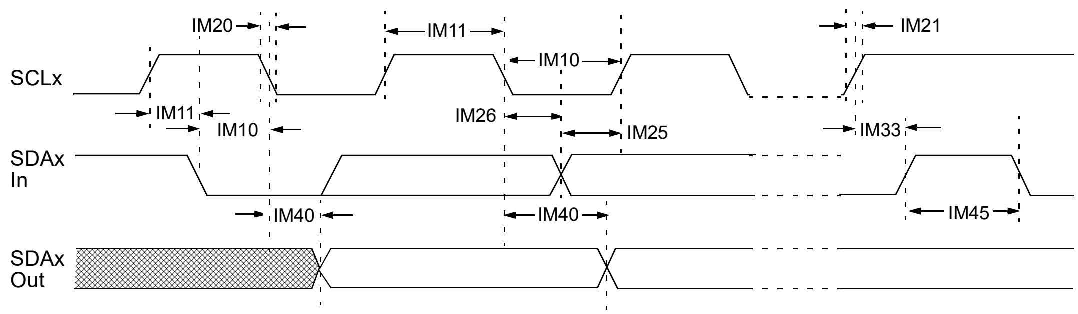
 © 2015-2019 Microchip Technology Inc.

FIGURE 37-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 37-1 for load conditions.

FIGURE 37-17: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				**Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	100	ns	

Note 1: BRG is the value of the I^2C Baud Rate Generator.
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).
3: The typical value for this parameter is 104 ns.

© 2015-2019 Microchip Technology Inc.

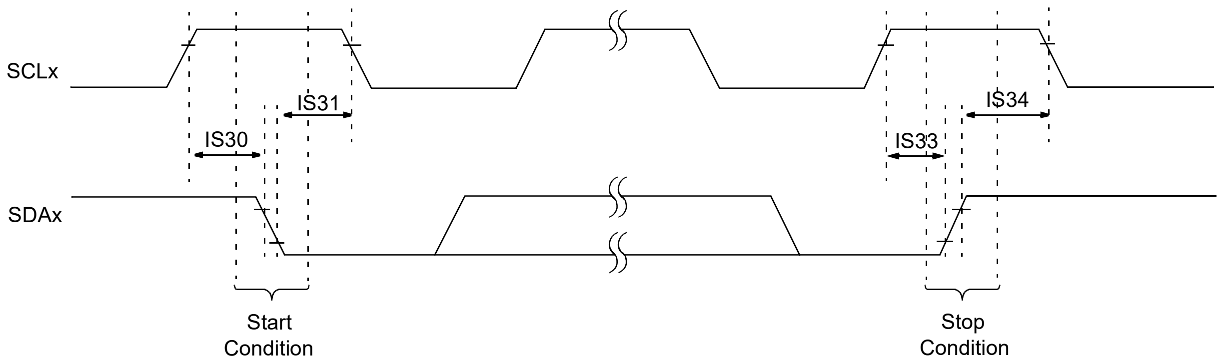
TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^{2}C Baud Rate Generator.
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).
3: The typical value for this parameter is 104 ns.

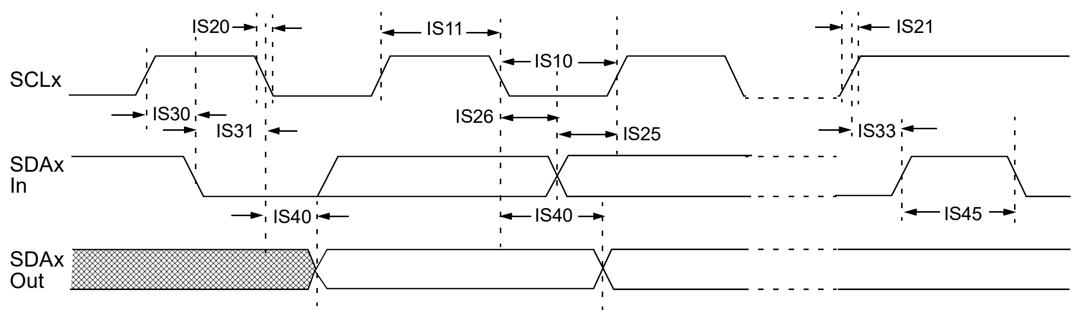
© 2015-2019 Microchip Technology Inc.

FIGURE 37-18: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 37-1 for load conditions.

FIGURE 37-19: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-36: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode **(Note 1)**	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode **(Note 1)**	0.5	—	μs	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

© 2015-2019 Microchip Technology Inc.

TABLE 37-36: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 1)**	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 1)**	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 1)**	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 1)**	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250		ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode **(Note 1)**	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 1)**	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

© 2015-2019 Microchip Technology Inc.

38.1 DC Characteristics

TABLE 38-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MZ EF Devices	
EDC5	2.1V-3.6V	-40°C to +125°C	180 MHz	—

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 38-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	Typical[3]	Maximum[6]	Units	Conditions
Operating Current (IDD)[1]				
EDC20	8	54	mA	4 MHz **(Note 4,5)**
EDC21	10	60	mA	10 MHz **(Note 5)**
EDC22	32	95	mA	60 MHz **(Note 2,4)**
EDC23	40	105	mA	80 MHz **(Note 2,4)**
EDC25	61	125	mA	130 MHz **(Note 2,4)**
EDC26	72	140	mA	160 MHz **(Note 2,4)**
EDC28	81	150	mA	180 MHz **(Note 2,4)**

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:
- Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), VUSB3V3 is connected to VSS
- CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to four
- L1 Cache and Prefetch modules are enabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

5: Note 2 applies with the following exceptions: L1 Cache and Prefetch modules are disabled, Program Flash memory Wait states are equal to seven.

6: Data in the "Maximum" column is at 3.3V, +125ºC at specified operating frequency. Parameters are for design guidance only and are not tested.

© 2015-2019 Microchip Technology Inc.

TABLE 38-3: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C for Extended	
Parameter No.	**Typical(2)**	**Maximum(4)**	**Units**	**Conditions**
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (Note 1)				
EDC30a	7	52	mA	4 MHz **(Note 3)**
EDC31a	8	56	mA	10 MHz
EDC32a	13	66	mA	60 MHz **(Note 3)**
EDC33a	21	86	mA	130 MHz **(Note 3)**
EDC34	26	96	mA	180 MHz **(Note 3)**

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}, PBCLKx divisor = 1:128 (‘x’ ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: Data in the “Maximum” column is at 3.3V, +125ºC at specified operating frequency. Parameters are for design guidance only and are not tested.

TABLE 38-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C for Extended		
Param. No.	**Typical(2)**	**Maximum(5)**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
EDC40m	20	46	mA	+125ºC	Base Power-Down Current
Module Differential Current					
EDC41e	15	50	µA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
EDC42e	25	50	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
EDC43d	3	3.8	mA	3.6V	ADC: ΔI_{ADC} **(Notes 3, 4)**
EDC44	15	50	µA	3.6V	Deadman Timer Current: ΔI_{DMT} **(Note 3)**

Note 1: The test conditions for I_{PD} current measurements are as follows:
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)

2: Data in the “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Voltage regulator is operational (VREGS = 1).

5: Data in the “Maximum” column is at 3.3V, +125ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

© 2015-2019 Microchip Technology Inc.

38.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

TABLE 38-5: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EOS51	FSYS	System Frequency	DC	—	180	MHz	USB module disabled
			30	—	180	MHz	USB module enabled
EOS55a	FPB	Peripheral Bus Frequency	DC	—	90	MHz	For PBCLKx, 'x' ≠ 4, 7
EOS55b			DC	—	180	MHz	For PBCLK4, PBCLK7
EOS56	FREF	Reference Clock Frequency	—	—	45	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

TABLE 38-6: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
EOS54a	FPLL	PLL Output Frequency Range	10	—	180	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

© 2015-2019 Microchip Technology Inc.

Apéndice B

Hojas de Datos del Medidor de Energía ADE7880

Polyphase Multifunction Energy Metering IC with Harmonic Monitoring

ADE7880

FEATURES

- Highly accurate; supports IEC 62053-21, IEC 62053-22, IEC 62053-23, EN 50470-1, EN 50470-3, ANSI C12.20, and IEEE1459 standards
- Supports IEC 61000-4-7 Class I and Class II accuracy specification
- Compatible with 3-phase, 3-wire or 4-wire (delta or wye), and other 3-phase services
- Supplies rms, active, reactive, and apparent powers, power factor, THD, and harmonic distortion of all harmonics within 2.8 kHz pass band on all phases
- Supplies rms and harmonic distortions of all harmonics within 2.8 kHz pass band on neutral current
- Less than 1% error in harmonic current and voltage rms, harmonic active and reactive powers over a dynamic range of 2000 to 1 at $T_A = 25°C$
- Supplies total (fundamental and harmonic) active and apparent energy and fundamental active/reactive energy on each phase and on the overall system
- Less than 0.1% error in active and fundamental reactive energy over a dynamic range of 1000 to 1 at $T_A = 25°C$
- Less than 0.2% error in active and fundamental reactive energy over a dynamic range of 5000 to 1 at $T_A = 25°C$
- Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at $T_A = 25°C$
- Battery supply input for missing neutral operation
- Wide supply voltage operation: 2.4 V to 3.7 V
- Reference: 1.2 V (drift 20 ppm/°C typical) with external overdrive capability
- 40-lead lead frame chip scale package (LFCSP), Pb-free, pin-for-pin compatible with ADE7854, ADE7858, ADE7868 and ADE7878

APPLICATIONS

- Energy metering systems
- Power quality monitoring
- Solar inverters
- Process monitoring
- Protective devices

GENERAL DESCRIPTION

The ADE7880[1] is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7880 device incorporates second-order sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all of the signal processing required to perform the total (fundamental and harmonic) active, and apparent energy measurements, rms calculations, as well as fundamental-only active and reactive energy measurements. In addition, the ADE7880 computes the rms of harmonics on the phase and neutral currents and on the phase voltages, together with the active, reactive and apparent powers, and the power factor and harmonic distortion on each harmonic for all phases. Total harmonic distortion (THD) is computed for all currents and voltages. A fixed function digital signal processor (DSP) executes this signal processing. The DSP program is stored in the internal ROM memory.

The ADE7880 is suitable for measuring active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services with, both, three and four wires. The ADE7880 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active powers, apparent powers, or the sum of the current rms values, and fundamental active and reactive powers.

The ADE7880 contains waveform sample registers that allow access to all ADC outputs. The devices also incorporate power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I²C, can be used to communicate with the ADE7880. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I²C to provide access to the ADC outputs and real-time power information. The ADE7880 also has two interrupt request pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, to indicate that an enabled interrupt event has occurred. Three specially designed low power modes ensure the continuity of energy accumulation when the ADE7880 is in a tampering situation. The ADE7880 is available in the 40-lead LFCSP, Pb-free package, pin-for-pin compatible with ADE7854, ADE7858, ADE7868, and ADE7878 devices.

[1] Protected by U.S. Patent 8,010,304 B2. Other patents pending.

Rev. C
Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2011–2014 Analog Devices, Inc. All rights reserved.

FUNCTIONAL BLOCK DIAGRAM

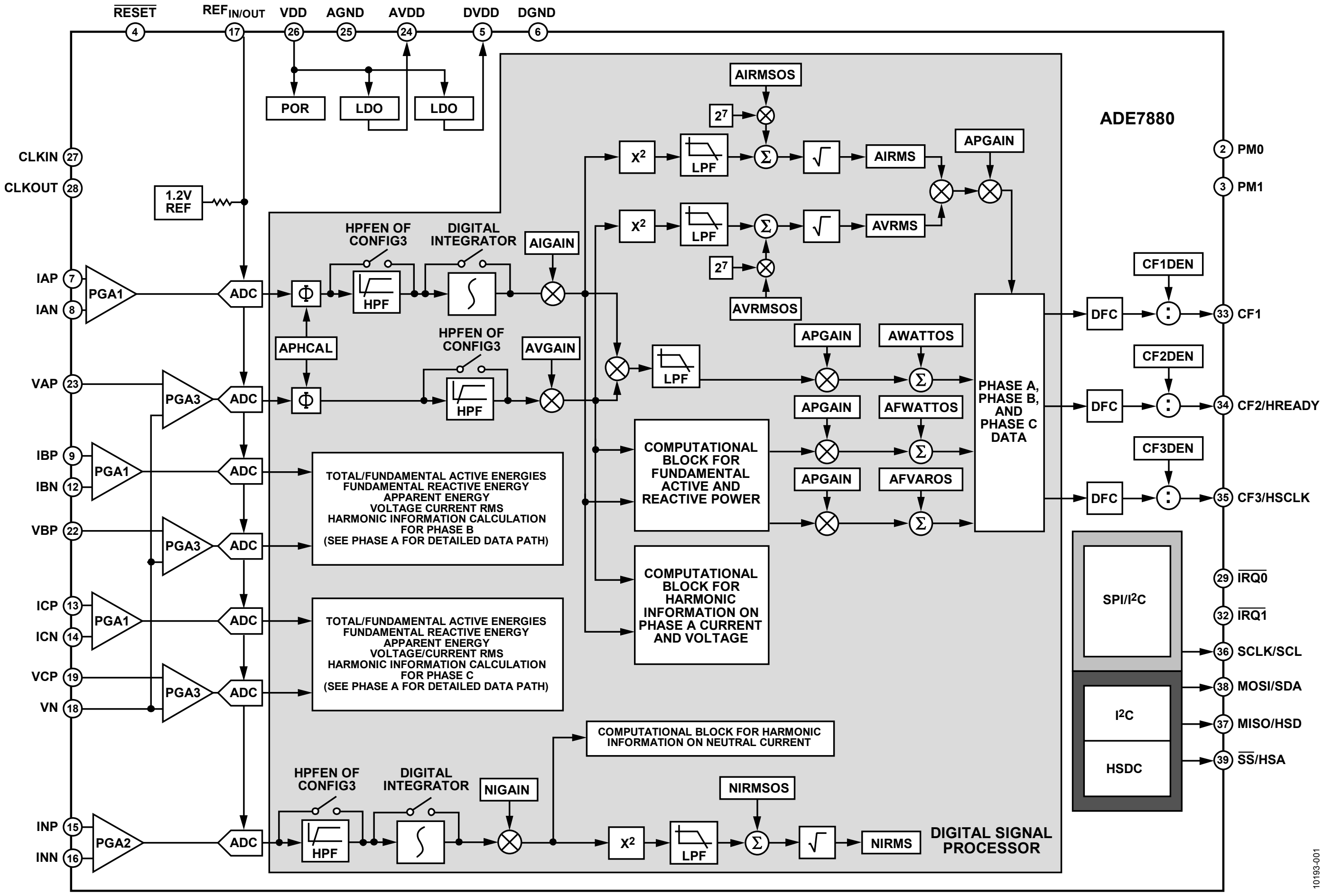


Figure 1. ADE7880 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT					
Active Energy Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 1
Fundamental Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 1
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth (−3 dB)		3.3		kHz	
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (per Phase)					
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 0, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 0
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 0
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IPx = VPx = ± 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Fundamental Reactive Energy Measurement Bandwidth (−3 dB)		3.3		kHz	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
RMS MEASUREMENTS (PSM0 Mode)					
I RMS and V RMS Measurement Bandwidth (−3 dB)		3.3		kHz	
I RMS and V RMS Measurement Error		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1
MEAN ABSOLUTE VALUE (MAV) MEASUREMENT (PSM1 Mode)					
I MAV Measurement Bandwidth		260		Hz	
I MAV Measurement Error		0.5		%	Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8
HARMONIC MEASUREMENTS					
Bandwidth (−3 dB)		3.3		kHz	
No attenuation Pass Band		2.8		kHz	
Fundamental Line Frequency, f_L	45		66	Hz	Voltage signal must have amplitudes greater than 100 mV peak at ADC stage. Set the SELFREQ bit of COMPMODE register based on the frequency. See the Managing Change in Fundamental Line Frequency section for details.
Maximum Number of Harmonics[3]			$\left\lfloor \frac{2800}{f_L} \right\rfloor$		
Absolute Maximum Number of Harmonics			63		
Harmonic RMS Measurement Error		1		%	Instantaneous reading accuracy over a dynamic range of 1000 to 1 for harmonics of frequencies within the pass band; after the initial 750 ms settling time; PGA = 1
					Accuracy over a dynamic range of 2000:1 for harmonics of frequencies within the pass band; average of 10 readings at 128 ms update rate, after the initial 750 ms setting time; PGA = 1
Harmonic Active/Reactive Power Measurement Error		1		%	Instantaneous reading accuracy over a dynamic range of 1000 to 1 for harmonics of frequencies within the pass band; after the initial 750 ms settling time; PGA = 1
					Accuracy over a dynamic range of 2000:1 for harmonics of frequencies within the pass band; average of 5 readings at 128 ms update rate, after the initial 750 ms setting time; PGA = 1
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	PGA = 1, differential or single-ended inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, INP and INN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP and VN
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins	490			kΩ	
VN Pin	170			kΩ	
ADC Offset		−35		mV	PGA = 1, uncalibrated error, see the Terminology section. Scales inversely proportional to the other PGA gains
Gain Error		±4		%	External 1.2 V reference

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		72		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz, see the Terminology section
Signal-to-Noise-and-Distortion Ratio, SINAD		72		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz, see the Terminology section
Bandwidth (−3 dB)		3.3		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		68.818		kHz	WTHR = VARTHR = VATHR = 3
Duty Cycle		50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1
		(1 + 1/CFDEN) × 50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1
Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 1.2 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
PSM0 and PSM1 Modes					
Temperature Coefficient	−50	±20	+50	ppm/°C	Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details
CLKIN					See the Crystal Circuit section for more details
Input Clock Frequency	16.22	16.384	16.55	MHz	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$, $\overline{RESET}$, PM0, AND PM1					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V
Input Current, I_{IN}			82	nA	Input = VDD = 3.3 V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V
Input Current, I_{IN}			−7.3	μA	Input = 0, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, AND MISO/HSD					VDD = 3.3 V
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE} = 800 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 500 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 8 mA
POWER SUPPLY					For specified performance
PSM0 Mode					
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		25	28	mA	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
PSM1 and PSM2 Modes					
VDD Pin	2.4		3.7	V	
I_{DD}					
PSM1 Mode		5.3	5.8	mA	
PSM2 Mode		0.2	0.27	mA	
PSM3 Mode					For specified performance
VDD Pin	2.4		3.7	V	
I_{DD} in PSM3 Mode		1.8	6	µA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] $\left[\frac{2800}{f_L}\right]$ means the whole number of the division.

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams (see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions).

Table 2. I²C-Compatible Interface Timing Parameter

		Standard Mode		Fast Mode		
Parameter	Symbol	Min	Max	Min	Max	Unit
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-Up Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0.1	3.45	0.1	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

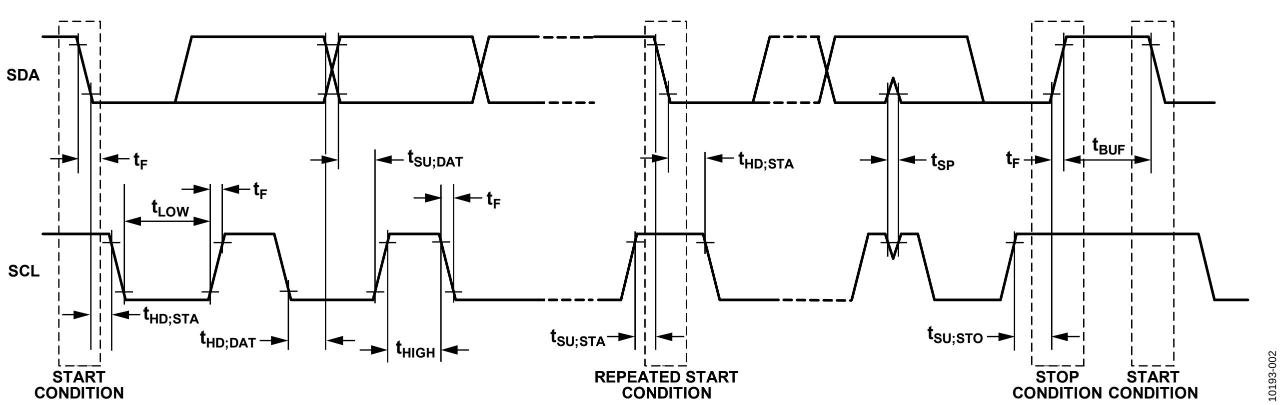


Figure 2. I²C-Compatible Interface Timing

Table 3. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	μs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

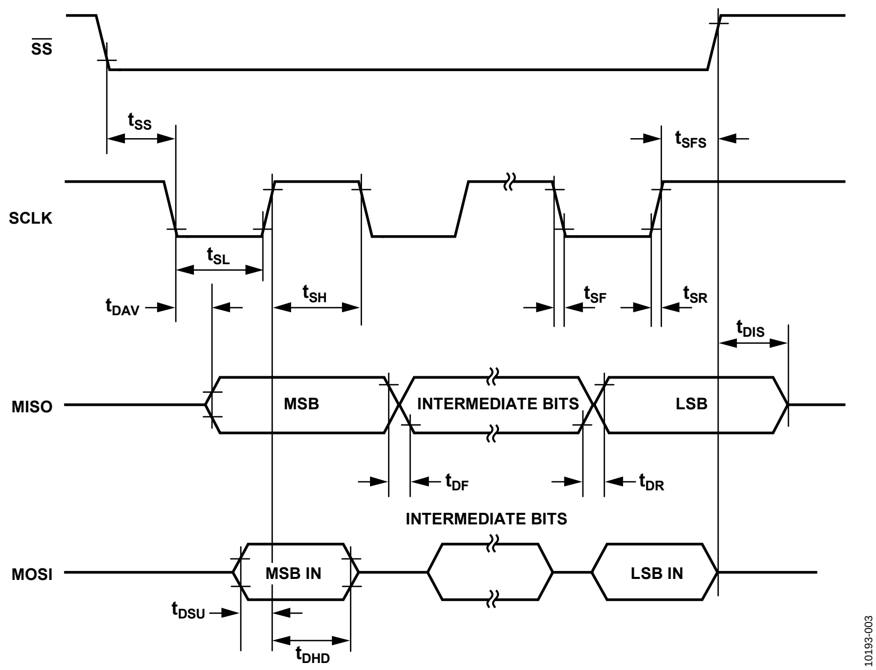


Figure 3. SPI Interface Timing

Table 4. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

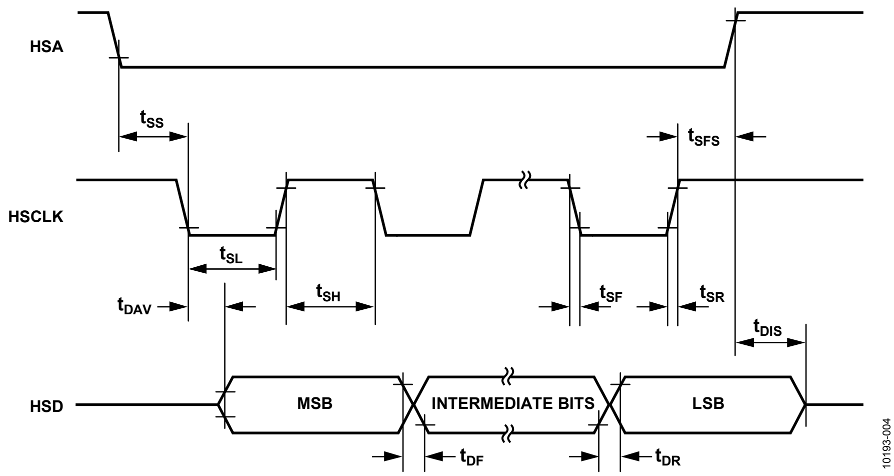


Figure 4. HSDC Interface Timing

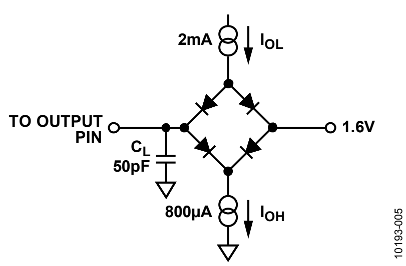


Figure 5. Load Circuit for Timing Specifications

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

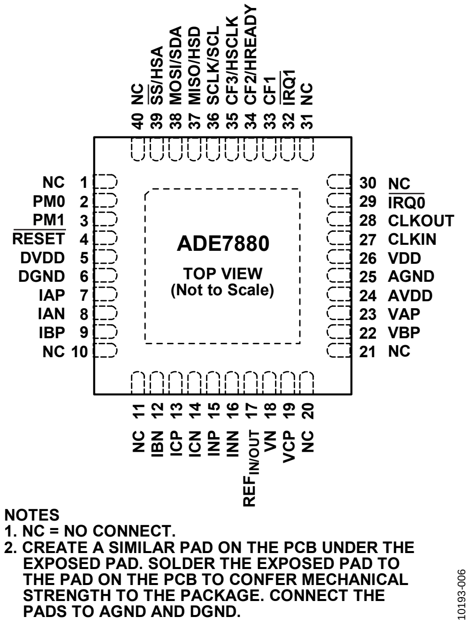


Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. Do not connect to these pins. These pins are not connected internally.
2	PM0	Power Mode Pin 0. This pin, combined with PM1, defines the power mode of the ADE7880, as described in Table 8.
3	PM1	Power Mode Pin 1. This pin defines the power mode of the ADE7880 when combined with PM0, as described in Table 8.
4	$\overline{\text{RESET}}$	Reset Input, Active Low. In PSM0 mode, this pin must stay low for at least 10 µs to trigger a hardware reset.
5	DVDD	2.5 V Output of the Digital Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7, 8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this data sheet as Current Channel A. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel B and Channel C.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this data sheet as Current Channel B. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel C and Channel A.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this data sheet as Current Channel C. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel A and Channel B.
15, 16	INP, INN	Analog Inputs for Neutral Current Channel N. This channel is used with the current transducers and is referenced in this data sheet as Current Channel N. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA, different from the ones found on the A, B, and C channels.
17	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled.

Pin No.	Mnemonic	Description
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this data sheet. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. This channel also has an internal PGA.
24	AVDD	2.5 V Output of the Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 μF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage. In PSM0 (normal power mode), maintain the supply voltage at 3.3 V ± 10% for specified operation. In PSM1 (reduced power mode), PSM2 (low power mode), and PSM3 (sleep mode), when the ADE7880 is supplied from a battery, maintain the supply voltage between 2.4 V and 3.7 V. Decouple this pin to DGND with a 10 μF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT-cut crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7880. The clock frequency for specified operation is 16.384 MHz. Use ceramic load capacitors of a few tens of picofarad with the gate oscillator circuit. Refer to the data sheet of the crystal manufacturer for load capacitance requirements.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as previously described with Pin 27 in this table) to provide a clock source for the ADE7880.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
33, 34, 35	CF1, CF2/HREADY, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, and CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). CF2 is multiplexed with the HREADY signal generated by the harmonic calculations block. CF3 is multiplexed with the serial clock output of the HSDC port.
36	SCLK/SCL	Serial Clock Input for SPI Port/Serial Clock Input for I²C Port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
37	MISO/HSD	Data Out for SPI Port/Data Out for HSDC Port.
38	MOSI/SDA	Data In for SPI Port/Data Out for I²C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

TEST CIRCUIT

In Figure 32, the PM1 and PM0 pins are pulled up internally to VDD. Select the mode of operation by using a microcontroller to programmatically change the pin values. See the Power Management section for details.

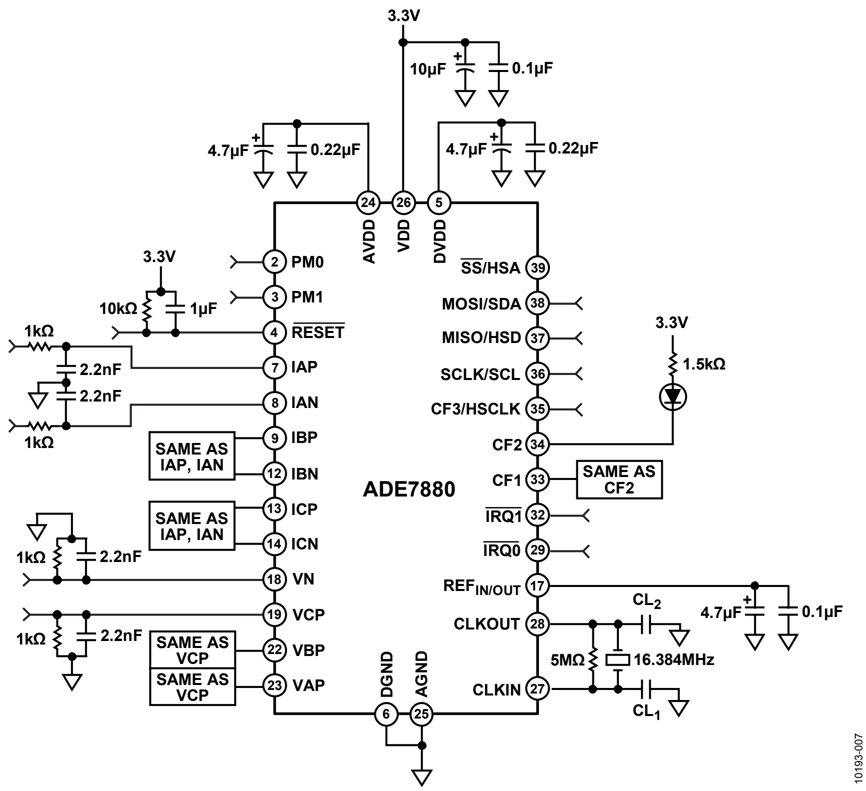


Figure 32. Test Circuit

Table 11. Recommended Actions When Changing Power Modes

Initial Power Mode	Before Setting Next Power Mode	Next Power Mode			
		PSM0	**PSM1**	**PSM2**	**PSM3**
PSM0	Stop DSP by setting the Run register = 0x0000 Disable HSDC by clearing Bit 6 (HSDCEN) to 0 in the CONFIG register Mask interrupts by setting MASK0 = 0x0 and MASK1 = 0x0 Erase interrupt status flags in the STATUS0 and STATUS1 registers		Current mean absolute values (mav) computed immediately xIMAV registers can be accessed immediately	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	No action necessary
PSM1	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1		Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	No action necessary
PSM2	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1	Wait until the $\overline{\text{IRQ1}}$ pin triggered low Current mean absolute values compute at this moment xIMAV registers may be accessed from this moment		No action necessary
PSM3	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Current mav circuit begins computations at this time xIMAV registers can be accessed from this moment	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	

POWER-UP PROCEDURE

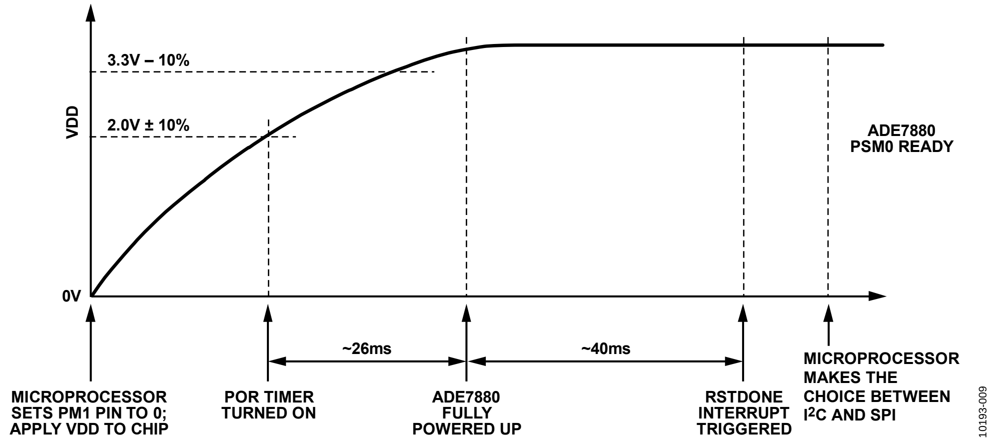


Figure 35. Power-Up Procedure

The ADE7880 contains an on-chip power supply monitor that supervises the power supply (VDD). At power-up, the device is inactive until VDD reaches 2.0 V ± 10%. When VDD crosses this threshold, the power supply monitor keeps the device in the inactive state for an additional 26 ms to allow VDD to rise to 3.3 V – 10%, the minimum recommended supply voltage.

The PM0 and PM1 pins have internal pull-up resistors, but it is necessary to set the PM1 pin to Logic 0, either through a microcontroller or by grounding the PM1 pin externally, before powering up the chip. The PM0 pin can remain open as it is held high, due to the internal pull-up resistor. This ensures that the ADE7880 always powers up in PSM0 (normal) mode. The time from the chip being powered up completely to all functionality being enabled is about 40 ms (see Figure 35). It is necessary to ensure that the $\overline{\text{RESET}}$ pin is held high during the entire power-up procedure.

If PSM0 mode is the only desired power mode, the PM1 pin can be tied to ground externally. When the ADE7880 enters PSM0 mode, the I2C port is the active serial port. To use the SPI port, toggle the $\overline{\text{SS}}$/HSA pin three times from high to low.

To lock I2C as the active serial port, set Bit 1 (I2C_LOCK) of the CONFIG2 register to 1. From this moment, the device ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and a switch to the SPI port is no longer possible.

If SPI is the active serial port, any write to the CONFIG2 register locks the port, and a switch to the I2C port is no longer possible. To use the I2C port, the ADE7880 must be powered down or the device must be reset by setting the $\overline{\text{RESET}}$ pin low. After the serial port is locked, the serial port selection is maintained when the device changes from one PSMx power mode to another.

Immediately after entering PSM0 mode, all registers in the ADE7880 are set to their default values, including the CONFIG2 and LPOILVL registers.

The ADE7880 signals the end of the transition period by pulling the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is cleared to 0 during the transition period and is set to 1 when the transition ends. Writing the STATUS1 register with the RSTDONE bit set to 1 clears the status bit and returns the $\overline{\text{IRQ1}}$ pin high. Because RSTDONE is an unmaskable interrupt, Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. Wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. At this point, as a good programming practice, cancel all other status flags in the STATUS1 and STATUS0 registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode and, therefore, does not execute any instructions. This is the moment to initialize all registers in the ADE7880. See the Digital Signal Processor section for the proper procedure to initialize all registers and start the metering.

If the supply voltage, VDD, falls lower than 2.0 V ± 10%, the ADE7880 enters an inactive state, which means that no measurements or computations are executed.

If the $\overline{\text{RESET}}$ pin is held low while the IC powers up or if the power-up sequence timing cannot be maintained as per Figure 35, perform the following sequence of write operations prior to starting the DSP (setting the RUN register to 0x01), to ensure that the modulators are reset properly.

1. 8-bit write: 0xAD is written at Address 0xE7FE.
2. 8-bit write: 0x14 is written at Address 0xE7E2.
3. Wait 200 µs.
4. 8-bit write: 0xAD is written at Address 0xE7FE.
5. 8-bit write: 0x04 is written at Address 0xE7E2.

to 750 ms, the settling time of the harmonic calculations. Other possible values are 500 ms (HSTIME = 00), 1 sec (10) and 1250 ms (11).

The second approach, enabled when Bit 0 (HRCFG) of HCONFIG register is set to 1, sets Bit 19 (HREADY) in STATUS0 register to 1 every time the harmonic calculations are updated at the update frequency determined by HRATE bits without waiting for the harmonic calculations to settle. This allows an external microcontroller to access the harmonic calculations immediately after they have been started. If the corresponding mask bit in the MASK0 interrupt mask register is enabled, the $\overline{\text{IRQ}}$ pin also goes active low. The status bit is cleared and the pin $\overline{\text{IRQ}}$ is set to high again by writing to the STATUS0 register with the corresponding bit set to 1.

Additionally, the ADE7880 provides a periodical output signal called HREADY at the CF2/HREADY pin synchronous to the moment the harmonic calculations are updated in the harmonic registers. This functionality is chosen if Bit 2 (CF2DIS) is set to 1 in the CONFIG register. If CF2DIS is set to 0 (default value), the CF2 energy to frequency converter output is provided at CF2/HREADY pin. The default state of this signal is high. Every time the harmonic registers are updated based on HRATE bits in HCONFIG register, the signal HREADY goes low for approximately 10 µs and then goes back high. If Bit 0 (HRCFG) in the HCONFIG register is set to 1, the HREADY bit in the STATUS0 register is set to 1 every HRATE period right after the harmonic calculations start, and the HREADY signal toggles high, low, and back synchronously. If the HRCFG bit is set to 0, the HREADY bit in the STATUS0 register is set to 1 after the HSTIME period, and the HREADY signal toggles high, low and back synchronously. The HREADY signal allows fast access to the harmonic registers without having to use HREADY interrupt in MASK0 register.

In order to facilitate the fast reading of the registers in which the harmonic calculations are stored, a special burst registers reading has been implemented in the serial interfaces. See the I²C Read Operation of Harmonic Calculations Registers and the SPI Read Operation sections for details.

Recommended Approach to Managing Harmonic Calculations

The recommended approach to managing the ADE7880 harmonic calculations is the following:

- Set up Bit 2 (CF2DIS) in the CONFIG register. Set the CF2DIS bit to 1 to use the CF2/HREADY pin to signal when the harmonic calculations have settled and are updated. The high to low transition of HREADY signal indicates when to read the harmonic registers. Use the burst reading mode to read the harmonic registers as it is the most efficient way to read them.
- Choose the harmonics to be monitored by setting HX, HY and HZ appropriately.
- Select all the HCONFIG register bits.
- Initialize the gain registers used in the harmonic calculations. Leave the offset registers to 0.
- Read the registers in which the harmonic information is stored using the burst or regular reading mode at high to low transitions of CF2/HREADY pin.

WAVEFORM SAMPLING MODE

The waveform samples of the current and voltage waveform, the active, reactive, and apparent power outputs are stored every 125 µs (8 kHz rate) into 24-bit signed registers that can be accessed through various serial ports of the ADE7880. Table 22 provides a list of registers and their descriptions.

Table 22. Waveform Registers List

Register	Description
IAWV	Phase A current
VAWV	Phase A voltage
IBWV	Phase B current
VBWV	Phase B voltage
ICWV	Phase C current
VCWV	Phase C voltage
INWV	Neutral current
AVA	Phase A apparent power
BVA	Phase B apparent power
CVA	Phase C apparent power
AWATT	Phase A active power
BWATT	Phase B active power
CWATT	Phase C active power

Bit 17 (DREADY) in the STATUS0 register can be used to signal when the registers listed in Table 22 can be read using I²C or SPI serial ports. An interrupt attached to the flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. (see the Digital Signal Processor section for more details on Bit DREADY).

The ADE7880 contains a high speed data capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. Read the HSDC Interface section for more details.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. All registers listed in Table 22 are transmitted signed extended from 24 bits to 32 bits (see Figure 45).

ENERGY-TO-FREQUENCY CONVERSION

The ADE7880 provides three frequency output pins: CF1, CF2, and CF3. The CF2 pin is multiplexed with the HREADY pin of the harmonic calculations block. When HREADY is enabled, the CF2 functionality is disabled at the pin. The CF3 pin is multiplexed with the HSCLK pin of the HSDC interface. When HSDC is enabled, the CF3 functionality is disabled at the pin. The CF1 pin and the CF2 pin are always available. After initial calibration at manufacturing, the manufacturer or end customer verifies the energy meter calibration. One convenient way to verify the meter calibration is to provide an output frequency proportional to

I²C-Compatible Interface

The ADE7880 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400 kHz.

The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system. Note that the ADE7880 requires a minimum of 100 ns hold time for I²C communication. Refer to the $t_{HD;DAT}$ specification in Table 2.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition, and the bus becomes idle.

I²C Write Operation

The write operation using the I²C interface of the ADE7880 initiate when the master generates a start condition and consists in one byte representing the address of the ADE7880 followed by the 16-bit address of the target register and by the value of the register.

The most significant seven bits of the address byte constitute the address of the ADE7880 and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a write operation, it has to be cleared to 0; therefore, the first byte of the write operation is 0x70. After every byte is received, the ADE7880 generates an acknowledge. As registers can have 8, 16, or 32 bits, after the last bit of the register is transmitted and the ADE7880 acknowledges the transfer, the master generates a stop condition. The addresses and the register content are sent with the most significant bit first. See Figure 103 for details of the I²C write operation.

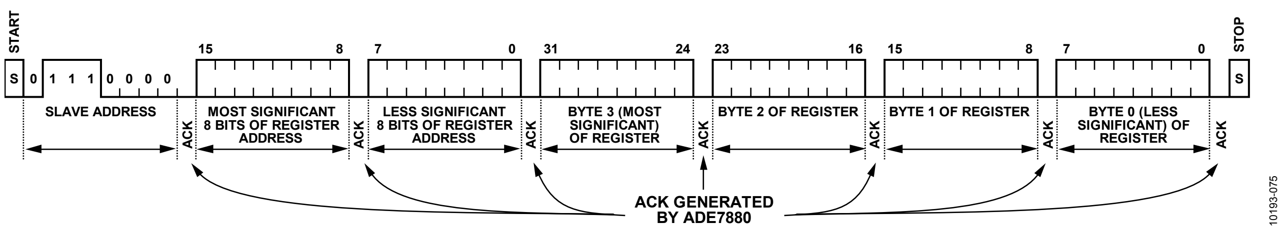


Figure 103. I²C Write Operation of a 32-Bit Register

I²C Read Operation

The read operation using the I²C interface of the ADE7880 is accomplished in two stages. The first stage sets the pointer to the address of the register. The second stage reads the content of the register.

As seen in Figure 104, the first stage initiates when the master generates a start condition and consists in one byte representing the address of the ADE7880 followed by the 16-bit address of the target register. The ADE7880 acknowledges every byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (see the I²C Write Operation section for details). After the last byte of the register address is sent and acknowledged by the ADE7880, the second stage begins with the master generating a new start condition followed by an address byte. The most significant seven bits of this address byte constitute the address of the ADE7880, and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a read operation, it must be set to 1; thus, the first byte of the read operation is 0x71. After this byte is received, the ADE7880 generates an acknowledge. Then, the ADE7880 sends the value of the register, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. Because registers can have 8, 16, or 32 bits, after the last bit of the register is received, the master does not acknowledge the transfer but generates a stop condition.

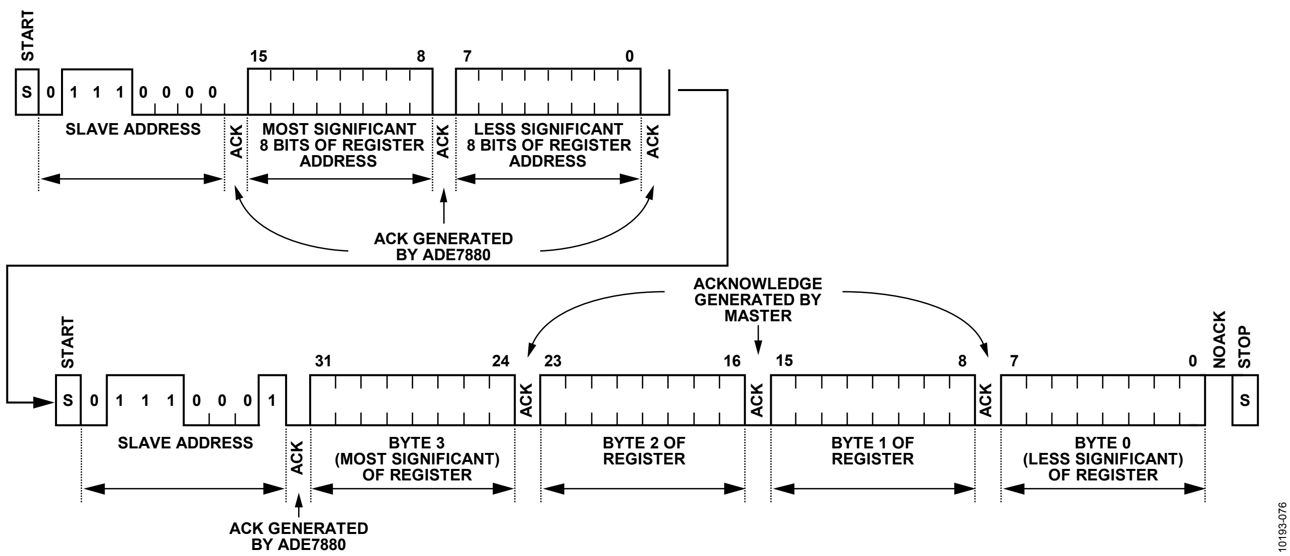


Figure 104. I²C Read Operation of a 32-Bit Register

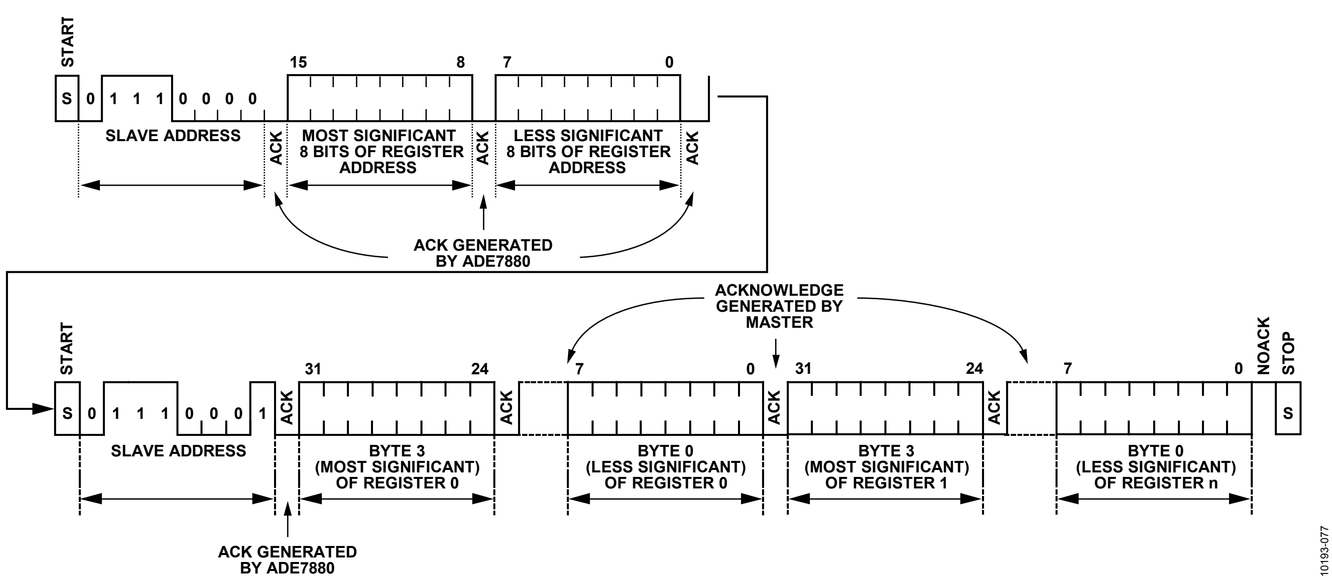


Figure 105. I²C Read Operation of n 32-Bit Harmonic Calculations Registers

I²C Read Operation of Harmonic Calculations Registers

The registers containing the harmonic calculation results are located starting at Address 0xE880 and are all 32-bit width. They can be read in two ways: one register at a time (see the I²C Read Operation section for details) or multiple consecutive registers at a time in a burst mode. This burst mode is accomplished in two stages. As seen in Figure 105, the first stage sets the pointer to the address of the register and is identical to the first stage executed when only one register is read. The second stage reads the content of the registers. The second stage begins with the master generating a new start condition followed by an address byte equal to the address byte used when one single register is read, 0x71. After this byte is received, the ADE7880 generates an acknowledge. Then, the ADE7880 sends the value of the first register located at the pointer, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. After the bytes of the first register are sent, if the master acknowledges the last byte, the ADE7880 increments the pointer by one location to position it at the next register and begins to send it out byte by byte, most significant bit first. If the master acknowledges the last byte, the ADE7880 increments the pointer again and begins to send data from the next register. The process continues until the master ceases to generate an acknowledge at the last byte of the register and then generates a stop condition. It is recommended to not allow locations greater than 0xE89F, the last location of the harmonic calculations registers.

SPI-Compatible Interface

The SPI of the ADE7880 is always a slave of the communication and consists of four pins (with dual functions): SCLK/SCL, MOSI/SDA, MISO/HSD, and $\overline{\text{SS}}$/HSA. The functions used in the SPI-compatible interface are SCLK, MOSI, MISO, and $\overline{\text{SS}}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7880 at the MOSI logic input on the falling edge of SCLK and the ADE7880 samples it on the rising edge of SCLK. Data shifts out of the ADE7880 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum serial clock frequency supported by this interface is 2.5 MHz. MISO stays in high impedance when no data is transmitted from the ADE7880. See Figure 106 for details of the connection between the ADE7880 SPI and a master device containing an SPI interface.

The $\overline{\text{SS}}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. Drive the $\overline{\text{SS}}$ input low for the entire data transfer operation. Bringing $\overline{\text{SS}}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{\text{SS}}$ logic input to low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, verify its value by reading it back. The protocol is similar to the protocol used in I²C interface.

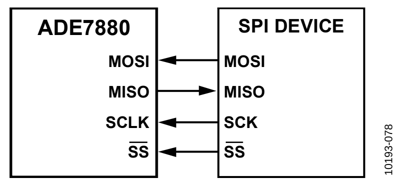


Figure 106. Connecting ADE7880 SPI with an SPI Device

SPI Read Operation

The read operation using the SPI interface of the ADE7880 initiates when the master sets the $\overline{\text{SS}}$/HSA pin low and begins sending one byte, representing the address of the ADE7880, on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7880 samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, it is recommended they be different from 0111000b, the seven bits used in the I²C protocol. Bit 0 (read/$\overline{\text{write}}$) of the address byte must be 1 for a read operation. Next, the master sends the 16-bit address of the register that is read. After the ADE7880 receives the last bit of address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit, it sets the $\overline{\text{SS}}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 107 for details of the SPI read operation.

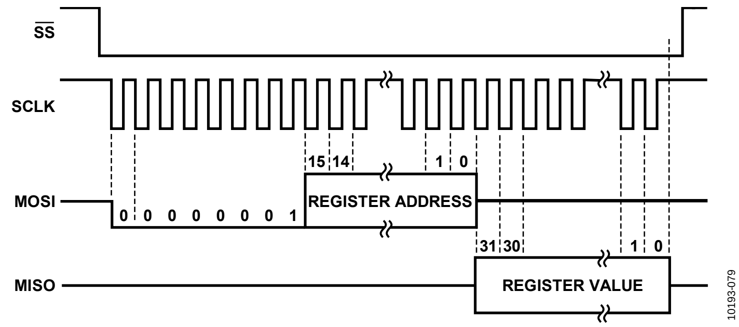


Figure 107. SPI Read Operation of a 32-Bit Register

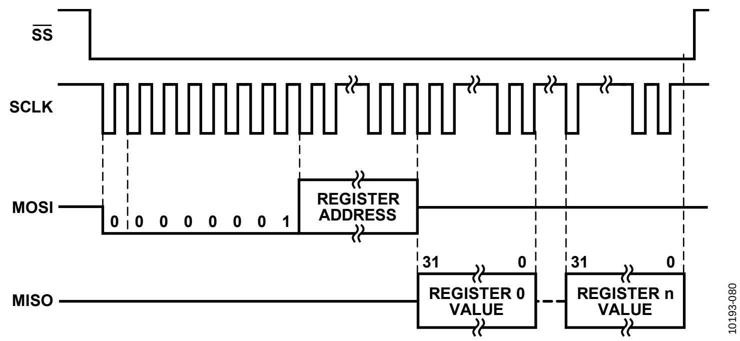


Figure 108. SPI Read Operation of n 32-Bit Harmonic Calculations Registers

SPI Read Operation of Harmonic Calculations Registers

The registers containing the harmonic calculation results are located starting at Address 0xE880 and are all 32-bit width. They can be read in two ways: one register at a time (see the SPI Read Operation section for details) or multiple consecutive registers at a time in a burst mode. The burst mode initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7880, on the MOSI line. The address is the same address byte used for reading only one register. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7880 samples data on the low-to-high transitions of SCLK. Next, the master sends the 16-bit address of the first harmonic calculations register that is read. After the ADE7880 receives the last bit of the address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit of the first register, the ADE7880 sends the harmonic calculations register placed at the next location and so forth until the master sets the $\overline{SS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 108 for details of the SPI read operation of harmonic calculations registers.

SPI Write Operation

The write operation using the SPI interface of the ADE7880 initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte representing the address of the ADE7880 on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7880 samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, it is recommended they be different from 0111000b, the seven bits used in the I^{2}C protocol. Bit 0 (read/$\overline{\text{write}}$) of the address byte must be 0 for a write operation. Next, the master sends the 16-bit address of the register that is written and the 32-, 16-, or 8-bit value of that register without losing any SCLK cycle. After the last bit is transmitted, the master sets the $\overline{SS}$ and SCLK lines high at the end of the SCLK cycle and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 109 for details of the SPI write operation.

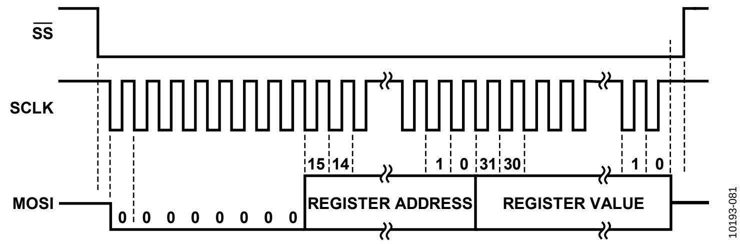


Figure 109. SPI Write Operation of a 32-Bit Register

HSDC Interface

The high speed data capture (HSDC) interface is disabled after default. It can be used only if the ADE7880 is configured with an I^2C interface. The SPI interface of ADE7880 cannot be used at the same time with HSDC.

Bit 6 (HSDCEN) in the CONFIG register activates HSDC when set to 1. If Bit HSDCEN is cleared to 0, the default value, the HSDC interface is disabled. Setting Bit HSDCEN to 1 when SPI is in use does not have any effect. HSDC is an interface for sending to an external device (usually a microprocessor or a DSP) up to sixteen 32-bit words. The words represent the instantaneous values of the phase currents and voltages, neutral current, and active, reactive, and apparent powers. The registers being transmitted include IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. All are 24-bit registers that are sign extended to 32-bits (see Figure 45 for details).

HSDC can be interfaced with SPI or similar interfaces. HSDC is always a master of the communication and consists of three pins: HSA, HSD, and HSCLK. HSA represents the select signal. It stays active low or high when a word is transmitted and it is usually connected to the select pin of the slave. HSD sends data to the slave and it is usually connected to the data input pin of the slave. HSCLK is the serial clock line that is generated by the ADE7880 and it is usually connected to the serial clock input of the slave. Figure 110 shows the connections between the ADE7880 HSDC and slave devices containing an SPI interface.

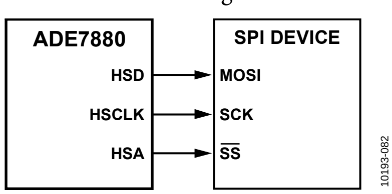


Figure 110. Connecting the ADE7880 HSDC with an SPI

The HSDC communication is managed by the HSDC_CFG register (see Table 52). It is recommended to set the HSDC_CFG register to the desired value before enabling the port using Bit 6 (HSDCEN) in the CONFIG register. In this way, the state of various pins belonging to the HSDC port do not take levels inconsistent with the desired HSDC behavior. After a hardware reset or after power-up, the MISO/HSD and $\overline{\text{SS}}$/HSA pins are set high.

Bit 0 (HCLK) in the HSDC_CFG register determines the serial clock frequency of the HSDC communication. When HCLK is 0 (the default value), the clock frequency is 8 MHz. When HCLK is 1, the clock frequency is 4 MHz. A bit of data is transmitted for every HSCLK high-to-low transition. The slave device that receives data from HSDC samples the HSD line on the low-to-high transition of HSCLK.

The words can be transmitted as 32-bit packages or as 8-bit packages. When Bit 1 (HSIZE) in the HSDC_CFG register is 0 (the default value), the words are transmitted as 32-bit packages. When Bit HSIZE is 1, the registers are transmitted as 8-bit packages. The HSDC interface transmits the words MSB first.

Bit 2 (HGAP) introduces a gap of seven HSCLK cycles between packages when Bit 2 (HGAP) is set to 1. When Bit HGAP is cleared to 0 (the default value), no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication and a data bit is placed on the HSD line with every HSCLK high-to-low transition.

Bits[4:3] (HXFER[1:0]) decide how many words are transmitted. When HXFER[1:0] is 00, the default value, then all 16 words are transmitted. When HXFER[1:0] is 01, only the words representing the instantaneous values of phase and neutral currents and phase voltages are transmitted in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and one 32-bit word that is always equal to INWV. When HXFER[1:0] is 10, only the instantaneous values of phase powers are transmitted in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. The value, 11, for HXFER[1:0] is reserved and writing it is equivalent to writing 00, the default value.

Bit 5 (HSAPOL) determines the polarity of HSA function of the $\overline{\text{SS}}$/HSA pin during communication. When HSAPOL is 0 (the default value), HSA is active low during the communication. This means that HSA stays high when no communication is in progress. When a communication is executed, HSA is low when the 32-bit or 8-bit packages are transferred, and it is high during the gaps. When HSAPOL is 1, the HSA function of the $\overline{\text{SS}}$/HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When a communication is executed, HSA is high when the 32-bit or 8-bit packages are transferred, and it is low during the gaps.

Bits[7:6] of the HSDC_CFG register are reserved. Any value written into these bits does not have any consequence on HSDC behavior.

Figure 111 shows the HSDC transfer protocol for HGAP = 0, HXFER[1:0] = 00 and HSAPOL = 0. Note that the HSDC interface sets a data bit on the HSD line every HSCLK high-to-low transition and the value of Bit HSIZE is irrelevant.

Figure 112 shows the HSDC transfer protocol for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 32-bit word.

Figure 113 shows the HSDC transfer protocol for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 8-bit word.

See Table 52 for the HSDC_CFG register and descriptions for the HCLK, HSIZE, HGAP, HXFER[1:0], and HSAPOL bits. Table 25 lists the time it takes to execute an HSDC data transfer for all HSDC_CFG register settings. For some settings, the transfer time is less than 125 μs (8 kHz), the waveform sample registers update rate. This means the HSDC port transmits data every sampling cycle. For settings in which the transfer time is greater than 125 μs, the HSDC port transmits data only in the first of two consecutive 8 kHz sampling cycles. This means it transmits registers at an effective rate of 4 kHz.

Table 25. Communication Times for Various HSDC Settings

HXFER[1:0]	HGAP	HSIZE[1]	HCLK	Communication Time (μs)
00	0	N/A	0	64
00	0	N/A	1	128
00	1	0	0	77.125
00	1	0	1	154.25
00	1	1	0	119.25
00	1	1	1	238.25
01	0	N/A	0	28
01	0	N/A	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25
10	0	N/A	0	36
10	0	N/A	1	72
10	1	0	0	43
10	1	0	1	86
10	1	1	0	66.625
10	1	1	1	133.25

[1] N/A means not applicable.

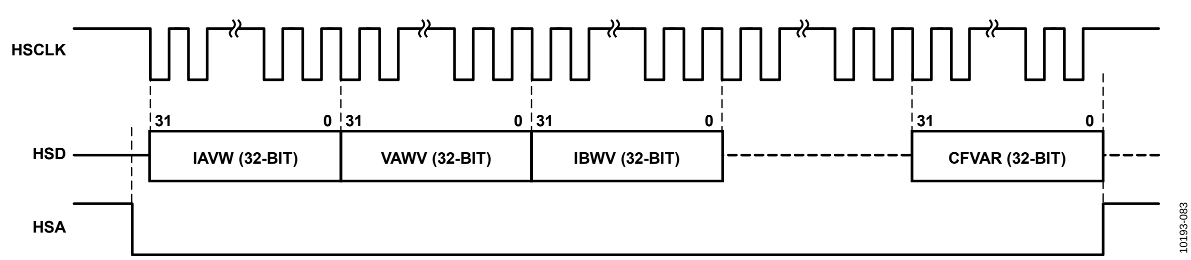


Figure 111. HSDC Communication for HGAP = 0, HXFER[1:0] = 00, and HSAPOL = 0; HSIZE Is Irrelevant

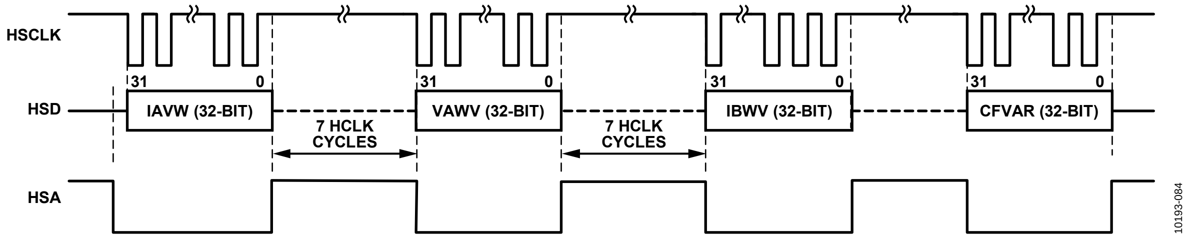


Figure 112. HSDC Communication for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

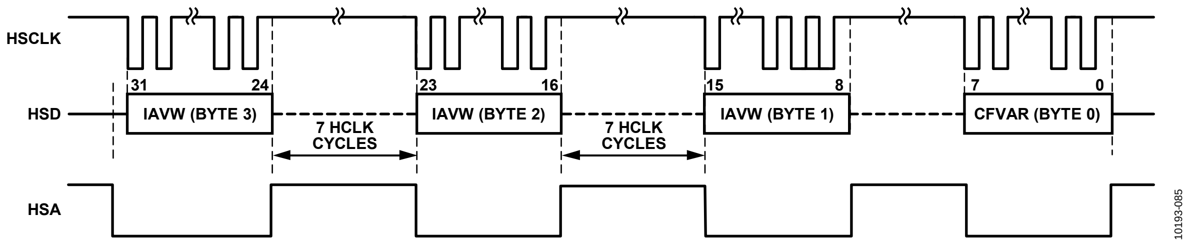


Figure 113. HSDC Communication for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

ADE7880 QUICK SETUP AS ENERGY METER

An energy meter is usually characterized by the nominal current I_n, nominal voltage V_n, nominal frequency f_n, and the meter constant MC.

To quickly set up the ADE7880, execute the following steps:

1. Select the PGA gains in the phase currents, voltages and neutral current channels: Bits[2:0] (PGA1), Bits[5:3] (PGA2) and Bits[8:6] (PGA3) in the Gain register.
2. If Rogowski coils are used, enable the digital integrators in the phase and neutral currents: Bit 0 (INTEN)set to 1 in the CONFIG register. Initialize the DICOEFF register to 0xFF8000 before setting the INTEN bit in the CONFIG register.
3. If f_n is between 55 Hz and 66 Hz, set Bit 14 (SELFREQ) in the COMPMODE register.
4. Initialize all the other data memory RAM registers. Write the last register in the queue three times to ensure that its value is written into the RAM.
5. Initialize the WTHR, VARTHR, VATHR, VLEVEL and VNOM registers based on Equation 26, Equation 37, Equation 44, Equation 22, and Equation 42, respectively.
6. Initialize CF1DEN, CF2DEN, and CF3DEN based on Equation 49.
7. Enable the data memory RAM protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
8. Read back all data memory RAM registers to ensure that they initialized with the desired values. If one or more registers did not initialize correctly, disable the protection by writing 0xAD to an internal 8-bit register at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3. Reinitialize the registers, and write the last register in the queue three times. Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
9. Start the DSP by setting Run = 1.
10. Read the energy registers xWATTHR, xVAHR, xFWATTHR, and xFVARHR to erase their content and start energy accumulation from a known state.
11. Enable the CF1, CF2, and CF3 frequency converter outputs by clearing bits 9, 10, and 11 (CF1DIS, CF2DIS, and CF3DIS) to 0 in the CFMODE register.

For a quick setup of the ADE7880 harmonic calculations, see the Recommended Approach to Managing Harmonic Calculations section.

REGISTERS LIST

Table 30. Registers Located in DSP Data Memory RAM

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust.
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust.
0x4382	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust.
0x4383	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust.
0x4384	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust.
0x4385	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust.
0x4386	NIGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral current gain adjust.
0x4387	Reserved	R/W	24	32 ZPSE	S	0x000000	Do not write this location for proper operation.
0x4388	DICOEFF	R/W	24	32 ZPSE	S	0x0000000	Register used in the digital integrator algorithm. If the integrator is turned on, it must be set at 0xFF8000. In practice, it is transmitted as 0xFFF8000.
0x4389	APGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A power gain adjust.
0x438A	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust.
0x438B	BPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B power gain adjust.
0x438C	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust.
0x438D	CPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C power gain adjust.
0x438E	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust.
0x438F	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset.
0x4390	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset.
0x4391	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset.
0x4392	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset.
0x4393	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset.
0x4394	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset.
0x4395	NIRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral current rms offset.
0x4396-0x4397	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x4398	HPGAIN	R/W	24	32 ZPSE	S	0x000000	Harmonic powers gain adjust.
0x4399	ISUMLVL	R/W	24	32 ZPSE	S	0x000000	Threshold used in comparison between the sum of phase currents and the neutral current.
0x439A-0x439E	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x439F	VLEVEL	R/W	28	32 ZP	S	0x0000000	Register used in the algorithm that computes the fundamental active and reactive powers. Set this register according to Equation 22 for proper functioning of fundamental powers and harmonic computations.
0x43A0-0x43A1	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x43A2	AFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental active power offset adjust.
0x43A3	BFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental active power offset adjust.
0x43A4	CFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental active power offset adjust.
0x43A5	AFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental reactive power offset adjust.
0x43A6	BFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental reactive power offset adjust.
0x43A7	CFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental reactive power offset adjust.
0x43A8	AFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental current rms offset.
0x43A9	BFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental current rms offset.
0x43AA	CFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental current rms offset.
0x43AB	AFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental voltage rms offset.
0x43AC	BFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental voltage rms offset.
0x43AD	CFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental voltage rms offset.
0x43AE	HXWATTOS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic X (see Harmonics Calculations section for details).

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43AF	HYWATTOS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Y (see Harmonics Calculations section for details).
0x43B0	HZWATTOS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Z (see Harmonics Calculations section for details).
0x43B1	HXVAROS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic X (see Harmonics Calculations section for details).
0x43B2	HYVAROS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Y (see Harmonics Calculations section for details).
0x43B3	HZVAROS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Z (see Harmonics Calculations section for details).
0x43B4	HXIRMSOS	R/W	24	32 ZPSE	S	0x000000	Current rms offset on harmonic X (see Harmonics Calculations section for details).
0x43B5	HYIRMSOS	R/W	24	32 ZPSE	S	0x000000	Current rms offset on harmonic Y (see Harmonics Calculations section for details).
0x43B6	HZIRMSOS	R/W	24	32 ZPSE	S	0x000000	Current rms offset on harmonic Z (see Harmonics Calculations section for details).
0x43B7	HXVRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset on harmonic X (see Harmonics Calculations section for details).
0x43B8	HYVRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset on harmonic Y (see Harmonics Calculations section for details).
0x43B9	HZVRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset on harmonic Z (see Harmonics Calculations section for details).
0x43BA to 0x43BF	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x43C0	AIRMS	R	24	32 ZP	S	N/A	Phase A current rms value.
0x43C1	AVRMS	R	24	32 ZP	S	N/A	Phase A voltage rms value.
0x43C2	BIRMS	R	24	32 ZP	S	N/A	Phase B current rms value.
0x43C3	BVRMS	R	24	32 ZP	S	N/A	Phase B voltage rms value.
0x43C4	CIRMS	R	24	32 ZP	S	N/A	Phase C current rms value.
0x43C5	CVRMS	R	24	32 ZP	S	N/A	Phase C voltage rms value.
0x43C6	NIRMS	R	24	32 ZP	S	N/A	Neutral current rms value.
0x43C7	ISUM	R	28	32 ZP	S	N/A	Sum of IAWV, IBWV and ICWV registers.
0x43C8 to 0x43FF	Reserved	N/A	N/A	N/A	N/A	N/A	Do not write these memory locations for proper operation.

[1] R is read, and W is write.
[2] 32 ZPSE = 24-bit signed register that is transmitted as a 32-bit word with four MSBs padded with 0s and sign extended to 28 bits. Whereas 32 ZP = 28- bit or 24-bit signed or unsigned register that is transmitted as a 32-bit word with four or eight MSBs, respectively, padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.

Table 31. Internal DSP Memory RAM Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE203	Reserved	R/W	16	16	U	0x0000	Do not write this memory location for proper operation.
0xE228	Run	R/W	16	16	U	0x0000	Run register starts and stops the DSP. See the Digital Signal Processor section for more details.

[1] R is read, and W is write.
[2] U is unsigned register, and S is signed register in twos complement format.

Table 32. Billable Registers

Address	Register Name	R/W[1, 2]	Bit Length[2]	Bit Length During Communication[2]	Type[2, 3]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Phase A total active energy accumulation.
0xE401	BWATTHR	R	32	32	S	0x00000000	Phase B total active energy accumulation.
0xE402	CWATTHR	R	32	32	S	0x00000000	Phase C total active energy accumulation.
0xE403	AFWATTHR	R	32	32	S	0x00000000	Phase A fundamental active energy accumulation.
0xE404	BFWATTHR	R	32	32	S	0x00000000	Phase B fundamental active energy accumulation.
0xE405	CFWATTHR	R	32	32	S	0x00000000	Phase C fundamental active energy accumulation.
0xE406 to 0xE408	Reserved	R	32	32	S	0x00000000	
0xE409	AFVARHR	R	32	32	S	0x00000000	Phase A fundamental reactive energy accumulation.
0xE40A	BFVARHR	R	32	32	S	0x00000000	Phase B fundamental reactive energy accumulation.
0xE40B	CFVARHR	R	32	32	S	0x00000000	Phase C fundamental reactive energy accumulation.
0xE40C	AVAHR	R	32	32	S	0x00000000	Phase A apparent energy accumulation.
0xE40D	BVAHR	R	32	32	S	0x00000000	Phase B apparent energy accumulation.
0xE40E	CVAHR	R	32	32	S	0x00000000	Phase C apparent energy accumulation.

[1] R is read, and W is write.
[2] N/A is not applicable.
[3] U is unsigned register, and S is signed register in twos complement format.

Table 33. Configuration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE500	IPEAK	R	32	32	U	N/A	Current peak register. See Figure 60 and Table 34 for details about its composition.
0xE501	VPEAK	R	32	32	U	N/A	Voltage peak register. See Figure 60 and Table 35 for details about its composition.
0xE502	STATUS0	R/W	32	32	U	N/A	Interrupt Status Register 0. See Table 36.
0xE503	STATUS1	R/W	32	32	U	N/A	Interrupt Status Register 1. See Table 37.
0xE504	AIMAV	R	20	32 ZP	U	N/A	Phase A current mean absolute value computed during PSM0 and PSM1 modes.
0xE505	BIMAV	R	20	32 ZP	U	N/A	Phase B current mean absolute value computed during PSM0 and PSM1 modes.
0xE506	CIMAV	R	20	32 ZP	U	N/A	Phase C current mean absolute value computed during PSM0 and PSM1 modes.
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage SAG level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0. See Table 38.
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1. See Table 39.
0xE50C	IAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A current.
0xE50D	IBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B current.
0xE50E	ICWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C current.
0xE50F	INWV	R	24	32 SE	S	N/A	Instantaneous value of neutral current.
0xE510	VAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A voltage.
0xE511	VBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B voltage.
0xE512	VCWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C voltage.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE513	AWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase A total active power.
0xE514	BWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase B total active power.
0xE515	CWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase C total active power.
0xE516 to 0xE518	Reserved	R	24	32 SE	S	0x000000	
0xE519	AVA	R	24	32 SE	S	N/A	Instantaneous value of Phase A apparent power.
0xE51A	BVA	R	24	32 SE	S	N/A	Instantaneous value of Phase B apparent power.
0xE51B	CVA	R	24	32 SE	S	N/A	Instantaneous value of Phase C apparent power.
0xE51F	CHECKSUM	R	32	32	U	0xAFFA63B9	Checksum verification. See the Checksum Register section for details.
0xE520	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the alternative computation of the apparent power. When the VNOMxEN bit is set, the applied voltage input in the corresponding phase is ignored and all corresponding rms voltage instances are replaced by the value in the VNOM register.
0xE521 to 0xE5FE	Reserved						Do not write these addresses for proper operation.
0xE5FF	LAST_RWDATA32	R	32	32	U	N/A	Contains the data from the last successful 32-bit register communication.
0xE600	PHSTATUS	R	16	16	U	N/A	Phase peak register. See Table 40.
0xE601	ANGLE0	R	16	16	U	N/A	Time Delay 0. See the Time Interval Between Phases section for details.
0xE602	ANGLE1	R	16	16	U	N/A	Time Delay 1. See the Time Interval Between Phases section for details.
0xE603	ANGLE2	R	16	16	U	N/A	Time Delay 2. See the Time Interval Between Phases section for details.
0xE604 to 0xE607	Reserved						Do not write these addresses for proper operation.
0xE608	PHNOLOAD	R	16	16	U	N/A	Phase no load register. See Table 41.
0xE609 to 0xE60B	Reserved						Do not write these addresses for proper operation.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation-mode register. See Table 42.
0xE60F	Gain	R/W	16	16	U	0x0000	PGA gains at ADC inputs. See Table 43.
0xE610	CFMODE	R/W	16	16	U	0x0EA0	CFx configuration register. See Table 44.
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator.
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator.
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator.
0xE614	APHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase A. See Table 45.
0xE615	BPHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase B. See Table 45.
0xE616	CPHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration Phase of C. See Table 45.
0xE617	PHSIGN	R	16	16	U	N/A	Power sign register. See Table 46.
0xE618	CONFIG	R/W	16	16	U	0x0002	ADE7880 configuration register. See Table 47.
0xE700	MMODE	R/W	8	8	U	0x1C	Measurement mode register. See Table 48.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE701	ACCMODE	R/W	8	8	U	0x80	Accumulation mode register. See Table 49.
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior. See Table 51.
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.
0xE704	SAGCYC	R/W	8	8	U	0x00	SAG detection half line cycles.
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches. See the Synchronizing Energy Registers with CFx Outputs section.
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register. See Table 52.
0xE707	Version	R	8	8	U		Version of die.
0xE7E4	Reserved	R	8	8	U	0x08	This register must remain at this value for checksum functionality to work. If this register shows a different value while being read, reset the chip before working with the checksum feature.
0xE7FD	LAST_RWDATA8	R	8	8	U	N/A	Contains the data from the last successful 8-bit register communication.
0xE880	FVRMS	R	24	32	S	N/A	The rms value of the fundamental component of the phase voltage.
0xE881	FIRMS	R	24	32	S	N/A	The rms value of the fundamental component of the phase current
0xE882	FWATT	R	24	32	S	N/A	The active power of the fundamental component.
0xE883	FVAR	R	24	32	S	N/A	The reactive power of the fundamental component.
0xE884	FVA	R	24	32	S	N/A	The apparent power of the fundamental component.
0xE885	FPF	R	24	32	S	N/A	The power factor of the fundamental component.
0xE886	VTHD	R	24	32	S	N/A	Total harmonic distortion of the phase voltage.
0xE887	ITHD	R	24	32	S	N/A	Total harmonic distortion of the phase current.
0xE888	HXVRMS	R	24	32	S	N/A	The rms value of the phase voltage harmonic X.
0xE889	HXIRMS	R	24	32	S	N/A	The rms value of the phase current harmonic X.
0xE88A	HXWATT	R	24	32	S	N/A	The active power of the harmonic X.
0xE88B	HXVAR	R	24	32	S	N/A	The reactive power of the harmonic X.
0xE88C	HXVA	R	24	32	S	N/A	The apparent power of the harmonic X.
0xE88D	HXPF	R	24	32	S	N/A	The power factor of the harmonic X.
0xE88E	HXVHD	R	24	32	S	N/A	Harmonic distortion of the phase voltage harmonic X relative to the fundamental.
0xE88F	HXIHD	R	24	32	S	N/A	Harmonic distortion of the phase current harmonic X relative to the fundamental.
0xE890	HYVRMS	R	24	32	S	N/A	The rms value of the phase voltage harmonic Y.
0xE891	HYIRMS	R	24	32	S	N/A	The rms value of the phase current harmonic Y.
0xE892	HYWATT	R	24	32	S	N/A	The active power of the harmonic Y.
0xE893	HYVAR	R	24	32	S	N/A	The reactive power of the harmonic Y.
0xE894	HYVA	R	24	32	S	N/A	The apparent power of the harmonic Y.
0xE895	HYPF	R	24	32	S	N/A	The power factor of the harmonic Y.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE896	HYVHD	R	24	32	S	N/A	Harmonic distortion of the phase voltage harmonic Y relative to the fundamental.
0xE897	HYIHD	R	24	32	S	N/A	Harmonic distortion of the phase current harmonic Y relative to the fundamental.
0xE898	HZVRMS	R	24	32	S	N/A	The rms value of the phase voltage harmonic Z.
0xE899	HZIRMS	R	24	32	S	N/A	The rms value of the phase current harmonic Z.
0xE89A	HZWATT	R	24	32	S	N/A	The active power of the harmonic Z.
0xE89B	HZVAR	R	24	32	S	N/A	The reactive power of the harmonic Z.
0xE89C	HZVA	R	24	32	S	N/A	The apparent power of the harmonic Z.
0xE89D	HZPF	R	24	32	S	N/A	The power factor of the harmonic Z.
0xE89E	HZVHD	R	24	32	S	N/A	Harmonic distortion of the phase voltage harmonic Z relative to the fundamental.
0xE89F	HZIHD	R	24	32	S	N/A	Harmonic distortion of the phase current harmonic Z relative to the fundamental.
0xE8A0 to 0xE8FF	Reserved		24	32			Reserved. These registers are always 0.
0xE900	HCONFIG	R/W	16	16	U	0x08	Harmonic Calculations Configuration register. See Table 54.
0xE902	APF	R	16	16	S	N/A	Phase A power factor.
0xE903	BPF	R	16	16	S	N/A	Phase B power factor.
0xE904	CPF	R	16	16	S	N/A	Phase C power factor.
0xE905	APERIOD	R	16	16	U	N/A	Line period on Phase A voltage.
0xE906	BPERIOD	R	16	16	U	N/A	Line period on Phase B voltage.
0xE907	CPERIOD	R	16	16	U	N/A	Line period on Phase C voltage.
0xE908	APNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/ fundamental active power data paths. Do not write 0xFFFF to this register.
0xE909	VARNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/ fundamental reactive power data path. Do not write 0xFFFF to this register.
0xE90A	VANOLOAD	R/W	16	16	U	0x0000	No load threshold in the apparent power data path. Do not write 0xFFFF to this register.
0xE9FE	LAST_ADD	R	16	16	U	N/A	The address of the register successfully accessed during the last read/write operation.
0xE9FF	LAST_RWDATA16	R	16	16	U	N/A	Contains the data from the last successful 16-bit register communication.
0xEA00	CONFIG3	R/W	8	8	U	0x01	Configuration register. See Table 53.
0xEA01	LAST_OP	R	8	8	U	N/A	Indicates the type, read or write, of the last successful read/write operation.
0xEA02	WTHR	R/W	8	8	U	0x03	Threshold used in phase total/ fundamental active power data path.
0xEA03	VARTHR	R/W	8	8	U	0x03	Threshold used in phase total/ fundamental reactive power data path.
0xEA04	VATHR	R/W	8	8	U	0x03	Threshold used in phase apparent power data path.
0xEA05 to 0xEA07	Reserved		8	8			Reserved. These registers are always 0.
0xEA08	HX	R/W	8	8	U	3	Selects an index of the harmonic monitored by the harmonic computations.
0xEA09	HY	R/W	8	8	U	5	Selects an index of the harmonic monitored by the harmonic computations.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xEA0A	HZ	R/W	8	8	U	7	Selects an index of the harmonic monitored by the harmonic computations.
0xEA0B to 0xEBFE	Reserved		8	8			Reserved. These registers are always 0.
0xEBFF	Reserved		8	8			This address can be used in manipulating the $\overline{SS}$/HSA pin when SPI is chosen as the active port. See the Serial Interfaces section for details.
0xEC00	LPOILVL	R/W	8	8	U	0x07	Overcurrent threshold used during PSM2 mode. See Table 55 in which the register is detailed.
0xEC01	CONFIG2	R/W	8	8	U	0x00	Configuration register used during PSM1 mode. See Table 56.

[1] R is read, and W is write.
[2] 32 ZP = 24- or 20-bit signed or unsigned register that is transmitted as a 32-bit word with 8 or 12 MSBs, respectively, padded with 0s. 32 SE = 24-bit signed register that is transmitted as a 32-bit word sign extended to 32 bits. 16 ZP = 10-bit unsigned register that is transmitted as a 16-bit word with six MSBs padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.
[4] N/A is not applicable.

Table 34. IPEAK Register (Address 0xE500)

Bit	Mnemonic	Default Value	Description
23:0	IPEAKVAL[23:0]	0	These bits contain the peak value determined in the current channel.
24	IPPHASE[0]	0	When this bit is set to 1, Phase A current generated IPEAKVAL[23:0] value.
25	IPPHASE[1]	0	When this bit is set to 1, Phase B current generated IPEAKVAL[23:0] value.
26	IPPHASE[2]	0	When this bit is set to 1, Phase C current generated IPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 35. VPEAK Register (Address 0xE501)

Bit	Mnemonic	Default Value	Description
23:0	VPEAKVAL[23:0]	0	These bits contain the peak value determined in the voltage channel.
24	VPPHASE[0]	0	When this bit is set to 1, Phase A voltage generated VPEAKVAL[23:0] value.
25	VPPHASE[1]	0	When this bit is set to 1, Phase B voltage generated VPEAKVAL[23:0] value.
26	VPPHASE[2]	0	When this bit is set to 1, Phase C voltage generated VPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 36. STATUS0 Register (Address 0xE502)

Bit	Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) has changed.
1	FAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental active energy registers, FWATTHR, BFWATTHR, or CFWATTHR, has changed.
2	Reserved	0	This bit is always 0.
3	FREHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental reactive energy registers, AFVARHR, BFVARHR, or CFVARHR, has changed.
4	VAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) has changed.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it indicates the end of an integration over an integer number of half line cycles set in the LINECYC register.

Bit	Mnemonic	Default Value	Description
6	REVAPA	0	When this bit is set to 1, it indicates that the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 0 (AWSIGN) of the PHSIGN register (see Table 46).
7	REVAPB	0	When this bit is set to 1, it indicates that the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 1 (BWSIGN) of the PHSIGN register (see Table 46).
8	REVAPC	0	When this bit is set to 1, it indicates that the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 2 (CWSIGN) of the PHSIGN register (see Table 46).
9	REVPSUM1	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF1 data path has changed sign. The sign itself is indicated in Bit 3 (SUM1SIGN) of the PHSIGN register (see Table 46).
10	REVFRPA	0	When this bit is set to 1, it indicates that the Phase A fundamental reactive power has changed sign. The sign itself is indicated in Bit 4 (AFVARSIGN) of the PHSIGN register (see Table 46).
11	REVFRPB	0	When this bit is set to 1, it indicates that the Phase B fundamental reactive power has changed sign. The sign itself is indicated in Bit 5 (BFVARSIGN) of the PHSIGN register (see Table 46).
12	REVFRPC	0	When this bit is set to 1, it indicates that the Phase C fundamental reactive power has changed sign. The sign itself is indicated in Bit 6 (CFVARSIGN) of the PHSIGN register (see Table 46).
13	REVPSUM2	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF2 data path has changed sign. The sign itself is indicated in Bit 7 (SUM2SIGN) of the PHSIGN register (see Table 46).
14	CF1		When this bit is set to 1, it indicates a high-to-low transition has occurred at CF1 pin; that is, an active low pulse has been generated. The bit is set even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 44).
15	CF2		When this bit is set to 1, it indicates a high-to-low transition has occurred at the CF2 pin; that is, an active low pulse has been generated. The bit is set even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 44).
16	CF3		When this bit is set to 1, it indicates a high-to-low transition has occurred at CF3 pin; that is, an active low pulse has been generated. The bit is set even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 44).
17	DREADY	0	When this bit is set to 1, it indicates that all periodical (at 8 kHz rate) DSP computations have finished.
18	REVPSUM3	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF3 data path has changed sign. The sign itself is indicated in Bit 8 (SUM3SIGN) of the PHSIGN register (see Table 46).
19	HREADY	0	When this bit is set to 1, it indicates the harmonic block output registers are updated. If Bit 0 (HRCFG) in the HCONFIG register is cleared to 0, this flag is set to 1 every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in the HCONFIG register starting HSTIME (Bits [4:3] in the HCONFIG register) after the harmonic block setup. If Bit HRCFG is set to 1, the HREADY flag is set to 1 every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in the HCONFIG register, starting immediately after the harmonic block setup.
31:18	Reserved	0 0000 0000 0000	Reserved. These bits are always 0.

Table 37. STATUS1 Register (Address 0xE503)

Bit	Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition determined by the total active power and apparent power. The phase is indicated in Bits[2:0] (NLPHASE[x]) in the PHNOLOAD register (see Table 41.)
1	FNLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on fundamental active and reactive powers. The phase is indicated in Bits[5:3] (FNLPHASE[x]) in the PHNOLOAD register (see Table 41).
2	VANLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on apparent power. The phase is indicated in Bits[8:6] (VANLPHASE[x]) in the PHNOLOAD register (see Table 41).
3	ZXTOVA	0	When this bit is set to 1, it indicates a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it indicates a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it indicates a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it indicates a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it indicates a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it indicates a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C current.
15	RSTDONE	1	In case of a software reset command, Bit 7 (SWRST) is set to 1 in the CONFIG register, or a transition from PSM1, PSM2, or PSM3 to PSM0, or a hardware reset, this bit is set to 1 at the end of the transition process and after all registers change value to default. The $\overline{\text{IRQ1}}$ pin goes low to signal this moment because this interrupt cannot be disabled.
16	SAG	0	When this bit is set to 1, it indicates one of phase voltages entered or exited a sag state. The phase is indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 40).
17	OI	0	When this bit is set to 1, it indicates an overcurrent event has occurred on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 40).
18	OV	0	When this bit is set to 1, it indicates an overvoltage event has occurred on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 40).
19	SEQERR	0	When this bit is set to 1, it indicates a negative-to-positive zero crossing on Phase A voltage was not followed by a negative-to-positive zero crossing on Phase B voltage but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it indicates $\left\| \|ISUM\| - \|INWV\| \right\| > ISUMLVL$, where *ISUMLVL* is indicated in the ISUMLVL register.
21	Reserved	1	Reserved. This bit is always set to 1.
22	Reserved	0	Reserved. This bit is always set to 0.
23	PKI	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the current channel has ended. The IPEAK register contains the peak value and the phase where the peak has been detected (see Table 34).

Bit	Mnemonic	Default Value	Description
24	PKV	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the voltage channel has ended. VPEAK register contains the peak value and the phase where the peak has been detected (see Table 35).
25	CRC	0	When this bit is set to 1, it indicates the ADE7880 has computed a different checksum relative to the one computed when the Run register was set to 1.
31:26	Reserved	000 0000	Reserved. These bits are always 0.

Table 38. MASK0 Register (Address 0xE50A)

Bit	Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) changes.
1	FAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental active energy registers (AFWATTHR, BFWATTHR, or CFWATTHR) changes.
2	Reserved	0	This bit does not manage any functionality.
3	FREHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental reactive energy registers (AFVARHR, BFVARHR, or CFVARHR) changes.
4	VAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) changes.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it enables an interrupt at the end of an integration over an integer number of half line cycles set in the LINECYC register.
6	REVAPA	0	When this bit is set to 1, it enables an interrupt when the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
7	REVAPB	0	When this bit is set to 1, it enables an interrupt when the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
8	REVAPC	0	When this bit is set to 1, it enables an interrupt when the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
9	REVPSUM1	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF1 data path changes sign.
10	REVFRPA	0	When this bit is set to 1, it enables an interrupt when the Phase A fundamental reactive power changes sign.
11	REVFRPB	0	When this bit is set to 1, it enables an interrupt when the Phase B fundamental reactive power changes sign.
12	REVFRPC	0	When this bit is set to 1, it enables an interrupt when the Phase C fundamental reactive power changes sign.
13	REVPSUM2	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF2 data path changes sign.
14	CF1		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at the CF1 pin, that is an active low pulse is generated. The interrupt can be enabled even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 44).
15	CF2		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at CF2 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 44).
16	CF3		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF3 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 44).
17	DREADY	0	When this bit is set to 1, it enables an interrupt when all periodical (at 8 kHz rate) DSP computations finish.

Bit	Mnemonic	Default Value	Description
18	REVPSUM3	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF3 data path changes sign.
19	HREADY	0	When this bit is set to 1, it enables an interrupt when the harmonic block output registers have been updated. If Bit 0 (HRCFG) in HCONFIG register is cleared to 0, the interrupt is triggered every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in HCONFIG register starting HSTIME (Bits [4:3] in HCONFIG register) after the harmonic block setup. If Bit HRCFG is set to 1, the interrupt is triggered every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in HCONFIG register starting immediately after the harmonic block setup.
31:19	Reserved	00 0000 0000 0000	Reserved. These bits do not manage any functionality.

Table 39. MASK1 Register (Address 0xE50B)

Bit	Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition determined by the total active power and VNOM based apparent power.
1	FNLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on fundamental active and reactive powers.
2	VANLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on apparent power.
3	ZXTOVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C current.
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit does not have any functionality attached. It can be set to 1 or cleared to 0 without having any effect.
16	SAG	0	When this bit is set to 1, it enables an interrupt when one of the phase voltages entered or exited a sag state. The phase is indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 40).
17	OI	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 40).
18	OV	0	When this bit is set to 1, it enables an interrupt when an overvoltage event occurs on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 40).

Bit	Mnemonic	Default Value	Description
19	SEQERR	0	When this bit is set to 1, it enables an interrupt when a negative-to-positive zero crossing on Phase A voltage is not followed by a negative-to-positive zero crossing on Phase B voltage, but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it enables an interrupt when $\left\|\left\|ISUM\right\|-\left\|INWV\right\|\right\| > ISUMLVL$ is greater than the value indicated in ISUMLVL register.
22:21	Reserved	00	Reserved. These bits do not manage any functionality.
23	PKI	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the current channel has ended.
24	PKV	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the voltage channel has ended.
25	CRC	0	When this bit is set to 1, it enables an interrupt when the latest checksum value is different from the checksum value computed when Run register was set to 1.
31:26	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Table 40. PHSTATUS Register (Address 0xE600)

Bit	Mnemonic	Default Value	Description
2:0	Reserved	000	Reserved. These bits are always 0.
3	OIPHASE[0]	0	When this bit is set to 1, Phase A current generates Bit 17 (OI) in the STATUS1 register.
4	OIPHASE[1]	0	When this bit is set to 1, Phase B current generates Bit 17 (OI) in the STATUS1 register.
5	OIPHASE[2]	0	When this bit is set to 1, Phase C current generates Bit 17 (OI) in the STATUS1 register.
8:6	Reserved	000	Reserved. These bits are always 0.
9	OVPHASE[0]	0	When this bit is set to 1, Phase A voltage generates Bit 18 (OV) in the STATUS1 register.
10	OVPHASE[1]	0	When this bit is set to 1, Phase B voltage generates Bit 18 (OV) in the STATUS1 register.
11	OVPHASE[2]	0	When this bit is set to 1, Phase C voltage generates Bit 18 (OV) in the STATUS1 register.
12	VSPHASE[0]	0	0: Phase A voltage is above SAGLVL level for SAGCYC half line cycles. 1: Phase A voltage is below SAGLVL level for SAGCYC half line cycles. When this bit is switches from 0 to 1 or from 1 to 0, the Phase A voltage generates Bit 16 (SAG) in the STATUS1 register.
13	VSPHASE[1]	0	0: Phase B voltage is above SAGLVL level for SAGCYC half line cycles. 1: Phase B voltage is below SAGLVL level for SAGCYC half line cycles. When this bit is switches from 0 to 1 or from 1 to 0, the Phase B voltage generates Bit 16 (SAG) in the STATUS1 register.
14	VSPHASE[2]	0	0: Phase C voltage is above SAGLVL level for SAGCYC half line cycles 1: Phase C voltage is below SAGLVL level for SAGCYC half line cycles When this bit is switches from 0 to 1 or from 1 to 0, the Phase C voltage generates Bit 16 (SAG) in the STATUS1 register.
15	Reserved	0	Reserved. This bit is always 0.

Table 41. PHNOLOAD Register (Address 0xE608)

Bit	Mnemonic	Default Value	Description
0	NLPHASE[0]	0	0: Phase A is out of no load condition determined by the Phase A total active power and apparent power. 1: Phase A is in no load condition determined by phase A total active power and apparent power. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
1	NLPHASE[1]	0	0: Phase B is out of no load condition determined by the Phase B total active power and apparent power. 1: Phase B is in no load condition determined by the Phase B total active power and apparent power. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
2	NLPHASE[2]	0	0: Phase C is out of no load condition determined by the Phase C total active power and apparent power. 1: Phase C is in no load condition determined by the Phase C total active power and apparent power. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
3	FNLPHASE[0]	0	0: Phase A is out of no load condition based on fundamental active/reactive powers. 1: Phase A is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.

Bit	Mnemonic	Default Value	Description
4	FNLPHASE[1]	0	0: Phase B is out of no load condition based on fundamental active/reactive powers. 1: Phase B is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
5	FNLPHASE[2]	0	0: Phase C is out of no load condition based on fundamental active/reactive powers. 1: Phase C is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
6	VANLPHASE[0]	0	0: Phase A is out of no load condition based on apparent power. 1: Phase A is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
7	VANLPHASE[1]	0	0: Phase B is out of no load condition based on apparent power. 1: Phase B is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
8	VANLPHASE[2]	0	0: Phase C is out of no load condition based on apparent power. 1: Phase C is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 42. COMPMODE Register (Address 0xE60E)

Bit	Mnemonic	Default Value	Description
0	TERMSEL1[0]	1	Setting all TERMSEL1[2:0] to 1 signifies the sum of all three phases is included in the CF1 output. Phase A is included in the CF1 outputs calculations.
1	TERMSEL1[1]	1	Phase B is included in the CF1 outputs calculations.
2	TERMSEL1[2]	1	Phase C is included in the CF1 outputs calculations.
3	TERMSEL2[0]	1	Setting all TERMSEL2[2:0] to 1 signifies the sum of all three phases is included in the CF2 output. Phase A is included in the CF2 outputs calculations.
4	TERMSEL2[1]	1	Phase B is included in the CF2 outputs calculations.
5	TERMSEL2[2]	1	Phase C is included in the CF2 outputs calculations.
6	TERMSEL3[0]	1	Setting all TERMSEL3[2:0] to 1 signifies the sum of all three phases is included in the CF3 output. Phase A is included in the CF3 outputs calculations.
7	TERMSEL3[1]	1	Phase B is included in the CF3 outputs calculations.
8	TERMSEL3[2]	1	Phase C is included in the CF3 outputs calculations.
10:9	ANGLESEL[1:0]	00	00: the angles between phase voltages and phase currents are measured. 01: the angles between phase voltages are measured. 10: the angles between phase currents are measured. 11: no angles are measured.
11	VNOMAEN	0	When this bit is 0, the apparent power on Phase A is computed regularly. When this bit is 1, the apparent power on Phase A is computed using the VNOM register instead of regular measured rms phase voltage. The applied Phase A voltage input is ignored, and all Phase A rms voltage instances are replaced by the value in the VNOM register.
12	VNOMBEN	0	When this bit is 0, the apparent power on Phase B is computed regularly. When this bit is 1, the apparent power on Phase B is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase B voltage input is ignored, and all Phase B rms voltage instances are replaced by the value in the VNOM register.
13	VNOMCEN	0	When this bit is 0, the apparent power on Phase C is computed regularly. When this bit is 1, the apparent power on Phase C is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase C voltage input is ignored, and all Phase C rms voltage instances are replaced by the value in the VNOM register.
14	SELFREQ	0	When the ADE7880 is connected to networks with fundamental frequencies between 45 Hz and 55 Hz, clear this bit to 0 (default value). When the ADE7880 is connected to networks with fundamental frequencies between 55 Hz and 66 Hz, set this bit to 1.
15	Reserved	0	This bit is 0 by default and it does not manage any functionality.

Table 43. Gain Register (Address 0xE60F)

Bit	Mnemonic	Default Value	Description
2:0	PGA1[2:0]	000	Phase currents gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7880 behaves like PGA1[2:0] = 000.
5:3	PGA2[2:0]	000	Neutral current gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7880 behaves like PGA2[2:0] = 000.
8:6	PGA3[2:0]	000	Phase voltages gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7880 behaves like PGA3[2:0] = 000.
15:9	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Table 44. CFMODE Register (Address 0xE610)

Bit	Mnemonic	Default Value	Description
2:0	CF1SEL[2:0]	000	000: the CF1 frequency is proportional to the sum of total active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 010: the CF1 frequency is proportional to the sum of apparent powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 011: the CF1 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 100: the CF1 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 001, 101, 110, 111: reserved.
5:3	CF2SEL[2:0]	100	000: the CF2 frequency is proportional to the sum of total active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 010: the CF2 frequency is proportional to the sum of apparent powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 011: the CF2 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 100: the CF2 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 001, 101,110,111: reserved.

Bit	Mnemonic	Default Value	Description
8:6	CF3SEL[2:0]	010	000: the CF3 frequency is proportional to the sum of total active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 010: the CF3 frequency is proportional to the sum of apparent powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 011: CF3 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 100: CF3 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 001, 101,110,111: reserved.
9	CF1DIS	1	When this bit is set to 1, the CF1 output is disabled. The respective digital to frequency converter remains enabled even if CF1DIS = 1. When this bit is set to 0, the CF1 output is enabled.
10	CF2DIS	1	When this bit is set to 1, the CF2 output is disabled. The respective digital to frequency converter remains enabled even if CF2DIS = 1. When this bit is set to 0, the CF2 output is enabled.
11	CF3DIS	1	When this bit is set to 1, the CF3 output is disabled. The respective digital to frequency converter remains enabled even if CF3DIS = 1. When this bit is set to 0, the CF3 output is enabled.
12	CF1LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF1 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
13	CF2LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF2 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
14	CF3LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF3 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
15	Reserved	0	Reserved. This bit does not manage any functionality.

Table 45. APHCAL, BPHCAL, CPHCAL Registers (Address 0xE614, Address 0xE615, Address 0xE616)

Bit	Mnemonic	Default Value	Description
9:0	PHCALVAL	0000000000	If the current leads the voltage, these bits can vary between 0 and 383. If the current lags the voltage, these bits can vary between 512 and 575. If the PHCALVAL bits are set with numbers between 384 and 511, the compensation behaves like PHCALVAL set between 256 and 383. If the PHCALVAL bits are set with numbers between 576 and 1023, the compensation behaves like PHCALVAL bits set between 384 and 511.
15:10	Reserved	000000	Reserved. These bits do not manage any functionality.

Table 46. PHSIGN Register (Address 0xE617)

Bit	Mnemonic	Default Value	Description
0	AWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is negative.
1	BWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is negative.
2	CWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase C is positive. 1: if the active power identified by Bit 6 (REVAPSEL) bit in the ACCMODE register (total of fundamental) on Phase C is negative.

Bit	Mnemonic	Default Value	Description
3	SUM1SIGN	0	0: if the sum of all phase powers in the CF1 data path is positive. 1: if the sum of all phase powers in the CF1 data path is negative. Phase powers in the CF1 data path are identified by Bits[2:0] (TERMSEL1[x]) of the COMPMODE register and by Bits[2:0] (CF1SEL[x]) of the CFMODE register.
4	AFVARSIGN	0	0: if the fundamental reactive power on Phase A is positive. 1: if the fundamental reactive power on Phase A is negative.
5	BFVARSIGN	0	0: if the fundamental reactive power on Phase B is positive. 1: if the fundamental reactive power on Phase B is negative.
6	CFVARSIGN	0	0: if the fundamental reactive power on Phase C is positive. 1: if the fundamental reactive power on Phase C is negative.
7	SUM2SIGN	0	0: if the sum of all phase powers in the CF2 data path is positive. 1: if the sum of all phase powers in the CF2 data path is negative. Phase powers in the CF2 data path are identified by Bits[5:3] (TERMSEL2[x]) of the COMPMODE register and by Bits[5:3] (CF2SEL[x]) of the CFMODE register.
8	SUM3SIGN	0	0: if the sum of all phase powers in the CF3 data path is positive. 1: if the sum of all phase powers in the CF3 data path is negative. Phase powers in the CF3 data path are identified by Bits[8:6] (TERMSEL3[x]) of the COMPMODE register and by Bits[8:6] (CF3SEL[x]) of the CFMODE register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 47. CONFIG Register (Address 0xE618)

Bit	Mnemonic	Default Value	Description
0	INTEN	0	This bit manages the integrators in the phase current channels. If INTEN = 0, then the integrators in the phase current channels are always disabled. If INTEN = 1, then the integrators in the phase currents channels are enabled. The neutral current channel integrator is managed by Bit 3 (ININTEN) of CONFIG3 register.
1	Reserved	1	Reserved. Maintain this bit at 1 for proper operation.
2	CF2DIS	0	When this bit is cleared to 0, the CF2 functionality is chosen at CF2/HREADY pin. When this bit is set to 1, the HREADY functionality is chosen at CF2/HREADY pin.
3	SWAP	0	When this bit is set to 1, the voltage channel outputs are swapped with the current channel outputs. Thus, the current channel information is present in the voltage channel registers and vice versa.
4	MOD1SHORT	0	When this bit is set to 1, the voltage channel ADCs behave as if the voltage inputs were put to ground.
5	MOD2SHORT	0	When this bit is set to 1, the current channel ADCs behave as if the voltage inputs were put to ground.
6	HSDCEN	0	When this bit is set to 1, the HSDC serial port is enabled and HSCLK functionality is chosen at CF3/HSCLK pin. When this bit is cleared to 0, HSDC is disabled and CF3 functionality is chosen at CF3/HSCLK pin.
7	SWRST	0	When this bit is set to 1, a software reset is initiated.
9:8	VTOIA[1:0]	00	These bits decide what phase voltage is considered together with Phase A current in the power path. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. When set, the ADE7880 behaves like VTOIA[1:0] = 00.
11:10	VTOIB[1:0]	00	These bits decide what phase voltage is considered together with Phase B current in the power path. 00 = Phase B voltage. 01 = Phase C voltage. 10 = Phase A voltage. 11 = reserved. When set, the ADE7880 behaves like VTOIB[1:0] = 00.

Bit	Mnemonic	Default Value	Description
13:12	VTOIC[1:0]	00	These bits decide what phase voltage is considered together with Phase C current in the power path. 00 = Phase C voltage. 01 = Phase A voltage. 10 = Phase B voltage. 11 = reserved. When set, the ADE7880 behaves like VTOIC[1:0] = 00.
15:14	Reserved		Reserved.

Table 48. MMODE Register (Address 0xE700)

Bit	Mnemonic	Default Value	Description
1:0	Reserved		Reserved.
2	PEAKSEL[0]	1	PEAKSEL[2:0] bits can all be set to 1 simultaneously to allow peak detection on all three phases simultaneously. If more than one PEAKSEL[2:0] bits are set to 1, then the peak measurement period indicated in the PEAKCYC register decreases accordingly because zero crossings are detected on more than one phase. When this bit is set to 1, Phase A is selected for the voltage and current peak registers.
3	PEAKSEL[1]	1	When this bit is set to 1, Phase B is selected for the voltage and current peak registers.
4	PEAKSEL[2]	1	When this bit is set to 1, Phase C is selected for the voltage and current peak registers.
7:5	Reserved	000	Reserved. These bits do not manage any functionality.

Table 49. ACCMODE Register (Address 0xE701)

Bit	Mnemonic	Default Value	Description
1:0	WATTACC[1:0]	00	00: signed accumulation mode of the total and fundamental active powers. The total and fundamental active energy registers and the CFx pulses are generated in the same way. 01: positive only accumulation mode of the total and fundamental active powers. In this mode, although the total and fundamental active energy registers are accumulated in positive only mode, the CFx pulses are generated in signed accumulation mode. 10: reserved. When set, the device behaves like WATTACC[1:0] = 00. 11: absolute accumulation mode of the total and fundamental active powers. The total and fundamental energy registers and the CFx pulses are generated in the same way.
3:2	VARACC[1:0]	00	00: signed accumulation of the fundamental reactive powers. The fundamental reactive energy registers and the CFx pulses are generated in the same way. 01: reserved. When set, the device behaves like VARACC[1:0] = 00. 10: the fundamental reactive power is accumulated, depending on the sign of the fundamental active power: if the active power is positive, the reactive power is accumulated as is, whereas if the active power is negative, the reactive power is accumulated with reversed sign. In this mode, although the total and fundamental reactive energy registers are accumulated in absolute mode, the CFx pulses are generated in signed accumulation mode. 11: absolute accumulation mode of the fundamental reactive powers. In this mode, although the total and fundamental reactive energy registers are accumulated in absolute mode, the CFx pulses are generated in signed accumulation mode.
5:4	CONSEL[1:0]	00	These bits select the inputs to the energy accumulation registers. IA', IB', and IC' are IA, IB, and IC shifted respectively by −90°. See Table 50. 00: 3-phase four wires with three voltage sensors. 01: 3-phase three wires delta connection. In this mode, BVRMS register contains the rms value of VA-VC. 10: 3-phase four wires with two voltage sensors. 11: 3-phase four wires delta connection.

Bit	Mnemonic	Default Value	Description
6	REVAPSEL	0	0: The total active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC). 1: The fundamental active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC).
7	Reserved	1	Reserved. This bit does not manage any functionality.

Table 50. CONSEL[1:0] Bits in Energy Registers[1]

Energy Registers	CONSEL[1:0] = 00	CONSEL[1:0] = 01	CONSEL[1:0] = 10	CONSEL[1:0] = 11
AWATTHR, AFWATTHR	VA × IA	VA × IA	VA × IA	VA × IA
BWATTHR, BFWATTHR	VB × IB	VB = VA – VC	VB = –VA – VC	VB = –VA
		VB ×IB[1]	VB × IB	VB × IB
CWATTHR, CFWATTHR	VC × IC	VC × IC	VC × IC	VC × IC
AVARHR, AFVARHR	VA × IA′	VA × IA′	VA × IA′	VA × IA′
BVARHR, BFVARHR	VB × IB′	VB = VA – VC	VB = –VA – VC	VB = –VA
		VB × IB′[1]	VB × IB′	VB × IB′
CVARHR, CFVARHR	VC ×IC′	VC × IC′	VC × IC′	VC × IC′
AVAHR	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms
BVAHR	VB rms × IB rms	VB rms × IB rms	VB rms × IB rms	VB rms × IB rms
		VB = VA – VC[1]	VB = –VA – VC	VB = –VA
CVAHR	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7880 computes the rms value of the line voltage between Phase A and and Phase C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase, 3-Wire Delta Configurations section). Consequently, the ADE7880 computes powers associated with Phase B that do not have physical meaning. To avoid any errors in the frequency output pins CF1, CF2 or CF3 related to the powers associated with Phase B, disable the contribution of Phase B to the energy to frequency converters by setting bits TERMSEL1[1], or TERMSEL2[1], or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Table 51. LCYCMODE Register (Address 0xE702)

Bit	Mnemonic	Default Value	Description
0	LWATT	0	0: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed in regular accumulation mode. 1: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed into line cycle accumulation mode.
1	LVAR	0	0: the var-hour accumulation registers (AFVARHR, BFVARHR, and CFVARHR) are placed in regular accumulation mode. 1: the var-hour accumulation registers (AFVARHR, BFVARHR, and CFVARHR) are placed into line-cycle accumulation mode.
2	LVA	0	0: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed in regular accumulation mode. 1: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed into line-cycle accumulation mode.
3	ZXSEL[0]	1	0: Phase A is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase A is selected for zero-crossings counts in the line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
4	ZXSEL[1]	1	0: Phase B is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase B is selected for zero-crossings counts in the line cycle accumulation mode.
5	ZXSEL[2]	1	0: Phase C is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase C is selected for zero-crossings counts in the line cycle accumulation mode.
6	RSTREAD	1	0: read-with-reset of all energy registers is disabled. Clear this bit to 0 when Bits[2:0] (LWATT, LVAR, and LVA) are set to 1. 1: enables read-with-reset of all xWATTHR, xVARHR, xVAHR, xFWATTHR, and xFVARHR registers. This means a read of those registers resets them to 0.

Bit	Mnemonic	Default Value	Description
7	PFMODE	0	0: power factor calculation uses instantaneous values of various phase powers used in its expression. 1: power factor calculation uses phase energies values calculated using line cycle accumulation mode. Bits LWATT and LVA in LCYCMODE register must be enabled for the power factors to be computed correctly. The update rate of the power factor measurement in this case is the integral number of half line cycles that are programmed into the LINECYC register.

Table 52. HSDC_CFG Register (Address 0xE706)

Bit	Mnemonic	Default Value	Description
0	HCLK	0	0: HSCLK is 8 MHz. 1: HSCLK is 4 MHz.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, most significant bit first. 1: HSDC transmits the 32-bit registers in 8-bit packages, most significant bit first.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.
4:3	HXFER[1:0]	00	00 = HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. 01 = HSDC transmits seven instantaneous values of currents and voltages: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and INWV. 10 = HSDC transmits nine instantaneous values of phase powers: AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. 11 = reserved. If set, the ADE7880 behaves as if HXFER[1:0] = 00.
5	HSAPOL	0	0: $\overline{SS}$/has output pin is active low. 1: $\overline{SS}$/HSA output pin is active high.
7:6	Reserved	00	Reserved. These bits do not manage any functionality.

Table 53. CONFIG3 Register (Address 0xEA00)

Bit	Mnemonic	Default Value	Description
0	HPFEN	1	When HPFEN = 1, then all high-pass filters in voltage and current channels are enabled. When HPFEN = 0, then all high-pass filters are disabled.
1	LPFSEL	0	When LPFSEL = 0, the LPF in the total active power data path introduces a settling time of 650 ms. When LPFSEL = 1, the LPF in the total active power data path introduces a settling time of 1300 ms.
2	INSEL	0	When INSEL = 0, the register NIRMS contains the rms value of the neutral current. When INSEL = 1, the register NIRMS contains the rms value of ISUM, the instantaneous value of the sum of all 3 phase currents, IA, IB, and IC.
3	ININTEN	0	This bit manages the integrator in the neutral current channel. If ININTEN = 0, then the integrator in the neutral current channel is disabled. If ININTDIS = 1, then the integrator in the neutral channel is enabled. The integrators in the phase currents channels are managed by Bit 0 (INTEN) of CONFIG register.
4	Reserved	0	Reserved. Maintain this bit at 0 for proper operation.
7:5	Reserved	000	Reserved. These bits do not manage any functionality.

Table 54. HCONFIG Register (Address 0xE900)

Bit	Mnemonic	Default Value	Description
0	HRCFG	0	When this bit is cleared to 0, the Bit 19 (HREADY) interrupt in MASK0 register is triggered after a certain delay period. The delay period is set by bits HSTIME. The update frequency after the settling time is determined by bits HRATE. When this bit is set to 1, the Bit 19 (HREADY) interrupt in MASK0 register is triggered starting immediately after the harmonic calculations block has been setup. The update frequency is determined by Bits HRATE.
2:1	HPHASE	00	These bits decide what phase or neutral is analyzed by the harmonic calculations block. 00 = Phase A voltage and current. 01 = Phase B voltage and current. 10 = Phase C voltage and current. 11 = neutral current.
4:3	HSTIME	01	These bits decide the delay period after which, if HRCFG bit is set to 0, Bit 19 (HREADY) in the STATUS0 register is set to 1. 00 = 500 ms. 01 = 750 ms. 10 = 1000 ms. 11 = 1250 ms.
7:5	HRATE	000	These bits manage the update rate of the harmonic registers. 000 = 125 µs (8 kHz rate). 001 = 250 µs (4 kHz rate). 010 = 1 ms (1 kHz rate). 011 = 16 ms (62.5 Hz rate). 100 = 128 ms (7.8125 Hz rate). 101 = 512 ms (1.953125 Hz rate). 110 = 1.024 sec (0.9765625 Hz rate). 111 = harmonic calculations disabled.
9:8	ACTPHSEL	00	These bits select the phase voltage used as time base for harmonic calculations. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. If selected, phase C voltage is used.
15:10	Reserved	0	Reserved. These bits do not manage any functionality.

Table 55. LPOILVL Register (Address 0xEC00)

Bit	Mnemonic	Default Value	Description
2:0	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8.
7:3	LPLINE[4:0]	00000	The measurement period is (LPLINE + 1)/50 seconds.

Table 56. CONFIG2 Register (Address 0xEC01)

Bit	Mnemonic	Default Value	Description
0	EXTREFEN	0	When this bit is 0, it signifies that the internal voltage reference is used in the ADCs. When this bit is 1, an external reference is connected to the Pin 17 $REF_{IN/OUT}$.
1	I2C_LOCK	0	When this bit is 0, the $\overline{SS}$/HSA pin can be toggled three times to activate the SPI port. If I^2C is the active serial port, this bit must be set to 1 to lock it in. From this moment on, toggling of the $\overline{SS}$/HSA pin and an eventual switch into using the SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2 register locks the port. From this moment on, a switch into using I^2C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7880 changes PSMx power modes.
7:2	Reserved	0	Reserved. These bits do not manage any functionality.