MINI_STAR_4K board user manual

2021-03-12

1, about this manual

1.1 Manual content

Mini_star_4K Board Suite User Manual Is divided Into Four PartS:

1. Briefly describe the functional characteristics and hardware resources of the development board
2. This paper introduces the function, circuit and pin distribution of each part of the hardware circuit on the development board
3. Precautions for board use.

1.2 Applicable products

The information described in this manual can be applied to the following GW1NR series FPGAs:

- GW1NSR-LV4CQN48p

1.3 Related documentation

You can download and view it by logging into the High Cloud Semiconductor website www.gowinsemi.com.cn

The following related documents:

1. GW1NSR Series FPGA Product Data Sheet
2. GW1NSR Series FPGA Product Package and Pin Manual
3. GW1NSR-4 device Pinout manual
4. GW1NSR Series FPGA Product Programming Configuration Manual
5. Gowin Cloud Source Software User Manual

1.4 Technical support

1、For the latest FPGA technical information, please follow the public number MYMNIEYE;

2、Teaching video link update address:https://space.bilibili.com/507416742

3、Taobao Store: Small Eye Semiconductor

4、Official website:www.myminieye.com

5、Technical guidance QQ group:808770961

1.5 Terms, acronyms

The terms, acronyms, and related interpretations that appear in this manual are listed in Table 1-1.

Table 1-1 terms, acronyms

Terms, acronyms	Full name	meaning
FPGA	Field Programmable Gate Array	Field programmable door array
LED	Light Emitting Diode	Light-emitting diodes
LDO	Low Dropout Regulator	Low pressure differential linear regulator

GPIO	General Purpose Input Output	Universal input /output
LUT4	4-input Look-up Table	4 Enter the find table
S-SRAM	Shadow SRAM	Distributed static random memory
B-SRAM	Block SRAM	Block static random memory
PLL	Phase-locked Loop	Locking the phase ring
DLL	Delay-locked Loop	Delayed phase lock ring
DSP	Digital Signal Processing	Digital signal processing
QN48p	QN48p	QN48p package

2, the development board introduction

2.1 Overview

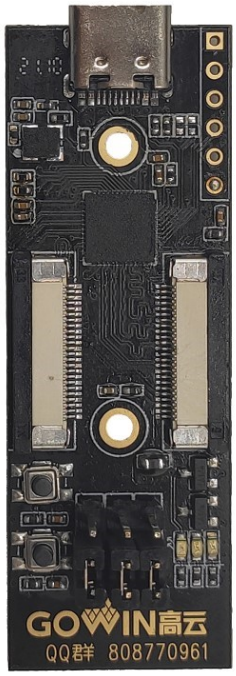


Figure 2-1 MINI_STAR_4K board

the MINI_STAR_4K board is based on the high cloud semiconductor GW1NSR series FPGA products as the core. The High Cloud Semiconductor GW1NSR Series FPGA product is the first generation ® of theLittleBee® family ofhigh cloud semiconductor fPGA products, a system-level package chip with integrated GW1NS series FPGA products and PSRAM memory chips, including GW1NSR-2C Devices,GW1NSR-4C devices and GW1NSR-2 devices,GW1NSR-4 devices.

Arm Cortex-M3 hardcore processors are embedded in GW1NSR-2C and GW1NSR-4C devices. In addition, the GW1NSR Series FPGA products are embedded in USB2 0 PHY, user flash, and ADC converter. The GW1NSR-2C / GW1NSR-4C device, with arm Cortex-M3 hardcore processors at its core, has the

minimum memory needed to implement system functionality; GW1NSR-2C devices enable a seamless connection between programmable logic devices and embedded processors, are compatible with a wide range of peripheral device standards, significantly reduce user costs, and can be widely used in industrial control, communications, Internet of Things, servo drive, consumption and other fields.

2.2 Board Kit

The board suite includes:

The development board

Quick application manual

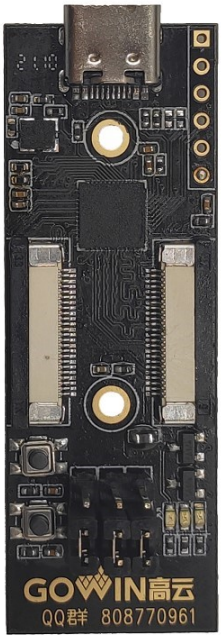


Figure 2 -2 MINI_STAR_4K board

2.3 PCB components

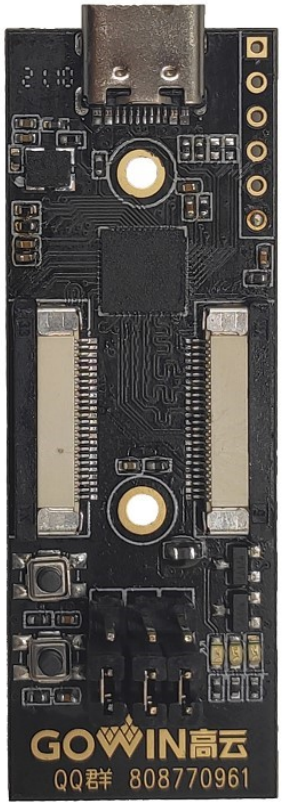


Figure 2-3 MINI_STAR_4K board

2.4 System framework

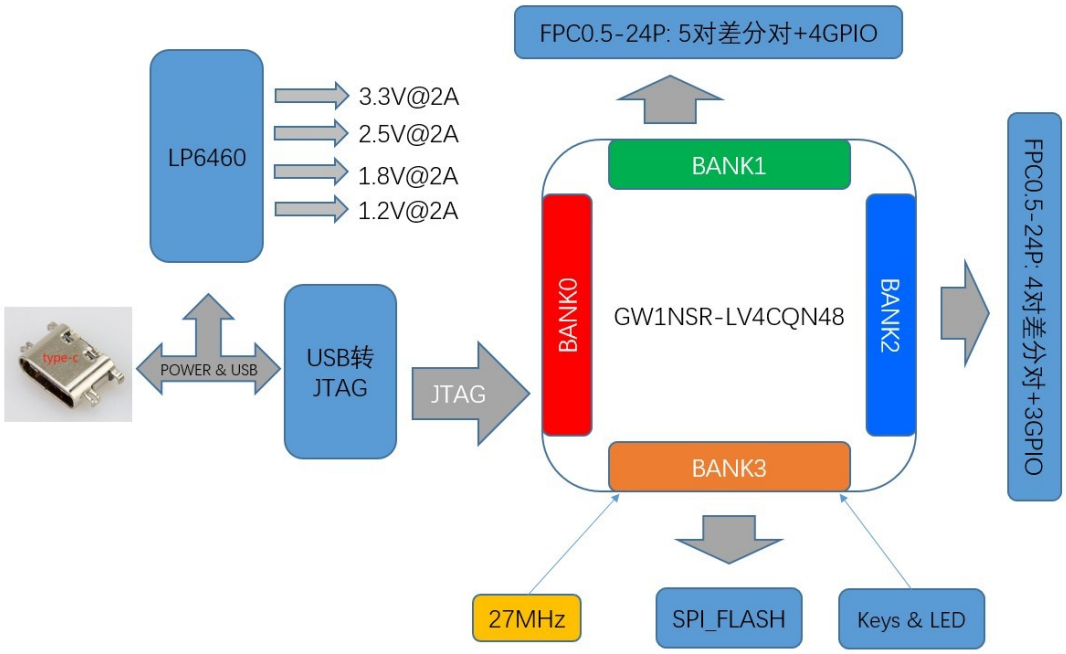


Figure 2-4 MINI_STAR_4K board

2.5 Features

The structure and characteristics of the board are as follows:

1. FPGA

   In QN48P package

   The ARM Cortex-M3 hardcore processor is embedded

2. FPGA Configuration Mode . . . JTAG

3. Clock resources

   27MHz clock crystal

8. keystroke

   2 key switches

9. LED

1 power LED (green).

2 user lights (green).

10. storage

□ 256Kbit flash

11. FPC extends the IO port

2 sets of FPC extended IO port

12. power supply

With voltage reverse protection;

2.6 indicator

Table 2 -1 A list of Combat board parameter metrics

serial number	project	parameter	Description of the function
1	5V power and download	5V DC-DC; Typc-USB	5V power supply. USB to JTAG interface
3	Tap the button	2 tap the button	Can be used as a test control input. (pressed low).
4	Light	2 LED	When the FPGA corresponding pin output signal is logic high, theLED is lit;
5	clock	1 way 27MHZ clock	Provides a 27MHz clock for FPGAs
6	Extend the interface	FPC seat extension	For control outputs such as cameras,HDMI,GPIO, etc
7	Operating temperature	Commercial grade from 0 to 70 degrees C	---
8	Ambient humidity	20% to 90%, non-condensation	---
9	Mechanical size	20mm×57mm	---
10	PCB specifications	4 layers, with white on black background	---

11	Power supply	5V/1A,typec-USB interface powered	---
12	System power consumption	---	---

2.7 Mechanical dimensions

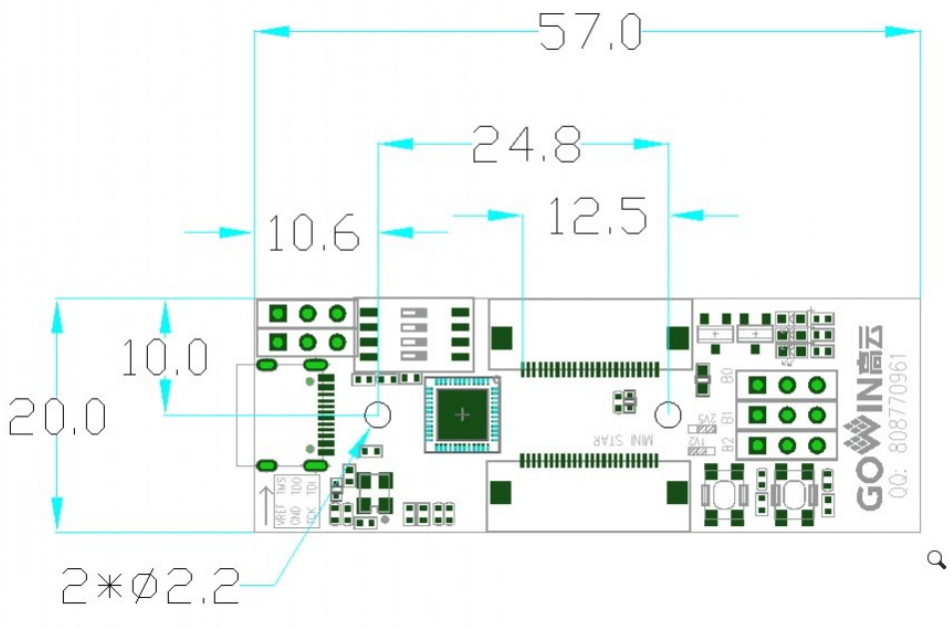


Figure 2-5 MINI_STAR_4K board

3, the development board details

3.1,FPGA module

3.1.1 Overview

GW1NSR-LV4CQN48P FPGA Product Resource Information is shown in Table 3-1.

Table 3-1 GW1NSR Series FPGA Product Information List

Devices	GW1NSR-4
Logical unit(LUT4).	4608
Register (FF).	3456
Block static random memory B-SRAM(bits)	180K
The number of block static random memory B-SRAM(个)	10
User flash (bits).	256K
HyperRAM(bit)	64M

Multiplier (18x18Multiplier)	16
Phase Lock ring (PLLs).	2
Hard-core processor	Cortex-M3
I/O Bank 总	4
The maximum number of users I/O	39
Nuclear voltage	1.2V

3.1.2 I/O BANK 说

The GW1NSR Series FPGA products are divided into four I/O BANKS zones, and Figure 3-1 is a holistic diagram of I/OBANKS for the GW1NSR Series FPGAs. Figure 3-2 is a diagram of the distribution of the QN48P package pins.

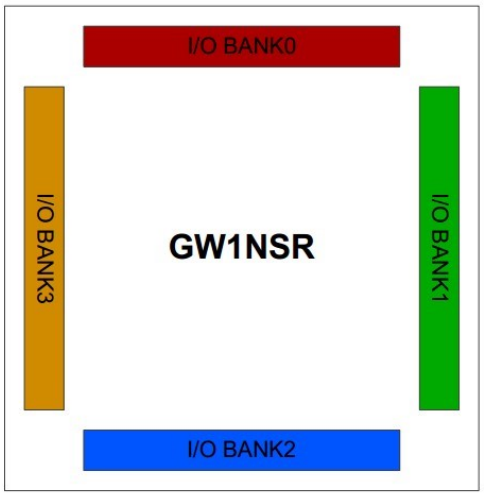


Figure 3-1 GW1NSR-LV4CQN48P Product I/O BANK Overall Diagram

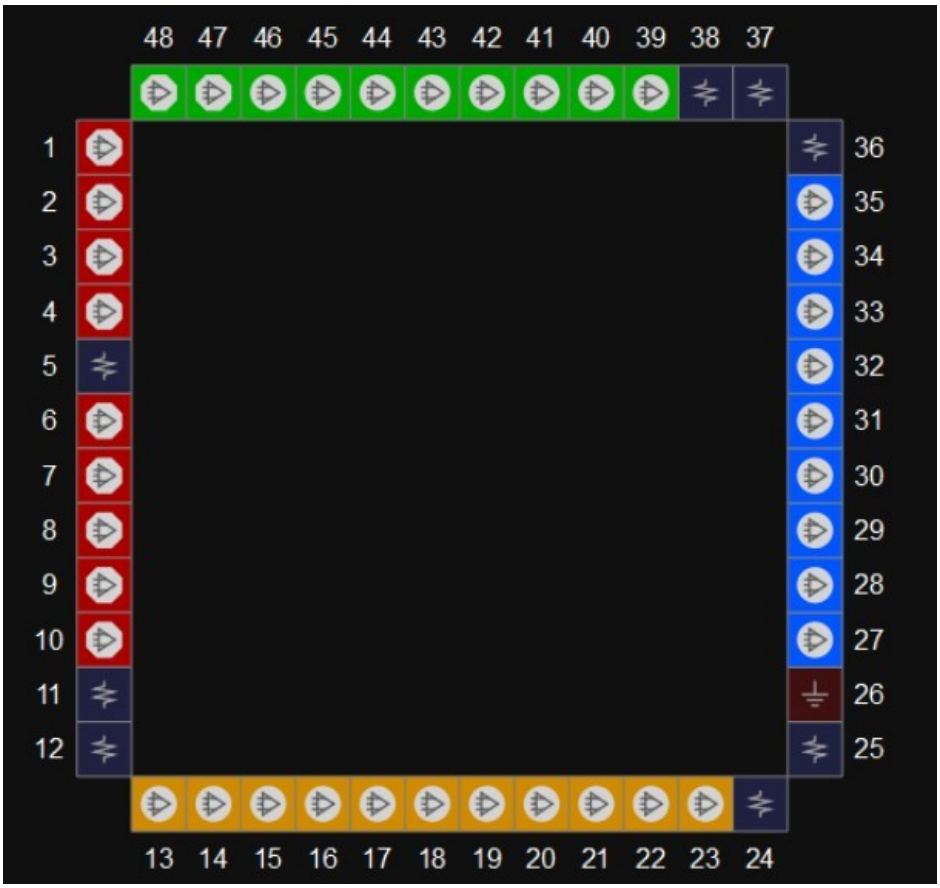


Figure 3-2 GW1NSR-LV4CQN48P package pin distribution diagram (top view).

Table 3-2 FPGA I/O BANK Voltage and Function Distribution

BANK	voltage	function	I/O occupancy

0	1.2V/2.5V	Jtag	4 GPIO
		IO extension	1 pair of differential pairs,2 GPIO
1	1.2V/2.5V	IO extension	5 pairs of differential pairs
2	1.2V/2.5V	IO extension	4 pairs of differential pairs,1 GPIO
3	1.8V	27M clock	1 GPIO
		LED	2 GPIO
		keystroke	2 GPIO
		spi-flash	5 GPIO

3.2 Download

3.2.1 Overview

The board provides a USB download interface, which is implemented by the A channel of the FT2232 USB conversion chip. Internal ARM Cortex-M3 hardcore processor downloads are also downloaded through the same set of IOs. The USB power supply needs to be maintained when debugging the download arm core, while the dial switch is dialed to disconnect the USB to JTAG module.

The downloaded connection diagram looks like the following image.

3.2.2 USB download circuit

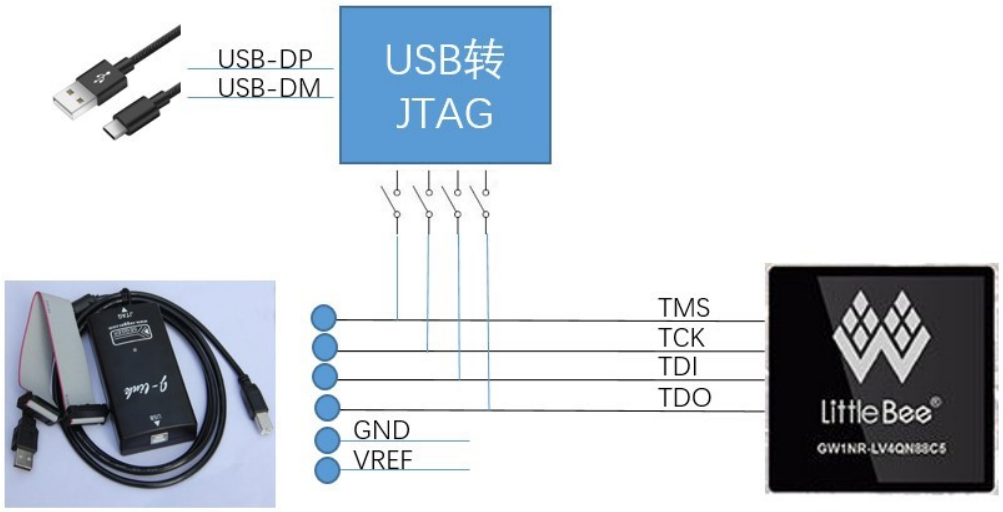


Figure 3-5 FPGA download circuit schematic

3.2.3 Pin distribution

Table 3-2 Download circuit pin assignments

Signal name	FPGA Pin No	BANK	description	I/O电平
FPGA_ TMS	6	0	Tms	3.3V
FPGA_ TCK	7	0	TCK	3.3V
FPGA_ TDI	3	0	Tdi	3.3V
FPGA_ TDO	4	0	TDO	3.3V

3.3 Power supply

3.3.1 Overview

The board provides DC5V input via the typec-USB interface, with 1.5A overcurrent protection against anti-reversal protection;

The input DC5V power supply passes through the power supply IC conversion output on the board 3.3V, 2.5, 1.8V, 1.2V

3.3.2 Power system allocation

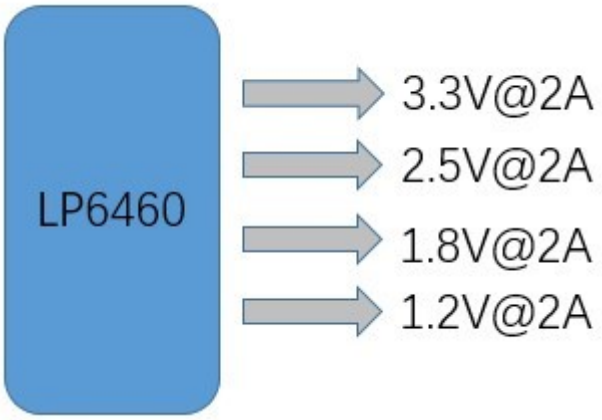


Figure 3-6 Power Circuit

3.4 Clock

3.4.1 Overview

The board provides the FPGA with a 27MHz active crystal connected to the global clock pin.

3.4.2 Clock circuit diagram

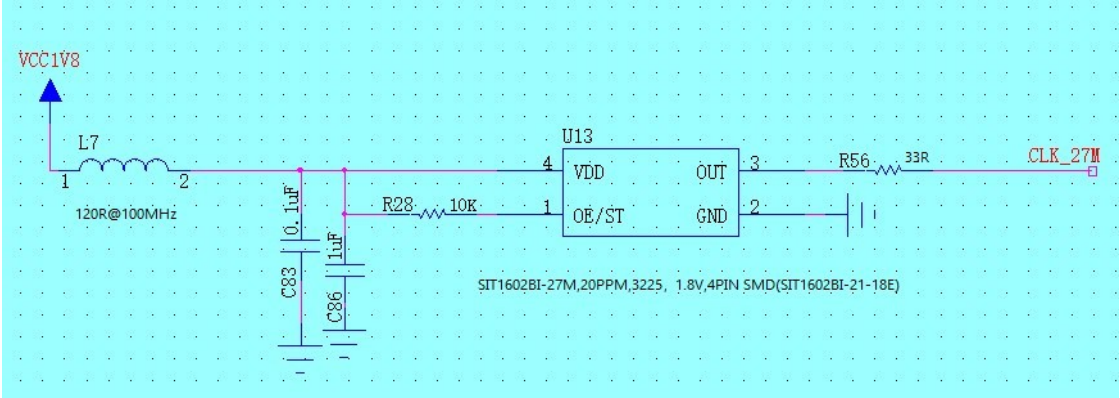


Figure 3-7 Clock-connected schematic

3.4.3 Pin distribution

Table 3-5 FPGA Clock with Reset Pin Allocation

Signal name	FPGA Pin No	BANK	description	I/O电平
CLK_27MHZ_IN	22	3	27MHz active crystal input	1.8V

3.5 LED

3.5.1 Overview

There are 2 user LEDs in the board that can display the desired status via LED lights. THE LED LIGHT CAN BE TESTED IN THE FOLLOWING WAYS:

When the FPGA corresponding pin output signal is logic high, theLED is lit;

When the output signal is low, theLED goes out

3.5.2 LED circuit

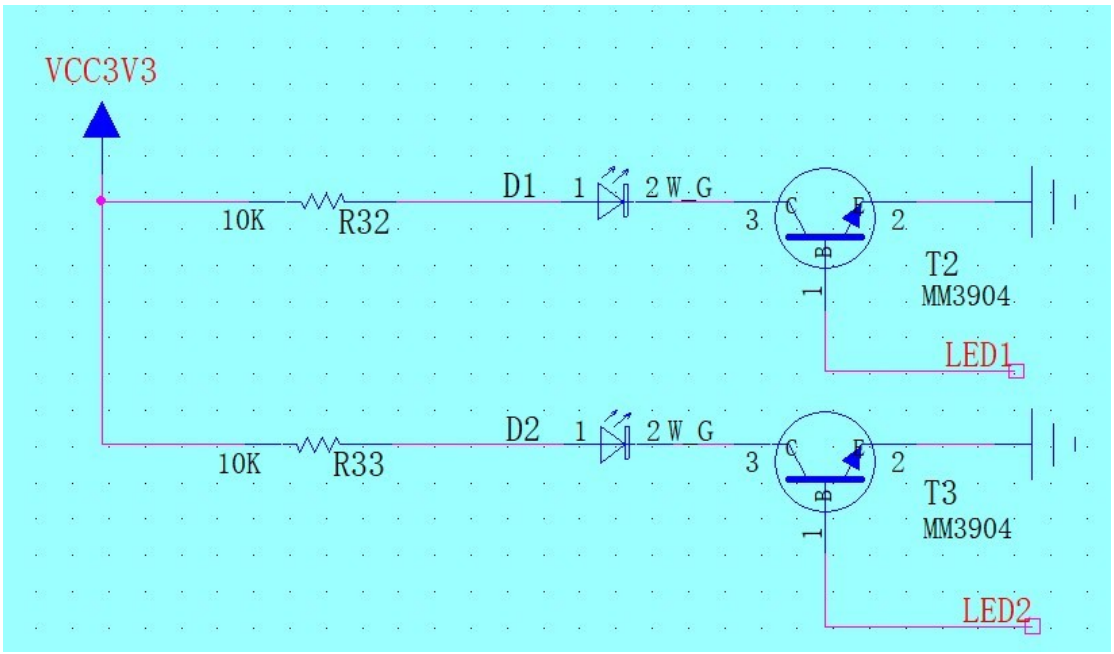


Figure 3-8 LED circuit schematic

3.5.3 Pin distribution

Table 3-6 LED pin allocation

Signal name	FPGA Pin No	BANK	description	I/O电平
LED1	13	3	LED 1	1.8V
LED2	14	3	LED 2	1.8V

3.6 Keystrokes

3.6.1 Overview

The board has 2 key switches that allow the user to enter a low level into the corresponding FPGA pin via manual control, which can be used as a test control input. (pressed low).

3.6.2 Key circuit

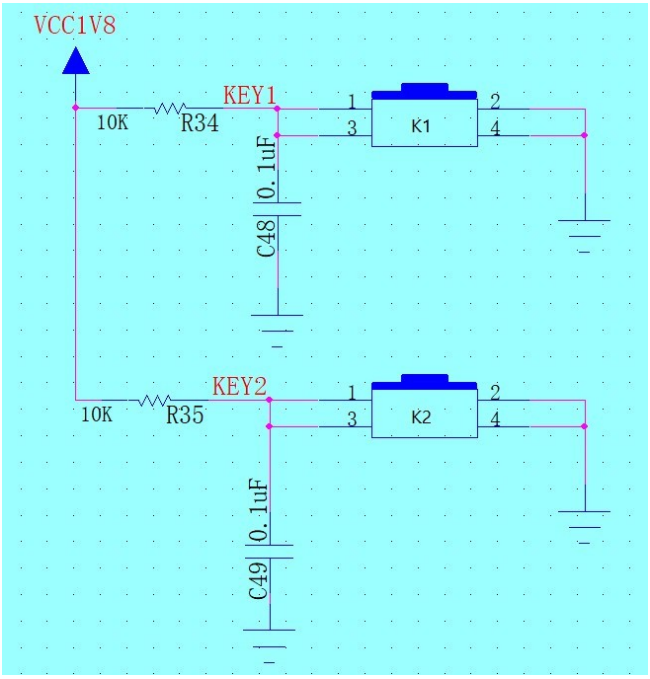


Figure 3-10 Key Circuit Schematic

3.6.3 Pin distribution

Table 3-8 Key Pin Allocation

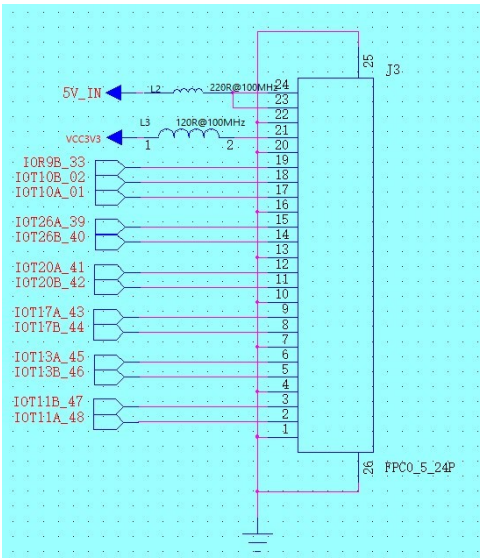
Signal name	FPGA Pin No	BANK	description	I/O电平
KEY1	23	3	Key 1	1.8V
KEY2	20	3	Key 2	1.8V

3.7 Extending the IO

3.7.1 Overview

The board contains two sets of extended IOs,each led by two 0.5mm-24P FPC seats. The first group consists of: 1,DC5V, DC3.3V power output;2,BANK1's 5-pair difference pair to 3,BANK0's pair of difference pairs, and BANK2's one GPIO. The second group consists of:1,DC5V, DC3.3V power output;2, BANK2's 4 pairs of differential pairs; 1 GPIO(IOR9B_33IO shared with the first group); 3,BANK0's 2 GPIO. Users can support the official recommended transfer board for camera input - HDMI output experiments, etc.

3.7.2 Extended IO schematics



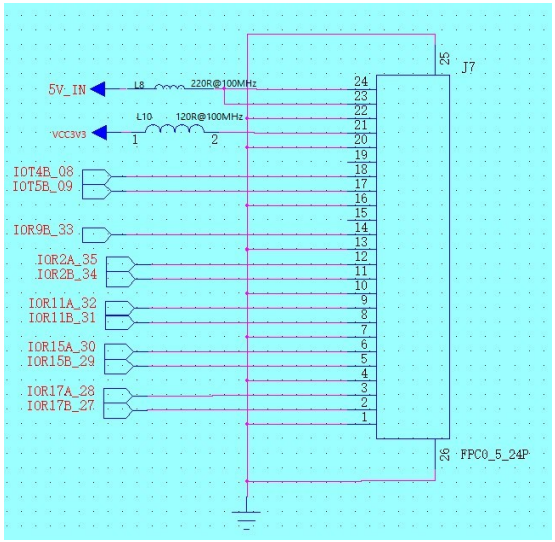


Figure 3-19 Extends the schematic

3.7.3 Pin distribution

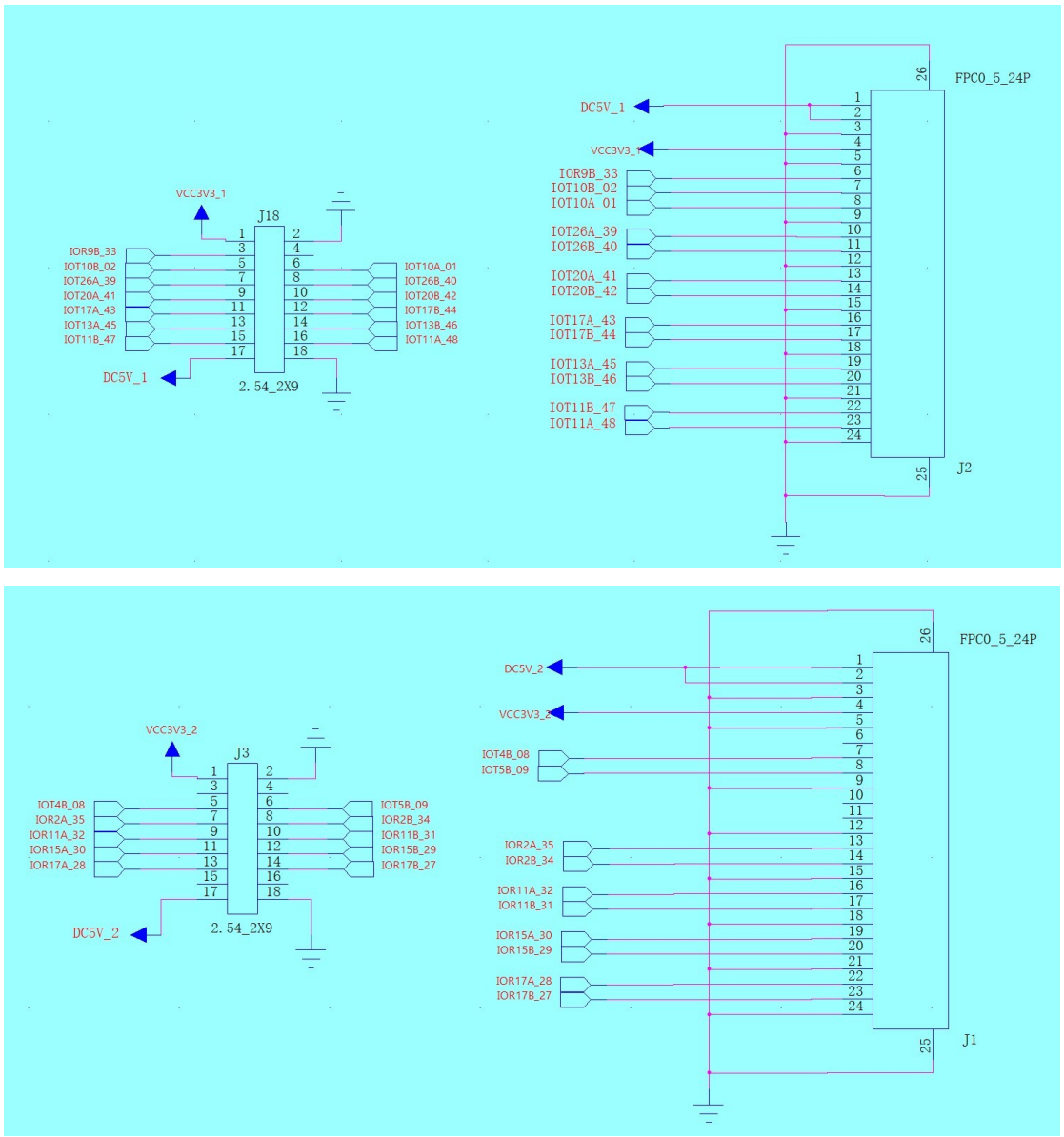
Signal name	FPGA Pin No	BANK	description	I/O电平
IOT10A_01	1	0	The difference is right	1.2V/2.5V
IOT10B_02	2	0		1.2V/2.5V
IOT4B_08	8	0	GPIO	1.2V/2.5V
IOT5B_09	9	0	GPIO	1.2V/2.5V
IOR17B_27	27	2	The difference is right	1.2V/2.5V
IOR17A_28	28	2		1.2V/2.5V
IOR15B_29	29	2	The difference is right	1.2V/2.5V
IOR15A_30	30	2		1.2V/2.5V
IOR11B_31	31	2	The difference is right	1.2V/2.5V
IOR11A_32	32	2		1.2V/2.5V
IOR9B_33	33	2	GPIO	1.2V/2.5V
IOR2B_34	34	2	The difference is right	1.2V/2.5V
IOR2A_35	35	2		1.2V/2.5V
IOT26A_39	39	1	The difference is right	1.2V/2.5V
IOT26B_40	40	1		1.2V/2.5V
IOT20A_41	41	1	The difference is right	1.2V/2.5V
IOT20B_42	42	1		1.2V/2.5V
IOT17A_43	43	1	The difference is right	1.2V/2.5V
IOT17B_44	44	1		1.2V/2.5V
IOT13A_45	45	1	The difference is right	1.2V/2.5V
IOT13B_46	46	1		1.2V/2.5V
IOT11B_47	47	1	The difference is right	1.2V/2.5V
IOT11A_48	48	1		1.2V/2.5V

3.8 Supporting the expansion of the experimental board

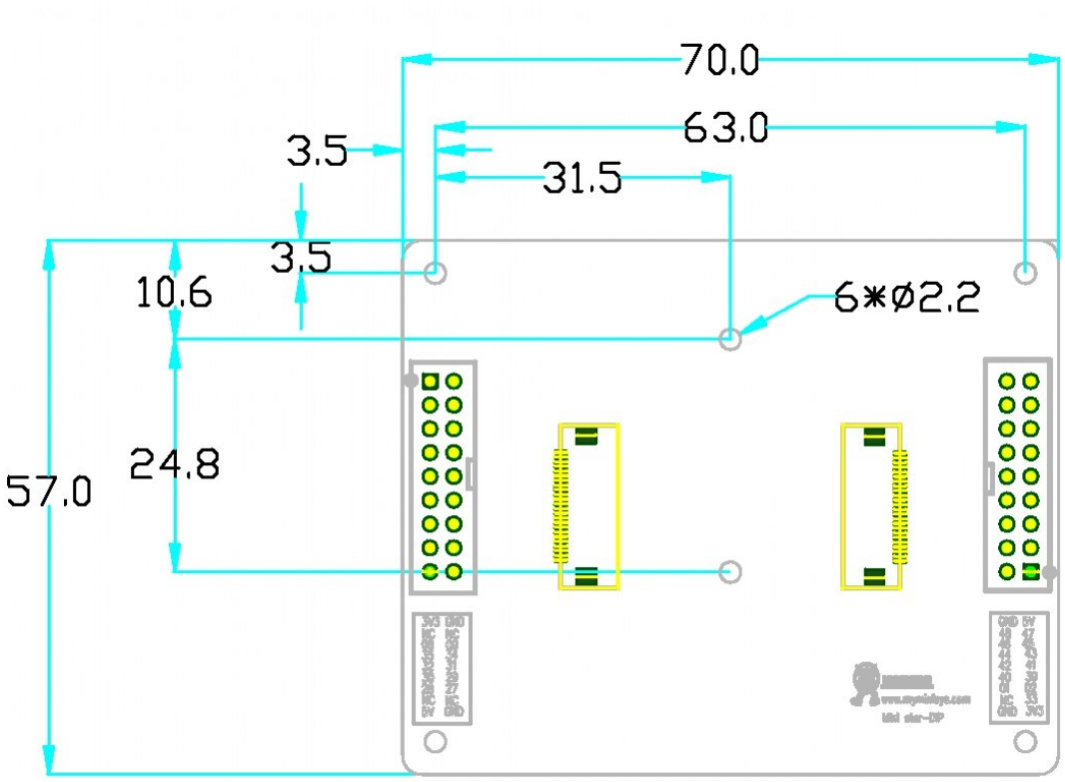
3.8.1 Overview

For the convenience of simple experiments, the development board is equipped withan FPC transfer needle test board. Other lab boards should be purchased or made by yourself.

3.8.2 Extended Lab Board Schematic



3.8.2 Extended test board size chart



4, the use of the board

4.1 Project Import

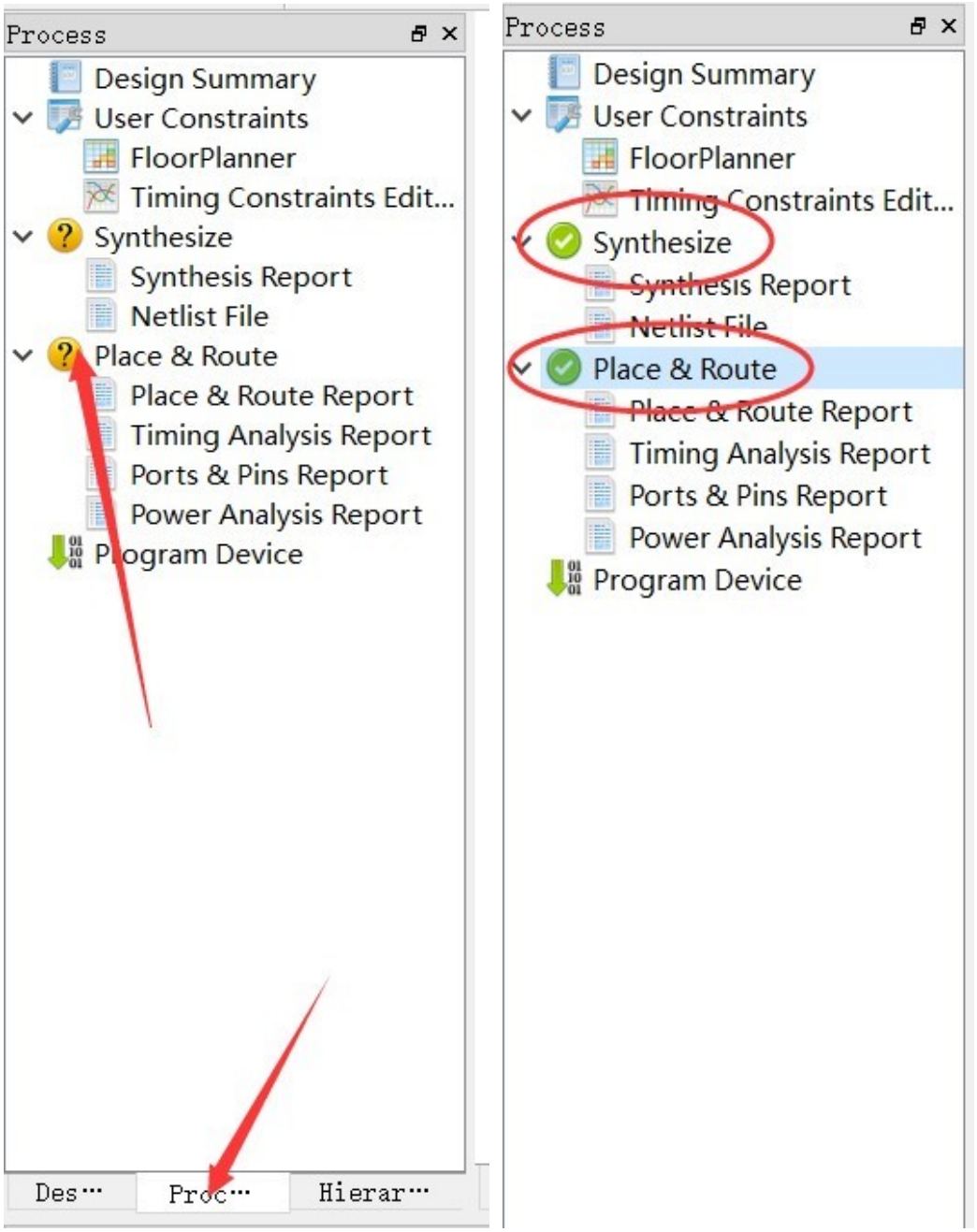
See the SUG100-1.7_Gowin Cloud Source Software User Guide for specific software operating instructions

1. Click directly on the .gprj file

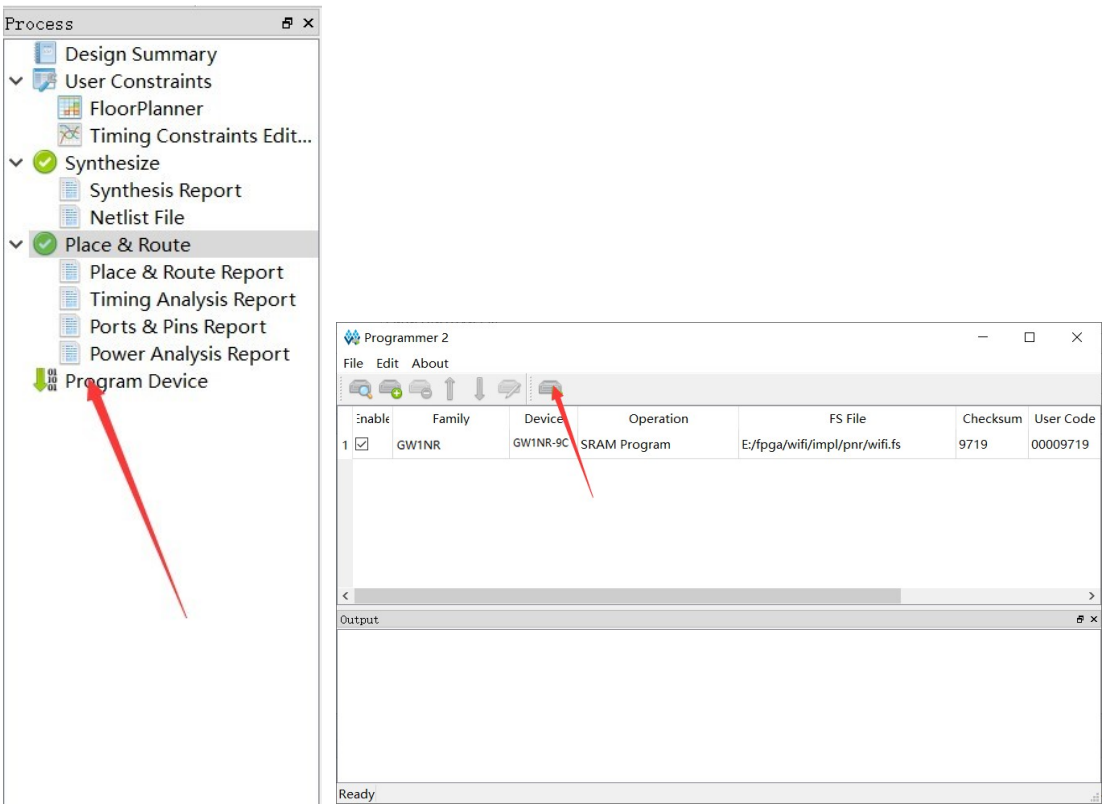
2. After entering the development software, click on the file "→" to open "Select .gprj file import

4.2 The program compiles and downloads

1. After writing the program, save the click Process click Place-Route compilation, after compilation through the front will appear a green tick



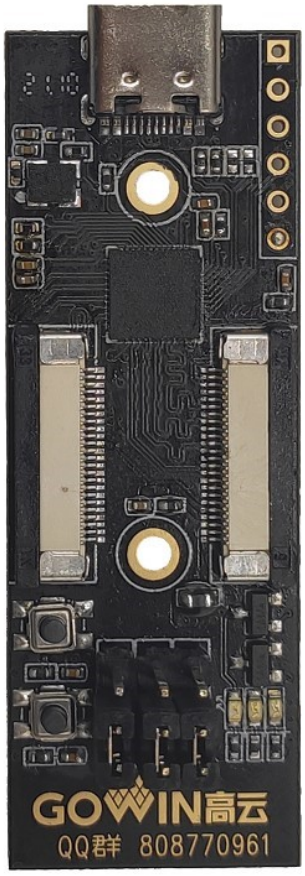
2. After compilation, double-click on Program Device to pop up the download window and click to start downloading



4.3 Routine operation and phenomenon description

The development board set companion video will be available in Bilibili(website : https://space.bilibili.com/507416742)and other websites and related public numbers are welcome to post welcome attention.

4.4 Precautions for the use of the board



1. When using the development board, pay attention to light and light, and do a good job of static protection.

2. When downloading bitstream files for internal flash or external Flash, you need to set

The MODE foot state is on the correct configuration value.

3. When connecting the module, the power must first be turned off.