RISC V Disassembly Flowchart

Instruction (32 bits)

Opcode (7 bits)

- **0x3** → I-Type (Loads)
- **0x33** → R-Type
- **0X13** → I-Type (Non Loads)
- **0x23** → S Type (Stores)
- **0x63** → SB (Branches)
- **0x67 or 0x6F** → Jumps (JAL, JALR)
- **0x37 or 0x17** → LUI or AUIPC
- **0x73** → Ecall EBreak (Imm)

I-Type (Loads) → Funct3 → **(0x0…0x2)** Loads (ld[w|h|b],unsigned?)

R-Type → Funct3 (3 bits) → **0x1..0x7** → Funct7 7 bits
- **0x00** → add, xor, sl
- ...
- **0x20** → sub, sra

I-Type (Non Loads) → Funct3 (3 bits) → **0x1..0x7** → Funct7 7 bits
- **0x00** → addi, xori, sli
- **0x20** → srai

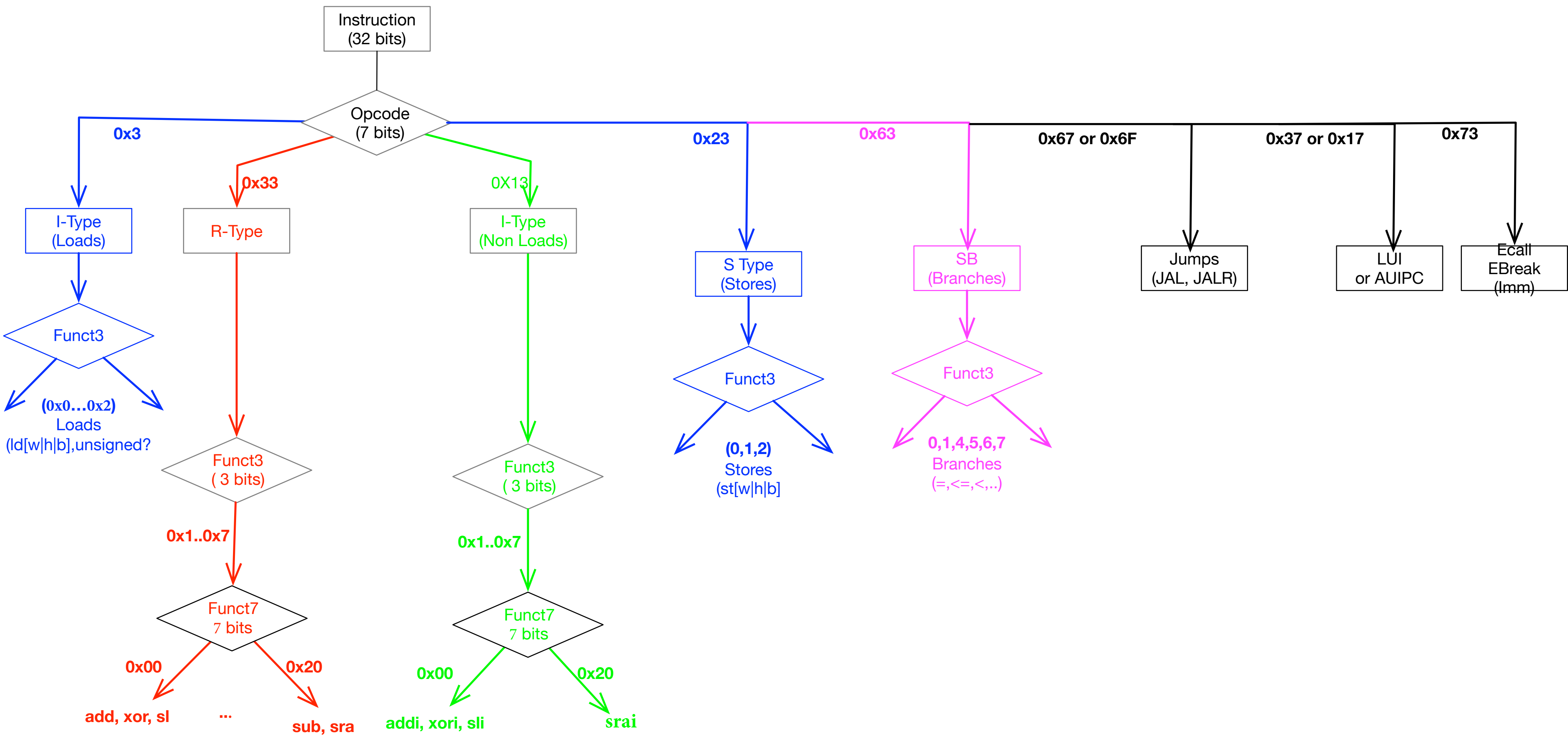*** No subi. Can be implemented using addi with -ve**

* Don't forget about immediate value embedded in instruction

S Type (Stores) → Funct3 → **(0,1,2)** Stores (st[w|h|b]

SB (Branches) → Funct3 → **0,1,4,5,6,7** Branches (=,<=,<,..)