



## 1. Description

### 1.1. Project

Project Name	SZWA
Board Name	STM32L476G-DISCO
Generated with:	STM32CubeMX 6.0.0
Date	03/14/2021

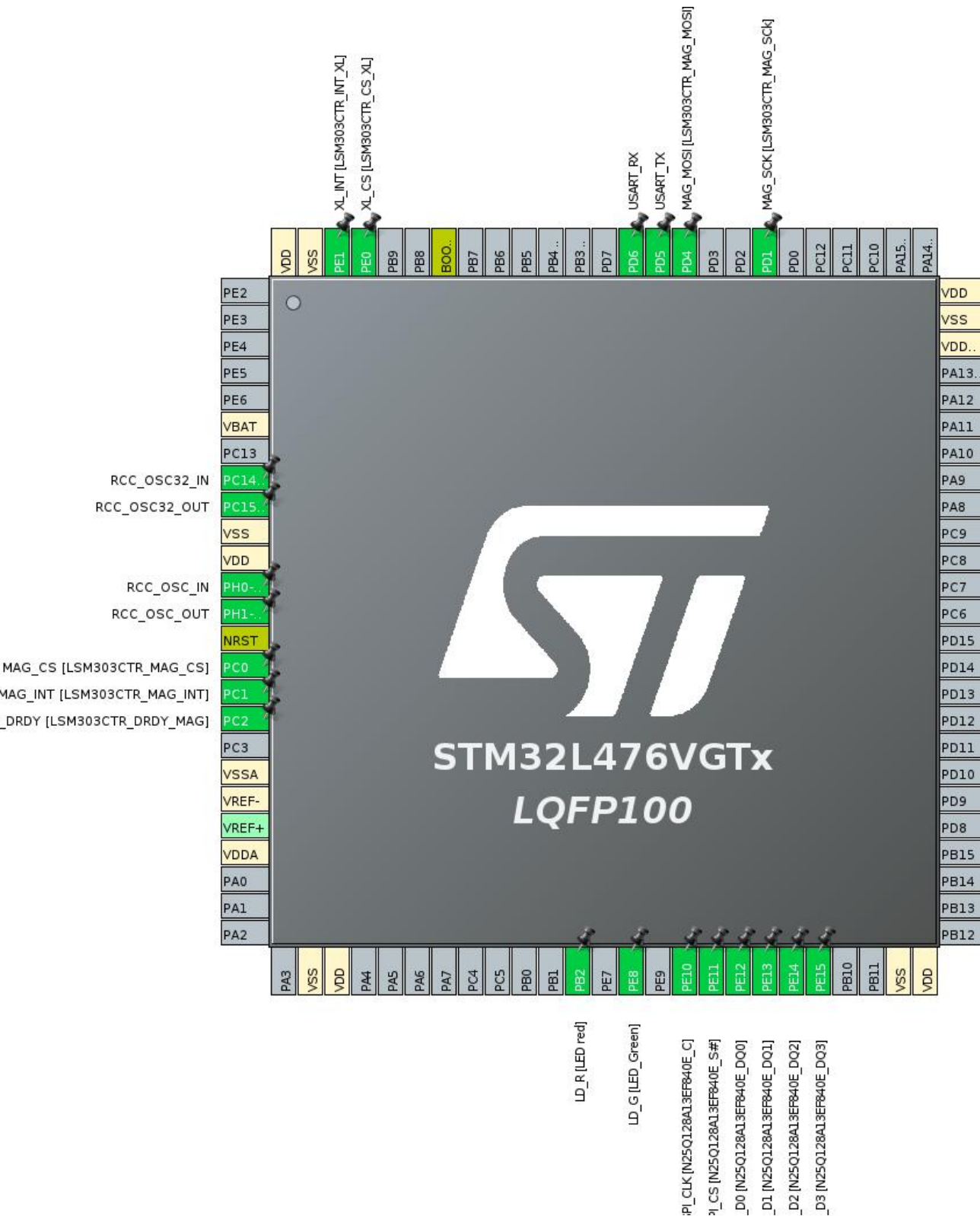
### 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476VGTx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



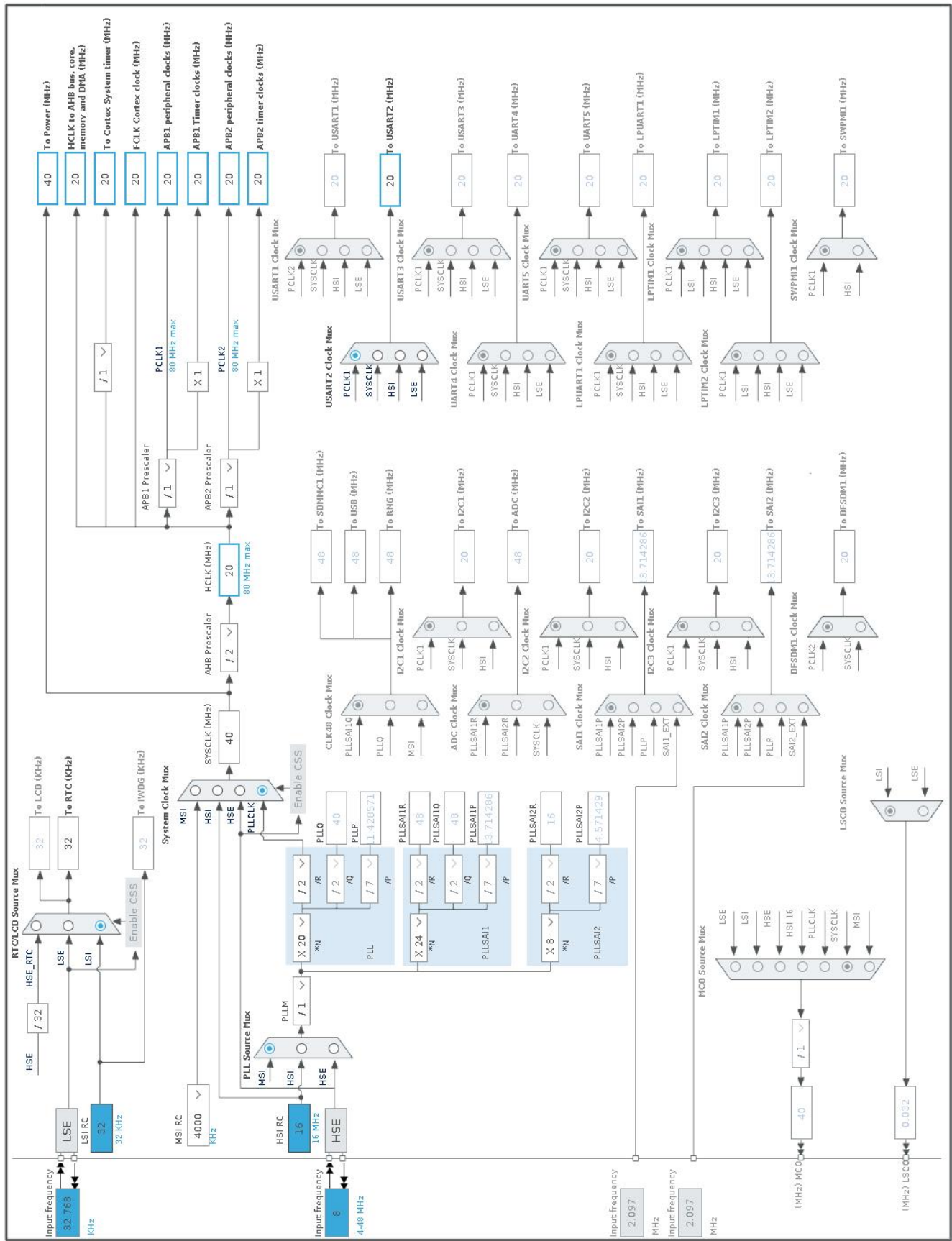
### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Input	MAG_CS [LSM303CTR_MAG_CS]
16	PC1 *	I/O	GPIO_Input	MAG_INT [LSM303CTR_MAG_INT]
17	PC2 *	I/O	GPIO_Input	MAG_DRDY [LSM303CTR_DRDY_MAG]
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
27	VSS	Power		
28	VDD	Power		
37	PB2 *	I/O	GPIO_Output	LD_R [LED red]
39	PE8 *	I/O	GPIO_Output	LD_G [LED Green]
41	PE10	I/O	QUADSPI_CLK	QSPI_CLK [N25Q128A13EF840E_C]
42	PE11	I/O	QUADSPI_NCS	QSPI_CS [N25Q128A13EF840E_S#]
43	PE12	I/O	QUADSPI_BK1_IO0	QSPI_D0 [N25Q128A13EF840E_DQ0 ]
44	PE13	I/O	QUADSPI_BK1_IO1	QSPI_D1 [N25Q128A13EF840E_DQ1 ]
45	PE14	I/O	QUADSPI_BK1_IO2	QSPI_D2 [N25Q128A13EF840E_DQ2 ]
46	PE15	I/O	QUADSPI_BK1_IO3	QSPI_D3 [N25Q128A13EF840E_DQ3 ]
49	VSS	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
50	VDD	Power		
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
82	PD1	I/O	SPI2_SCK	MAG_SCK [LSM303CTR_MAG_SCK]
85	PD4	I/O	SPI2_MOSI	MAG_MOSI [LSM303CTR_MAG_MOSI]
86	PD5	I/O	USART2_TX	USART_TX
87	PD6	I/O	USART2_RX	USART_RX
94	BOOT0	Boot		
97	PE0 *	I/O	GPIO_Output	XL_CS [LSM303CTR_CS_XL]
98	PE1	I/O	GPIO_EXTI1	XL_INT [LSM303CTR_INT_XL]
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	SZWA
Project Folder	/home/mbober/STM32CubeIDE/workspace_1.4.0/SZWA
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_QUADSPI_Init	QUADSPI
4	MX_SPI2_Init	SPI2
5	MX_USART2_UART_Init	USART2
6	MX_RTC_Init	RTC

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476VGTx
Datasheet	DS10198_Rev4

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1



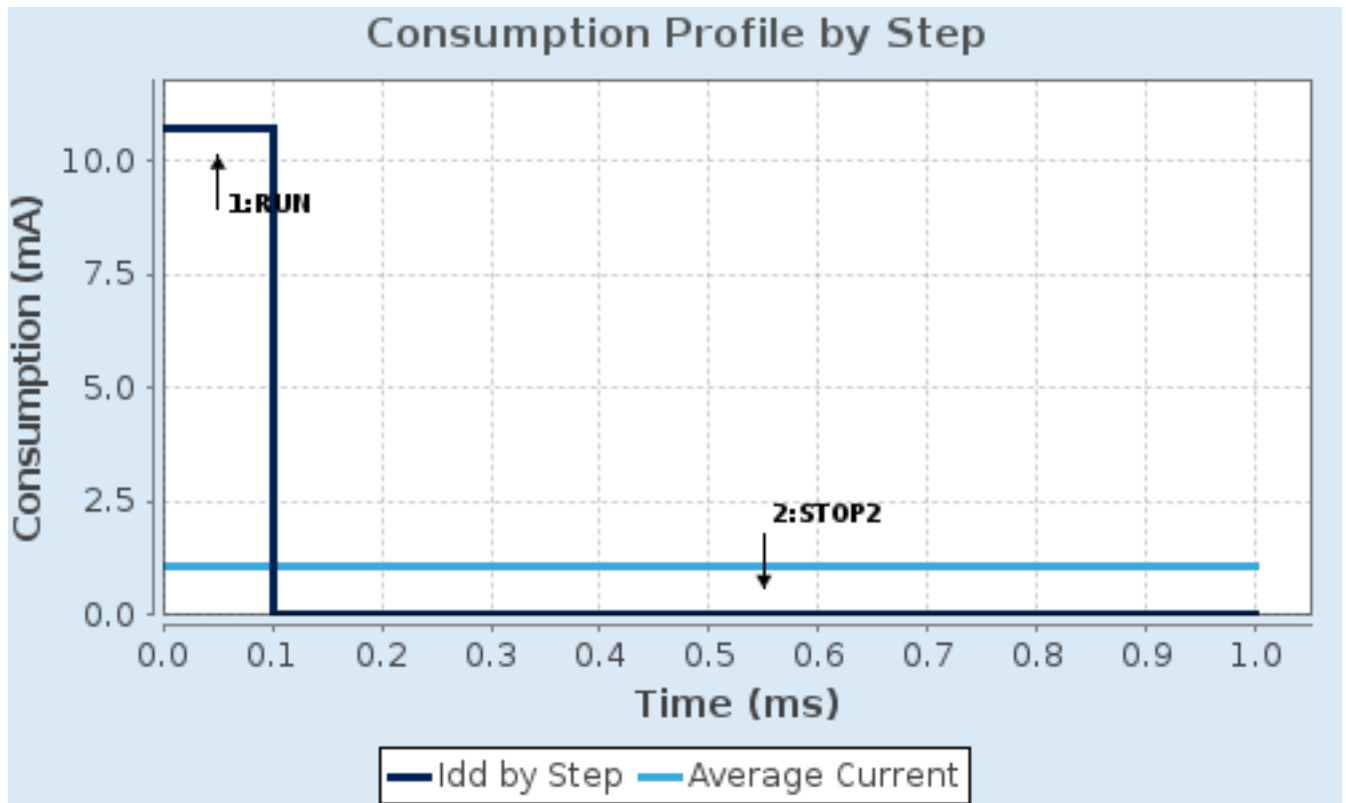
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP2
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Range1-High	NoRange
<b>Fetch Type</b>	SRAM2	n/a
<b>CPU Frequency</b>	80 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	ALL CLOCKS OFF
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	10.7 mA	1.18 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	100.0	0.0
<b>Ta Max</b>	103.65	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

#### 6.6. Chart



## 7. IPs and Middleware Configuration

### 7.1. GPIO

### 7.2. QUADSPI

#### Single Bank: Quad SPI Line

##### 7.2.1. Parameter Settings:

###### General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low

### 7.3. RCC

#### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### Low Speed Clock (LSE) : Crystal/Ceramic Resonator

##### 7.3.1. Parameter Settings:

###### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	<b>Enabled *</b>
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

###### RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Enabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

###### Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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## 7.4. RTC

**mode: Activate Clock Source**

**mode: Activate Calendar**

### 7.4.1. Parameter Settings:

#### **General:**

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

#### **Calendar Time:**

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

#### **Calendar Date:**

Week Day	Monday
Month	January
Date	1
Year	0

## 7.5. SPI2

**Mode: Half-Duplex Master**

### 7.5.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

#### **Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>10.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

#### **Advanced Parameters:**

CRC Calculation	Disabled
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NSSP Mode	Enabled
NSS Signal Type	Software

## 7.6. SYS

**Timebase Source: SysTick**

## 7.7. USART2

**Mode: Asynchronous**

### 7.7.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

#### **Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
QUADSPI	PE10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	QSPI_CLK [N25Q128A13EF840E_C]
	PE11	QUADSPI_NCS	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	QSPI_CS [N25Q128A13EF840E_S#]
	PE12	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	QSPI_D0 [N25Q128A13EF840E_DQ 0]
	PE13	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	QSPI_D1 [N25Q128A13EF840E_DQ 1]
	PE14	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	QSPI_D2 [N25Q128A13EF840E_DQ 2]
	PE15	QUADSPI_BK1_I O3	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	QSPI_D3 [N25Q128A13EF840E_DQ 3]
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PD1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	MAG_SCK [LSM303CTR_MAG_SCK]
	PD4	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	MAG_MOSI [LSM303CTR_MAG_MOSI ]
USART2	PD5	USART2_TX	Alternate Function Push Pull	<b>Pull-up *</b>	<b>Very High</b> *	USART_TX
	PD6	USART2_RX	Alternate Function Push Pull	<b>Pull-up *</b>	<b>Very High</b> *	USART_RX
GPIO	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MAG_CS [LSM303CTR_MAG_CS]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MAG_INT [LSM303CTR_MAG_INT]
	PC2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MAG_DRDY [LSM303CTR_DRDY_MAG]
	PB2	GPIO_Output	Output Push Pull	<b>Pull-up *</b>	<b>Very High *</b>	LD_R [LED red]
	PE8	GPIO_Output	Output Push Pull	<b>Pull-up *</b>	<b>Very High *</b>	LD_G [LED_Green]
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	XL_CS [LSM303CTR_CS_XL]
	PE1	GPIO_EXTI1	<b>External Event Mode with Rising edge trigger detection *</b>	No pull-up and no pull-down	n/a	XL_INT [LSM303CTR_INT_XL]

## 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI2 global interrupt	unused		
USART2 global interrupt	unused		
QUADSPI global interrupt	unused		
FPU global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Prefetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true

\* User modified value



## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/DM00108832.pdf">http://www.st.com/resource/en/datasheet/DM00108832.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/DM00083560.pdf">http://www.st.com/resource/en/reference_manual/DM00083560.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/DM00046982.pdf">http://www.st.com/resource/en/programming_manual/DM00046982.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/DM00111498.pdf">http://www.st.com/resource/en/errata_sheet/DM00111498.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
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