How Ocarina of Time was decompiled

Darius Engler November 06, 2021

Presentation

- Presentation
- Matching decompilation

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- Matching decompilation
- Workflow/Tooling

Presentation

Code documentation

- Code documentation
- Glitch hunting (speedrunning)

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- Modding

- Code documentation
- Glitch hunting (speedrunning)
- Modding
- Fun/Challenge

Byte identical output

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- Harder

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- Equivalence testing becomes trivial (we just compare the hashes)

What do we need to figure out?

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• Which compiler was used?

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- Which compilers flags were used?

• C compiler developed by Silicon Graphics (SGI)

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- Part of IRIX OS

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- Discontinued

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IDO

00000000 <test>:

0: 03e00008 jr ra

4: afa40000 sw a0,0(sp)

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IDO GCC

00000000 <test>:

0: 03e00008 jr ra 4: afa40000 sw a0,0(sp) 00000000 <test>:

0: 03e00008 4: 00000000 jr nop

ra

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- Most of the code compiled with IDO 7.1
- Some of "libultra" compiled with IDO 5.3

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Switched to static recompilation of IDO

Static Recompilation

Static Recompilation

Translates assembly to ugly but compilable C code

```
1 a3 = 0x0;
 2 a3 = a3 + qp;
 3 a3 = MEM_U32(a3 + -32684);
 4 a0 = MEM_U32(sp + 0);
 5 a1 = sp + 0x4;
 6 a3 = MEM U32(a3 + 0);
 7 \text{ at} = 0 \times \text{fffffff};
 8 \text{ sp} = \text{sp & at};
 9 a2 = a1 + 0x4;
10 \ v0 = a0 << 2;
11 \text{ sp} = \text{sp} + 0 \text{xffffffe0};
12 if (a3 != 0) \{a2 = a2 + v0;
13 goto L40cf80;}
14 a2 = a2 + v0;
15 \text{ at} = 0x0;
16 \text{ at} = \text{at} + \text{gp};
17 \text{ at} = MEM\_U32(at + -32684);
18 MEM_U32(at + 0) = a2;
19 L40cf80:
20 \text{ at} = 0x0;
21 at = at + gp;
22 \text{ at} = MEM\_U32(\text{at} + -30028);
```

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⇒ We get a native binary

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Static Recompilation

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QEMU

real 3m17,946s user 22m24,901s sys 1m4,315s

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Translates assembly to ugly but compilable C code

⇒ We get a native binary

QEMU

real 3m17,946s user 22m24,901s sys 1m4,315s

Static Recomp

real 1m12,407s user 6m45,375s sys 0m40,974s

```
1 a3 = 0x0;
 2 a3 = a3 + qp;
 3 a3 = MEM_U32(a3 + -32684);
 4 a0 = MEM_U32(sp + 0);
 5 a1 = sp + 0x4;
 6 a3 = MEM U32(a3 + 0);
 7 \text{ at} = 0 \times \text{fffffff0};
 8 \text{ sp} = \text{sp & at};
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- Some files compiled with -mips3 -32

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- Some of libultra compiled with -O1
- Some files compiled with -O2 -g3
- Some files compiled with -mips3 -32
- Some files compiled with -trapuv

Workflow/Tooling

IDO alignes every object file to 0x10

```
80001b0c 0c 00 0c a0
                                              osRecvMesq
         80001b10 24 06 00 01
                                  li
                                              size.0xl
         80001b14 00 00 10 25
                                              v0, zero, zero
         80001b18 8f bf 00 24
                                              ra, 0x24(sp)
                              LAB 80001blc
                                                                              XREF[1]: 80001
         80001blc 27 bd 00 70
                                              sp, sp, 0x70
         80001b20 03 e0 00 08
         80001b24 00 00 00 00
                                              00h
         80001b29 00
         80001b2a 00
                                              00h
                                  22
         80001b2b 00
                                              OOh
         80001b2c 00
                                              00h
         80001b2d 00
                                              00h
         80001b2e 00
                                  22
                                              00h
                                              00h
          80001b2f 00
                                                         FUNCTION
                              undefined * stdcall Yaz0 FirstDMA(void)
              undefined *
                                v0 lo:4
              undefined4
                                Stack[-0xc]:4 local c
                                                                                       XREF[21:
              undefined4
                                Stack[-0x14]:4 local 14
                                                                                       XREF[2]:
                              Yaz0 FirstDMA
                                                                                          Yaz0
         80001b30 3c 02 80 01
                                             v0,0x8001
         80001b34 8c 42 44 e0
                                             v0.offset sYaz0CurDataEnd(v0)
         80001b38 3c 07 80 01
                                             a3.0x8001
         80001b3c 3c 01 80 01
                                             at,0x8001
n Call Trees: DmaMgr_SendRequest1 - (OotEuropeMQDbg)
```

IDO alignes every object file to 0x10

Ш		80001b0c 0c 00 0c		osRecvMesg		uno					
Ш		80001b10 24 06 00	01 _1i	size,0xl							
Ш		80001b14 00 00 10	25 or	v0,zero,zero							
Ш		80001b18 8f bf 00	24 lw	ra,0x24(sp)							
Ш											
₽			LAB_80001b1	c	XREF[1]:	80001k					
ш		80001blc 27 bd 00	70 addiu	sp, sp, 0x70							
П		80001b20 03 e0 00	08 jr	ra							
ш		80001b24 00 00 00	00 _nop								
ш		80001b28 00	??	00h							
П		80001b29 00	??	00h							
ш		80001b2a 00	??	00h							
П		80001b2b 00	??	00h							
П		80001b2c 00	??	00h							
П		80001b2d 00	??	00h							
П		80001b2e 00	??	00h							
П		80001b2f 00	??	00h							
ш	"										
П				********	*******	***					
П			*	FUNCTION		*					
П		undefined * stdcall Yaz0 FirstDMA(void)									
П	undefined * v0 lo:4 <return></return>										
П		undefined4	_	c]:4 local c	XF	XREF[2]:					
П	maria and and and and and and and and and an										
П		undefined4	Stack[-0x	Stack[-0x14]:4 local_14		XREF[2]:					
П											
ш			Yaz0_FirstDl		XREF[1]:	Yaz0_I					
ш		80001b30 3c 02 80		v0,0x8001							
ш		80001b34 8c 42 44		v0,offset sYaz0CurDataEnd((√0)	= 1					
ш		80001b38 3c 07 80		a3,0x8001							
		80001b3c 3c 01 80	01 lui	at,0x8001							
	<										
	n Call Trees: DmaMgr_SendRequest1 - (OotEuropeMQDbg)										
n C	all Trees:	DmaMgr SendRequest1 - (0	OotEuropeMODbg)		♠ %	I - 5					

75% chance of detecting a file boundary automatically

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Ш		80001b0c 0c 00 0c a0	jal	osRecvMesg		uno											
Ш		80001b10 24 06 00 01	_li	size,0xl													
Ш		80001b14 00 00 10 25	or	v0, zero, zero													
Ш		80001b18 8f bf 00 24	lw	ra, 0x24(sp)													
Ш																	
Þ		LJ	AB_80001b1c		XREF[1]:	80001k											
П		80001blc 27 bd 00 70	addiu	sp, sp, 0x70													
П		80001b20 03 e0 00 08	jr	ra													
П		80001b24 00 00 00 00	_nop														
П		80001b28 00	??	00h													
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П		80001b2a 00	??	00h													
ш		80001b2b 00	??	00h													
П		80001b2c 00	22	00h													
П		80001b2d 00	??	00h													
ш		80001b2e 00	2?	00h													
П		80001b2f 00	??	00h													
П				********													
П		*		FUNCTION	******	***											
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П	undefined *stdcall Yaz0_FirstDMA(void)																
П	undefined * v0_lo:4 <return></return>																
П		undefined4]:4 local_c	XF	EF[2]:												
П																	
П		undefined4	Stack[-0x1	4]:4 local_14	XF	EF[2]:											
П	Yaz0_FirstDMA			4	XREF[1]:	Yaz0 I											
ш		80001b30 3c 02 80 01	lui	v0,0x8001		_											
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	<																
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The rest can be guessed based on context

Split the assembly file into one file per function

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- Add a C file that includes all the assembly

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- Add a C file that includes all the assembly
- Progressively turn every function from asm to C

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#pragma GLOBAL_ASM("my_function.s")

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#pragma GLOBAL_ASM("my_function.s")



```
void my_function(void) {
   *(volatile int*)0 = 0; // sw zero,0(zero)
   *(volatile int*)0 = 0; // sw zero,0(zero)
   *(volatile int*)0 = 0; // sw zero,0(zero)
   ...
}
```

mips_to_c

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- Specific to MIPS
- Recognizes IDO specific patterns
- Great for matching

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- Interactive
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- Not ideal for matching



Original

```
u32 StackCheck_CheckAll(void) {
    u32 ret = 0;
    StackEntry* iter = sStackInfoListStart;

while (iter) {
        u32 state = StackCheck_GetState(iter);
        if (state != STACK_STATUS_OK) {
            ret = 1;
        }
        iter = iter->next;
    }

return ret;
}
```

Original

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u32 StackCheck_CheckAll(void) {
    u32 ret = 0;
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while (iter) {
    u32 state = StackCheck_GetState(iter);
    if (state != STACK_STATUS_OK) {
        ret = 1;
    }
    iter = iter->next;
}

return ret;
}
```

```
int StackCheck_CheckAll(void)
{
   int state;
   StackEntry *iter;
   int ret;

   ret = 0;
   iter = sStackInfoListStart;
   if (sStackInfoListStart != (StackEntry *)0x0) {
        do {
            state = StackCheck_GetState((int)iter);
            if (state == 0) {
                iter = iter->next;
            }
        else {
                ret = 1;
                iter = iter->next;
            }
        while (iter != (StackEntry *)0x0);
    }
    return ret;
}
```

Original

```
u32 StackCheck_CheckAll(void) {
    u32 ret = 0;
    StackEntry* iter = sStackInfoListStart;

while (iter) {
    u32 state = StackCheck_GetState(iter);
    if (state != STACK_STATUS_OK) {
        ret = 1;
    }
    iter = iter->next;
}

return ret;
}
```

Ghidra

```
int StackCheck_CheckAll(void)
{
   int state;
   StackEntry *iter;
   int ret;

   ret = 0;
   iter = sStackInfoListStart;
   if (sStackInfoListStart != (StackEntry *)0x0) {
        do {
            state = StackCheck_GetState((int)iter);
            if (state == 0) {
                iter = iter->next;
            }
        else {
                ret = 1;
                iter = iter->next;
            }
        while (iter != (StackEntry *)0x0);
    }
    return ret;
}
```

mips2c

```
u32 StackCheck_CheckAll(void) {
    StackEntry *temp_s0;
    StackEntry *temp_s0_2;
    StackEntry *phi_s0;
    u32 phi_s1;
    u32 phi_s1_2;
    temp_s0 = sStackInfoListStart;
    phi_s0 = temp_s0;
    phi_s1 = 0U;
    phi_s1_2 = 0U;
    if (temp_s0 != 0) {
            if (StackCheck_GetState(phi_s0) != 0) {
                phi_s1_2 = 1U;
            temp_s0_2 = phi_s0->next;
            phi_s0 = temp_s0_2;
            phi_s1 = phi_s1_2;
        } while (temp_s0_2 != 0);
    return phi_s1;
```



Checking for differences

Checking for differences

```
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/oot$ make
python3 tools/asm processor/build.py tools/ido recomp/linux/7.1/cc -- mips-linux
-qnu-as -march=vr4300 -32 -Iinclude -- -c -G 0 -non shared -Xfullwarn -Xcpluscom
m -Iinclude -Isrc -Iassets -Ibuild -I. -Wab,-r4300 mul -woff 649,838,712 -mips2
-02 -o build/src/boot/yaz0.o src/boot/yaz0.c
qcc -fno-builtin -fsyntax-only -fsigned-char -std=gnu90 -D LANGUAGE C -D NON MA
TCHING -Iinclude -Isrc -Iassets -Ibuild -I. -include stdarg.h -Wall -Wextra -Wno
-format-security -Wno-unknown-pragmas -Wno-unused-parameter -Wno-unused-variable
-Wno-missing-braces -Wno-int-conversion -m32 src/boot/yaz0.c
mips-linux-gnu-ld -T build/undefined syms.txt -T build/ldscript.txt --no-check-s
ections --accept-unknown-input-arch --emit-relocs -Map build/z64.map -o zelda oc
arina mq dbg.elf
tools/elf2rom -cic 6105 zelda_ocarina_mq_dbg.elf zelda_ocarina_mq_dbg.z64
f0b7f35375f9cc8ca1b2d59d78e35405 zelda ocarina mg dbg.z64
zelda ocarina mg dbg.z64: OK
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/oot$
```

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f0b7f35375f9cc8ca1b2d59d78e35405 zelda ocarina mg dbg.z64
zelda ocarina mg dbg.z64: OK
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```
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tools/elf2rom -cic 6105 zelda ocarina mg dbg.elf zelda ocarina mg dbg.z64
20aea272a0eaee7acf2946c3e8d34d24 zelda ocarina mg dbg.z64
zelda ocarina mg dbg.z64: FAILED
md5sum: WARNING: 1 computed checksum did NOT match
make: *** [Makefile:167: all] Error 1
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/oot$
```



asm-differ

asm-differ

\$./diff.py -mwo StackCheck_CheckAll

asm-differ

\$./diff.py -mwo StackCheck_CheckAll

```
u32 StackCheck CheckAll(void) {
           u32 ret = 0;
          StackEntry* iter = sStackInfoListStart;
          while (iter) {
               u32 state = StackCheck GetState(iter);
               if (state != STACK STATUS OK) {
                   ret = 1;
121
           return ret;
                                     TERMINAL
TARGET
                                                           CURRENT (600)
2fc:
        addiu
                                                       112 2fc:
                sp,sp,-0x20
                                                                   addiu
                                                                           sp,sp,-0x20
                s0,0x14(sp)
                                                       112 300:
300:
        SW
                                                                   SW
                                                                           s0,0x14(sp)
304:
        lui
                s0,%hi(sStackInfoListStart)
                                                       114 304:
                                                                   lui
                                                                           s0,%hi(sStackInfoListStart)
308:
        lw
                s0,%lo(sStackInfoListStart)(s0)
                                                       114 308:
                                                                   lw
                                                                           s0,%lo(sStackInfoListStart)(s0)
30c:
        SW
                s1,0x18(sp)
                                                       112 30c:
                                                                   SW
                                                                           s1,0x18(sp)
310:
        SW
                ra,0x1c(sp)
                                                       112 310:
                                                                   SW
                                                                           ra,0x1c(sp)
314:
        beqz
                s0,33c ~>
                                                       116 314:
                                                                   beqz
                                                                           s0,338 ~>
318:
                                                       113 318:
        move
                s1,zero
                                                                   move
                                                                           s1,zero
31c: ~>
        ial
                StackCheck GetState
                                                       117 31c:
                                                                   ial
                                                                           StackCheck GetState
320:
                                                       117 320:
                                                                           a0,s0
        move
                a0,s0
                                                                   move
                                                      118 324:
                s0.0(s0)
                                                      118 328:
                                                       119 32c:
                                                                           s1,1
                s1,1
334:
        bnez
                s0.31c ->
                                                       116 330: -> bnez
                                                                           s0.31c ->
338:
                                                       116 334:
                                                                   nop
        nop
33c: ~>
        lw
                ra,0x1c(sp)
                                                       124 338: ~> lw
                                                                           ra,0x1c(sp)
                                                       124 33c:
340:
        move
                v0,s1
                                                                   move
                                                                           v0,s1
                                                       124 340:
344:
        lw
                s1,0x18(sp)
                                                                   lw
                                                                           s1,0x18(sp)
348:
        lw
                                                       124 344:
                s0,0x14(sp)
                                                                   lw
                                                                           s0,0x14(sp)
                                                       124 348:
34c:
                ra
                                                                           ra
350:
        addiu
                                                       124 34c:
                                                                   addiu
                sp,sp,0x20
                                                                           sp,sp,0x20
```

large reordering

large reordering

/50:	D	/au ~>		/50:	D	/au ~>
754:	lbu	v0,0x35(s0)		754:	lbu	v0,0x35(s0)
						7e0 ~>
758: ~>		t1,0x35(s0)		770: ~>		t3,0x35(s0)
75c:	beqzl	t1,770 ->		774:	beqzl	t3,788 ~>
760:				778:		
764:	jal	osSyncPrintf		77c:	jal	osSyncPrintf
768:	move	a0,s7		780:	move	a0,s7
76c: ->	lhu	t2,4(s0)		784:		t4,4(s0)
770:	lhu	t3,0xe(s0)	233	788:	lhu	t5,0xe(s0)
774:	lbu	t4,0x1c(s0)	233	78c:	lbu	t6,0x1c(s0)
778:	sh	t2,0x14(s0)	231	790:	sh	t4,0x14(s0)
77c:	andi	v1,t2,0xffff	232	794:	andi	v1,t4,0xffff
798:		7e0 ~>		798:		7e0 ~>
79c:	subu	a0,t5,t6		79c:	subu	a0,t5,t6

stack placement

66c:	1	+6 0::70/==)	257	66c:	lw'	+6 0:200(==)
	lw	t6,0x70(sp)				t6,0x200(sp)
670:	lw	t7,0x74(sp)	257	670:	lw	t7,0x204(sp)
674:	SW	v1,0x74(sp)	258	674:	SW	v1,0x204(sp)
678:	subu	t8,v0,t6		678:	subu	t8,v0,t6
67c:	sltu	at,v1,t7		67c:	sltu	at,v1,t7
680:	subu	a0,t8,at		680:	subu	a0,t8,at
684:	subu	a1,v1,t7		684:	subu	a1,v1,t7
688:	SW	a1,0x7c(sp)	257	688:	SW	a1,0x74(sp)
68c:	SW	a0,0x78(sp)	257	68c:	SW	a0,0x70(sp)
690:	SW	v0,0x70(sp)	258	690:	SW	v0,0x200(sp)

large reordering

/50:	D	/au ~>	220		D	/au ~>
754:	lbu	v0,0x35(s0)		754:	lbu	v0,0x35(s0)
758: ~>	lbu	t1,0x35(s0)		770: ~>	lbu	t3,0x35(s0)
75c:	beqzl	t1,770 ~>	227	774:	beqzl	t3,788 ~>
760:				778:		
764:	jal	osSyncPrintf		77c:	jal	osSyncPrintf
768:	move	a0,s7		780:	move	a0,s7
76c: ->	lhu	t2,4(s0)	231	784:	lhu	t4,4(s0)
770:	lhu	t3,0xe(s0)	233	788:	lhu	t5,0xe(s0)
774:	lbu	t4,0x1c(s0)	233	78c:	lbu	t6,0x1c(s0)
778:		t2,0x14(s0)	231	790:		t4,0x14(s0)
77c:	andi	v1,t2,0xffff	232	794:	andi	v1,t4,0xffff
798:		7e0 ~>		798:		7e0 ~>
79c:	subu	a0,t5,t6		79c:	subu	a0,t5,t6

stack placement

66c:	lw	t6,0x70(sp)	S	257	66c:	lw	t6,0x200(sp)
670:	lw	t7,0x74(sp)		257	670:	lw	t7,0x204(sp)
674:	SW	v1,0x74(sp)		258	674:	SW	v1,0x204(sp)
678:	subu	t8,v0,t6			678:	subu	t8,v0,t6
67c:	sltu	at,v1,t7			67c:	sltu	at,v1,t7
680:	subu	a0,t8,at			680:	subu	a0,t8,at
684:	subu	a1,v1,t7			684:	subu	a1,v1,t7
688:	SW	al,0x7c(sp)		257	688:	SW	a1,0x74(sp)
68c:	SW	a0,0x78(sp)		257	68c:	SW	a0,0x70(sp)
690:	SW	v0,0x70(sp)	S	258	690:	SW	v0,0x200(sp)

instruction reordering

144:	lui	at,0x3f80	66	144:	lui	at,0x3f80
148:		t7,t6,at	65	148:		v0,0(a0)
14c:		v0,0(a0)	j 66	14c:		t7,t6,at
150:	SW	t7,0(v1)		150:	SW	t7,0(v1)

large reordering

/50:	D	/au ~>	220		D	/au ~>
754:	lbu	v0,0x35(s0)		754:	lbu	v0,0x35(s0)
758: ~>	lbu	t1,0x35(s0)		770: ~>	lbu	t3,0x35(s0)
75c:	beqzl	t1,770 ~>	227	774:	beqzl	t3,788 ~>
760:				778:		
764:	jal	osSyncPrintf		77c:	jal	osSyncPrintf
768:	move	a0,s7		780:	move	a0,s7
76c: ->	lhu	t2,4(s0)	231	784:	lhu	t4,4(s0)
770:	lhu	t3,0xe(s0)	233	788:	lhu	t5,0xe(s0)
774:	lbu	t4,0x1c(s0)	233	78c:	lbu	t6,0x1c(s0)
778:		t2,0x14(s0)	231	790:		t4,0x14(s0)
77c:	andi	v1,t2,0xffff	232	794:	andi	v1,t4,0xffff
798:		7e0 ~>		798:		7e0 ~>
79c:	subu	a0,t5,t6		79c:	subu	a0,t5,t6

stack placement

$\begin{array}{cccccccccccccccccccccccccccccccccccc$	
674: sw v1,0x74(sp) s 258 674: sw v1,0x 678: subu t8,v0,t6 257 678: subu t8,v0	(200(sp)
678: subu t8,v0,t6 257 678: subu t8,v0	(204(sp)
	(204(sp)
	, t6
67c: sltu at,v1,t7	.,t7
680: subu a0,t8,at 257 680: subu a0,t8	,at
684: subu a1,v1,t7 257 684: subu a1,v1	,t7
688: sw al,0x7c(sp) s 257 688: sw al,0x	(74(sp)
68c: sw a0,0x78(sp) s 257 68c: sw a0,0x	(70(sp)
690: sw v0,0x70(sp) s 258 690: sw v0,0x	(200(sp)

regalloc

b0: ~> move b4: jal b8: move bc: move c0: jal c4: move	a0,s5 osInvalICache a1,s4 a0,s5 osInvalDCache a1,s4	r 1584 b0: -> 1584 b4: r 1584 b8: r 1585 bc: 1585 c0: r 1585 c4:	jal move move jal move	a0,s6 osInvalICache a1,s5 a0,s6 osInvalDCache a1,s5
c8: addiu	s6,sp,0x80	r 1585 c8:	addiu	s7,sp,0x80
cc: move	a0,s6	r 1586 cc:	move	a0,s7

instruction reordering

144:	lui	at,0x3f80	66	144:	lui	at,0x3f80
148:		t7,t6,at	65	148:		v0,0(a0)
14c:		v0,0(a0)	j 66	14c:		t7,t6,at
150:	SW	t7,0(v1)		150:	SW	t7,0(v1)

Compiler patterns

• !(a ^ b) ⇔ a == b

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- $(x << 24) >> 24 \Leftrightarrow (s8)x$

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- struct copy

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- $(x << 24) >> 24 \Leftrightarrow (s8)x$
- $x * 7 \Leftrightarrow (x << 2) x$
- loop unrolling
- struct copy
- deduplicating sub-expressions

What can affect codegen? Stupid things

Stupid things

• if (1) { ... }

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- using temps

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\$./permuter.py nonmatchings/DmaMgr_DMARomToRam/

\$./permuter.py nonmatchings/DmaMgr_DMARomToRam/

```
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/decomp-permuter$ ./permuter.py
nonmatchings/DmaMgr DMARomToRam/
Loading...
nonmatchings/DmaMgr DMARomToRam/base.c (DmaMgr DMARomToRam)
No perm macros found. Defaulting to randomization.
Will try 1 different base sources.
[DmaMgr_DMARomToRam] base score = 415
[DmaMgr DMARomToRam] tied best score! (415 vs 415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-415-9
[DmaMgr DMARomToRam] tied best score! (415 vs 415)
wrote to nonmatchings/DmaMgr_DMARomToRam/output-415-10 [DmaMgr_DMARomToRam] found new best score! (410 vs 415)
wrote to nonmatchings/DmaMgr_DMARomToRam/output-410-1
[DmaMgr DMARomToRam] found new best score! (355 vs 415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-355-2
[DmaMgr DMARomToRam] found different asm with same score (415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-415-11
[DmaMgr DMARomToRam] found new best score! (10 vs 415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-10-6
iteration 625, 19 errors, score = 13010^C
Exiting.
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/decomp-permuter$
```

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wrote to nonmatchings/DmaMgr DMARomToRam/output-10-6
iteration 625, 19 errors, score = 13010^C
Exiting.
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/decomp-permuter$
```

\$ cat nonmatchings/DmaMgr_DMARomToRam/output-10-1/diff.py

\$./permuter.py nonmatchings/DmaMgr_DMARomToRam/

```
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/decomp-permuter$ ./permuter.py
nonmatchings/DmaMgr DMARomToRam/
Loading...
nonmatchings/DmaMgr DMARomToRam/base.c (DmaMgr DMARomToRam)
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Will try 1 different base sources.
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[DmaMgr_DMARomToRam] found new best score! (355 vs 415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-355-2
[DmaMgr DMARomToRam] found different asm with same score (415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-415-11
[DmaMgr DMARomToRam] found new best score! (10 vs 415)
wrote to nonmatchings/DmaMgr DMARomToRam/output-10-6
iteration 625, 19 errors, score = 13010^C
Exiting.
darius@darius-ZenBook-UX425EA-UX425EA:~/Documents/dev/n64/decomp-permuter$
```

\$ cat nonmatchings/DmaMgr_DMARomToRam/output-10-1/diff.py

Honorable mentions

Honorable mentions

decomp.me

Honorable mentions

decomp.me

github.com/n64decomp/ido

mostly the same

- mostly the same
- less sensitive to small differences

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- matching data sections might be harder

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- matching data sections might be harder
- better inlining
- LTO (Link Time Optimizations)

Conclusion

Links

zelda64.dev github.com/zeldaret/oot

Questions?