

Memory protection on AVR32

Pierre Surply

Memory

External B

Interface

MPU

Conclusion

Memory protection on AVR32 LSE Summer Week 2014

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EPITA 2016

Jul 19, 2014



AVR32 Architecture

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Introduction Memory

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- 32-bit RISC microprocessor
- Modified Harvard
- Up to 15 general-purpose 32-bit registers
- Instruction length: 16 bits
- Big-endian
- Fast interrupts and multiple interrupt priority levels
- Privileged and unprivileged modes



AVR32 AP7

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Memory Layout

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Interrace

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- Application Processors
- 221 DMIPS @ 150 MHz
- SIMD/DSP Instructions
- Instruction and Data caches
- Memory Management Unit
- Java hardware acceleration



NGW100 Development Board

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Figure: NGW100



AVR32 UC3

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- Flash Microcontrollers
- 91 DMIPS @ 66 MHz
- DSP Instructions
- Instruction and Data prefetch
- Memory Protection Unit
- Embedded Flash/RAM



UC3 Development Board

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Figure: EVK1100



Memory Layout

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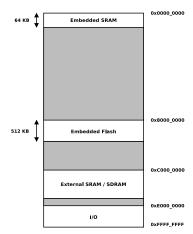


Figure: Memory Map (0x0000000 - 0xFFFFFFF)



Memory Layout

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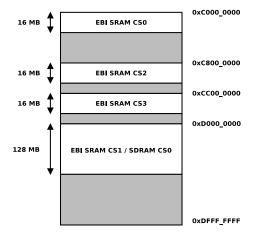


Figure: Memory Map (0xC0000000 - 0xDFFFFFFF)



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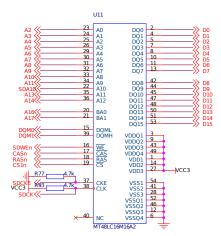


Figure: Synchronous DRAM 32MB - 4M x 16 x 4 banks



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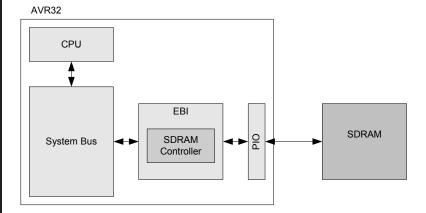


Figure: EBI Conceptual schematics



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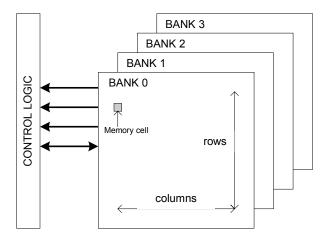


Figure: Generic SDRAM device



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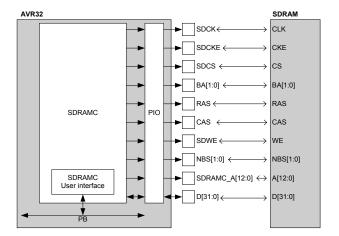


Figure: SDRAM Connection



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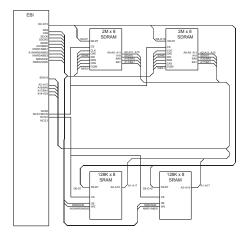


Figure: EBI Connections to Memory Devices



Memory Protection Unit

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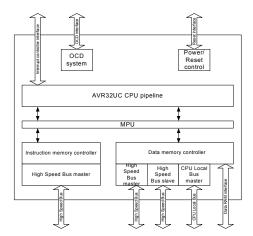


Figure: Overview of the AVR32UC CPU



Memory Protection Unit

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- Allows the user to divide the memory space into different protection regions.
- Each region is divided into 16 subregions, each of these subregions can have one of two possible sets of access permissions.

AVR32 Architecture Document

This is a simpler alternative to a full MMU, while at the same time allowing memory protection.



MPU Exception Handling

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- ITLB Protection Violation
- DTI B Protection Violation
 - ITI B Miss Violation
- DTLB Miss Violation
- TLB Multiple Hit Violation



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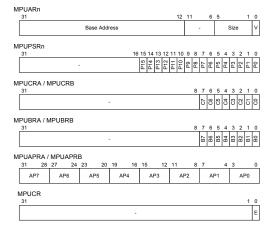


Figure: MPU Registers



System Registers

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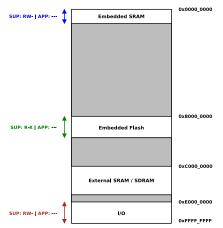


Figure: Basic MPU configuration



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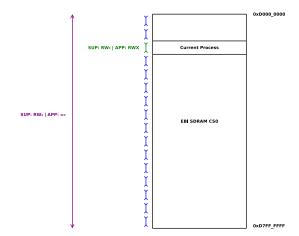


Figure: Application MPU configuration I



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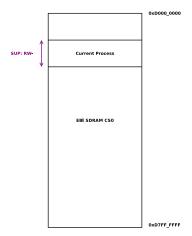


Figure: Application MPU configuration II



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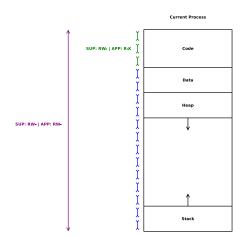


Figure: Application address space



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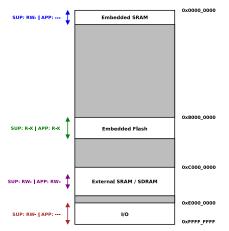


Figure: Builtin MPU Configuration



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- Not an alternative to a full MMU
 - Limited number of regions
 - Fixed size regions
- FreeRTOS-MPU
 - vTaskAllocateMPURegions()
 - portSWITCH_TO_USER_MODE()
 - xTaskCreate() -> xTaskCreateRestricted()



Contact

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