Delay-locked loop

Luis Guillermo Macias Rojas

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1. Background
2. Analysis
   - Basic concepts
3. Design

Where is it used?

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- The DLL is used in applications where the phase of the clock signal is critical, such as in high-speed communication systems.
- Where you need a PVT robust clock distribution.

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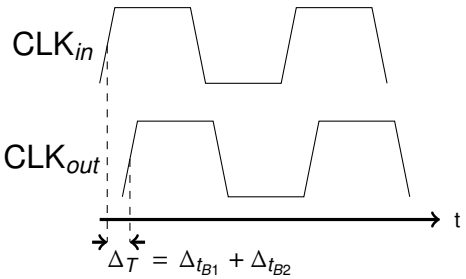

Skew in transmission lines

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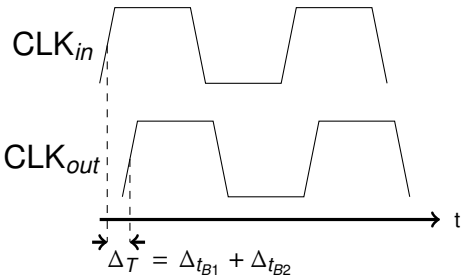
- If an interconnection's length is similar to that of the wave length (λ) of the signal, then a delay ($\Delta_{t_{TL}}$) will exist between A and B.

$$\lambda = \frac{\nu_p}{f}$$



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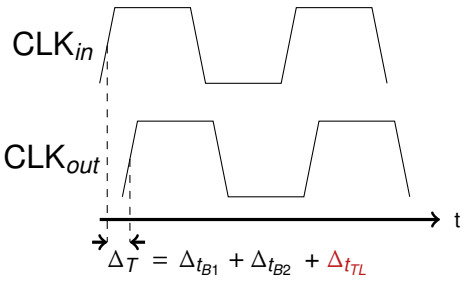

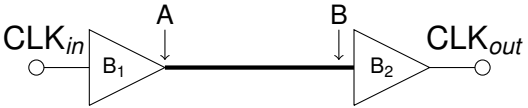

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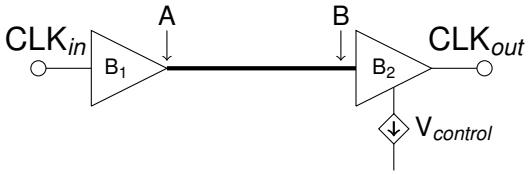

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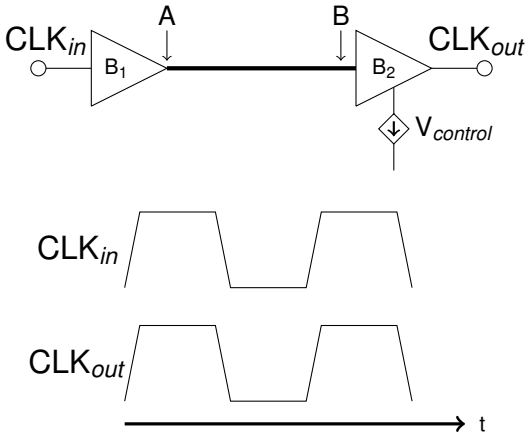

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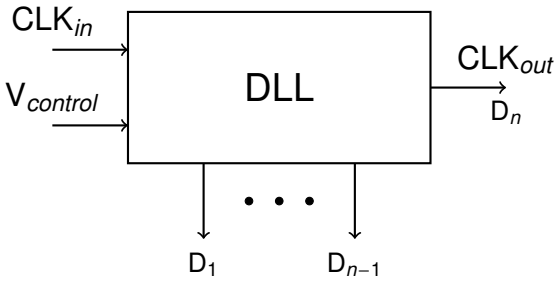

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Because of $\Delta_{t_{TL}}$ and the DLL's ability to generate multiple phases.

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- The charge pump convert of the voltage-controlled delay line.

Example

This is a cp deign example.

two column design

lkadjhv;kaj;vkja;vn;;;;ncolum1
column1
akj;akj;av;asadbadbaab

column2
a;fwkjap;hvah;v;ahav;av'a;jv;lajvlaj