

# Delay-locked loop

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## 1 Background

## 2 Analysis

- Basic concepts
- Blocks
- Schematics

## 3 Design

# Where is it used?

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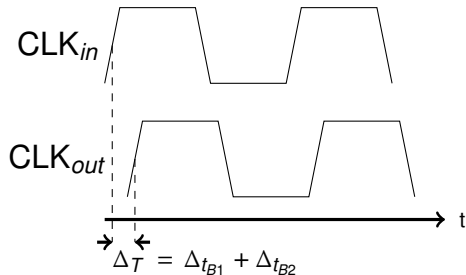
- The delay-locked loop (DLL) is a circuit that is used to align the phase of a clock signal with the phase of a reference signal.
- The DLL is used in applications where the phase of the clock signal is critical, such as in high-speed communication systems.
- Where you need a **PVT robust** clock distribution.

# Skew in transmission lines

- Skew ( $\Delta_T$ ) can be viewed as the difference in phase between two signals.

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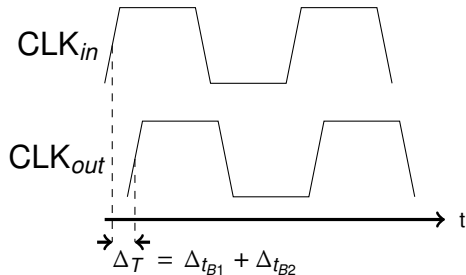
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- If an interconnection's length is similar to that of the wave length ( $\lambda$ ) of the signal, then a delay ( $\Delta_{t_{TL}}$ ) will exist between A and B.

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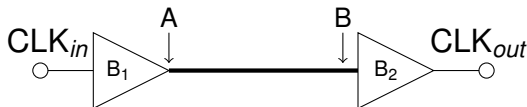
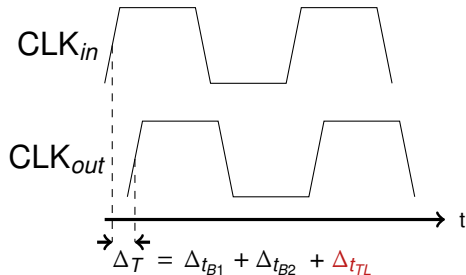




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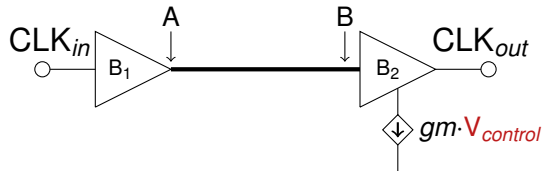


# Skew correction

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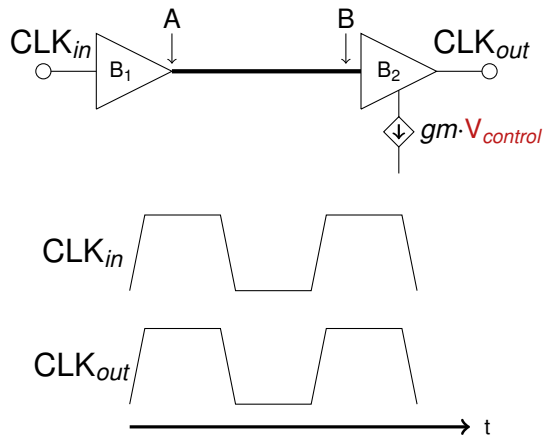
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- The DLL can be modeled as a box that takes in a control voltage and  $\text{CLK}_{in}$ , and outputs  $\text{CLK}_{out}$  in phase with the reference.

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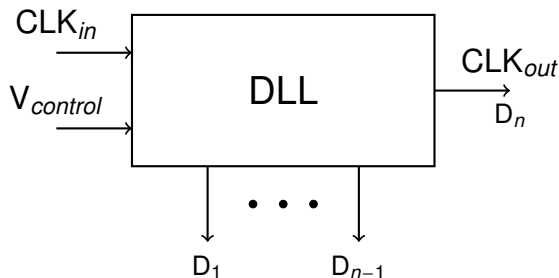
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Why use a DLL at all?

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## Why use a DLL at all?

Because of  $\Delta t_{TL}$  and the DLL's ability to generate multiple phases.



# DLL block diagram

DLL block diagram

PFD schematic

# Design of the DLL

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- The phase detector compares the phase of the reference signal with the phase of the feedback signal and generates an error signal.
- The charge pump convert of the voltage-controlled delay line.

## Example

This is a cp deign example.

# two column design

lkadjhv;kaj;vkja;vn;;;ncolum1  
column1  
akj;akj;av;asadbadaab

column2  
a;fwkjap;hvah;v;ahav;av'a;jv;lajvla