

A Register Controlled Delay Locked Loop using a TDC and a new Fine Delay Line scheme

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Abstract—This paper presents a Register Controlled Delay Lock Loop (RCDLL) with a Time-to-Digital Converter (TDC) and a new Fine Delay Line (FDL) scheme. The architecture of the proposed DLL uses a Time-to-Digital Converter (TDC), a Digital-to-Time Converter (DTC) scheme for short length of Coarse Delay Line (CDL), and a Open Loop Duty Cycle Corrector (DCC). While the conventional DLL has two feedback loops, the DLL with an open loop DCC has only one loop. So, it occupies a small area compared to the conventional one. Moreover, new FDL scheme is proposed which is capable of seamless boundary switching with a fixed delay step. HSPICE simulation results are based with ANAM 0.18um 1P6M CMOS process with 1.5V power supply voltage. Upon the simulation results, the proposed DLL operates correctly from 200MHz to 800MHz. The power consumption is less than 24mW at 800MHz. The active area of the design is 0.178mm²

I. INTRODUCTION

As the demand for high performance memory system grows, it becomes more important to develop a Delay Locked Loop (DLL) with high speed, less area, power and low jitter. A DLL can be classified into three categories: analog DLLs, digital DLLs and mixed-mode DLLs. Among them, digital DLLs provide fast locking and robust operation over all process variations. So, currently much effort are made to carry out the digital DLL. A research on Digital Register Controlled DLL (Digital RCDLL), which is focal point of this paper, has been done by [1] – [2]. In this paper, we improved the performance for the conventional digital RCDLLs in two ways: one is for less area and less power consumption. In the case of the digital RCDLL proposed in [1], it has a disadvantage with large area and high power consumption because it has a dual-loop structure for inherent duty cycle correction. Moreover, the continuing scaling down of CMOS technologies had leads to shorter length of unit coarse delay. As a result, the number of Coarse Delay Unit (CDU) in a DLL has been increased. The other is improvement of the conventional Fine Delay Line (FDL) structure. A FDL scheme in conventional DLLs uses a inverter chain with capacitive load or vernier delay line. But a recent phase mixing method through the weighted inverter is widely used to solve a boundary switching problem [1], [3]. The phase mixing method has two advantages: one is

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that the way to increase phase resolution is simple, and the other is that the seamless boundary switching scheme can be implemented easily. However, phase mixing method has a sensitivity problem to variations of process and temperature.

To meet all the aforementioned requirement and improve the performance of DLL further, (1) Uses TDC-DTC block for the delay compensation between the reference clock (ref_clk) and the feedback clock (fb_clk). And with the method the length of CDL can be greatly reduced. (2) A one loop structure through the open loop digital DCC with use of TDC is proposed. The properties (1) and (2) are proposed to solve the problems of area and power consumption in the conventional DLLs. (3) A new Fine Delay Line (FDL) scheme is proposed to improve sensitivity problem according to variations of process and temperature in a conventional phase mixing based FDL.

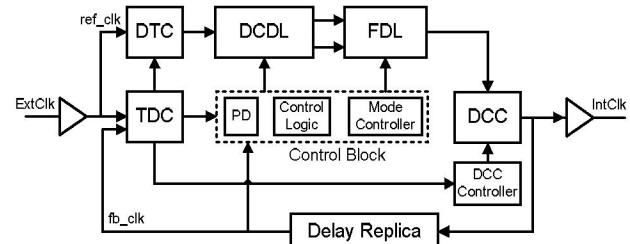


Figure 1. Top level architecture of the proposed Digital RCDLL

II. ARCHITECTURE

The top level architecture of the proposed digital RCDLL is shown in Fig. 1. This digital RCDLL has a similar architecture compared to that of the above-mentioned previous RCDLL with a dual loop structure [1]. However, the digital RCDLL of this work has only one loop structure with use of a open loop DCC. The proposed DLL illustrated in Fig. 1 comprises a Dual Coarse Delay Line (DCDL) for the seamless boundary switching [1], a FDL, a open loop DCC, a delay replica and a control block. In addition to these blocks, the proposed DLL has a TDC-DTC block to reduce a CDL length and improve the performance of the DLL.

The locking process of the conventional digital RCDLL is performed in two steps, which are coarse and fine locking. In this work, before the coarse locking a TDC based on ring oscillator converts time difference between *ref_clk* and *fb_clk* into digital code. After the digital code is decided, a Mode Controller selects the method of coarse locking based on this code. Upon the coarse locking being completed, the remaining delay error is eliminated by operations of fine delay line. During the fine locking time, the drift of operation conditions such as temperature and supply voltage may result in a situation that a FDL cannot provide the required variable delay [8]. In order to mitigate this problem, the method of the seamless boundary switching has been proposed in [1] and [8]. However, a FDL scheme using phase mixing in [1], has a sensitivity problem as mentioned before. In order to improve this problem, new FDL scheme with seamless boundary switching ability is proposed. After the completion of fine locking, the output of the FDL goes through the DCC block to duty cycle correction, and then becomes a input signal of the output buffer and delay replica.

III. CIRCUIT DESCRIPTION

A. TDC

A TDC converts a specific amount of time duration into digital code. In this work, a TDC based on Ring-OSC [5] is adopted. The TDC block in this paper performs two kinds of conversion at the beginning of the DLL operation. The first conversion is to convert phase difference between *ref_clk* and *fb_clk* into digital code as mentioned before. The result code of this conversion is used to select a coarse locking method. In order words, the digital code proportional to the amount of phase difference between *ref_clk* and *fb_clk* is compared to the specific digital code which represents a predetermined fixed delay amount. With a result of comparison, the Mode Controller selects a method of CDL locking. If the measured delay code is bigger than internal delay code, then this digital code will become an input of the DTC which has a similar structure with a TDC, to provide a compensation delay. In another case, a DLL operates as a conventional RCDLL. With use of TDC-DTC block, the length of CDL has greatly reduced. The second conversion is to convert one cycle clock period of *ref_clk* to digital code. These digital codes are used to decide a half cycle clock period code in the DCC block.

B. Open Loop DCC

The all-digital open loop DCC consists of two major blocks. A DCC core and a DCC control block, as shown in Fig. 2. The timing diagram of the DCC is also shown in Fig. 2. The operation principles of the proposed DCC are as follows. When the external clock which has a distorted duty cycle ratio passes through the DELAY LINE block, the rising edge of the delayed clock lags the rising edge of the input clock by half of the cycle time. The DELAY LINE block is used to get the half period delay as in [6] – [7], which give the fixed rising edge property. After the generation of the delayed clock, if the input clock and

delayed clock are used as the two inputs of the clock recovery circuit in DCC, then the output clock will have a 50% duty-cycle ratio. The fast duty cycle correction with less power consumption can be done in an open loop manner.

The method of the proposed open loop DCC which uses a half period delay line and the clock recovery circuit is already proposed in [6] – [7]. Most of the DCCs proposed in [6] – [7] has a wide correction range of input duty cycle, fast locking time and fixed rising edge property. The proposed DCC also has those characteristics mentioned above. However, the conventional DCCs have a complex control circuit to evaluate the half period delay of the input signal. On the other hand, the proposed DCC uses a digital code of one cycle clock period made by the TDC to make a half period delay code. So the DCC control block becomes just a simple decoder block. Because of this, the proposed DCC has a less area and less power consumption. Moreover, since the operation frequency of the proposed DCC has a close relation with operation frequency of the TDC, this proposed DCC has a larger operation frequency range. HSPICE simulation shows that the maximum operation frequency is up to 1GHz.

Among the building blocks of the proposed DCC, the architecture of the DELAY LINE and the Half Period Code Generator block is shown in Fig. 3. The conventional CDL scheme is used for the delay line for simplicity. Half Period Code Generator converts one cycle clock period code made by TDC, into half cycle clock period code. During this operation, just 1 bit signals from *en_part<0:5>*, *en_path<0:4>* are turn into low state, and then 1 bit output signal from NOR array is selected. The amount of delay provided by DELAY LINE is determined by this signal. For the clock recovery circuit, C2MOS inverter type clock generator [6] has been used.

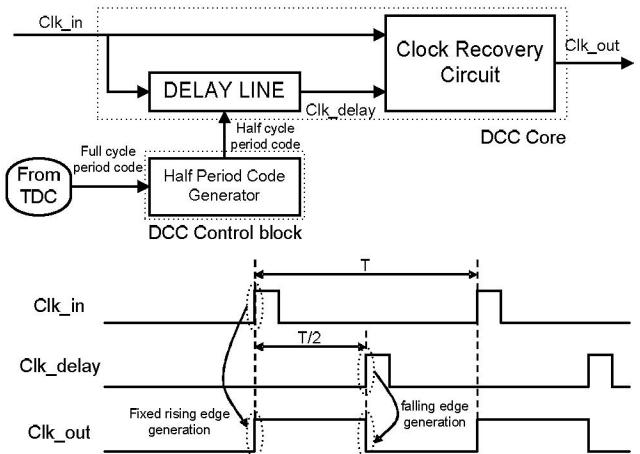


Figure 2. Block diagram and timing diagram of the proposed DCC

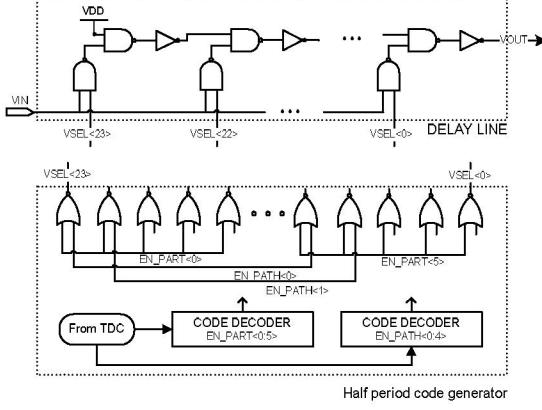


Figure 3. The architecture of the Delay Line and Half Period Code Generator for the proposed DCC

C. Fine Delay Line

The architecture of the FDL unit cell and FDL is shown in Fig. 4. As shown in Fig. 4, a fine delay unit inverter has the 2 transistors which are normally-on and 4 load transistors which can be controlled by switches. The amount of delay in FDU can be controlled by the switch conditions. The FDL consists of 5 stages FDU and 2 inverters with load transistors are placed in serial in FDU. The block diagram of the proposed Fine Delay Block (FDB) to achieve a seamless boundary switching is shown in Fig. 5. The structure of the proposed FDB has two FDLs to receive two DCDL output signals as each input signal of FDL. FDL CONTROLLER, code generator with control circuit, is placed inside FDB. The FDB have a output selector at the end of structure to select a one FDL signal as Clk_out among outputs of FDL1 or FDL2. Each of FDL1 and FDL2 can shift the input signal by 1 CDU delay and each of the FDL initially resets to have a normal delay. As a result the delay between FDL input and output signal can be vary by $\pm 1/2$ CDU delay. The FDL1 and FDL2 operate reciprocally each other through the code inversion block. In other words, if the delay provided by FDL1 increases, then the delay of FDL2 decreases.

The timing diagram to represent the operation of seamless boundary switching is shown in Fig. 6. Each block in Fig. 6 represents an amount of delay of the peripheral blocks in Fig. 5. A DCDL has two kinds of delay lines which are CDL1 and CDL2 as shown in Fig. 5. And a CDL1 delay and a CDL2 delay have a constant phase difference of 1 CDU's delay as shown in Fig. 6. The variable delays of FDL1 and FDL2 are represented by the dot line inside the FDL1 delay and FDL2 delay. Total variable delays of FDL1 and FDL2 are equal to 1 CDU delay as shown in Fig. 5. When the delay of the FDL1 becomes minimum and the delay should be decreased further, the delay of FDL2 is increased reciprocally – Fig. 6-(a) – and the output signals of FDL1 (VF_1) and FDL2 (VF_2) are almost aligned to each other. At this point, output selector switches to select a VF_2 signal as a output. Since VF_1 and VF_2 are the almost same delay during the switching as shown in Fig. 6-(b),

meaning that the delay switching is seamless. From this point, the delay of the FDL2 can be further decreased as desired. In this manner seamless boundary switching through the conventional inverter chain structure can be implemented.

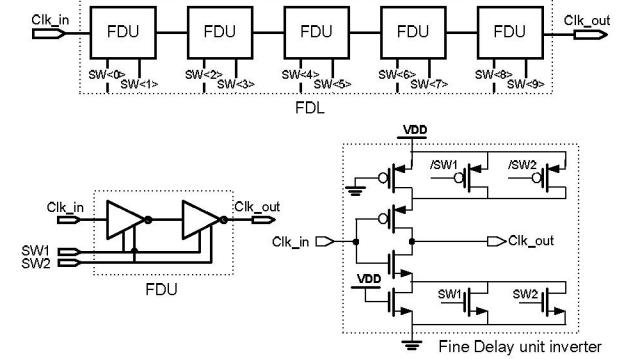


Figure 4. The schematics of FDL, FDU and Fine Delay unit inverter

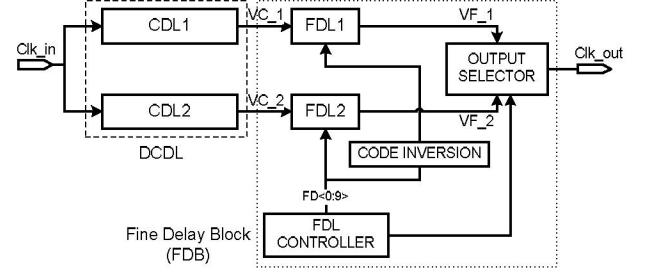


Figure 5. The block diagram of the proposed FDL for the seamless boundary switching

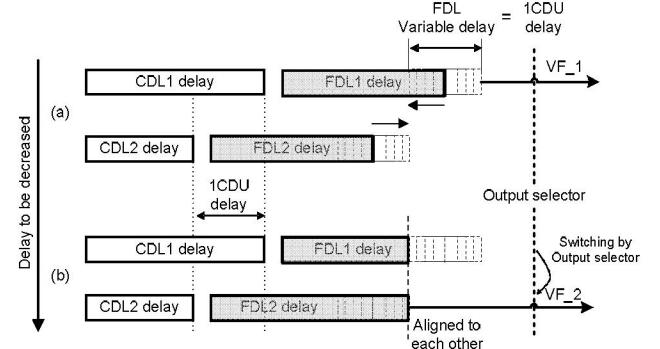


Figure 6. The seamless boundary switching method with proposed FDB.

IV. SIMULATION RESULTS

The proposed all-digital RCDLL circuit was designed using a 0.18um CMOS technology with supply voltage of 1.5V and the power consumption is 24mW at 800MHz. The active area is $0.85 \times 0.21\text{mm}^2$ including input and output digital buffers. From the simulation results, the proposed

DLL can operate correctly from 200MHz to 800MHz. By the operation of the proposed open-loop DCC circuit, the duty cycle is corrected to be $50\pm1\%$ duty error for the 400MHz input clock, and correctable duty cycle range is from 10% to 85% at 400MHz. In the case of 800MHz input clock, the duty cycle of the output signal is corrected to be $50\pm1\%$ duty error for the 20% to 75% duty cycle range of the input signal. The simulated values of the duty cycle ratio of the output clock for different input clocks with different duty cycles are shown in Fig. 7. The simulated output jitter characteristics of the proposed DLL are shown in Fig. 8. When the power supply noise is added in the supply voltage, we added the power supply noise which is the random Gaussian noise of $\text{rms}=10\text{mV}$ and the power supply fluctuation because of switching activities of the internal gates. In the Fig. 8, two kinds of results are represented. One is RMS jitter and the other is peak-to-peak (p-p) jitter. The simulation data are evaluated based on sampling data of the output signal. The sampling is carried out after the coarse and fine locking of the DLL, and 1000 samples are used for each result. Table I summarizes the simulated performance characteristics of the proposed RCDLL.

V. CONCLUSION

In this paper an all-digital Register Controlled DLL to achieve small area, less power consumption and improve the performance of the conventional RCDLL is presented. The novel features of the proposed DLL are as follows. First, with use of TDC-DTC block for the delay compensation, the length of CDL is greatly reduced. Second, the proposed DCC operates in open loop fashion in order to achieve small area and lower power consumption. Moreover, by using the TDC to the proposed DCC, the size and complexity of conventional DCC can be reduced. At last, a new FDL scheme with a seamless boundary switching ability was proposed.

The proposed DLL is implemented in 0.18um CMOS technology with a core area of 0.178mm^2 . The simulation result shows its operation frequency range to be from 200MHz to 800MHz. the power consumption is less than 24mW at its highest frequency (800MHz).

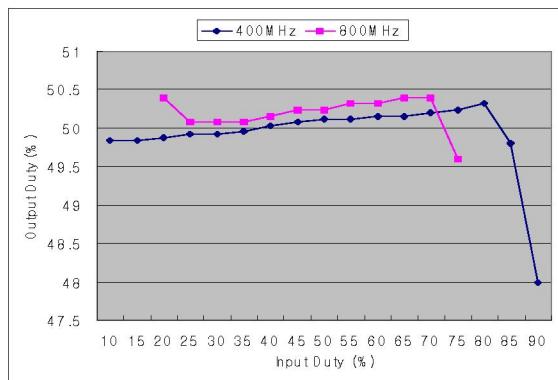


Figure 7. Output duty cycle against input duty cycle

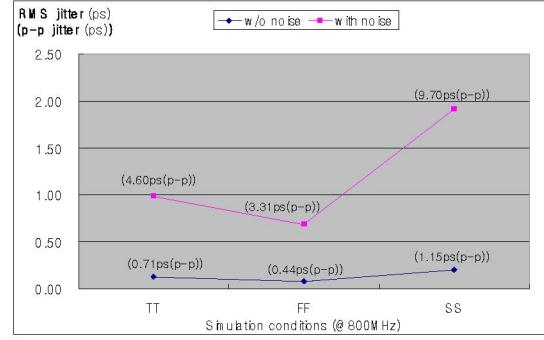


Figure 8. The jitter characteristics of the DLL output signal at 800MHz

TABLE I. PERFORMANCE SUMMARY

Performance summary	
Process	0.18 um 1P6M CMOS
Supply Voltage	1.5V
Operating Frequency Range	200MHz ~ 800MHz
Lock Time	< 150 cycles
Duty Cycle Correction	$\pm 1\%$ for external duty error of 10% ~ 85% @ 400MHz
Power Dissipation	24mW @ 800MHz
Active Area	$0.85 \times 0.21 \text{ mm}^2$

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