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DIALOG and SYNC: A VLSI Chip Set for Timing of the LHCb Muon Detector

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***Abstract*—The Muon detector of the Large Hadron Collider (LHCb) experiment at the Center for Nuclear Research plays a fundamental role in the first trigger level. It is mainly realized by means of a MWPC technology and consists of about 126,000 front-end channels. High efficiency is necessary both at detector and front-end level to satisfy the trigger requirement of five hits per five Muon stations with an overall efficiency of 95%. This corresponds to having a single front-end channel detection efficiency of 99% within a time window of 20 ns and also poses the problem of an accurate time alignment of the whole detector. The problem is addressed by designing two custom integrated circuits, named DIALOG and SYNC, realized in the IBM 0.25 μm technology.**

I. Introduction

THE LARGE Hadron Collider (LHCb) experiment [1] is one of the four experiments of the LHC machine—currently under construction at the European Center for Nuclear Research (CERN)—and it aims at the study of CP violation in the B meson sector. The LHCb muon detector is based on about 1,400 Multi-Wire Proportional Chambers (MWPC) distributed in five stations along the beam axis. It gives space-point information in binary form. In total the detector consists of 126 000 channels. The muon detector is especially important in the first LHCb trigger level (L0—level zero in the LHCb terminology). About 26 000 so-called logical channels are generated out of the 126 000 detector ("physical") channels as proper logical combinations of them and sent to the trigger. The L0 trigger gives a fast response (4 μs latency) on the transverse momentum of the detected muon track. A muon track is identified by five space points (hits), one per station, aligned and pointing to the interaction point. In order to have a satisfactory trigger performance, we require a detection efficiency of 95% in muon identification, which reflects to the requirement of a 99% detection efficiency per muon station.

The LHCb interactions have a bunched structure with a possible Bunch Crossing (BX) every 25 ns. The L0 muon trigger expects from the detector front-end electronics the complete binary map of the muon detector along with the associated BX identifier, which univocally defines the event time. This information must be supplied every 25 ns. Both the trigger and the read-out electronics operate synchronously according to a pipelined architecture. In order to assign the correct BX identifier, it is necessary to equalize all the different contributions to channel signal delays before sending the detector information to the trigger. The main contributions to channel delays are due to the time of flight of the particles (M1, the first muon station is about 7 m from the last one—M5) and the cable lengths (there are 10–15 m from the chambers and the place where the channel information is collected before being sent to the trigger). These contributions can give a relative delay among different channels of more than one BX and must be compensated.

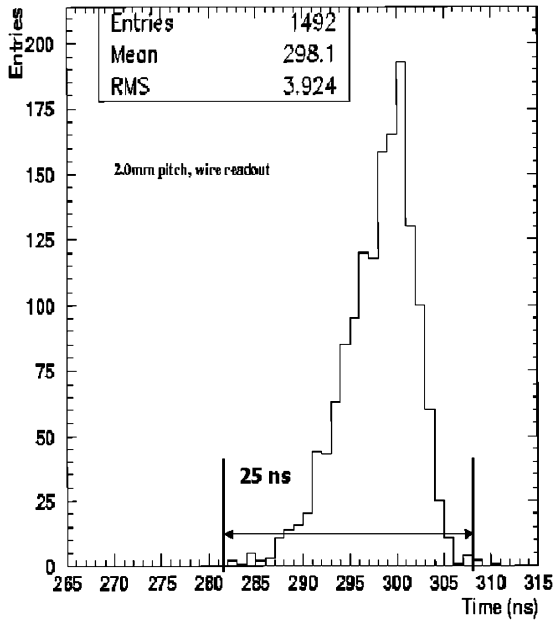

Fig. 1. Typical time distribution of LHCb MWPC signals.

Another important point to consider is the specific time resolution of detector and associated front-end electronics, which corresponds to a typical R.M.S. of 3–4 ns (Fig. 1). In order to avoid that the tails of the time distributions are assigned to a wrong BX, it is necessary to align them accurately inside the time window of 25 ns. This means that it is also necessary to measure the phase of the hits inside a BX period and reconstruct the time distribution of the hits for each channel. This information is not used by the muon trigger, but is important for proper time alignment of the whole detector channels and, in the end, to ensure the required trigger efficiency.

Once the time alignment is reached, it is still important to monitor possible variation of the time behavior, due to environmental conditions variations (e.g., atmospheric pressure, temperature) or possible changes in the rest of the system (e.g., supply voltage variations).

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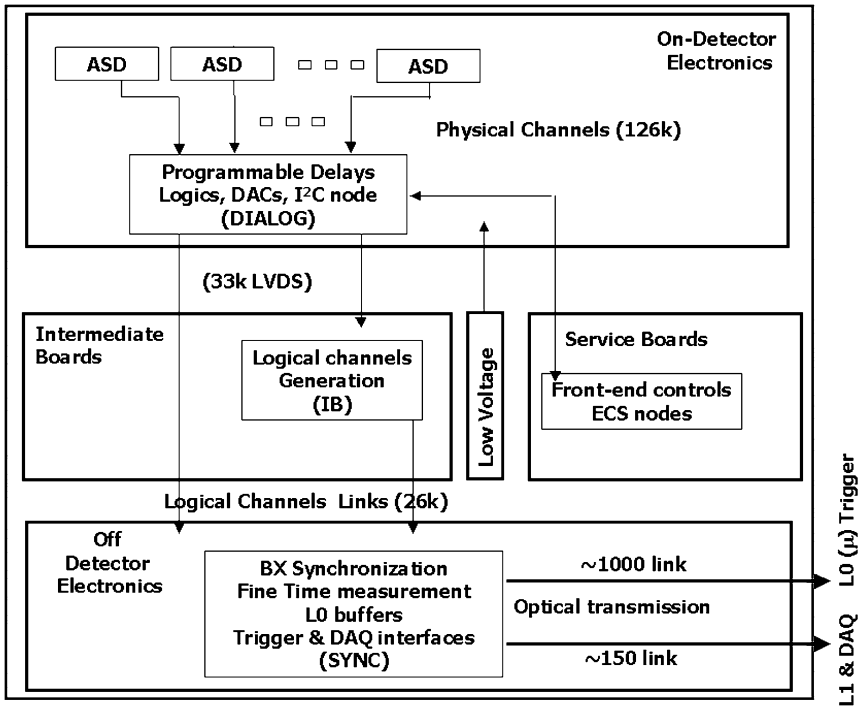

Fig. 2. Architecture of Muon system electronics.

All these reasons motivate the use of built-in dedicated circuitry in the muon front-end electronics in order to:

1) measure the arrival time of the detector signals with sufficient resolution;
2) build the signal time distributions;
3) compensate for the relative delay among the system channels;
4) monitor the proper time alignment while the whole system operates.

In the present paper, we will describe the above functionalities as implemented in two custom integrated circuits, named DIALOG and SYNC. DIALOG and SYNC are two basic building blocks in the muon electronics system and implement also other important functionalities. In this paper, however, we will only focus on structures dedicated to system timing.

II. Front-End Electronics

In order to define the field where we are playing, in the present Section we briefly describe the system architecture.

The muon front-end electronics architecture scheme is shown in Fig. 2. It can be subdivided into three parts. Proceeding from the chambers to the trigger and DAQ systems, we find the "on-detector" part, the "intermediate" part, and the "off-detector" part.

The on-detector part contains the Amplifier-Shaper-Discriminator (ASD) chip, named CARIOCA [2], and the DIALOG chip. Binary signals are output from the ASD. DIALOG processes them (see Section III) and performs a first logic reduction at the detector level.

The "intermediate" part consists of the so-called Intermediate Boards (IBs), that are placed at the two sides of the detector, at an average distance from the on-detector boards of about 10 m. They are necessary because the logical channels are generated from physical channels that not always belong to the same chamber, so the logical combination must be completed outside the detector. Service Boards, used to configure and monitor the front-end electronics parameters and low voltage supply system are also placed at the intermediate level, but do not influence the path of the signals.

The Off-Detector Electronics (ODE) is also placed at the two sides of the detector. Each 25 ns, the binary information generated on chambers is collected on the ODE boards, where it is endowed with its BX identifier and it is stored on a pipeline memory. There, it waits for the L0 trigger response in order to be passed to the next trigger level or to be discarded. While being written onto pipeline memories, data have to be tagged with their BX identifier and sent to the L0 trigger. At this point, all the signals have to be already aligned in time. The SYNC chip, placed inside the ODE boards, performs the operation of time alignment check and BX identifier tagging.

In order to realize a proper time alignment of the detector channels *at the beginning* of data taking and to monitor the system time alignment *during* data taking, dedicated electronic tools have been developed.

The idea is to measure the signals' occurrence time at the end of the chain, where all the delay contribution have already had their effect, just before sending the detector information to the L0 trigger. There the phase of the signal inside a BX period is measured and time distributions can be built. This operation is performed inside the SYNC chip, on the ODE boards. Once the amount of the delay to be compensated is determined, the due corrections have to be applied channel by channel at the beginning of the chain, before signals start to be combined the one with the others. The delay compensation is realized inside the DIALOG chip, placed on the chambers.

TABLE I
MAIN DAC CHARACTERISTICS

Architecture	R-2R
Resolution	8 bits
Area	146 x 153 μm^2
Supply voltage	2.5 V
DNL (peak to peak)	± 0.4 LSB
INL	± 0.4 LSB
Power consumption	500 μW (average)
Output resistance	~ 30 kW (code dependent)
Input resistance	8 kW
Settling time (@0pF load)	50 ns max
Settling time (@5pF load)	250 ns max

As the total delay can fairly exceed one single BX period, we divide the total delay compensation Δt in two parts

$$\Delta t = \Delta t_C + \Delta t_F \tag{1}$$

where Δt_C is called *Coarse delay* and Δt_F is called *Fine delay*. Δt_C is an integer number of BX periods, while Δt_F gives the fraction of BX period to be added for a fine alignment at the level of a few nanoseconds. For practical reasons, the Δt_C is compensated at the end of the chain (SYNC chip), when the BX identifier is assigned to data, while the Δt_F is compensated at the beginning of the chain (DIALOG chip) by means of programmable delays.

The circuits dedicated to delay measurement and compensation are the subjects of Sections III and IV.

III. TIMING STRUCTURES AND THE DIALOG CHIP

DIALOG is developed in IBM 0.25 μm technology. By using specific layout techniques [3], this technology provides good radiation resistance, able to sustain an accumulated dose of several Mrad. For the muon detector, the maximum accumulated dose during ten years of LHCb operation is estimated to be about 1 Mrad.

On the front-end boards, one DIALOG serves two ASD, for a total of 16 front-end channels. DIALOG contains the logics to reduce the physical channels into logical ones. The specific logic function has to be selected inside a number of configurations, because it varies according to the detector position. DIALOG provides 16 different thresholds to the ASD, using 16 custom integrated DACs [4]. The DAC characteristics are given in Table I. DIALOG also integrates many features used for system control and diagnostics. Internal functionalities can be set by writing internal registers via an I^2C interface [5]. In this paper, however, we want to concentrate our attention on the DIALOG facilities dedicated to the time alignment of the system. Further details on the DIALOG internal structure and functionalities can be found in [4].

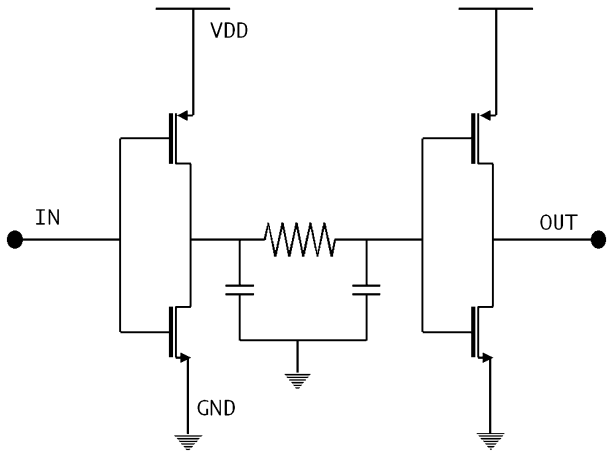

Fig. 3. RC delay unit.

Each single channel of the 16 DIALOG input channels can be delayed by a programmable number of steps, from 0 to 32. As the intrinsic time resolution of the detector and its associated ASD is around 4 ns R.M.S., a delay step of 1–2 ns is appropriate. Our initial choice was simply to set the delay step to around 1.5 ns, by using a cascade of RC delay units of the kind showed in Fig. 3.

This trivial solution, however, is extremely prone to technology process parameters variations, which affect the value of the resistance and capacitance of the delay step, in such a way that one single delay unit does not univocally correspond to a well-defined value. In order to get rid of process parameters variation, a calibration scheme has been conceived. The simple RC delay step has been changed into a Voltage Controlled Delay Unit, according to the scheme given in Fig. 4. Voltages $\mathbf{V_n}$ and $\mathbf{V_p}$ are generated from a control voltage (see below) and regulate the current flowing trough the cascaded inverters M1–M2 and M3–M4. This allow to change the rising time at the output of the first two inverters, thus changing the effective delay from input $\mathbf{I}$ to output $\mathbf{O}$.

The problem now is to find the appropriate control voltage corresponding to the wanted value of the delay step. For this purpose we use a Delay Locked Loop (DLL), as explained in Section III-A.

A. DLL and Delay Calibration

We designed a classic DLL scheme of the kind shown in Fig. 5, formed by a Phase Detector, a Charge Pump and a Voltage Controlled Delay Line (VCDL) [6], [7]. The VCDL is formed by a cascade of 16 Delay Units, perfectly matched to the Delay Units used on the Programmable Delay lines of the input channels. By using a Reference Clock of a given frequency, the value corresponding to a delay step is determined. As the DLL locks in an interval of frequencies, this gives an additional flexibility in setting the desired value for the delay step. The DLL characteristics and performance are listed in Table II.

After a calibration procedure, which typically lasts less than 500 ns (see Table II), the Voltage $V_{\rm ctrl}$ is used to drive all the Delay Lines of the single channels. The desired amount of delay is set by selecting the relevant output from the multiplexers (MUX) associated to the delay line of each channel.

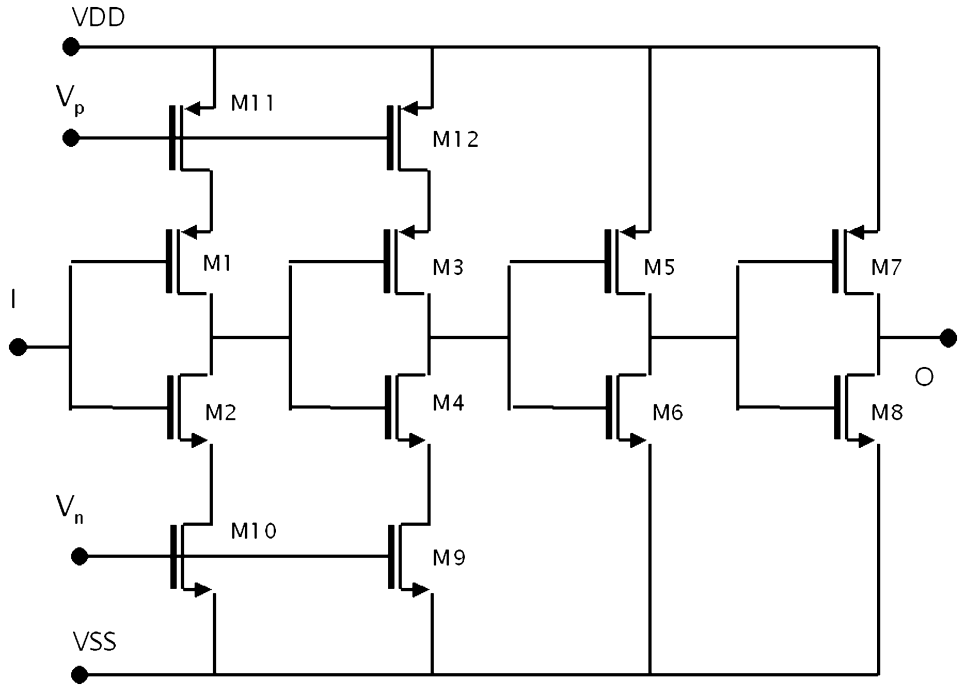

Fig. 4. Voltage controlled delay unit.

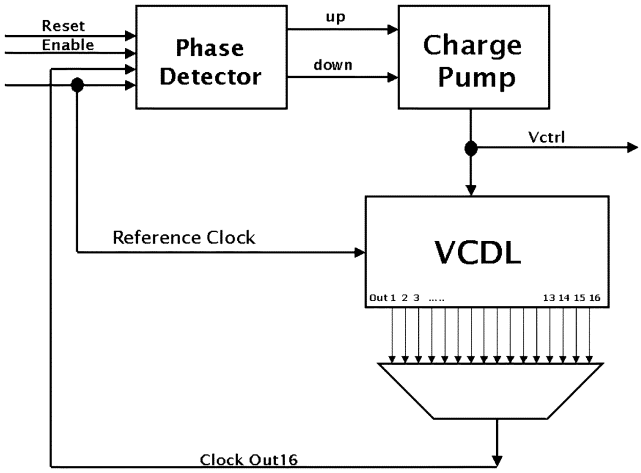

Fig. 5. DIALOG DLL scheme.

TABLE II
MAIN DLL CHARACTERISTICS

Locking Time	< 500 ns
Locking range	55MHz ÷ 25 MHz
Nominal frequency	40 MHz
DNL @ 40 MHz	± 0.3 LSB

Of course, in order to keep the calibration on the DLL, the Reference Clock should be kept running during normal system operation. This would imply to have a free running clock of around 40 MHz on all the front-end boards. We would prefer to avoid a high frequency clock on the analogue boards, as we consider this quite critical for system operation.

The solution to this problem would be to store the determined $V_{\rm ctrl}$ into an easily storable form after calibration. The Section III-B explains how this problem has been solved.

B. ADC-DLL

We use a dedicated ADC to convert the $V_{\rm ctrl}$ found from calibration. The scheme of the so-called ADC-DLL is shown in Fig. 6.

During the calibration phase, a Reference Clock is input to the ADC-DLL structure. The same clock is used to drive the ADC circuit—having an 8-bit resolution—which is based on a Successive Approximation Register (SAR) architecture. Once the calibration phase is concluded, the ADC conversion is started. Finally, the converted value of $V_{\rm ctrl}$ is written onto an 8-bit register, which is accessible for both writing and reading via the I^2C interface. After conversion, the clock can be switched off, as the rest of the DIALOG circuit works without the use of a master clock. The same 8-bit DAC of the SAR ADC is used to reconvert the stored $V_{\rm ctrl}$ bits into the voltage level needed to set the appropriate delay on all the VCDL associated to the 16 input channels. The 8-bit DAC used in the ADC structure is the same custom DAC used for threshold setting (Table I).

The calibration phase, comprising the conversion phase also, lasts about 3 μs. The value found for the $V_{\rm ctrl}$ can be uploaded from the storage registers and saved in a database. In such a way, it is not necessary to repeat the calibration procedure every time the system is switched on, but only write the appropriate value onto the registers via the I^2C interface.

Fig. 7 gives the unit delay values as a function of the ADC code measured for different DIALOG chips. The dispersion due to the process parameters variation is clearly visible. This demonstrates the need for a fine-tuning via the calibration procedure.

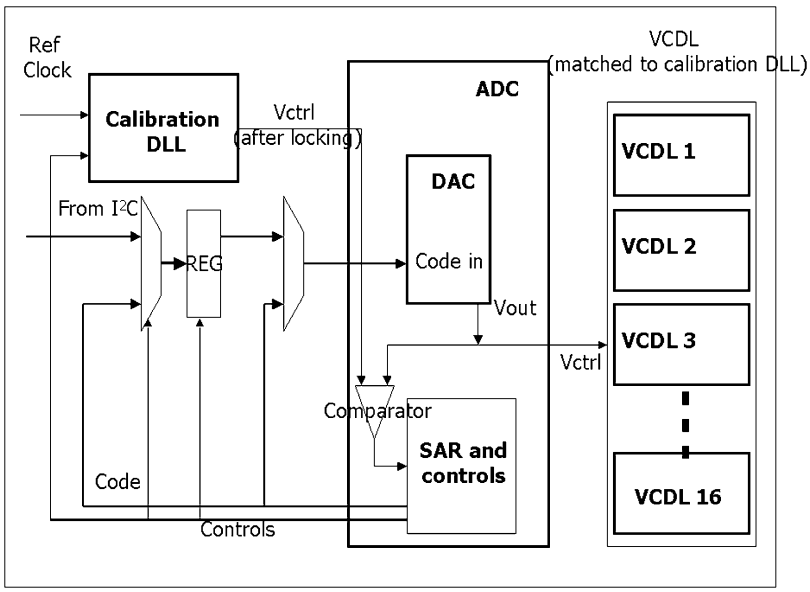

Fig. 6. ADC-DLL scheme.

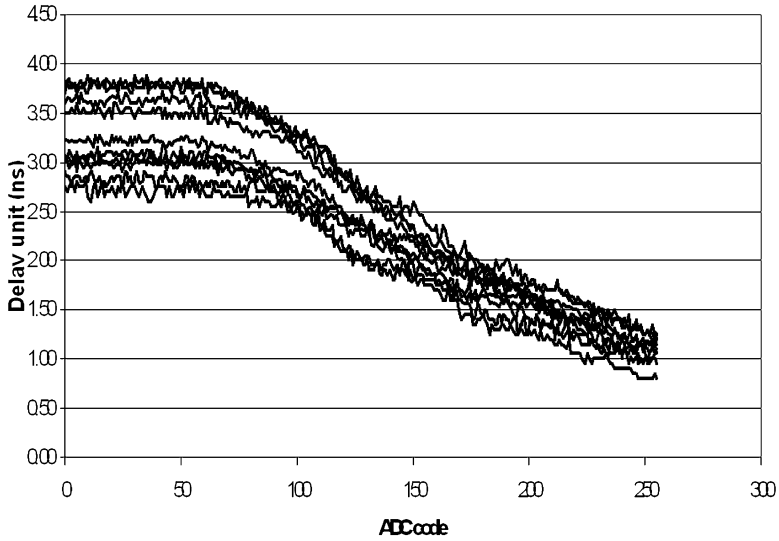

Fig. 7. Unit delay versus ADC code for different DIALOG chips.

IV. Timing Structures and the SYNC Chip

In order to use the right amount of delay compensation, it is necessary to measure the accumulated delay channel by channel. This task is performed inside the SYNC chip, placed in the ODE boards. Also the SYNC chip is realized in the IBM 0.25-μm technology.

Each SYNC chip houses eight channels. It contains the pipeline memories for the L0 trigger and the interfaces to both the L0 trigger and the subsequent trigger level (L1). Here, we again concentrate ourselves on its timing-dedicated facilities.

Differently from DIALOG, the SYNC is housed in a completely synchronous board, working under a master clock of 40.08 MHz (the same LHC clock regulating the BX structure). Each SYNC chip works synchronously at 40.08 MHz.

As already stated, we need to determine two values of the delay, Δt_C and Δt_F [see (1)]. Δt_C is determined by referring to the BX structure. The BX structure is a repetitive structure characterized by a regular sequence of BX periods with and without interactions (Fig. 8). This pattern can be used to determine the local position of the channels with respect to the absolute time corresponding to the experiment BX numbering. The BX structure is reconstructed inside the SYNC chip, by accumulating the received hits on dedicated counters. The start for the counters is given by an external reset, providing the reference of the BX sequence start.

The Δt_C can be compensated inside the SYNC chip, by adding an offset to the local BX counter inside the chip itself. This is done just before writing the incoming data onto the pipeline memories and sending them to the L0 trigger.

The tools for Δt_F determination are described in Sections IV-A and B.

A. SYNC TDC

Just after entering the chip, the phase of the signals with respect to the master clock is measured. In order to perform the phase measurement, and build the time distribution histograms

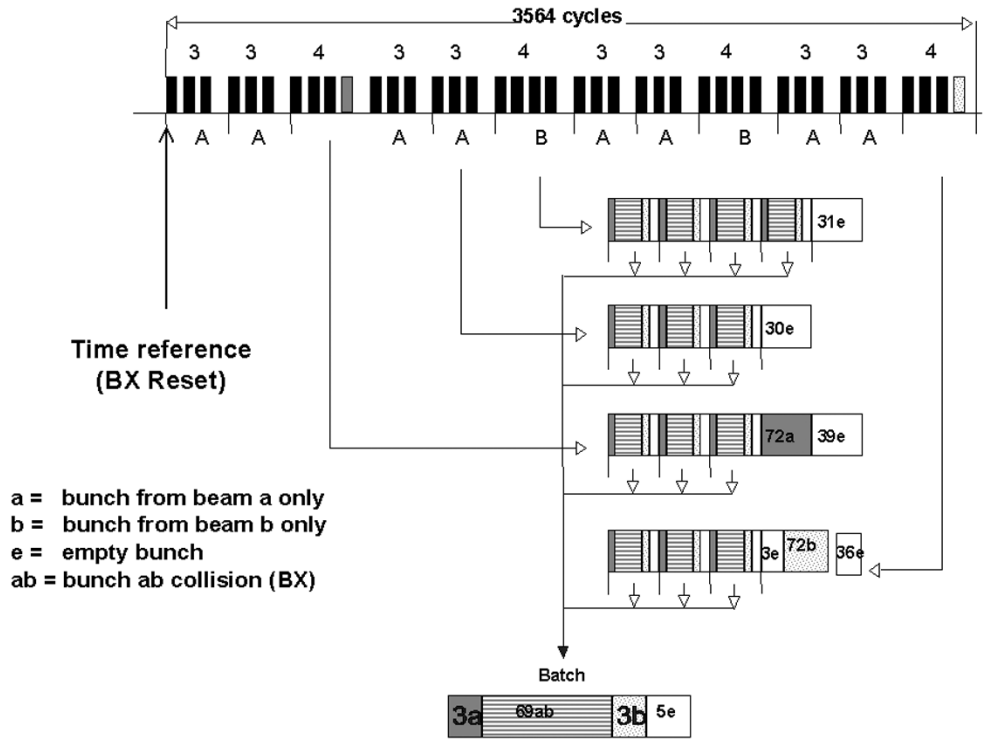

Fig. 8. LHCb orbit structure at the interaction point.

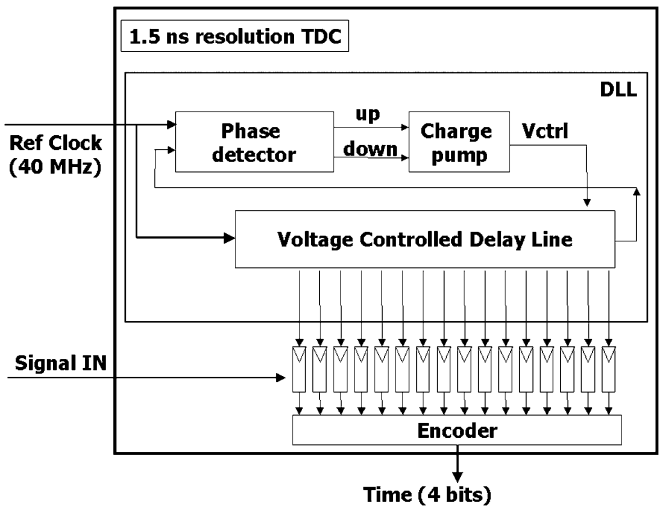

Fig. 9. Conceptual scheme of the SYNC TDC.

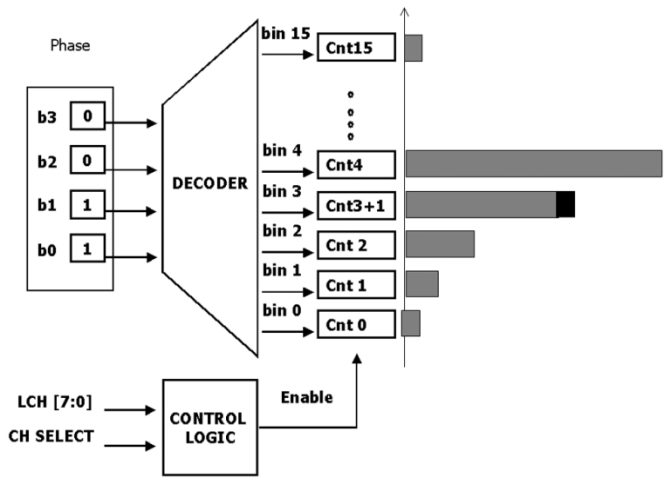

Fig. 10. SYNC Time histogram builder scheme.

for each SYNC channel, we developed a Time-to-Digital Converter (TDC), having a time resolution of about 1.5 ns. The SYNC TDC is based on the DLL cell already developed for the DIALOG calibration circuit. The block scheme of the TDC is shown in Fig. 9. The DLL is used to generate 16 de-phased 40.08 MHz clocks, starting from the chip master clock. Each clock runs with a delay of 1.56 ns with respect to the next one. The 16 clock signals clock continuously 16 flip-flops. When a signal arrives, it is input to all the 16 flip-flops. As a result a certain 16 bits code is output from the registers. This is encoded into 4 bits, being the number corresponding to the measure of the signal arrival time. This information is called *Fine Time*. The encoding operation is performed within one clock cycle, so the circuit can process a new signal every master clock cycle. The Fine Time information is written onto the pipeline memories for further use. The same information is used to build time distributions, one for each channel.

B. Time Histograms

The time distributions are built-up inside SYNC. This allows accumulating very high statistics without passing through the normal data acquisition chain, which would be much slower and heavy. As the Fine Time information is stored on the pipeline memories, it can be accessed also from the acquired data, after the normal trigger and data acquisition procedures. In such a way, the internally built time histograms are also a powerful crosscheck tool to monitor the correct operation of the read-out chain at different stages.

Time histograms are built according to the scheme of Fig. 10. Sixteen 24-bit counters are used for each channel. The Fine Time is used to select among the 16 counters. Every time a given code is received, the corresponding counter is incremented by one. When any of the 16 counters reaches the maximum allowed number (i.e., $2^{24}-1$), the counter update on all the group of 16 counters is disabled. The histograms' content is accessible via an I^2C interface.

The shape of the registered time histograms is used to calculate Δt_F for each channel.

V. Conclusion

System time alignment is crucial for the proper operation of the LHCb L0 muon trigger. Dedicated tools are needed to control the system time alignment and synchronization. We have described a number of tools for time measurement and time adjustment and monitoring which we plan to use in the procedures for synchronization of the LHCb muon system. These tools are integrated inside two custom chips, recently developed and successfully tested, named DIALOG and SYNC. The muon system electronics will contain about 4,000 SYNC chips and 8,000 DIALOG chips.

References

[1] A Wide range of information about the LHCb experiment. [Online]. Available: http://lhcb.web.cern.ch/lhcb/

[2] D. Moraes *et al.*, "CARIOCA—0.25 μm CMOS fast binary front-end for sensor interface using a novel current-mode feedback technique," in *Proc. IEEE Int. Symp. Circuits and Systems*, Sidney, Australia, May 6–9, 2001.

[3] P. Jarron *et al.*, "Deep submicron CMOS technology for the LHC experiments," *Nucl. Phys. B*, vol. 78, no. 1–3, pp. 625–634, Aug. 1999.

[4] S. Cadeddu and A. Lai, "DIALOG-β DATA SHEET," LHCb note-16, 2003.

[5] "I^2C-Bus Specifications v 2.1," Philips Semiconductor, 2000.

[6] J. G. Maneatis, "Low-Jitter process independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, Nov. 1996.

[7] C.-Y. Yang and S.-I. Liu, "A one-wire approach for skew-compensating clock distribution based on bidirectional techniques," *IEEE J. Solid-State Circuits*, vol. 36, Feb. 2001.