

# An 18.4 GHz Low-Jitter and Fast-Locking Fractional- $N$ Digital PLL Using Function-Reused TDC and Path-Selection BBPDs

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**Abstract**—This work presents an 18.4 GHz fractional- $N$  digital phase-locked loop (DPLL) featuring a novel digital phase and frequency detector (PFD), which combines the functions of the time-to-digital converter (TDC) and the path-selection bang-bang phase detectors (PS-BBPDs), achieving fast-locking time and low jitter with little hardware and power overhead. During the locking transient, the PFD functions as a TDC, ensuring a large lock-in range and accelerating the locking process. In the locked state, it functions as a PS-BBPDs to compensate quantization error (QE) with minimal thermal noise. The residual QE after the PS-BBPDs is compensated by a fine digital-to-time converter (F-DTC), which only needs to cover one LSB of the PS-BBPDs, ensuring low thermal noise and better linearity. Fabricated in a 28-nm CMOS technology, the proposed DPLL employs a 100-MHz reference (REF) clock, consumes 14.83-mW power, and occupies an active area of 0.11 mm<sup>2</sup>. At a fractional channel of 18.4066 GHz, it achieves an rms jitter of 124 fs. The measured worst case fractional spurs across all fractional frequency control words (FCWs) near 18.4 GHz remain below −54.8 dBc. At a frequency hopping of ±1.6 GHz, the DPLL achieves locking within 334 REF cycles (3.34 μs) with an accuracy of <60 ppm.

**Index Terms**—Bang-bang phase detector (BBPD), digital phase-locked loop (DPLL), digital-to-time converter (DTC), fast-locking, fractional- $N$ , frequency synthesis, low-jitter, phase and frequency detector (PFD), time-to-digital converter (TDC).

## I. INTRODUCTION

THE growing demand for high-speed wireless communications and high-accuracy radar systems has driven the expansion into millimeter-wave (mm-Wave) bands to

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accommodate wider channel and modulation bandwidths, which impose stringent phase noise (PN) and spurious tone constraints on the frequency synthesizer. For instance, in 5G FR2, the integrated PN (IPN) of the local oscillator (LO) needs to be lower than −34 dBc for 64-QAM [1], [2], corresponding to an rms jitter requirement of 160 fs at 28 GHz. In addition, to improve the power efficiency of mobile terminals and radar systems, duty-cycled operation enables the frequency synthesizer to power down during inactive periods. Thus, a frequency synthesizer with fast and reliable locking capabilities is crucial for maintaining efficient duty-cycled operation with minimal power overhead [3], [4].

Digital phase-locked loops (DPLLs) offer distinct advantages over their analog counterparts, particularly in ultrascaled technologies, due to their compact digital loop filters (DLFs) and compatibility with low supply voltages [5]. Their digitally intensive implementation also enables straightforward process node migration. The divider-based DPLLs can leverage the higher-order delta-sigma modulator (DSM) to effectively randomize the quantization error (QE) from the multimodulus divider (MMD) when synthesizing a fractional channel [6], thereby suppressing in-band fractional spurs. However, the higher-order DSM increases the range of accumulated QE ( $\phi_q$ ), which necessitates a digital phase and frequency detector (PFD) with a wide linear range. Besides, when a low-noise reference (REF) clock is used and the MMD's output is retimed by the digitally controlled oscillator (DCO), the remaining opportunity to optimize the in-band PN lies with the digital PFD. However, achieving a digital PFD with low noise and superior linearity is quite difficult.

The block diagram of a typical DPLL utilizing a multibit time-to-digital converter (TDC) is shown in Fig. 1(a) [7]. A fine-resolution TDC is desirable for minimizing quantization noise (Q-noise) and reducing the PLL's in-band PN. However, the resolution of a conventional flash TDC is fundamentally constrained by the CMOS technology, reaching only ~10 ps in the 28-nm CMOS [8]. Various structures have been proposed to enhance TDC resolution, such as the Vernier TDC [9], stochastic TDC [10], pipelined TDC [11], noise-shaping TDC [7], [12], time-amplifier-based TDC [13], [14], [15], and two-step TDC [16], [17]. However, these designs still face trade-offs between linearity, power consumption, area, and TDC range, ultimately limiting the jitter and fractional

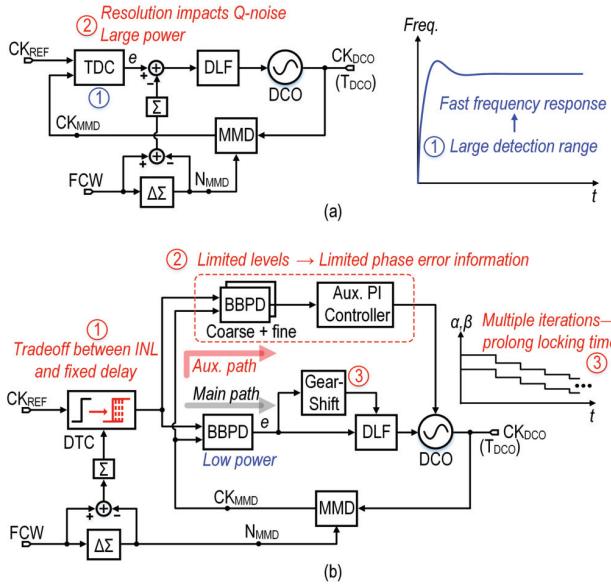


Fig. 1. Block diagrams of the divider-based fractional- $N$  DPLLS using (a) multibit TDC and (b) BBPD.

spur of these PLLs to 490 fs and  $-51.5$  dBc at a 4.5-GHz output [15]. Alternatively, a digital-to-time converter (DTC) can achieve fine resolution with lower power consumption. By incorporating a DTC for QE compensation, a narrow-range and high-gain bang-bang phase detector (BBPD) can be employed to suppress the in-band PN [18]. With digital predistortion to compensate for DTC nonlinearity, the BBPD-based DPLL (BB-DPLL) can achieve sub-100-fs jitter, including fractional spurs [19], [20], [21], [22], [23]. However, the BB-DPLL suffers from prolonged locking time due to the narrow linear range of the BBPD.

The TDC provides a large linear range, leading to a wide lock-in range.<sup>1</sup> Thus, the TDC-based DPLL generally exhibits a superior frequency acquisition capability and a fast-locking time [see Fig. 1(a)]. In contrast, the BB-DPLLS require additional circuits to accelerate the locking process [20], [26], [27]. As illustrated in Fig. 1(b), an auxiliary path with multilevel BBPDs is used to capture larger phase errors for fast locking. However, the number of BBPDs in the auxiliary path is typically restricted, which results in insufficient phase error information and leaves large frequency and phase errors to be corrected by the main path. Thus, the gear-shift technique is necessary to adjust the loop bandwidth, preventing limit cycles and minimizing locking time. However, this gear-shift operation relies on iterative adjustments to progressively reduce the frequency and phase error, which still limits the overall locking time.

In this work, we present a digital PFD that performs the functions of: a flash-type wide-range coarse TDC during the locking transient to reduce locking time, and a set of path-selection BBPDs (PS-BBPDs) in the locked state to achieve low jitter and fractional spurs with high power efficiency.

<sup>1</sup>The lock-in range of a PLL is defined as the maximum frequency deviation ( $|\Delta f|$ ) from the targeted frequency  $f_{CKV}$  that can be reacquired by the PLL without cycle slipping [24], [25]. In this work, the TDC operates within its linear region when  $|\Delta f|$  is smaller than the lock-in range.

With a multiplexer (MUX) to adaptively select the appropriate delay cells and corresponding BBPD, the PS-BBPDs reuse the TDC's delay line as a coarse DTC, providing coarse QE compensation. The fine QE compensation is achieved by a dedicated fine DTC (F-DTC). A sign-least-mean-square (sign-LMS) algorithm generates the adaptive selection signal, thereby keeping the input range of the F-DTC within one TDC step despite process, voltage, and temperature (PVT) variations and output frequency changes. In addition, the sign-LMS algorithm serves to calibrate the PS-BBPDs' nonlinearity and the F-DTC's gain, effectively suppressing the in-band PN and fractional spurs. This article is organized as follows. Section II presents the proposed DPLL architecture and operation principle. The locking behavior of the DPLL is elaborated in Section III. Section IV discusses the sign-LMS-based digital calibration of the proposed PFD. Section V analyzes the jitter contributions from individual building block. Section VI shows the experimental results, and Section VII draws the conclusion.

## II. DPLL USING THE PROPOSED VERSATILE DIGITAL PFD

### A. Overall Architecture and Operation Principle

Fig. 2(a) illustrates the overall architecture of the proposed fractional- $N$  DPLL. The DCO output ( $CK_{DCO}$ ) is divided by four through an inductor-less current-mode-logic (CML) divider to ease the speed requirement of the subsequent MMD. A MASH 1-1 DSM controls the MMD. Thus, the QE between the reference (REF) clock ( $CK_{REF}$ ,  $f_R = 100$  MHz) and feedback ( $CK_{MMD}$ ) clock due to fractional- $N$  operation is within two cycles of the MMD input clock ( $CK_{DIV4}$ ), i.e.,  $2T_{CKV}$ , resulting in  $\phi_q \in [0, 2]$ . In the conventional BB-DPLL, the DTC needs to cover this  $2T_{CKV}$  range to compensate  $\phi_q$  and ensure the BBPD is in the linear range during the locked state. Assuming  $T_{CKV} = 200$  ps for  $CK_{DIV4}$  at 5 GHz ( $f_{CKV} = FCW \cdot f_R = 5$  GHz), a 10-bit DTC is required to achieve a resolution of <400 fs. To maintain sufficient linearity, the variable-slope (VS) DTC [18], [28] relies on a large fixed delay [29], [30], which inevitably contributes additional thermal noise.

In this design,  $CK_{REF}$  is fed into the delay chain of a  $N_{tdc}$ -bit TDC covering a range of  $T_C = 2T_{CKV}$ . The DFFs in the TDC also function as BBPDs, which operate in the linear range when their two inputs are close enough. As long as the TDC characteristic is monotonic and the dedicated F-DTC can cover a range of one TDC LSB ( $2T_{CKV}/2^{N_{tdc}}$ ), only one BBPD operates in the linear range per REF cycle. Here, we choose  $N_{tdc} = 4$ . In the system model, we can normalize the QE to the TDC step by multiplying  $\phi_q$  with  $2^{N_{tdc}}$ , resulting in  $\phi_{qn} \in [0, 16]$ . The BBPD that operates within the linear range is adaptively selected based on  $\phi_{qn}$  to generate the phase error  $e_1$ . This approach effectively reuses the TDC as a coarse DTC during the locked state. Compared with the solution employing a dedicated VS-DTC for coarse QE compensation, where the DTC has a total delay much larger than  $2T_{CKV}$  due to the unavoidable fixed delay, the TDC embedded in the PS-BBPDs shows zero fixed delay and minimal hardware overhead, which offers minimal additional thermal noise and

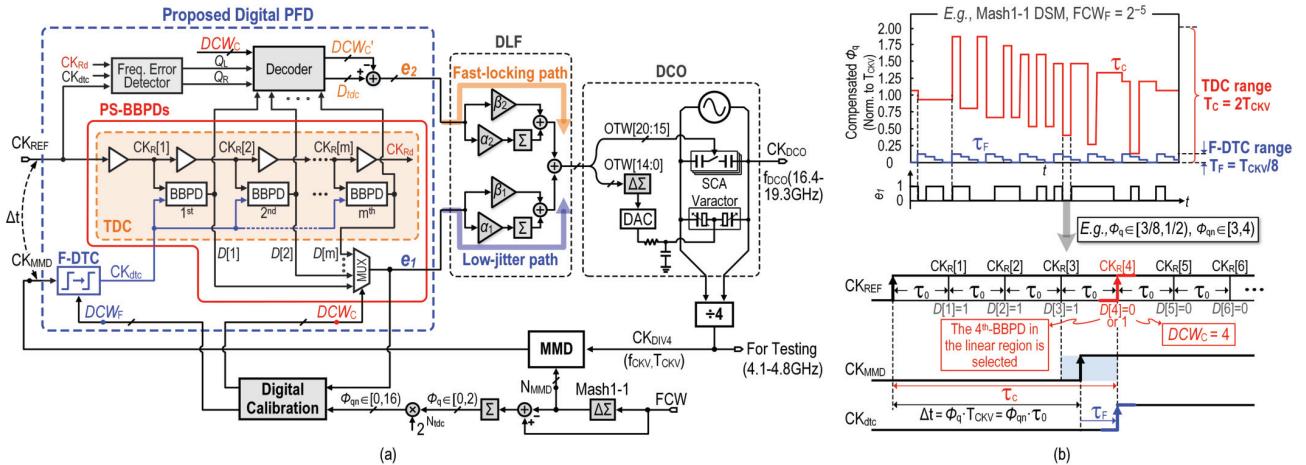


Fig. 2. (a) Overall architecture of the proposed fractional- $N$  DPLL and implementation of the proposed digital PFD (standard cells are highlighted with gray). (b) Operation principle of the proposed digital PFD under ideal conditions (an example with  $\text{FCW}_F = 2^{-5}$ ,  $\tau_0 = 1/8 \cdot T_{\text{CKV}}$ ).

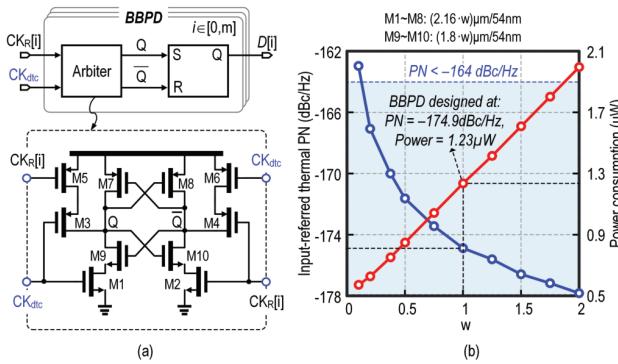


Fig. 3. (a) Schematic of the BBPD unit. (b) Input-referred thermal PN and power consumption of the BBPD under various transistor sizes.

better power efficiency [31]. However, digital predistortion is required to calibrate the TDC's INL, which will be detailed in Section IV.

When used for coarse QE compensation, the PS-BBPDs share a similar function to the PS-DTC described in [31], [32], [33], and [34]. However, in the prior art, multiple MUXs are placed on the critical input path to select analog signals. The mismatch of the MUX and delay cells may result in a nonmonotonic DTC characteristic [34]. In contrast, our BBPD exploits a symmetrical topology (see Fig. 3) to minimize mismatch and our dynamic selection MUX processes digital outputs from the BBPDs rather than analog inputs, which inherently secures monotonicity. On the other hand, the wide-range TDC embedded in the PS-BBPDs provides a large amount of phase error information, which significantly expands the PLL's lock-in range and accelerates the locking transient. This is beyond the capability of the prior PS-DTC and will be detailed in Section III.

Fig. 2(b) illustrates the operation of the proposed function-reused TDC and PS-BBPDs, where the fractional part of the frequency control word (FCW) is  $\text{FCW}_F = 2^{-5}$ . The input time error is  $\Delta t = t_M - t_R$ , with  $t_M$  and  $t_R$  being the time stamps of CK<sub>MMD</sub> and CK<sub>REF</sub>, respectively. In the PS-BBPDs, the CK<sub>REF</sub> traverses the delay chain, producing a group of delayed reference signals (CK<sub>R</sub>[1 : m]). Subsequently, CK<sub>R</sub>[i]

( $1 \leq i \leq m$ ) is compared with the delayed feedback signal (CK<sub>dtc</sub>) via the BBPD to determine if CK<sub>R</sub>[i] leads or lags CK<sub>dtc</sub>. In the locked state, by choosing  $\text{DCW}_C = \lceil \phi_{qn} \rceil$ , the MUX selects the BBPD whose input CK<sub>R</sub>[i] coming right after CK<sub>MMD</sub>, compensating the input time error ( $\Delta t = \phi_q \cdot T_{\text{CKV}}$ ) with a coarse delay  $\tau_C$ . For example, if  $3/8 \leq \phi_{qn} < 1/2$ , the fourth-BBPD is selected because  $3 \leq \phi_{qn} < 4$ . Since the delay step of the buffer chain is relatively coarse, an F-DTC is employed to generate a delay of  $\tau_F$  to compensate for the residual time error, aligning CK<sub>dtc</sub> with CK<sub>R</sub>[4] and ensuring the fourth-BBPD operates in linear range. The TDC step delay is  $\tau_0 = 25$  ps at the maximum output frequency of  $f_{\text{CKV}} = 5$  GHz, leading to a required dynamic range of 25 ps for the F-DTC.

When the DPLL synthesizes a lower output frequency,  $\tau_0$  will increase. For instance, at the minimum output frequency of  $f_{\text{CKV}} = 4$  GHz,  $\tau_0$  will rise to 31.25 ps if the TDC still employs 16 delay cells. To avoid expanding the F-DTC range, we increase the number of TDC delay cells from 16 to 25 while keeping the TDC delay step as 25 ps. This adjustment extends the total TDC range to 625 ps, which reliably covers  $2T_{\text{CKV}}$  at the minimum output frequency despite PVT variations. In this scenario, if  $3/8 \leq \phi_{qn} < 1/2$  at  $f_{\text{CKV}} = 4$  GHz, the adaptive selection mechanism will choose the fifth-BBPD instead of the fourth-BBPD, and the F-DTC dynamic range remains at 25 ps to align CK<sub>dtc</sub> with CK<sub>R</sub>[5]. To robustly cover this dynamic range across PVT variations, the F-DTC is designed with 7 bits ( $N_{\text{dte}} = 7$ ), delivering a dynamic range of 50 ps and a resolution of  $\sim 390$  fs. Such a resolution is small enough to ensure the BBPD operates in the linear region. Implemented with a VS topology, the F-DTC contributes an in-band PN lower than that of the REF clock when achieving an integral nonlinearity (INL) below 0.27 LSB, as will be detailed in Section IV. Moreover, the sign-LMS algorithm-based digital calibration uses the phase error  $e_1$  as an input to detect the nonlinearity of the PS-BBPDs and compensates through both the PS-BBPDs and the F-DTC. The adaptive selection of the correct BBPD is also managed by the digital calibration, which will be described in Section IV.

During the locking transient, the TDC output ( $D[1:m]$ ) is used to measure a large phase error. After thermometer to binary (T2B) decoding, the resulting output ( $D_{\text{tdc}}$ ) is compared with the modified predicted QE<sup>2</sup> ( $DCW'_C$ ) to generate the phase error  $e_2$ , which is sent to a DLF to form a fast-locking path [see Fig. 2(a)]. The PLL's lock-in range is proportional to the linear range of the PD. As a hard limiter, the BBPD is linearized by the random noise of its input, resulting in a very narrow linear range due to the low PLL noise. For instance, behavioral modeling indicates that a BB-DPLL with a 100-fs output jitter has an equivalent BBPD linear range of only 300 fs, leading to a narrow lock-in range of <1 MHz. In contrast, our TDC with a linear range of 625 ps significantly extends the lock-in range compared to a single BBPD solution. Meanwhile, large coefficients  $\alpha_2$  and  $\beta_2$  are chosen to boost the loop bandwidth of the fast-locking path, thereby extending the lock-in range to 153.6 MHz and accelerating the locking process. Once the DPLL is locked,  $D_{\text{tdc}}$  tracks  $DCW_C$ , such that  $e_2 = D_{\text{tdc}} - DCW'_C = 0$ , which automatically disables the fast-locking path. The frequency error detector and decoder implementations, as well as the locking behavior analysis, will be detailed in Section III. Consequently, only the low-jitter path in the separate DLF remains active to generate the DCO control word based on  $e_1$ , with the corresponding coefficients  $\alpha_1$  and  $\beta_1$  set independently to achieve optimal loop bandwidth for minimizing output jitter.

### B. Noise Performance of the PS-BBPDs

The delay cell of the PS-BBPDs exhibits a delay of 25 ps and consumes 5.0  $\mu\text{W}$  according to post-layout simulation results. The entire delay line, including dummy delay cells, consumes 0.38 mW at  $f_R = 100$  MHz. The simulated PNs at 1 MHz offset are <-168.6, <-165.8, and <-164 dBc/Hz at the minimum, middle and maximum delays, respectively, which is lower than the PN (<-162.9 dBc/Hz) of the REF clock. With this level of PN, the jitter contribution from the delay line's noise to the PLL's output is only 6.1% (at maximum delay), as will be shown in Section V. If a REF clock with lower PN is available, the delay line's PN can be further reduced by increasing transistor sizes and power consumption. For example, increasing transistor sizes by 25% and 50% results in <6% variation in delay time. In these cases, the delay line's PN at 1 MHz offset are reduced by 1.2 and 1.9 dB, while power consumption increases by 48% and 97%.

The intrinsic noise of the BBPD directly depends on the transistor dimensions and thus the power consumption. For the proposed PS-BBPDs, which incorporate multiple bang-bang detectors, choosing appropriate transistor sizes is crucial to reducing power consumption while maintaining adequate PN performance. Fig. 3(a) shows the BBPD topology used in this design [35], [36], comprising an arbiter followed by a cascaded SR-latch. Here, the transistors M1–M8 contribute most of the noise; thus, their sizes are relatively large to minimize their impact on PN. The nMOS regenerative pair (M9, M10), used to cutoff the dc path from VDD to GND, can be sized smaller

<sup>2</sup>The generation from  $DCW_C$  to  $DCW'_C$  will be detailed in Section III [see Fig. 4].

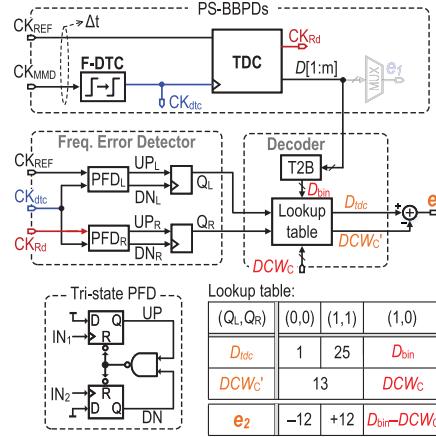


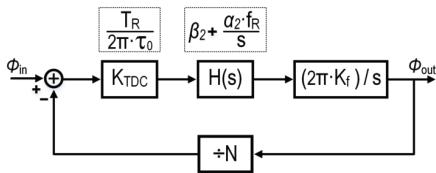
Fig. 4. Implementation of the frequency error detector and decoder in the proposed digital PFD.

to reduce loading at the output nodes, which helps reduce power consumption.

Since the BBPD is a nonlinear circuit with a large input/output signal, evaluating its performance by an analytical method is challenging. Instead, we resort to circuit simulations to investigate its performance and optimize the transistor size. The BBPD is essentially a comparator, where the dynamic preamplifier is an arbiter. Thus, we assume the input-referred noise of the BBPD follows a Gaussian distribution and simulate it using the method described in [37]. Once the cumulative distribution function of the Gaussian noise is obtained, we can compute the rms jitter ( $\sigma$ ) caused by the Gaussian noise and relate it to the input-referred thermal PN ( $\mathcal{L}$ ) by using  $\sigma/T_R = (\mathcal{L} \cdot f_R)^{1/2}/(2\pi)$  [38], where  $T_R = 1/f_R$ . Fig. 3(b) presents the simulated BBPD input-referred thermal PN and power consumption as the sizes of M1–M8 are varied from 0.216  $\mu\text{m}/54$  nm to 4.32  $\mu\text{m}/54$  nm. The BBPD's input-referred thermal PN is <-173.4 dBc/Hz when the BBPD consumes >1  $\mu\text{W}$ , indicating that the BBPD can achieve superior performance while consuming negligible power. In this work, we design the BBPD with a power consumption of 1.23  $\mu\text{W}$ , achieving a PN of <-174.9 dBc/Hz, which is significantly lower than that of the delay line. The 25 BBPDs together dissipate only 30.8  $\mu\text{W}$ , which is lower than the power consumed by the delay line. Therefore, the multiple BBPDs design incurs almost no penalty in the jitter-power trade-off.

### III. FAST LOCKING AIDED BY THE PROPOSED DIGITAL PFD

Since the TDC detects the phase error between CK<sub>REF</sub> and CK<sub>dtc</sub>, it cannot distinguish the frequency difference between them. As a result, if the initial frequency error ( $\Delta f_{\text{ini}}$ ) exceeds the lock-in range, cycle slipping will occur during the locking transient, significantly prolonging the locking time or even causing locking failure, similar to the behavior observed in the subsampling PLL (SS-PLL) [25]. To address this issue, a simple frequency error detector is placed ahead of the TDC decoder [14], [15], as illustrated in Fig. 4. This detector consists of two classic tri-state PFDs, where both PFD<sub>L</sub> and PFD<sub>R</sub> share a common input (IN<sub>2</sub>) triggered by CK<sub>dtc</sub>. Their other inputs (IN<sub>1</sub>) are triggered by CK<sub>REF</sub> and CK<sub>Rd</sub>, respectively.

Fig. 5. Linear  $s$ -domain model of the TDC-based type II PLL.

This setup creates a deadzone equal to the range of the TDC's delay line,  $T_C$ .

The UP signals from the two PFDs are sampled by their respective DN signals to generate  $Q_L$  and  $Q_R$ . When the time error  $\Delta t$  exceeds  $T_C$ , both  $Q_L$  and  $Q_R$  are either 0 or 1, setting  $D_{\text{tdc}}$  to its minimum (1) or maximum ( $m = 25$ ). Meanwhile,  $\text{DCW}'_C$  is set to 13, resulting in  $e_2 = D_{\text{tdc}} - \text{DCW}'_C = -12$  or +12, ensuring that the frequency correction step applied to the DCO remains identical for both positive and negative  $\Delta f_{\text{ini}}$ . When the TDC operates in the linear region,  $Q_L = 1$  and  $Q_R = 0$ , so that  $D_{\text{tdc}}$  equals the T2B decoder output ( $D_{\text{bin}}$ ). In this case,  $\text{DCW}'_C = \text{DCW}_C$ , yielding  $e_2 = D_{\text{bin}} - \text{DCW}_C$ . The output of the low-jitter path ( $e_1$ ) has a minor influence during the locking process due to the narrow linear range of the single BBPD. Thus, we only consider the output of the fast-locking path ( $e_2$ ) in the following analysis.

When choosing the loop coefficients for the fast-locking path ( $\alpha_2$  and  $\beta_2$ ) to minimize locking time and ensure stability, the linear  $s$ -domain model is useful as an analogy despite the DPLL is inherently nonlinear [20]. Fig. 5 depicts the linear  $s$ -domain model of the TDC-based type II PLL. The input-to-output transfer function is given by [20]

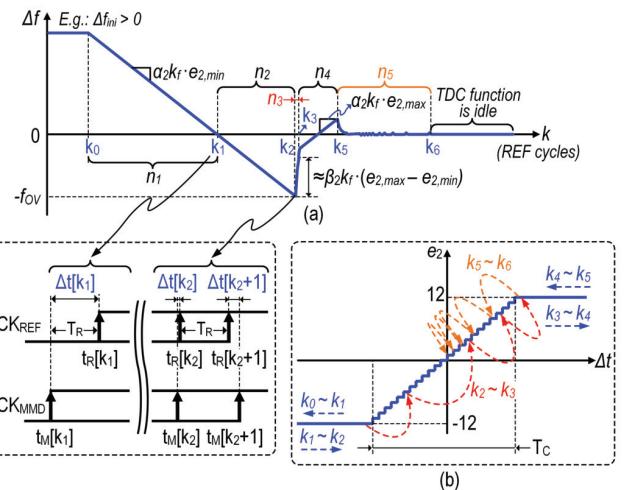
$$H_{\text{cl}}(s) = \frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{NK(\alpha_2/\beta_2 \cdot f_R + s)}{s^2 + Ks + K \cdot \alpha_2/\beta_2 \cdot f_R} \quad (1)$$

where  $K = \beta_2 T_R K_f / (N\tau_0)$ ,  $K_f = K'_f/4$  and  $K'_f$  is the bit-to-frequency resolution of the DCO.<sup>3</sup> When  $\alpha_2/\beta_2 < K/(4f_R)$ , the two poles of  $H_{\text{cl}}(s)$  are real and the bandwidth depends on the one closer to the imaginary axis. As  $\alpha_2/\beta_2$  increases, the two poles move toward each other. When  $\alpha_2/\beta_2 = K/(4f_R)$ , the poles are real and coincide, resulting in the largest bandwidth and minimal locking time. For  $\alpha_2/\beta_2 > K/(4f_R)$ , the two poles form a complex-conjugate pair. The phase margin degrades, and the system becomes less stable if  $\alpha_2/\beta_2$  is increased further. Given that  $K/(4f_R) \approx 2^{-3}$ , we choose  $\alpha_2/\beta_2 = 2^{-4}$  in this design to guarantee loop stability.<sup>4</sup> This system's step response exhibits exponential decay with a settling time constant of  $(\xi\omega_n)^{-1}$ , where  $\xi$  is the damping ratio and  $\omega_n$  is the natural frequency. Since  $\xi\omega_n = K/2$  and  $K$  is proportional to  $\beta_2$ , a large  $\beta_2$  of 2 is chosen for a small time constant and thus fast settling,<sup>5</sup> making  $\alpha_2 = 2^{-3}$ . In addition, during the locking period, the bandwidth of the low-jitter path is extended ( $\beta_1 = 2^{-6}$  and  $\alpha_1 = 2^{-10}$ ) to avoid limit cycles.

<sup>3</sup>Here, the CK<sub>DCO</sub> is divided by four to obtain CK<sub>DIV4</sub>, making  $K_f = K'_f/4$ .

<sup>4</sup>In this work, the DLF coefficients are designed as a power of 2 to facilitate convenient bit-shift in digital circuits.

<sup>5</sup>If  $\beta_2$  is increased further, the residual frequency error will be larger when the TDC becomes idle, which will exceed the lock-in range of the BB-DPLL in our low-jitter path. Thus, limit cycles will occur and prolong the locking time. A similar case is analyzed in [20].

Fig. 6. (a) Illustration of the worst case locking process. (b) Transfer function of  $\Delta t$  to  $e_2$  in integer- $N$  mode.

To analyze the locking process and worst case locking time of the DPLL, we can start with the integer- $N$  mode for simplicity. Since  $D_{\text{bin}} = 1 \sim 25$ , to attain a symmetrical positive and negative detection range for the TDC, we set  $\text{DCW}_C = 13$  in integer- $N$  mode. The transfer function of  $\Delta t$  to  $e_2$  is shown in Fig. 6(b). Assuming a positive  $\Delta f_{\text{ini}}$  between the transient ( $f_D$ ) and the target ( $f_{CKV}$ ) frequencies of the divide-by-4 output (CK<sub>DIV4</sub>), i.e.,  $\Delta f_{\text{ini}} = f_D - f_{CKV} > 0$ , the loop locking process is illustrated in Fig. 6(a). At  $k_0$  (in units of REF cycle), a large frequency hop occurs, and the input time error  $\Delta t$  quickly exceeds the TDC's linear range. The loop starts searching the oscillator tuning word (OTW) for the DCO's switched-capacitor array (SCA), and the TDC shows bang-bang behavior. In  $k_0 \sim k_2$ , the correction amount of  $\Delta f$  is  $f_c = \alpha_2 K_f \cdot e_{2,\text{min}} = -4.8$  MHz per REF cycle, where  $K_f = K'_f/4 \approx 12.8/4$  MHz = 3.2 MHz. The REF cycles consumed to reduce  $\Delta f$  from  $\Delta f_{\text{ini}}$  to 0 is

$$n_1 = \Delta f_{\text{ini}}/|f_c|. \quad (2)$$

The time error at  $k_1$  ( $\Delta t[k_1]$ ) could range from  $-T_R$  to 0 because of the uncertain initial time error ( $\Delta t_{\text{ini}}$ ).<sup>6</sup> During  $k_1$  to  $k_2$ , the loop gradually eliminates  $\Delta t$  until  $\Delta t[k_2] \approx 0$ . Thus, we have

$$\Delta t[k_2] = \Delta t[k_1] + \sum_{j=1}^{n_2} \frac{\text{FCW}}{f_{CKV} + f_c \cdot j} - n_2 \cdot T_R \quad (3)$$

where  $n_2 = k_2 - k_1$  and  $n_2$  reaches maximum when  $\Delta t[k_1] = -T_R$ . Meanwhile, the overshoot frequency at  $k_2$  is the largest, which can be estimated by

$$\text{fov} \approx |f_c| \cdot n_{2,\text{max}} \quad (4)$$

By combining (3) with (4), we can obtain  $\text{fov} \approx 196.8$  MHz and  $n_{2,\text{max}} \approx 41$ . As illustrated by the timing diagram in Fig. 6(a)

$$\Delta t[k_2 + 1] - \Delta t[k_2] = \frac{\text{FCW}}{f_{CKV} + \Delta f[k_2]} - T_R. \quad (5)$$

<sup>6</sup>Once  $|\Delta t|$  exceeds  $T_R$ , it is wrapped by the frequency error detector to 0.

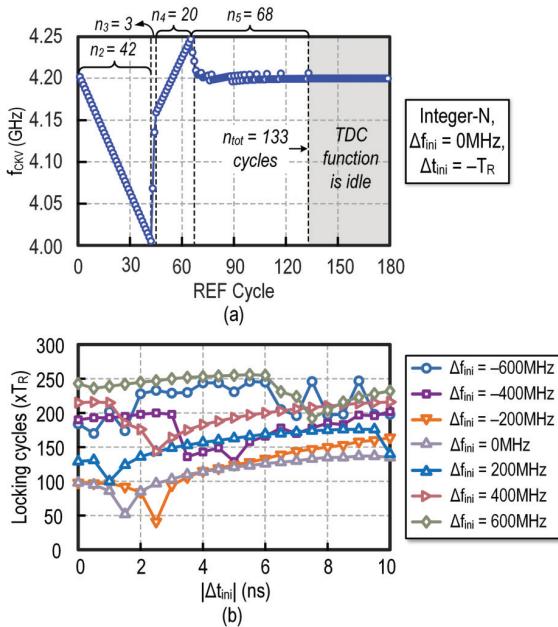


Fig. 7. Behavioral simulation results in integer- $N$  mode. (a) Simulated locking transient when  $\Delta f_{ini} = 0$  MHz and  $\Delta t_{ini} = -T_R$ . (b) Simulated locking time under various  $\Delta f_{ini}$  and  $\Delta t_{ini}$ .

Since  $f_{CKV,\min} = 4$  GHz,  $\Delta f[k_2]_{\min} = -f_{OV}$  and  $\Delta t[k_2] \approx 0$ , we have  $\Delta t[k_2+1]_{\max} \approx 517$  ps <  $T_C = 625$  ps. Thus, in the several REF cycles of  $n_3 = k_3 - k_2$ ,  $\Delta t$  enters the TDC's linear region, avoiding the abrupt change of  $e_2$  from  $-12$  to  $+12$  and preventing limit cycles.

The maximum  $\Delta f$  correction generated by proportional path (P-path) is  $f_P = \beta_2 K_f \cdot (e_{2,\max} - e_{2,\min}) = 153.6$  MHz. If the overshoot frequency  $|\Delta f[k_2]|$  is smaller than  $f_P$ , the frequency error can be quickly corrected by the loop's P-path, and the TDC remains in the linear region; thus, the lock-in range is approximately equal to  $f_P$ .<sup>7</sup> However, when  $|\Delta f[k_2]| > f_P$ , the loop cannot rely on the P-path to quickly reduce  $\Delta f$  to 0, and  $\Delta t$  will exceed the TDC's linear range again. Thus, during  $k_3$  to  $k_5$ , the loop's integral path (I-path) changes  $\Delta f$  by  $f_C = \alpha_2 K_f \cdot e_{2,\max} = 4.8$  MHz per REF cycle, thereby  $\Delta t$  is accumulated until its sign changes again at  $[k_5 + 1]$ . Since both  $\Delta t[k_3]$  and  $\Delta t[k_5]$  are close to the TDC's linear range,  $\Delta f[k_5] \approx -\Delta f[k_3] \approx f_{OV} - f_P = 43.2$  MHz at worst case, leading to  $n_4 = k_5 - k_3 \approx 2(f_{OV} - f_P)/f_C = 18$ . To verify the above analysis, the simulated locking transient when  $\Delta f_{ini} = 0$  MHz and  $\Delta t_{ini} = -T_R$  is plotted in Fig. 7(a). The simulated  $n_2$ ,  $n_3$ , and  $n_4$  match well with the predicted results.

Since  $\Delta f[k_5]$  lands within the lock-in range of the TDC, both  $\Delta f$  and  $\Delta t$  are rapidly rectified in  $n_5 = k_6 - k_5$ . After  $k_6$ , the TDC function becomes idle. The frequency has settled with an accuracy of  $<60$  ppm, and we can consider the loop as locked.<sup>8</sup> Based on behavioral simulation, when  $\Delta t \approx 0$  and

<sup>7</sup>To achieve fast locking and avoid instability issues, the coefficient of the P-path ( $\beta_2$ ) is set to be  $2^4$  times of the I-path ( $\alpha_2$ ). When the sign of  $\Delta t$  changes, the correction amount of  $\Delta f$  is dominated by the loop's P-path. Thus, we can ignore the correction amount caused by the I-path when estimating the lock-in range.

<sup>8</sup>In this work, the locking time is observed when settling to a frequency accuracy is  $<60$  ppm. This accuracy is chosen for a reasonable comparison with the locking performance of recent works in [27] ( $<70$  ppm) and [20] ( $<80$  ppm).

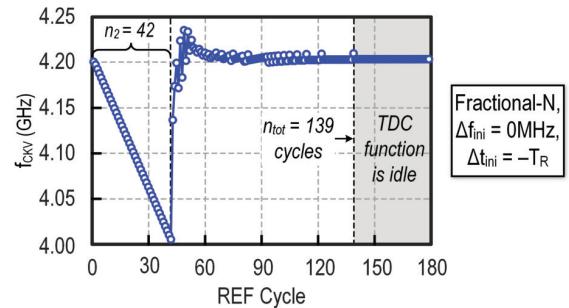


Fig. 8. Simulated locking transient in fractional- $N$  mode when  $\Delta f_{ini} = 0$  MHz and  $\Delta t_{ini} = -T_R$  ( $FCW_F = 2^{-5}$ ).

$|\Delta f| < f_P$ , the worst case locking time, i.e.,  $n_{5,\max}$ , is 101 REF cycles.

In summary, thanks to the large lock-in range,  $\Delta f$  will only exhibit one positive and one negative overshoot in the worst case. At a large  $\Delta f_{ini}$  of 600 MHz,  $n_1 = 125$ . The total worst case locking time can be estimated as

$$n_{tot} \approx n_1 + n_2 + n_4 + n_5 = 285 \quad (6)$$

where  $n_3$  is just several cycles and can be ignored. According to the behavioral simulations at various  $\Delta t_{ini}$  and  $\Delta f_{ini}$  conditions [see Fig. 7(b)], the worst case locking time for achieving a frequency accuracy of  $<60$  ppm is 252 REF cycles, which is smaller than the estimated 285 mainly because  $n_5$  is overestimated in (6). The locking time increases as  $|\Delta f_{ini}|$  increases because it takes longer to reduce the frequency error within the lock-in range. If the  $\Delta f_{ini}$  can be rapidly calibrated to within the lock-in range, the TDC can stay in the linear region during the locking transient and the locking time can be reduced to within  $n_{5,\max} = 101$  REF cycles (1.01  $\mu$ s at  $f_R = 100$  MHz).

In the fractional- $N$  mode, when the TDC saturates ( $|\Delta t| > T_C$  for  $n_1 \sim n_4$ ), the DCW<sub>C</sub> is set to a fixed value of 13, causing the PS-BBPDs' output  $e_2 = D_{bin} - DCW_C$  to be  $\pm 12$ . Thus, the locking behavior is the same as that in integer- $N$  mode. When the TDC operates in its linear range ( $|\Delta t| < T_C$  for  $n_5$ ), the DCW<sub>C</sub>, generated by the calibration circuit and DSM, is always varying. This leads to a variable upper/lower limit of the TDC. For example, if DCW<sub>C</sub> = 16 in a REF cycle, the upper limit becomes  $m - DCW_C = 9$ , rather than 12 as in integer- $N$  mode. If the phase error due to frequency error exceeds 9, the TDC will saturate. Meanwhile, the lower limit is extended to  $-15$ . With each update of DCW<sub>C</sub>, the boundary of the TDC changes, which is unavoidable due to the function-reuse feature of the TDC for both QE compensation and frequency error detection. However, DCW<sub>C</sub> has a high probability density around the middle value of 13, making the average boundary the same as in integer- $N$  mode. Thus, the impact on locking time in fractional- $N$  mode is negligible, which is also supported by the simulation results shown in Fig. 8, where  $\Delta f_{ini} = 0$  MHz,  $\Delta t_{ini} = -T_R$ , and  $FCW_F = 2^{-5}$ . The locking time is 139 REF cycles, which is almost equal to the locking time of 133 REF cycles in integer- $N$  mode [see Fig. 7(a)]. Behavioral simulations with  $\Delta f_{ini} = -600 \sim +600$  MHz and  $|\Delta t_{ini}| = 0 \sim T_R$  were also conducted. The locking times are under 257 REF cycles, proving that the

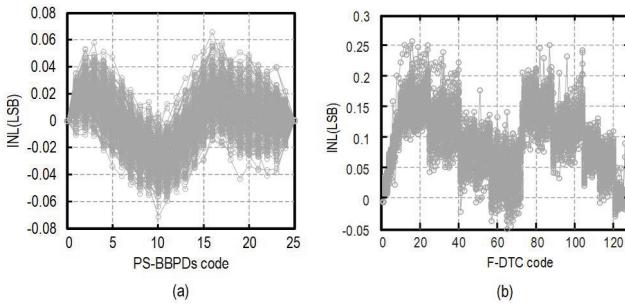
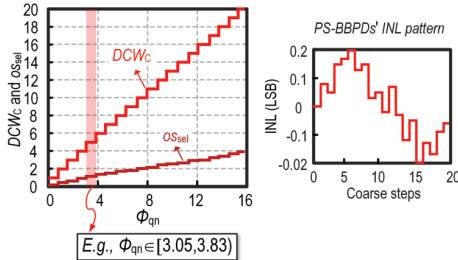


Fig. 9. Simulated INL of (a) PS-BBPDs and (b) F-DTC. Monte-Carlo number of points = 300.



(1) Ideal PS-BBPDs:  $DCW_C = \lceil \phi_{qn} \rceil = 4 \rightarrow CK_R[4]$  is selected.

(2) Nonlinear PS-BBPDs:

$DCW_C = \lceil \phi_{qn} + OS_{sel} \rceil = \lceil \phi_{qn} + 1.17 \rceil = 5 \rightarrow CK_R[5]$  is selected.

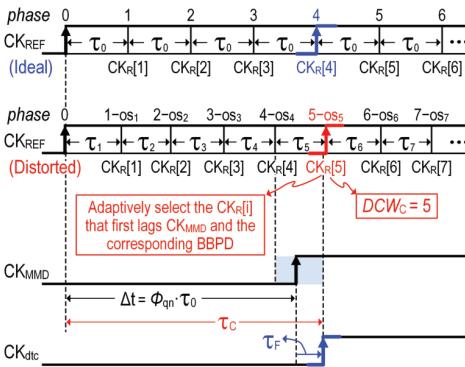


Fig. 10. Operation principle of the proposed calibration method, where the gain error of the PS-BBPDs is assumed as +20%.

function-reuse ability of the TDC for QE compensation has only a minor impact on the total locking time.

#### IV. DIGITAL CALIBRATION OF THE PROPOSED DIGITAL PFD

For the DTCs with fine-grained delay control spanning a wide range, the calibration methods proposed in [39] and [40] use piecewise first-order curve fitting and second-third-order polynomial curve fitting, respectively, to cancel the INL and effectively suppress fractional spurs. In contrast, for the PS-BBPDs with coarse delay steps, the nonlinearity primarily stems from the layout mismatch between individual delay cells. The Monte-Carlo simulation results in Fig. 9 show the INL of the PS-BBPDs including the extracted parasitics. Thus, calibrating the gain between adjacent coarse codes is unnecessary. Instead, a simple offset correction for each delay cell is sufficient to fit the target INL curve.

The step of the ideal PS-BBPDs is expressed as

$$\tau_0 = \frac{2 \cdot T_{CKV}}{2^{N_{tdc}}} \quad (7)$$

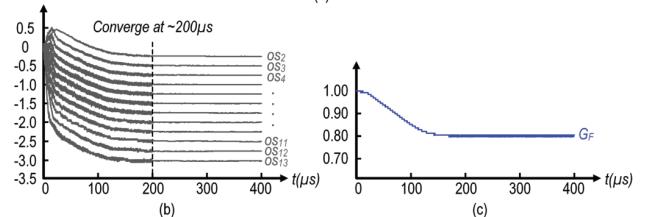
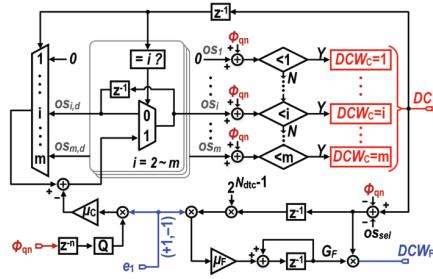


Fig. 11. (a) Implementation of the offset calibration of the PS-BBPDs and gain calibration of the F-DTC. The simulated digital calibration convergence transient of (b) PS-BBPDs and (c) F-DTC, where the gain error of both the PS-BBPDs and the F-DTC is +20%.

where  $T_{CKV} = 1/(FCW \cdot f_R)$ . The nonlinearity of the PS-BBPDs includes the deviation of buffers' delay from  $\tau_0$ , the mismatch of the BBPDs and the skew of BBPD's input edges. Since the above nonlinearity sources are uncorrelated, we can combine them and denote the equivalent delay of the delay cell in the nonlinear PS-BBPDs as  $\tau_i$  ( $1 \leq i \leq m$ ) (see Fig. 10).

Define the normalized phase offset between the ideal and distorted CK<sub>R</sub>[i] as os<sub>i</sub>, which is obtained by normalizing the timing difference to the ideal PS-BBPDs' unit delay  $\tau_0$

$$os_i = \frac{i \cdot \tau_0 - \sum_{j=1}^i \tau_j}{\tau_0}. \quad (8)$$

Consider the phase of CK<sub>REF</sub> as 0, the normalized absolute phase of CK<sub>R</sub>[i] can be derived as  $i - os_i$  from (8). In each cycle with a QE  $\phi_{qn}$ , the PS-BBPDs select the  $n^{\text{th}}$ -BBPD whose input CK<sub>R</sub>[n] has the smallest positive phase error relative to  $\phi_{qn}$ . As illustrated in Fig. 11(a), this selection is accomplished by incrementally searching the path that first satisfies  $(i - os_i) > \phi_{qn}$  for  $i = 2 \sim m$ . Only one BBPD will be selected without ambiguity thanks to the PS-BBPDs' monotonicity. The BBPD selection signal can be expressed as

$$DCW_C = \lceil \phi_{qn} + os_n \rceil \quad (9)$$

where os<sub>n</sub> is the offset of the  $n^{\text{th}}$  BBPD path, and the operator  $\lceil \cdot \rceil$  represents the ceiling function. Furthermore, before the loop is locked, the PD output primarily reflects frequency and phase errors, masking the INL information of the PD. Therefore, during cold start, the calibration is initiated only after the PLL is locked.

To illustrate the calibration concept, consider the PS-BBPDs with a normalized gain  $G_C = 0.8$  and INL pattern depicted in Fig. 10. Applying (8), we can express the combined gain error and INL-induced phase offset as

$$os_i = i - iG_C + \text{INL}(i) = 0.2i + \text{INL}(i). \quad (10)$$

In an ideal scenario, the range  $3.05 \leq \phi_{qn} < 3.83$  corresponds to the selection of CK<sub>R</sub>[4] [see Fig. 2(b)]. However, when

$\text{CK}_R[i]$  experiences distortion from gain error and INL, our analysis identifies the fifth-BBPD as the first to fulfill the condition  $5 - \text{os}_5 = 5 - (0.2 \times 5 + 0.17) = 3.83 > \phi_{\text{qn}}$ . Consequently,  $\text{CK}_R[5]$  becomes the delayed REF phase that first lags  $\text{CK}_{\text{MMD}}$ , with the F-DTC compensating for the residual phase offset within a delay range of  $\tau_5$ . Prior to convergence of  $\text{os}_i$ , correlation persists between  $\phi_{\text{qn}}$  and  $e_1[k]$ , prompting continuous adjustment of  $\text{os}_i$  by the LMS algorithm.

The F-DTC covers a modest range of 50 ps, with Monte-Carlo simulations indicating an INL of <105 fs, corresponding to 0.27 LSB of the F-DTC, as shown by Fig. 9(b). This minimal nonlinearity permits effective fractional spur reduction through gain error calibration alone. The F-DTC control code, which addresses residual QE, is formulated as

$$\begin{aligned} \text{DCW}_F &= \left\lfloor \frac{(\text{DCW}_C - \phi_{\text{qn}} - \text{os}_n) \cdot \tau_0}{t_{\text{res}}} \right\rfloor \\ &= \left\lfloor (\text{DCW}_C - \phi_{\text{qn}} - \text{os}_n) \cdot G_F \cdot 2^{N_{\text{dte}}-1} \right\rfloor \end{aligned} \quad (11)$$

where  $t_{\text{res}}$  is the time resolution of F-DTC and  $G_F = \tau_0/(t_{\text{res}} \cdot 2^{N_{\text{dte}}-1})$  is the normalized gain of F-DTC. The LMS calibration will update  $G_F$  until  $\text{DCW}_F$  is uncorrelated with  $e_1[k]$  (see Fig. 11).

In contrast to the zero-order interpolation (ZOI) method presented in [31], which needs gain calibration of the PS-DTC for path selection, the proposed adaptive PS-BBPDs selection algorithm employs only addition and subtraction, eliminating complex multiplication operations and reducing hardware cost [see Fig. 11(a)]. The F-DTC's gain is calibrated through a separate sign-LMS loop. To avoid conflict between the two LMS loops, their scaling factors are set with  $\mu_C \gg \mu_F$ . The simulated convergence transients of the calibration coefficients are plotted in Fig. 11(b) and 11(c), with both the PS-BBPDs and the F-DTC exhibiting an initial gain error of +20%. The simulation results confirm that the exercised  $\text{os}_2$  to  $\text{os}_{13}$  and  $G_F$  converge within  $\sim 200 \mu\text{s}$  by setting the scaling factors to  $\mu_C = 2^{-9}$  and  $\mu_F = 2^{-20}$ . Following convergence,  $\mu_C$  and  $\mu_F$  are shrunk to minimize the noise contribution from LMS loops. These calibrations can track slow changes in the DTC's characteristics caused by temperature drift, ensuring stable performance [6].

The calibration does not need to be reactivated to obtain new coefficients during frequency hopping events. Instead, the new coefficients can be directly derived from the previous calibrated values through a preknown FCW ratio, ensuring seamless jitter performance in the presence of fast frequency hopping. At system power-up, a one-time calibration is performed in a fractional channel to obtain an initial set of coefficients, denoted as  $\text{os}_i$  and  $G_F$ . From (8), the absolute phase of the edges  $\text{CK}_R[i]$  is

$$\sum_{j=1}^i \tau_j = (i - \text{os}_i) \cdot \tau_0. \quad (12)$$

When  $\text{FCW}_0$  changes to  $\text{FCW}_1$ , the ideal PS-BBPDs' step also changes from  $\tau_0$  to  $\tau'_0$ , which can be expressed by

$$\tau'_0 = \frac{2 \cdot 1 / (\text{FCW}_1 \cdot f_R)}{2^{N_{\text{dte}}}}. \quad (13)$$

Substitute (7) into (13), we can obtain

$$\tau'_0 = \tau_0 \cdot \frac{\text{FCW}_0}{\text{FCW}_1}. \quad (14)$$

Similar to (8), the new group of offset coefficients  $\text{os}'_i$  after frequency hopping is

$$\text{os}'_i = i - \frac{\sum_{j=1}^i \tau_j}{\tau'_0}. \quad (15)$$

By substituting (14) and (8) into (15) to eliminate  $\tau_0$  and  $\tau'_0$ , we obtain

$$\text{os}'_i = i - (i - \text{os}_i) \cdot \frac{\text{FCW}_1}{\text{FCW}_0}. \quad (16)$$

Since the ratio  $\text{FCW}_1/\text{FCW}_0$  is known, the equation (16) can be used to update calibrated offsets of PS-BBPDs after frequency hopping. For the F-DTC, based on the definition of  $G_F = \tau_0/(t_{\text{res}} \cdot 2^{N_{\text{dte}}-1})$  [from (11)] and substitute (14), we have

$$G'_F = G_F \cdot \frac{\text{FCW}_0}{\text{FCW}_1}. \quad (17)$$

As long as the voltage and temperature do not change abruptly,  $\text{os}'_i$  and  $G'_F$  can be mapped to the target value immediately. In this way, the calibration loop can swiftly track frequency changes. The relationship between the new and old offset coefficients follows the ratio  $\text{FCW}_1/\text{FCW}_0$ , which reflects how output frequency changes alter the ideal time delay corresponding to  $\phi_{\text{qn}}$ . While the coefficient mapping technique was not implemented in the current prototype, it relies on simple digital circuits and can be incorporated with some hardware overhead.

## V. JITTER CONTRIBUTIONS

Since the proposed DPLL operates as a BB-DPLL in the steady state, we can conduct PN analysis based on the discrete time-variant noise model introduced in [41]. Fig. 12(a) presents the simulated PN at the PLL's output contributed by the DCO, REF clock, MMD, BBPD's Q-noise and thermal noise, PS-BBPDs' delay line and F-DTC. The jitter breakdown is summarized in Fig. 12(b). The total integrated jitter (from 1 kHz to 100 MHz) at the divide-by-4 output ( $f_{\text{CKV}} = 46 \times 100\text{M} = 4.6 \text{ GHz}$ ) is 94.6 fs. The out-of-band PN is dominated by the DCO. Assisted by a MASH 1-1-1 DSM, the DCO quantization noise is negligible. The retiming DFF<sup>9</sup> at the MMD's output is not optimally designed. With a power consumption of only 18  $\mu\text{W}$ , its PN at the 1 MHz offset is only  $-159.1 \text{ dBc/Hz}$ , making it the dominant source of in-band PN. Simulation indicates that increasing the size and power consumption of the retiming DFF to 64  $\mu\text{W}$  would improve its PN at the 1 MHz offset to  $-165.4 \text{ dBc/Hz}$ , effectively reducing its jitter contribution to 9%.

When considering the maximum delay, the PS-BBPDs' delay line contributes only 6.1% to the total jitter. Since the

<sup>9</sup>The MMD uses the Vaucher divider topology, which consists of a cascade of divide-by-2/3 cells [42]. To eliminate the accumulated jitter from the divide-by-2/3 cells, a DFF triggered by the MMD's input clock ( $\text{CK}_{\text{DIV4}}$ ) is used to retime the MMD's output [43], [44]. As a result, the output jitter at  $\text{CK}_{\text{MMD}}$  is mainly contributed by the retiming DFF.

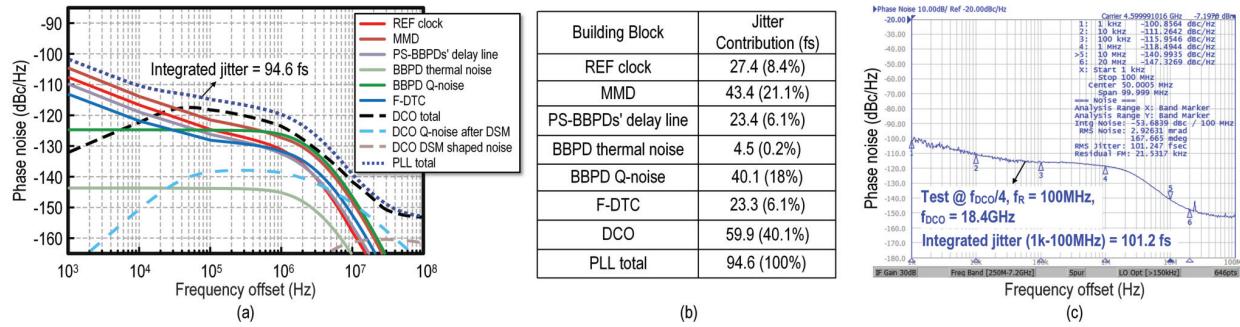


Fig. 12. (a) Simulated PLL output PN based on the discrete time-variant noise model. (b) Corresponding jitter breakdown table. (c) Measured PN profile at the divide-by-4 output, where  $f_{CKV} = 46 \times 100\text{M} = 4.6 \text{ GHz}$  and  $f_{DCO} = 18.4 \text{ GHz}$ .

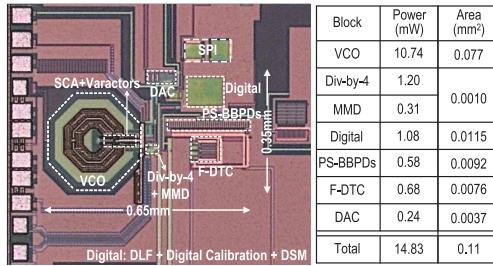


Fig. 13. Chip micrograph and breakdown table of power and area.

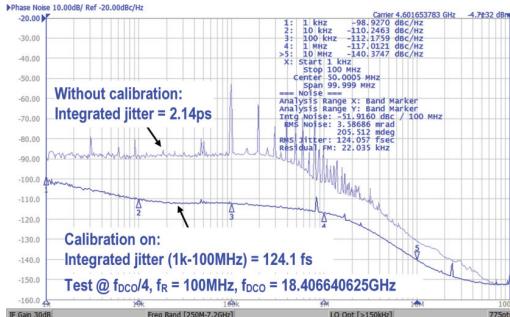


Fig. 14. Measured PN profile at a fractional channel ( $\text{FCW}_F = 2^{-6} + 2^{-10}$ ).

PS-BBPDs are not the dominant jitter contributors, in integer-*N* mode where  $\text{DCW}_C = 13$  and only half of the PS-BBPDs' delay chain is used, the PLL output jitter is reduced by only 2 fs. In addition, a fixed delay is applied to the F-DTC to improve its INL, resulting in its total delay being 1.08 times that of the PS-BBPDs' maximum delay. As shown in Fig. 13, the F-DTC consumes 1.17 times the power of the PS-BBPDs; thus, their jitter contributions are nearly identical. Fig. 12(c) presents the measured PN profile at 4.6 GHz (divide-by-4 output), where  $f_{DCO} = 18.4 \text{ GHz}$ . The integrated jitter is 101.2 fs, which is slightly larger than the predicted value.

## VI. EXPERIMENTAL RESULTS

The chip photograph of this work is shown in Fig. 13. Fabricated in a 28-nm CMOS technology, the fractional-*N* DPLL occupies a core area of  $0.11 \text{ mm}^2$ . The power breakdown for each block is also shown in Fig. 13. The entire PLL consumes 14.8 mW. The DCO exploiting an inverse-class-F topology [45] dissipates 10.74 mW.

The DPLL uses a 100-MHz REF clock and is measured at the divide-by-4 output. Fig. 14 shows the measured PN profile

at a fractional channel of  $f_{DCO} \approx 18.4066 \text{ GHz}$  ( $\text{FCW}_F = 2^{-6} + 2^{-10}$ ). Without nonlinearity calibration, the measured rms jitter is 2.14 ps, which is integrated from 1 kHz to 100 MHz and including all spurs, with an in-band PN of  $\sim -88 \text{ dBc/Hz}$ . After calibration, the rms jitter is notably reduced to 124.1 fs with an in-band PN of  $\sim -115 \text{ dBc/Hz}$ . The DPLL achieves  $\text{FoM}_J$  and  $\text{FoM}_N^{10}$  of  $-246.4$  and  $-269.1 \text{ dB}$ , respectively.

To demonstrate the effectiveness of the proposed calibration method in suppressing fractional spurs, the PLL output spectrum is measured at a near-integer channel close to 18.4 GHz ( $\text{FCW}_F = 2^{-13}$ ). Without calibration for PS-BBPDs' nonlinearity and F-DTC's gain, the worst case fractional spur is  $-6.1 \text{ dBc}$  as shown in Fig. 15(a). After calibration, it is significantly improved to  $-56.5 \text{ dBc}$  as demonstrated in Fig. 15(b). In addition, the measured worst case fractional spurs across fractional channels ( $\text{FCW}_F$  varying from  $2^{-1}$  to  $2^{-14}$ ) near 18.4 GHz are shown in Fig. 15(c). The worst case spur levels are all below  $-54.8 \text{ dBc}$ . Behavioral simulations are conducted to analyze the dominant source of fractional spur at a near-integer channel close to 18.4 GHz ( $\text{FCW}_F = 2^{-13}$ ). Here, we assume the PS-BBPDs have  $\sim 1\text{-ps DNL}$  and both PS-BBPDs and F-DTC have  $+30\%$  gain error under the worst case. When the F-DTC has  $\sim 105 \text{ fs}$  (0.27 LSB) INL, the worst case fractional spur is  $-55.3 \text{ dBc}$  after calibration. If using an ideal F-DTC, the worst case fractional spur is  $-61.8 \text{ dBc}$ . This verifies that the fractional spur is mainly contributed by the INL of F-DTC after calibration.

The measured PN profile at the near-integer channel close to 18.4 GHz with  $\text{FCW}_F = 2^{-13}$  is shown in Fig. 16. The integrated jitter is 153.6 fs, corresponding to a  $\text{FoM}_J$  ( $\text{FoM}_N$ ) of  $-244.6 \text{ dB}$  ( $-267.2 \text{ dB}$ ). In addition, Fig. 17 displays the measured reference spur at an integer channel, which is  $-69.9 \text{ dBc}$  at 18.4 GHz.

Fig. 18(a) shows the measured transient response of the DPLL to a negative frequency jump of 1.2 GHz in the DCO. A locking time of  $2.54 \mu\text{s}$  (254 REF cycles) is achieved for the loop settling within  $\pm 260 \text{ kHz}$  band error ( $< 60 \text{ ppm}$  accuracy). During the initial phase of the locking process, the OTW[20:15] for the DCO's SCA is automatically searched by the loop, consuming 73% of the total locking time. The adaptive frequency switching (AFS) technique proposed in [20] enables rapid estimation of the SCA's OTW, reducing the

<sup>10</sup>The  $\text{FoM}_J$  and  $\text{FoM}_N$  are defined in the performance comparison table (Table I).

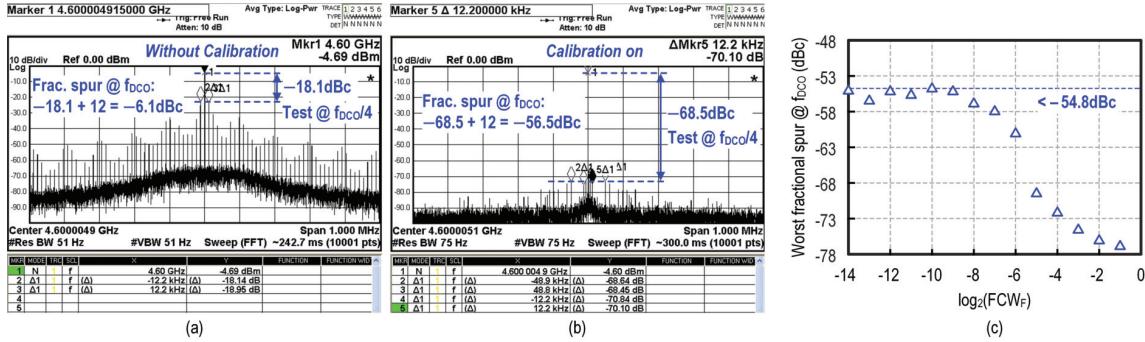


Fig. 15. Measured PLL output spectrum at the near-integer channel close to 18.4 GHz ( $\text{FCW}_F = 2^{-13}$ ) (a) without calibration and (b) after calibration. (c) Measured worst case fractional spurs across  $\text{FCW}_F$  codes (from  $2^{-1}$  to  $2^{-14}$ ) near 18.4 GHz.

TABLE I  
COMPARISON WITH THE STATE-OF-THE-ART FRACTIONAL-N PLLS ABOVE 10 GHz

	Fully-Integrated Fractional-N PLLs							
	This work	JSSC'25 [46]	JSSC'25 [47]	JSSC'24 [48]	JSSC'22 [23]	JSSC'20 [27]	JSSC'18 [2]	TMTT'17 [49]
Architecture	Digital	Digital	Digital	Digital	Digital	Digital	Analog	Digital
Phase Detector	Function-Reused TDC and PS-BBPDs + DTC	Charge-steering sampler + ADC	LC DTC + BBPD	DAC + SSPD	DTC + S-BBPD	DTC + BBPD	PFD + CP	TDC + Counter
Frequency Range (GHz)	18.4 (16.4-19.3)	24 (21-25)	11.25 (11.1-14.8)	14 (12.8-15.0)	13 (12.9-15.1)	13.5 (12.8-15.2)	25.6 (23.3-30.2)	11.2 (9.4-14.8)
REF Freq.(MHz)	100	250	250	100	250	500	491.5	100
RMS Jitter	124.1 <sup>a</sup>   153.6 <sup>b</sup>	167.8	61.7	104	99.6	66.2 <sup>a</sup>	160	740
Integration BW (Hz)	1k-100M	10k-40M	1k-100M	1k-100M	1k-100M	1k-100M	20k-500M	10k-100M
Total Power (mW)	14.83	13.81	34	7.3	10.8	19.8	15.4	18.3
#Frac. Spur (dBc)	-54.8	-50.1	-58.1	-53.6	-48.1	-58.3	-33	-30.7
#REF Spur (dBc)	-69.9	-62.3	-61.0	N/A	-70.2	-77.4	-68.1	-51.7
*Fom <sub>J</sub> (dB)	-246.4 <sup>a</sup>   -244.6 <sup>b</sup>	-244.1	-250.7	-251.0	-249.7	-250.6	-244	-230
**Fom <sub>N</sub> (dB)	-269.1 <sup>a</sup>   -267.2 <sup>b</sup>	-263.9	-267.2	-272.5	-266.9	-264.9	-261.3	-250.5
Core Area (mm <sup>2</sup> )	0.11	0.08	0.21	0.21	0.21	0.17	0.22	0.0625
Technology	28nm CMOS	22nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	28nm FD-SOI	40nm CMOS

<sup>a</sup>Normalized to 18.4GHz   \*Fom<sub>J</sub> =  $10\log_{10}[(\text{Jitter}_{\text{all}}/\text{spurs})/1\text{s}]^2 \cdot (\text{Power}/1\text{mW})$    \*\*Fom<sub>N</sub> = Fom<sub>J</sub> +  $10\log_{10}(1/N)$    <sup>b</sup>FCWF =  $2^{-6} + 2^{-10}$    <sup>c</sup>FCWF =  $2^{-13}$    <sup>d</sup>Integrated without spurs

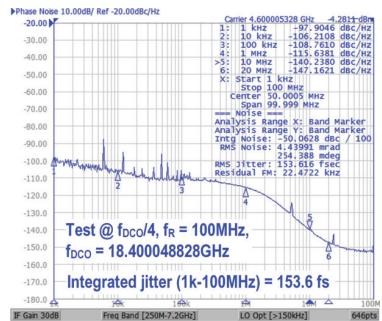


Fig. 16. Measured PN profile at a near-integer channel close to 18.4 GHz ( $\text{FCWF} = 2^{-13}$ ).

locking time in the initial phase. In this work, this technique is not implemented. We rely solely on the proposed digital PFD for fast locking and achieve a locking performance comparable to [20]. If we manually preset the SCA's OTW to approximate the final target using the digital tuning knob, the locking time can be significantly reduced to  $0.88 \mu\text{s}$  (88 REF cycles), as depicted in Fig. 18(b). This result matches well with the predicted locking time when  $\Delta f$  is within the lock-in range ( $n_5$  in Section III).

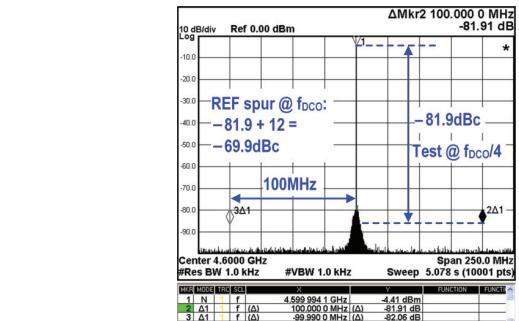


Fig. 17. Measured PLL output spectrum at an integer channel ( $f_{\text{CO}} = 18.4 \text{ GHz}$ ).

Without the OTW preset, the measured PLL locking times for positive and negative frequency jumps of up to 2.4 GHz are shown in Fig. 18(c). The locking time for the 2.4 GHz positive frequency hop is  $4.68 \mu\text{s}$  (468 REF cycles). The OTW searching consumes 374 REF cycles, which is longer than the predicted results ( $n_1 + n_2 + n_4 = 184$  REF cycles) in Section III. This is because the mapping of  $e_2$  in this prototype is slightly different from the implementation we discussed in Section III (lookup table in Fig. 4). Rather than fixed to 13,  $e_2$  is still mapped to  $D_{\text{bin}} - DCW_C$  when the input time error

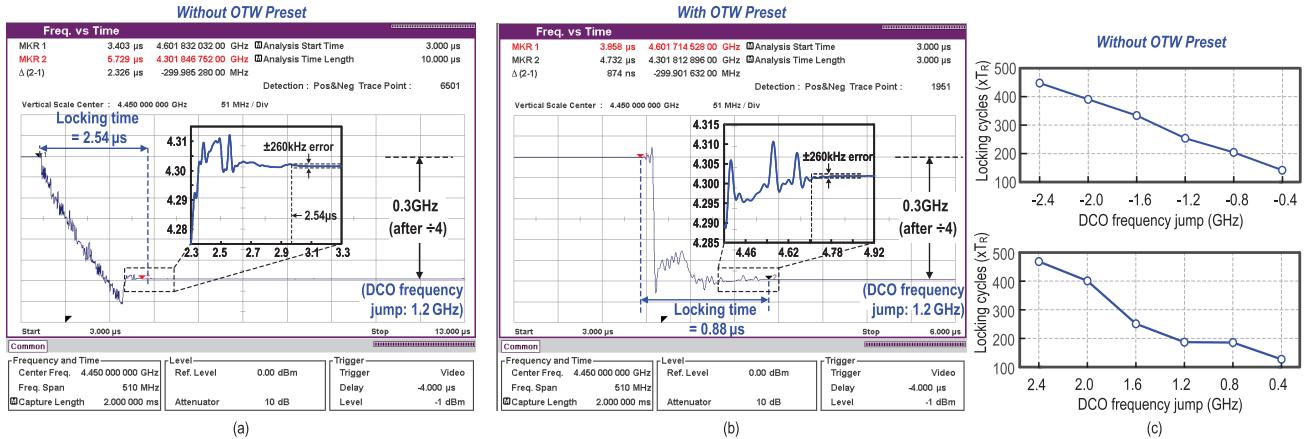


Fig. 18. Measured PLL frequency transient for a 1.2-GHz DCO frequency jump (a) without and (b) with OTW preset. (c) Measured PLL locking time (without OTW preset) for positive and negative frequency jumps up to 2.4 GHz (settling to <60 ppm accuracy).

TABLE II  
COMPARISON WITH THE STATE-OF-THE-ART PLLS WITH FAST-LOCKING FEATURES

	Fast-Locking Fractional- <i>N</i> PLLs					Fast-Locking Integer- <i>N</i> PLLs		
	This work	JSSC'25 [47]	JSSC'20 [27]	JSSC'22 [20]	ISSCC'18 [26]	SSCL'24 [50]	JSSC'19 [51]	TCAS-I'15 [52]
Architecture	Digital	Digital	Digital	Digital	Digital	Analog	Digital	Digital
Locking method	Function-Reused TDC and PS-BBPDs	FLL + Type-II GS	Aux. BBPD + DFER	Aux. BBPDs + AFS + Type-II GS	Aux. BBPDs	DAD + AZ-PEC	Computation Lock	DGAC + Multi-level BBPD
REF Freq.(MHz)	100	250	500	250	52	50	50	19.53125
Frequency Range (GHz)	18.4 (16.4-19.3)	11.25 (11.1-14.8)	13.5 (12.8-15.2)	8.75 (8.5-10)	3.85 (3.7-4.1)	2.5 (1-3)	1.5 (1-2)	1.25 (0.2539-1.367)
Frequency Jump (GHz)	0.4~1.6	0.4~2.4	0.25~3.5	1	0.25~1.5	0.364	+1.5	-1.5
Locking Time (μs)	< 3.34	< 4.68	< 0.55	18.55	< 1.56	115	0.52	0.2
Locking Cycles	< 334	< 468	< 130	9275	< 390	5980	26	10
Setting Accuracy (ppm)	< 60	80	70	< 80	90	N/A	N/A	N/A
Total Power (mW)	14.83	34	19.8	20	5.28	12	10.8	35
Core Area (mm <sup>2</sup> )	0.11	0.21	0.17	0.23	0.61	0.147	0.044	0.7735
Technology	28nm CMOS	28nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	0.18μm CMOS

exceeds the TDC's linear range. Thus,  $e_2$  becomes dependent on variations of  $DCW_C$ , leading to a nonmonotonic locking transient during OTW searching and prolonging the time required to reduce  $\Delta f$  to within the lock-in range. However, once  $\Delta f$  enters the lock-in range, the remaining frequency and phase error is corrected within 0.94  $\mu$ s (94 REF cycles).

The performance of the proposed DPLL is compared with the state-of-the-art fractional-*N* PLLs in Table I [2], [23], [27], [46], [47], [48], [49]. Our design achieves a best-in-class fractional spur among PLLs [48], [49] using a reference clock of 100 MHz and below. Although the digital PLL in [48] using a subsampling PD achieves a higher FoM<sub>J</sub>, our design features a smaller area and a faster locking time. Table II compares the locking performance of this work with prior fast-locking PLLs [20], [26], [27], [47], [50], [51], [52]. Among these works, integer-*N* PLLs generally achieve fast frequency settling within fewer REF cycles than fractional-*N* PLLs. This work achieves a short locking time comparable to other fast-locking fractional-*N* PLLs. Although [47] demonstrates a faster locking speed, its synchronized counter-based FLL architecture results in significantly higher power consumption.

## VII. CONCLUSION

This work presents a fractional-*N* DPLL with a function-reused TDC and PS-BBPDs. It achieves a 153.6-fs rms jitter at a near-integer channel close to 18.4 GHz. The measured worst case fractional spurs at near-integer channels are below -54.8 dBc. For a frequency hop of  $\pm 2.4$  GHz, the DPLL settles to the target frequency with an accuracy of <60 ppm within 468 REF cycles (4.68  $\mu$ s). Compared with other state-of-the-art designs, this work provides a phase and frequency detection structure for the DPLL to achieve low jitter, low fractional spur, and fast locking simultaneously while maintaining low circuit complexity.

## REFERENCES

- [1] C.-W. Yao et al., "A 14-nm 0.14-psrms fractional-*N* digital PLL with a 0.2-ps resolution ADC-assisted coarse/fine-conversion chopping TDC and TDC nonlinearity calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3446–3457, Dec. 2017.
- [2] S. Ek et al., "A 28-nm FD-SOI 115-fs jitter PLL-based LO system for 24–30-GHz sliding-IF 5G transceivers," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1988–2000, Jul. 2018.

- [3] P. T. Renukaswamy et al., "4.1 a 16GHz, 41 kHz<sub>rms</sub> frequency error, background-calibrated, duty-cycled FMCW charge-pump PLL," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 74–76.
- [4] H. Li, T. Xu, X. Meng, J. Yin, R. P. Martins, and P.-I. Mak, "10.9 a 23.2-to-26GHz sub-sampling PLL achieving 48.3fsrms jitter, -253.5dB FoMI, and 0.55μs locking time based on a function-reused VCO-buffer and a type-I FLL with rapid phase alignment," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 204–206.
- [5] R. B. Staszewski et al., "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.
- [6] M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, "A wideband 3.6 GHz digital ΔΣ fractional-N PLL with phase interpolation divider and digital spur cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 627–638, Mar. 2011.
- [7] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise wide-BW 3.6-GHz digital ΔΣ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, 2008.
- [8] H. Li, T. Xu, X. Meng, J. Yin, R. P. Martins, and P.-I. Mak, "A 23.2-to-26-GHz low-jitter fast-locking sub-sampling PLL based on a function-reused VCO-buffer and a type-I FLL with rapid phase alignment," *IEEE J. Solid-State Circuits*, vol. 59, no. 12, pp. 3952–3965, Dec. 2024.
- [9] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.
- [10] H. Chung, M. Hyun, and J. Kim, "A 360-fs-time-resolution 7-bit stochastic time-to-digital converter with linearity calibration using dual time offset arbiters in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 56, no. 3, pp. 940–949, Mar. 2021.
- [11] K. Kim, W. Yu, and S. Cho, "A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, Apr. 2014.
- [12] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators—Analysis, design, and measurement techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.
- [13] M. Lee, M. E. Heidari, and A. A. Abidi, "A low-noise wideband digital phase-locked loop based on a coarse–fine time-to-digital converter with subpicosecond resolution," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2808–2816, Oct. 2009.
- [14] S.-K. Lee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim, "A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2874–2881, Dec. 2010.
- [15] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, Apr. 2015.
- [16] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse–fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.
- [17] A. Samarah and A. C. Carusone, "A digital phase-locked loop with calibrated coarse and stochastic fine TDC," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1829–1841, Aug. 2013.
- [18] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs<sub>rms</sub> integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.
- [19] F. Buccolieri et al., "A 72-fs-total-integrated-jitter two-core fractional-N digital PLL with digital period averaging calibration on frequency quadrupler and true-in-phase combiner," *IEEE J. Solid-State Circuits*, vol. 58, no. 3, pp. 634–646, Mar. 2023.
- [20] S. M. Dartizio et al., "A fractional-N bang-bang PLL based on type-II gear shifting and adaptive frequency switching achieving 68.6 fs-rms-total-integrated-jitter and 1.56 μs-locking-time," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3538–3551, Dec. 2022.
- [21] F. Tesolin et al., "A novel LO phase-shifting system based on digital bang-bang PLLs with background phase-offset correction for integrated phased arrays," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2466–2477, Sep. 2023.
- [22] S. M. Dartizio et al., "A low-spur and low-jitter fractional-N digital PLL based on an inverse-constant-slope DTC and FCW subtractive dithering," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3320–3337, Dec. 2023.
- [23] S. M. Dartizio et al., "A 12.9-to-15.1-GHz digital PLL based on a bang-bang phase detector with adaptively optimized noise shaping," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1723–1735, Jun. 2022.
- [24] G. A. Leonov, N. V. Kuznetsov, M. V. Yuldashev, and R. V. Yuldashev, "Hold-in, pull-in, and lock-in ranges of PLL circuits: Rigorous mathematical definitions and limitations of classical theory," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2454–2464, Oct. 2015.
- [25] Y. Lim, J. Kim, Y. Jo, J. Bang, and J. Choi, "A wide-lock-in-range and low-jitter 12–14.5 GHz SSPLL using a low-power frequency-disturbance-detecting and correcting loop," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 480–491, Feb. 2022.
- [26] L. Bertulessi, L. Grimaldi, D. Cherniak, C. Samori, and S. Levantino, "A low-phase-noise digital bang-bang PLL with fast lock over a wide lock range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 252–254.
- [27] A. Santiccioli et al., "A 66-fs-rms jitter 12.8-to-15.2-GHz fractional-N bang-bang PLL with digital frequency-error recovery for fast locking," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3349–3361, Dec. 2020.
- [28] N. Markulic, K. Raczkowski, P. Wambacq, and J. Crainckx, "A 10-bit, 550-fs step digital-to-time converter in 28nm CMOS," in *Proc. ESSCIRC - 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 79–82.
- [29] W. Wu et al., "A 28-nm 75-fsrms analog fractional-N sampling PLL with a highly linear DTC incorporating background DTC gain calibration and reference clock duty cycle correction," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1254–1265, May 2019.
- [30] M. Rossoni et al., "A low-jitter fractional-N digital PLL adopting a reverse-concavity variable-slope DTC," *IEEE J. Solid-State Circuits*, vol. 60, no. 6, pp. 2122–2133, Jun. 2025.
- [31] B. Liu et al., "A fully synthesizable fractional-N MDLL with zero-order interpolation-based DTC nonlinearity calibration and two-step hybrid phase offset calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 2, pp. 603–616, Feb. 2021.
- [32] V. K. Chillara et al., "9.8 an 860μW 2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth smart and ZigBee) applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 172–173.
- [33] A. Santiccioli, M. Mercandelli, A. L. Lacaita, C. Samori, and S. Levantino, "A 1.6-to-3.0-GHz fractional-N MDLL with a digital-to-time converter range-reduction technique achieving 397-fs jitter at 2.5-mW power," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3149–3160, Nov. 2019.
- [34] P. Chen, J. Yin, F. Zhang, P.-I. Mak, R. P. Martins, and R. B. Staszewski, "Mismatch analysis of DTCs with an improved BIST-TDC in 28-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 196–206, Jan. 2022.
- [35] S.-K. Lee, S.-J. Park, Y. Suh, H.-J. Park, and J.-Y. Sim, "A 1.3μW 0.6 V 8.7-ENOB successive approximation ADC in a 0.18μm CMOS," in *Proc. Symp. VLSI Circuits*, May 2009, pp. 242–243.
- [36] Y.-S. Kim, S.-K. Lee, H.-J. Park, and J.-Y. Sim, "A 110 MHz to 1.4 GHz locking 40-phase all-digital DLL," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 435–444, Feb. 2011.
- [37] B. Razavi, "The StrongARM latch [a circuit for all seasons]," *IEEE Solid State Circuits Mag.*, vol. 7, no. 2, pp. 12–17, Spring 2015.
- [38] N. Da Dalt and A. Sheikholeslami, *Understanding Jitter and Phase Noise: A Circuits and Systems Perspective*. Cambridge, U.K.: Cambridge Univ. Press, 2018.
- [39] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.
- [40] C. Hwang, H. Park, Y. Lee, T. Seong, and J. Choi, "A low-Jitter and lowfractional-spur ring-DCO-based fractional-N digital PLL using a DTC's second-/third-order nonlinearity cancellation and a probability-densityshaping ΔΣM," *IEEE J. Solid-State Circuits*, vol. 57, no. 9, pp. 2841–2855, Sep. 2022.
- [41] L. Avallone, M. Mercandelli, A. Santiccioli, M. P. Kennedy, S. Levantino, and C. Samori, "A comprehensive phase noise analysis of bang-bang digital PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 7, pp. 2775–2786, Jul. 2021.
- [42] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallsson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000.
- [43] L. Romano, S. Levantino, S. Pellerano, C. Samori, and A. Lacaita, "Low jitter design of a 0.35μm-CMOS frequency divider operating up to 3GHz," in *Proc. 28th Eur. Solid-State Circuits Conf.*, Jun. 2002, pp. 611–614.

- [44] Y. Zhao, M. Forghani, and B. Razavi, "A 20-GHz PLL with 20.9-fs random jitter," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1597–1609, Jun. 2023.
- [45] C. C. Lim, H. Ramiah, J. Yin, P.-I. Mak, and R. P. Martins, "An inverse-class-F CMOS oscillator with intrinsic-high-Q first harmonic and second harmonic resonances," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3528–3539, Dec. 2018.
- [46] W. Tao, Y. Yang, W. Chen, R. B. Staszewski, and Y. Hu, "A charge-domain fractional-N ADPLL based on charge-steering sampling," *IEEE J. Solid-State Circuits*, vol. 60, no. 7, pp. 1–13, Jul. 2025.
- [47] H. Liu, W. Deng, H. Jia, Z. Wang, and B. Chi, "An ultra-low-jitter fast-hopping fractional-N PLL with LC DTC and hybrid-proportional paths," *IEEE J. Solid-State Circuits*, vol. 60, no. 3, pp. 785–798, Mar. 2025.
- [48] J. Kim, Y. Jo, H. Park, T. Seong, Y. Lim, and J. Choi, "A 12.8–15.0-GHz low-jitter fractional-N subsampling PLL using a voltage-domain quantization-error cancellation," *IEEE J. Solid-State Circuits*, vol. 59, no. 2, pp. 424–434, Feb. 2024.
- [49] A. Ximenes, G. Vlachogiannakis, and R. B. Staszewski, "An ultra-compact 9.4–14.8-GHz transformer-based fractional-N all-digital PLL in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4241–4254, Nov. 2017.
- [50] C.-Y. Yang, H.-C. Hsu, P.-H. Wu, and S. Palermo, "A 1–3 GHz fast-locking frequency synthesizer based on a combination of PLL and MDLL with auto-zero phase-error compensation," *IEEE Solid-State Circuits Lett.*, vol. 7, pp. 315–318, 2024.
- [51] F. U. Rahman, G. Taylor, and V. Sathe, "A 1–2 GHz computational-locking ADPLL with sub-20-cycle locktime across PVT variation," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2487–2500, Sep. 2019.
- [52] J.-M. Lin and C.-Y. Yang, "A fast-locking all-digital phase-locked loop with dynamic loop bandwidth adjustment," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2411–2422, Oct. 2015.



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