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Time-to-digital converters—A comprehensive review

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Summary

This work presents a comprehensive literature review on different topologies of time-to-digital converters (TDCs). A brief history, applications, classification, characterization, and working principle of each TDC are mentioned. A survey of both Field Programmable Gate Array (FPGA) and Application-Specific Integrated Circuit (ASIC) architectures is covered. The trade-off with respect to applications, pros, and cons of different architectures and future scope of TDC as an alternative data converter is also explored.

KEYWORDS

counter TDC, delay line, flash TDC, GRO, multiphase clock, pipeline TDC, pulse shrinking, SAR TDC, time counter, time interval measurement, time-to-digital converter, Vernier delay line, Vernier ring

1 | INTRODUCTION

Precise measurement of *time elapsed between two events* or *time pulse* is an age-old requirement of many science and engineering applications. Time-to-digital converter (TDC) is the one that converts incoming *time pulse* to its digital equivalent. Unknowingly, TDCs have been a part of electronic engineer's life in the form of Counters, Capture modules in microcontrollers. TDC is also known with different names, namely, time counter, time interval measurement, stop watch for time, time quantization, time interval meter (TIM), and time digitizer. Figure 1 shows a general principle of TDC. For simplicity, it can be compared with analog-to-digital converter (ADC) as presented in Table 1. Time mode signal processing allows designers to make fully digital architectures. Advantages of fully digital integrated circuits (ICs) compared to the mixed-signal Integrated Circuits are with respect to parameters like compactness, silicon area, power, robustness against noise, and coupling.

TDC has been deployed as a key component in some of the applications, namely, ADPLL,[1] ADDLL,[2] clock and data recovery (CDR) circuit,[3] time-over-threshold (TOT) positron emission tomography (PET),[4] jitter measurement,[5] time-of-flight (TOF) laser radar,[6] TOF PET scanner,[7] silicon photomultiplier SiPM PET,[8] Light Detection And Ranging (LiDAR),[9] digital storage oscilloscope,[10] fluorescence–lifetime imaging microscopy (FLIM),[11] 3-D imaging,[12] Raman spectroscopy,[13] on-chip temperature sensor [14,15], time domain ADCs,[16] DC–DC converter,[17] and radio frequency identification (RFID) tag sensor.[18] Earlier, TDC applications limited to high energy physics experiments and later found in ADPLL (all digital phase-locked loop) as a phase detector. Afterward, scientific community reinvented TDCs with tremendous possibilities. This is already evident as the steep increase in the number of applications.

A study on TDCs[19] describes the motivation from the *amplitude/voltage* domain to the *time* domain. This resource also presents the fundamentals of six major TDCs along with mathematics, pros, and cons of each topology. One more study on TDC[20] expands the work of Henzler[19] by adding four new TDC topologies. The present work tries to identify the missing link between all TDCs by (1) exploring remaining architectures, (2) broad classification to fit all topologies, and (3) identifying the similarities and evolution of working principles.

Similar to ADC, there are some parameters to be considered for TDC characterization. Resolution is one of the main parameters, which indicate smallest *time* pulse that TDC can quantize. Measurement range, nonlinearities like INL

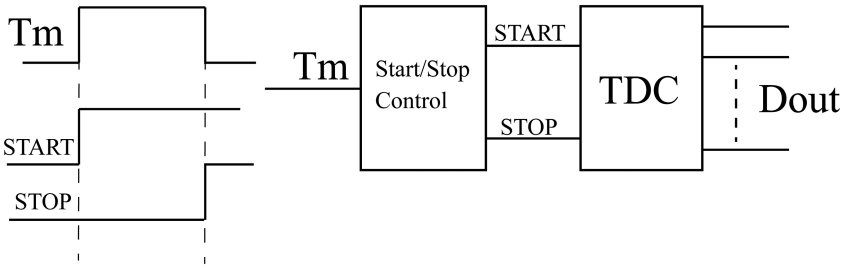

FIGURE 1 Principle block diagram of time-to-digital converter

TABLE 1 Comparison between ADC and TDC

Parameter	Amplitude domain (ADC)	Time mode (TDC)
Input	Voltage or current	Time pulse or time difference between two inputs
Conversion time	Independent of input amplitude	Dependent on the input duration (most of the architectures)
Input integration and sample-hold	Possible and easy	Difficult and complex
Resolution	milli to micro volts	Pico to femto seconds
Technology scaling	Affects nonlinearities at large	Minimal effect on nonlinearities

(integral nonlinearity) and DNL (differential nonlinearity), conversion speed, PVT (process, voltage, and temperature) effects, and dead time are some other parameters to be noted. There are few other parameters that correspond to specific applications.

Classification covering all TDCs has been made in Section 2. Section 3 describes Counter as TDCs. Section 4 explains about indirect measurement, architecture, pros, and cons. Remaining sections discuss about different architectures for time measurement. A comparison of different architectures has been tabulated at last.

This review presents the evolution of different TDC architectures. The survey is useful for beginners and those who are searching for suitable TDC architecture for their application. It is a motivating guide for those who are already good at ADC (analog domain) and trying to migrate toward TDC (time domain). Almost 20 major architectures are illustrated with diagrams.

2 | CLASSIFICATION

One of the literatures[21] tried to classify TDCs, broadly into three categories, namely, course, interpolation, and time stretching techniques. In Yuan,[22] TDCs are classified as sampling and noise shaping TDCs. If the conversion principle uses a reference clock or delay line, then techniques are classified as sampling techniques. Most of the TDCs fit into this category. These sampling TDCs are further divided into single shot and averaging TDCs, whereas noise shaping suppresses quantization noise using different techniques. However, reference Wang et al.[23] classified TDCs as direct and indirect measurement techniques. In the direct method, time is measured with a relative reference clock or delay element, wherein indirect method time is quantized to its equivalent voltage and then digitized using ADC. In a broad sense, direct method is called as *Time* mode technique and indirect methods are can be classified as *amplitude* mode methods. Direct methods can be classified into further categories based on operating principles. Figure 2 shows a detailed view of the classification of TDCs. Further sections describe fundamentals, working principle, and advantages of each architecture. Figure 2 also shows the TDC design hexagon. Six important design parameters are considered. The trade-off among the parameters is also presented. To keep the diagram simple, cross connections are not shown in the hexagon. For example, CMOS technology affects the silicon area, which most of the electronics engineers know.

3 | COUNTER—THE FIRST TDC

Counter is the simplest and most reliable way of time measurement. The conceptual diagram of counter as TDC is as depicted in Figure 3. The resolution depends on the frequency of the clock input. For example, Counter is driven by 1-MHz clock; hence, the resolution will be 1 μs. The range is decided by the number of bits of the counter. One can

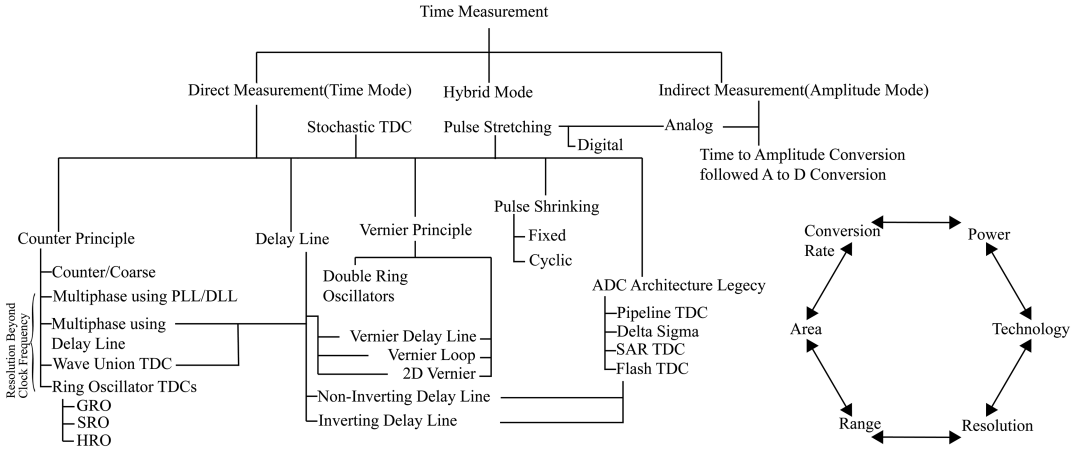

FIGURE 2 Classification of TDCs and design hexagon

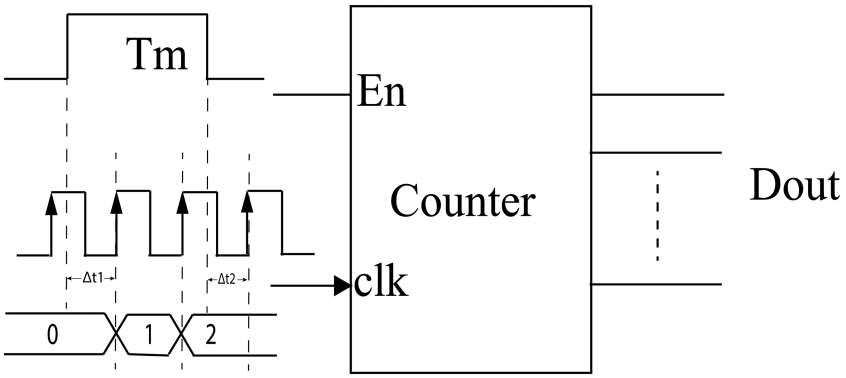

FIGURE 3 Counter as TDC

double the measurement range, just by increasing one flipflop in the counter. However, it is difficult to enhance the resolution because of the bandwidth limitations of the circuit components and/or printed circuit board (PCB). However, the clock can be easily multiplied using of phase-locked loop (PLL) or DLL (delay-locked loop) inside the IC. One should notice that enhancing the resolution will reduce the measurement range. In other words, for the same range, the enhanced resolution requires more hardware.

The advantage of Counter remains in its simplicity and reliability. Hence, most of the modern multistage conversion techniques employ Counter TDC at the coarse stage. The Counter has its inherent limitation toward resolution. For example, Counter clock frequency should not exceed 500 MHz in a commercial FPGA. Similarly, there will be an upper frequency limit with ASICs, irrespective of technology. The second drawback is the error associated with measurement. Most of the time the input time pulse (*Tm* in Figure 3) will be asynchronous. Hence, probably ending up with measurement error. Equation (1) represents possible errors in the measurement. This error will be nearly equal (but less than) the resolution of the Counter TDC. This error is modeled and expressed mathematically in Liu and Wang.[39] This error can be minimized by sampling the same input multiple times and averaging the outputs.

$$T_m = D_{out} * T_{clk} + \Delta t1 - \Delta t2 \tag{1}$$

4 | INDIRECT MEASUREMENT–AMPLITUDE DOMAIN: THE FIRST GENERATION

Different applications and their requirements forced designers to move away from classical Counter TDC. Sub-nanosecond and sub-picosecond resolution became a common specification of many applications. Hence, designers

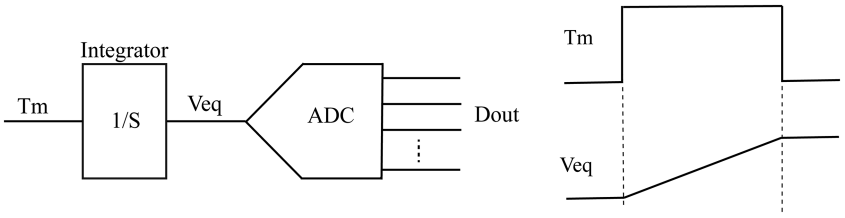

FIGURE 4 Principle diagram of indirect measurement

were forced to roll back into the voltage domain by the 1970s. By the time, many reliable ADC architectures caught the attention of the designers. The working principle of indirect measurement is nothing but *time* to voltage to digital converter. This is as depicted in Figure 4.

4.1 | Time-to-voltage converter

The first stage in the indirect measurement would be time-to-voltage converter (TVC) also known as time-to-amplitude converter (TAC). Many works implemented TVC with their topologies keeping charge pumps in common.[24–27] TVC output will be fed to ADC for final conversion.

4.2 | Integrating ADC as TDC

Well-known single-slope and dual-slope integrating ADC with slight modifications can be used as integrating TDC. One such attempt is presented in recent work[28] for low-resolution applications. The principle diagram and theoretical waveforms of the same are depicted in Figure 5. The input *Vin* for dual-slope ADC is generated by charge pump-based TAC. Similar architecture implemented in Kim et al.[29] and reached a fine resolution of 8.87 ps. Using successive approximation register (SAR) ADC for indirect measurement,[30] nearly 1-ps resolution is reported.

4.3 | Pulse stretching/time amplification

One of the main limitations of indirect measurement and Counter TDC is the resolution. Resolution can be enhanced by stretching the *time* pulse followed by conversion. There are two ways to apply this technique: first, pulse stretching followed by ADC and second, time residue stretching followed by Counter/TDC. In the latter method, time residues $\Delta t1$ and $\Delta t2$ expressed in Equation (1) are very small. One needs to amplify or stretch these tiny pulses to measurable ones. Pulse stretching is an essential block in interpolation or multistage conversion. Let's consider different time-stretching techniques one by one.

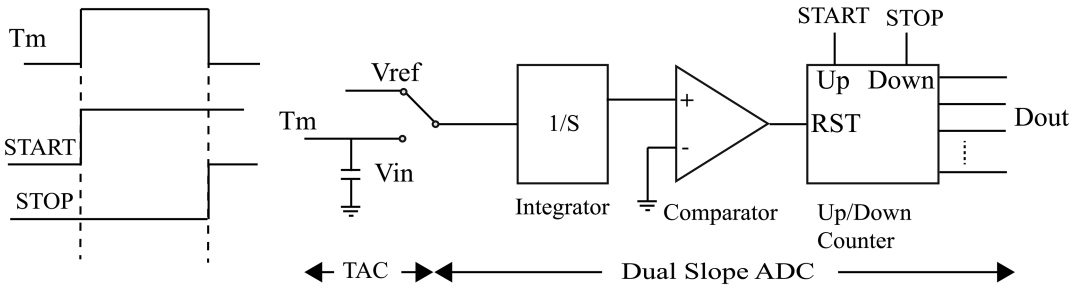

FIGURE 5 Conceptual diagram of dual slope integrating TDC

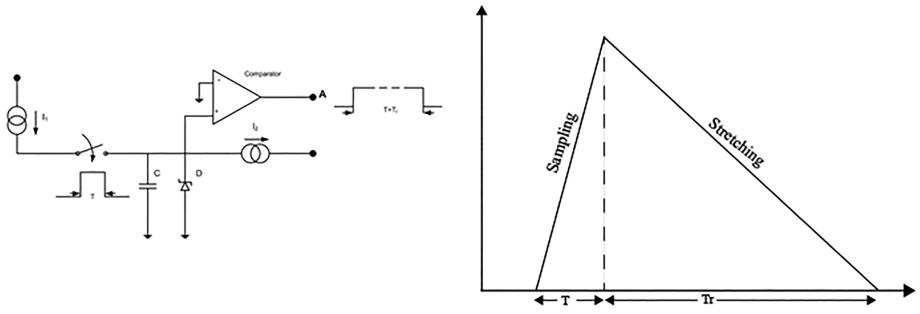

FIGURE 6 Single slope pulse stretching circuit and timing diagrams

4.3.1 | Single-slope pulse stretching

The method involves charging capacitor C with constant current(*I2-I1*) during START, and discharging slowly with small current(*I2*). In other words, with $I2 \ll I1$, the capacitor charges quickly(T) and discharges slowly (Tr). The overall output of the circuit is stretched pulse ($T + Tr$), which is proportional to T. The same concept is expressed as shown in Figure 6. Though there are two slopes in the timing diagram, stretching happens while discharging. Hence, the name can be declared as single-slope stretching. The stretched pulse is then converted using Counter TDC in Park and Park.[31] One can go for any other TDC.

4.3.2 | Dual-slope pulse stretching

Pulse stretching can also be done using a dual-slope method. This is done in the same way as the single slope, except stretching is done on both *residue* and $\overline{residue}$.[32] Additionally, the discharging path is gated by the clock. This will give complete control of the *stretch factor*. Both currents and capacitors are scaled to get better control.

4.3.3 | Time to amplitude, amplify, and ADC

This technique involves two steps: first, converting time residues $\Delta t1$ and $\Delta t2$ to their equivalent voltage levels using TAC and second, amplifying these voltage levels to a *stretch factor*, followed by ADC.[26,27]

4.3.4 | Other techniques

Most of the pulse stretching methods mentioned in previous sections are charge pump-based techniques. There are other techniques other than capacitor-based techniques. One such technique uses regenerative property of the Set-Reset (SR) latch.[33] One more method uses the DLL closed loop approach.[34,35] The DLL-based technique has added advantage of better PVT insensitivity. Nakura et al.[36] used two closed loop delay lines along with DLL for time stretching.

4.4 | Limitations of indirect measurement

TVC and ADC have their own limitations. The first limitation is inherent to its topology, that is, dual conversion. TAC followed by ADC will take a long time compared to direct measurement. The dead time between each conversion cannot be ignored. Quantization error in the first stage (TVC) may worsen the second-stage performance. Moreover, these circuits are power hungry.[19] The resolution of TDC depends on the resolution of the ADC. Most of the time, it is a trade-off between area and ADC resolution. In spite of that, TDC resolution requirement went high and reached sub-picoseconds, which is a very hard task in indirect measurement and the same explained in detail.

In pulse stretching methods, the linearity of the overall conversion is mainly dependent on the pulse stretcher. The reliability of different time amplifiers is questionable over electronic aging. Another drawback is its latency. The conversion time will also be stretched along with the pulse. The converter may have to wait for the *time* amplifier to finish time amplification. Hence, the resolution of the architecture will be at the cost of latency.

Modern designers trying hard to exclude ADC in their design. Few reasons for the same are explained here. Consider a 10-bit ADC with 2-V reference, which then has to be scaled to 1 V. The resolution or step size of the 2-V reference ADC will be approximately 2 mV, whereas 1-V ADC will have a step size of 1 mV. This will pose difficulties in terms of nonlinearities (INL and DNL). Hence, ADC should be redesigned while scaling. Most on-chip ADCs will have a higher reference voltage compared to the chip operating voltage. Some designers provide separate pins for external reference voltages to suit this situation. Many modern VLSI systems try to avoid the classical mixed-signal approach because of their bad scaling behavior; that is, whether it is area scaling or voltage scaling, a whole redesigning of the system is required. On the other hand, direct measurement will measure *time* rather than voltage. So, irrespective of technology scaling, nonlinearities will be under the designer's control. Most of the early architectures of direct measurement are prototyped on FPGA as they are completely digital architectures. Fully digital circuits are most suitable for scaling.[54]

5 | DIRECT MEASUREMENT TECHNIQUE–TIME DOMAIN: SECOND GENERATION

The advantage of *time* domain data converters can only be explored with direct measurement TDC architectures. The basic principle of any converter is to compare the input with a known reference value or fraction of reference value. For example, flash ADC and SAR ADC have to compare input values with known fractions of reference values. Similarly, fully digital TDCs also take reference of known reference clock or delay element.

6 | DELAY LINE TDC

Delay line TDC is also called as flash TDC, classical delay line TDC, or tapped delay line TDC. The flash TDC architecture is most popular because of its simplicity, low latency, and reliability. Figure 7 shows a general diagram of all digital flash TDC. It is also possible to interchange *clk* and *D* inputs in the diagram. In CMOS implementation, resolution of the TDC is equal to the delay(τ) of the buffer. In FPGA implementation, the delay line can be constructed using a carry chain.[37–40] Length of the delay line can be decided by the required dynamic range. Conversion time of the architecture is proportional to input (*Tm* in Figure 7). However, a major drawback in the delay line TDC is its resolution. The resolution of the architecture depends on the delay of the buffer, thereby depending on VLSI technology. Hence, over the time, as with the evolution of the technology, the same architecture will give better resolution. There are two ways to enhance the resolution of flash TDC in the ASIC platform: first, increasing the aspect ratio (size) of transistors in delay elements, thereby making buffers faster than the standard sized buffer. An increase in the size of the transistor will be

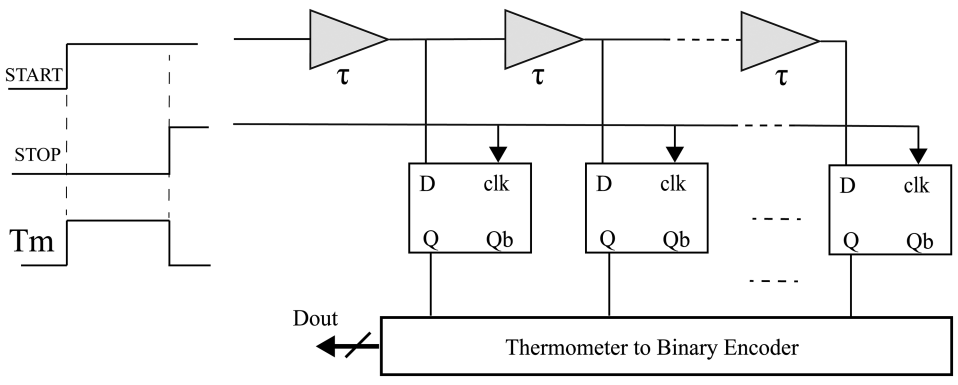

FIGURE 7 Delay line TDC using buffers

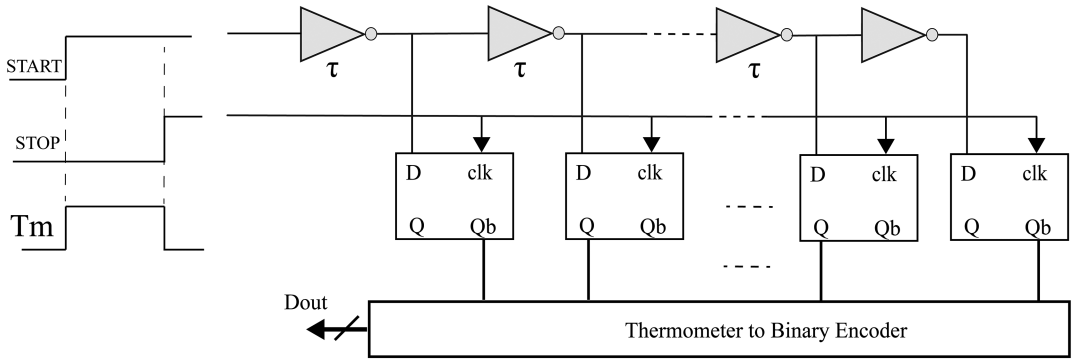

FIGURE 8 Delay line TDC using inverters

at the cost of the silicon area. Second, replace buffer (two cascaded inverters) with inverter. Figure 8 shows a conceptual way of inverter-based delay-line-TDC. For the same delay line length, the architecture doubles the resolution but reduces the dynamic range by half. However, to eliminate its practical difficulties of the architecture pseudo-differential delay line using inverter has been proposed.[41,42] One more serious consequence in the architecture is its complexity in the thermometer-to-binary encoder stage. There is an exponential increase in the complexity of most of the encoders with an increase in the delay line stages. To improve nonlinearities, another modification of the architecture called *merged delay line* TDC has been proposed.[43,44]

7 | VERNIER DELAY LINE TDC

Resolution of the classical delay line TDC is limited by the (delay) cell delay. Vernier delay line TDC was adopted by designers to enhance TDC resolution beyond cell delay.[45,46] Consider a conceptual Vernier delay line TDC as shown in Figure 9. The cell delay of START line is $\tau 1$ and that of STOP line is $\tau 2$, where $\tau 1 > \tau 2$ and the incremental resolution is given by $\tau 1 - \tau 2$. *Tm* is the time pulse to be measured. Looking into the timing diagrams, it is evident that the measurement completes when STOP overtakes the START signal as shown in Figure 10. The STOP signal overtakes the START signal in steps of resolution ($r = \tau 1 - \tau 2$). The event can be easily recognized with the phase detector. The phase detector output indicates end of conversion (EOC). It is also possible to exchange D and *clk* lines, with the reverse encoding scheme. Resolution can be improved by making the difference between $\tau 1$ and $\tau 2$ minimal. One technique to improve the resolution is the fractional difference scheme.[47] Two additional DLLs require to control the delay of two voltage-controlled Vernier delay lines. The biasing voltage of these lines can be adjusted from DLLs. The scheme has an added advantage of PVT insensitivity as DLLs are controlling delay lines. Making the delay line multidimensional will also improve the resolution. A 2-D Vernier TDC approach[48,49] reported 4.8- and 2.2-ps resolutions, respectively. The

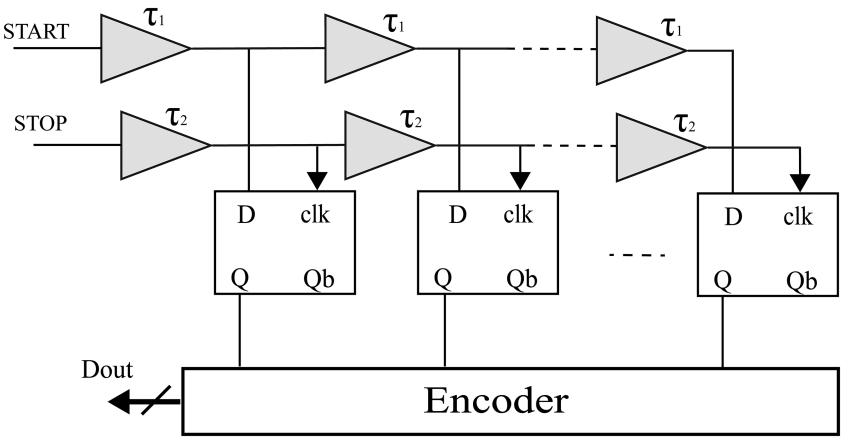

FIGURE 9 Vernier delay line TDC

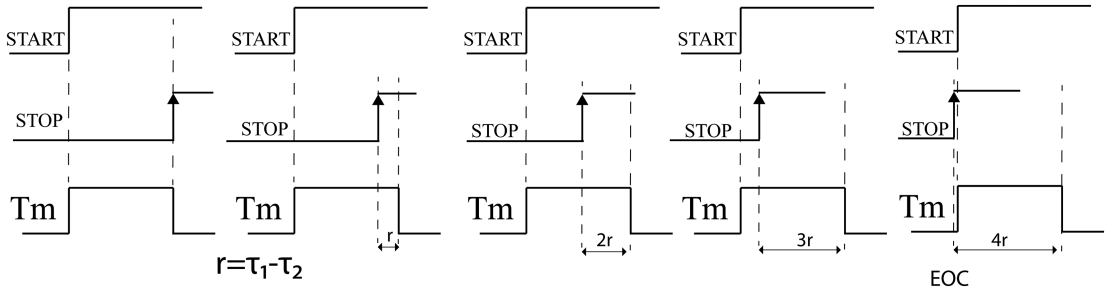

FIGURE 10 Timing diagram of Vernier principle

architecture also reduces the jitter problems associated with one dimensional Vernier delay line but suffers from a large number of comparators required at each meeting point of the delay lines.

For a given measurement range Vernier delay line TDC needs more silicon area for two reasons. First, the number of delay lines and delay elements is doubled with respect to classical delay line TDC. Second, the better the resolution, the longer the delay line, hence the lengthier the conversion time.

8 | REDUCING THE SILICON AREA IN DELAY LINE TDCS

To overcome the area overhead in classical and Vernier TDC, a delay line loop can be formed. Hence, repetitive and effective use of the limited number of delay elements is possible.[50,51] The second option is to use multistage conversion, also known as interpolation, where coarse stage will take care of the measurement range and the fine (delay line) stage will yield a better resolution. In this method, residues from the coarse stage are fed to the fine stage. Normally, counter TDC is used for the coarse stage and the residues, $\Delta t1$ and $\Delta t2$ shown in Figure 3, are converted using the fine stage. Fine stage conversion ensures high resolution. In some references, the second technique is also referred to as the *Nutt* interpolation method. Two-stage architectures are common, but in reference Razmdideh and Saneei,[52] we can observe three-stage conversion.

9 | STOCHASTIC TDC

Most of the TDCs mentioned previously are suffering from random mismatches. Their performance will degrade along with the scaling of VLSI technology. We can remove delay elements (in delay line TDC shown in Figure 7) and deploy arbiters with random mismatches advantageously to improve the resolution. Stochastic TDC employs arbiters or latches with mismatches due to process variation.[53] If any designer wishes, these mismatches or setup times or voltage thresholds can be intentionally obtained by sizing the transistors. If not, the mismatches exhibit inherently due to process variation. These mismatches are random Gaussian distribution and represented using an offset voltage in Figure 11. We have to provide the same input signals to all arbiters, and summing up the arbiter output will provide the precise time difference between two inputs. In other words, the majority number of orbiters decides the TDC resolution; that

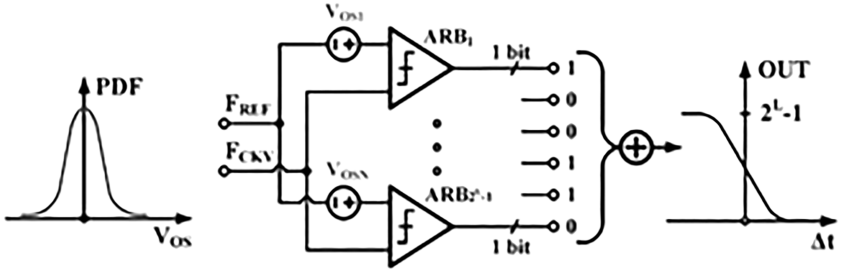

FIGURE 11 Conceptual diagram of stochastic TDC[53]

is, resolution can be enhanced at the cost of area and power. Resolution up to 1 ps obtained using the edge-interchanging technique.[54] The expression for the resolution of Stochastic TDC (STDC) is given by Equation (2). The measurement depends on the mismatches of the arbiters. Hence, the resolution is affected by PVT variations. This intern necessitates a separate calibration block for STDC stability. Since the STDC will not employ delay cell, it can also be called as delay-cell-less TDC (DLTDC). A similar approach is presented in Song et al.[55] Because of its high-resolution STDC used for fine conversion in the coarse–fine approach,[56] STDC operating principle limits its applications. It is very much suitable for ADPLL circuits.

$$T_{LSB} = \frac{\sqrt{2\pi}\sigma_T}{N}, \tag{2}$$

where σT represents the standard deviation of time offsets $TOSi$ ($i - 1, 2, ... N$), N is the number of arbiters used in the STDC.

10 | VERNIER RING OSCILLATOR TDC (CYCLIC VERNIER/NONIUS TDC)

If the delay line has feedback, then it can form a ring oscillator. Further minimizing the number of elements in the loop will make a high-frequency oscillator. Two such controllable oscillators with a difference in their oscillating period can be used to form Vernier ring oscillator TDC.[57,58] Figure 12 shows the arrangement in the topology. Figure 13 shows the timing diagram of the Vernier ring oscillator TDC. The difference in the period of two oscillators decides the incremental resolution of the TDC. Equation (3) depicts the final readout calculations. The fast oscillator is also called as *Nonius* oscillator, hence the architecture name *Nonius* TDC. The architecture easily fits into both CMOS and FPGA platforms. The architecture is more area efficient than Vernier delay line TDC. The *fractional difference* scheme used for Vernier delay line TDC has been adopted here.[59,60] PVT insensitive property of these architectures makes them suitable for many applications. Vernier TDC normally preferred in fine stage interpolation. Vernier TDCs trade latency for resolution and silicon for range. Two-dimensional Vernier ring oscillator technique similar to the 2-D Vernier delay line TDC proposed in the previous studies.[61,62]

$$T_m = Count_{slow} * T_{slow} - Count_{fast} * T_{fast} \tag{3}$$

11 | PULSE SHRINKING TDC

It is evident from the observation of Vernier TDC timing diagrams, STOP signal chasing the START signal at the rate of the resolution. In other words, the space between START and STOP reduces or shrinks every cycle. The same can be

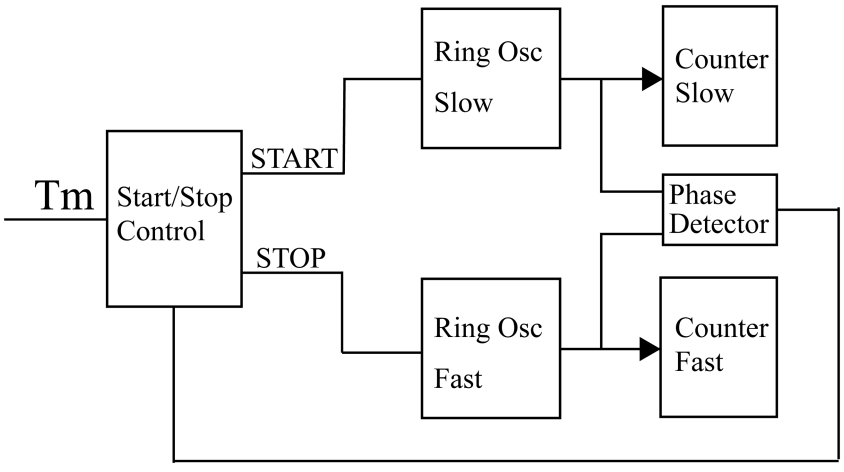

FIGURE 12 Block diagram of Vernier ring oscillator TDC

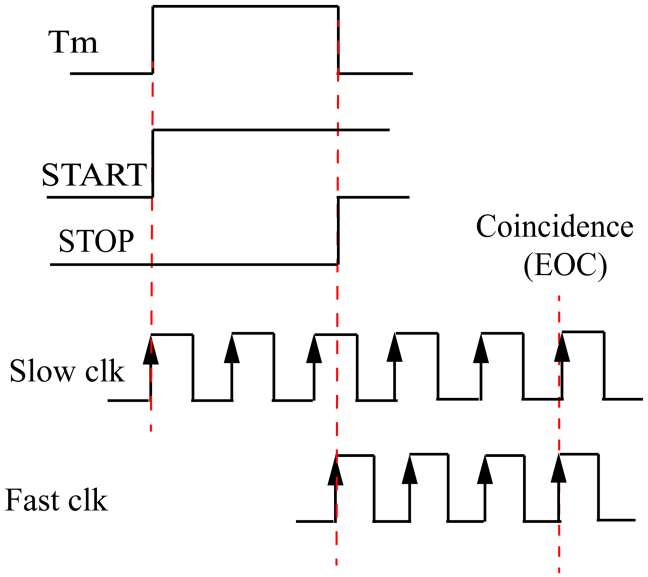

FIGURE 13 Timing diagram of Vernier ring oscillator TDC [Colour figure can be viewed at wileyonlinelibrary.com]

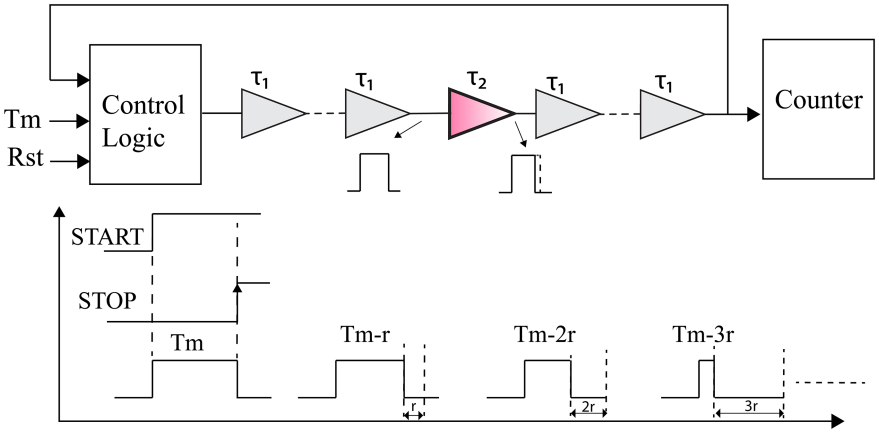

FIGURE 14 Conceptual timing diagram and circuit diagram of pulse shrinking circuit [Colour figure can be viewed at wileyonlinelibrary.com]

observed in Figure 13. In the same way, pulse *Tm*, that is, the time to be measured, can be made to shrink. The technique is commonly known as the pulse shrinking method.[63–66] There are different ways to implement pulse shrinking TDC. Figure 14 depicts the concept of cyclic pulse shrinking. Reducing the pulse normally involves adjusting the transistor size. All buffers in the delay line except one have equal rising and falling timing. Hence, the given input pulse will be preserved when the signal passes through it.

However, there is one delay element, which has unequal rise and fall times, preferably having a quick fall time. The resultant pulse coming out of this buffer will be made to shrink. Since it's a cyclic loop, the shrinking continues till the pulse vanishes. The number of cycles taken to vanish the signal will be proportional to input pulse *Tm*. This is the simplest way of doing time measurement as it includes only a delay line and a counter. Resolution can be as fine as the designer wishes. However, the resolution trades not only area but also the conversion time. The conversion time of this TDC is not suitable for applications like ADPLL. In other words, pulse shrinking TDC suitable for single-shot and very low sampling rate applications.

12 | MULTIPHASE CLOCK COUNTER TDC

As discussed earlier, Counter is a simpler and more reliable TDC. However, the Counter TDC limits its usage only at the coarse level in multistage architecture. The major limitation was quantization errors associated with its conversion.

These errors can be minimized using *multisampling and averaging* technique. Increasing the clock frequency will also minimize the errors: at the cost of dynamic range or area. But frequency cannot be increased beyond the bandwidth of the circuit.

Inherent errors in the Counter TDC can be minimized by sampling at different phases of the clock and accumulating all counter outputs to obtain the final result. This will enhance the resolution as expressed in Equation (4). For example, consider four phases, namely,0°, 90°, 180°, and 270°, used for multiphase sampling as depicted in Figure 16. As a result, the resolution improves by 4 times and quantization error drops by 4 times compared to single-phase sampling.

$$Resolution\ T_{MPTDC} = \frac{T_{Counter}}{Number\ of\ Phases} \tag{4}$$

There are two ways to generate multiple phases of a clock. The first method uses a delay line to generate phase shifts and the later method uses PLL or DLL. For example, phase-shifted clocks, namely, *clk_0, clk_90, clk_180*, and

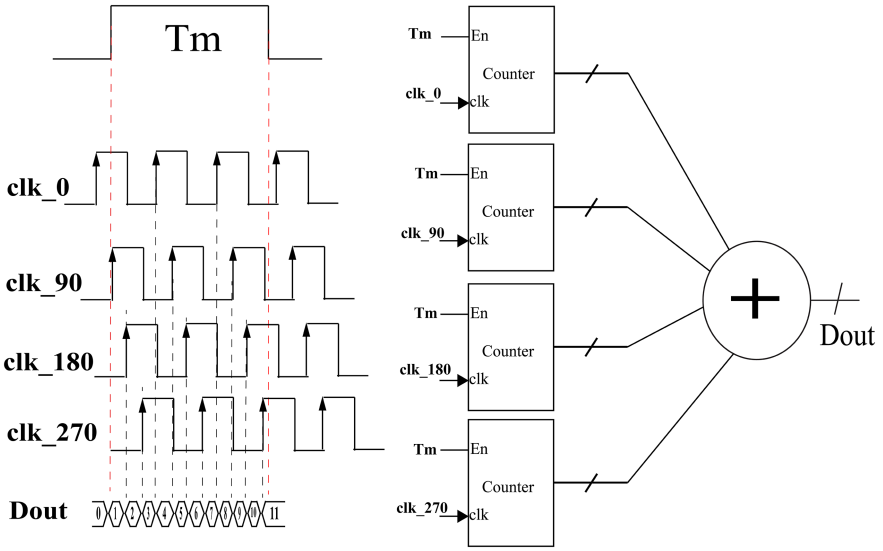

FIGURE 15 Concept of multiphase clock TDC [Colour figure can be viewed at wileyonlinelibrary.com]

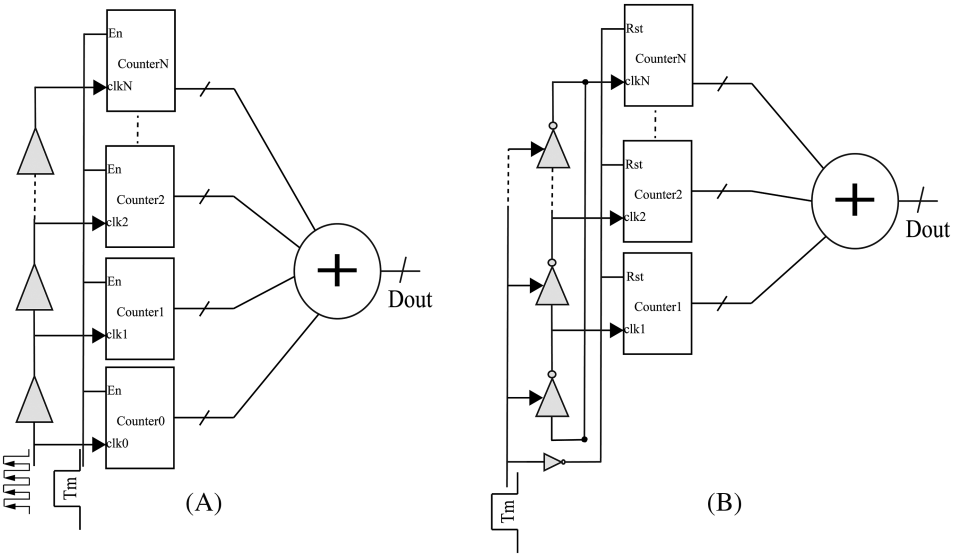

FIGURE 16 (A) MPTDC using delay line and (B) general structure of ring oscillator TDC

clk_270 shown in Figure 15, can be generated by the PLL/DLL. Some of the previous works[67,68] use a delay line-based phase generator for ASIC platform. The conceptual diagram of the delay line phase generator is presented in Figure 16a. However, even for ASIC TDC[69] DLL-based phase generator has been adopted.

Most of the multiphase TDCs use a special encoding technique to avoid counter array. This will save the silicon area. But reliability may be a problem as the number of phases increases. An increase in the number of phases will also increase the area.

In most cases, the resolution of these TDCs is mentioned as root mean square (RMS) resolution. RMS resolution will be better than the mentioned LSB or *single-shot resolution*. Many researchers often express LSB as the worst-case resolution. The improvement in the resolution is due to a greater number of hits or samples in favor of the measurement setup. Hence, the architecture is not suitable for applications, which require fixed resolution. Also, circuits in the topology are very sensitive to placement and routing delays. Hence, require a properly distributed clock network topology.

13 | RING OSCILLATOR TDCS

13.1 | Gated ring oscillator TDC

Consider the multiphase clock generated using the delay line shown in Figure 16a. Instead of connecting an external clock, one can generate a clock using feedback, that is, forming a ring oscillator and tapping every delay element to form multiphase clocks as shown in Figure 16b. However, the overall counts can be increased by making a multipath ring oscillator.[70,71] The operation principle includes noise shaping by gating the oscillator and preserving the phase during the off-state. A similar approach is called interpolative oscillator, which is presented in Gebara et al.[72] Further, having a considerably large number of stages in the ring oscillator will improve noise shaping characteristics as well as resolution. A novel approach called *GRO with gate-switch-based delay cell* presented in Park et al.[73] improves the resolution by a factor of 2. Figure 17 shows the structural difference between the single path and the multipath ring oscillator.

13.2 | Switched ring oscillator TDC

Gated ring oscillator (GRO) TDCs suffers from the following limitation. While maintaining the off-state phase, the gate ring oscillator susceptible to leakage and charge injection increases with scaling. These limitations can be minimized using the switched ring oscillator (SRO).[74–76] SRO TDC switches to slow frequency mode instead of off-state as shown in Figure 18. This will reduce the *gating delay*, leakage, and dead time. The added advantage of SRO TDC is its oversampling capability, which not possible with other TDCs. To have the advantages of both SRO and GRO TDCs; gated switched ring oscillator (GSRO) TDC has been proposed in Yu et al.[77]

13.3 | Harmonic ring oscillator TDC

The purpose of multipath ring oscillators mentioned in earlier sections is to increase the frequency of oscillation to enhance the resolution. The harmonic ring oscillator (HRO) is another effort for the same cause. It is a simple yet effective architecture.[78] HRO is also suitable to store the phase difference between multiple input edges.

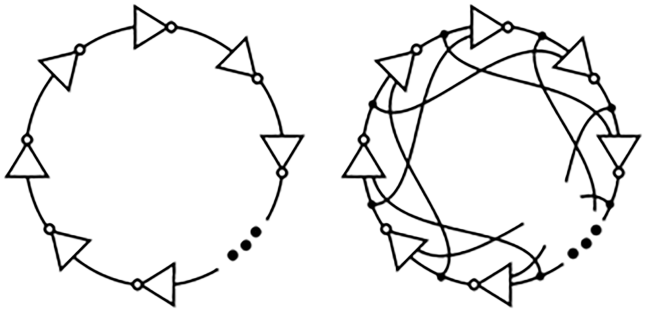

FIGURE 17 (A) Single path ring oscillator and (B) multipath ring oscillator[70]

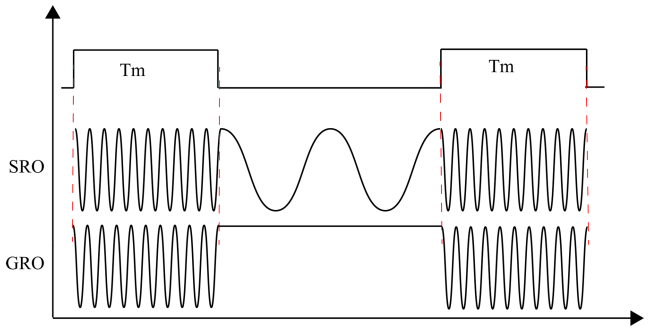

FIGURE 18 Timing diagram of SRO and GRO [Colour figure can be viewed at wileyonlinelibrary.com]

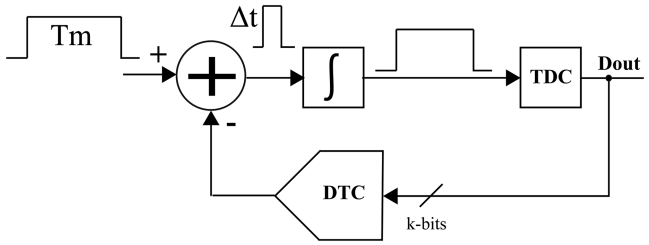

FIGURE 19 Time-mode delta–sigma modulator

14 | DELTA–SIGMA TDC

Along with ring oscillator TDCs, delta–sigma (ΔΣ) TDCs also fall under the noise shaping category. An application like ADPLL requires noise shaping to reduce the quantization noise while frequency synthesis. Delta–sigma modulation is successfully adapted to ADC architecture. But it is difficult to realize in *time* mode due to difficulty in designing a time integrator. So designers switch between time mode (direct measurement)[79,80] and pseudo time mode (indirect measurement).[81,82] Figure 19 shows the ΔΣ modulator with and without TDC quantizer. Voltage controlled oscillator (VCO) can be used as a quantizer instead of ADC as presented in Hsu et al.[83] Further, ΔΣ TDCs can be classified as 1 bit[84,85] and multibit architectures. Most of the TDCs are continuous time ΔΣ TDCs[86] suitable for ADPLL applications. Multi-stAge noise SHaping (MASH)[87,88] is useful for higher order noise shaping with a stable system response.

The advantages of these TDCs are large oversampling ratio, compatibility of technology, does not require precise matches, PVT insensitive, and radiation tolerant. However, these types of TDCs are not suitable for single-shot measurement setups.

15 | WAVE UNION TDC

Both multipath and harmonic ring structures are trying to create more phases (hence more counts) to improve resolution, that is, creating multiple trains of pulse compared to the single path ring structure. Hence, multiphase and multipath techniques discussed in the previous sections are different ways to enhance the resolution beyond the cell delay. On the other hand, one can go for multiple measurements and averaging the results, to improve the resolution and nonlinearity. Upon *hit* (trigger input *Tm*), a train of pulses or *wave union* will be launched into the regular delay line (or carry chain in FPGA) of a delay line TDC, to make multiple measurements. To generate and launch the train of pulse, a separate circuit called *Wave Union Launcher* has been proposed in Wu and Shi.[89] There are two possible wave union launchers, namely, the finite step response (FSR) and infinite step response (ISR)[90,91] launchers. Further improvements in the architecture with temperature correction are made in Pan et al.[92] The ISR type wave union closely resembles the HRO discussed in the previous section. The wave union architecture specifically meant for TDCs on FPGA also suffers from the same drawbacks of multiphase clock TDCs.

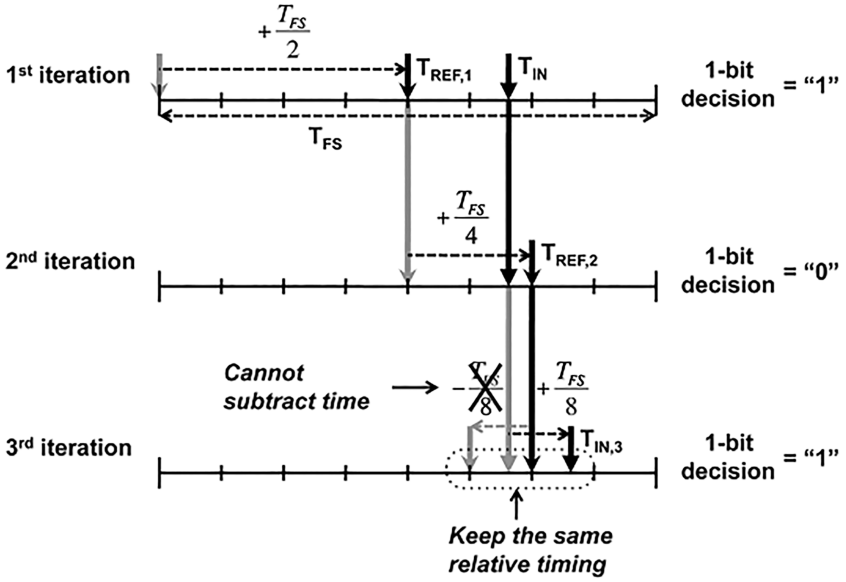

FIGURE 20 Cyclic time domain successive approximation proposed in Mantyniemi et al.[93]

16 | SAR TDC

Unlike SAR, ADC designing SAR TDC is difficult as it is not possible to hold input time/event. A TDC uses the cyclic time domain successive approximation method developed in Mantyniemi and Rahkonen.[93] The concept has been depicted in Figure 20. One more difference between SAR ADC and SAR TDC is its rollback possibility. When the comparison output is false, the subtraction of time is not possible. Instead of rolling back, a new input reference will be created by adding reference time to it.

Be it ADC or TDC, the inherent drawback of the SAR algorithm is its longer conversion time. This will limit the overall sampling rate of the system. Like SAR-ADC requires a digital-to-analog conversion (DAC); TDC also requires digital-to-time conversion (DTC). However, the architecture mentioned in Mantyniemi and Rahkonen[93] requires two DTCs. On the other hand, *decision-select successive approximation*[94] shifts the reference every cycle followed by a decision dependent shift for the input. The working principle of the same is presented in Figure 21. The architecture reduces the conversion time and improves the sampling rate.

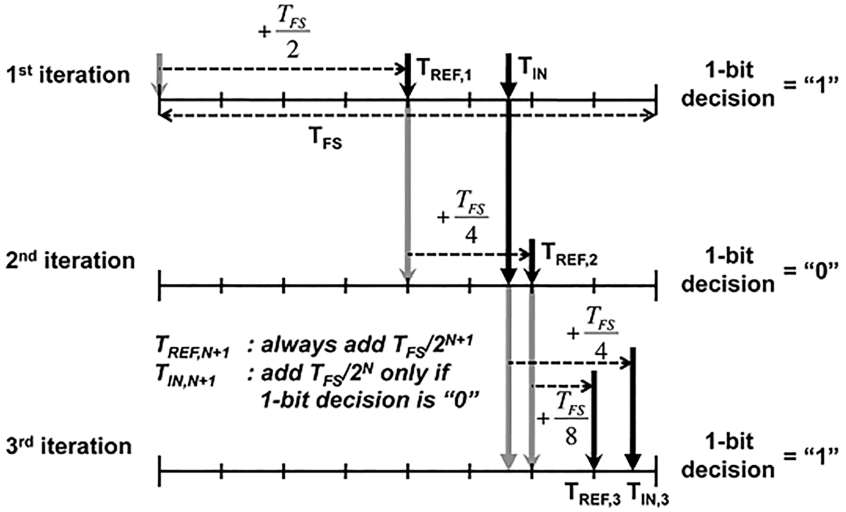

FIGURE 21 Decision-select successive approximation time to digital converter proposed in Chung et al.[94]

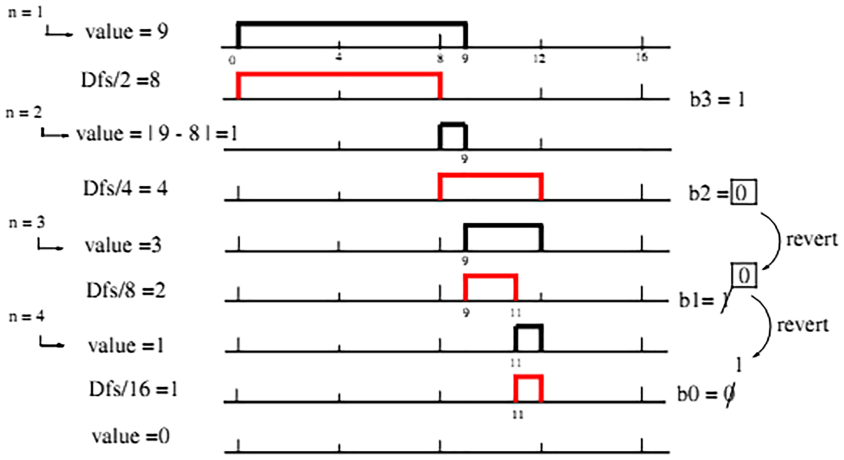

FIGURE 22 Timing diagram for continuous disassembly successive approximation register TDC[95] for input value "9" [Colour figure can be viewed at wileyonlinelibrary.com]

Another novel method called continuous disassembly is presented in Ragab et al.,[95] and the timing diagram of the same is depicted in Figure 22, which subtracts the input with reference using exclusive-or operation. Depending on the resultant subtraction, one-bit output will be decided in each iteration.

One more SAR TDC presented in Jiang et al.[96] verified on both Spice and FPGA platform, claims Vernier level resolution. A novel way to combine both SAR and Vernier technique has been proposed. But the architecture is designed with two repetitive input timing events. In other words, *Start* and *Stop* input signals for the TDC must be two clocks, hence not suitable for a single shot measurement setup.

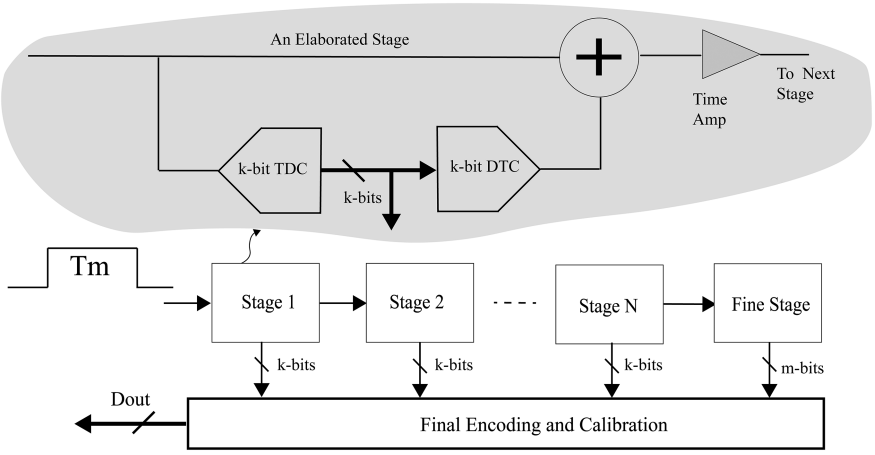

FIGURE 23 Conceptual diagram of pipeline TDC

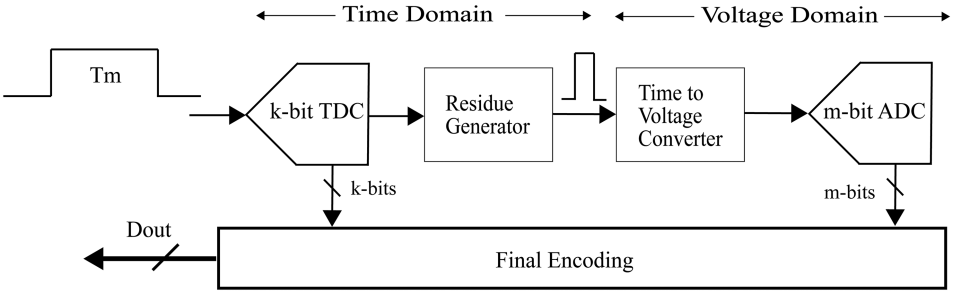

FIGURE 24 Conceptual diagram of hybrid domain TDC

TABLE 2 Comparison of indirect and hybrid TDCs

Reference and year	Method	Technology	Resolution	DNL	INL	Range	Clock/ rate	Power	Target application
Stevens et al.[24] (1989)	TVC	1.6 μm	0.5 ns	-	1.7 mV	6.5–27 ns	100 MHz	-	HEPD
Raisanen-Ruotsalainen et al.[25] (1991)	TAC + dual slope ADC	-	400 ps	-	-	500 ns	10 MHz		Range finders
Rezvanyvardom et al.[28] (2014)	TAC + dual slope ADC	0.18 μm	5 bit	-	-	Dynamic	100 MHz	186 μW	Raman spectroscopy
Xu et al.[30] (2013)	TAC + SAR ADC	90 nm	1 ps	−0.6/0.7 LSB	−1.1/2.3 LSB	256 ps	10 MSPS	20 mW	-
Määttä and Kostamovaara[26] (1998)	Counter + TAC + ADC	Discrete	10 ps	±20 ps	-	2.5 μs	100 KHz		TOF laser radar
Keränen et al.[27] (2011)	Counter + TAC + ADC	Discrete	1 ps	-	±10 ps	328 μs	200 MHz	5.8 W	TOF application
Kim et al.[99] (2015)	Delay line + TAC+SAR ADC	65 nm	630 fs	−0.87/0.98 LSB	−3.01/2.78 LSB	-	120 MSPS	3.7 mW	-

TABLE 3 Comparison of direct measurement techniques

Reference	Method	Technology/ device	Resolution	DNL	INL	Range	Clock/rate	Power	Target application
Torres et al.[38] (2014)	FTDC/buffer delay line	FPGA Kintex-7	22.7 ps	2.6 LSB	3.4 LSB	5.24 μs	-	-	TOF-PET
Staszewski et al.[41] (2006)	FTDC/INV delay line	90 nm	20 ps	<0.7 LSB	<0.7 LSB	0.96 ns	26 MHz	6.9 mW	ADPLL
Wang et al.[44] (2017)	Merged delay line	FPGA Kintex-7	4.3 ps rms	-	< ±2 LSB	50 ns	544 MHz	-	-
J. Yu et al.[50] 2010	Vernier ring TDC	130 nm	8 ps	-	-	32.768 ns	15 MSPS	7.5 mW	TOF/ADPLL
N. Xing et al.[59] (2010)	Cyclic Vernier DL	180 nm	14.6 ps	−1/+1.2 LSB	±1.5 LSB	50 ns	1 MHz	6.4 mW	Read out ICs
J. Zhang and Zhou[100] (2018)	2-stage Vernier loop shrinking	Actel FPGA	8.5 ps	0.36/−0.2 LSB	0.91/−0.6 LSB	10 ns	1,042 ns/conversion	-	-
Lu et al.[49] (2016)	2D Vernier using GROs	65 nm	2.2 ps	-	-	20 ns	50 MSPS	2.3 mW	ADPLL
Vercesi et al.[48] (2010)	2D VDL	65 nm	4.8 ps	±1 LSB	−1/3.3	0.6144 ns	50 MSPS	1.65 mW	ADPLL
Mattada[58] (2016)	VRO TDC	FPGA Spartan 3	4 ps	±2 LSB	±2 LSB	-	2us	10 μW dynamic	Temperature measurement
Mantyniemi et al.[93] (2019)	Cyclic SAR	350 nm	3.2 ps rms	0.8 ps	7.8 ps	327μS	100 MHz	33 mW	Laser range finder
H. Chung et al.[94] (2012)	Decision select SAR	65 nm	9.76 ps	−1.2/1.3 LSB	±2 LSB	10 ns	80 MSPS	9.6 mW	-
Ragab et al.[95] (2016)	Continuous disassembly SAR	65 nm	30.76 ps	±1 LSB	−2.38/1.8 LSB	31.5 ns	29.4 MSPS	2.8 mW	-
Kim et al.[101] (2015)	Stochastic	14 nm FinFET	1.17 ps	0.8 LSB	2.3 LSB	1.198 ns	100 MSPS	0.78 mW	ADPLL
J. Wu et al.[54] (2015)	Stochastic	130 nm	1 ps	−0.7/0.5 LSB	−1.7/0.5 LSB	75 ps	2 MHz	0.9 mW	ADPLL
Strayer et al.[70] (2009)	GRO TDC	130 nm	6 ps	-	-	95 dB	5 MSPS	2.2-21 mW	ADPLL
Caram et al.[78] (2015)	HRO TDC	45 nm	18 ps	-	2.7 LSB	3.1 ns	10 MSPS	2.7 mW	-
Krishna et al.[75] (2019)	SRO TDC	180 nm	12 ps	-	<0.5 LSB	30 ns	2.5 MSPS	2.2 mW	Temp sensor
Rezvanyvardom and Farshidi[102] (2015)	Pipeline TDC	180 nm	195 fs	1.15/−1.1 LSB	1.1/−0.8 LSB	300 ps	300 MSPS	720 μW	-
Kim et al.[103] (2013)	Pipeline TDC	130 nm	1.76 ps	±0.6 LSB	±1.9 LSB	1.8 ns	300 MSPS	14 mW	PET
Cao et al.[87] (2012)	ΔΣ MASH	130 nm	6 ps	-	-	20 ns	62.5 MHz	1.7 mW	LIDAR TOF
X. Chen et al.[85] (2014)	ΔΣ TDC	180 nm	25 ps	-	-	200 ps	8 MHz	33.2 mW	RADAR SYSTEMS

TABLE 3 (Continued)

Reference	Method	Technology/ device	Resolution	DNL	INL	Range	Clock/rate	Power	Target application
Dayanik et al.[86] (2015)	1-bit CTΔΣ	65 nm	176 fs	-	-	NA	270 MHz	8.4 mW	Fractional-N PLL
P. Chen et al.[63] (2000)	Pulse shrinking	350 nm	68 ps	-	-	16 ns	100 KSPS	1.2 mW	-
Park and Yuan[64] (2015)	Pulse shrinking	130 nm	296 ps	−0.25/0.3 LSB	−0.15/0.78 LSB	0.3to 76.8 ns	12.88 MSPS	0.516 mW	-
Chen et al.[65] (2014)	Pulse shrinking (2 stage)	350 nm	40 ps	-	±0.6 LSB	22 ns	10 SPS	165 nm	-
Szplet and Klepacki[66] (2010)	Pulse shrinking (2 stage)	Spartan 3 FPGA	42 ps	−0.98/0.5 LSB	−4.17 to 3.5 LSB	11.5 ns	734 ns/conversion	-	-
P. Chen et al.[32] (2016)	Pulse stretching	350 nm	50 ps	-	±1.1 LSB	250 ns	150 KSPS	0.75 mW	Laser range finders
Wang et al.[4] (2014)	MPTDC	Cyclone-III	625 ps	-	-	625 ns	200 MHz	-	PET detector
Wang et al.[104] (2016)	MPTDC	Kintex-7	27.1 ps	0.44/0.87 LSB	0.44 to 0.82 LSB	4.3 ns	233 MSPS	-	-
Chen et al.[105] (2013)	MPTDC	Startix 4	84 ps	−0.48 to 0.45 LSB	−0.6 to 0.57 LSB	5 to 205 ns	300 MHz	-	-

17 | PIPELINE TDC

Like the SAR method, the pipeline structure is also borrowed from ADC architecture legacy. Multistage conversion is required to have both long measurement and fine resolution.[97] In some cases, it is important to ensure the reliability of the results. Most of the two-stage conversion will be sufficient for all applications. Sometimes the multistage architecture is called coarse–fine TDC. However, one inherent drawback of the coarse–fine stage is its inefficiency in hardware utilization. That is, while one stage is doing a conversion, another stage is idle. To improve the hardware utilization pipeline structure can be adopted. The pipeline structure dramatically minimizes the conversion and dead time inherent to the architecture. The general structure of Pipeline TDC is as depicted in Figure 23.

18 | HYBRID DOMAIN TDC

There are few works in which switching between *time* domain and *amplitude* domain has been observed. The conceptual diagram of hybrid domain TDC is as depicted in Figure 24. Simplest hybrid domain TDC proposed by adding coarse (Counter) stage prior to indirect measurement.[98] In another case, the first stage is designed using delay line TDC, and the second stage is implemented using SAR ADC.[99] It is possible to have the voltage domain (ADC) first and time domain (TDC) at the second stage. These architectures are suitable if one wants to embed the advantages of both the time domain and amplitude domain.

19 | SUMMARY AND COMPARISON

By observing many TDC architectures, principles and trends some of the following observations are summarized.

1. Counter TDC is the most simple and reliable TDC. Hence, it is suitable at the coarse level in multistage conversion.
2. Multistage conversion (Interpolation) has the advantages of a wide range and high resolution.
3. Delay TDCs are fast and low powered and suitable for short-range applications.
4. Not all TDCs suitable for all applications. For example, some TDC architectures are not suitable for single-shot measurement.
5. Measuring nonlinearities of a long-range and high precision TDC is challenging. Also, INL and DNL of TDC may extend beyond one digit (LSB).
6. Pulse shrinking/stretching TDCs can yield high resolution but suffers from slow conversion rate.
7. TDC architectures like Vernier TDC has fine resolution beyond silicon technology. TDC with femtoseconds is already reported.
8. All ADC-architecture principles and characteristics cannot be imported for TDC design. Also holding and integrating *time* samples are still major challenges.
9. Researchers moving toward *time* mode and many new applications of TDCs are yet to be discovered. Fully digital architectures are more stable and linear over the measurement range.

Tables 2 and 3 compare different performance metrics of various TDC architectures.

20 | CONCLUSION

A comprehensive study of different time measurement principles, architectures, and designing techniques has been carried out. Necessity, scope, and different applications of TDC were listed. Working principle along with illustrations, advantages and limitations of most of the TDCs were described. To compare and quantify TDC metrics, we referred and tabulated key results of several publications. Important key performance metrics of TDCs such as resolution, range, nonlinearities, conversion time, and power were observed and presented.

A whole lot of applications of TDCs are yet to be discovered as it is considered a promising future data converter. TDC can be an integral part of 3-D imaging, human detection behind the wall, and autonomous vehicle system. DTC is yet to be employed for modern instrumentation.

A set of standards with respect to TDC parameters and nomenclature are possible by making proven TDC architecture as a part of IEEE standards. Fortunately, most of the TDC performance improvements are due to continuous CMOS technology developments. There are few commercially available TDCs (e.g., TDC7200 by Texas Instruments) that indicate the enormous opportunities for developers and vendors.

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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REFERENCES

1. Lee SK, Seo YH, Park HJ, Sim JY. A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS. *IEEE J Solid-St Circ*. 2010;45(12):2874-2881. https://doi.org/10.1109/JSSC.2010.2077110
2. Kao S-K, Hsieh Y-H, Cheng H-C. An all-digital DLL with duty-cycle correction using reusable TDC. *Int J Circ Theor App*. 2016;44(5):1055-1070. https://doi.org/10.1002/cta.2124
3. Wang Y, Jiang M, Liu B, Jia S, Zhang X. A 1-Gbps reference-less burst-mode CDR with embedded TDC in a 65-nm CMOS process. *Int J Circ Theor App*. 2018;46(8):1565-1576. https://doi.org/10.1002/cta.2490
4. Wang Y, Cheng X, Li D, Zhu W, Liu C. A linear time-over-threshold digitizing scheme and its 64-channel DAQ prototype design on FPGA for a continuous crystal PET detector. *IEEE Trans Nucl Sci*. 2014;61(1):99-106. https://doi.org/10.1109/TNS.2013.2293758
5. Chan AH, Roberts GW. A jitter characterization system using a component-invariant Vernier delay line. *IEEE Trans Very Large Scale Integr VLSI Syst*. 2004;12(1):79-95. https://doi.org/10.1109/TVLSI.2003.820531
6. Palojärvi P, Määttä K, Kostamovaara J. Integrated time-of-flight laser radar. *IEEE Trans Instrum Meas*. 1997;46(4):996-999. https://doi.org/10.1109/19.650815
7. Nissinen J, Nissinen I, Kostamovaara J. Integrated receiver including both receiver channel and TDC for a pulsed time-of-flight laser rangefinder with cm-level accuracy. *IEEE J Solid-St Circ*. 2009;44(5):1486-1497. https://doi.org/10.1109/JSSC.2009.2017006
8. Won JY, Ko GB, Lee JS. Delay grid multiplexing: simple time-based multiplexing and readout method for silicon photomultipliers. *Phys Med Biol*. 2016;61(19):7113-7135. https://doi.org/10.1088/0031-9155/61/19/7113
9. Yoshioka K, Kubota H, Fukushima T, et al. A 20-ch TDC/ADC hybrid architecture LiDAR SoC for 240 × 96 pixel 200-m range imaging with smart accumulation technique and residue quantizing SAR ADC. *IEEE J Solid-St Circ*. 2018;53(11):3026-3038. https://doi.org/10.1109/JSSC.2018.2868315
10. Park K, Park J. 20 Ps resolution time-to-digital converter for digital storage oscilloscopes. In: *Nuclear Science Symposium*. 1998:876–881.
11. Mattad MP, Guhilot H, Kamat RK. Area efficient time to digital converter (TDC) architecture with double ring-oscillator technique on FPGA for fluorescence measurement application. In: *IEEE Recent Advances in Intelligent Computational Systems, RAICS*. 2011:260–263.
12. Niclass C, Favi C, Kluter T, Gersbach M, Charbon E. A 128 × 128 single-photon image sensor with column-level 10-bit time-to-digital converter array. *IEEE J Solid-St Circ*. 2008;43(12):2977-2989. https://doi.org/10.1109/JSSC.2008.2006445
13. Nissinen I, Nissinen J, Holma J, Kostamovaara J. A TDC-based 4×128 CMOS SPAD array for time-gated Raman spectroscopy. In: *European Solid-State Circuits Conference*. 2014. https://doi.org/10.1109/ESSCIRC.2014.6942041
14. Chen CC, Lu WF, Tsai CC, Chen P. A time-to-digital-converter-based CMOS smart temperature sensor. In: *Proceedings - IEEE International Symposium on Circuits and Systems*. 2005. https://doi.org/10.1109/ISCAS.2005.1464649
15. Mattada MP, Magadum SM, Guhilot H. Identification of hotspots on FPGA using time to digital converter and distributed tiny sensors. In: *ISPTS 2015-2nd International Symposium on Physics and Technology of Sensors: Dive Deep Into Sensors, Proceedings*; 2015:235–239.
16. El-Halwagy W, Mousavi P, Hossain M. A 79 dB SNDR, 10 MHz BW, 675 MS/s open-loop time-based ADC employing a 1.15 ps SAR-TDC. In: *2016 IEEE Asian Solid-State Circuits Conference, A-SSCC 2016 - Proceedings*. 2017. https://doi.org/10.1109/ASSCC.2016.7844200.
17. Luo P, Bai C, Zhou C, Luo M. A PWM DC-DC converter with optimum segmented output stage and current detector. *Microelectron J*. 2015;46(8):723-730. https://doi.org/10.1016/j.mejo.2015.06.003
18. Jimenez-irastorza A, Sevillano JF, Arizti F, Rebollo I, Berenguer R. Comparative study on time-to-digital converters for low-power RFID tag sensors. *Microelectron J*. 2013;44(10):912-919. https://doi.org/10.1016/j.mejo.2012.11.007
19. Henzler S. Time-to-digital converters. Springer US. 2010. https://doi.org/10.1007/978-90-481-8628-02
20. Szplet R. Time-to-digital converters. In: Carbone P, Kiaei S, Xu F, eds. *Design, modeling and testing of data converters*. Berlin, Heidelberg: Springer. 2014:211-246.
21. Kang X, Wang S, Liu Y, Sun X, Zhou R, Ma T, Wu Z, Jin Y. A simple smart time-to-digital converter based on Vernier method for a high resolution LYSO MicroPET. In: *IEEE Nuclear Science Symposium Conference Record*. 2007. https://doi.org/10.1109/NSSMIC.2007.4436739.
22. Yuan F. CMOS time-to-digital converters for mixed-mode signal processing. *J Eng*. 2014;4(4):140-154. https://doi.org/10.1049/joe.2014.0044

23. Wang Z, Huang C, Wu J. A review of Cmos time-to-digital converter. *J Circuits Syst Comput*. 2014;23(07):1-21. https://doi.org/10.1142/S0218126614300013
24. Stevens AE, Van Berg RP, Van der Spiegel J, Williams HH.. Sub-nanosecond time-to-voltage converter and analog memory. In: *EEE International Symposium on Circuits and Systems*. 1989:268-271.
25. Raisanen-Ruotsalainen E, Rahkonen T, Kostamovaara J. Time interval measurements using time-to-voltage conversion with built-in dual-slope and conversion. In: *Proceedings - IEEE International Symposium on Circuits and Systems*. 1991:2573-2576.
26. Määttä K, Kostamovaara J. A high-precision time-to-digital converter for pulsed time-of-flight laser radar applications. *IEEE Trans Instrum Meas*. 1998;47(2):521-536. https://doi.org/10.1109/19.744201
27. Keränen P, Määttä K, Kostamovaara J. Wide-range time-to-digital converter with 1-ps single-shot precision. *IEEE Trans Instrum Meas*. 2011;60(9):3162-3172. https://doi.org/10.1109/TIM.2011.2122510
28. Rezvanyvardom M, Nejad TG, Farshidi E. A 5-bit time to digital converter using time to voltage conversion and integrating techniques for agricultural products analysis by Raman spectroscopy. *Inf Process Agric*. 2014;1(2):124-130. https://doi.org/10.1016/j.inpa.2014.11.003
29. Kim Y, Shon D, Kim TW. A 0.008-mm 2, 35-μW, 8.87-ps-resolution CMOS time-to-digital converter using dual-slope architecture. *Int J Circ Theor App*. 2017;45(4):466-482. https://doi.org/10.1002/cta.2272
30. Xu Z, Miyahara M, Matsuzawa A. A 1ps-resolution integrator-based time-to-digital converter using a SAR-ADC in 90 nm CMOS. In: *IEEE 11th International New Circuits and Systems Conference, NEWCAS*. Paris; 2013:1-4.
31. Park K, Park J. Time-to-digital converter of very high pulse stretching ratio for digital storage oscilloscopes. *Rev Sci Instrum*. 1999;70(2):1568-1574. https://doi.org/10.1063/1.1149626
32. Chen P, Chen CC, Shen YS. A low-cost low-power CMOS time-to-digital converter based on pulse stretching. *IEEE Trans Nucl Sci*. 2006;53(4):2215-2220. https://doi.org/10.1109/TNS.2006.876051
33. Lee M, Abidi AA. A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue. *IEEE J Solid-St Circ*. 2008;43(4):769-777. https://doi.org/10.1109/JSSC.2008.917405
34. Rashidzadeh R, Muscedere R, Ahmadi M, Miller WC. A delay generation technique for narrow time interval measurement. *IEEE Trans Instrum Meas*. 2009;58(7):2245-2252. https://doi.org/10.1109/TIM.2009.2013685
35. Lin CH, Syrzycki M. Pico-second time interval amplification. In: *International SoC Design Conference, ISOCC*. Seoul; 2010:201-204.
36. Nakura T, Mandai S, Ikeda M, Asada K. Time difference amplifier using closed-loop gain control. In: *Symposium on VLSI Circuits (VLSIC)*. Kyoto. 2009:208-209.
37. Bayer E, Traxler M. A high-resolution (<10 ps RMS) 48-channel time-to-digital converter (TDC) implemented in a field programmable gate Array (FPGA). *IEEE Trans Nucl Sci*. 2011;58(4):1547-1552. https://doi.org/10.1109/tns.2011.2141684
38. Torres J, Aguilar A, Garcia-Olcina R, et al. Time-to-digital converter based on FPGA with multiple channel capability. *IEEE Trans Nucl Sci*. 2014;61(1):107-114. https://doi.org/10.1109/TNS.2013.2283196
39. Liu C, Wang Y. A 128-channel, 710 M samples/second, and less than 10 ps RMS resolution time-to-digital converter implemented in a kintex-7 FPGA. *IEEE Trans Nucl Sci*. 2015;62(3):773-783. https://doi.org/10.1109/TNS.2015.2421319
40. Chen Y-H. Run-time calibration scheme for the implementation of a robust field-programmable gate array-based time-to-digital converter. *Int J Circ Theor App*. 2019;47(1):19-31. https://doi.org/10.1002/cta.2571
41. Staszewski RB, Vemulapalli S, Vallur P, Wallberg J, Balsara PT. 1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2006;53(3):220-224. https://doi.org/10.1109/TCSII.2005.858754
42. Yu G, Wang Y, Yang H. A low power time-to-digital converter for all-digital phase-locked loop. *Journal of Electronics*. 2011;28(3):402-408. https://doi.org/10.1007/s11767-011-0720-8
43. Chen YH. A high resolution FPGA-based merged delay line TDC with nonlinearity calibration. In: *Proceedings - IEEE International Symposium on Circuits and Systems*. 2013:2432-2435.
44. Wang Y, Cao Q, Liu C. A multi-chain merged tapped delay line for high precision time-to-digital converters in FPGAs. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2017;65(1):96-100. https://doi.org/10.1109/tcsii.2017.2698479
45. Ljuslin C, Christiansen J, Marchioro A, Klingsheim O. An integrated 16-channel CMOS time to digital converter. *IEEE Trans Nucl Sci*. 1994;41(4):1104-1108. https://doi.org/10.1109/23.322866
46. Dudek P, Szczepanski S, Hatfield JV. high_resolution_CMOS_TDC_utilizing_a_vernier_delay_line. *Jssc*. 2000;35(2):1-8.
47. Xing N, Song H, Jeong DK, Kim S. A PVT-insensitive time-to-digital converter using fractional difference Vernier delay lines. In: *Proceedings - IEEE International SOC Conference, SOCC*. Belfast. 2009:43-46.
48. Vercesi L, Liscidini A, Castello R. Two-dimensions vernier time-to-digital converter. *IEEE J Solid-St Circ*. 2010;45(8):1504-1512. https://doi.org/10.1109/JSSC.2010.2047435
49. Lu P, Wu Y, Andreani P. A 2.2-ps two-dimensional gated-Vernier time-to-digital converter with digital calibration. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2016;63(11):1019-1023. https://doi.org/10.1109/TCSII.2016.2548218
50. Yu J, Dai FF, Jaeger RC. A 12-bit Vernier ring time-to-digital converter in 0.13 μ CMOS technology. *IEEE J Solid-St Circ*. 2010;45(4):830-842. https://doi.org/10.1109/JSSC.2010.2040306
51. Markovic B, Tisa S, Villa FA, Tosi A, Zappa F. A high-linearity, 17 ps precision time-to-digital converter based on a single-stage Vernier delay loop fine interpolation. *IEEE Trans Circuits Syst, II, Reg Briefs*. 2013;60(3):557-569. https://doi.org/10.1109/TCSI.2012.2215737
52. Razmdideh R, Saneei M. Low-power, latch-based multistage time-to-digital converter in 65 nm CMOS technology. *Int J Circ Theor App*. 2018;46(6):1264-1271. https://doi.org/10.1002/cta.2468

53. Kratyuk V, Hanumolu PK, Ok K, Mayaram K, Moon UK. A digital PLL with a stochastic time-to-digital converter. In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*. Honolulu, HI; 2006:31-32.
54. Wu J, Wang Z, Chen C, Huang C, Zhang M. A 2.4-GHz all-digital PLL with a 1-ps resolution 0.9-mW edge-interchanging-based stochastic TDC. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2015;62(10):917-921. https://doi.org/10.1109/TCSII.2015.2457792
55. Song M, Jung I, Pamarti S, Kim C. A 2.4 GHz 0.1-Fref-bandwidth all-digital phase-locked loop with delay-cell-less TDC. *IEEE Trans Circuits Syst, II, Reg Briefs*. 2013;60(12):3145-3151. https://doi.org/10.1109/TCSI.2013.2265975
56. Samarah A, Carusone AC. A digital phase-locked loop with calibrated coarse and stochastic fine TDC. *IEEE J Solid-St Circ*. 2013;48(8):1829-1841. https://doi.org/10.1109/JSSC.2013.2259031
57. Mattada MP, Guhilot H. Area efficient Vernier time to digital converter (TDC) with improved resolution using identical ring oscillators on FPGA. In: *IEEE International Conference on 'Smart Structures and Systems', ICSSS*. 2013:125-130.
58. Mattada MP, Magadum SM, Guhilot H. Identification of hotspots on FPGA using time to digital converter and distributed tiny sensors. *J Inst Smart Struct Syst (ISSS) JISSS*. 2016;5(September):1-11.
59. Xing N, Woo JK, Shin WY, Lee H, Kim S. A 14.6 ps resolution, 50 ns input-range cyclic time-to-digital converter using fractional difference conversion method. *IEEE Trans Circuits Syst, II, Reg Briefs*. 2010;57(12):3064-3072. https://doi.org/10.1109/TCSI.2010.2073810
60. Chen P, Chen CC, Zheng JC, Shen YG. A PVT insensitive Vernier-based time-to-digital converter with extended input range and high accuracy. *IEEE Trans Nucl Sci*. 2007;54(2):294-302. https://doi.org/10.1109/TNS.2007.892944
61. Lu P, Andreani P, Liscidini A. A 90 nm CMOS gated-ring-oscillator-based 2-dimension Vernier time-to-digital converter. In: *NORCHIP*. Copenhagen; 2012:1-4.
62. Lu P, Andreani P, Liscidini A. A 2-D GRO Vernier time-to-digital converter with large input range and small latency. In: *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*. Seattle, WA. 2013:151-154.
63. Chen P, Liu SI, Wu J. A CMOS pulse-shrinking delay element for time interval measurement. *IEEE Trans Circuits Syst II Analog Digit Signal Process*. 2000;47(9):954-958. https://doi.org/10.1109/82.868466
64. Park YJ, Yuan F. A 12.88 MS/s 0.28 pJ/conv.step 8-bit stage-interleaved pulse-shrinking time-to-digital converter in 130 nm CMOS. In: Midwest Symposium on Circuits and Systems. 2015. https://doi.org/10.1109/MWSCAS.2015.7282114
65. Chen CC, Lin SH, Hwang CS. An area-efficient CMOS time-to-digital converter based on a pulse-shrinking scheme. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2014;61(3):163-167. https://doi.org/10.1109/TCSII.2013.2296192
66. Szplet R, Klepacki K. An FPGA-integrated time-to-digital converter based on two-stage pulse shrinking. *IEEE Trans Instrum Meas*. 2010;59(6):1663-1670. https://doi.org/10.1109/TIM.2009.2027777
67. Choi KC, Lee SW, Lee BC, Choi WY. A time-to-digital converter based on a multiphase reference clock and a binary counter with a novel sampling error corrector. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2012;59(3):143-147. https://doi.org/10.1109/TCSII.2012.2184370
68. Uchida D, Ikebe M, Motohisa J, Sano E. A 12-bit, 5.5-μW single-slope ADC using intermittent working TDC with multi-phase clock signals. In: *21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. Marseille. 2014:770-773.
69. Mota M, Christiansen J, Debieux S, Ryjov V, Moreira P, Marchioro A. A flexible multi-channel high-resolution time-to-digital converter ASIC. In: *IEEE Nuclear Science Symposium and Medical Imaging Conference (2000) -2*. 2000, pp 9/155–9/159.
70. Straayer MZ, Perrott MH. A multi-path gated ring oscillator TDC with first-order noise shaping. *IEEE J Solid-St Circ*. 2009;44(4):1089-1098. https://doi.org/10.1109/JSSC.2009.2014709
71. Yu M, Zong S, Tang X, Wang Y. A temperature stabilized multi-path gated ring oscillator based TDC. In: *Proceedings - International Conference on Computer Science and Information Processing, CSIP*. Lyon, France. 2012:703-708.
72. Gebara FH, Schaub JD, Drake AJ, Nowka KJ, Brown RB. 4.0 GHz 0.18 μm CMOS PLL based on an interpolative oscillator. In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*. 2005. https://doi.org/10.1109/VLSIC.2005.1469343
73. Park J-H, Jung D-H, Jung S-O. GRO-TDC with gate-switch-based delay cell halving resolution limit. *Int J Circ Theor App*. 2017;45(12):2211-2225. https://doi.org/10.1002/cta.2344
74. Elshazly A, Rao S, Young B, Hanumolu PK. A noise-shaping time-to-digital converter using switched-ring oscillators—analysis, design, and measurement techniques. *IEEE Journal of Solid-State Circuits*. 2014;49(5):1184-1197. https://doi.org/10.1109/JSSC.2014.2305651
75. Krishna RS, Mal AK, Mahapatra R. Time-domain smart temperature sensor using current starved inverters and switched ring oscillator-based time-to-digital converter. *Circ Syst sig Process*. 2019;39(4):1751-1769. https://doi.org/10.1007/s00034-019-01233-8
76. Atef M, El-Nozahi M, Hegazi E. A second-order noise-shaping time-to-digital converter using switched-ring oscillator. In: *Proceedings - IEEE International Symposium on Circuits and Systems*. 2015. https://doi.org/10.1109/ISCAS.2015.7169010
77. Yu W, Kim K, Cho S. A 148fsrms integrated noise 4 MHz bandwidth second-order ΔΣ time-to-digital converter with gated switched-ring oscillator. *IEEE Trans Circuits Syst, II, Reg Briefs*. 2014;61(8):2281-2289. https://doi.org/10.1109/TCSI.2014.2321195
78. Caram JP, Galloway J, Kenney JS. Harmonic ring oscillator time-to-digital converter. In: *Proceedings - IEEE International Symposium on Circuits and Systems*; 2015. https://doi.org/10.1109/ISCAS.2015.7168595
79. Song W, Lee J, Cho N, Burm J. An ultralow power time-domain temperature sensor with time-domain delta–sigma TDC. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2017;64(10):1117-1121. https://doi.org/10.1109/TCSII.2015.2503717
80. Park YJ, Parekh P, Yuan F. All-digital ΔΣ time-to-digital converter with bi-directional gated delay line time integrator. *Microelectron J*. 2018;81:179-191. https://doi.org/10.1016/j.mejo.2018.05.010
81. Wei CL, Liu SI. A digital PLL using oversampling delta–sigma TDC. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2016;63(7):633-637. https://doi.org/10.1109/TCSII.2016.2530904

82. Chujo T, Hirabayashi D, Arafune T, et al. Timing measurement BOST with multi-bit delta–sigma TDC. In: *Proceedings of the 2015 IEEE 20th International Mixed-Signals Test Workshop, IMSTW 2015*. 2015. https://doi.org/10.1109/IMS3TW.2015.7177881
83. Hsu CM, Straayer MZ, Perrott MH. A low-noise wide-BW 3.6-GHz digital ΔΣ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation. *IEEE Journal of Solid-State Circuits*. 2008;43(12):2776-2786. https://doi.org/10.1109/JSSC.2008.2005704
84. Young B, Kwon S, Elshazly A, Hanumolu PK. A 2.4 ps resolution 2.1 mW second-order noise-shaped time-to-digital converter with 3.2 ns range in 1 MHz bandwidth. In: *Proceedings of the Custom Integrated Circuits Conference*. 2010. https://doi.org/10.1109/CICC.2010.5617612.
85. Chen X, Zhang W, Rhee W, Wang Z. A ΔΣ-TDC-based beamforming method for vital sign detection radar systems. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2014;61(12):932-936. https://doi.org/10.1109/TCSII.2014.2362793
86. Dayanik MB, Collins N, Flynn MP. A 28.5–33.5 GHz fractional-N PLL using a 3rd order noise shaping time-to-digital converter with 176 fs resolution. In: *European Solid-State Circuits Conference*. 2015. https://doi.org/10.1109/ESSCIRC.2015.7313906
87. Cao Y, De Cock W, Steyaert M, Leroux P. Design and assessment of a 6 ps-resolution time-to-digital converter with 5 MGy gamma-dose tolerance for LIDAR application. *IEEE Trans Nucl Sci*. 2012;59(4):1382-1389. https://doi.org/10.1109/TNS.2012.2193598
88. Cao Y, De Cock W, Steyaert M, Leroux P. 1-1-1 MASH delta–sigma time-to-digital converters with 6 ps resolution and third-order noise-shaping. *IEEE J Solid-St Circ*. 2012;47(9):2093-2106. https://doi.org/10.1109/JSSC.2012.2199530
89. Wu J, Shi Z. The 10-ps wave union TDC: improving FPGA TDC resolution beyond its cell delay. In: *IEEE Nuclear Science Symposium Conference Record*. 2008. https://doi.org/10.1109/NSSMIC.2008.4775079
90. Wu J. On-chip processing for the wave union TDC implemented in FPGA. In: 2009 *16th IEEE-NPSS Real Time Conference - Conference Record*. 2009. https://doi.org/10.1109/RTC.2009.5322002
91. Qi J, Deng Z, Gong H, Liu Y. A 20 ps resolution wave union FPGA TDC with on-chip real time correction. In: *IEEE Nucl Sci Symp Conf Rec*. 2010. https://doi.org/10.1109/NSSMIC.2010.5873788
92. Pan W, Gong G, Li J. A 20-ps time-to-digital converter (TDC) implemented in field-programmable gate array (FPGA) with automatic temperature correction. *IEEE Trans Nucl Sci*. 2014;61(3):1468-1473. https://doi.org/10.1109/TNS.2014.2320325
93. Mantyniemi A, Rahkonen T, Kostamovaara J. A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method. *IEEE J Solid-St Circ*. 2009;44(11):3067-3078. https://doi.org/10.1109/JSSC.2009.2032260
94. Chung H, Ishikuro H, Kuroda T. A 10-bit 80-MS/s decision-select successive approximation TDC in 65-nm CMOS. *IEEE J Solid-St Circ*. 2012;47(5):1232-1241. https://doi.org/10.1109/JSSC.2012.2184640
95. Ragab KO, Mostafa H, Eladawy A. A novel 10-bit 2.8-mW TDC design using SAR with continuous disassembly algorithm. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2016;63(10):909-913. https://doi.org/10.1109/TCSII.2016.2536238
96. Jiang R, Li C, Yang M, et al. Successive approximation time-to-digital converter with Vernier-level resolution. In: *2016 IEEE 21st International Mixed-Signal Testing Workshop, IMSTW 2016*. 2016. https://doi.org/10.1109/IMS3TW.2016.7524226
97. Mattada M, Guhilot H. 10-bit 2-stage time to digital converter for Raman spectroscopy. *Int J Innov Technol Explor Eng (IJITEE)*. 2019;8(8):2744-2749.
98. Keränen P, Kostamovaara J. Noise and nonlinearity limitations of time-to-voltage based time-to-digital converters. In: *2016 IEEE 21st International Mixed-Signal Testing Workshop, IMSTW 2016*. 2016. https://doi.org/10.1109/IMS3TW.2016.7524226
99. Kim J, Kim YH, Kim K, Yu W, Cho S. A hybrid-domain two-step time-to-digital converter using a switch-based time-to-voltage converter and SAR ADC. *IEEE Trans Circuits Syst, II, Exp Briefs*. 2015;62(7):631-635. https://doi.org/10.1109/TCSII.2015.2415631
100. Zhang J, Zhou D. An 8.5-ps two-stage Vernier delay-line loop shrinking time-to-digital converter in 130-nm flash FPGA. *IEEE Trans Instrum Meas*. 2018;67(2):406-414. https://doi.org/10.1109/TIM.2017.2769239
101. Kim SJ, Kim W, Song M, Kim J, Kim T, Park H. A 0.6V 1.17 ps PVT-tolerant and synthesizable time-to-digital converter using stochastic phase interpolation with 16× spatial redundancy in 14 nm FinFET technology. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. 2015. https://doi.org/10.1109/ISSCC.2015.7063035
102. Rezvanyvardom M, Farshidi E. Design of a novel pipeline time-to-digital converter based on dual-slope interpolation and time amplification. *IETE J Res*. 2015;61(3):300-307. https://doi.org/10.1080/03772063.2015.1018849
103. Kim JS, Seo YH, Suh Y, Park HJ, Sim JY. A 300-MS/s, 1.76-ps-resolution, 10-b asynchronous pipelined time-to-digital converter with on-chip digital background calibration in 0.13-μm CMOS. *IEEE J Solid-St Circ*. 2013;48(2):516-526. https://doi.org/10.1109/JSSC.2012.2217892
104. Wang Y, Kuang P, Liu C. A 256-channel multi-phase clock sampling-based time-to-digital converter implemented in a Kintex-7 FPGA. In: *Conference Record - IEEE Instrumentation and Measurement Technology Conference*. Taipei. 2016:1-5.
105. Chen P, Cheng HC, Widodo A, Tsai WX. A PVT insensitive field programmable gate array time-to-digital converter. In: *2013 IEEE Nordic-Mediterranean Workshop on Time-to-Digital Converters (NoMe TDC)*. Perugia. 2013:1-4. https://doi.org/10.1109/NoMeTDC.2013.6658232

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