A 12-Bit Digital-to-Time Converter (DTC) for Time-to-Digital Converter (TDC) and Other Time Domain Signal Processing Applications

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***Abstract*—This paper describes a digital-to-time converter (DTC) architecture that can be used as a fine interpolator in a time-to-digital converter (TDC) or as an adjustable delay in clock deskewing, for example. The new architecture of the DTC achieves adjustable sub-ps-level resolution with high linearity in ns-level dynamic range. The propagation delay adjustment is implemented by digitally controlling both the unit load capacitors and the discharge current of the load capacitance. The proposed DTC achieves 610 fs resolution and ~1.25 ns dynamic range. The total simulated power consumption is 3.5 mW with 125 MHz input signal frequency with 3 V supply. The design was simulated using a 0.35 μm CMOS process.**

***Index Terms*—CMOS integrated circuits, digital-to-time converter (DTC), time digitizer, time interval measurement, time-to-digital converter (TDC).**

I. Introduction

Especially when using deep sub-micron technologies the signal processing is moving into time domain because the reduced voltage headroom makes it difficult to implement analogue signal processing functions. Furthermore, with deep sub-micron CMOS technologies the time domain resolution of digital signals is better than the voltage resolution of analogue signals [1]. Digital-to-time converters (DTC) can be used in time domain signal processing to adjust the propagation delays of signals paths with digital control words. The operation of the DTC is analogous to the digital-to-analog converter (DAC) used in analog signal processing. In this work DTCs are designed to be used as building blocks of a time-to-digital converter (TDC) architecture, in which the conversion is based on cyclic time domain successive approximation (CTDSA) method utilizing binary search [2].

Reaching ps-level resolution in time-to-digital conversion is feasible for example with architectures that utilize the delay difference between the logic gates[3], the RC delay of the on-chip wiring [4], the frequency difference between two oscillators [5], time amplification [6], pulse shrinking [7], the difference between logic thresholds [8], passive on-chip voltage divider [9] or random variation of the timing of the digital logic gates [10][11]. In addition, multi-stage interpolation architectures have been developed to shorten the dynamic range and to improve the linearity of the interpolators providing the ps-level resolution [12].

In this paper the high timing resolution of the DTC is achieved by digitally adjusting the load capacitance of an adjustable delay cell and by digitally controlling the discharge current of the load capacitance. Compared to the earlier design with an 8-bit DTC used in a TDC prototype [2], the 12-bit DTC architecture presented in this paper aims to improve the resolution, dynamic range and linearity of the DTC to make it possible to improve the single-shot precision, i.e. random error, of the TDC to simplify the TDC architecture and to reduce the power consumption of the TDC.

The paper is organized as follows. Section II explains the architecture of the DTC. In Section III design details and simulation results of the TDC are presented. The conclusions are summarized in Section IV.

II. DTC

A. DTC Architecture

The new DTC uses four parallel adjustable delay cells with enable inputs a[2:0] and tri-state outputs, a matrix of 512 digitally, controllable moscaps as load capacitances adjustable as blocks of powers of two with control signals b[9:0], and a comparator, as shown in Fig. 1. Depending on the control signals a[2:0] the discharge current of the load capacitance can have three values I, 2I and 4I. With the control signals b[9:0] the apparent capacitance of the adjustable moscaps can be varied between two values depending on the value of the control signal CTRL of each block.

Depending on the digitally controllable combination of the discharge current and the load capacitance the propagation delay of the DTC can be linearly scaled with 12-bit dynamic range with a nominal resolution of 610 fs and 1.25 ns dynamic range. This makes it also suitable for high resolution clock de-skewing for example. In the binary search algorithm of the CTDSA method, however, only adjustments made as powers of two are required [2].

The main difference compared to the old DTC design used in [2] is the comparator in the output of the DTC block. The previous DTC used a simple CMOS inverter as a comparator

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to determine when the capacitively loaded node CL was discharged below the inverter threshold value, as shown in Fig. 2. However, the slew rate dependency of the simple inverter limits the achievable linear dynamic range. The comparator has a much more stable propagation delay as a function of the input signal slew rate [13]. Using the comparator with the other input connected to the reference voltage Vref we can reach a much larger linear dynamic range in propagation delay scaling.

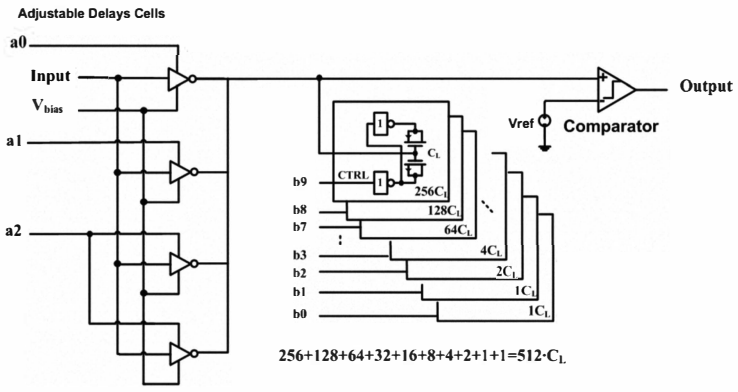


Figure 1. 12 bit Digital-to-time converter (DTC).

Improving the linearity by using the comparator and using the selectable delay cells allows for adding more capacitors and more bits. Although the number of the load capacitors is quadrupled compared to the previous design, the new DTC is able to achieve 12 linear dynamic range.

In the previous design the dynamic range of ~300 ps of the DTC was adequate for the TDC prototype used as a proof of concept for the new CTDSA interpolation method, because the CTDSA was used as the fine interpolator in a TDC architecture combining a 100 MHz counter, a coarse delay-locked delay line interpolator with 312 ps nominal resolution and a CTDSA fine interpolator with 1.2 ps resolution and 312 ps dynamic range. However, increasing the dynamic range of a high resolution interpolator to ns-level makes it possible to reach a large linear μs-level dynamic range and sub-ps resolution just by combining a counter and CTDSA interpolator.

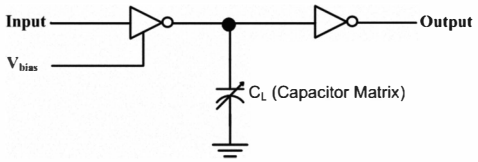


Figure 2. Previous Digital-to-time converter (DTC)

III. CIRCUIT IMPLEMENTATION & SIMULATION

The design was simulated using 0.35μm CMOS technology parameters while operating from 3 V supply.

A. Adjustable Delay Cell

The schematic of the adjustable delay cell is shown in Fig. 3. The delay cell is a three state current starved inverter. The input signal a enables the output of the delay cell for the discharge current selection. The overall propagation delay of the delay cell can be adjusted with a bias voltage V_{bias}, which makes it possible to adopt the propagation delay to the given application and giving conditions so that the propagation delay can be stabilized against the process, voltage and temperature variations. Instead of only scaling the load capacitance, also the discharge current of the load capacitance is digitally controlled with selectable and adjustable delay cells, which markedly reduces the layout area compared to [2] with the same dynamic range and resolution. The four delay cells with the load capacitors have dynamic power consumption of approximately 2.6 mW with 125 MHz input signal frequency.

According to simulation, adding an additional control bit with four more delay cells would reduce the linearity in discharging the current scaling because of the increased parasitic capacitance.

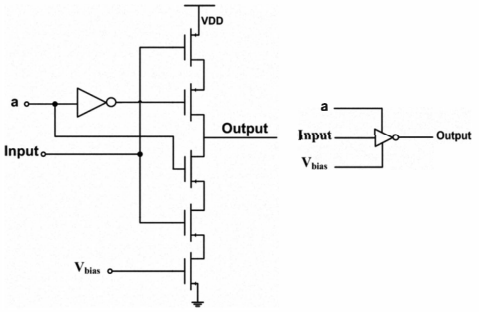


Figure 3. Schematic of Adjustable and Selectable Delay Cell

B. Comparator

The schematic of the two stage comparator is shown in Fig. 4. The output stage is a current sink/source inverter [14]. M6 was sized to have sufficient current to reduce the slew rate [14]. To make sure that the comparator has constant delay regardless of the input signal slew rate, the bandwidth has to be large [15]. Therefore, I_{bias} was chosen to have large bandwidth without significantly increasing the power consumption of the whole DTC [13][14]. The simulated static power consumption of the comparator is less than 900 μW.

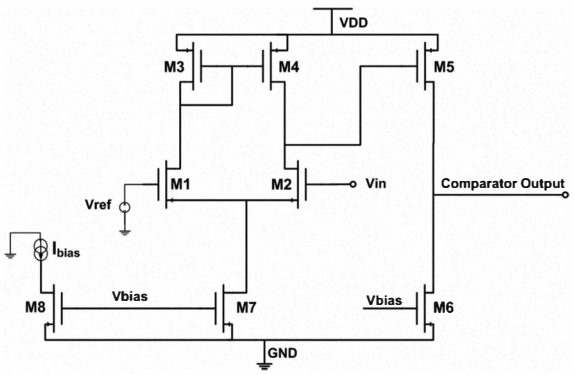
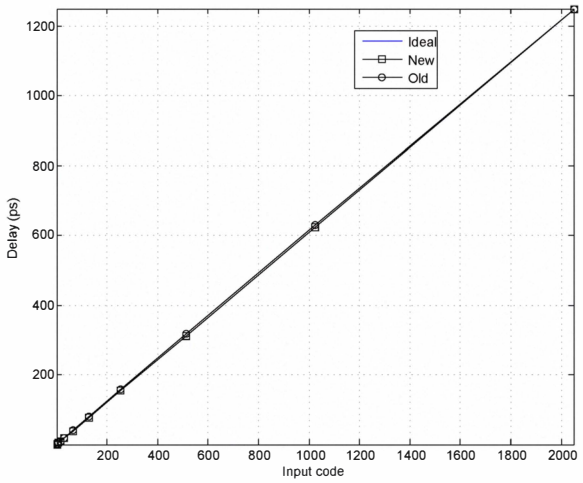


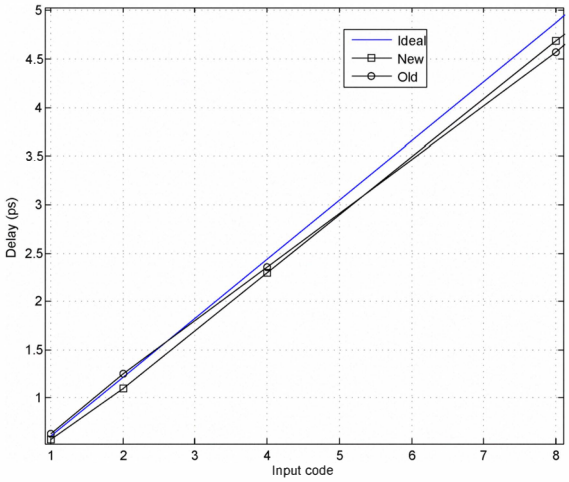
Figure 4. Schematic of the Comparator

C. System Simulation

The simulated linearity over the 2048 LSBs of the new DTC architecture and the DTC architecture used in [2] are presented in Fig. 5. The bias voltages are adjusted to match the propagation delays of both designs. The total simulated power consumption is 6.1 mW of the new DTC.



(a)



(b)

Figure 5. (a) Linearity of the new and old DTC. (b) Linearity of the first 8 bit input code

To see the differences between the two DTCs, the simulation result for the first 8 input codes is presented in Fig. 5(b). The differences seem small, but it is the INL over the whole dynamic range, show is Fig. 6, which shows the improvement achieved with new DTC architecture. Using the comparator instead of the inverter is the main reason for improving the linearity of the DTC.

As shown in Fig. 6, for a large dynamic range, the INL of the new DTC architecture is much less than the case in [2]. The INL of the new and old DTC are +0.23/-0.45 LSB and +9.3/-0.5 LSB, respectively. The INL of the new DTC is less than 1 LSB which means that no missing codes will occur.

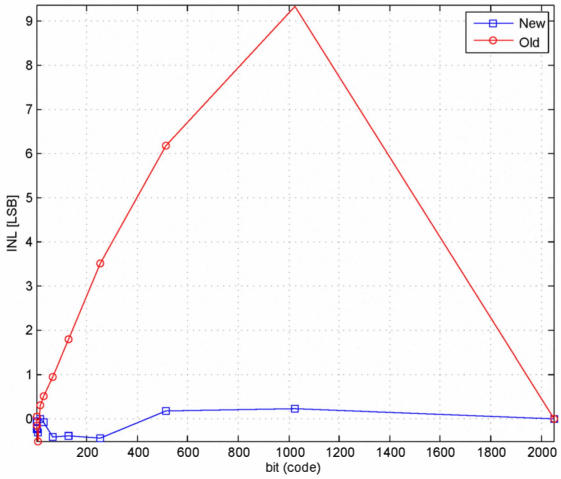


Figure 6. INL of the new and old DTC

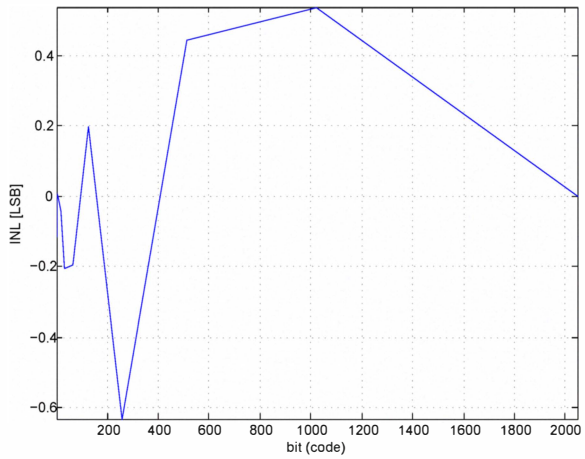


Figure 7. INL of the extended Dynamic Range of 2.5ns

The dynamic range of the new DTC could be further extended by making the unit load capacitor larger and by changing the dimension of the delay cells. The INL of the extended dynamic range of 2.5 ns with resolution of 1.2 ps is presented in Fig. 7. As shown in Fig. 7, the INL is +0.53/-0.63 LSB. The linearity of the new DTC is maintained even for a larger dynamic range. The dynamic range of the new DTC can be extended at the expense of LSB resolution.

IV. Conclusions

In this paper, a 12-bit digital-to-time converter (DTC) using a comparator instead of a simple inverter improves the linearity of the DTC. The improved linearity of the comparator with larger capacitor area allows for extending the dynamic range to ns-level with sub-ps resolution. However, to limit the size of the capacitor matrix, four selectable delay cells are used to scale the capacitor discharge current. With a nominal resolution of 610 fs and 1.25 ns dynamic range the INL of the DTC was +0.23/-0.45 LSB. Even with extended dynamic range of

2.5 ns, the INL is +0.53/-0.63 LSB. The total simulated power consumption is 3.5 mW with 125 MHz input signal frequency with 3 voltage supply.

REFERENCES

[1] R. Staszewski, C.-M. Hung, K. Maggio, J. Wallberg, D. Leipold, and P. Balsara, "All-digital phase-domain tx frequency synthesizer for bluetooth radios in 0.13 mu;m cmos," feb. 2004, pp. 272 – 527 Vol.1.

[2] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A cmos time-to-digital converter (tdc) based on a cyclic time domain successive approximation interpolation method," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 11, pp. 3067 –3078, nov 2009.

[3] J. Rivoir, "Fully-digital time-to-digital converter for ate with autonomous calibration," in *Test Conference, 2006. ITC '06. IEEE International*, oct. 2006, pp. 1 –10.

[4] M. Mota and J. Christiansen, "A high-resolution time interpolator based on a delay locked loop and an rc delay line," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 10, pp. 1360 –1366, oct 1999.

[5] A. Chan and G. Roberts, "A jitter characterization system using a component-invariant vernier delay line," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, no. 1, pp. 79 – 95, jan. 2004.

[6] M. Lee and A. Abidi, "A 9 b, 1.25 ps resolution coarse fine time-to-digital converter in 90 nm cmos that amplifies a time residue," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 4, pp. 769 –777, apr. 2008.

[7] T. Rahkonen and J. Kostamovaara, "The use of stabilized cmos delay lines for the digitization of short time intervals," *Solid-State Circuits, IEEE Journal of*, vol. 28, no. 8, pp. 887 –894, aug. 1993.

[8] K. Minami, M. Mizuno, H. Yamaguchi, T. Nakano, Y. Matsushima, Y. Sumi, T. Sato, H. Yamashida, and M. Yamashina, "A 1 ghz portable digital delay-locked loop with infinite phase capture ranges," 2000, pp. 350 –351, 469.

[9] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 7, pp. 1666 –1676, jul. 2008.

[10] P. Levine and G. Roberts, "High-resolution flash time-to-digital conversion and calibration for system-on-chip testing," *Computers and Digital Techniques, IEE Proceedings* -, vol. 152, no. 3, pp. 415 – 426, may. 2005.

[11] V. Gutnik and A. Chandrakasan, "On-chip picosecond time measurement," 2000, pp. 52 –53.

[12] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "An integrated 9-channel time digitizer with 30 ps resolution," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, vol. 1, 2002, pp. 266 –465 vol.1.

[13] R. J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters.* Springer, 2003.

[14] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design.* Oxford University Press, 2002.

[15] R. van de Grift, I. Rutten, and M. van der Veen, "An 8-bit video adc incorporating folding and interpolation techniques," *Solid-State Circuits, IEEE Journal of*, vol. 22, no. 6, pp. 944 – 953, dec. 1987.