Implementation of a High-Precision and Wide-Range Time-to-Digital Converter With Three-Level Conversion Scheme

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***Abstract*—This brief presents a time-to-digital converter (TDC) with a three-level conversion scheme based on a dual delay-locked loop (DLL) structure. The linear-feedback-shift-register counter is implemented for measurement range extension, and a differential delay cell is adopted for time resolution improvement. Furthermore, the DLL is applied to improve the stability of the multiphase clock frequency. The test chip is designed and fabricated in a Taiwan Semiconductor Manufacturing Company 0.35-μm CMOS process. With an input reference clock of 40 MHz, the total 15-bit three-level TDC can realize a 3-μs maximum range and a 476-ps resolution. The differential nonlinearity is less than $\pm$0.65 LSB, and the integral nonlinearity is within $-$1.35 LSB to $+$1.4 LSB.**

***Index Terms*—Delay-locked loop (DLL), measurement range, time resolution, time-to-digital converter (TDC).**

I. Introduction

SIMILAR to the widely used analog-to-digital converter (ADC), a time-to-digital converter (TDC) can be used to convert a time interval into a digital code; thus, it can be recognized as a particular category of ADCs [1]. If the measured time is converted to a voltage or current signal, the time measurement can be implemented indirectly by the ADC and *vice versa*. However, as compared with ADCs with the same accuracy and measurement range, the digital TDC has more significant advantages. Consequently, the digital TDC with strong noise immunity capability [2] can be used in various fast and weak signal detecting systems, such as the photon time-of-flight (TOF) measurement in an infrared array sensing system [3], as well as the narrow pulsewidth measurement in a wide measurement range temperature detection system [4].

For a single-mode TDC with only one kind of quantization unit, the requirement of the quantization-unit scale for high precision and wide range is completely opposite. In other words, a small unit scale is beneficial for precision improvement, but range extension requires a large unit scale. Thus, a TDC with multiquantization levels is critical in balancing high resolution with wide range in time measurement. Clearly, for a multilevel TDC, the inherent contradiction between accuracy and range can be more effectively alleviated so that the chip area and power consumption can be significantly reduced compared with the single-mode TDC [5].

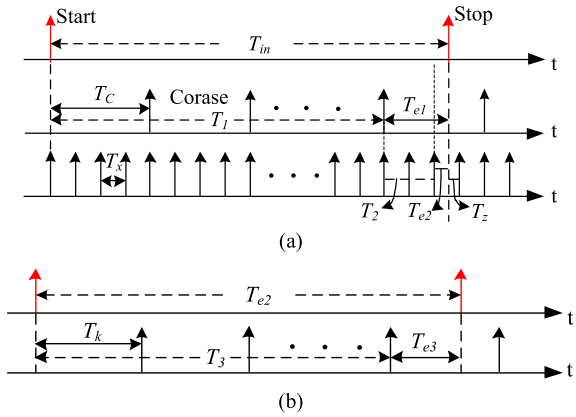

Fig. 1. Time measurement for the segment TDC with multilevel quantization units. (a) Two-level quantization TDC. (b) Fine quantization of error time generated by the two-level TDC.

For these aforementioned reasons, a three-level TDC based on a dual delay-locked loop (DLL) is presented in this brief. Based on a two-level TDC, the Vernier method is introduced to further reduce the residual quantization error, and the time resolution can be far less than the minimum gate delay time determined by the process, while the property of wide range maintains [6].

This brief is organized as follows. In Section II, the basic operation principle, pattern, and constraint conditions are summarized. The descriptions of the TDC circuit structure and sequential control are given in Section III. In Section IV, the experiment results and analysis are presented to verify the circuit's performance. Finally, the conclusions of this brief are summarized in Section V.

II. Principle of Multilevel TDC

In order to release the intrinsic restriction between the fine resolution and the wide range in the time measurement of a single-mode TDC, two or even more quantization units of timescale should be adopted in a combinational way, as shown in Fig. 1. In Fig. 1(a), a two-level TDC is used to measure the time interval $T_{\rm in}$ with two kinds of quantization units, i.e., T_C and T_x. First, the coarse measurement of $T_{\rm in}$ is achieved by the larger quantization unit T_C, where T_1 is the measured time by the high-level TDC and the residual time of T_{e1} is further

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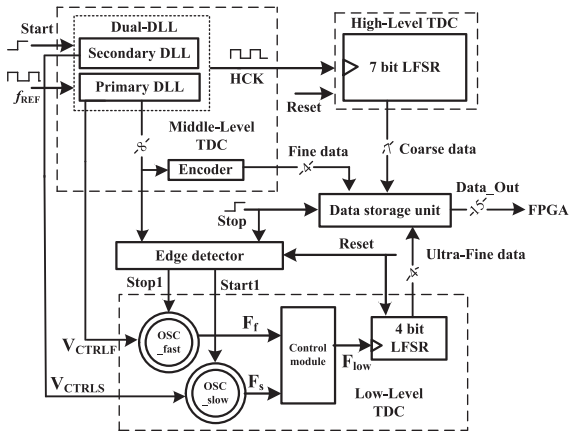

Fig. 2. System architecture of 15-bit three-level TDC.

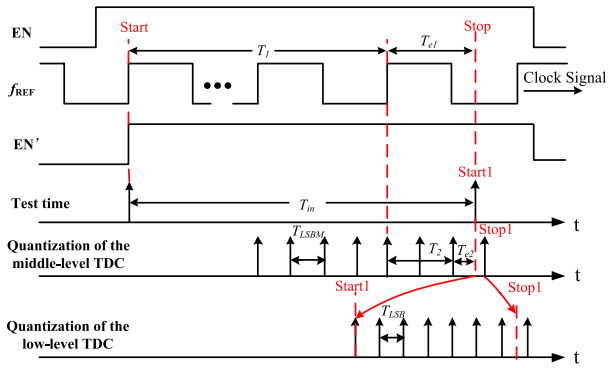

Fig. 3. Timing diagram of the three-level TDC.

distinguished by the smaller quantization unit of T_x. Similarly, T_2 is the measured time by the low-level TDC; thus, the total measured time is $T = T_1 + T_2$, and the residual time of T_{e2} is the final quantization error of the TDC [5].

The continuous discrimination for the residual time can be carried out in a similar way if a much smaller quantization unit is used. As presented in Fig. 2(b), the residual time of the two-level TDC T_{e2} can be further measured by a more accurate timescale of T_k, the measured time is T_3 and the final residual time is T_{e3}. Thus, the more accurate time of $T_1 + T_2 + T_3$ is quantized.

For the segment TDC with multilevel quantization units, each stage of a single-mode TDC should seamlessly cooperate; for this reason, the following principles should be satisfied.

1) Bridging principle: The full range of the low-level TDC must be no less than the quantization unit of the adjacent high-level TDC.
2) Matching principle: For each single-mode TDC, the initial phase of the measured time or the residual time should exactly match with that of the corresponding quantization unit time; thus, the initial errors in multistage quantization can be effectively eliminated.

III. Overall Circuit Architecture

The three-level TDC proposed in this brief is improved from the traditional two-level TDC. The high-level countertype TDC driven by the stable external input clock cycle is used to achieve a high measurement range. In the middle-level fine TDC, the DLL's multiphase clock is utilized to realize the resolution at a level of gate delay time [7]. In addition, a Vernier TDC is adopted in constructing the low-level TDC to obtain a subgate delay resolution.

Taking measurement range extension, power consumption, and signal distortion into consideration, the input clock frequency of counter-type TDC should not be too high. The traditional single-mode DLL can be extended into a dual DLL by adding an extra delay chain [8]. The dual DLL combined with an identical frequency encode block is used as the middle-level TDC. The proposed encoding method chooses the former four tap signals from the primary DLL as encoding outputs directly. Since there is no need for extra encoding circuits, the bit error rate introduced by the delay mismatch of the encoding circuit is eliminated. In addition, two individual stable voltages generated by the dual DLL are used to control the corresponding voltage-controlled ring oscillators (VCOs). Then, the constant differential gate delay time between two oscillation loops is used as the smallest quantization unit to realize ultrafine quantization. Finally, the outputs of each level TDC stored in D-type flip-flop (DFF) chain are transferred to a field-programmable gate array for further processing, including decoding. Fig. 2 presents the system architecture frame of the high-precision three-level TDC.

The proposed TDC can be represented as a three-stage time converter. The first stage is a coarse counter-based TDC that attains a resolution equal to its clock input period t_{CLK} (25 ns at 40 MHz) and offers a high measurement range. The second stage is a dual-DLL-based TDC that delivers a fine time resolution of t_f defined by the unit delay of eight-stage voltage-controlled delay line in the primary DLL; thus, $t_f = t_{\mathrm{CLK}}/8 = 3.125$ ns. The last Vernier TDC stage implemented by the dual VCO is used to get the ultrafine time measurement; the final time resolution can be expressed as $\Delta\mathrm{tr} = t_f/8 = 390$ ps.

Fig. 3 shows the timing diagram of the three-level TDC, where EN is the gated signal to start the system. After the initial phase adjustment by a DFF, EN is turned into EN', fitting with the linear-feedback-shift-register (LFSR) counting clock signal. When the rising edge of Stop comes, the output of the encoder fine data is latched as middle-level TDC output data, and the output of 7-bit LFSR counter coarse data, as high-level TDC output data, is also latched at this moment. Meanwhile, the residual error time of T_{e2} is obtained and Stop serves as the new start signal Start1 to activate low-level TDC. Stop1 is at the spot of the next state of the middle-level TDC after the arrival of Stop; when it arrives, the low-level TDC stops counting, and ultrafine data are latched. Eventually, the total data of the three-level TDC stored at the output registers is transmitted outside in a serial way for further processing.

IV. Circuit Functionality and Characteristics

A. High-Level LFSR Counter

An LFSR is utilized in the high-level TDC, which is driven by a synchronous clock. The maximum range of the output pseudorandom numbers determined by the bit scale can be achieved with only one additional XNOR logic gate embedded in the DFF chain. Moreover, the high-level TDC can be configured both under the counting mode and the data transmission mode by using a multiplexer Mux2_1 to select the signal transportation path.

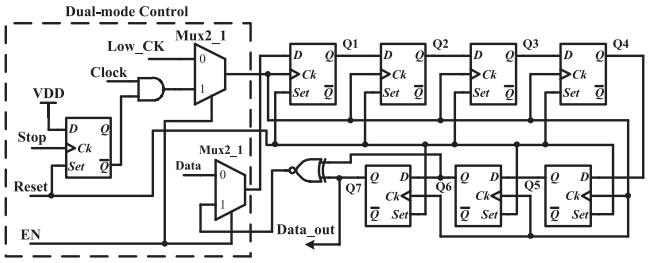

Fig. 4. Dual-mode 7-bit LFSR structure.

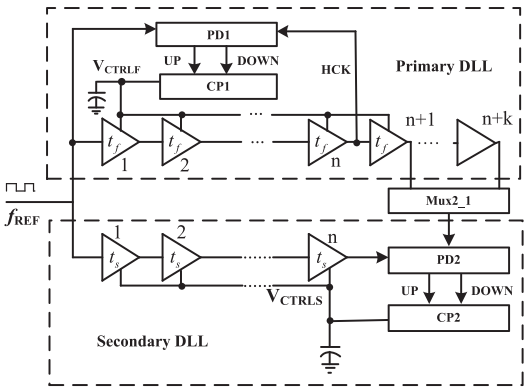

Fig. 5. Dual DLL structure.

The block diagram of the LFSR is shown in Fig. 4. When EN $= 1$, the LFSR works under the counting mode, where the clock signal is provided by the dual DLL. During this gate control period, when Stop arrives, the LFSR stops counting and holds the data until EN falls to low; Low_CK is selected to drive the LFSR. Meanwhile, the feedback loop of the LFSR is immediately cut off; thus, the LFSR shifts from counting mode driven by high frequency to serial data transmission mode driven by the low-frequency clock.

B. Dual DLL

In order to improve the accuracy and stability of the Vernier TDC, a classic dual DLL is adopted to provide the control voltage for the VCO, as shown in Fig. 5. The dual DLL consists of a primary DLL and a secondary one. The dual DLL can be configured under different lengths of the delay chain, corresponding to the resolution varied from $(t_{\rm CLK}/n^2)$ to $k(t_{\rm CLK}/n^2)$. Compared with n-stage delay units in a traditional circuit, extra k delay units are increased to adjust the precision according to the value of k. When $k = 1$, the highest resolution is achieved.

After locking the primary DLL, the rising edge of EN' is aligned with that of $f_{\rm REF}$ and used to start middle-level TDC. HCK, as the nth tap signal of primary DLL, is fed back to PD1, as shown in Fig. 5 and also serves as driving clock of the high-level TDC. When Stop arrives, the statues of the primary DLL are latched and encoded as the output of middle-level TDC. Meanwhile, $V_{\rm CTRLF}$ and $V_{\rm CTRLS}$ depicted in Fig. 5 are used to control two oscillators in the low-level TDC [9]. The output of the $(n+1)$th stage from the primary DLL is chosen to match with that of the nth stage from the secondary DLL. If the phases of the two signals are well matched, the following expression can be obtained:

$$nt_s = (n+1)t_f \tag{1}$$

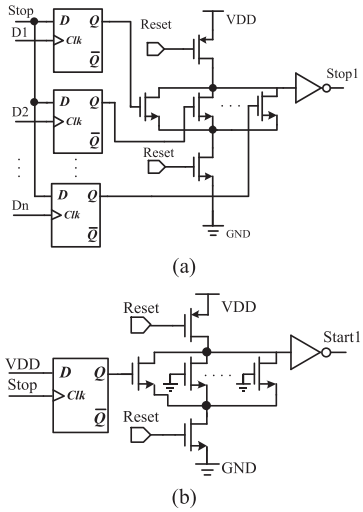

Fig. 6. Schematic of the edge detector. (a) Stop1 signal generating circuit. (b) Start1 signal generating circuit.

where t_f and t_s are the time of primary and secondary DLL delay units, respectively.

Obviously, $t_s > t_f$ can be obtained by the difference between the control voltages of the dual DLL. Under the equilibrium situation, an external input clock cycle $t_{\rm CLK}$ is equally divided by n delay units with a delay of $t_f (= t_{\rm CLK}/n)$. From the aforementioned equations, we obtain

$$t_s = \frac{t_{\rm CLK}}{n} \times \frac{n+1}{n} = \frac{t_{\rm CLK}(n+1)}{n^2}. \tag{2}$$

The difference between the delay time of the two delay units is defined as

$$\Delta t_r = t_s - t_f = \frac{t_{\rm CLK}(n+1)}{n^2} - \frac{t_{\rm CLK}}{n} = \frac{t_{\rm CLK}}{n^2} = \frac{t_f}{n}. \tag{3}$$

The main advantage of the dual DLL is that only a single reference clock is needed. Consequently, the detection resolution is significantly improved with a larger value of n, which breaks the limit of the minimum delay time determined by the CMOS process.

C. Edge Detector

The residual error time of the middle-level TDC is extracted by an edge detector, where the Start1 and Stop1 signals are generated to define the period to be measured by the low-level TDC. As shown in Fig. 6, the edge-detector dynamic circuit consists of two components, one for generating Start1 and the other for Stop1. During precharge mode when Reset $= 0$, the output of Start1 and Stop1 are both preset at a low logic level. In evaluation mode when Reset $= 1$, the variation of Start1 and Stop1 can be detected. In Fig. 6(a), D1 to Dn are signals sampled from the primary DLL's former n taps after the arrival of the Stop signal. Among them, the closest one to the Stop is sampled as Stop1. As shown in Fig. 6(b), Stop serves as a clock to trigger DFF; when the rising edge of Stop arrives, a high logic level is transmitted to turn on the NMOS switch to discharge the preset logic level, and the rising edge of Start1 is thus generated. The other normally ON transistors in parallel are used to match with the delay of Stop1 signal.

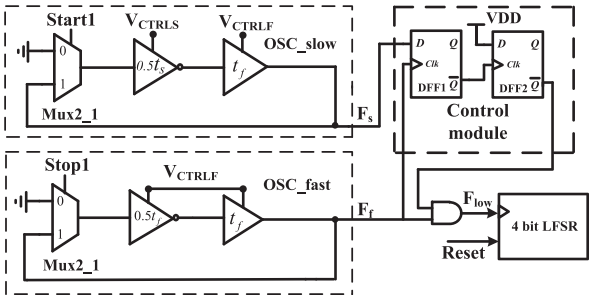

Fig. 7. Low-level TDC structure.

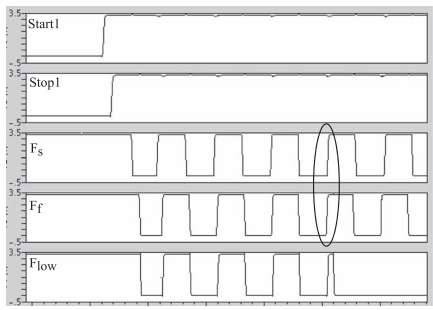

Fig. 8. Transient simulation diagram of low-level TDC.

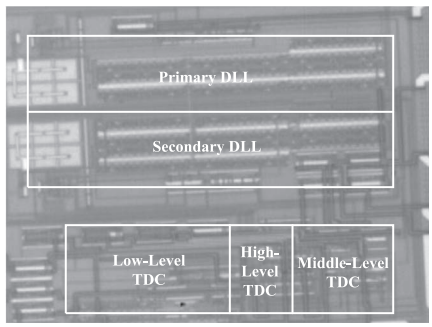

Fig. 9. Chip micrograph.

D. Low-Level Vernier TDC Circuit

As shown in Fig. 7, the low-level Vernier TDC constructed by two similar three-stage ring oscillators is implemented to generate the quantization unit of Δt_r for the middle-level TDC's residual time measurement. Before the gated signal EN turns to high, DLL should finish the transient procedure and be kept stable. The control signal of the V_{ctrlf} provided by the primary DLL is applied to all delay stages in two oscillator rings, except for the inverter delay stage in the OSC_slow ring; only this stage is controlled by the secondary DLL's control voltage V_{ctrls}. In the two oscillators, the identical multiplexers Mux2_1 are utilized to start oscillation by loop path selection. In addition, the noninverter delay units in the two oscillator rings are used to alter the period of the two delay rings; thus, the period time difference between the two OSC rings can be expressed as follows:

$$\Delta t_r = 2(0.5t_s + t_{\mathrm{mux}} + t_f) - 2(0.5t_f + t_{\mathrm{mux}} + t_f) = t_s - t_f \quad (4)$$

where t_{mux} is the delay time of Mux2_1 used in the two rings.

Since the frequency of the fast oscillator is a little bit faster than that of the slow one, the rising edge of the fast clock will finally catch up with that of the slow clock when the measured time defined by Stop1 and Start1 is just elapsed. This event is called a phase coincidence. The phase coincidence is detected by the control module, and a 4-bit LFSR counter driven by F_{low} signal is employed to record the number of the clock cycles (N) of the OSC_fast ring. The quantized time can then be obtained as follows:

$$t_{\mathrm{Low-end}} = N\Delta t_r = N(t_s - t_f). \quad (5)$$

The control module consists of two DFFs and an AND gate. The time interval between Start1 and Stop1 is equal to the initial phase difference of the two ring oscillation signals; it varies from 0 to the top range of t_f for matching with the resolution of the middle-level TDC. In the process of the fast oscillator catching up with the slow one, the clock signal of F_{low} generated by the control circuit is the same as F_f, and when the phase coincidence is detected, F_{low} is reset to zero to stop counting (the transient process is shown in Fig. 8); the logical data latched at this moment by the 4-bit LFSR counter are fixed as the quantization data of the low-level ultrafine TDC and are finally stored at the output registers.

V. Analysis of the Experimental Results

A test chip of the proposed TDC was designed and fabricated in the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm CMOS process. The micrograph of the test chip is shown in Fig. 9.

TABLE I
Data Test for Different Time

TOF(ns)	Data numbers	Random error(ns)	Confidence intervals(ns)	Standard deviation(ns)
50	47	2.822	2.801-2.843	0.01702
200	48	2.844	2.824-2.864	0.01643
300	96	2.953	2.873-3.033	0.01834
500	46	3.052	2.982-3.122	0.01534
2000	47	2.954	2.925-2.983	0.02432

For TOF measurement, random error is defined as the absolute value of the deviation between the measured results A_V and the TOF to be measured, which is given by

$$E_a = |\mathrm{TOF} - A_v|. \quad (6)$$

All data were processed according to the statistical principles, those not between the interval $(\mu - 3\sigma,\ \mu + 3\sigma)$ were considered the error data that should be canceled first, where μ and σ are the mean value and standard deviation of statistics, respectively. The confidence level is set at 0.95 with Gaussian statistics, confidence intervals, and standard deviations of these data shown in Table I.

The TDC can operate at clock rate within 20–100 MHz. Since the resolution is related to the frequency of the input reference clock, the proposed TDC achieves the resolution of 476 (40 MHz) and 250 ps (80 MHz). The tested resolution is slightly larger than the theoretical one due to the effects of process variations and nonlinear factors. Taking power dissipation and clock jitter into considerations, a 40-MHz reference clock is used. The rms jitter of the proposed TDC is around 50 ps (< 476 ps), which need to be further decreased to improve the TDC's accuracy.

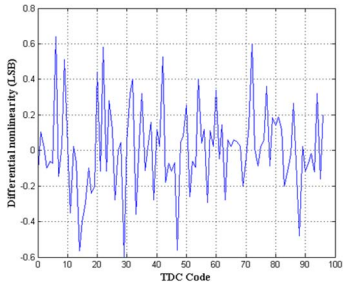

Fig. 10. DNL.

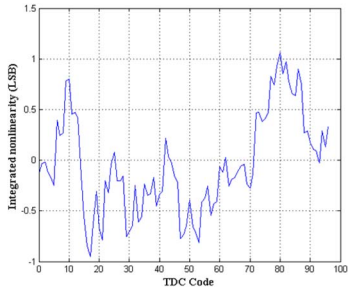

Fig. 11. INL.

TABLE II
PERFORMANCE COMPARISON TO PREVIOUS WORK

	This Work	[10]	[3]	[11]	[12]
Technology	0.35 μm	0.13 μm	0.35 μm	0.13 μm	0.18 μm
Clock	40 MHz	0.64 GHz	80 MHz	0.4 MHz	1.25GHz
Resolution	476 ps	1.56 ns	400 ps	62.5 ps	8.125 ps
Range	3 μs	-	400 ns	64 ns	204.8 ns
DNL	±0.65LSB	20%	4.9%	<4LSB	0.64
INL	<1.4LSB	20%	11.7%	<8LSB	1.21
Power	<6.3 mW	-	6 mW	2.15 mW	32 mW
Area	0.16 mm^2	-	-	-	0.23 mm^2

The corresponding differential nonlinearity (DNL) and the integral nonlinearity (INL) were also calculated to evaluate the linearity of the system, indicating that DNL is less than ±0.65 LSB and INL is within −1.35 LSB–+1.4 LSB, as shown in Figs. 10 and 11, respectively. The degeneration of DNL and INL is mainly due to the mismatch of layout paths in the multiphase sampler and crosstalk of input signals, as well as the mismatch of EN' signal. The performance of the proposed TDC is summarized and compared with other state-of-the-art TDCs in Table II.

VI. CONCLUSION

In this brief, a three-level TDC adopting a multistage conversion scheme has been proposed and fabricated in the TSMC 0.35 μm CMOS process. Different from a conventional coarse-fine two-level TDC, a low-level Vernier TDC is implemented with a dual-DLL-based middle-level TDC for time-resolution improvement. Although the proposed circuit costs more chip area and some power, it realized a high resolution and a wide measurement range with a low-frequency reference clock.

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