Design And Implementation Of Time To Digital Converters

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***Abstract*— Modern VLSI technology is mainly driven by digital circuits because digital circuits has many advantages over analog circuits. By using very small and simple circuits atomic digital functions can be realized. All digital phase locked loops (ADPLL) plays an important role in applications such as Bluetooth, GSM and Wi-Fi. A Time to digital converter (TDC) is the critical part in the ADPLL. The concept of TDC is to sample the outputs of all delay elements at the same time. To know the performance of TDC we are analyzing various TDC architectures using buffers and inverters. Flash type TDC have less resolution which uses single delay line. Whereas Vernier delay line TDC uses two delay lines which resolves finely. Replica delay line TDC reduces mismatches among the delay cells. The Vernier ring TDC places the Vernier delay cells in a ring format and reuses them for the measurement of the input time interval. This TDC architecture will give high resolution than conventional TDC models. The power consumed by various TDC architectures are analyzed. Analysis are done by using Xilinx and cadence virtuoso gpdk 180nm technology .**

***Keywords*— All digital phase locked loops (ADPLL), Time to Digital Converter (TDC), Flash type TDC, Vernier delay TDC, Vernier delay ring TDC.**

I. INTRODUCTION

A Time-to-digital converter (TDC) is similar to an analog-to-digital converter (ADC), except that, instead of quantizing voltage or current, the TDC quantizes time intervals between two rising edges. It is originally developed for nuclear experiments to locate single-shot events , the TDC is now being used in many applications such as laser range finders, space science instruments, physical instruments, phase meters, high energy particle detectors, and digital storage oscilloscopes and measurement devices. Recently, it has been employed to measure phase in all-digital phase-locked loops (PLLs). Precise measurements of time interval are performed with the use of various methods in both the analog and digital domains. The digital methods become dominant due to ease of implementation in integrated circuits, shorter conversion time, and higher immunity to external disturbances. First, the physical quantity is converted to a time signal and then digitized by a time-to digital converter (TDC) to get the corresponding digital output.

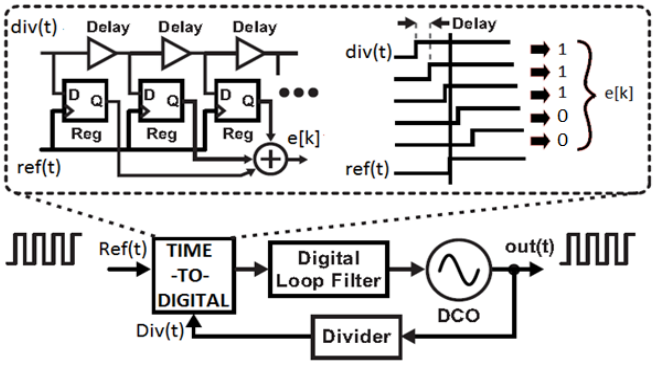

Fig.1. TDC in All-Digital Phase-Locked Loop

Fig. 1 shows the block diagram of a ADPLL where a TDC detects the phase error between the reference and clocks.

II. FLASH-TYPE TDC ARCHITECTURE

Flash architecture in which the digital output is generated by quantizing the time input in units of delay T_{delay}. The architecture of a basic flash-type TDC is shown in Fig.2. It consists of a delay-line using delay cells in the signal path and an array of flip-flops. The input Start signal passes to the delay cells, where the delay elements are connected in series. And then each output signal is connected to a input terminal of the D flip-flop array.

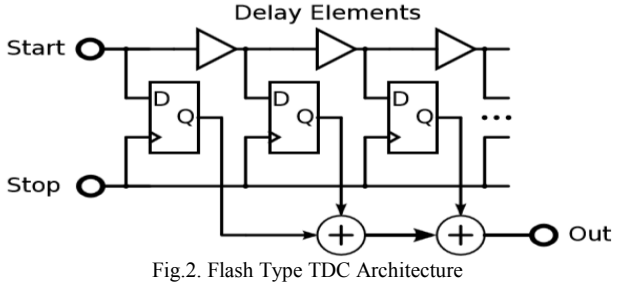

Fig.2. Flash Type TDC Architecture

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Start signal is delayed only by an integer multiple of the buffer delay . The D flip-flop is latched by the rising edge of the Stop signal. This circuit converts the time delay between the signals to a certain number of steps of buffer delay. The quantized output represented in thermometer code corresponds to the time difference between the input signal start and the reference signal stop. The thermometer coded bits are then added together to form the overall TDC output $D_{out.}$ using a thermometer-code-to-binary encoder. The flash-type TDC has the advantage of being able to measure a single-event input. Although the flash type TDC is simple to implement, its resolution is limited by the minimum gate delay. Furthermore, increasing the measurement range requires large chain of delay buffers, thus substantially increasing both area and power. For instance, an N-bit flash TDC will require 2^N delay elements.

III. VERNIER LINE TDC ARCHITECTURE

A vernier TDC overcomes the technology limited resolution of a flash type TDC. By delaying both the input and the reference edges using slightly mismatched delay elements a vernier TDC achieves a resolution equal to the delay difference between two buffers (T_{delay1}-T_{delay2}) which can be smaller than that of the basic TDC, but note that it uses 2N buffers (N buffers of $\tau 1$ and N buffers of $\tau 2$) for an input range from 0 to N ($\tau 1 - \tau 2$).

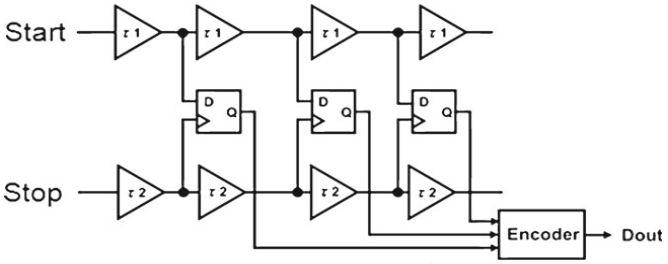

Fig.3 Vernier Type TDC Architecture

Vernier technique may appear to considerably improves the TDC resolution the mismatch between the delay line severely limits the resolution in practice. Wide measurement range requires much more delay cells compared with a flash TDC, making it impractical in high resolution wide range applications.

IV. REPLICA DELAY LINE TDC

The delay chain of buffers and the Vernier delay line, are well-known methods to realize a TDC. In the delay chain the rising edge of the Start signal propagates through the chain of buffers; when the rising edge of the Stop signal arrives, a flip-flop samples the output of each buffer and produces a thermometer code that locates the relative time interval. However, this simple scheme cannot resolve the time interval better than a single buffer delay. On the other hand, using the delay difference between unequal buffers, the Vernier delay line can resolve more finely, but its area increases linearly with the resolution, and the devices must match more tightly. The main concern is in compensating for the mismatch that exists among the delay elements. We use the replica delay line for compensating mismatch in individual delay cells in both the generic delay line TDC and in the vernier delay line TDC architecture. Replica delay line added to the original TDC with the intention of generating additional outputs.

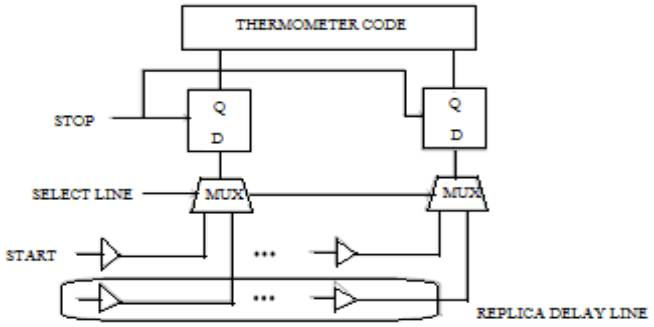

Fig.4 Replica Delay Line TDC Architechture

V. VERNIER DELAYRING TDC ARCHITECTURE

The principle of this architecture is nearly the same as that of delay ring architecture. The end of each chain in the Vernier delay chain architecture is folded back to its beginning to increase the dynamic range without adding more delay elements like in Figure 5. This architecture provides a high resolution. Short delay chain realize a wide dynamic range by reusing of delay elements.

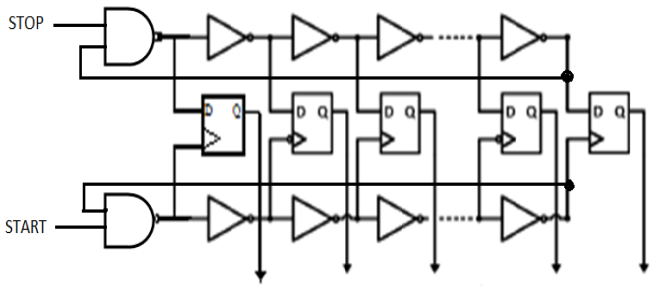

Fig.5. Vernier Ring TDC Architecture

The vernier ring time-to-digital converter evolves from the conventional vernier delay line TDC. Inverters were used as the delay stages to construct the vernier ring TDC. Connecting the outputs of the last delay element of a vernier delay line TDC to the inputs of the first pair of delay element constructs a vernier ring TDC. A NAND gate replaces an inverter as the first delay stage and is used to input the signals. The signal to be measured can be fed in to the delay ring

through one of the inputs of the NAND gate. The vernier ring TDC core consists of a fast ring with smaller delay, a slow ring with larger delay. The propagation delays of the inverters in fast and slow rings are set to T1 and T2 respectively. Thus, the time resolution of the TDC is (T2-T1).

VI. SIMULATION RESULTS

A. FLASH TYPE TDC

Flash type tdc output from the D flip-flop which is obtained as a thermometer code showing the time delay between start signal and stop signal, and this time delay is obtained as a digital output D_{out} using a thermometer-code-to-binary encoder. The simulation ouput for flash TDC is shown in figure.6.

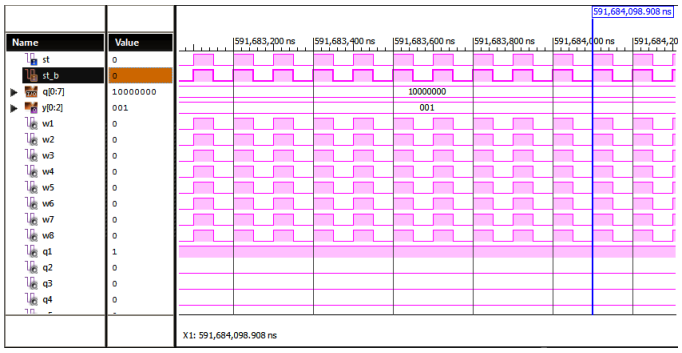

Fig.6. Simulation Output For Flash Type Tdc

The output waveform for flash type TDC architecture is obtained by using gpdk 180nm technology cadence virtuoso tool is shown in Figure 7.

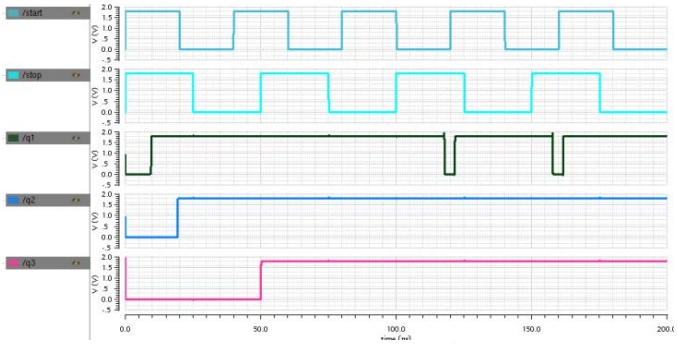

Fig.7. Output Waveform For Flash TDC

B. VERNIER TYPE TDC

Vernier type tdc which uses two delay lines: one, with a buffer delay of t1, for the reference edge, and the other, with a buffer delay of t2, for the edge under measurement. The RTL schematic can be obtained by writing verilog code for the corresponding architecture using Xilinx ISE (Integrated Software Environment) software. The RTL schematic obtained for vernier type TDC is shown in Figure 8.

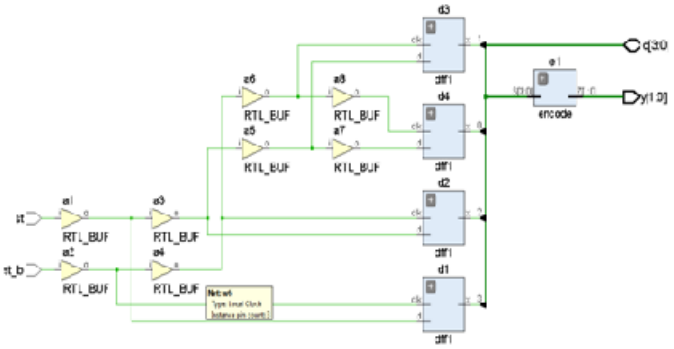

Fig.8. RTL schematic For Vernier Type Tdc

C. REPLICA DELAY LINE TDC

Replica delay line is used for compensating the mismatch in individual delay cells in both the generic delay line TDC and in the vernier delay line TDC architecture. The replica TDC uses the multiplexer to select one of the delay line's output which is given as D inputs of the flip flops. The simulation results are shown in Figure 9.

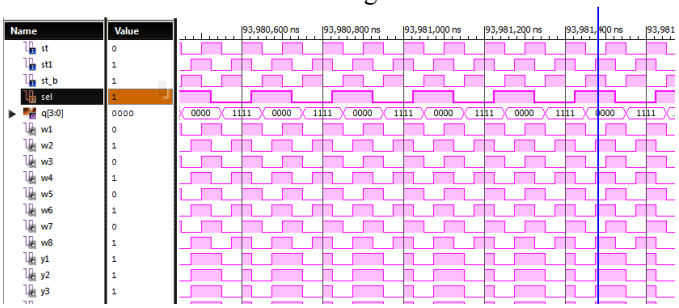

Fig.9. Simulation Output For Replica Delay Line TDC

The output waveform for replica type TDC architecture is obtained by using gpdk 180nm technology cadence virtuoso tool is shown in Figure 10.

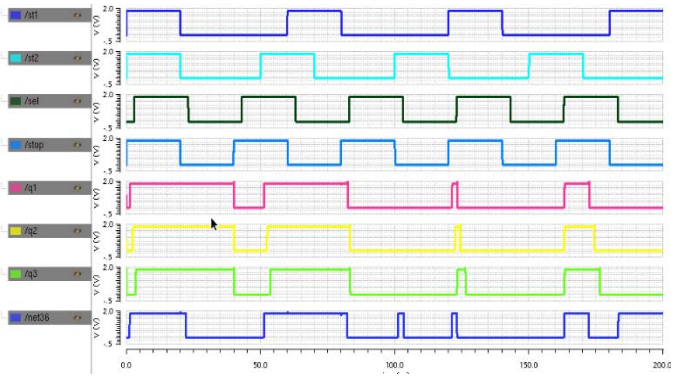

Fig.10. Waveform for replica delay line TDC

D. VERNIER DELAY RING TDC

The vernier delay ring architecture uses inverters as delay stages in the signal path. Vernier ring TDC places the Vernier delay cells and arbiters in a ring format and reuses them for the measurement of the input time interval. The vernier delay ring architecture is implemented using gpdk 180nm technology is shown in Figure 10.

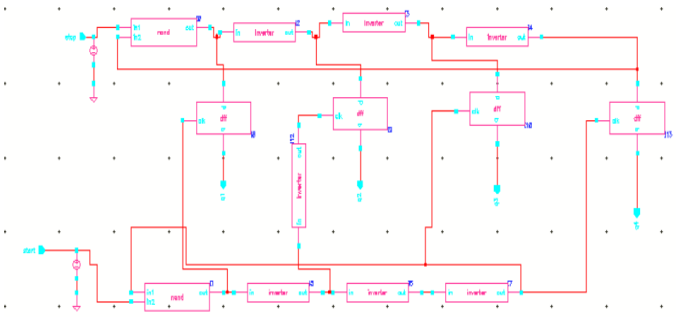

Fig.10. vernier delay ring tdc

The simulation output for this architecture using Xilinx is shown in Figure 11.

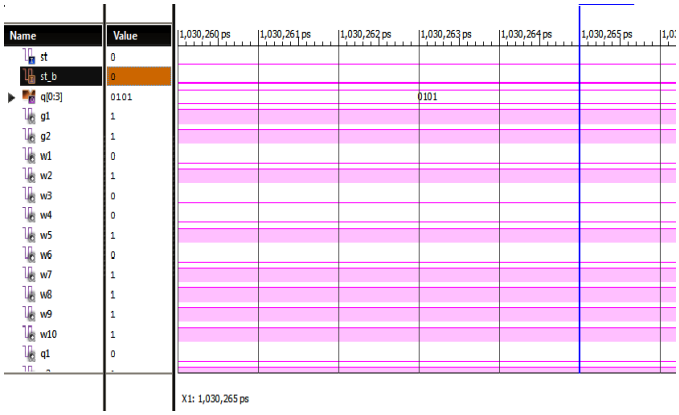

Fig.11. Simulation Output For Vernier Ring TDC

The average power consumption for various TDC architectures are analyzed in cadence virtuoso gpdk 180nm technology. The comparison of power values are shown in table.

TABLE I. COMPARISON TABLE

TDC	FLASH	VERNIER	REPLICA	VERNIER RING
POWER VALUES	381uW	671uW	458uW	506nW

VII. CONCLUSION

The proposed work presents various Time-to-digital converters using buffers and inverters implemented in Xilinx 14.5 software and cadence virtuoso gpdk 180nm technology. Analysis of various TDC have performed. The resolution of flash type TDC is limited by the delay associated with the buffers. The resolution can be increased by replacing the buffers by CMOS inverters. Replica delay line TDC reduces the mismatch of delay elements. Vernier delay ring architecture is folded back to its beginning to increase the dynamic range without adding more delay elements and also achieves low power consumption.

REFERENCES

[1] Amer Samarah, Anthony Chan Carusone, "A Digital Phase-Locked Loop With Calibrated Coarse and Stochastic Fine TDC", IEEE journal of solid-state circuits, vol. 48, 2013, no. 8.

[2] Guansheng Li, Yahya, M. Tousi, ArjangHassibi, EhsanAfshari, "Delay-Line-Based Analog-to-Digital Converters", IEEE transactions on circuits and systemsii: express briefs, vol. 56,2009, no. 6.

[3] Jianjun Yu, Fa Foster Dai, Fellow, Richard C. Jaeger, Life Fellow, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 m CMOS Technology", IEEE journal of solid-state circuits, vol. 45,2010, no. 4.

[4] Moon Seok Kim, Yong-Bin Kim , Kyung-Ki Kim, "All Digital Phased Locked Loop with Local Passive Interpolation Time- to-Digital Converter Based on a Tristate Inverter", IEEE journal of solid-state circuits, vol. 45,2012.

[5] Ping Lu, Antonio Liscidini, PietroAndreani, "A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps", IEEE journal of solid-state circuits, vol. 47,2012, no. 7.

[6] PiotrDudek, Stanislaw Szczepan ´ski, John, V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line",IEEE transactions on solid-state circuits, vol. 35,2000, no. 2 .