This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



# A Review of New Time-to-Digital Conversion Techniques

Scott Tancock, Ekin Arabul and Naim Dahnoun

***Abstract*—Time-to-Digital Converters (TDCs) are vital components in time and distance measurement and frequency locking applications. There are many architectures for implementing TDCs, from simple counter TDCs to hybrid multi-level TDCs which use many techniques in tandem. This paper completes the review literature of TDCs by describing new architectures along with their benefits and trade-offs, as well as the terminology and performance metrics that must be considered when choosing a TDC. It describes their implementation from the gate level upwards and how it is affected by the fabric of the device (FPGA or ASIC) and suggests suitable use cases for the various techniques. Based on the results achieved in the current literature, we make recommendations on the appropriate architecture for a given task based on the number of channels and precision required, as well as the target fabric.**

***Index Terms*—Review, Field Programmable Gate Arrays, Application Specific Integrated Circuits, Time-Digital Conversion, Measurement Techniques, Time Measurement**

## I. Introduction

TIME-TO-DIGITAL converters (TDCs) play a vital role in almost all computational systems in existence. From their appearance in Phase-Locked Loops (PLLs), where they measure the difference between the loop and the reference clock to avoid clock drift, to Time of Flight (ToF) applications where the time between an emission and reception is measured to discover information about an object from which the signal was reflected or the environment through which the signal passed. In addition, there are also quantum versions of these applications, where the signal is a single quantum, and the PLL or time-of-flight measurement must perform well despite some quanta being lost in-flight. They also make an appearance in medical imaging, as some systems such as Positron Emission Tomography (PET) and Fluorescence Lifetime Imaging (FLIM) use the ToF or absorption time of tissues or substances to form an internal image of a complex structure such as a human body.

Time-to-digital converters can be also utilised as time taggers in time correlation systems such as coincidence counters. These systems play an essential role in quantum physics experiments for gating the events of interest from the background noise and measuring the gamma ray correlation in PET systems. Coincidence counters are correlator tools which are tailored to measure the occurrences of simultaneous signal events over multiple channels. This is done by checking whether the events are happening within the same time window called the coincidence window. In a PET scanner setup, a positron emitting radiotracer substance is introduced into the subject's body and the subject is surrounded by detectors which observe gamma rays. While the positron emitting substance decays inside the patient's body, positrons meet with electrons and this results in annihilation of both the positron and electron. An annihilation of a positron and electron pair generates two gamma rays that travel in opposite directions towards two photon detectors placed in the surroundings. Counting the coincidences caused by the two gamma rays emitted allows analysis of the radiotracer's distribution in the body, which is then used for image formation. TDCs can be utilised to digitise gamma ray pairs' times of flight in such a set-up. An example of such a scheme can be found in [1].

Another area where TDCs are commonly used is spectrometry. Spectrometry can be defined as distinguishing mixed substances based on an interaction between light and their matter. Common spectrometry examples where TDCs can be used are Time of Flight Mass Spectrometry (TOFMS) and fluorescence spectrometry. In TOFMS, the times of flight of ions are used to measure the ions' mass to charge ratio. This process starts with ionising the atoms and molecules to be measured causing the required number electrons to be knocked off to form a positive ion. Then, the ions are accelerated to the same kinetic energy and projected for a known distance. Since heavier and lighter ions have different velocities due to their different masses, their time of flight will vary and this reveals information about their charge to mass ratio [2]. ToF tomography is an example of mass spectrometry. Fluorescence spectroscopy, which is commonly used in chemistry, biomedicine and medicine to analyse organic compounds [3], is used to determine the fluorescence content of the substance by measuring the decay time after the substance has been excited by a light beam. TDCs are employed as a part of the Time-Correlated Single Photon Counting (TCSPC) tools used to measure the decay time [4].

Range finding ToF systems such as LiDARs are another common application of TDCs. In a typical LiDAR, a START signal corresponds to the time when the laser transmitter starts to illuminate the target with photons and the detection of reflected photons from the target by the receiver is denoted as the STOP signal. The photons' time of flight can be used to measure the distance. The differences between these values are used to determine the photons' time of flight between transmission and detection. A TDC is employed to quantise and digitise the events of START and STOP signals in such applications.

As the time resolution of single-photon detectors is in the order of 100 ps [5], the desired resolution and precision of a TDC is approximately 10 ps. On the other hand, readily-available Avalanche Photo-Diodes (APDs) can easily reach $<$ 10 ps rise time error [6], so a TDC resolution and precision of $<$ 1 ps is desirable to obtain the highest accuracies. The Differential Non-Linearity (DNL) must also be low enough

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



to avoid significant mis-measurements if the largest code is hit by coincidence. For PET detectors, the Full-Width Half-Maximum (FWHM) is in the order of 10 ns [7], so a detector resolution of 1ns, achievable with a counter, is acceptable.

Many TDC products are available commercially for different purposes. An example of a low cost 2-channel LiDAR TDC is the Texas Instruments TDC7201 chip which provides 55 ps resolution [8]. For applications such as coincidence correlation, a TDC such as Swabian Instrument's Time Tagger, which provides 18 channels with 10 ps second resolution, can be used [9]. PicoQuant's Picoharp and Hydraharp series, which can provide down to 1 ps resolution in up to 8 channels of operation, are popular TDC products in Time-Correlated Single Photon Counting (TCSPC) [10]. In addition, IdQuantique's ID900 Time Controller is another example of a commercial time tagging box which provides 20 ps resolution with up to 64-channel operation [11].

Previously, Porat wrote the first review on sub-nanosecond time interval measurements [12] in 1973, examining Time-to-Amplitude Converter (TAC), counter and Vernier TDCs. Then, Kalisz wrote a review [13] in 2004 on time interval measurement methods, which analysed the architecture of TAC, dual-slope time amplifier, counter, delay line, Vernier and Voltage-Controlled Oscillator (VCO) TDCs. Zielinski wrote a review of time interval measurement techniques [14] in 2009 which covered counter, multi-phase clock, delay line and Vernier TDCs implemented on FPGAs.

In 2010, Napolitano et al. wrote a "survey" on time interval measurement techniques [15] which discussed counter, dual-slope time amplifier, TAC, Vernier, delay line and stochastic TDCs, while Henzler wrote a book [16] describing all the aforementioned as well as local passive interpolation, gated ring oscillator, pulse shrinking and metastable time amplifier TDCs in detail, with a particular focus on their ASIC (Application-Specific Integrated Circuit) implementation and proof of concept. Then, in 2014, Wang, Huang and Wu [17] also performed a review focused on the CMOS implementations of delay line, pulse-shrinking, Vernier, gated ring oscillator, metastable time amplifier and stochastic TDCs. Most recently, Chaberski et al. published a comparison [18] in 2017 covering two forms of delay line TDC (delayed start, delayed stop) and a Vernier TDC. They also mention the use of multiple delay lines in an Equivalent Coding Line (ECL) topology.

This paper aims to complete the current review literature by describing the methods that have not yet been mentioned, along with their benefits and drawbacks, to aid the designer in choosing an appropriate TDC to satisfy their design requirements. It will look at TDCs implemented both on field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs), which differ vastly in terms of the resources and flexibility available, both in production and in the field and hence benefit more or less from various techniques.

The rest of this paper will be structured as such: the paper will start with Section II where calibration and linearisation techniques for TDCs will be described. We will then explore new TDC architectures in Section III, with a subsection dedicated to each new TDC design. Section IV will then compare the results achieved from the various designs in the literature, while considering the difference in technology platforms. This will lead on to Section V, where the various advantages and disadvantages of the architectures will be compared, with Section VI concluding with recommendations on which architectures provide the best trade-offs.

## II. Calibration and Linearisation Techniques

In an ideal fine time to digital converter, each delay element that is used for time quantisation should have an equal bin width. However, due to the internal routing of the TDC and temperature and power fluctuations, the TDC suffers from non-constant and inconsistent bin widths. Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are expressions used to define the measurement errors affecting the TDCs' linearity. To overcome these converter errors, various calibration (II-A and II-B) and linearisation (II-C and II-D) methods are utilised.

### A. Statistical Code Density Testing Method

The statistical code density testing method is one of the common methods used for TDC calibration and is described in [19, 20].

The measurement of each bin width determines the likelihood of each bin to get hit within the delay line, so the probability density function (PDF) can be applied to characterise the bin width in comparison to the other bins. The width of the i$^{\text{th}}$ bin can be seen in Equation 1, where $\tau_i$ is the width of the i$^{\text{th}}$ bin, $T_{CLK}$ is the clock period, $N_i$ is the number of hits in the i$^{\text{th}}$ bin and $N_{total}$ is the total number of counts.

The transfer function of the delay line can then be formed by determining the cumulative distribution function (CDF) of the calculated bin widths (Equation 2). The transfer function is used as a look-up table to correct the code generated by the converter.

To be able to statistically analyse the bin width distribution of the delay line, there needs to be a sufficient number of random triggers to provide a high confidence level. As was described in [21], the required number of hits can be formulated as in Equation 3, where $B$ is the number of bits needed to represent the code, $z_{\alpha/2}$ is the area under the normal distribution and $\beta$ is the tolerance level.

For instance, if the tolerance level required is 10% ($\beta = 0.10$), the confidence level is 97% ($\alpha = (1 - 0.97) = 0.03$) and there are 10 bits of resolution, then 481 760 histogram hits are required.

$$\tau_i = \frac{T_{CLK} \times N_i}{N_{total}} \tag{1}$$

$$H(n) = \frac{\tau_n}{2} + \sum_{i=1}^{n-1} \tau_i \tag{2}$$

$$M = \left(\frac{z_{\alpha/2}}{\beta}\right)^2 \times (2^B - 1) \tag{3}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



### B. Direct Calibration

Alternatively, a TDC can also be calibrated directly using an adjustable delay. With this method, the width of each bin can be characterised manually by adjusting the delay on the input.

The direct calibration process starts by setting the input delay to a value which will result in generation of the Least Significant Bit (LSB) code of the converter. The input delay is gradually increased and by observing the change in each digit of the code, each bin's width in the delay line can be characterised. It should be noted that this method is only usable if the delay generator allows the user to adjust delays smaller than the time value represented by the least significant bit (LSB) of the code. This method can be very exhaustive, especially for large carry chains. Thus, it cannot be considered an ideal calibration method for a typical picosecond resolution TDC. The variable clock generation methods described in [22, 20] are an example of direct calibration.

### C. Double Registration

An alternative approach to compensate for the effects of the non-linearity is the double registration approach, which is a multi-hit technique used for reducing the DNL error affecting the bins [23] by averaging after registering the codes for the same input trigger twice. In this method, the length of the delay line is chosen to be longer than the clock period. Thus, a logic transition for the trigger can be recorded twice, once on each of two consecutive clock edges. The average of these codes is utilised as the final fine code which has improved linearity. If the registered logic transitions for the input are $K_1$, $K_2$ and the clock period is $T_{clk}$, the LSB bin width for the bin can be formulated as $T_{clk}/(K_1 - K_2)$. This method provides fast runtime but does not provide bin-by-bin calibration.

### D. Sliding Scale Technique

Another TDC linearisation method used is called the sliding scale technique. The sliding scale technique is a simple method to average the bin width through the delay line to improve the linearity. In order to find the average bin widths, signals that are asynchronous to the reference signal are used as STOP signals to generate codes [24].

This method aims to generate codes for the same asynchronous pulse in different regions of the delay line and then the average of the generated codes is taken in order to find the average bin widths to improve the linearity.

A few random delay periods are added to the pulses and different codes are generated for the same signal. Once different codes are generated, the delays added to the signals are subtracted from the codes. Thus, the same signal is represented by multiple different codes. It should be noted that the time difference between the START and STOP signals is kept unchanged and separate delay lines are employed for the START and STOP signals. After the added delays are subtracted from the code, the same pulse becomes represented by different codes. Finally, the codes are averaged and an average bin width value is calculated. The diagram for this implementation can be seen in Figure 1.

The main advantage of this method is an improvement in linearity without measuring each bin width inside the delay line, which is significantly faster in terms of the runtime. However, the implementation requires two signal interpolations, START and STOP, and it will introduce a large quantisation error. Even though this method improves the linearity, it does not achieve perfect linearity since every bin is not characterised and the linearity depends on a randomly chosen bin range and randomly delayed signals. With this method, 0.04 LSB DNL was achieved at 17 ps RMS precision in [24].

Depending on the implementation of the differing delays, architectural changes may or may not be required. If the start signal is synchronous to the TDC system clock, then the start time is known precisely and time-scrambling circuitry is required on the stop signal. If the start signal is asynchronous to the TDC system clock, then merely measuring multiple times over will introduce the required random delay. If the start signal is of a higher frequency than the system clock or the scrambler logic can produce two pulses less than a clock period apart, additional decoder circuitry is required to read multiple starts/stops from the delay lines. Reference [24] opts for an asynchronous start signal (explicitly stated) slower than the system clock (implied by the use of a looped Vernier delay line) and so does not need extra circuitry.

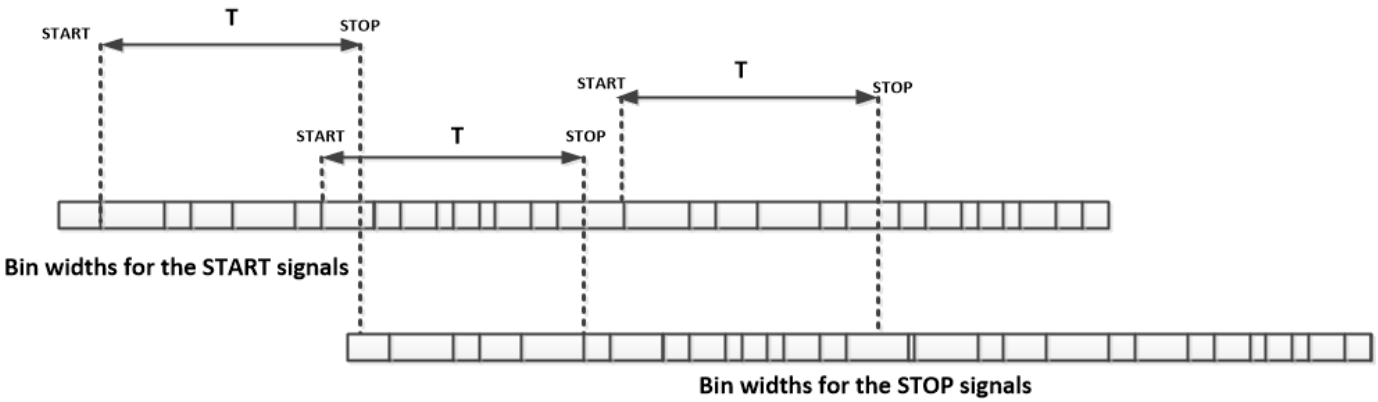



Fig. 1: An illustration of the sliding scale method.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



## III. TDC Architectures

### A. Introduction

In this section, we review new TDC architectures that have not appeared in previous literature reviews. For completeness, a Venn diagram showing the TDC architectures described in this paper and other review literature, classified by three categories (Synchronous, Asynchronous, Differential), is shown in Figure 2. For the architectures not mentioned in this paper, the reader is advised to read previous review literature, most prominently [16].

As a brief overview, the asynchronous methods use asynchronous logic to generate small delays based on the width of a logic element, whereas the synchronous methods operate relative to an oscillator (clock). The differential methods take the difference between two measurements to produce a finer measurement. Some examples would be the delay line, which sequences the smallest delay elements and counts the number that transition asynchronously, the multi-phase clock, which takes multiple different phases of an oscillator and compares them all to sub-divide the oscillator, and the Vernier method, which uses the difference between two logic elements (asynchronous) or two oscillators (synchronous) to obtain finer time resolution.

### B. Successive Approximation TDC

Successive Approximation TDCs (SA TDCs), named due to their derivation from successive approximation Analog-to-Digital Converters (ADCs), operate by delaying the start and stop signals using a variable delay line and comparing which signal exits first, then routing the signal to propagate through a shorter delay line.

Simple linear SA TDCs are relatively straightforward to implement, as each stage of the approximation is a fixed delay line with the propagation delay being half that of the previous stage. However, they subsequently suffer in terms of large area utilisation and poor matching over the course of the TDC due to local process variations. The delay can be stabilised by applying bias voltages derived from a delay-locked loop (DLL) that divides the previous stage's time by two, but this adds extra complexity, and therefore cost, to the circuit.

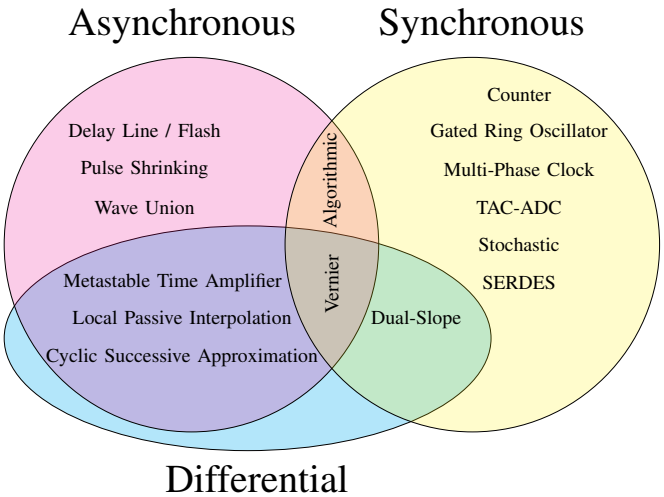



Fig. 2: A Venn diagram of some of the classifications of TDCs.

Therefore, Cyclic SA TDCs (CSA TDCs) have been proposed where the signal is routed repeatedly through the same delay element - a Digital-to-Time Converter (DTC), which has its delay repeatedly halved as the start and stop signals converge. As the same delay elements are being used each time, the effect of local process variation is much smaller, and for the same range and precision, only half the delay elements are needed, as per Equations 4, 5 and 6. This means that the full-scale range of the CSA TDC (without the addition of another level of TDC) is twice the length of the largest generatable delay ($\sum_{i=0}^{\infty}\left(\frac{1}{2^i}\right)=2$).

$$N = \frac{T}{T_{min}} \tag{4}$$

$$\begin{aligned} A_{SA} &= A_{min}\left(\frac{N}{2}+\frac{N}{4}+\ldots+\frac{N}{N}+\frac{N}{N}\right) \\ &\quad + B\left(2A_{mux}+A_{arb}\right) \\ &= A_{min}\left(\frac{N}{N=2^B}+\sum_{i=1}^{B}\left(\frac{N}{2^i}\right)\right) \\ &\quad + B\left(2A_{mux}+A_{arb}\right) \\ &= N*A_{min}+B(2A_{mux}+A_{arb}) \end{aligned} \tag{5}$$

$$\begin{aligned} A_{CSA} &= A_{DTC}+A_{arb}+A_{sel} \\ &= \left(\frac{N*A_{min}}{2}+(B-1)A_{mux}\right) \\ &\quad + A_{arb}+(2A_{mux}+2A_{OR}) \end{aligned} \tag{6}$$

Specifically, Equation 4 describes the number of elements $N$ in the DTC as a function of the full-scale range $T$ and the minimum time resolution $T_{min}$. For simplicity, only a homogeneous DTC (only one type of delay element) is considered in these equations. Equation 5 describes the area of a linear SA-TDC in terms of the area of a minimum-sized delay element $A_{min}$, $N$ as defined in Equation 4, the number of bits of resolution $B$, the area of a multiplexer $A_{mux}$ and the area of an arbitrator (flip-flop, SR latch, current-sense amplifier etc.) $A_{arb}$. It can be seen that the result includes roughly the same number of elements as a simple delay-line TDC, so the linear SA-TDC only benefits when non-homogeneous elements are used (e.g. by adjusting load through capacitors).

Equation 6 shows the area of a CSA-TDC in terms of the area of a DTC $A_{DTC}$, the area of an arbitrator $A_{arb}$ and the area of a selector $A_{sel}$. The DTC only needs to cover half the full-scale range $T$ of the TDC so only needs half the delay elements $\frac{N}{2}$, and then must use $B-1$ multiplexers to enable or disable sections of the DTC. The selector can be composed of 2 multiplexers and two OR gates.

Figure 3 shows the operation of a CSA TDC. The "Arbiter and Selector" block in Figure 3a chooses to forward either A' and B or A' and B' to its outputs depending on whether A' or B arrives first. If A' arrives before B, this implies that the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement

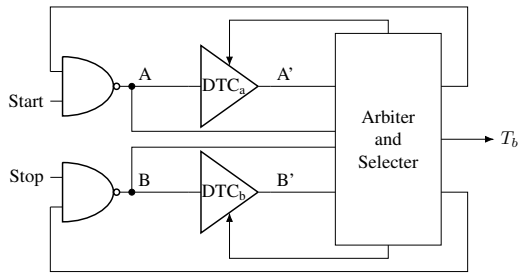


delay between A and B is longer than the period of $DTC_a$ (Digital to Time Converter 'a'), therefore it forwards A' and B to reduce this delay and then halves the delay for the next cycle. If B arrives before A', then the delay between A and B does not exceed $DTC_a$, therefore it forwards A' and B', which have the same delay difference as A and B, so that the delay is maintained for the next round where the delay is once again halved. If A' arrives before B, a '1' is output on $T_b$ when B arrives, otherwise a '0' is output on $T_b$ when B arrives. The A signal can be used to allow double-ended operation (stop before start) or to clear the state of the arbiter for the next round. The TDC here outputs the code "1011001", which is a fractional number with an MSB of 1, resulting in $1 + 0.25 + 0.125 + 0.015625 = 1.390625$, which is the closest number below 1.4.

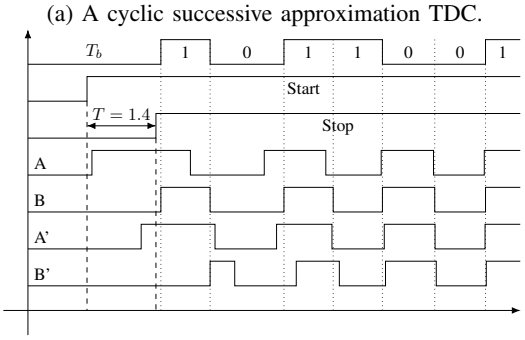
It can be seen that the hierarchical TDC [25] bears a remarkable resemblance to the SA TDC, and in fact can be considered a less efficient form of the SA TDC, as the next stage is triggered twice, whereas the SA TDC only triggers the next stage once. Also, as the hierarchical TDC does not choose between the delayed and non-delayed versions of the signals, some conditional bit flipping is needed on the outputs which is not needed in the SA TDC.

The asynchronous pipelined TDC demonstrated in [26] is also a form of successive approximation TDC. However, since the aim is to quantify pulse time (rising edge to falling edge), the residue is formed by finding the dead time or overlap between the signal and the delayed version of the same signal. If the signal overlaps it's delayed version, then the period of the signal is longer than the delay, otherwise it is shorter. The residue is the quantity by which it overlaps or misses the delayed version, and is then quantised by an exponentially shorter delay. The authors of [26] achieved a resolution of 200 ps due to the dead zone of the residue generator, which was shown to be 189.7 ps.

Similarly to Local Passive Interpolation (LPI) TDCs (see Henzler [16]), SA TDCs are relatively new in the current literature, with more than half of the papers published by Mäntyniemi et al. [27, 28, 29]. These papers show a TDC operating at up to 610 fs resolution with a 5 ns range (or 1.21 ps resolution with a 328 us range) using a switched capacitor array (and a Voltage-Controlled Oscillator (VCO) for the 328 us range) for the Digital-to-Time Converter (DTC), which is explained in more detail in [30]. Building on this, Chung et al. [31] propose unrolling the SA loop in order to increase sample rates. Using 65 nm CMOS (compared with 350 nm in [29]), 80MS/s was achieved, compared to 5MS/s in [29]. However, due to the inferior switched-capacitor implementation, [31] only managed a 9.77 ps resolution. [32] presents a technique one might call a linear SA TDC, in that it linearly increases the delay until the two signals align. However, as it has no signal recovery, duplication or residue, it requires multiple samples of the input signal before it can detect the correct time difference, which is not tolerable in many applications. Also, this system exhibits a 474 ps resolution, which is well behind even delay line implementations available in 2016 (17 ps in [32]), when this paper was written. [33, 34] also present a linear (unrolled) implementation of the SA-TDC, achieving 25 ps and 12.5 ps respectively on 180 nm.




(a) A cyclic successive approximation TDC.




(b) Waveform of a CSA TDC.

Fig. 3: (a) Block diagram and (b) waveform of a CSA TDC.

### C. Algorithmic TDC

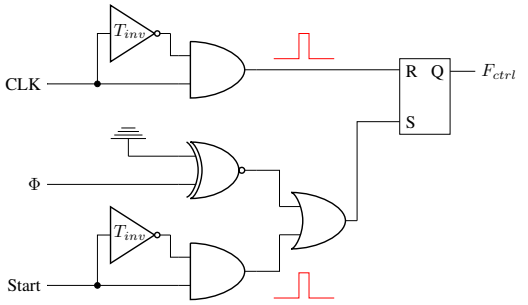
Algorithmic TDCs, first proposed by Keranen and Kostamovaara in [35] and used again in [36], are functionally similar to CSA TDCs (see Section III-B). However, at each stage of the successive approximation, instead of looping the residue back round and reducing the delay exponentially, it amplifies the residue exponentially and re-quantises it with the same delays.

Keranen's paper uses a scheme similar to a dual-slope TAC, but instead of increasing and decreasing the amplitude, it increases the phase of a ring oscillator at two different speeds. The number of 'fast' oscillations between the start and stop (system clock edge) are counted, and then the oscillator is switched to its 'slow' mode. The time taken for the oscillator to reach a full oscillation (phase is zero) will be dependent on the quantisation residue of the counter process, and will be amplified by a ratio of $\frac{F_{fast}}{F_{slow}}$, where $F_{fast}$ is the frequency in 'fast' mode, and $F_{slow}$ is the frequency in 'slow' mode.

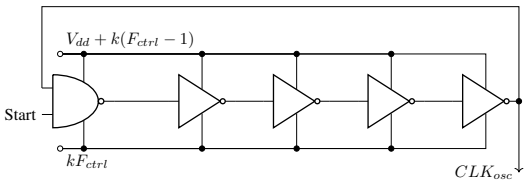
Figure 4c shows the wave trace for an algorithmic TDC. The ring oscillator starts oscillating at a high frequency (e.g. $F_{fast} = 6 \times F_{clk}$) when the trigger signal transitions from 0-1 (first dashed line, red) and oscillates until the next clock edge (second dashed line, blue). At this point the value of the M counter (which counts ring oscillator periods) is sampled to produce the first residue. Then, the ring oscillator is switched to a low frequency (e.g. $F_{slow} = 2 \times F_{clk}$) and the N counter (which counts whole clock periods) is started. This runs until the ring oscillator wraps around to $\Phi = 0$ at which point the N counter is sampled to produce the next residue and the counter is set back to the high frequency. At each stage, the algorithmic TDC is amplifying and quantising the residue from

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement

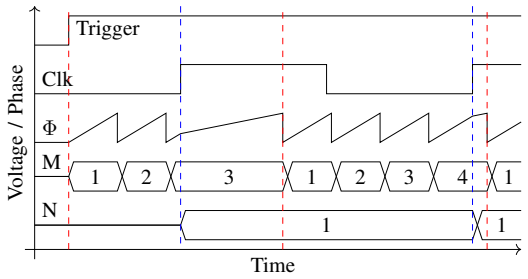





(a) Frequency Control.




(b) Ring Oscillator.




(c) Wave trace for a sample conversion based on [35] (residue = 38% of a clock period).

Outputs (M, N, M, N, ...) are 3, 1, 4, 1, ....

Fig. 4: Algorithmic TDC.

the previous stage through the change of the ring oscillator's frequency. If $F_{slow}$ were to be slower than $F_{clk}$, it would be possible to reach $N > 1$ and also increase the amplification at each stage, at the expense of longer conversion times.

In [36], a second oscillator is started in fast mode while the first is in slow mode to quantise the amplified residue, and then the first oscillator is used to quantify the second amplified residue (etc.). On the other hand, in [35], the system clock is used to quantify the amplified residue, and then a further residue is generated from the time between the oscillator reaching zero phase and the next system clock edge, which is quantified using the same method as the original pulse (using the oscillator in fast mode to quantify, then switching to slow mode to amplify).

### *D. Wave Union Launchers*

In [23], Wu and Shi propose a method of improving precision past the gate delay: the wave union TDC. Rather than dispatching one edge per trigger and quantising this edge, the authors suggest dispatching multiple edges and quantising all of them by a method similar to the gated ring oscillator (GRO), but without the need for more than one input sample.

The authors suggest two methods for doing this. The first (type A) is to store a wavelet inside a delay line and release it on incidence of a trigger. When the stop signal occurs, the wavelet is held in place and quantised. Each edge in the wavelet is individually quantised and the edges are then combined to give a more accurate measurement of the original trigger position. This is referred to as an FSR (finite step response) wave union launcher.

Figure 5 shows the design of an FSR wave union TDC. The first M bins are used to store the FSR pulse and for quantisation, with the remaining N bins being used solely for quantisation. In [23], M was 16 bins (with the distance between edges in the FSR being 13 bins), while N was 48 (i.e. the delay line was 3 times the length of the FSR storage).

The second method (type B) is to attach a startable ring oscillator to the front of the delay line. The trigger signal starts the ring oscillator, which then oscillates for a number of cycles before stopping. This is referred to as an ISR (infinite step response). The oscillations happen over multiple system clock (stop) cycles.

In the type B wave union TDC, shown in Figures 6a and 6b, the period of the oscillator must not be too similar to the period of the system clock so that the sampling process does not repeatedly hit the same large bin (as this would result in a large DNL). However, this means that there will be cases where ring oscillator edges will not be seen once. The authors of [23] identify 3 possible cases: U, V and W patterns, corresponding to jumps of 0, 1 and 2 ring oscillator periods. The jump type is determined from the output values of the priority encoder:

- For a value in the range $3N/4 \rightarrow N$ followed by a value in the range $N/4 \rightarrow N/2$, this implies both signals were the same ring oscillator edge (based on the operation of the priority encoder) and hence is a case of the U pattern.
- For a value in the range $N/4 \rightarrow N/2$ followed by a value in the range $3N/4 \rightarrow N$, this implies that a ring oscillator edge has been missed, and hence is a case of the W pattern. This will only happen if the ring oscillator is faster than the clock period (meaning an edge can pass between two samples).
- All other jumps are classified as V patterns, and are indicative of the standard operation of the TDC.

The first method is able to increase the accuracy quite significantly, from 165 ps per bin worst case and 60 ps per bin average case (in the original TDC), to 65 ps per bin worst case and 30 ps per bin best case. It does this without significantly increasing the dead time (2.5 ns to 5 ns), but does increase the decoding complexity due to increasing the number of edges to be decoded per output (although this was performed on a computer in the original paper). The second method was measured through the RMS error of measuring a fixed time difference, and resulted in an improvement from 40 ps to 10 ps for 16 measurements (in comparison to 25 ps RMS for the FSR method), albeit at an 18 times dead time increase (2.5 ns to 45 ns). This is summarised in Table I.

Subsequently, the authors of [37] made use of the wave union TDC and managed a 1.8 times improvement on the bins inside their Virtex 4 FPGA from 16 ps RMS to 9 ps RMS.

In [38], Hu et al. suggest a Stepped-Up Tree Encoder (SUTE) to efficiently encode the edges on a Virtex 4 FPGA in the presence of bubbles and the non-thermometer code

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



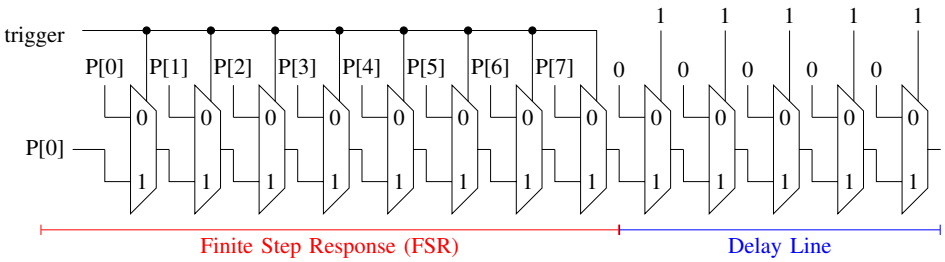
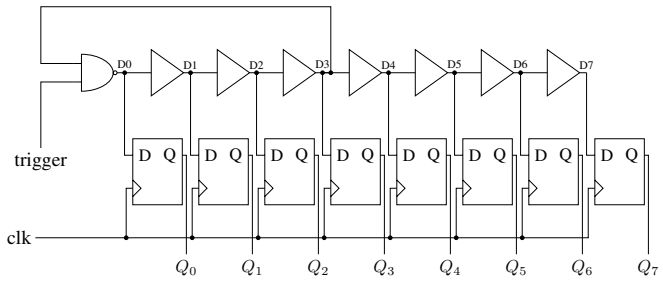
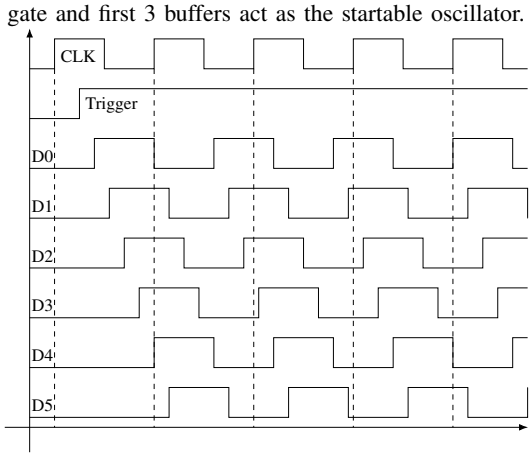



Fig. 5: Initial section of a wave union launcher using multiplexers (the delay line continues further).




(a) Example of a type B (ISR) wave union launcher. The NAND gate and first 3 buffers act as the startable oscillator.




(b) Waveform of a type B wave union launcher where $F_{CLK} > F_{OSC}$.

Fig. 6: (a) Gate-level implementation and (b) waveform of a Type-B wave union launcher.

presented by the type A wave union TDC. The encoder uses a pre-processing stage capable of removing single-bit bubbles (e.g. 0000 1011 1111) which encodes the position of the $0 \rightarrow 1$ edge in subgroups of 4 bits, plus a flag to determine if the transition occurs in that subgroup and a flag to determine if a transition happens on the border of subgroups.

The 4-wide grouping suppresses the single-bit bubbles and hence allows the resultant outputs to be sent to an array of standard priority encoders for encoding via some switching

| Method | Mean Bin | Worst Bin | RMS Error | Dead Time |
|---|---|---|---|---|
| Delay line | 60 ps | 165 ps | 40 ps | 2.5 ns |
| Type A (FSR) | 30 ps | 65 ps | 25 ps | 5 ns |
| Type B (ISR) | – | – | 10 ps | 45 ns |

TABLE I: Performance of the wave union TDCs in [23].

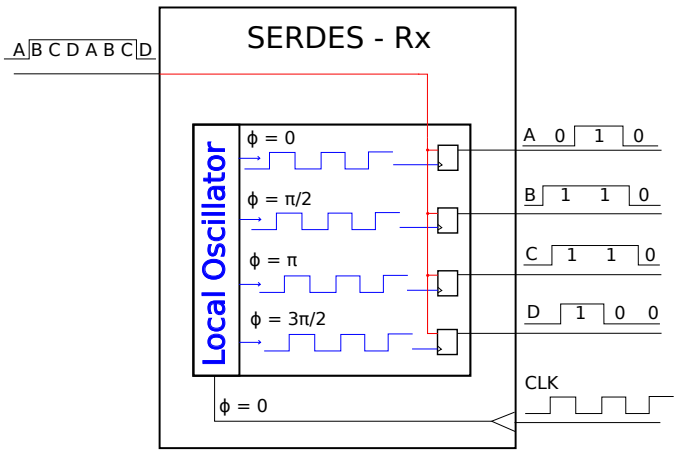



Fig. 7: A SERDES TDC with 4 x interpolation.

multiplexers which distribute the edges to the encoders. This ensures that multiple edges can be encoded in a single clock cycle, and the maximum number of edges is determined by the number of terms in the FSR (wavelet generator).

### *E. SERDES TDC*

When operating on an FPGA, serialiser deserialiser (SERDES) blocks can be used to create uniform delay elements to form high resolution fine time interpolation TDCs. SERDES are generally used in high speed communication applications where the input/output (I/O) channels are limited. The transmitter's parallel input is serialised using a high speed clock. At the receiver, the data is deserialised to the original parallel format. In other words, SERDES blocks have lower data rates at the input, they conduct the transmission at a faster clock frequency and have the lower data rate again at the output. As a result the I/O required for the transmission is minimised and no data is lost during transmission due to the faster data rate. Modern FPGAs offer SERDES blocks which can provide 10 times clock multiplication and so 10 times faster serialisation. Since SERDES blocks are uniform chains of shift registers which are synchronised with a high speed clock throughout the transmission, they provide high resolution fine time quantisation. As described in [39], a SERDES based 96-channel TDC was implemented on two Altera Stratix EP1S30F780C6 FPGAs which achieved a 1.2 ns resolution.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



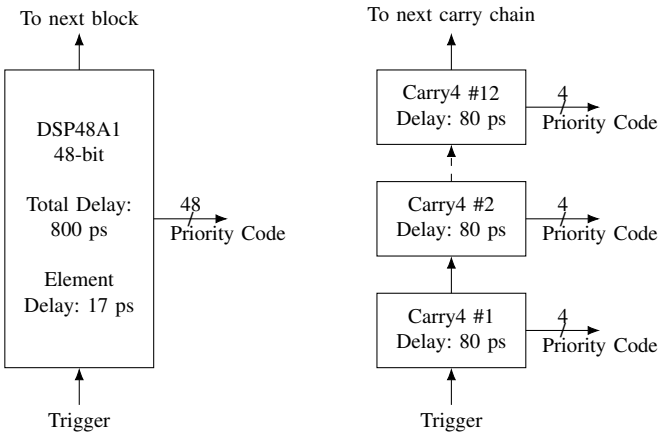



Fig. 8: A DSP delay line compared to a carry chain.

### *F. DSP Delay Line*

In 2018, Tancock et al. published a paper on implementing delay lines in DSP blocks on an FPGA [40]. Conventional TDCs on FPGAs utilise Look-Up Tables (LUTs) or carry chains built into the FPGA fabric to generate small delays. However, as this logic is configurable, the fan-out and on-resistance of the elements is much higher than dedicated logic, resulting in sub-optimal results. The on-chip DSP blocks (DSP48A1) contain dedicated carry logic for the 48-bit adder, so it was suggested that this logic could be used to generate more optimal delays. While the total delay of a DSP block was less than the equivalent number of carry elements in the general-purpose fabric (Figure 8), the elements were severely out-of-order and the majority of the delay fell into a single large bin at the boundary of DSP blocks.

Subsequently, in 2019, Tancock and Dahnoun published a follow-up paper detailing the use of a population counter and starting offsets to compensate for the nature of the DSP blocks [41]. The population counter relies on the monotonic increase of the number of bins in the '1' state (from the '0' state) to effectively re-order the bins into a linearly increasing sequence. Then, the initial offsets on 4 parallel delay lines allow each DSP block to cover for a third of the large bin present in each of the others, with the codes being summed to produce the final output code. On the newer Artix-7 architecture (DSP48E1 blocks), the authors achieved 5.25 ps resolution, compared to approximately 20 ps that would be achieved with carry chains or 10 ps for 4 parallel carry chains.

## IV. Performance

Discussion of various architectures' merits and demerits is, unfortunately, insufficient to make a decision on which architecture is best for a particular use case. Hence, this section analyses a portion of TDCs available in current literature, showing the achieved performance in each case as well as the architecture and process technology used. Table II displays key performance metrics from a number of recent (last 20 years) papers on time-to-digital converters. The table is sorted by resolution, as this is arguably the most important metric for a TDC, but it also includes information on process technology, integral and differential non-linearity, single-shot precision, number of channels, and the architecture used.

For many implementations, such as the wave union method, the only appropriate measure of resolution is the Single-Shot Precision (SSP), so for these papers the resolution and SSP are equivalent (SSP is 1 LSB). For other papers, there is a distinct difference between resolution (which defines the quantisation noise floor, and is the minimal discernible difference between two values) and single-shot precision (which is affected by other aspects such as clock jitter, voltage variation and temperature variation, and is the standard deviation of measurements of a single time pulse).

In many cases, the SSP is not measured or stated, whereas some measure of resolution is always available, hence the choice of resolution as the main figure of merit. Resolution will always be a lower bound for precision, but the precision may be higher for the aforementioned reasons.

While a high internal DNL and INL are beneficial to multiple hit or multiple registration methods (such as the wave union method), a high DNL or INL at the output (the value which is stated in Table II) implies a loss of precision even after applying these methods.

Not all information can be expressed in such a table, and so exceptions worthy of note are as follows: [68], [60] and [50] are the only papers in the table that do not use CMOS, using an unspecified FPGA, a $0.8\mu m$ BiCMOS process and an unspecified ECL process respectively. [70], [66] and [64] are unique in that they also integrate arrays of single-photon avalanche photodiode (SPAD) pixels on the same chip, with either a one-to-one or one-to-many matching between TDC and SPAD, thereby incorporating an entire depth-mapping system onto a single chip.

[65], [57] and [52] are also worthy of mention, as they use multi-dimensional schemes to reduce area requirements. The former arranges its pulse-shrinking elements into a two-dimensional grid, with row and column decoders being used to ascertain the position at which the pulse was extinguished, and the latter two employ a scheme of splitting their delays into a sequential set (e.g: 1, 2, ..., 8) which operates on each column, and a sparse set (e.g: 1, 9, 17, ...) which operates on the rows, with the arbiters comparing the two delayed signals to each other, as opposed to a delayed signal against an undelayed signal. Finally, the usage of switched capacitor arrays in [29] and [27] and resistive dividers in [46] and [47] shows how analog components can be used to great effect while still exhibiting technology scaling improvements.

## V. Architecture Comparison

It can be seen from Table II that the main trade-off many designs make is between conversion time, resolution and range. Stochastic and metastable time amplifier systems are both similar in that they sacrifice their range to increase their resolution and conversion rate. This makes them excellent for systems that have events happening very quickly (such as short-range time-of-flight (ToF)) or close to a known reference (such as frequency synthesis), but makes them bad for applications that require a large dynamic range, such as

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



| Method | Technology* | Resolution (ps) | DNL (LSB) | INL (LSB) | SSP (LSB) | Channels | Ref |
|---|---|---|---|---|---|---|---|
| Algo TDC | 350 | 0.61 | ±0.4 | ±4.5 | ±1.2 | 1 | [36] |
| CSA-TDC + Counter | 350 | 0.61 | N/A | N/A | N/A | 1 | [29] |
| STDC | 130 | 0.7 | ±1.4 | ±2.4 | N/A | 1 | [42] |
| Branching CRO | 65 | 0.85 | ±0.27 | ±2.94 | 1 | 1 | [43] |
| TAC-ADC | N/A | 1 | N/A | ±10 | 1 | 1 | [42] |
| CSA-TDC + Counter | 350 | 1.2 | N/A | ±6.67 | 3 | 1 | [44] |
| DL + TA + DL | 90 | 1.25 | ±0.8 | ±3 | 1 | 1 | [45] |
| Algo TDC | 350 | 2 | N/A | ±1.25 | ±0.15 | 1 | [35] |
| Looped LPI-TDC | 90 | 4.7 | ±0.6 | ±1.2 | 0.7 | 1 | [46] |
| Looped LPI-TDC | 90 | 4.7 | ±0.5 | ±1.0 | N/A | 1 | [47] |
| Wave Union A | FPGA | 6 | N/A | N/A | 1 | 48 | [37] |
| GRO | 130 | 6 | N/A | N/A | N/A | 1 | [48] |
| VDL + DL + Counter | 180 | 10 | N/A | N/A | N/A | 1 | [49] |
| Wave Union B | FPGA | 10 | N/A | N/A | 1 | 8 | [23] |
| TAC-ADC + Counter | ECL | 10 | N/A | ±2 | 1.5 | 1 | [50] |
| TA + DL | 180 | 11.25 | N/A | N/A | 1.33 | 1 | [51] |
| Flash (2D) + CRO + Counter | 350 | 12.2 | N/A | ±0.41 | 0.66 | 1 | [52] |
| Vernier SA-TDC | 180 | 12.5 | ±0.4 | ±0.4 | N/A | 1 | [34] |
| Looped ps | 800 | 20 | ±0.5 | N/A | 1 | 1 | [53] |
| TA + SA-TDC | 90 | 20 | N/A | N/A | N/A | 8 | [54] |
| DDL + Counter | 90 | 21 | ±0.7 | ±0.7 | N/A | 1 | [55] |
| VDL + CRO + Counter | 350 | 24 | ±0.55 | ±1.5 | N/A | 1 | [56] |
| Flash (2D) + CRO + Counter | 600 | 30 | N/A | ±1.33 | 32 | 1 | [57] |
| VDL | 700 | 30 | N/A | ±1.0 | 0.2 | 1 | [58] |
| Hierarchical TDC | 90 | 31.25 | N/A | N/A | N/A | 1 | [59] |
| Dual-Slope TAC + Counter | 800 | 32 | N/A | ±0.16 | 0.94 | 1 | [60] |
| DL + Counter | 130 | 40 | N/A | N/A | N/A | 1 | [61] |
| CSA-TDC + CRO + Counter | 350 | 42 | N/A | N/A | N/A | 1 | [62] |
| GRO | 130 | 45 | N/A | N/A | N/A | 1 | [63] |
| CRO + Counter | 130 | 50 | ±0.5 | ±2.4 | N/A | 1024 | [64] |
| PS (2D Array) | 800 | 50 | N/A | ±3.5 | N/A | 1 | [65] |
| CRO + Counter | 130 | 55 | ±0.3 | ±2.5 | N/A | 20480 | [66] |
| Wave Union A | FPGA | 60 | +1.17 | ±1.08 | 0.42 | 1 | [23] |
| CRO + Counter | 180 | 61 | ±0.23 | ±0.3 | 1 | 24 | [67] |
| VDL + DL + Counter | FPGA | 75 | N/A | N/A | 0.53 | 1 | [68] |
| CRO | 65 | 80 | N/A | N/A | N/A | 1 | [69] |
| DDL + CRO + Counter | 350 | 97 | ±0.09 | ±1.89 | N/A | 32 | [70] |
| TAC-ADC + Counter | 500 | 312.5 | ±0.2 | ±0.3 | 0.32 | 1 | [71] |
| CRO | 800 | 530 | ±0.36 | ±0.36 | N/A | 1 | [72] |
| SERDES, 2 chips x 48 channels | FPGA | 1200 | ±0.167 | N/A | ±0.5 | 48x2 | [39] |

TABLE II: Comparison of TDCs in the reviewed literature. N/A = Not Available. * CMOS ASICs in nm, FPGAs by series number.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIM.2019.2936717, IEEE Transactions on Instrumentation and Measurement



| Method | Merits | Demerits |
|---|---|---|
| Successive Approximation | • Area-efficient for an asynchronous design.<br>• Variable delay architecture. | • Asynchronous path is difficult to design.<br>• ASIC only. |
| Algorithmic | • Very small area.<br>• High resolution. | • Long dead time (multiple clock cycles). |
| Wave Union | • Low area penalty for up to 1 order of magnitude improvement. | • Design of decoder is difficult and increases area utilisation. |
| SERDES | • Order of magnitude increase without using general FPGA fabric.<br>• Easy to use. | • Uses high-speed communications resources, which may be needed elsewhere. |
| DSP Delay Line | • Higher resolution than carry chains with few changes.<br>• Can be used alongside carry chains for higher channel numbers. | • Not as many DSP resources as carry chains.<br>• Need multiple cascaded to account for DNL.<br>• Requires population counter. |

TABLE III: Merits and demerits of the TDCs reviewed here.

long-range ToF systems. However, due to their high count rate and resolution, they are also useful as the lowest level in a multi-level system, where they provide the least significant bits while leaving the more significant bits to other methods.

Vernier, pulse-shrinking, dual-slope time amplifier and, to a lesser extent, successive approximation and algorithmic systems instead decide to sacrifice conversion rates and area for better range and resolution. This is excellent for systems with a low repetition rate or where the repetition rate can be controlled (such as long-range ToF), but suffers when a high repetition rate (such as short-range ToF or quantum key distribution) is required, as often the only option is to employ an interpolation or pipelining scheme which can massively hurt area efficiency.

Delay line, controlled ring oscillator and gated ring oscillator methods avoid low count rates and low range, but suffer in terms of resolution, meaning they are often a good choice either as a mid or upper level of a multi-level TDC, or in the case where the application does not require high precision, such as for low-rate frequency synthesis, long-distance low resolution time of flight and quantum key distribution with low dead count rates. The GRO method can also suffer from some signal integrity issues in low count rate systems, but excels when measuring the same time period multiple times over due to its first order noise shaping.

TAC-ADCs and local passive interpolation methods perform very well in all three areas, but suffer from a lack of technology scaling in the TAC-ADC's case as well as signal integrity and area efficiency problems. If an LPI TDC were extended to its logical extreme with a large quantity of resistors in its potential divider, it could probably achieve much higher resolutions than shown in Table II, although the area utilisation would increase exponentially due to the number of resistors needed.

Flash and Wave Union TDCs are highly configurable, with high resolutions and ranges available at the expense of area and conversion time, making them excellent as a mid or low-level section of a system, although they do not achieve the same resolutions as stochastic, time amplification, vernier or local passive interpolation methods.

## VI. Conclusions and Recommendations

In conclusion, time to digital conversion has developed many approaches over the last 2 decades, each of which has its own unique characteristics. When measuring the same signal many times over, such as with frequency locking applications or high-resolution low-speed surface mapping, it is worth employing a gated ring oscillator for its first order (and higher order when multiple are used together) noise shaping. If the conversion rate of the target system is of little concern then, depending on area constraints, utilising looped Vernier or pulse shrinking methods is advised, as the analog components in dual-slope systems do not scale well with technology.

Beyond this, the systems that have been shown to perform best are multi-level systems that exploit the benefits of multiple architectures while covering the weaknesses with the others. Most notably, SA-TDCs are delay-element agnostic, meaning they can incorporate a large variety of delay generation methods to assist in obtaining the correct range and resolution, and, at each stage, also output the residue - the difference between the measured and actual value of the time difference, which can then be passed directly to a higher resolution TDC. If a small-enough residue can be obtained at the final output of the SA-TDC, we suggest utilising either a stochastic or metastable time amplification method be used to obtain optimal accuracy. Similarly, if a CSA-TDC were employed, a time amplifier could be switched in as the system approaches the lowest bits to amplify the time difference and hence reduce the requirements for small delays.

Methods that use traditional analog components in a way that allows them to scale, such as local passive interpolation and switched capacitor arrays (as seen in the CSA-TDC papers) allow for very small time differences typically not seen in digital methods. However, these systems require careful choice of components and layout to minimise non-linearity and interference from other components, and often require large areas of the layout (although not as much as other analog methods). Hence, they are worth consideration if the expertise and design constraints allow for such an approach.

When constrained to FPGAs for the underlying technology, the only options often available are delay line, stochastic and wave union TDCs. For resolutions of as high as 10 ps, this can be achieved with delay lines (sometimes requiring averaging between many) on their own. If the required range is less than 100 ps, stochastic TDCs may be an option depending on the device size and metastability window of the discriminators (normally D-type flip-flops or latches). Otherwise, wave union TDCs are the only option, and care must be taken to optimise the design of the encoder to reduce its area requirements. If a low count rate is acceptable (relative to the system clock), a type B wave union TDC will be optimal, otherwise a type A will be required.

## REFERENCES


[1] E. Arabul, J. Rarity, and N. Dahnoun, "FPGA based fast integrated real-time multi coincidence counter using a time-to-digital converter," *2018 7th Mediterranean Conference on Embedded Computing (MECO)*, pp. 1–4, 2018.

[2] "Time-of-flight fundamentals," Nov 2013. [Online]. Available: https://msr.dom.wustl.edu/time-of-flight-fundamentals/

[3] K. Naresh, "Applications of fluorescence spectroscopy," *National Level Workshop on Spectroscopic Techniques in Structural Elucidation Journal of Chemical and Pharmaceutical Sciences*, 2014. [Online]. Available: https://www.jchps.com/specialissues/Specialissue5/05jchpssi5knaresh18-21.pdf

[4] M. Wahl, "Time-correlated single photon counting," 2014. [Online]. Available: https://www.picoquant.com/images/uploads/page/files/7253/technote_tcspc.pdf

[5] P. Vines, K. Kuzmenko, J. Kirdoda, D. C. Dumas, M. M. Mirza, R. W. Millar, D. J. Paul, and G. S. Buller, "High performance planar germanium-on-silicon single-photon avalanche diode detectors," *Nature communications*, vol. 10, no. 1, p. 1086, 2019.

[6] OSI Optoelectronics. (2013) 1.25Gbps Silicon Photodiodes. [Online]. Available: http://osioptoelectronics.com/standard-products/silicon-photodiodes/high-speed-silicon-photodiodes/1-25gbps-photodiodes.aspx

[7] D. Parker, R. Forster, P. Fowles, and P. Takhar, "Positron emission particle tracking using the new birmingham positron camera," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 477, no. 1, pp. 540 – 545, 2002, 5th Int. Conf. on Position-Sensitive Detectors. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900201019192

[8] "Tdc7201 (active)." [Online]. Available: http://www.ti.com/product/TDC7201

[9] J. Smith, "Time tagger series." [Online]. Available: https://www.swabianinstruments.com/time-tagger/

[10] P. GmbH, "Home." [Online]. Available: https://www.picoquant.com/products/category/tcspc-and-time-tagging-modules

[11] "Id900 time controller." [Online]. Available: https://www.idquantique.com/single-photon-systems/products/id900-time-controller/

[12] D. I. Porat, "Review of Sub-Nanosecond Time-Interval Measurements," *IEEE Transactions on Nuclear Science*, vol. 20, no. 5, pp. 36–51, Oct 1973.

[13] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," *Metrologia*, vol. 41, no. 1, p. 17, 2004. [Online]. Available: http://stacks.iop.org/0026-1394/41/i=1/a=004

[14] M. Zieliński, "Metrology and measurement systems review of single-stage time-interval measurement modules implemented in fpga devices," *Metrology and Measurement Systems*, vol. 16, 01 2009.

[15] P. Napolitano, A. Moschitta, and P. Carbone, "A survey on time interval measurement techniques and testing methods," in *2010 IEEE Instrumentation Measurement Technology Conference Proceedings*, May 2010, pp. 181–186.

[16] S. Henzler, *Time-to-digital converters*. Springer Science & Business Media, 2010, vol. 29.

[17] Z. Wang, C. Huang, and J. Wu, "A REVIEW OF CMOS TIME-TO-DIGITAL CONVERTER," *Journal of Circuits, Systems and Computers*, vol. 23, no. 07, p. 1430001, 2014. [Online]. Available: https://doi.org/10.1142/S0218126614300013

[18] D. Chaberski, R. Frankowski, M. Gurski, and M. Zieliński, "Comparison of Interpolators Used for Time-Interval Measurement Systems Based on Multiple-Tapped Delay Line," *Metrology and Measurement Systems*, vol. 24, 01 2017.

[19] M. W. Fishburn and E. Charbon, "Statistical Limitations of TDC Density Tests," in *In Proc. IEEE Nuclear Science Symposium (NSS)*, October 2012.

[20] J. Wu, "Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs," *IEEE Transactions on Nuclear Science*, vol. 57, no. 3, pp. 1543–1548, June 2010.

[21] M. Mota and J. Christiansen, "A high-resolution time interpolator based on a delay locked loop and an RC delay line," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1360–1366, Oct 1999.

[22] K. Katoh and K. Namba, "A low area calibration technique of TDC using variable clock generator for accurate on-line delay measurement," in *Sixteenth International Symposium on Quality Electronic Design*, March 2015, pp. 430–434.

[23] J. Wu and Z. Shi, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay," in *2008 IEEE Nuclear Science Symposium Conference Record*, Oct 2008, pp. 3440–3446.

[24] B. Markovic, S. Tisa, F. A. Villa, A. Tosi, and F. Zappa, "A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 557–569, March 2013.

[25] A. S. Yousif and J. W. Haslett, "A fine resolution TDC architecture for next generation PET imaging," *IEEE Transactions on Nuclear Science*, vol. 54, no. 5, pp. 1574–1582, 2007.

[26] O. C. Akgun, "An Asynchronous Pipelined Time-to-Digital Converter Using Time-Domain Subtraction," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–5.

[27] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A CMOS Time-to-Digital Converter (TDC) Based On a Cyclic Time Domain Successive Approximation Interpolation Method," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3067–3078, Nov 2009.

[28] S. Alahdab, A. Mäntyniemi, and J. Kostamovaara, "Cyclic time domain successive approximation time-to-

digital converter (TDC) with sub-ps-level resolution," in *2011 IEEE International Instrumentation and Measurement Technology Conference*, May 2011, pp. 1–4.

[29] S. Alahdab, A. Mäntyniemi, and J. Kostamovaara, "A time-to-digital converter (TDC) with a 13-bit cyclic time domain successive approximation interpolator with sub-ps-level resolution using current DAC and differential switch," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2013, pp. 828–831.

[30] S. Alahdab, A. Mäntyniemi, and J. Kostamovaara, "A 12-bit digital-to-time converter (DTC) with sub-ps-level resolution using current DAC and differential switch for time-to-digital converter (TDC)," in *2012 IEEE International Instrumentation and Measurement Technology Conference Proceedings*, May 2012, pp. 2668–2671.

[31] H. Chung, H. Ishikuro, and T. Kuroda, "A 10-Bit 80-MS/s Decision-Select Successive Approximation TDC in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1232–1241, May 2012.

[32] R. Jiang, C. Li, M. Yang, H. Kobayashi, Y. Ozawa, N. Tsukiji, M. Hirano, R. Shiota, and K. Hatayama, "Successive approximation time-to-digital converter with vernier-level resolution," in *2016 IEEE 21st International Mixed-Signal Testing Workshop (IMSTW)*, July 2016, pp. 1–6.

[33] D. Kościelnik, M. Miśkowicz, J. Szyduczyński, and D. Rzepka, "Optimizing time-to-digital converter architecture for successive approximation time measurements," in *2013 IEEE Nordic-Mediterranean Workshop on Time-to-Digital Converters (NoMe TDC)*, Oct 2013, pp. 1–8.

[34] D. Kościelnik, J. Szyduczyński, D. Rzepka, W. Andrysiewicz, and M. Miśkowicz, "Optimized design of successive approximation time-to-digital converter with single set of delay lines," in *2016 Second International Conference on Event-based Control, Communication, and Signal Processing (EBCCSP)*, June 2016, pp. 1–8.

[35] P. Keränen and J. Kostamovaara, "Algorithmic time-to-digital converter," in *2013 NORCHIP*, Nov 2013, pp. 1–4.

[36] P. Keränen and J. Kostamovaara, "A Wide Range, 4.2 ps(rms) Precision CMOS TDC With Cyclic Interpolators Based on Switched-Frequency Ring Oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 12, pp. 2795–2805, Dec 2015.

[37] E. Bayer and M. Traxler, "A High-Resolution (¡ 10 ps RMS) 48-Channel Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA)," *IEEE Transactions on Nuclear Science*, vol. 58, no. 4, pp. 1547–1552, Aug 2011.

[38] X. Hu, L. Zhao, S. Liu, J. Wang, and Q. An, "A Stepped-Up Tree Encoder for the 10-ps Wave Union TDC," *IEEE Transactions on Nuclear Science*, vol. 60, no. 5, pp. 3544–3549, Oct 2013.

[39] M. Bogdan, H. Frisch, M. Heintz, A. Paramonov, H. Sanders, S. Chappa, R. DeMaat, R. Klein, T. Miao, P. Wilson, and T. J. Phillips, "A 96-channel fpga-based time-to-digital converter (tdc) and fast trigger processor module with multi-hit capability and pipeline," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 554, no. 1, pp. 444 – 457, 2005.

[40] S. Tancock, E. Arabul, N. Dahnoun, and S. Mehmood, "Can DSP48A1 adders be used for high-resolution delay generation?" in *2018 7th Mediterranean Conference on Embedded Computing (MECO)*, June 2018, pp. 1–6.

[41] S. Tancock and N. Dahnoun, "A 5.25ps-resolution TDC on FPGA using DSP blocks," in *Proceedings of the Digital Image & Signal Processing'19 conference*. Springer, 10 2018.

[42] V. Kratyuk, P. K. Hanumolu, K. Ok, U. K. Moon, and K. Mayaram, "A Digital PLL With a Stochastic Time-to-Digital Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 8, pp. 1612–1621, Aug 2009.

[43] J. S. Teh, L. Siek, A. M. Alonso, A. Firdauzi, and A. Matsuzawa, "A 14-b, 850fs Fully Synthesizable Stochastic-Based Branching Time-to-Digital Converter in 65nm CMOS," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–5.

[44] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3067–3078, 2009.

[45] M. Lee and A. A. Abidi, "A 9b, 1.25ps Resolution Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue," in *2007 IEEE Symposium on VLSI Circuits*, June 2007, pp. 168–169.

[46] S. Henzler, S. Koeppe, W. Kamp, H. Mulatz, and D. Schmitt-Landsiedel, "90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2008, pp. 548–635.

[47] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "Variation tolerant high resolution and low latency time-to-digital converter," in *ESSCIRC 2007 - 33rd European Solid-State Circuits Conference*, Sept 2007, pp. 194–197.

[48] C. M. Hsu, M. Z. Straayer, and M. H. Perrott, "A Low-Noise Wide-BW 3.6-GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec 2008.

[49] V. Ramakrishnan and P. T. Balsara, "A wide-range, high-resolution, compact, CMOS time to digital converter," in *19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems Design (VLSID'06)*, Jan 2006.

[50] K. Maatta and J. Kostamovaara, "A high-precision time-to-digital converter for pulsed time-of-flight laser radar

applications," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, no. 2, pp. 521–536, Apr 1998.

[51] M. Safi-Harb and G. W. Roberts, "Embedded Narrow Pulse Measurement in Digital CMOS," in *2006 IEEE Instrumentation and Measurement Technology Conference Proceedings*, April 2006, pp. 1195–1200.

[52] J. P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, June 2006.

[53] S. Tisa, A. Lotito, A. Giudice, and F. Zappa, "Monolithic time-to-digital converter with 20ps resolution," in *ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705)*, Sept 2003, pp. 465–468.

[54] M. Takayama, S. Dosho, N. Takeda, M. Miyahara, and A. Matsuzawa, "A time-domain architecture and design method of high speed A-to-D converters with standard cells," in *IEEE Asian Solid-State Circuits Conference 2011*, Nov 2011, pp. 353–356.

[55] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 3, pp. 220–224, March 2006.

[56] C.-S. Hwang, P. Chen, and H.-W. Tsao, "A high-precision time-to-digital converter using a two-level conversion scheme," *IEEE Transactions on Nuclear Science*, vol. 51, no. 4, pp. 1349–1352, Aug 2004.

[57] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "An integrated 9-channel time digitizer with 30 ps resolution," in *2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315)*, vol. 1, Feb 2002, pp. 266–465 vol.1.

[58] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, Feb 2000.

[59] M. Rashdan, A. Yousif, J. Haslett, and B. Maundy, "A new time-based architecture for serial communication links," in *2009 16th IEEE International Conference on Electronics, Circuits and Systems - (ICECS 2009)*, Dec 2009, pp. 531–534.

[60] E. Raisanen-Ruotsalainen, T. Rahkonen, and J. Kostamovaara, "An integrated time-to-digital converter with 30-ps single-shot precision," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1507–1510, Oct 2000.

[61] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de Obaldia, and P. T. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec 2004.

[62] A. Mäntyniemi and J. Kostamovaara, "Time-to-digital converter (TDC) based on startable ring oscillators and successive approximation," in *NORCHIP, 2014*. IEEE, 2014, pp. 1–4.

[63] B. M. Helal, M. Z. Straayer, G. Wei, and M. H. Perrott, "A Highly Digital MDLL-Based Clock Multiplier That Leverages a Self-Scrambling Time-to-Digital Converter to Achieve Subpicosecond Jitter Performance," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 855–863, April 2008.

[64] J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach, and R. K. Henderson, "A 32×32 50ps resolution 10 bit time to digital converter array in 130nm CMOS for time correlated imaging," in *2009 IEEE Custom Integrated Circuits Conference*, Sept 2009, pp. 77–80.

[65] K. Karadamoglou, N. P. Paschalidis, E. Sarris, N. Stamatopoulos, G. Kottaras, and V. Paschalidis, "An 11-bit high-resolution and adjustable-range CMOS time-to-digital converter for space science instruments," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 214–222, Jan 2004.

[66] C. Veerappan, J. Richardson, R. Walker, D. Li, M. W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R. K. Henderson, and E. Charbon, "A 160×128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter," in *2011 IEEE International Solid-State Circuits Conference*, Feb 2011, pp. 312–314.

[67] I. Nissinen and J. Kostamovaara, "Time-to-Digital Converter based on an On-chip Voltage Reference Locked Ring Oscillator," in *2006 IEEE Instrumentation and Measurement Technology Conference Proceedings*, April 2006, pp. 250–254.

[68] D. K. Xie, Q. C. Zhang, G. S. Qi, and D. Y. Xu, "Cascading delay line time-to-digital converter with 75 ps resolution and a reduced number of delay cells," *Review of Scientific Instruments*, vol. 76, no. 1, p. 014701, 2005.

[69] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sanchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen, and E. Pankratz, "A 20MHz BW 68dB DR CT $\Delta\Sigma$ ADC based on a multi-bit time-domain quantizer and feedback element," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2009, pp. 174–175,175a.

[70] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128 × 128 Single-Photon Image Sensor With Column-Level 10-Bit Time-to-Digital Converter Array," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2977–2989, Dec 2008.

[71] B. K. Swann, B. J. Blalock, L. G. Clonts, D. M. Binkley, J. M. Rochelle, E. Breeding, and K. M. Baldwin, "A 100-ps time-resolution CMOS time-to-digital converter for positron emission tomography imaging applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1839–1852, Nov 2004.

[72] D. M. Santos, S. F. Dow, J. M. Flasck, and M. E. Levi, "A CMOS delay locked loop and sub-nanosecond time-to-digital converter chip," *IEEE Transactions on Nuclear Science*, vol. 43, no. 3, pp. 1717–1719, Jun 1996.