Behavioral Modelling and Optimization of a Cyclic Feedback-Based Successive Approximation TDC with Dynamic Delay Equalization

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***Abstract*—This paper investigates the performance of cyclic feedback-based Successive Approximation Time-to-Digital Converter (SA-TDC) with dynamic delay equalization aimed to improve its conversion speed. The converter architecture is studied through numerical and behavioral modelling simulations presenting relevant implementation details and the impact of circuit non-idealities such as devices mismatch and noise. A comprehensive investigation of the dynamic delay equalization technique provides useful insights on the nominal achievable performance (i.e. effective time resolution), as well as circuit implementation guidelines. Furthermore, two novel alternative SA TDC topologies are proposed, targeting superior power efficiency with negligible hardware overhead.**

***Keywords*—successive-approximation, event-based, time-to-digital converter, delay equalization, CMOS, calibration, behavioral modelling.**

I. Introduction

Deep nanoscale CMOS technologies enable time-mode analog signal processing (TMASP). The exploitation of TMASP is becoming increasingly attractive given that the time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals [1]. The main information carrier in time-mode circuits is represented by the time difference between two digital edges (commonly referred to as $start$ and $stop$ event or, similarly, set and $reset$, S and R). Time-to-digital converters (TDCs) are a class of time-mode circuits leveraging on TMASP to digitize a time difference information, hence representing the interface between the continuous-time, discrete-amplitude domain and the digital world. Time mode circuits are increasingly widespread solution in RF and mixed-signal applications, as well as in event-based signal processing [1-4]. Different TDC architectures have been recently developed, among which the successive approximation, which is the object of this work. SA-TDCs exploit binary-scaled delay lines to perform the binary search conversion in the time domain [5-8]. The principle of SA-TDC operation is based on successively delaying the signal event S and reference event R by binary-scaled delays within separate signal paths, such that, at the end of conversion, their relative time difference will have converged to zero. Recent works reporting design and implementations of SA-TDC have proposed both feedforward and feedback-based architectures, although suboptimal as for the trade-off between complexity, area, and conversion time. Most of the SA-TDCs reported in literature are of feedforward type [7-12] and include a number of time comparators equal to the number of output bits n. The binary-scaled delay lines of SA-TDCs can be implemented

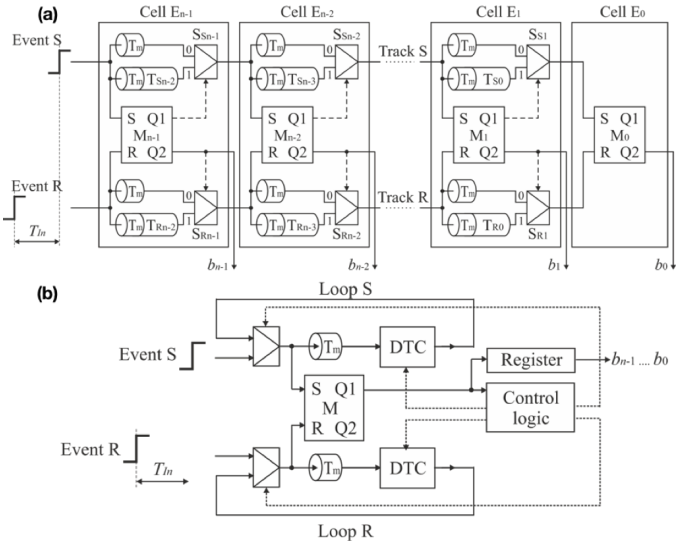

Fig. 1. Basic models of feedforward (a) and feedback SA-TDC (b).

by using unit delay elements consisting, for instance, of a pair of cascaded CMOS inverters [8], [12]. In particular, the propagation time of a single inverters pair defines the quantization step of the converter (the least-significant-bit, LSB), while all of the others binary-scaled delays are integer multiples of such unit element. A viable way to increase the time resolution of the TDC is to leverage on the Vernier interpolation principle, idea which will be further analyzed in Sec. III. This allows the unit delay to be defined as the time difference between the propagation times of two unit elements with different sizing (e.g. one being 1.5 times smaller than the other) [2]. The basic diagrams of feedforward and feedback-based SA-TDC architectures are shown in Fig.1(a) and Fig.1(b), respectively. Both of the architectures comprise multiplexers, digitally programmable delay lines (which can be seen as flash digital-to-time converters, DTCs) and time comparators. The latter can be implemented as MUTEX blocks [8], [12]. Furthermore, the feedback-based SA-TDC is equipped with only a single time comparator, whose output triggers the operation of the asynchronous control logic unit, which drive the multiplexer and set the proper delay introduced by the loop DTCs.

The concept of feedback-based SA-TDC (also referred to as cyclic SA-TDC) has been introduced by University of Oulu

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in [6], and has been further developed in [13-15]. It consists of two loops, in which events S and R are propagated and successively delayed by binary-scaled latencies. The need of using two loops lies on the fact that, along the successive approximation algorithm, the binary scaled delays are added on both the reference and signal paths [15]. The cyclic feedback-based SA-TDC presented in [6] suffers from a low conversion speed, mainly due to the long time offset present in both S and R loops (T_m, hereinafter referred to as T_m offset), which is necessary to compensate the propagation time of the fixed delay logic blocks (i.e. any delay other than that introduced by the DTCs, such as that of the time comparator and multiplexers). Indeed, a long time offset within each loop ensures that both the events S and R propagate through the same number of fixed delay elements, therefore preserving the correctness of the binary search conversion process. A recent proposition to reduce the conversion time of cyclic SA-TDC down to its theoretical limit has been presented in [15]. Such reduction can be achieved by exploiting a dynamic equalization of logic propagation delays in both of the feedback loops. The application of this technique in a feedback-based SA-TDC architecture allows in principle to attain the same conversion time of the feedforward counterpart, inherently faster. To ensure that the feedback SA scheme works, one must guarantee that at every comparison of the time comparator inputs, the two events S and R must have undergone the same constant propagation delay through the T_m delay element and multiplexers. In other words, the time comparator result during the i^{th} comparison (the i^{th} bit decision) must be a function of only the time difference between the events S and R, and of the binary-scaled loop delays (indicated with $T_{S,i}$ and $T_{R,i}$ in Fig.2, with i = 0, 1, ..., n-3), within the T_S and T_R main delay lines. The authors in [6] accomplish this by introducing a 3.5 ns T_m offset within each loop, which is about ten times the maximum time difference to be resolved. Proper circuit operation demands indeed T_m to be much larger than half the input full-scale range of the TDC (i.e. the maximum absolute input time difference to detect), which in turn impairs the conversion speed of the converter. It is also worth noting that, with such a constraint, the two edges S and R will propagate within loops S and R the same number of times. The time difference between events S and R (both the initial time difference and that during each bit decision) is resolved by means of a simple phase detector (lead/lag status). The conversion speed of the TDC is much reduced and, furthermore, long T_m offsets increase the residual mismatch between the two loops. On the contrary, in a scenario where T_m is shorter than half the TDC FSR the events S and R will not propagate within their loops with approximately the same phase, i.e. S may have circulated several times in loop S before the arrival of the event R at the input of the time comparator. This arises the need for a fundamentally different algorithm than the one adopted in [6], such as indeed the dynamic delay equalization network introduced and extensively described in [15], and proposed here again for illustration in Fig.2.

A first asynchronous control logic block (indicated with ACL1 in Fig.2), consisting of the time comparator and of the successive approximation logic, exploits the binary search algorithm by properly controlling the loop DTCs (the T_S and T_R main delay lines described above). Concurrently, the task of the second asynchronous controller (ACL2), and of the counters marked as CNT_R and CNT_S, is to count the number of circulations of each event in its loop, and to compensate by adding more time delay (in terms of integer multiples of the loop time offset T_m) to the event which has encountered less loop circulations. This is exploited through the compensation delay line, which comprises the unit delays marked with T_C in Fig.2. Such dynamic control mechanism equalizes the number of T_m time offsets experienced by each of the events and allows in principle the conversion speed to be theoretically comparable to that of a feed-forward SA-TDC [8].

This work investigates the feasibility of the idea proposed in [15] through numerical and behavioral modelling simulations and by means of circuit-level insights, with the aim of assessing the potential advantages and implications of reducing the loop time offset T_m.

This paper is organized as follows: Section II presents the adopted system modelling approach, describes relevant implementation details and outlines circuit non-idealities. A comprehensive investigation of the feedback SA-TDC with dynamic delay equalization is supported by simulation results. Section III proposes power-efficient architectural enhancements of the basic TDC topology, while Section IV draws the conclusions.

II. System Behavioral Modelling

A. Modelling Approaches

A top-down driven mixed-signal design methodology [16] is adopted here for the development of the SA-TDC. The circuit is first numerically modelled in MATLAB^{TM}, later described in Verilog-A and finally verified through SPECTRE simulations in Cadence^{TM} Virtuoso. The models developed include the effect of the most relevant circuit non-idealities which impair the feedback SA-TDC performance (i.e. its effective time resolution) such as noise and devices mismatch. Both MATLAB^{TM} and Verilog-A modelling approaches exploit an event-driven simulation protocol, where each operation is executed at specific time-stamps (i.e. the arrival of events S and R at the input of the time comparator). The operation of the feedback SA-TDC is essentially that of an event-driven clock-less system. The states of ACL1 and ACL2 are updated only when the event S or R (i.e. a low-to-high digital transition edge) occurs at the inputs of the time comparator.

The MATLAB^{TM} numerical model is based on the description of various delay elements present in the circuit through time-domain representations, and on the logical interaction of these components in an iterative time-domain process. The first modelled phenomenon is the propagation delay time uncertainty of the unit delay elements due to devices mismatch. Indeed, the propagation delay through the j^{th} unit element can be written as:

$$T_{unit,j,0} = T_0 + \Delta t_{mism,j,0} \tag{1}$$

where T_0 is the nominal delay while $\Delta t_{mism,j,0}$ is the propagation time deviation due to mismatch, which is a Gaussian-distributed statistical variable with zero mean and standard deviation equal to σ_{mism}. Given that each TDC loop

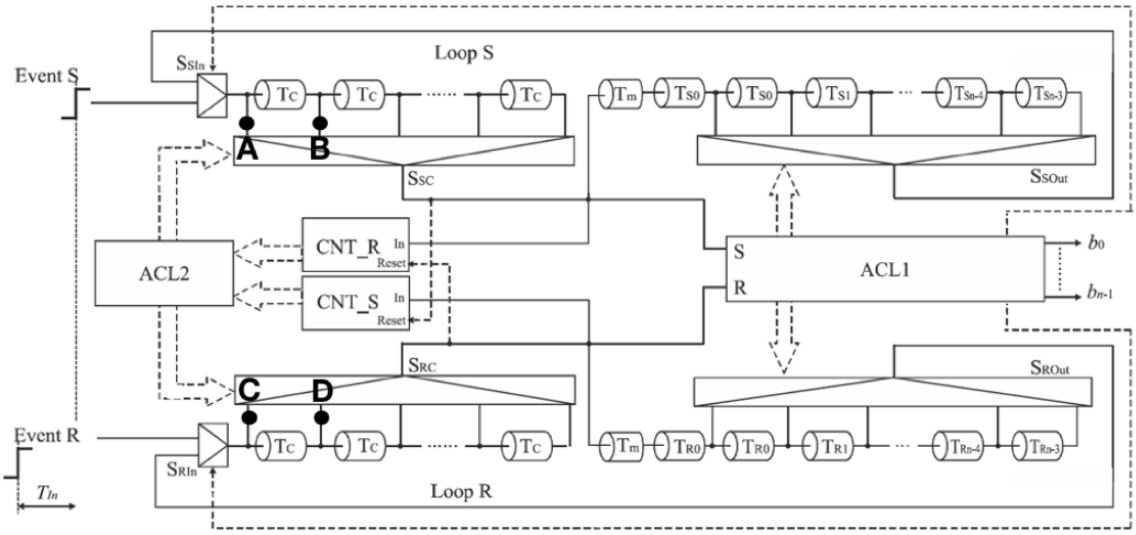

Fig. 2. Feedback SA-TDC architecture with dynamic delay equalization [15].

is made of 2^{n-2} unit delay elements (n being the number of bits of the TDC), the numerical model initializes the propagation delay of each unit delay element of both loops. It is worth noting that CMOS process mismatch is a time-invariant phenomenon, in the sense that the timing deviations of the unit elements propagation delay from their nominal value do not change during circuit operation. This is, indeed, the variables initialization section of the MATLAB^{TM} model. What follows is the modelling of the proposed feedback SA-TDC operation, accounting for the noise of devices. Again, the propagation time of an event through the j^{th} unit element can be written as:

$$T_{unit,j,k} = T_{unit,j,0} + \Delta t_{jitt,j,k} \tag{2}$$

where $\Delta t_{jitt,j,k}$ is the propagation time deviation due to noise (time jitter), which is a Gaussian-distributed statistical variable with zero mean and standard deviation equal to σ_{jitt}, while k is the index of the edge propagating through such delay element. Differently from process mismatch, noise is a time-variant phenomenon, thus the timing deviation $\Delta t_{jitt,j,k}$ will be different for each different edge which is propagated through the j^{th} delay element. Note that, since the noise of different unit delay elements can be considered uncorrelated, to the first order, an edge propagating through a delay line made of m cascaded unit delays (e.g. the first m elements) will experience a delay with mean equal to $\sum_{j=1}^{m} T_{unit,j,0}$ and standard deviation of $\sqrt{m} \cdot \sigma_{jitt}$. Recalling the operation of the proposed feedback SA-TDC [5], the first event detected by the time comparator will be diverted to the longest delay line of the corresponding loop, made of 2^{n-2} unit delay elements. The subsequent delays experienced by the events detected by the time comparator are binary scaled, until the last bit-decision, during which the edge S (or R) will be delayed by a single unit delay. In the proposed feedback SA-TDC topology, the delay elements T_C of the compensation delay line, as well as the loop time offset T_m, also consist of cascaded unit delays T_{unit}, and therefore the above mentioned definitions of propagation time deviations still apply. The logic operation of the SA-TDC can be summarized by the pseudo-code presented in Fig.3.

```
//Initialisation of SA − TDC
T_S[1] = 0;
T_R[1] = T_in;
CNT_S = 0;
CNT_R = 0;
n = 8;
//SA − TDC operation loop
for i = 1:n − 1
    BIT[i] = (T_S[i] − T_R[i] ≤ 0);
    if (BIT[i] == 1)
        CNT_S = 0;
        CNT_R = CNT_R + 1;
        T_S[i + 1] = T_S[i] + T_S,delay[i];
        T_R[i + 1] = T_R[i] + {T_C,R(CNT_R + 1) − T_C,R(CNT_R)};
    if (BIT[i] == 0)
        CNT_R = 0;
        CNT_S = CNT_S + 1;
        T_R[i + 1] = T_R[i] + T_R,delay[i];
        T_S[i + 1] = T_S[i] + {T_C,S(CNT_S + 1) − T_C,S(CNT_S)};
end
BIT[n] = (T_S[n] − T_R[n] ≤ 0);
```

Fig. 3. Pseudo-code describing the core behavior of the feedback SA-TDC architecture with dynamic delay equalization.

T_S and T_R represent the time-stamps of the arrival times of respectively events S and R at the input of the time comparator while T_{in} represents the S-R input time difference to be digitized. CNT_S and CNT_R are the corresponding counter values of the delay equalization network (i.e. CNT_S is the number of times that event R have circulated within its loop which is, therefore, the number of T_C unit delays that event S has to undergo within the compensation delay line). $T_{S,delay}$ and $T_{R,delay}$ are the delays undergone by the events S and R propagating within their corresponding T_S and T_R main delay lines. The latter are initialized as indexed arrays, with i equals to 1 representing the propagation through all of the 2^{n-2} unit delay elements (and so on for the next binary scaled delays). The fixed T_m offset and propagation delays through

the multiplexers are also included in this term. $T_{C,r}$ and $T_{C,s}$ are arrays initialized to form the T_C compensating delay line, using the same modelling approach for the T_S and T_R main delay lines described above. $BIT(i)$ is instead the i^{th} TDC bit.

The Verilog-A behavioural model of the feedback SA-TDC with dynamic delay equalization network has been developed following the same approach introduced above, and is verified through SPECTRE simulations in Cadence^{TM} Virtuoso. Furthermore, actual hardware components such as multiplexers, counters, flip-flops and combinational logic are also included, and modelled as additional noisy delay blocks whose delay is subject to process variability. The control block ACL1 generates the digital control signals for the multiplexers S_{SIn}, S_{RIn}, S_{SOut}, S_{ROut} as well as the TDC digital output. The delay equalization network, controlled by ACL2, consists of a D-bit counter (for a 2^D-bit SA-TDC), where counter CNT_S (CNT_R) increments on the positive edge of event S (R), and is reset on the positive edge of event R (S). This black-box approach is extremely flexible and powerful, as it produces a rapid construction of the required circuitry to be designed, allowing a mix-match substitution of transistor level circuits to follow a truly mixed-signal design methodology.

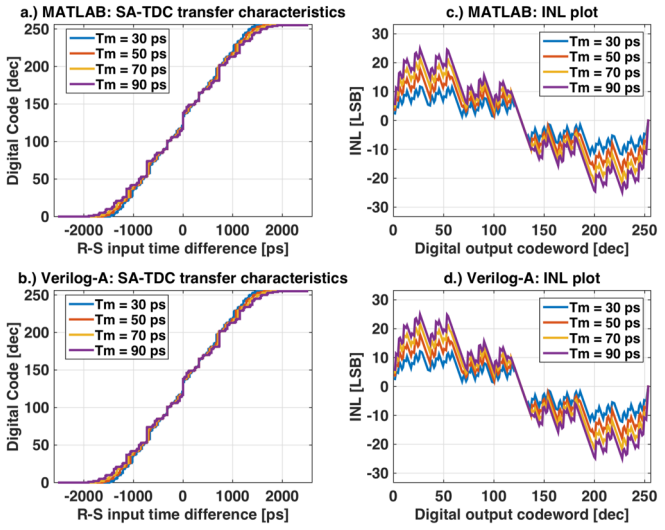

Fig. 4. Transfer characteristics and integral non-linearity of an 8-bit feedback SA-TDC without dynamic delay equalization and for different T_m values, for both the MATLAB^{TM} numerical model (a)(c) and Verilog-A behavioral model (b)(d).

The SA-TDC S-R input time difference versus digital output transfer characteristics and the static linearity parameters (differential and integral nonlinearity, DNL and INL) obtained from both the MATLAB^{TM} and Verilog-A models, and in the case of n = 8, are shown in Fig.4 and 5, with the dynamic delay equalization network disabled and enabled respectively. The good matching between the models in both case scenarios validate the appropriateness of the adopted modelling approaches. It is worth emphasizing that the adoption of dynamic delay equalization is mandatory when targeting T_m loop offset values comparable to (or lower than) the maximum input time difference to convert. Indeed, as shown by the strongly nonlinear transfer characteristics in Fig.4, the TDC operation is logically incorrect in the absence of dynamic delay

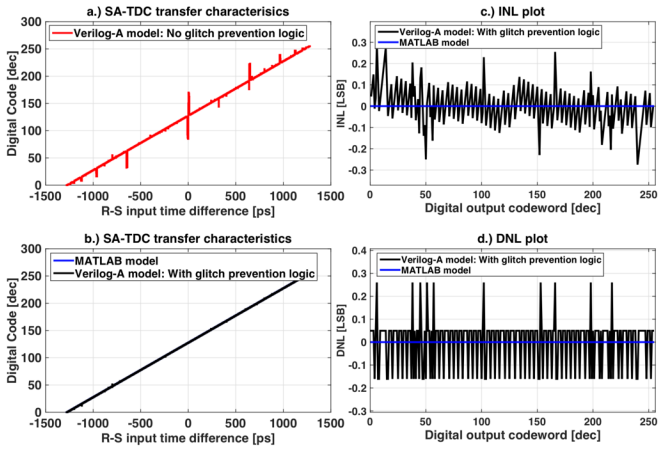

Fig. 5. Transfer characteristics of the SA-TDC with dynamic delay equalization simulated in Verilog-A and when the glitch prevention logic is disabled (a) and enabled (b), the latter compared to the MATLAB^{TM} numerical model. INL (c) and DNL (d) of the transfer characteristics in (b).

equalization. An intuitive explanation of such behaviour can be exemplified as follows. Let us consider a unit delay T_0 of 10 ps and a T_m offset of 50 ps (equivalent to 5 LSBs, which is a good estimation, as shown in Sec. III b). Let us then assume that the S-R input time difference T_{In} is such that, during the conversion process, event S will have to circulate within its loop four times before event R occurs at the input of the time comparator. This means, for instance, that event S will have passed through T_m four times more than R, equivalent to a 20 LSBs error in the input-output transfer characteristic in correspondence of that particular T_{In}. Therefore, greater T_m offsets lead to larger INL errors if proper delay equalization is not performed. An interesting (although unwanted) behaviour of the feedback SA-TDC with dynamic delay equalization can be observed in the transfer characteristics of the Verilog-A model shown in Fig.5(a) in the form of large glitches, which were not spotted in the MATLAB^{TM} numerical model. These glitches occur from the false triggering of the time comparator due to the residual pulses in the T_C compensation delay line. Such spurious behaviour is best explained through an example, first reminding once more that the term *event* means here a low-to-high transition edge of a digital signal. Starting from a condition in which the value of both counters CNT_S and CNT_R is zero, if event S leads R, then it will arrive at the input of the time comparator passing from node A in Fig.2 (indeed, CNT_S = 0 is equivalent of saying that the node A of the compensation delay line T_C is connected to the input of the MUTEX by the multiplexer S_{SC}). As a consequence, CNT_R is incremented from 0 to 1. Let us then assume that event R arrives at the input of its T_C compensation delay line immediately after this (node C of Fig.2). Accordingly, it will be propagated through one T_C unit delay (recall that CNT_R = 1) and it will afterwards arrive at the input of the time comparator. Therefore, CNT_S is incremented from 0 to 1 and CNT_R is reset to 0. This means that the multiplexer S_{SC} will now immediately select the output of the first T_C delay element (node B), which is likely to still retain a HIGH logic value since, in practice, the on-time of each signal within the loop is non-zero (i.e. a low-to-high voltage transition of a node is not immediately followed by a high-to-low transition,

since other system constraints, not addressed in this paper, bound the on-time of the digital signals in the loops to a few hundreds of picoseconds). Therefore, the S input terminal of the time comparator will be triggered by an unwanted event, which will cause erroneous operation in the subsequent bit cycles. Such unwanted scenario causes greater nonlinearity errors if occurring during the first bit decisions, due to the MSB-first scheme utilized. A solution to this is to disable the T_C compensation delay lines right after events S or R has been output multiplexed through S_{SC} or S_{RC} respectively, and only re-enabling them when their corresponding events will return back at their inputs (nodes A and C). Such glitch prevention logic has been included in the Verilog-A model, and its effectiveness is demonstrated by the transfer characteristics of Fig.5(b), showing now an almost ideal matching with the MATLAB^{TM} numerical model.

B. Circuit non-idealities

As previously mentioned, the main impairments to the performance of SA-TDCs, as for the achievable effective time resolution, are noise (time jitter) and devices mismatch. Both phenomena, inherent to the physics of the transistor, are statistical, although the former is time-variant while mismatch is time-invariant (given an IC, the timing deviation of each unit delay from its nominal value does not change during circuit operation). In general, any deviation from the nominal propagation time of delay elements is particularly harmful since it accumulates along the propagation of the event through the delay lines of its loop. The total accumulated time error on the last bit decision (the LSB) could therefore exceed the targeted time resolution (i.e. the nominal value of the unit element delay T_0), resulting in poor linearity. Let us further convey such point through an example, neglecting for the sake of simplicity the dynamic delay equalization network and considering only noise. Imagine the input time difference between the events S and R is equal to half the full-scale range of a bipolar SA-TDC, with S leading; the number of loop circulations of the event S within its loop is equal to $n-1$, while the number of unit delays encountered is $2^{(n-1)}-1$, equivalent to a total propagation time $\sum_{j=1}^{2^{(n-1)}-1} T_{unit,j}$. Therefore, the standard deviation of the total propagation time error due to jitter is $\sqrt{2^{(n-1)}-1}\cdot\sigma_{jitt}$. Similar considerations apply to the effect of mismatch. It is then evident that, in order not to excessively impair the effective resolution of the SA-TDC, the total accumulated time error must be smaller than 1 LSB. A solution to mitigate the accumulation of the propagation time error due to the mismatch between the two loops (S and R) has been presented in [6] and relies on loop swapping. Loops S and R are swapped on every consecutive event circulation (bit decision) so as to avoid conversion errors associated with the accumulation of propagation time deviation, thus limiting the time error to the mismatch between the propagation time of the DTCs in the two loops. As previously mentioned, the feedback loops consist of mostly delay lines (T_m, T_C, $T_{S0} \div T_{Sn-3}$, $T_{R0} \div T_{Rn-3}$) built by cascading unit delay elements (each of which is an inverters pair). In order to estimate the impact of jitter and mismatch on the operation of the feedback-based SA-TDC, we had first designed the unit delay element in a standard 28 nm CMOS process with a nominal delay of about 10 ps. Accordingly, the designed unit element is characterized by σ_{jitter} and σ_{mism} of 16.87 fs and 0.6 ps respectively. In the example of an 8-bit SA-TDC, the standard deviation of the accumulated time jitter along the total loop delay would then be equal to 190 fs, thus still not concerning for this particular value of T_0, which is significantly higher. An additional non-ideality so far not considered and potentially harmful for correct circuit operation, if not properly addressed, is the metastability of the time comparator. As explained in [15], the output of the MUTEX block must be available before a particular event is diverted into a specific delay line of its loop (in other terms, the selection codes of the multiplexers S_{Sout} and S_{Rout} must be ready before the events S and R have propagated through their delay line). This is accomplished by adding the time offset T_m within the loops, whose value should be equal to or larger than the propagation time through the time comparator. Therefore, in order to estimate the value of T_m, we have simulated the metastability window of the MUTEX block, shown in Fig.6.

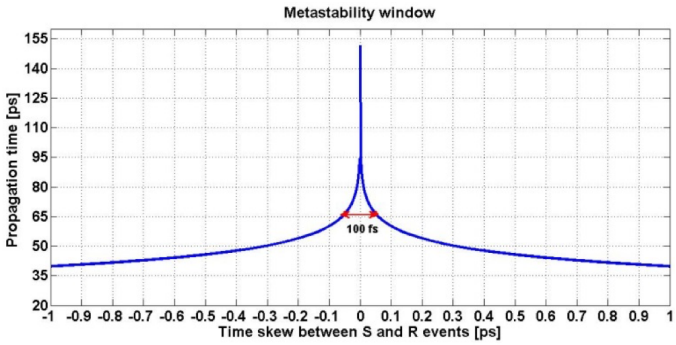

Fig. 6. Metastability window of the MUTEX time comparator.

The x-axis reports the time skew between the input events (difference between the S and R rising edge time-stamps), while the vertical axis is the propagation time of the comparator, defined as the time between the commutation of the output and the occurrence of the first input event. To the first order, if we outline 100 fs as the minimum S-to-R time difference the system must be able to resolve, the propagation time of the MUTEX time comparator is 66 ps. The delay T_m should therefore be longer than 66 ps to ensure the output of the MUTEX block is available before the arrival of events S and R at the T_S and T_R main delay lines. Accordingly, the delay T_C of the elements in the delay equalization network will be equal to the value just outlined for T_m, plus the additional constant loop propagation delays of the multiplexers.

C. Simulation Results

To investigate the effect of both time-invariant (devices mismatch) and time-variant statistical non-idealities (device noise/jitter) on the operation of the proposed feedback SA-TDC, the simulation results have been extracted from the MATLAB^{TM} numerical model, given its superiority over the Verilog-A model in terms of simulation time. Indeed, large parametric analyses of multiple different circuit parameters can be performed very quickly, still quite accurately reproducing the behavior of the circuit. The two main metrics for characterization are INL and N_{lin}, the latter being the effective number of bit of the converter (what in analog-to-digital converters is referred to as ENOB), expressed as:

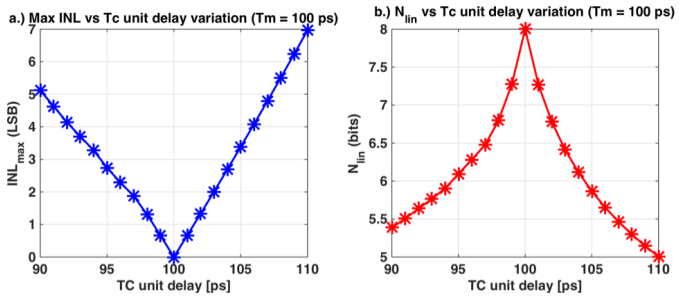

Fig. 7. Integral nonlinearity (a) and N_{lin} (b) of the TDC for case scenario number 1.

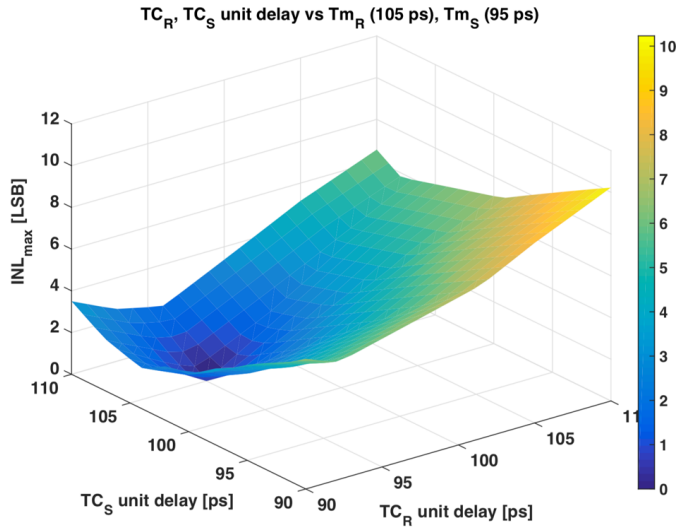

Fig. 8. Integral nonlinearity of the TDC for case scenario number 2.

$$N_{lin} = n - \log_2(|INL_{max}| + 1) \tag{3}$$

The first two case scenarios which have been explored, shown respectively in Fig.7 and Fig.8, are:

1) Identical T_m offset in both S and R loops, fixed to 100 ps; identical T_C unit delays in both S and R loops, but swept together between 90 ps and 110 ps (with 100 ps being the optimal value).
2) Different but fixed T_m offsets in the S and R loops ($T_{m,S}$=95 ps,$T_{m,R}$=105 ps); different T_C unit delays in the S and R loops, swept independently between 90 ps and 110 ps (2D parametric sweep).

While both of the abovementioned case scenarios focus on the performance impairment induced by the compensation delay lines T_C, the first highlights the effect of the mismatch between the unit delay T_C of the compensation network and the loop offset T_m, while the second addresses the differential mismatch between the S and R compensation delay elements, T_{CR} and T_{CS}. It must be pointed out that both T_m and T_C can differ from their nominal values not only because of devices mismatch but also because of asymmetry arising during the physical layout design of the circuit, which however could be kept reasonably negligible by appropriate layout techniques. From both Fig.7 and 8, it could be observed that if T_C is affected by even a single unit delay time deviation (T_0 of 10 ps) from its nominal value (which is T_m), N_{lin} will deteriorate by nearly 2.5 bits. This is understandable, as this 10 ps mismatch accumulate over the time-to-digital conversion process, as previously explained. It is interesting observing, from Fig.8, that the best linearity is achieved when the T_C delay in loop S matches the T_m delay in loop R and vice versa (T_{CS} = $T_{m,R}$ = 105 ps and T_{CR} = $T_{m,S}$ = 95 ps).

Another set of non-idealities which have been studied, categorized into time-invariant and time-variant phenomena, are listed as follows.

Time-invariant non-idealities due to process mismatch:

1) Input-referred timing offset of the time comparator, $\sigma_{off,tcomp}$ (which could be seen as a right/left shift of the time comparator meta-stability curve presented in Fig. 6 from its center value of 0 fs). Fig.9
2) Process mismatch in the unit delay of the T_S and T_R main delay lines unit element (nominally 10 ps). Fig.10.
3) Process mismatch between the compensation delay line unit delay T_C and the loop offset T_m (nominally 100 ps). Fig.11.

Time-variant non-idealities due to circuit noise:

1) Time jitter of the unit elements delay of the main delay lines T_S and T_R. Fig.12.
2) Time jitter in the T_C elements of the compensation delay line and in the loop offset delay element T_m. Fig.13.

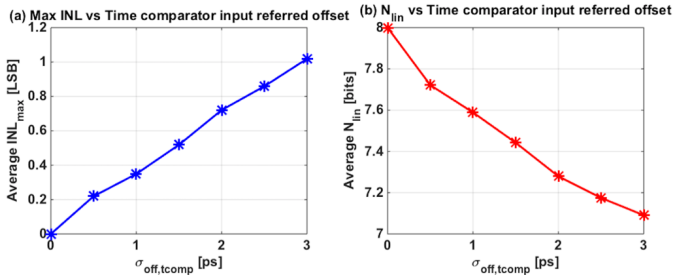

Fig. 9. TDC INL (a) and N_{lin} (b) with various input-referred time comparator offset standard deviations.

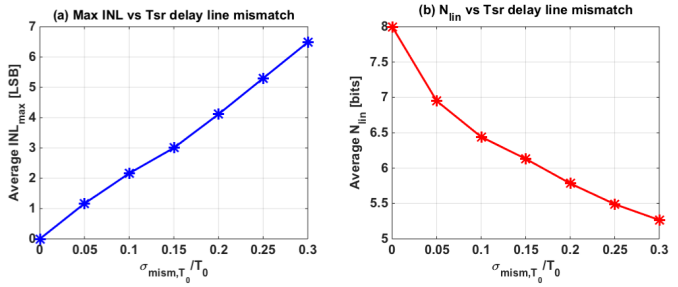

Fig. 10. TDC INL (a) and N_{lin} (b) versus standard deviation of the unit delay in the T_S and T_R main delay lines. The standard deviation is normalized to the unit delay of 10 ps.

Fig.9 shows the maximum tolerable time comparator offset for acceptable feedback SA-TDC linearity performance.

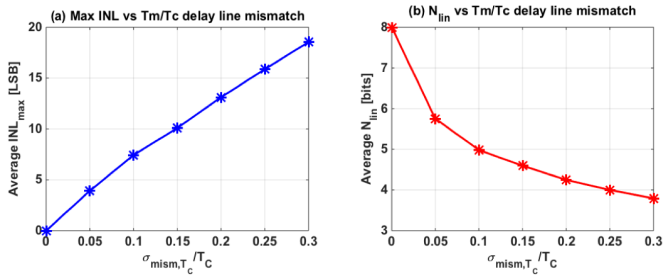

Fig. 11. TDC INL (a) and N_{lin} (b) versus standard deviation of the propagation time of the unit delay element of the T_C compensation delay line affected by process mismatch. The standard deviation is normalized to the T_C unit delay of 100 ps. The loop time offset T_m is equal to the T_C unit delay.

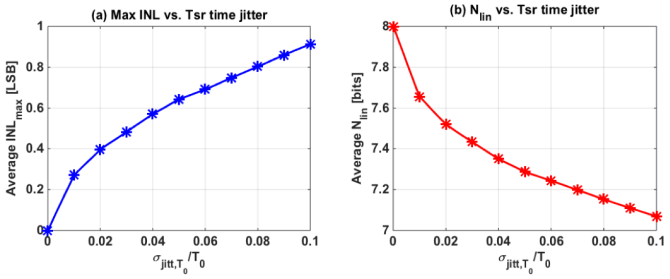

Fig. 12. TDC INL (a) and N_{lin} (b) versus standard deviation of the time jitter of the unit delay element of the the T_S and T_R main delay lines. The standard deviation is normalized to the unit delay of 10 ps.

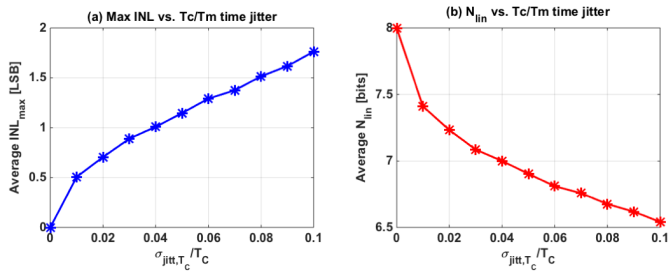

Fig. 13. TDC INL (a) and N_{lin} (b) versus standard deviation of the time jitter of the unit delay element of the T_C compensation delay lines. The standard deviation is normalized to the T_C unit delay of 100 ps. The loop time offset T_m is equal to the T_C unit delay.

Optimal circuit sizing to balance the trade-off between power consumption and time comparator input referred offset (and thus area) can be derived from this top-down specification driven approach. In the 28 nm CMOS technology considered as a reference example for this work, the time comparator input referred offset standard deviation is less than 500 fs, thus the resulting N_{lin} deterioration is about 0.2 bit. Figs. 10 and 11 provide insights about the specifications on the maximum tolerable mismatch of the delay cells (which is inversely proportional to their area). Fig.11 suggests that particular attention should be paid to the design of the T_m delay element and T_C compensation delay line, given their greater impact on the TDC linearity, compared to the mismatch of the T_S and T_R main delay lines, which instead contributes less. Similarly to devices mismatch, circuit noise (time jitter) can be optimized through the curves shown in Figs. 12 and 13. For TDCs which prioritize power efficiency, it is indeed important to understand exactly how much jitter can be tolerated in the system for a certain power budget (jitter and power consumption are in trade-off). In reality, all of these non-idealities coexist in the feedback SA-TDC, meaning that the overall performance deterioration of the converter is expected to be the superposition of all of their individual effects. The time comparator input referred timing offset, as well as the mismatch of the T_C compensation delay line relative to the corresponding T_m delays, should be compensated via an offset calibration procedure similar to the one introduced in [6]. Due to the feedback nature of the TDC, the small residual delay offset (post-calibration) between the two loops and its corresponding T_C compensation delay line will accumulate along the successive circulations of the S and R events in their loops, unless loop-swapping is employed [6], at the cost however of an increased hardware complexity. Time jitter cannot be calibrated due to its time-variant nature, thus one must overcome this at circuit design level (i.e. low-noise delay lines), at the cost of higher power consumption [17]. For the special case, addressed in this paper, of a TDC with 10 ps resolution (i.e. unit delay T_{unit}), the accumulated jitter does not result in a significant performance loss from a linearity perspective, as already outlined in Section II.b and shown in Figs 12 and 13.

III. Power-Efficient Architectural Enhancements

This section presents two alternative SA-TDC topologies aimed to: 1) increase the converter time resolution with negligible power overhead, and 2) minimize power consumption with no deterioration in the time resolution, therefore both targeting superior power efficiency (i.e. figure-of-merit, defined as ratio between resolution and power, for the same conversion time). Focusing on the first, as introduced before, the time resolution of feedback-based SA-TDC with dynamic equalization of logic delays is the propagation time of a unit delay element (pair of cascaded CMOS inverters). In order to double the time resolution, thus extending the SA-TDC output bit-width by one bit, we here propose the topology depicted in Fig.14, which makes use of the Vernier time interpolation technique for only the last conversion step (the LSB-bit decision).

The proposed hybrid SA/Vernier-TDC topology develops from the original architecture of Fig.2, and can be obtained by adding only four extra delay elements (T_{S0}, T_D and T_{R0}, T_D) and two multiplexers (S_{SD} and S_{RD}). In order to still maintain binary scaling between the successive delays introduced by the loops along the conversion procedure, the propagation time through both the new delay elements T_D must be 1.5 times the unit delay T_0. The operating principle of this alternative hybrid topology is the same as for the original one for the first $n-1$ conversion steps (from the MSB- to the (LSB+1)-bit decisions), while Vernier time interpolation is used to extend the time resolution in the LSB-bit decision. To exemplify such operation, let us assume that after delaying the event S by the shortest delay line T_{S0} (delay T_0), this event still leads event R at the input of MUTEX (time comparator). Accordingly, S will be diverted towards the new delay element T_D, and the multiplexer S_{RD} will be controlled by ACL1 is such a way that the oncoming event R will instead be diverted towards T_{R0}. As a consequence, the relative time shift between events S and R will be equal to the difference between T_D and T_{R0}, which is indeed $T_0/2$. It worth noting that only one of the two

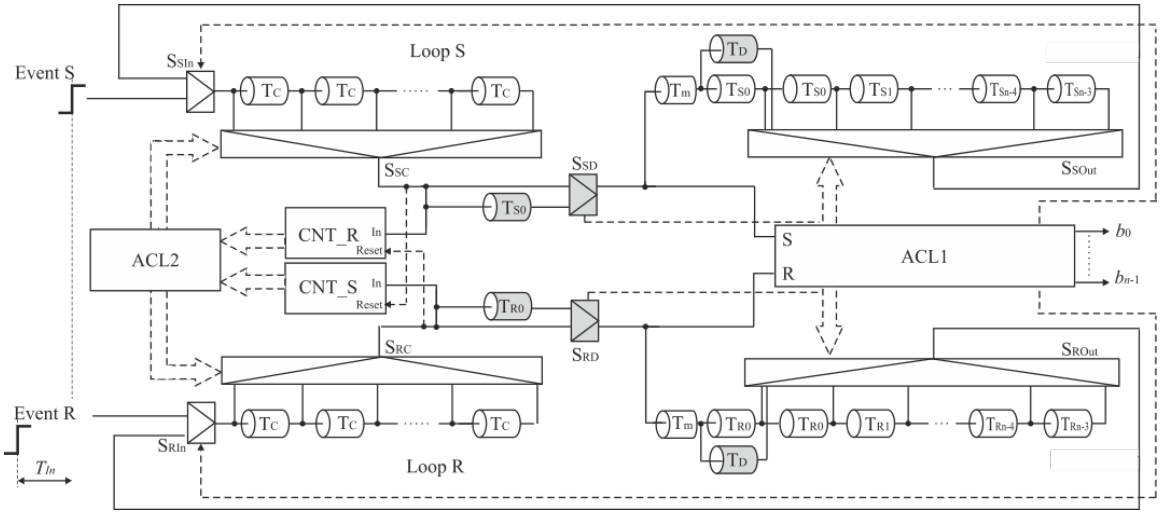

Fig. 14. n-bit successive-approximation/Vernier hybrid TDC.

multiplexers S_{SD} and S_{RD} is switched during the LSB-bit decision (the Vernier interpolation phase of the conversion) while, during all of the previous conversion steps, these multiplexers are in idle state. The proposed hybrid successive-approximation/Vernier TDC topology here described allows in principle to reduce the quantization step by a factor 2, with an increase in power consumption of only approximately $12,5\%$ compared to the original topology, thus resulting in over 70% higher power efficiency.

Addressing now the minimization of the TDC power consumption, it should be noted that during the propagation of events S and R in their loops, all of the unit delay elements comprised in the DTCs will commutate (events S and R will be properly multiplexed by the MUXes S_{Sout} and S_{Rout}, but the digital edges always propagate until the end of the delay line made of 2^{n-2} units), therefore causing unnecessary power consumption (as exemplified by Fig.15).

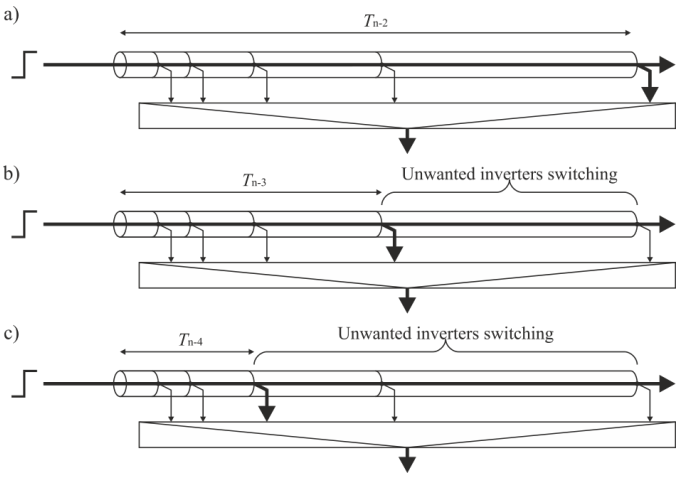

Fig. 15. Main delay line highlighting unnecessarily switched sections. Total main delay line used in the first step of conversion (MSB decision) (a), half of delay line, used in the second step of conversion (b) and quarter of the delay line, used in the third step of conversion (c).

In order to improve the power efficiency, we propose to switch off those sections of the main delay lines which are not used in that particular step of time-to-digital conversion (i.e. all of the delay elements which follow the MUX tap through which the events S and R are output multiplexed). From a circuit implementation perspective, this can be realized by interposing AND logic gates between the binary scaled delay sections of the main delay line (i.e. right after the nodes connected to the multiplexers S_{Sout} and S_{Rout}), as shown in Fig.16. The signal propagation towards the end of the delay line can indeed be interrupted by using one of the two inputs of the AND gates as enable signal, properly controlled by the ACL1 block (i.e. if we want to stop the edge propagation after the i^{th} AND gate, a logic 0 is assigned to one of its inputs).

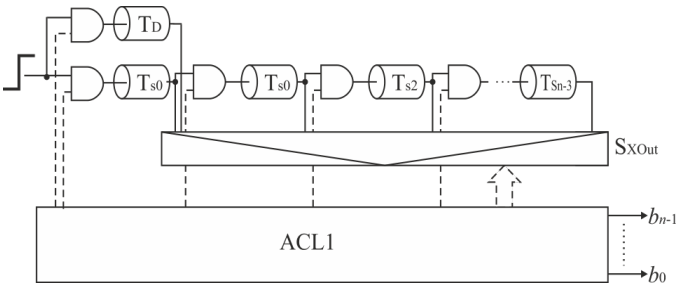

Fig. 16. Main delay line with AND gates to turn off unused sections.

The effectiveness of the proposed solution is demonstrated by comparing the average power consumption of the main delay line of the original architecture with that of this new proposed topology. As evident from the second and third columns of Table 1, in the special case of a 28 nm CMOS process at 1.05 V nominal supply, turning off unused sections of the main delay line during each conversion cycle results in about 47% lower power consumption.

IV. Conclusion

The cyclic feedback-based SA-TDC with dynamic delay equalization features a conversion time close to its theoretical minimum defined by the operation of the binary search algorithm in the time domain [15]. The main advantage of the feedback topology over the feedforward counterpart is the use

TABLE I. POWER CONSUMPTION OF THE MAIN DELAY LINE

	Original main delay line	Delay line with AND gates to turn off unused sections
Average power * [mW]	1.75	0.93 (-47 %)

**The power consumption has been simulated by applying a 1 GHz input square wave at the input of the main delay line, whose MUX and AND gates are controlled as in normal TDC circuit operation.*

of only a single time comparator. However, the exploitation of the dynamic delay equalization technique increases circuit complexity because of the required additional logic and delay compensation elements. The presented study investigates the performance of cyclic feedback-based SA-TDC with dynamic delay equalization through numerical and behavioral modelling simulations, with the aim of assessing the sensitivity of the converter to noise (time jitter) and devices mismatch. The impact of such non-idealities on the TDC performance is investigated using a standard 28 nm bulk CMOS process, so as to outline relevant design guidelines for the future converter implementation. In the end, two incremental evolutions of the TDC architecture are presented, both targeting improved power efficiency by means of higher time resolution and lower power consumption respectively.

V. ACKNOWLEDGEMENTS

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