Cost-Effective Time-to-Digital Converter Using Time-Residue Feedback

Jung-Chin Lai and Terng-Yin Hsu, *Member, IEEE*

***Abstract*—This paper proposes a time-residue feedback scheme to balance resolution and complexity in a cell-based time-to-digital converter (TDC). The time residue is amplified and fed back into a cyclic-ring Vernier recursively until it cannot be detected correctly. Only one variable-resolution cyclic-ring Vernier and one tunable delay-chain time amplifier (TA) are adopted. Both coarse and fine oscillators of the proposed Vernier which are designed by the same variable-resolution digital controlled oscillator can be switched off to decrease ground bounce during TA activities. With various control codes, the TDC resolution is also programmable. The test application-specified integrated circuit which has a 13-b resolution and occupies 0.02 mm^2 in TSMC 65-nm CMOS process can operate in either feedback or feedforward mode. In feedback mode, the measurements of sampling rate, resolution, input range, differential nonlinearity, and integral nonlinearity are 10 MHz, 0.98 ps, 5.76 ns, $\pm$ 0.8 LSB, and $\pm$ 2.2 LSB, respectively; it also consumes 3 mW at 1 V supply voltage. The sampling rate, resolution, and power dissipation of the feedforward operation are 250 MHz, 6.01 ps, and 17.5 mW, respectively.**

***Index Terms*—Cyclic-ring Vernier, feedback, time amplifier (TA), time residue, time-to-digital converter (TDC).**

I. Introduction

TIME-TO-DIGITAL converters (TDCs) are widely used for time interval measurements such as lifetime measurement in atomic physics, jitter measurement, and laser scanning microscopy measurements. Moreover, TDCs are applied in all-digital phase-locked loops [1]–[3] and delay-locked loops [4]–[6] for digitalizing phase differences in clock synchronization. TDCs with a wide input range and high resolution are used for time-of-flight measurement [7]–[11]. Similarly, analog-to-digital converters (ADCs), using a voltage-controlled delay line to convert voltage differences according to the variation of delay time, require a wide range and high-resolution TDC [12], [13].

Several types of TDC have been developed, with a chain-of-buffers Vernier TDC being the basic type [14]. The number of propagated buffers is the TDC code for a time interval, and the resolution of a TDC is determined by the propagation delay of each buffer. A Vernier delay line [15], [16] comprises two buffer chains with different propagation delays, and this property enables enhancing the resolution by determining the difference in propagation delays between the buffers in both chains. Therefore, the high resolution afforded by the Vernier delay line is attributable to its small time steps. Realizing a wide input interval requires a design that applies numerous buffer chains; however, such a design also involves considerable complexity and a large area. Fig. 1 displays a cyclic-ring Vernier [17], [18], which is similar to a Vernier delay line but replaces buffer chains with ring oscillators to reduce the necessary area and to extend input interval adequately. A coarse ring is used for counting coarse steps and a fine ring is used for counting fine steps, which denote the period difference between the coarse and fine rings. The coarse count affords a wide input interval within a given bit range, and the fine count enables achieving high resolution by minimizing the period difference between the coarse and fine rings. Thus, a two-stage TDC [14], [21], [26] is implemented, including a chain-of-buffers Vernier for coarse measurement and a Vernier delay line for fine measurement, where a time amplifier (TA) amplifies the input pulse residue to improve the TDC resolution. A Vernier-ring TDC [19], [20] applies Vernier delay cells and arbiters to cascade in a ring format, and it reuses the ring for the measurement of input intervals; this scheme, therefore, has a wide input interval and a small area. Moreover, a two-dimensional Vernier scheme [22] is implemented for comparing two signals in different delay lines through various buffers; this scheme entails using the same delay cells as a Vernier delay line, but involves a more complicated algorithm to extend the input range. A pipeline TDC [23], [25],

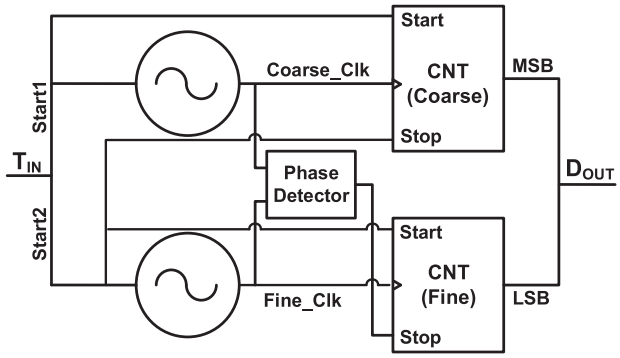

Fig. 1. Cyclic-ring Vernier.

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J.-C. Lai is with the Institute of Computer Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the National Chip Implementation Center, Hsinchu 300, Taiwan (e-mail: jungchin.cs96g@g2. nctu.edu.tw).

T.-Y. Hsu is with the Department of Computer Science, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: tyhsu@cs.nctu.edu.tw).

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[27], [36] offers a multistage operation to achieve considerable gain and a more rapid conversion rate, whereas a cyclic TDC [28], [29] applies cyclical ADC architecture in the TDC. A multiplying digital-to-analog converter is repetitively used for converting and generating residue from a subtraction operation (the original pulse and the pulse generated by the digital-to-time converter) for time amplification. Finally, a delta-sigma TDC [30], [37]–[39] uses highly digital time-domain arithmetic circuits, which employ MASH architecture with a gated ring oscillator TDC.

The current study proposes a cost-effective feedback TDC that recursively shares a cyclic-ring Vernier and a TA. The proposed design adopts only one tunable delay-chain TA and one variable-resolution cyclic-ring Vernier. The time residue is fed back (not cascaded) into the cyclic-ring Vernier, similar to a two-stage TDC (feedforward approach), after which the TA amplifies the time residue. Thus, the cyclic-ring Vernier is successfully shared and suspended recursively to balance the chip area, input range, power dissipation, and noise. To improve development efficiency as well as process, voltage, and temperature (PVT) effects, both coarse and fine oscillators are implemented by the same digitally controlled oscillator (DCO) with various control codes. A feedback operation achieving high resolution incurs more latency, consequently resulting in a low sampling rate. However, if latency is more critical than resolution, then our design can become a feedforward (one-stage) TDC directly. Overall, the proposed scheme is a cell-based all-digital design that is portable and easy to implement.

The remainder of this paper is organized as follows: Section II introduces a pipeline and feedforward TDC, and Section III proposes the time residue feedback scheme. The circuit designs are described in Section IV. Section V presents very-large-scale integration (VLSI) implementation and measurement processes. Section VI presents conclusions.

II. Previous Work and Problem Statement

A. Pipeline and Feedforward TDC

Fig. 2(a) and (b) shows the two-stage feedforward TDC [14] and its time residue interval, and this scheme comprises several TAs and two TDCs. The coarse TDC uses the chain-of-buffers Vernier [14] at the first stage and the fine TDC uses the Vernier delay line [15], [16] at the second stage. The time residues are amplified in parallel and then fed forward into the fine TDC. The output can be formulated by

$$C_{\mathrm{TDC}} = C_{\mathrm{CTDC}} + C_{\mathrm{FTDC}}/G_{\mathrm{TA}} \tag{1}$$

where C_{CTDC} is the coarse TDC output, C_{FTDC} is the fine TDC output, and G_{TA} is the TA gain. The resolution of this scheme is calculated as the minimum time step of the TDC divided by the TA gain. For example, if the minimum time step is 6.01 ps and the TA gain is 6.1, then the resolution is 0.98 ps; additionally, the higher the TA gain, the higher the subsequent TDC resolution. There are two solutions to get better resolution. One is to have the smaller time step. The other is to have higher TA gain. Both of these solutions also increase the TDC conversion time.

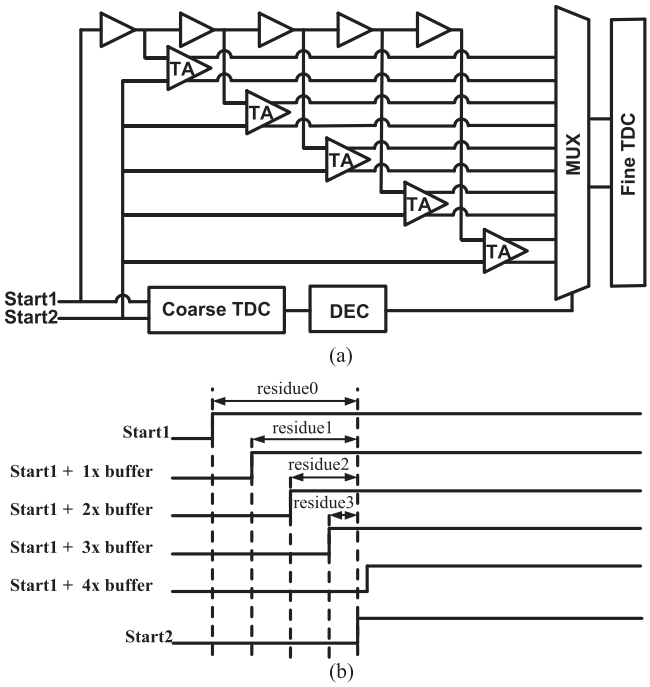


Fig. 2. Feedforward TDC with parallel TAs: (a) block diagram and (b) time-residue interval.

B. Problem Statements

Because time residue is derived as the delay of buffers subtracted from the input interval, the feedforward TDC uses a chain-of-buffers Vernier, comprising several buffers and TAs, to amplify the time residue (see Fig. 2). The TAs dissipate considerable current and induce noise during operation. The coarse TDC drives the designated time residue intervals and forwards them to the fine TDC. To reduce hardware cost, a new feedback structure with a single TA is derived herein to attain four main objectives in this work:

1) extend the input range;
2) enhance the resolution;
3) reduce the transient current for low noise and jitter; and
4) compensate for the PVT effects.

III. Proposed Time-Residue Feedback TDC

A. Feedback Architecture

Fig. 3(a) illustrates plots of the block diagram of the proposed feedback TDC, which comprises a TA, residue generator, ordering output register, and cyclic-ring Vernier. The time residue is generated in each feedback cycle (i.e., from the end of the input interval to the next rising edge of the clock) by the residue generator, as depicted in Fig. 3(b). The timing diagram of the proposed feedback TDC is shown in Fig. 3(c). In each feedback cycle, the input pulse is loaded into the cyclic-ring Vernier to measure the time interval of the input pulse and generate a new time residue, which is then amplified by the TA and fed back into the cyclic-ring Vernier. During the conversion cycle, the TA gain also cyclically accumulates in the time-residue amplification. The final resolution is determined by the TA gain

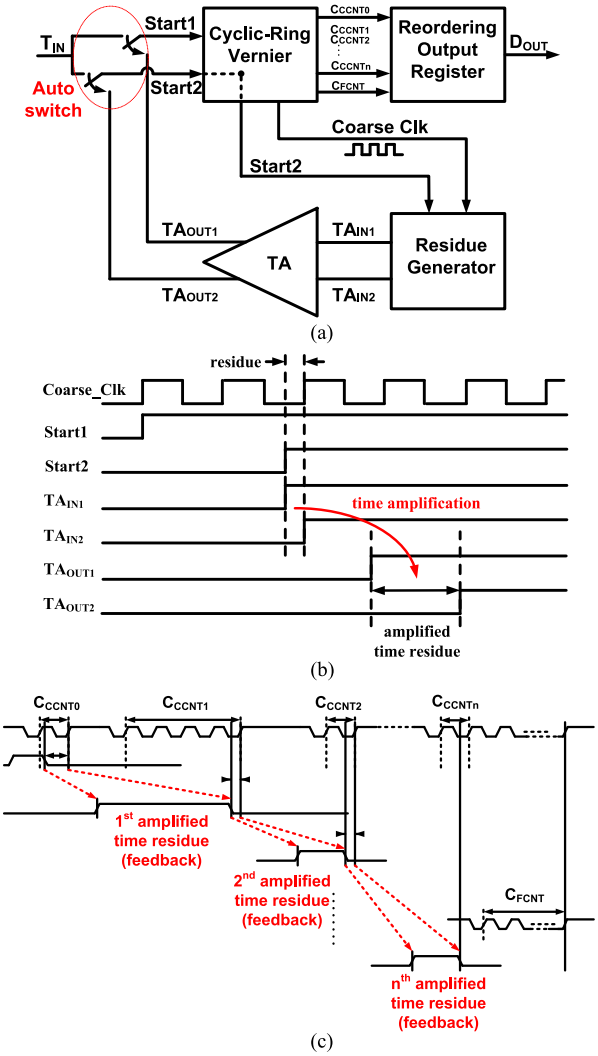


Fig. 3. Feedback TDC with single TA: (a) block diagram; (b) time-residue interval; and (c) feedback operation.

accumulated and feedback cycles. Notably, the feedback cycle is limited by the convert latency and expected TA gain.

The major advantage of the proposed feedback scheme is the effective accumulated TA gain. The final TDC output is

$$C_{\mathrm{TDC}} = (C_{\mathrm{CCNT0}} + 1) - C_{\mathrm{AR}_{1\mathrm{st}}}/G_{\mathrm{TA}} \tag{2}$$

where C_{TDC} is the overall output, C_{CCNT0} is the initial coarse conversion, $C_{\mathrm{AR}_{1\mathrm{st}}}$ is the conversion of the amplified time residue, and G_{TA} is the TA gain. The first amplified interval after TDC is

$$C_{\mathrm{AR1st}} = (C_{\mathrm{CCNT1}} + 1) - C_{\mathrm{AR2nd}}/G_{\mathrm{TA}} \tag{3}$$

where C_{CCNT1} is the coarse conversion of the amplified interval and $C_{\mathrm{AR}_{2\mathrm{nd}}}$ is the conversion of the second time-residue feedback. The general representation of the amplified time residue is

$$C_{\mathrm{AR}_{n-1\mathrm{th}}} = \left(C_{\mathrm{CCNT}(n-1)} + 1\right) - C_{\mathrm{AR}_{n\mathrm{th}}}/G_{\mathrm{TA}} \tag{4}$$

where no further amplification of the time residue is conducted, but the fine conversion is executed. $C_{\mathrm{CCNT}n}$ and C_{FCNT} represent the coarse and fine conversions, respectively. This time residue is the recursion of the amplified interval. In the final feedback (*n*th) cycle, the conversion of the *n*th amplified time residue and the accumulated TA gain become

$$C_{\mathrm{AR}_{n\mathrm{th}}} = C_{\mathrm{CCNT}n} + C_{\mathrm{FCNT}} \tag{5}$$

$$G_{\mathrm{CAS}} = G_{\mathrm{TA}}^{n} \tag{6}$$

where n is the number of feedback cycles. The actual resolution is derived as the propagation delay in the cyclic-ring Vernier, divided by the accumulated gain of TA after the *n*th feedback cycle

$$R_{\mathrm{TDC}} = \tau / G_{\mathrm{CAS}} \tag{7}$$

where τ is the fine step of the cyclic-ring Vernier and G_{CAS} is the accumulated TA gain after the *n*th feedback. Each feedback conversions is inputted to the ordering output register serially, and it is subsequently outputted in parallel when all feedback cycles are complete.

If the time-residue feedback TDC is simplified to involve only one feedback cycle, the proposed feedback loop can be switched OFF to amplify the time residue only once and to simplify our TDC operations. Although it is similar to the two-stage TDC [14], [26], the cyclic-ring Vernier must be operated twice. Initially, the ring generates the coarse result, and the single TA amplifies the time residue. Subsequently, the ring engenders the fine conversion of the amplified interval again. Its formulas are presented as follows:

$$\mathrm{C}_{\mathrm{TDC}} = (C_{\mathrm{CCNT0}} + 1) - C_{\mathrm{AR}}/G_{\mathrm{TA}} \tag{8}$$

$$C_{\mathrm{AR}} = C_{\mathrm{CCNT1}} + C_{\mathrm{FCNT}} \tag{9}$$

where C_{AR} is the conversion result of the amplified time residue.

B. Signal Flow

Fig. 4 illustrates the feedback flow, which amplifies the time residue and feeds back to the cyclic-ring Vernier. In each cycle, the proposed TDC produces a coarse conversion and generates a new amplified time residue for the next run; if latency is unlimited, the time residue can be subsequently amplified and fed back until the new time residue is less than the buffer propagation delay of the cyclic-ring Vernier. The details are described as follows.

The signal $\mathrm{TA}_{\mathrm{EN}}$ switches between the ordinary cyclic-ring Vernier and the time-residue feedback TDC. If the signal $\mathrm{TA}_{\mathrm{EN}}$ is 0 in the initial state, it is an ordinary cyclic-ring Vernier; otherwise, it is a time-residue feedback TDC, where $\mathrm{TA}_{\mathrm{EN}}$ is 1 to enable the TA, and to switch the input path to feedback mode. The operation of the time-residue feedback TDC involves several coarse conversions, but only one fine conversion, which operates during the final loop. Furthermore, the input interval is composed of two edges. The first edge is the signal Start1 (which initiates the coarse oscillator), and the second edge is the signal Start2 (which terminates the coarse oscillator at the next rising edge of the coarse clock). The result of the coarse conversion is stored in the coarse counter while the time residue is generated. The coarse oscillator operates again when the amplified time

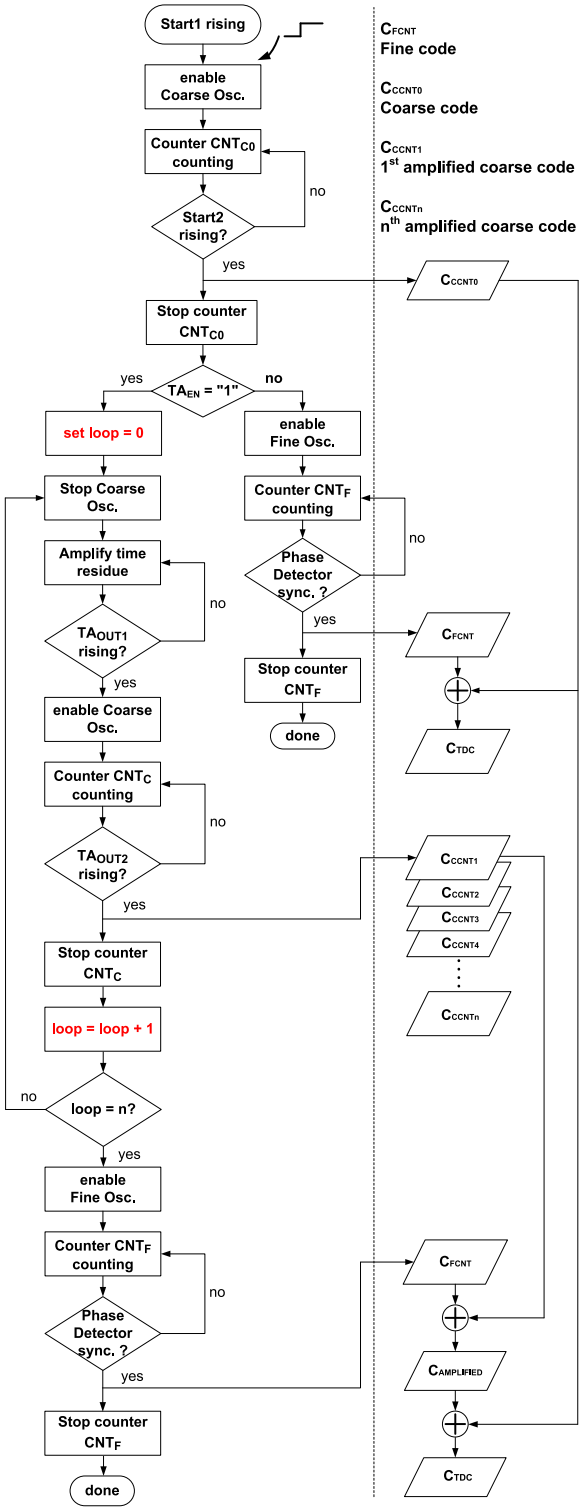


Fig. 4. Flowchart of proposed time residue feedback TDC.

residue is fed back into the input path. However, the coarse oscillator is suspended during the amplification process, and this saves power and reduces the noise, because of the minimized transient current (single TA). $\mathrm{TA_{IN1}}$ and $\mathrm{TA_{IN2}}$ are generated by residue generator and amplified by TA, namely $\mathrm{TA_{OUT1}}$ and $\mathrm{TA_{OUT2}}$. Both $\mathrm{TA_{OUT1}}$ and $\mathrm{TA_{OUT2}}$ are the inputs of the

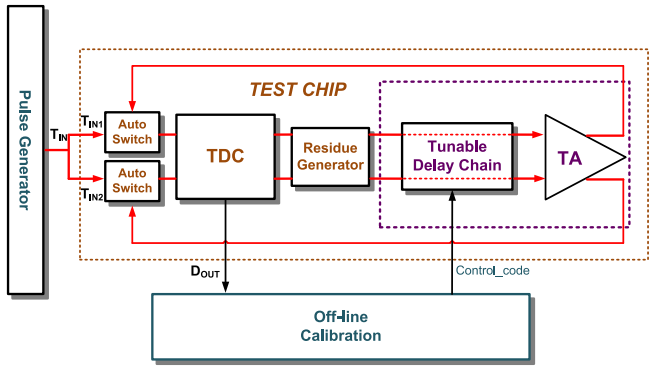


Fig. 5. Block diagram of offline calibration.

coarse oscillator and fine oscillator of TDC after autoswitch, respectively. During the final loop, $\mathrm{TA_{OUT1}}$ starts the coarse oscillator and coarse counter, and $\mathrm{TA_{OUT2}}$ terminates the coarse counter and starts the fine oscillator for fine conversion. One cyclic-ring Vernier and one TA are then used to measure the amplified pulse of a coarse conversion. Because of the feedback structure, the TA gain accumulates to amplify the time residue and enhance the TDC resolution. Several coarse conversions and one fine conversion are performed during recursive feedback. The flowchart as shown in Fig. 4 indicates both coarse conversion and fine conversion. C_{CCNT0} is the coarse conversion in the initial cycle. C_{CCNT1}, C_{CCNT2} , . . . , $C_{\mathrm{CCNT}n}$ are the coarse conversion in the first, second, . . . , nth feedback cycles, respectively, and C_{FCNT} is the fine conversion in the final feedback (nth) cycle. The reordering output register will combine all coarse conversions and one fine conversion in the final feedback cycle, otherwise we only get the coarse conversion and time residue for the next feedback.

C. Offline Calibration

In the proposed design, an offline calibration is provided to eliminate the distortion caused by PVT variation [31], [32]. This calibration process also corrects the TA gain as expected and adjusts the conversion result derived from the TDC. The precise TDC with high resolution needs good differential nonlinearity (DNL). Through the calibration, the good DNL is achieved and the resolution of TDC can be maintained. The chip is an IP for system-on-a-chip solutions, because the route passes through the interface of IPs, and matching the input paths facilitates achieving TDC performance. In our test chip, the calibration is offline as displayed in Fig. 5, where the external *pulse generator* generates the specified input pulse for calibration. The *offline calibration* calculates the data converted from TDC and transfers the control codes to a *tunable delay-chain*. The reference parameter obtained from the calibration process for the expected TA gain and ideal TDC is saved for operational adjustment.

IV. Circuit Designs

A. Feedback TDC

As illustrated in Fig. 6(a), our design involves a cyclic-ring Vernier, a counter ($\mathrm{CNT_{C0}}$), a residue generator, a TA, an

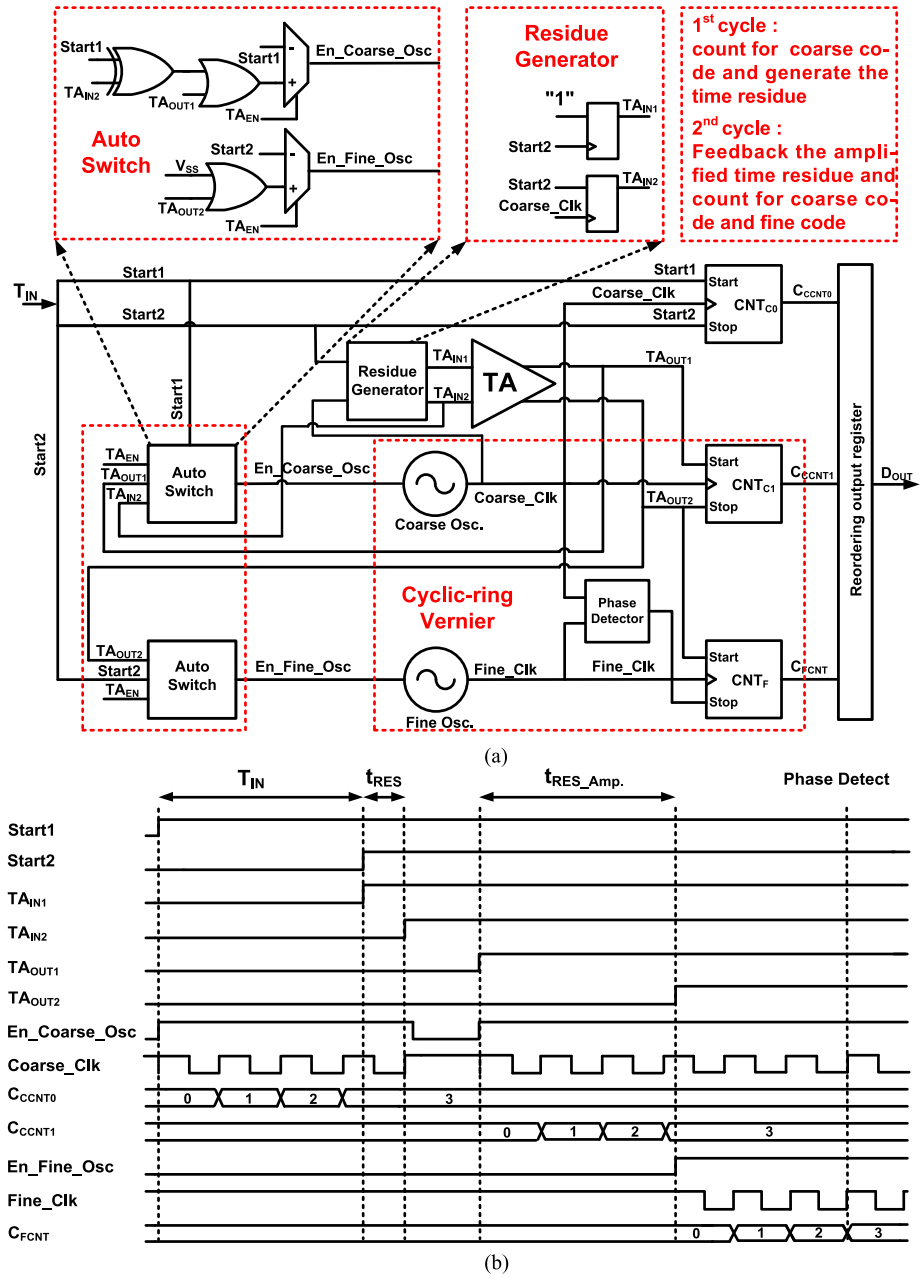


Fig. 6. Proposed feedback TDC with a cyclic-ring Vernier reusing: (a) schematic and (b) timing diagram.

autoswitch, and a reordering output register. The autoswitch, implemented with XOR and OR gates, and controlled by $\mathrm{TA_{EN}}$, changes the data path to an initial feedforward or feedback loop. If $\mathrm{TA_{EN}}$ is 0, the TDC is an ordinary cyclic-ring Vernier and the data path is initially fed forward to measure the input signal (without a TA and feedback loop). If $\mathrm{TA_{EN}}$ is 1, the TDC is the time-residue feedback TDC, where the reordering output register receives the code of counters in serial and transmits the data in parallel. The cyclic-ring Vernier is composed of two oscillators, a phase detector, and two counters (CNT_{C1} and CNT_F). Notably, the counter (CNT_{C0}) is an extended part of cyclic-ring Vernier for coarse count. In cyclic-ring Vernier, both coarse and fine oscillators, realized by DCOs, are used to generate coarse and fine clocks. The phase detector detects the signal precisely and synchronously. The cyclic-ring Vernier adopts a counter to extend the input range. The counters CNT_{C0} and CNT_{C1} have 3 bits, the counter CNT_F has 10 bits. The counter CNT_{C0} is for the coarse conversion in the first (feedforward) cycle, whereas the counters CNT_{C1} and CNT_F are the coarse and fine conversions, respectively, in the second (feedback) cycle. The residue generator derives the time residue by using input interval end against the next rising edge of the coarse clock. Moreover, the TA is designed based on set–reset (SR) latches with tunable delay chains. Because of the low TA gain implementation, the test chip is limited to only one complete feedback cycle (comprising the initial feedforward cycle and the corresponding feedback

cycle). It means that there are only two cycles in operations: one is the initial feedforward (first cycle) and the other is the feedback (second cycle).

Fig. 6(b) indicates the timing diagram of the proposed feedback TDC. In the first cycle (feedforward) of the time-residue feedback TDC, the first edge of the interval, named *Start1*, activates the coarse oscillator and the counter CNT_{C0}. Subsequently, the second edge of the interval, named *Start2*, deactivates the coarse oscillator by the signal $\mathrm{TA}_{\mathrm{IN2}}$ derived from the next rising edge of the coarse clock when *Start2* is valid. The residue generator then creates the time residue from the rising edge of signal *Start2* to the next rising edge of coarse clock. The time residue interval involves two edges for the TA to obtain the amplified time residue, named $\mathrm{TA}_{\mathrm{IN1}}$ and $\mathrm{TA}_{\mathrm{IN2}}$. During the second cycle (feedback), the time residue is amplified and fed back into the cyclic-ring Vernier for the second conversion. The signal En_Coarse_Osc is thus a combined result of the signals Start1, $\mathrm{TA}_{\mathrm{IN2}}$, and $\mathrm{TA}_{\mathrm{OUT1}}$. The signals Start1 and $\mathrm{TA}_{\mathrm{OUT1}}$ enable the coarse oscillator and the signal $\mathrm{TA}_{\mathrm{IN2}}$ disables the coarse oscillator. The signal En_Fine_Osc is the combined result of the signals Start2 and $\mathrm{TA}_{\mathrm{OUT2}}$. The signal Start2 enables the fine oscillator when $\mathrm{TA}_{\mathrm{EN}}$ is 0 and the signal $\mathrm{TA}_{\mathrm{OUT2}}$ enables the fine oscillator when $\mathrm{TA}_{\mathrm{EN}}$ is 1. The counting result of the first cycle is C_{CCNT0}, and this cycle contributes only to the coarse conversion. The remaining residue time is inputted to the TA for time amplification and feedback. The counting results of the second cycle are C_{CCNT1} and C_{FCNT}. After time-residue amplification, $\mathrm{TA}_{\mathrm{OUT1}}$ triggers the coarse oscillator for the counter CNT_{C1}, then $\mathrm{TA}_{\mathrm{OUT2}}$ terminates the coarse counter CNT_{C1} and triggers the fine oscillator for the counter CNT_{F} to obtain the fine conversion code C_{FCNT}. The fine counter is terminated by the synchronized signal of the phase detector.

Because *Start1* is the beginning of the interval and *Start2* is the end of the interval, the input interval is calculated as the time remaining to the next rising edge of the coarse clock minus the time residue

$$T_{\mathrm{IN}} = tCK_C \cdot (C_{\mathrm{CCNT0}} + 1) - t_{\mathrm{RES}} \tag{10}$$

where tCK_C is the clock period of the coarse ring and t_{RES} represents the time residue. The counting result is C_{CCNT0}, and then t_{RES} is

$$t_{\mathrm{RES}} = (tCK_C \cdot C_{\mathrm{CCNT1}} + \tau \cdot C_{\mathrm{FCNT}})/G_{\mathrm{TA}} \tag{11}$$

where the counting numbers of the coarse and fine clocks are C_{CCNT1} and C_{FCNT}, respectively. G_{TA} is the TA gain and the cycle time of the coarse clock is tCK_C. The fine conversion is τ which is the time difference between the period of the coarse and fine oscillators. The resolution R_{PD} is

$$R_{\mathrm{PD}} = \tau / G_{\mathrm{TA}} \tag{12}$$

where τ is the minimum buffer delay of the cyclic-ring Vernier and G_{TA} is the TA gain.

B. Subcircuits

1) Time Amplifier: We use a tunable SR-based TA [33]–[35] where delay chains and loading capacitors are settable to prevent circuit mismatches, as displayed in Fig. 7(a). The signal $\mathrm{TA}_{\mathrm{IN2}}$ is transmitted to the SR-latch component SR_1 faster than the signal $\mathrm{TA}_{\mathrm{IN1}}$ is transmitted. Additionally, the transition of R_1 occurs ahead of the S_1 transition. The later the transition of $\mathrm{TA}_{\mathrm{IN2}}$ from 0 to 1 occurs, the less time difference there is between $\mathrm{TA}_{\mathrm{IN1}}$ and $\mathrm{TA}_{\mathrm{IN2}}$ arriving at SR_1. Thus, a longer metastable time of SR_1 results in a longer R_1 transition (from 0 to 1), as well as a longer T_{OUT}. If the delay chain T_{OFF} is longer, the time difference between $\mathrm{TA}_{\mathrm{IN1}}$ and $\mathrm{TA}_{\mathrm{IN2}}$ arriving at SR_1 is wider. Moreover, if the metastable state is shorter, the amplified time T_{OUT} is also shorter. Specifically, the gain G_{TA} is lower if the delay chain T_{OFF} is longer. If the input pulse T_{IN} is longer than T_{OFF}, the signal $\mathrm{TA}_{\mathrm{IN1}}$ arrives at SR_1 faster than the signal $\mathrm{TA}_{\mathrm{IN2}}$ does. A longer T_{IN} renders the metastable state shorter because of the later $\mathrm{TA}_{\mathrm{IN2}}$. The characteristic curve of T_{IN} versus T_{OUT} is not in the finite linearity error region when the input interval is out of range [see Fig. 7(b)]. The input range is limited by

$$-T_{\mathrm{OFF}} < T_{\mathrm{IN}} < T_{\mathrm{OFF}} \tag{13}$$

meaning that the input interval T_{IN} must be less than T_{OFF} in Fig. 7(a). The delay time is the multiplier of *R* and *C*, where *R* is the intrinsic resistance of the standard cell and *C* is the total parasitic and additional capacitances considered in the design. The delay time is prolonged through the additional capacitances.

The TA gain is directly proportional to the capacitance and is inversely proportional to the input delay T_{OFF}. To achieve a wider input range, T_{OFF} involving additional delay chains is required; however, this involves a larger area and reduces the overall TA gain. A high capacitance is thus necessary to achieve

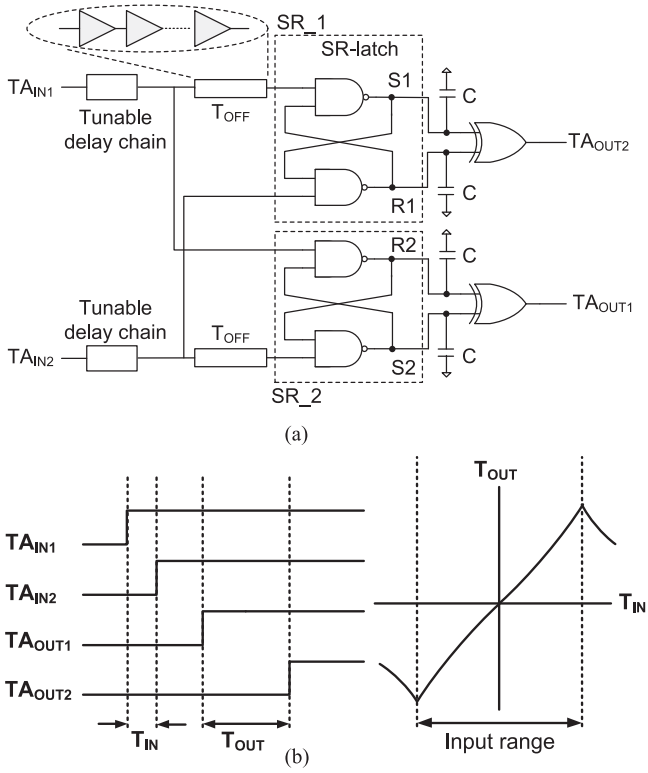


Fig. 7. Proposed TA: (a) schematic and (b) timing diagram.

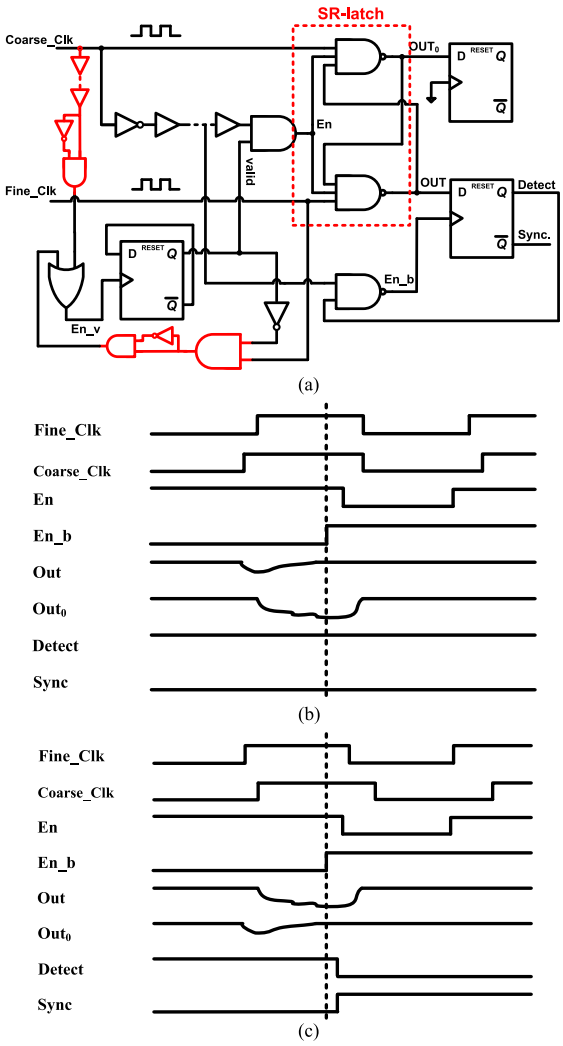


Fig. 8. Proposed phase detector: (a) schematic; (b) timing diagram of phase tracking; and (c) timing diagram after phase locked.

both a high gain and wide input range, which is expensive in VLSI implementations. The time residue must be shorter than the TA input range to ensure the finite linearity error. In addition, the input delay chains T_{OFF} for both SR-latches must be well-matched to make the curve of T_{IN} versus T_{OUT} pass through the original point; that is, T_{OUT} is zero if T_{IN} is zero. Moreover if the capacitance for both SR-latches is not appropriately matched, the gain becomes inconsistent in the entire input range—adequately matching the placement and routing are also imperative. In this study, the input range of TA is 900 ps and its gain is 6.1.

2) Phase Detector: Fig. 8(a) depicts the proposed phase detector with an SR-latch. Compared with D flip-flop, the metastability of SR-latch is effective to reduce the dead zone, because we can cascade a D flip-flop and delay to sense the output of SR-latch after a sufficient delay; this is advantageous because it enables the detection of the precise timing for the fine conversion and enhances the TDC resolution. Thus, this study detects the exact timing of synchronization between the fine and coarse clocks, and maintains the latched state until the signal is

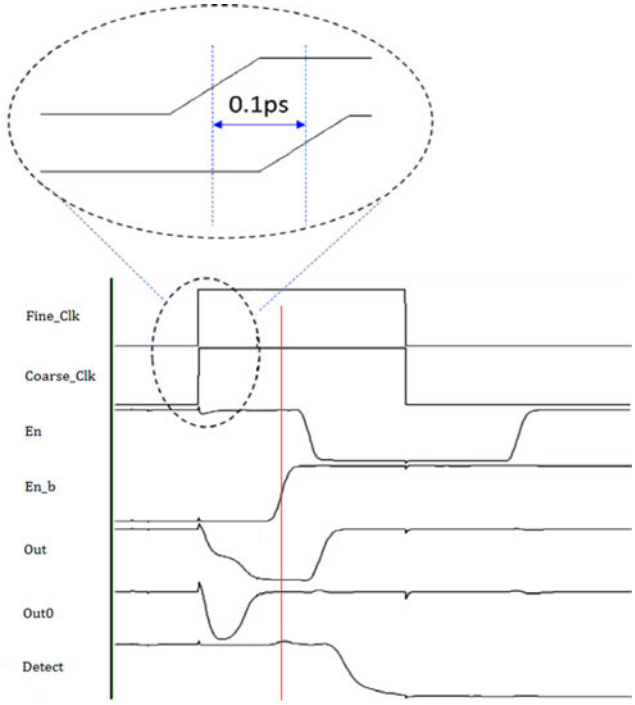
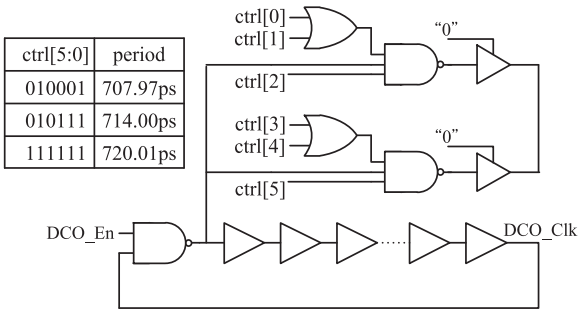


Fig. 9. Simulation result of the proposed phase detector.

reset to start for the next detection. This avoids toggling of the signal Sync and influences the counting results of the fine code. Fig. 9 presents the simulations of the Fine_Clk and the Coarse_Clk synchronized that the dead zone approaches subpicosecond by using the hard macro with semifully custom of cell placements and interconnection to ensure matching well.

a) Phase tracking: The timing diagram for a scenario in which coarse clock is ahead of fine clock, as plotted in Fig. 8(b). The signal Sync, which stops the fine counter, is always maintained at a low state when the phase synchronization is not completed. When Coarse_Clk approaches the phase detector slightly faster than Fine_Clk does, the signal Out_0 is transmitted from 1 to 0 and the SR-latch is transformed into a metastable state. After the developing, the signal Out is approaching to the state 1 and the signal En_b triggers the D flip-flop to latch the state of signal Out. Moreover, when the signal Detect is maintained in state 1 and the signal Sync is maintained in state 0, the phase detection operation is incomplete. Subsequent to the phase detection process, the signal En transitions to 0, and the signal Out_0 and Out transitions to 1 to await the next detection.

b) Phase locked: Fig. 8(c) illustrates a timing diagram for a scenario in which the fine clock synchronizes with the coarse clock; the signal Sync is generated when the phase detection is completed. When Fine_Clk approaches the phase detector slightly faster than Coarse_Clk does, the signal Out transitions to 0 slightly earlier than the signal Out_0 does, and the SR-latch is converted to a metastable state. When the synchronization is completed, the signal En_b triggers the D flip-flop to latch the comparison result. Subsequently, the signal Sync transitions to 1 and stops the fine counter. Concurrently, the signal Detect transitions to 0, and the signal En_b is set constant to prevent



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010001	707.97ps
010111	714.00ps
111111	720.01ps

Coarse Osc. Ctrl[5:0]	Fine Osc. Ctrl[5:0]	Fine step	Fine step/TA_gain
111111	010111	6.01ps	0.98ps
111111	010001	12.04ps	1.97ps

Fig. 10. Proposed variable-resolution DCO.

the signal Sync from being altered by the jitters in the next cycle. The signal Sync is thus maintained at the state 1 until reset occurs.

3) Variable-Resolution DCO: Fig. 10 presents a variable-resolution DCO that comprises buffers and a negative-AND (NAND) gate, as delay chains [40], [41]. One of the input devices in the NAND gate is a button for enabling the oscillator. Two OAI cells provide the loading capacitance, and each cell is assigned three control codes to modify the capacitance. The tunable capacitance changes the slew rate of the transition and adjusts the delay time. The variable period and frequency are obtained by changing the control codes. The OAI cell includes four input pins, each connected to the gate of one PMOS and one NMOS. The gate capacitance is changed through the applied voltage. Furthermore, the intrinsic resistance altered through the applied voltage influences the gate capacitance. The control codes apply various voltages to other input gates and change the status of the loading capacitances. This subsequently modifies the slew rate and yields a distinct clock period. Both the coarse and fine oscillators are implemented through the same circuit with diverse control codes in the cyclic-ring Vernier, indicating that the TDC resolution is programmable. For example, a control code of [111111] for coarse oscillator and a control code of [010001] for fine oscillator result in a 12.04-ps fine resolution. Conversely, in this study, the control codes for the coarse and fine oscillators set at [111111] and [010111], respectively. A 6.01-ps fine resolution represents the period difference between the coarse and fine rings, and the TDC resolution is 0.98 ps. Notably, the resolution level is influenced by jitter, which is largely contributed by power and ground bouncing. Thus, a substantial chip area is dedicated to the implementation of a decoupling capacitance in the test chip to effectively reduce the jitters caused by power and ground bouncing.

V. Performance Evaluation

A. VLSI Implementation and Measurements

The proposed feedback TDC is implemented in a TSMC 65-nm digital CMOS process with a 1-V supply voltage to ensure a resolution of 0.98 ps and power consumption of only 3 mW. In the cyclic-ring Vernier, the DCO period is 708–720 ps. Moreover, the bandwidth is 10 MHz and the input range is 5.76 ns (720 ps $\times$ 8 = 5.76 ns). The phase detector is placed at the intermediate position of the coarse and fine oscillators for layout matching. The width and height of the chip are 500 and 400 μm, respectively, occupying an area of 0.02 mm^2. Two clock inputs with a 0.02-Hz frequency difference at 10 MHz are then applied to generate a ramp input for INL and DNL. The measured results reveal that DNL is $\pm$ 0.8 LSB and INL is $\pm$ 2.2 LSB, as displayed in Fig. 11. When the ring oscillators are turn ON and OFF, the fine resolution error can be large depending on the initial phases after the turn ON. Furthermore, it can be

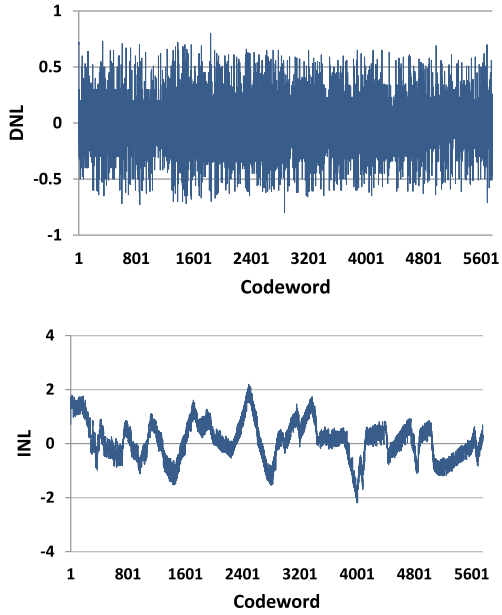

Fig. 11. Measurements of DNL and INL.

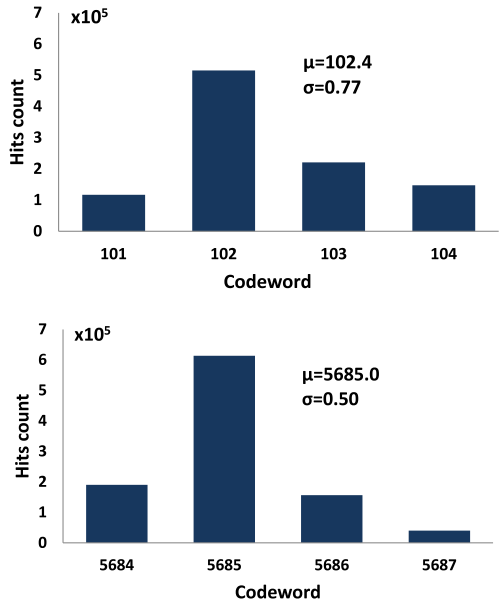

Fig. 12. Single shot measurement at both ends of TDC.

TABLE I
COMPARISON OF THE DESIGNED FEATURES

	JSSC'11 [17]	JSSC'12 [28]	TCASII'14 [15]	JSSC'14 [27]	JSSC'15 [30]	This Work
Scheme	Cyclic-ring Vernier	Cyclic	Vernier delay-line	True Pipeline	Delta-sigma	Time-Residue Feedback
Technology	65 nm	0.13 μm	65 nm	65 nm	65 nm	65 nm
Area (mm^2)	0.02	0.07	0.004	0.14	0.03	0.02
Resolution	5.5 ps	1.25 ps	5.7 ps	1.12 ps	2.64 ps	$*$0.98 ps $**$6.01 ps
Bits	15	N/A	7	9	N/A	13
Range	100 ns	0.16 ns	0.73 ns	578 ps	5.4 ns	5.76 ns
Supply	1 V	1.3 V	1.2 V	1.2 V	1 V	1 V
Power	1.4 mW @10 MS/s	4.3 mW @50 MS/s	1.14 mW @100 MS/s	15.4 mW @250 MS/s	3.52 mW @150 MS/s	$*$3.0 mW@10 MS/s $**$17.5 mW@250 MS/s
DNL/INL (LSB)	N/A	0.7/–3$\sim$+1	N/A	0.6/1.7	N/A	0.8/2.2

$*$Feedback mode.
$**$Feedforward mode.

accumulated in the feedback TDC architecture. As a result, INL can be larger than the DNL, as shown in measurement results. The single shot measurement at both ends of the TDC is illustrated in Fig. 12. The jitter impact is not always proportional to the amplified time interval in the proposed feedback scheme. The simulation of the TA gain indicates that the gain is distributed between 6.05 and 6.15, with a maximum error of 0.05 and linearity error of 0.82%. Notably, the gain error variety is strong in some input ranges and minimal in other range; this is one factor that DNL is diverse and has some little spikes. Table I presents a comparison of the proposed TDC with cyclic-ring Vernier, cyclic, Vernier delay-line, pipeline, and delta-sigma TDCs. Overall, the proposed design is characterized by higher resolution (because of time amplification), a small chip area, a wide input range, and low power, it is also capable of noise reduction. Additionally, our TDC is smaller than the cyclic and pipeline TDC because of its efficient time residue feedback scheme, and exhibits a wide input range attributed to the cyclic-ring Vernier scheme. The input range is determined by the counter bits, and the suspension of the oscillator during TA development produces limited power. However, the drawback of the feedback TDC includes a low sampling rate in conversion and a considerable latency of feedback switching. Thus, according to the proposed time-residue feedback TDC, we can change the path to a feedforward path (i.e., TA switched OFF) to obtain a high sampling rate directly. Our test chip includes both feedback and feedforward, and Fig. 13 presents a microphotograph of the chip.

B. Discussion

The autoswitch only uses one XOR gate, two OR gates, and two multiplexers to transport the signal from the initial input to the feedback path. The chip requires only 0.02mm^2 for automatic placement and routing, which is markedly smaller than the space required by cyclic [28] and pipeline [25], [27] TDCs for amplifying the time residue demonstrated in this study. The design for both cyclic and pipeline TDCs requires a DTC and subtractor to retrieve the time residue. In the proposed design, the time residue is generated by using two flip-flops and transferred to the TA directly. The flip-flops occupy a much smaller

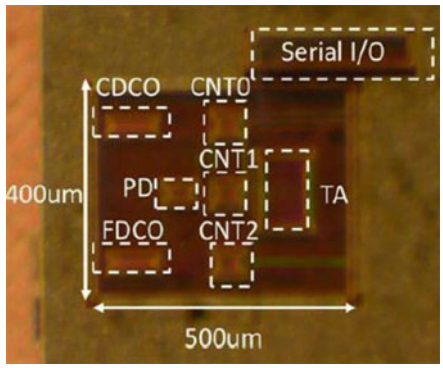

Fig. 13. Chip photograph of the proposed ASIC.

area than the DTC and subtractor do, as does the chip area compared with the novel design of delta-sigma TDC [30]. The feedback of amplified intervals using the same cyclic-ring Vernier also saves space. In Table I, both Vernier delay-line [15] and the ordinary cyclic-ring Vernier [17] have good power consumptions, but our design supports two modes in a single TDC to balance resolution and cost. Of course, additional power of TA is required. Chip measurements indicate that a high-gain TA and cyclic-ring Vernier with precise fine steps provides the expected resolution and a wide input range. In feedback mode, the low sampling rate is due to the latency of TA development and input path switching. A higher resolution with smaller step periods requires more time for fine count. Conversely, the power is 17.5 mW at a sampling rate of 250 MS/s. Because the proposed design generates the time residue from the end of interval to the rising edge of next cycle by using two flip-flops rather than subtractor and DTC, we save significant area.

VI. CONCLUSION

A cost-effective TDC using a new time-residue feedback structure was proposed and implemented with cell-based CMOS technology. By applying one variable-resolution cyclic-ring Vernier and one tunable delay-chain TA recursively, we balanced the resolution, power dissipation, and chip area. To improve turnaround efficiency and mitigate circuit mismatches, we

also used a variable-period DCO (which created programmable resolution in the cyclic-ring Vernier as well) for coarse and fine oscillators (with different control codes). Furthermore, we reduced the noise and jitter by switching the oscillators OFF during TA activities. Because offline calibration ensures adequate matches and high accuracy, our design is suitable for implementation with hardware description language and automatic placement and routing using a digital cell library. The test chip involving feedback and feedforward operations, as implemented in TSMC 65-nm digital CMOS process, occupied 0.02 mm^2. In feedback mode, its resolution was 0.98 ps, with a 5.76-ns input range. It consumed 3 mW at a 10-MHz sampling rate, and 1-V supply voltage. This prototyping circuit hints the proposed feedback scheme is working properly.

REFERENCES

[1] S. Kimx *et al.*, "A 2 GHz synthesized fractional-N ADPLL with dual-referenced interpolating TDC," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 391–400, Nov. 2015.

[2] A. Hamza, S. Ibrahim, M. EL-Nozahi, and M. Dessouky, "A wideband 5 GHz digital PLL using a low-power two-step time-to-digital converter," in *Proc. IEEE Int. Conf. Electron., Circuits, Syst.*, Dec. 2015, pp. 328–331.

[3] F. Opteynde, "A 40nm CMOS all-digital fractional-N synthesizer without requiring calibration," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 1–3.

[4] D. Zhang *et al.*, "A fast-locking digital DLL with a high resolution time-to-digital converter," in *Proc. IEEE 2013 Custom Integr. Circuits Conf.*, Sep. 2013, pp. 22–25.

[5] Y. Urano, W. J. Yun, T. Kuroda, and H. Ishikuro, "A 1.26Mw/Gbps 8 locking cycles versatile all-digital CDR with TDC combined DLL," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2013, pp. 1576–1579.

[6] Y. Han, W. Rhee, and Z. Wang, "A PVT-insensitive self-dithered TDC design by utilizing a $\Delta\Sigma$ DLL," in *Proc. IEEE 55th Int. Midwest Symp. Circuits Syst.*, Aug. 2012, pp. 542–545.

[7] P. Palojarvi, K. Maatta, and J. Kostamovaara, "Integrated time-of-flight laser radar," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 4, pp. 996–999, Aug. 1997.

[8] J. H. Yu, M. K. Park, and S. W. Kim, "A 2ps minimum-resolution, wide-input-range time-to-digital converter for the time-of-flight measurement using cyclic technique and time amplifier," in *Proc. IEEE Int. Conf. Consum. Electron.*, Jan. 2016, pp. 151–152.

[9] Z. Cheng, X. Zheng, M. J. Deen, and H. Peng, "A low-power gateable Vernier ring oscillator time-to-digital converter for biomedical imaging applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 445–454, Apr. 2016.

[10] Y. Kim and T. W. Kim, "An 11 b 7 ps resolution two-step time-to-digital converter with 3-D Vernier space," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 61, no. 8, pp. 2326–2336, Feb. 2014.

[11] S. Kurtti and J. Kostamovaara, "An integrated laser receiver channel utlilizing a time-domain walk error compensation scheme," *IEEE Trans. Instrum. Meas.* vol. 60, no. 1, pp. 146–157, May 2012.

[12] H. J. Kwon, J. S. Lee, J. Y. Sim, and H. J. Park, "A high-gain wide-input range time amplifier with an open-loop architecture and a gain equal to current bias ratio," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2011, pp. 325–328.

[13] S. Ok *et al.*, "A dc-dc converter with a dual VCDL-based ADC and a self-calibrated DLL-based clock generator for an energy-aware EISC processor," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 551–554.

[14] M. Lee and A. A. Abidi, "A 9b, 1.25ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.

[15] N. U. Anderson and M. Vesterbacka, "A Vernier time-to-digital converter with delay latch chain architecture," *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 61, no. 10, pp. 773–777, Oct. 2014.

[16] R Rashidzadeh, M. Ahmadi, and W. C. Miller, "An all-digital self-calibration method for a Vernier-based time-to-digital converter," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 2, pp. 463–469, Feb. 2010.

[17] Y. Park and D. D. Wentzloff, "A cyclic Vernier TDC for ADPLLs synthesized from a standard cell library," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 58, no. 7, pp. 1511–1517, Jul. 2011.

[18] M. Kim *et al.*, "High-resolution and wide-dynamic range time-to-digital converter with a multi-phase cyclic Vernier delay line," in *Proc. IEEE ESSCIRC*, Sep. 2013, pp. 311–314.

[19] J. Yu, F. F. Dai, and R.C. Jaeger, "A 12-bit Vernier ring time-to-digital converter in 0.13 um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 830–842, Apr. 2010.

[20] B. Zhou, Y. He, and P. Luo, "A high PVT tolerance TDC with symmetrical Vernier delay ring," in *Proc. 11th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, Oct. 2012, pp. 1–3.

[21] M. Kang and J. Burm, "Time-domain temperature sensor using two stae Vernier type time to digital converter for mobile application," in *Proc. IEEE Int. SoC Des. Conf.*, Nov. 2012, pp. 431–434.

[22] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.

[23] Y. H. Seo, J. S. Kim, H. J. Park, and J. Y. Sim, "A 0.63ps resolution, 11b pipeline TDC in 13um CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2011, pp. 152–153.

[24] M. Z. Straayer and M. H. Perrott, "An multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, Apr. 2009.

[25] J. S. Kim, Y. H. Seo, Y. Suh, H J. Park, and J.Y. Sim, "A 300-MS/s,1.76-ps-resolution, 10-b asynchronous pipelined time-to-digital converter with on-chip digital background calibration in 0.13 um CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 516–526, Oct. 2012.

[26] K. S. Kim, Y. H. Kim, W. S. Yu, and S. H. Cho, "A 7b, 3.75 ps resolution two-step time-to-digital converter in 65nm CMOS using pulse-train time amplifier," in *Proc. Symp. VLSI Circuits*, Jun. 2012, pp. 192–193.

[27] K. S. Kim, W. S. Yu, and S. H. Cho, "A 9 bit, 1.12 ps resolution2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, Jan. 2014.

[28] Y. H. Seo, J. S. Kim, H. J. Park, and J. Y. Sim, "A 1.25ps resolution 8b cyclic TDC in 0.13 um CMOS, " *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 736–743, Dec. 2011.

[29] S. J. Kim, T. Kim, and H. Park, "A 0.63ps, 12b, synchronous cyclic TDC using a time adder for on-chip measurement of a Soc in 28nm CMOS technology," in *Proc. Symp. VLSI Circuits*, Jun. 2014, pp. 1–2.

[30] W. Yu, K. S. Kim, and S. H. Cho, "A 0.22 ps rms integrated noise 15 MHz bandwidth fourth-order $\Delta\Sigma$ time-to-digital converter using time-domain error-feedback filter," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1251–1262, Feb. 2015.

[31] J. C. Lai and T. Y. Hsu, "Mismatch-tolerant time amplifier with embedded self-calibration," in *Proc. 5th IEEE Int. Conf. Consum. Electron.*, Sep. 2015, pp. 393–396.

[32] S. Mandai, T. Lizuka, T. Nakura, M. Ikeda, and K. Asada, "Time-to-digital converter based on time difference amplifier with non-linearity calibration," in *Proc. IEEE ESSCIRC*, Sep. 2010, pp. 266–269.

[33] A. M. Abas, A. Bystrov, D. J. Kinniment, O. V. Maevsky, G. Russell, and A. V. Yakovlev, "Time difference amplifier," *Electron. Lett.*, vol. 38, no. 23, pp. 1437–1438, Nov. 2002.

[34] M. A. Abas, G. Russell, and D. J. Kimmiment, "Design of sub-10-picoseconds on-chip time measurement circuit," in *Proc. Des. Autom. Test Eur. Conf.*, vol. 2, 2004, pp. 804–809.

[35] C. P. Laura and P. Susana, "Time difference amplifiers to improve the dynamic range of MASH time encoded ADCs," in *Proc. 57th IEEE Int. Midwest Symp. Circuits Syst.*, Aug. 2014, pp. 177–180.

[36] T. Oh, H. Venkatram, J. Guerber, and U. K. Moon, "Correlated jitter sampling for jitter cancellation in pipelined TDC," in *Proc. Int. Symp. Circuits Syst.*, May 2012, pp. 810–813.

[37] D. W. Jee, B. Kim, H. J. Park, and J. Y. Sim, "A 1.9-GHz fractional-N digital PLL with subexponent $\Delta\Sigma$ TDC and IIR-based noise cancellation," *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 59, no. 11, pp. 721–725, Dec. 2012

[38] Y. Li, N. Xu, W. Rhee, and Z. Wang, "A 2.5GHz ADPLL with PVT-insensitive $\Delta\Sigma$ dithered time-to-digital conversion by utilizing an AD-DLL," in *Proc. Int. Symp. Circuits Syst.*, Jun. 2014, pp. 1440–1443.

[39] D. W. Jee, Y. H. Seo, H. J. Park, and J. Y. Sim, "A 2 GHz fractional-N digital PLL with 1b noise shaping $\Delta\Sigma$," in *Proc. Symp. VLSI Circuits*, Jun. 2011, pp. 116–117.

[40] W. Chaivipas, T. Ito, T. Kurashina, K. Okada, and A. Matsuzawa, "Fine and Wide frequency tuning digital controlled oscillators utilizing capacitance position sensitivity in distributed resonators," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 424–427.

[41] D.C. Lee *et al.*, "A low power all-digital PLL with power optimized digitally controlled oscillator," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, Dec. 2010, pp. 1–4.

Jung-Chin Lai was born in Taichung, Taiwan. He is currently working toward the Ph.D. degree in the Institute of Computer Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan.

He joined the National Chip Implementation Center, Hsinchu, in 2015. He has extensive experience in the field of DDR DRAM. He worked as a DDRIO and DDRPHY Designer with Global Unichip, Taiwan, during 2010–2015, and as a DDR2/3 DRAM Designer with Nanya Technology Corporation, Taiwan, during 2006–2009. He is also skilled in system-on-chip implementation, and has rich experience of system analysis, in particular, for noise inhibition.

Terng-Yin Hsu (M'07) received the B.S. and M.S. degrees from Feng Chia University, Taichung, Taiwan, in 1993 and 1995, respectively, and the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1999, all in electronics engineering.

In 2003, he joined the Department of Computer Science, National Chiao Tung University, where he is currently an Associate Professor. His current research interests include VLSI architectures, wireless communications, multi-spec transmissions, high-speed networking, analog-like digital circuits, system-on-a-chip design technology, and related application-specific integrated circuits designs.