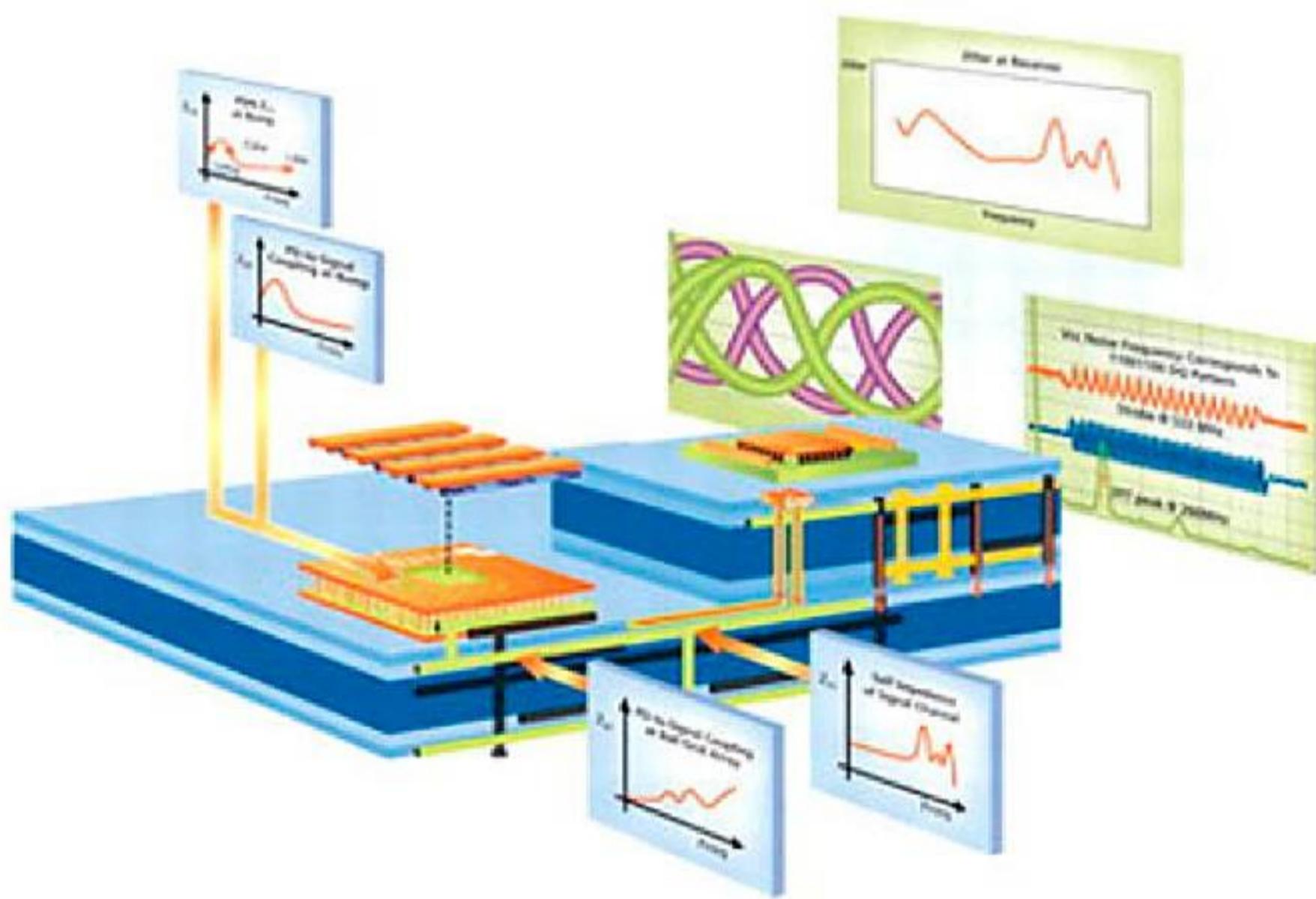


Power Integrity for I/O Interfaces: With Signal Integrity/Power Integrity Co-Design



Foreword by Joungho Kim

Vishram S. Pandit • Woong Hwan Ryu • Myoung Joon Choi

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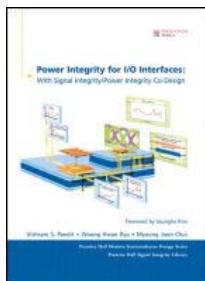
POWER INTEGRITY FOR I/O INTERFACES

**With Signal Integrity/
Power Integrity Co-Design**

Vishram S. Pandit
Woong Hwan Ryu
Myoung Joon Choi



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Power Integrity for I/O Interfaces: With Signal Integrity/Power Integrity Co-Design

By: Vishram S. Pandit; Woong Hwan Ryu; Myoung Joon Choi

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Dedication

We would like to dedicate this book to our families for their devotion, untiring support, and encouragement.

—Authors

Vishram S. Pandit thanks his wife, kids, parents, brother and family.

Woong Hwan Ryu thanks his wife Cindy; his kids Josh, Erin, Lauren, and Jacob; his parents, brothers, sisters, and family.

Myoung Joon Choi thanks his wife Joo Young and his daughter Giana, his parents, his brother and family.

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Foreword

With recent advancement of the semiconductor technology, microprocessors and System-On-Chip (SoC) products are taking advantage of cheaper production cost and the extended Moore's law. This has reinvigorated more widespread use of personal computing devices and consumer electronics devices. Most of these recent electronics systems are getting faster, smaller, and, are operating at lower power. In addition, the design cycle for products is getting shorter, putting more pressure on efficient design capability while the robust operation of devices is a definite requirement. The issues arising from these trends range from physical design, electromagnetic compatibility, electromagnetic interference, to thermal and power consumption reduction. The designers of the cutting-edge products try to manage all of these problems together while keeping the overall price down as much as possible. Too much over-design tends to make the system lose competitive edge, and under-design apparently makes the system lose its robustness.

Digital design portion of the semiconductor circuit design has advanced significantly since the advent of the transistor CAD design tools. However, for high-speed Input/Output (IO) interfaces, the digital signals pass through power and signal distribution networks, and analog effects become important. The advances in the analog signaling techniques—or more specifically, the advances in the signal and power integrity assurance techniques—had been relatively slow compared with digital design techniques. Electromagnetic effects occurring in the systems were not reflected very accurately in the earlier digital systems. With increase in operating frequencies, it became necessary to consider the transmission line and electromagnetic effects for signal quality and timing analysis. Availability of more accurate, faster, and more user-friendly electromagnetic simulation tools facilitated the signal integrity analysis.

Power integrity has been catching up with signal integrity in terms of tools, methodologies, and standardized techniques. The initial development of the power integrity techniques in the last decade focused largely on designing for low impedance power distribution networks. Commercial electromagnetic tools to model power networks started to come in the market in late 1990s. With the increase of system speeds and decrease in

operating voltages, it was required to design the power network to meet tighter noise tolerances. Simultaneously Switching Output (SSO) noise has become a major noise source, and its analysis and mitigation techniques have been developed. It is necessary to predict the effect of power noise on the receiver jitter. For today's I/O interfaces, operating at multi-Gbps data rates, voltage and timing margins are influenced by the Power Distribution Network (PDN) designs. This book describes a systematic comprehensive methodology for analyzing power integrity, and its impact on the I/O interface performance.

The signal and power integrity is moving faster toward the cheaper and more efficient solution, until the cost of the interference reduction or improved integrity adds up to competitive level. Whatever the means of signal transfer solutions are, the signal and power integrity analysis has been and will dictate significant portion of the system design. With increased system complexity and demand for the low-cost designs, it will become more and more important to analyze power/signal integrity concurrently.

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Preface

Power Integrity is becoming increasingly important in today's high-speed digital I/O systems. The cover of this book gives a high-level summary of its system impact. It shows an electronic system with a Printed Circuit Board (PCB), a daughter card, and their layer stackup. A driver chip is mounted on the PCB and a receiver chip is mounted on the daughter card. The expanded view of the power grid of the driver chip is also shown. The receiver jitter impact is due to Power Delivery (PD) to signal coupling, and there are different coupling mechanisms. Self impedance response of the PDN at the driver chip shows a resonance in the mid-frequency range. The PD to signal coupling response at the driver chip follows the PDN self impedance response. The jitter at the receiver follows a similar signature at those frequencies when the transmission line effect is negligible. The PD to signal coupling at the package to PCB interface increases as the frequency goes higher. The channel response shows resonances at high frequencies, due to impedance discontinuities. The power to signal coupling noise can get amplified due to the channel effects and resonances. This, in turn, gets translated into jitter at the receiver at high frequencies. Referencing scheme, such as dual referencing, also causes the PD to signal coupling.

Intended audience for this book is Signal Integrity (SI) and Power Integrity (PI) Engineers (On-chip, package, and PCB designers). It can also be used by graduate students who want to pursue careers in these fields. Overall discussion level is beginner to intermediate; however, some advanced topics are also discussed. There may be different designers working on specific components, such as on-chip or package or PCB. However, this book presents power integrity design techniques along with power-to-signal coupling mechanisms at various stages in the system, such as chip level coupling and interconnect level coupling. This will give the component SI or PI engineers a perspective of system level impact of power integrity, and enable them to proactively design the system to avoid possible problem areas and also to identify the root-cause, in case of any system problems.

[Chapter 1](#), "Introduction," describes digital electronic systems and gives a high-level overview of the PDN and signal network. It describes signal and power integrity effects on system performance and highlights power noise to signal coupling mechanisms. Finally, it addresses the need for concurrent

SI/PI design methodology.

Chapter 2, “I/O Interfaces,” describes basic Input Output interfaces. The currents in power node generate noise that is basis of power integrity effects for I/O interfaces. This chapter addresses details of single-ended and differential drivers and receivers. Single-ended and differential interfaces produce different current profiles in the PDN, and their dependency on the bit pattern is also different. The PDN current flows are demonstrated with corresponding noise.

Chapter 3, “Electromagnetic Effects,” discusses the electromagnetic (EM) theory and how it is important in signal integrity, power integrity and ElectroMagnetic Interference (EMI) analysis. It begins with basic Maxwell’s equations, and addresses transmission line theory and interconnect network parameters (Z , Y , S). It also describes Linear Time Invariant (LTI) systems and their properties.

Chapter 4, “System Interconnects,” addresses the entire path for power and signal propagation, including the chip, package, and PCB. It gives an overview of the PCB technology and different package types. In the PDN section it describes PCB PDN components (DC/DC converter, PCB capacitors, PCB planes, vias, and so forth), package PDN, and on-chip PDN components (intentional/unintentional capacitors, and power-grid). In the signal network section, it describes PCB signal propagation with microstrip, stripline, and coupled line. It also addresses the package and on-chip signal networks. Then, it states the coupling mechanism from the PDN to signal network. Finally, it addresses modeling tools for the PDN and signal networks.

Chapter 5, “Frequency Domain Analysis,” begins with Fourier transform and its properties. It lists the key frequency domain design parameters for signal integrity and power integrity applications. It then addresses frequency domain PDN design with Z_{11} impedance target. It utilizes chip, package, and PCB co-design approach for the PDN design. Some important frequency domain concepts in the PDN design, such as voltage transfer function, SSO in frequency domain, and power to signal coupling, are illustrated. The next section describes the frequency domain signal network analysis and its correlation. A case study for “crosstalk amplification by resonance” is discussed in detail. The signal network analysis is performed with the PDN and on-chip parameters (on-die termination, pad capacitor, and so on) taken into account. Differential signaling parameters in frequency domain are also presented.

Chapter 6, “Time Domain Analysis,” begins with describing the necessary components for the time domain simulations. It addresses various kinds of buffer models used in signal integrity and power integrity analysis. Next, it describes the time domain PDN specifications, and simulation flow to achieve the specifications. Different examples of single ended drivers and

differential drivers are presented for AC noise analysis. Next, the concept of chip level driver noise coupling on the signal is discussed. It shows examples of the jitter analysis due to the PDN noise, for single ended and differential interfaces.

[Chapter 7](#), "Signal/Power Integrity Interactions," is devoted to unintended interactions between power/ground and signals, which has become an important consideration for optimizing high-bandwidth I/O signaling scheme. Power noise coupling can be amplified through channel resonance. It describes the power noise amplification mechanism that is due to a combination of three factors: SSO generation, power to signal coupling, and signal channel resonance. Then two case studies are demonstrated: DDR2-800 control bus resonance problem and DDR2-667 Vref bus noise issue. Next, it describes the referencing/stitching/and decoupling effects for single ended and differential interfaces.

[Chapter 8](#), "Signal/Power Integrity Co-Analysis," addresses the eye-margin analysis with SI-PI co-simulations. It describes the basic elements for the co-simulations: buffer models, 3D EM models for package and PCB, on-chip PDN models, and so on. The simulation deck is constructed and the worst case pattern is identified. Full-time domain simulations are performed with ISI, crosstalk, and SSO analysis; and response decomposition techniques are illustrated. The linear interaction indicator between power and signal is defined and evaluated for single ended and differential interfaces.

[Chapter 9](#), "Measurement Techniques," covers the frequency domain and time domain measurement techniques for validating signal/power integrity, in high-speed I/O signaling. The theory and some applications of the enhanced 2-port VNA technique for low impedance power delivery network characterization are discussed in the first part of this chapter. It also describes the on-chip interconnect and pad capacitance characterization techniques. In addition, it presents S-parameter measurement-based extraction methods to obtain the high-frequency SPICE model, with microwave network analysis and parametric optimization. Next, it describes the time domain characterization techniques. It includes Time Domain Reflectometry (TDR) measurement, PDN noise measurement, SSO coupling measurement, and jitter measurement.

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Vishram S. Pandit is a technical lead in the Signal/Power Integrity Engineering team at Intel Corporation. He works on developing power delivery designs for high-speed interfaces. His focus areas include high-speed system power delivery, on-chip power delivery, and Signal/Power Integrity co-design. Prior to Intel he worked at Hughes Network Systems on Electromagnetic Interference (EMI), Electromagnetic Compatibility (EMC), power integrity, and signal integrity technologies. He has received a B.E. (Instrumentation) from College of Engineering, Pune, India, an M.S. (Electrical Engineering) from University of Utah, USA, and an Advanced Certificate for Post-Master's Study (Computer Science) from Johns Hopkins University, USA. He is a senior member of IEEE and a member of the CPMT Technical Committee on Electrical Design, Modeling and Simulation; and he serves as a technical program committee member for DesignCon. He was a recipient of the International Engineering Consortium's paper awards for DesignCon 2008 and DesignCon 2009.



Woong Hwan Ryu is currently a Signal/Power Integrity Engineering Manager at Intel Corporation. He has been responsible for pre-silicon signal integrity and power integrity analysis for high speed interfaces. He received his Ph.D. degree in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST). Dr. Ryu holds an IEEE Senior Member status; he serves as a reviewer for several IEEE journals; and he serves as a technical program committee member and organizing committee member for DesignCon. He was a recipient of the International Engineering Consortium's paper awards for DesignCon 2006 and DesignCon 2008. Dr. Ryu has authored and co-authored more than 80 technical publications in premier journals and international conferences, and holds three issued patents and has one patent pending.



Myoung Joon Choi is a technical lead in the Signal/Power Integrity Engineering team at Intel Corporation. He works on developing methodologies for high-speed interface simulation and analysis. His focus areas include high-speed system SI-PI co-simulation, on-chip signal and power integrity, and computational analysis of entire high-speed systems. Dr. Choi has received a Ph.D. and an M.S. from University of Illinois at Urbana-Champaign, Urbana, IL, USA, and a BS from Korea University, Seoul, Korea. He has authored and co-authored many technical publications in journals and conferences.



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Chapter 1. Introduction

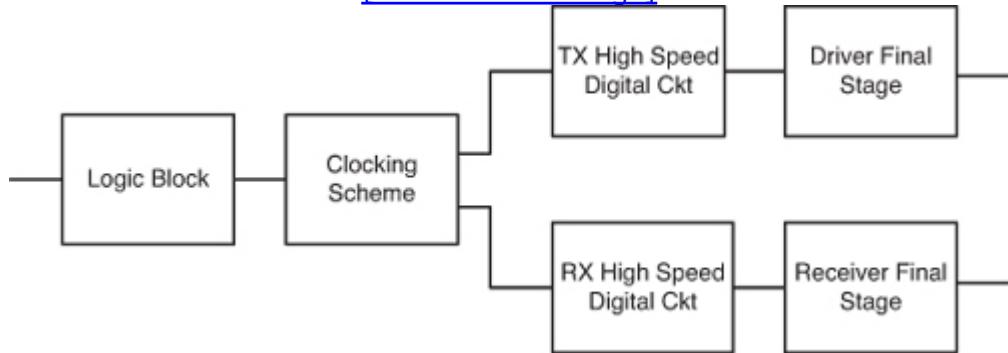
In a digital electronic system, when high-speed signals pass through the interconnect network, different unwanted effects such as Inter Symbol Interference (ISI) and crosstalk are produced that degrade the signal integrity. Power integrity is related to noise in the Power Distribution Network (PDN). Various techniques have been developed to model and design the PDN and analyze the noise impact [1, 2]. Simultaneously Switching Output (SSO) noise is produced when charging/discharging currents from the multiple buffers go through the PDN. This noise affects the circuit response and produces timing skews and delays. The power noise is coupled to signals at the chip level and at the interconnect level. It is becoming increasingly essential to determine not only the PDN noise, but also the margin degradation due to the noise coupling to signals. Due to ISI, crosstalk, SSO, and combinations thereof, the signal quality and timing margin becomes degraded at the receiver. System designers need to consider a concurrent design methodology to evaluate power integrity and its effects on signal integrity.

1.1. Digital Electronic System

The digital electronic system comprises a processing unit and an I/O controller unit. Different types of data flow from one part of the system to others in digital format, on different buses. Internal buses communicate within the different components of the system, and external buses communicate with the external devices. Various networking devices communicate with the digital electronic system with different protocols and standards. The I/O controller unit manages various types of input and output data on the buses and networking devices. The processing unit and the I/O controller unit are on different integrated circuits or chips in a conventional personal computer system, whereas they are on the same chip in a System-on-chip– (SoC) based platform. The I/O controller unit has several I/O interfaces that communicate with different I/Os. [Figure 1.1](#) shows the block diagram of a typical I/O interface in a digital system.

Figure 1.1. Input output interface

[\[View full size image\]](#)



A typical I/O interface has a logic block, clocking scheme, transmitter block, and receiver block. The logic block consists of digital circuits that communicate with the processing unit. The clocking is based on individual interface architecture and provides clocking for transmitter and receiver blocks. It can include Phase Locked Loops (PLLs) or Delay Lock Loops (DLLs). There are two types of I/O interfaces: a single-ended interface and a differential interface. The transmitter unit has high-speed digital circuits and a final stage driver unit. Transmitter high-speed digital circuits can include a predriver, equalizer, multiplexer, and parallel-to-serial converter, and so on, depending on the architecture and interface type. Similarly, the receiver block has high-speed digital circuits and a final stage receiver unit. Receiver high-speed digital circuits can include a sampling amplifier, serial-to-parallel converter, and so on, depending on the interface type and architecture. Single-ended and differential interfaces have different types of drivers, receivers, and high-speed digital circuits.

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1.2. I/O Signaling Standards

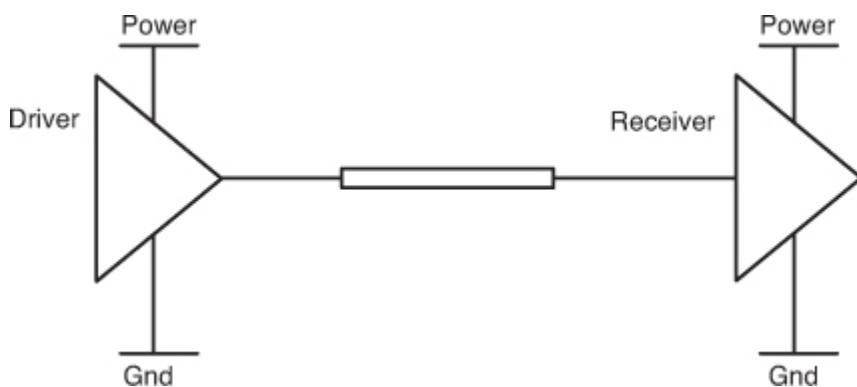
Examples of the logic families include Transistor Transistor Logic (TTL), Complementary Metal Oxide Semiconductor Logic (CMOS), Emitter Coupled Logic (ECL), and Bipolar Complementary Metal Oxide Semiconductor Logic (Bi-CMOS). Voltage requirements for the I/O signaling are dependent on the semiconductor process. The I/O standard defines a circuit topology with a logic family. It includes driving current, operating voltage, termination schemes, and switching behaviors [3].

I/O signaling can be in voltage mode or current mode. In voltage-mode circuits, the information processed by the electric network is represented by nodal voltages. In current-mode circuits, information processed is represented by branch currents. The sensing circuit at the destination determines the logic or signal state. The signal state is determined by the voltage value in voltage mode signaling, whereas it is determined by the current value in current mode signaling.

1.2.1. Single-Ended and Differential Signaling

Single-ended and differential signaling is categorized based on how voltages and currents are observed at the driver and the receiver. Figure 1.2 shows a single-ended signaling link. It comprises a driver, a receiver, and a transmission line from the driver to the receiver.

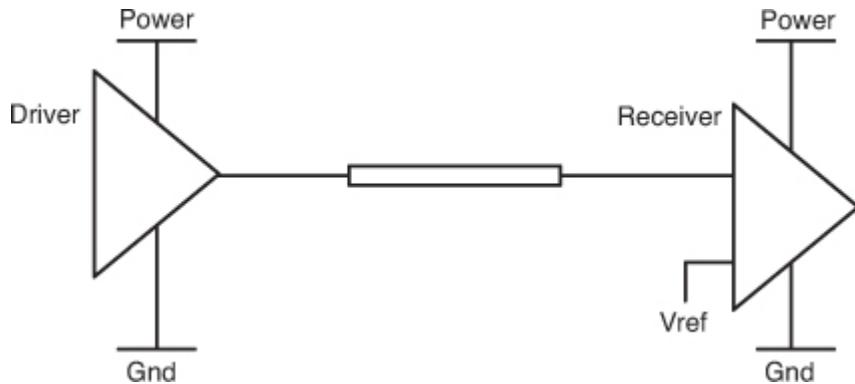
Figure 1.2. Single-ended link



A single-ended driver has one output port and assumes a common ground or power connection as a reference. For a single-ended receiver, there is one input port that assumes a common ground or power connection as a reference. In this chapter and in [Chapter 2, "I/O Interfaces,"](#) generic nomenclature is used for power (Power) and ground (Gnd) nodes, for the driver as well as the receiver. Power nodes are electrically different from the driver and the receiver due to PDN parasitics. Similarly, the ground nodes are electrically different for the driver and the receiver.

The single-ended signaling scheme with two input terminals at the receiver is shown in [Figure 1.3](#). Similar to the previous scheme, it also has a single output terminal at the driver. This terminal is referenced to common power or ground.

Figure 1.3. Single-ended link with Vref at RX



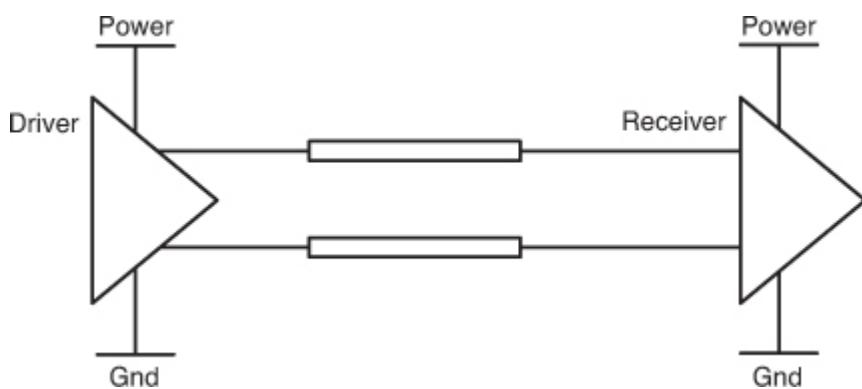
However, at the receiver end, there is one input terminal along with a locally generated reference voltage (V_{ref}). This receiver has a differential amplifier, so it is similar to a pseudo differential receiver. Overall link is still a single-ended link. This locally generated V_{ref} is on the Printed Circuit Board (PCB) and is primarily used to compensate the DC and low-frequency voltage drop. A single-ended push-pull driver can be designed in a current mode or a voltage mode configuration [4].

A single-ended signal has a power or ground reference or both. The referencing scheme can be identified by the proximity of the signal line to the power or ground domains. The proximity of the signal to the power or ground domain tends to make a return path to the domain in high frequencies, because capacitive coupling makes a low impedance path between the signal and that domain. Frequently, unintentional referencing change occurs in complex multilayer PCBs. When the signal is routed on the board from one layer to the other layer, there may be some regions with signal over void. The signal's reference change due to the vertical structure inside of a rather flat power/ground domain structure works as one of the major sources of unintended radial wave propagation. It contributes to signal noise and power delivery noise when it is captured by other structures inside of the PCB. In addition to referencing change, rather loose

coupling of single-ended signaling makes it more susceptible to noise than differential signaling. In general single-ended signaling is preferred in many interfaces including Double Data Rate (DDR) memory signaling because of its rather simpler structure, less pincount, and simpler buffer circuit.

[Figure 1.4](#) shows a differential link. A differential driver can be designed in a current mode or a voltage mode configuration [5]. A differential driver has two ports, which are separate from the power or ground connections. At the driver output, the differential signal is referenced from one of its ports to the other ports. At the driver output, two transmission lines are connected to the output ports. These lines are coupled lines: tightly coupled or loosely coupled. Tightly coupled differential links typically perform better at higher data rate and are physically smaller than loosely coupled ones. If the reference power or ground plane is far away, then one line has the other line as a reference. However, for most of the practical systems, due to the vicinity of the reference planes, most of the return current goes through the reference planes. At the input of the receiver, there are two ports, which are different than power or ground connections. At the receiver input, the signal is referenced from one port to the other port. Differential signaling can achieve higher data rates and has low susceptibility to noise. The impact of power/ground noise coupling to signal line on differential signaling is less than that on single-ended signaling. However, differential signaling requires twice the number of wires compared to those for single-ended signaling. More number of wires results in a higher cost of the system. The mismatch of the coupled lines causes common mode fluctuations at the receiver; therefore either a well-designed receiver, well-matched coupled lines, or both are needed to fully utilize the advantages of differential signaling.

Figure 1.4. Differential Link



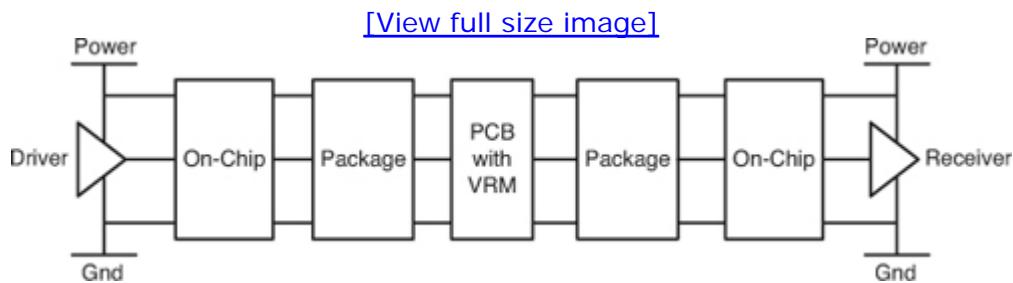
[Chapter 2](#) describes in details single-ended and differential drivers/receivers with the associated currents in different nodes. When the interface is switching, the current is generated on the power and ground nodes of the circuits. This current produces noise at the chip, which gets coupled to the signal lines.

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1.3. Power and Signal Distribution Network

Chapter 4, "System Interconnects," describes the power and signal distribution networks, and their interactions. For a semiconductor I/O interface, the driver and receiver circuits are implemented in the chip. The chip is packaged and then placed on a PCB. The block diagram of the PDN and signal network is shown in Figure 1.5.

Figure 1.5. Power and signal distribution network



PCB PDN comprises Voltage Regulator Module (VRM), power/ground plane structure, and decoupling capacitors. The VRM converts the input voltage from the power supply to the desired DC output. PCB typically has a multilayer stackup, and power and ground planes form a cavity structure. Package PDN can have a power/ground plane structure and package capacitors. The package connects to the chip at the pad or the bump. The power routes from the bump to the I/O circuit through the on-chip interconnects.

The signal network is routed on the chip, on the package, and then on the PCB. The impedance mismatch at the interface can cause the signal reflections. The two basic types of transmission lines in a package and PCB are microstrip and stripline. Differential signaling utilizes coupled lines. Chapter 4 also describes the details of the on-chip power and signal networks, and Chapter 9, "Measurement Techniques," illustrates the characterization of on-chip components.

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1.4. Signal and Power Integrity

The I/O signal integrity addresses two major concerns in the electrical design aspects—the timing and the quality of the signal. Timing is critical in a high-speed digital system. Signal timing pertaining to interconnects depends on the delay caused by the electrical length of the interconnect structure where the electromagnetic energy flows from one end to another. It also depends on the modes of the signal propagation—even and odd modes especially in an inhomogeneous medium, that is, microstrip line. The even mode is the behavior of system when driven with identical signals of the same magnitude and same phase. The signal propagation delay can be increased, for the microstrip line, due to the even mode excitation. By contrast, the odd mode is the behavior of a system when it's driven by identical signals of the same magnitude but with different phase. An odd mode type of excitation would make signals faster for the microstrip line. In summary, signal propagation delay in odd mode is shorter than that in the even mode due to signal coupling in a microstrip or embedded microstrip. Lowering even/odd mode coupling results in lower timing jitter. We can achieve less mode coupling by using low k and thinner dielectric PCB in the microstrip systems. However, for a homogeneous medium, such as a stripline, the phase velocity of even and odd mode propagation is the same. Furthermore, we need to carefully examine all other coupling mechanisms due to 3-dimensional structures, for example vias, connectors, and so on. Electromagnetic simulation can help determine acceptable levels of coupling. [Chapter 3](#), "Electromagnetic Effects," describes the fundamentals of electromagnetic theory and its applications for the signal and power integrity analysis.

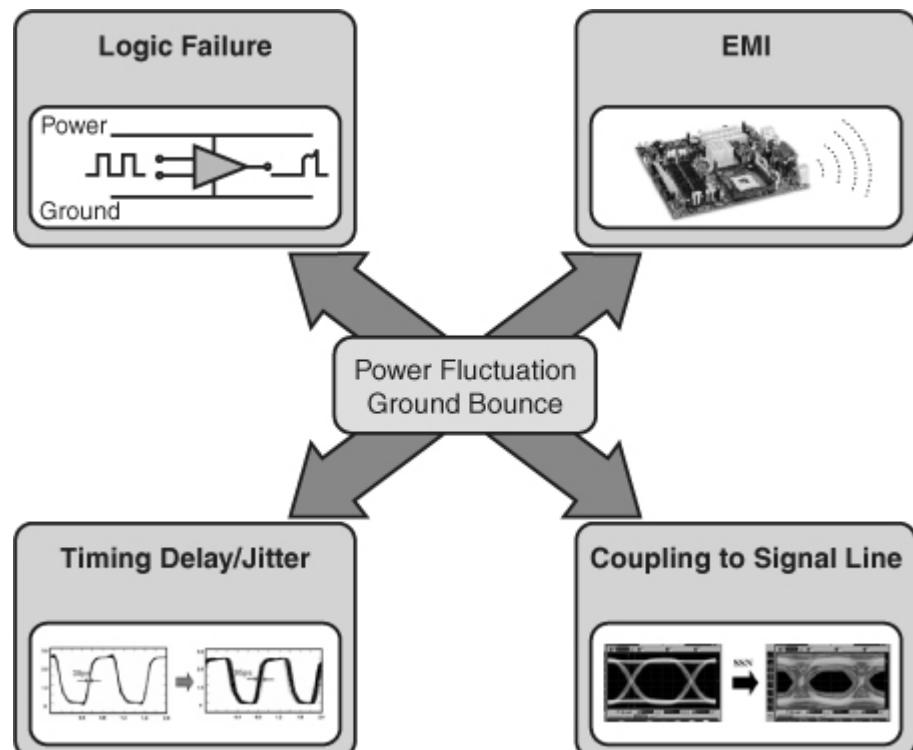
Signal waveform distortions can be caused by many different mechanisms, but three major noise sources exist. The first noise element is the ISI. For multidrop single-ended interfaces, it is primarily caused by reflection noise due to impedance mismatch, stubs, vias, and other interconnect discontinuities causing energy disruption along the signal path. For high-speed differential interfaces, it is primarily due to the PCB losses, having different transfer function at different frequencies. The effect of ISI causes a reduction in the system voltage margin by reducing the peak and causes an ambiguity in the timing information. The second noise element is the crosstalk noise due to electromagnetic coupling between adjacent signal

traces and vias. The third noise element is the power/ground noise due to parasitics of the power/ground distribution system during the drivers' SSO. It is sometimes also called ground bounce, Delta-I Noise, or Simultaneous Switching Noise (SSN). In addition to these three kinds of electrical integrity problems, other Electromagnetic Compatibility (EMC) and Electromagnetic Interference (EMI) problems can contribute to the signal waveform distortions. Signal integrity, power integrity, and EMI are all based on the same electromagnetic fundamentals and cannot be separated.

Power integrity for I/O interfaces is related to the voltage variations in the power/ground network due to the noise. The power/ground noise causes various problems in high-speed systems, such as logic failure, EMI, timing delay, and jitter, as shown in [Figure 1.6](#). The power integrity problems can be identified and root-caused based on the electromagnetic Maxwell's equations. The system noise margin requirements may not be satisfied when power integrity problems happen. The power integrity has several impacts to the I/O signaling as follows:

- 1. Signal Quality:** Power noise exists on the signals due to the coupling power/ground noise in signal interfaces through signal reference transition.
- 2. Timing Delay/Jitter (Lateral SSO push-out or pull-in, slew rate impact):** The I/O interface has three stages: logic stage, high-speed I/O stage (clocking and other circuitry such as predrivers), and final stage (driver/receiver circuitry).

Figure 1.6. Power noise impact on IO signaling



There is a delay associated with the multiple stages of devices the signal needs to pass through from core logic to the I/O output stage. As the rail voltage fluctuates, the delay through each stage increases or decreases. So the time from an edge leaving the core to the time it arrives at the output of the I/O interface can change with power/ground noise. Also, the signal edge will be faster or slower depending on the power/ground noise. All these internal stages may or may not be tied to the same power/ground networks as the final I/O stage (driver, receiver). Noise coupling from other stages need to be considered when determining the supply noise induced timing variations.

3. **Functionality:** Power/ground voltage fluctuations disturb the data in the latch; then logic error, data drop, false switching, or even system failure can occur. This can happen when the noise causes the signal voltage to fall below VIH (input high level) minimum or above VIL (input low level) maximum.

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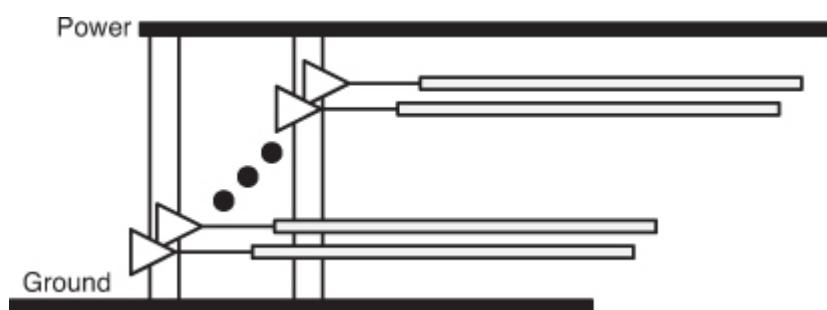
1.5. Power Noise to Signal Coupling

When an I/O interfaces is switching, SSO noise is produced when rapid charging/discharging currents flow through the PDN. The power to the signal coupling can be attributed to two major mechanisms. First is the chip level SSO coupling and the second is the interconnect level SSO coupling.

1.5.1. SSO

SSO or SSN occurs in a system with multiple buffers nearby switching at the same time, as shown in [Figure 1.7](#). Rapid current draws from the buffers leave instantaneous void of electrons in power and ground planes. The instantaneous formation of an electron void may be too fast in a high-speed channel for the electrons from the nearby capacitor to fill in, which shows up as noise in the PDN that should be kept as stable as possible. As a result of the PDN fluctuation, signals of the buffers in the vicinity are affected, so the simultaneous switching impacts not only the PDN but also signal outputs. In this process, inductance in the PDN contributes to the voltage variation of the PDN through Delta-I noise. The term Delta-I refers to the $\frac{di}{dt}$ voltage drop due to the inductance. SSO noise can occur for both single ended and differential drivers [\[6, 7\]](#).

Figure 1.7. Block diagram of multiple buffers switching simultaneously



1.5.2. Chip-Level SSO Coupling

The impact of supply on signaling is dependent on the driver type and the

signaling schemes. The power noise at the driver is coupled to the signals at the chip level. SSO noise at the buffer power/ground nodes propagates in the package and the PCB. This noise depends on the impedance of the PDN at the chip level, which is influenced by various stages on the PDN, including on-chip capacitance and package inductance. The chip level power noise to the signal coupling is significant. This coupling is important for single-ended signaling and differential signaling. [Chapter 5](#), “Frequency Domain Analysis,” describes the PDN resonance behavior and the power to signal coupling in frequency domain. [Chapter 6](#), “Time Domain Analysis,” describes the on-chip power noise coupling and its impact on signal performance in the time domain both for single-ended and differential channels. The power noise coupling at the chip results in signaling impact such as jitter.

1.5.3. Interconnect Level SSO Coupling

There are various mechanisms of interconnect level SSO coupling. A PCB power and signal distribution network includes not only planar conductors but also vertical structures, such as vias. A via is a pad with plated hole for electrical connections between conductor traces on different layers. The flat power-ground plane pair becomes a parallel plate wave guide or parallel plate cavity with short dimension along z-axis, as shown in [Figure 1.8](#). The figure shows the ground net vias that are orthogonal to the power and ground plane structure. When the multiple buffers are switching, the excitation applied to the power-ground plane generates dominant radial waves that propagate in between the two planar conductors, as shown in [Figure 1.9](#). Here, higher order waves are usually small in magnitude. The radial waves picked up by structures that are orthogonal to the planar power-ground conductors become unwanted noise. The noise in the power/ground planar cavity is coupled to the power/ground vias as well as signal vias. If there is a signal trace in between the power and ground cavity, the power/ground noise is coupled to the trace.

Figure 1.8. Pulse excitation of a power-ground plane pair with 1mm dielectric thickness

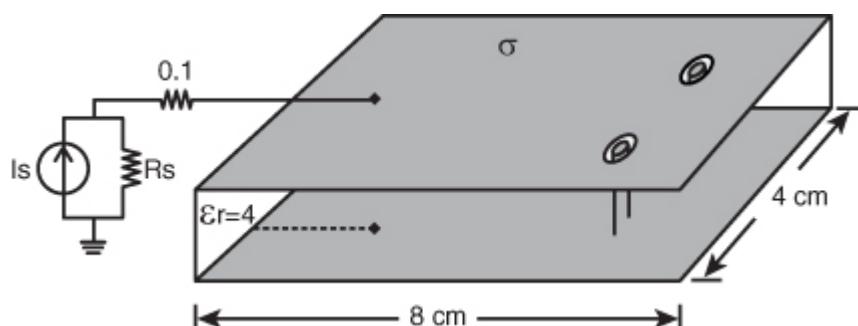
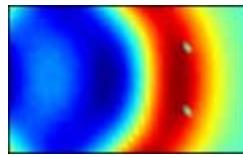


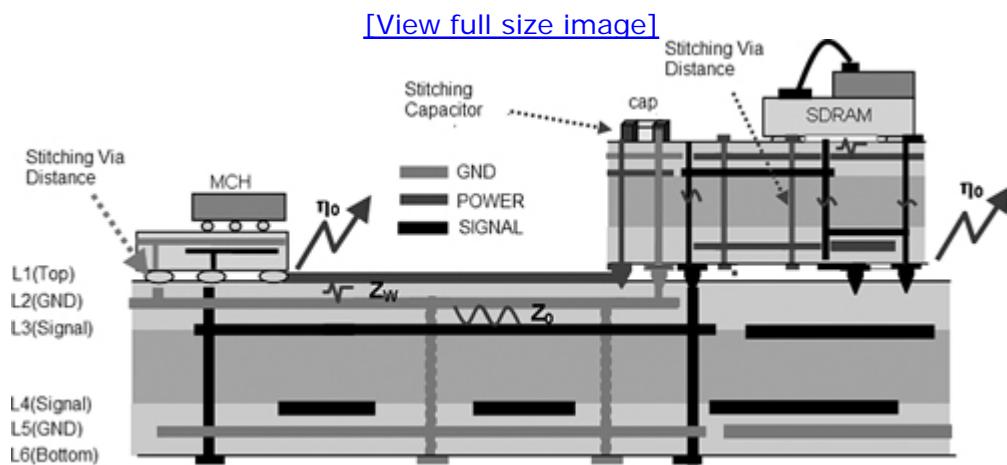
Figure 1.9. Radial wave propagation in power-ground plane pair



Sockets, connectors, and adjacent signal/power vias, introduce electromagnetic coupling between PDN and signal nets. In high-speed channel, these vertical structures with adjacent power/ground nets, and signal nets become vulnerable to the unwanted parallel coupling. Crosstalk in sockets' vertical structures often becomes the source of coupling between the signal and power.

Figure 1.10 shows a digital I/O channel with two IC chips: one (MCH) mounted on a PCB and the other (DRAM) mounted on a daughter-card. For the multi-layered high-speed systems, as shown in the figure, Delta-I noise, or SSO generated by I/O buffer switching propagates in the power and ground planes and significantly couples to the interconnects through signal reference transition. The coupled noise can be amplified due to transmission line effect and can cause severe signal integrity problems. In [Chapter 7](#), "Signal/Power Integrity Interactions," various case studies are presented that illustrate the interaction between power and signal integrity including the interconnect level coupling. [Chapter 8](#), "Signal/Power Integrity Co-Analysis," addresses the combined power and signal integrity analysis. It is essential for combined modeling and simulation of signal and power integrity to understand how SSO noise is translated into receiver jitter. Radiated emissions may occur at edge of the printed circuit board (PCB) due to the power/ground noise. Stitching capacitors or vias help mitigate these risks, but the effectiveness of the stitching capacitors appear to deteriorate at speeds higher than a few hundreds MHz.

Figure 1.10. Power/ground noise coupling to signal line in a multilayers link



These types of noise issues and faults are extremely difficult to diagnose

and solve after the system is built or prototyped. Understanding and solving these problems before they occur can eliminate having to deal with them further into the project cycle and in turn cut down the development cycle and reduce the cost.

A signaling scheme impacts power integrity and signal integrity because of their coupling differences in various stages of channels. Designing a system with a tight margin necessitates exploring the impact of these signaling options. Generally, differential signaling offers better quality signal at all speeds than single-ended signaling if all the physical conditions are reasonable. Single-ended signaling is usually easier to implement; however, it is usually more susceptible to reference disturbance, SSO noise, or ground bounce. For single-ended signaling, the impact of power noise coupling at the interconnect level is higher than that for differential signaling. For differential signaling, with lines tightly coupled, common-mode noises affect both lines. Thus at the receiver, the difference between the two lines remains almost constant. Stray transient noise on the two lines will get canceled at the receiver, alleviating the impact due to interconnect level power noise coupling. [Chapters 7 and 8](#) address the power noise coupling to the signal at the interconnect level for single-ended and differential channels. [Chapter 9](#) describes the signal and power integrity measurement techniques, including power to signal coupling characterization.

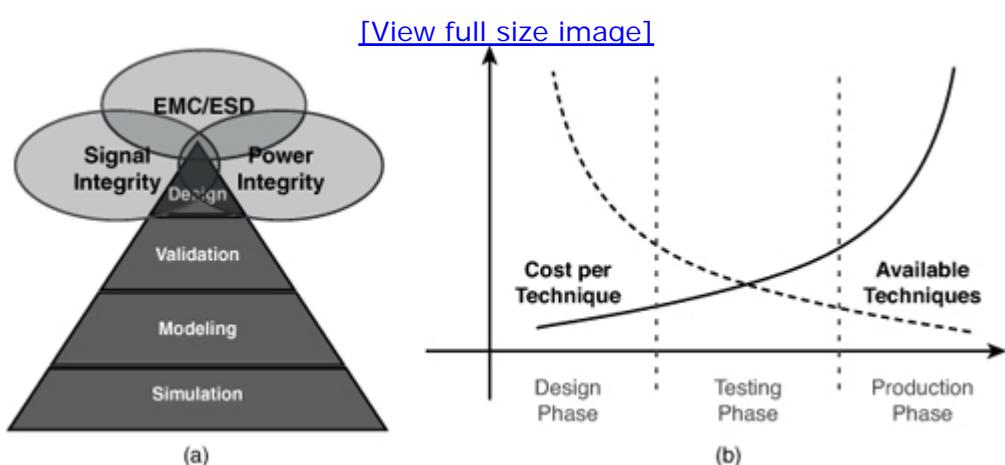
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1.6. Concurrent Design Methodology

Power integrity, signal integrity, and EMC design techniques are inter-related, and their interactions need to be considered. A concurrent design methodology is needed to analyze these interactions [8, 9, 10, 11].

Common mode noise always exists due to power fluctuation and ground bounce. The common mode noise is the main contributor to EMI. The co-design approach considering signal/power integrity and EMC throughout the design, as illustrated in Figure 1.11 (a), is a fundamentally more cost-effective approach compared to a crisis-management approach. If the designer anticipates interactions between signal/power integrity and EMC at the beginning of the design process, and if noise suppression is considered for one stage or subsystem at a time, the noise mitigation techniques are simpler and more straightforward. If the designer proceeds with a disregard of various interactions until the design is close to being finished, mitigation techniques become considerably more costly, less effective, and less available, as shown in Figure 1.11 (b).

Figure 1.11. Concurrent SI/PI/EMI design



The design methodology proposed in this book is a further unified solution to the co-design of signaling systems by proposing a new metric to unify power integrity and signal integrity designs. In the co-design of signal/power integrity, several sources of coupled noise need to be considered in the signaling system that can degrade the quality of a

transmitted signal. As the speed and width of interfaces increase, understanding these signal impediments and designing low-cost solutions become challenging. Signals can contaminate one another through ISI, crosstalk among adjacent signals, and PDN noise. All three items and their interaction need to be closely examined within the signaling system [13]. In summary, this book presents the power integrity design techniques taking into account the effects on signal integrity.

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Chapter 2. I/O Interfaces

An Input/Output (I/O) interface, when in operation, produces current in power and ground nodes. This current produces the noise, which is the source for the power integrity effects. The rate of change of current and the effective loop inductance of the Power Distribution Network (PDN) determine the noise. This chapter examines the current flow paths when different types of drivers are in operation. The currents at the power node are dependent upon the termination schemes. An example is provided on how the current changes when the termination scheme is altered from the center tap to the power termination for a push-pull driver. When multiple drivers are switching, the overall current in the PDN at the driver chip increases and produces higher noise. The noise is dependent on the bus operating conditions, and is different for single-ended and differential signaling. This chapter presents the I/O interface currents and their noise impact.

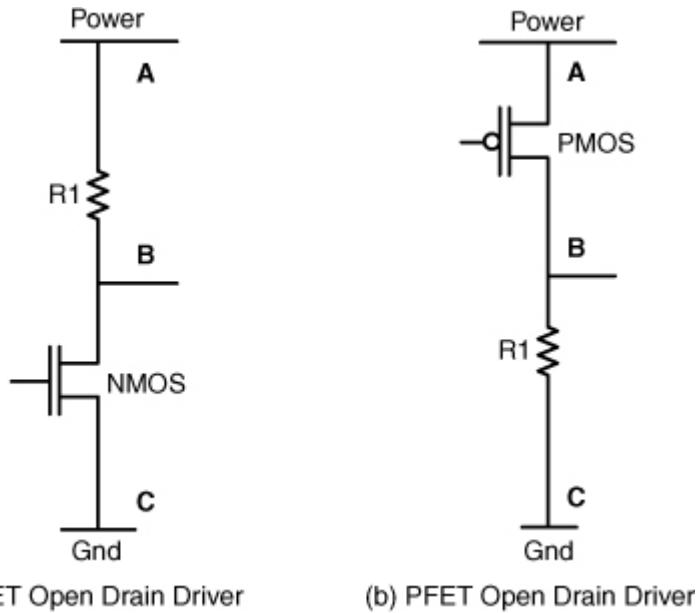
2.1. Single-Ended Drivers and Receivers

This section presents different types of single-ended drivers. It includes open drain, open source, and push-pull drivers. A push-pull receiver is also shown. For the single-ended driver, output is pulled high or low depending on the configuration. A path of the current is established between the output and power or ground terminals. Correspondingly, the voltage appears on the output terminal with reference to the power or ground terminals. The single-ended drivers can be designed in multiple ways. The next section shows a conceptual representation.

2.1.1. Open Drain Drivers

N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS or NFET) and P-channel MOSFET (PMOS or PFET) open drain drivers are shown in [Figure 2.1 \[1\]](#). An NMOS open drain driver has no pull-up device. Node A is the power node, node B is the output node, and node C is the ground node, as shown in [Figure 2.1\(a\)](#).

Figure 2.1. Open drain drivers



The output at B is typically referenced to common ground C. For the NMOS open drain driver, there is a resistor R_1 connected to the power at A. When the NMOS is disabled, the output is pulled up to supply voltage through the resistor. R_{eff} is an effective resistance at the driver output node. When pulling up, R_{eff} is R_1 , because R_1 is parallel with the high output resistance of the disabled NMOS. The logic low state is when NMOS turns on that the output is pulled low. When pulling down the NMOS resistance can be on the same order of R_1 , which would make R_1 in parallel with R_1 , giving R_{eff} a half of R_1 . The lower R_{eff} during the high-to-low transition causes the falling edge to be faster than rising edge. If there are different operating voltage levels, open drain circuits can interface that device. In this case, pull-up resistors connect to the different logic levels. The location of the termination resistor R_1 is dependent on the topology and can be at the receiver.

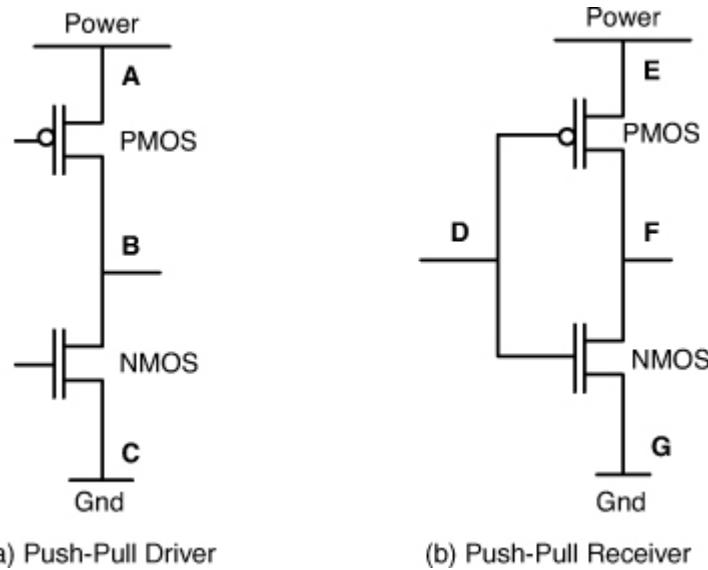
The PMOS open drain driver has a pull-down resistor, as shown in Figure 2.1(b). When the PMOS is turned on, the output at B is high. When PMOS is turned off, the output is pulled low. PMOS has higher on-state resistance, and it requires a much larger area than NMOS for similar performance. As a result, NMOS open drain drivers are more common than PMOS open drain drivers.

The signal integrity benefit of an open drain driver compared to a push-pull driver is its typically low parasitic capacitance that provides better impedance matching to a transmission line at higher frequencies. However, its usefulness should be carefully weighed in when it comes to power-limited devices because of the driver's static power consumption through the resistor, which is significantly larger than the push-pull driver without on-die terminations.

2.1.2. Push-Pull Driver and Receiver

Figure 2.2 shows a push-pull driver and a receiver [2]. A push-pull device has two MOSFETs, one sourcing current from the power supply into the load and the other dissipating current from the load to the ground. The circuit representation shows two transistors vertically, which is also known as “totem pole” configuration.

Figure 2.2. Push-pull driver and receiver



The driver has one pull-up and one pull-down device. PMOS pulls the output at B up to logic high (power at A), and NMOS pulls it down to logic low (ground at C). The driver circuitry is designed in such a way that one transistor is on and the other is off. Similarly, a receiver has input D that is connected to NMOS, and an inverted version of the input is sent to PMOS. Essentially, it acts as an inverter.

For the push-pull driver, the rise time and fall time mismatch occurs when R_{on} impedance for pull-up and pull-down becomes different because of tolerance and design specification. The mismatch can be easily minimized by transistor compensation circuits. The driver also could suffer the direct noise coupling from power delivery network through simultaneous switching because of its rather low impedance connection to the power delivery network.

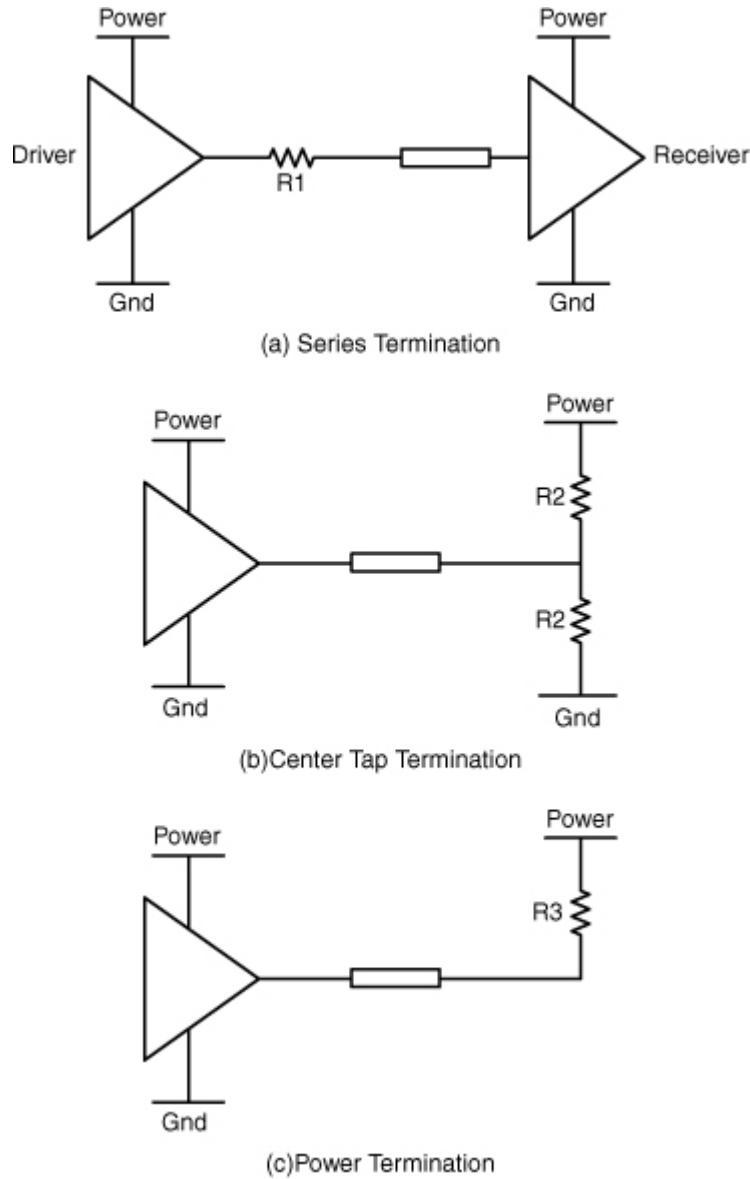
The push-pull driver from one chip and the receiver from another chip are connected by the transmission line. For a single-ended system, impedance matching of the connected transmission lines and driver/receiver should be carefully calculated. The push-pull driver can be used for voltage mode and current mode configurations.

2.1.3. Termination Schemes for a Single-Ended System

Termination of single-ended signaling is particularly important as it affects the quality of a transmitted signal at the receiver. Mismatched impedance causes reflection of the transmitted signal and consequently degrades the signal quality.

At the receiver end, parasitic capacitance of devices and pad interconnects provides pF range capacitance, C_{pad} . The impact of the receiver end capacitance is a frequency dependent signal reflection, which makes wide-bandwidth signal distortion inevitable. In general, the I/O receiver end capacitance should be minimized to improve signal integrity at the receiver. [Figure 2.3\(a\)](#) shows a series termination scheme that simply provides basic matching impedance for the transmission line. The series resistor value is dependent on the difference between the transmission line characteristic impedance and the output impedance of the driver. To improve the signal quality, the parallel resistive termination can be added to the receiver, as shown in [Figure 2.3\(b\)](#). The parallel resistive termination is used for impedance matching between the receiver and the transmission line. This type of termination, as shown in [Figure 2.3\(b\)](#), is also called Center Tap Termination (CTT). It increases the overall cost and also increases the current consumption. In Double Data Rate (DDR) memory interface, fixed on-board termination, in DDR2 On-Die Termination (ODT), and in DDR3, dynamic On-Die Termination (ODT) is provided. Dynamically controlled ODT provides better matching for the active receiver. Consequently, the eye diagram at the receiver is improved significantly. An alternative way of parallel termination is termination to power only, as shown in [Figure 2.3\(c\)](#). This termination scheme has lower current consumption compared to that for the CTT but sacrifices some signal integrity in terms of overshoot. The single-ended termination scheme should be chosen carefully to consider the power consumption and I/O interconnection specification.

Figure 2.3. Termination schemes for single-ended system



2.1.4. Current Profiles in a Push-Pull Driver

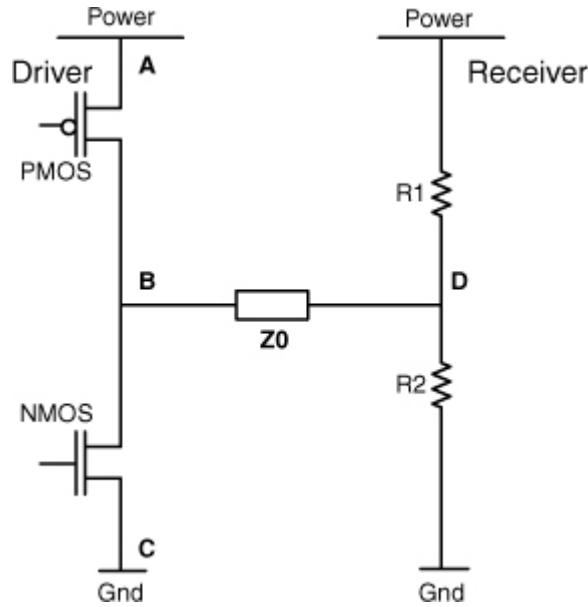
The rate of change of current (di/dt) in the power/ground nodes will produce noise. This section demonstrates the currents in power, ground, and output nodes of a push-pull driver. The current flow is based on the termination scheme at the receiver. Two types of termination schemes are examined: center tap termination and power termination. Ground termination can enable compatibility between different voltage domains but usually requires PMOS receivers, which are not as good as NMOS receivers.

2.1.4.1. Push-Pull Driver with CTT

[Figure 2.4](#) shows a push-pull driver with a CTT. Node B is output at the driver, and node D is input to the receiver. There is a transmission line in between node B and node D with characteristic impedance Z_0 . Current profiles at various nodes at the driver side are captured with the transistor

level simulations [3], including some amount of DC current from associated circuitry.

Figure 2.4. Push-pull driver with CTT



PMOS pulls voltage of the line high; NMOS pulls it low. The inputs at the gates are inverted inputs, with respect to each other. At time $t=0\text{ns}$, the NMOS is on and PMOS is off. The current flows from the receiver power node, to the resistor R_1 , to the transmission line node D , to the node B , and to the ground node C . [Figure 2.5](#) shows the current at node A (power); [Figure 2.7](#) shows the current from the node D to the node B ; and [Figure 2.6](#) shows the current at node C (ground). At time $t = 10\text{ns}$, there is a low-to-high transition. The PMOS is switched on and NMOS is off. At time $t=20\text{ns}$, the transistors change their states: PMOS is now off, and NMOS is on. Again, at time $t=30\text{ns}$, PMOS switches on, and NMOS is off. The currents shown in [Figure 2.5](#) and [Figure 2.6](#) have some DC value and do not go all the way to zero, because simulations include some associated circuits aside from the final stage, that have some DC currents.

Figure 2.5. CTT: Current in node A

Source: V. Pandit, M.J. Choi, and W.H. Ryu, “Power Integrity for I/O Interfaces,” Tutorial, EPEP-2008, © [2008] IEEE.

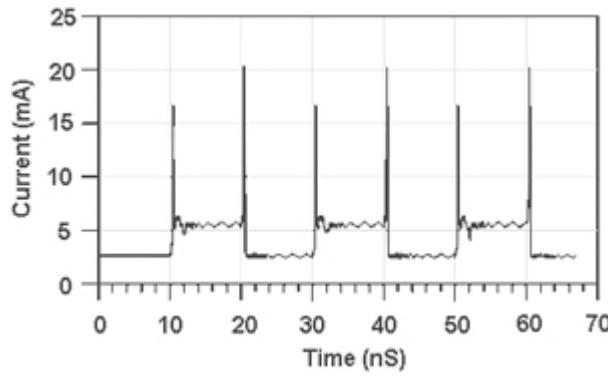


Figure 2.6. CTT: Current in node C

Source: V. Pandit, M.J. Choi, W.H. Ryu, “Power Integrity for I/O Interfaces,” Tutorial, EPEP-2008,
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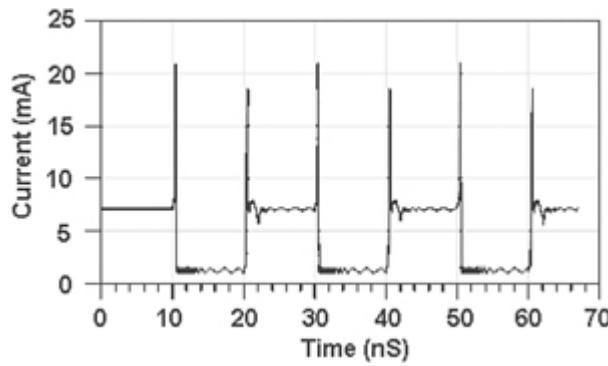
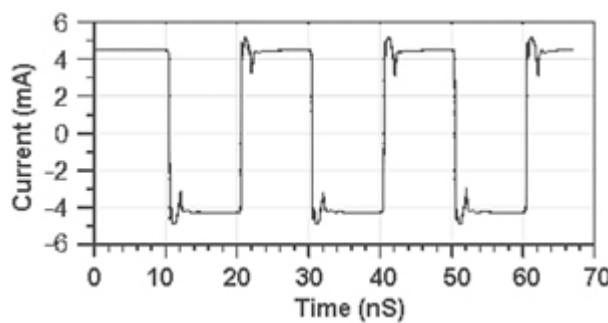


Figure 2.7. CTT: Current from Node D to node B

Source: V. Pandit, M.J. Choi, W.H. Ryu, “Power Integrity for I/O Interfaces,” Tutorial, EPEP-2008,
© [2008] IEEE



When PMOS and NMOS transistors change their state, they both are momentarily on. A sharp spike of current, which is known as a crowbar current, flows from the power to the ground. Figure 2.5 shows current from the power node A to the node B. At $t=10\text{ns}$, there is a crowbar current from the node A to the node C, as both transistors change their states. After that, it is a logic high state. The power current then goes from low to high. The current path is now from PMOS, to the transmission line, then to the bottom R2 resistor, and finally to the ground at the far end. When there is a

high-to-low transition at $t=20\text{ns}$, both transistors change their states again. There is a crowbar current from the node A (power) to the node C. The current path is from the receiver power, to the top R1 resistor, then to the transmission line node D, then to the node B, and then to the ground node C.

The current at node C is shown in [Figure 2.6](#). As in power current, there is a crowbar current every time the logic state is changed. The ground current goes from high to low, when the logic state changes to high at 10ns . The ground current goes back to high, when the logic state changes to low at 20ns .

[Figure 2.7](#) shows the current in the buffer output from the node D to the node B. When the logic state is low, the transmission line current flows from the node D to the node B. When the logic state is high, the transmission line current flows from the node B to the node D.

[Table 2.1](#) summarizes the current flows in logic low and logic high states for the push-pull driver.

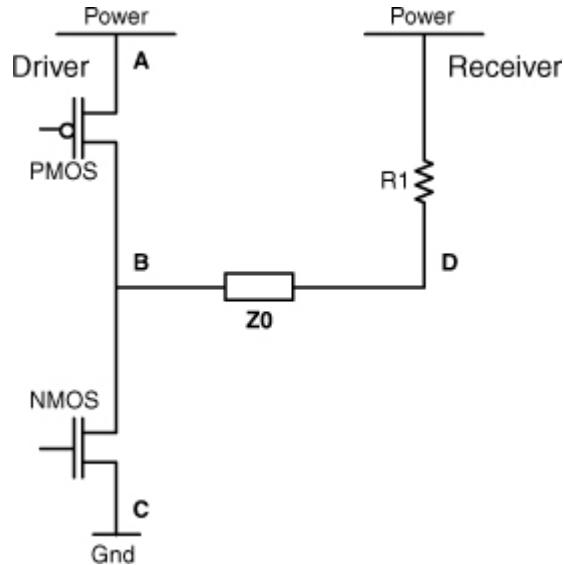
Table 2.1. Currents for a Push-Pull Driver with CTT

Currents For	Power Node	Ground Node	Output Node
Logic low	Low	High	Enters node B from power node of receiver
Logic high	High	Low	Exits node B to ground node of receiver

2.1.4.2. Push-Pull Driver with Power Termination

In CTT, for both logic levels there is a DC current flow. To reduce the overall power, a power termination scheme can be constructed. [Figure 2.8](#) shows the power termination scheme for a push-pull driver.

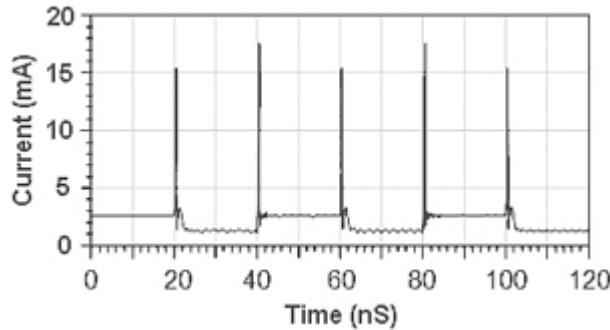
Figure 2.8. Push-pull driver with power termination



[Figure 2.9](#) shows currents in power node A. Whenever there is a logic state change, there is a crowbar current from the power node to the ground node of the driver. However, the steady state current remains the same, because there is no termination to ground at the receiver [1].

Figure 2.9. Power termination: Current from the node A to the node B

Source: V. Pandit and M.J. Choi, “Power Integrity for Single Ended Systems,” IBIS Summit, June 2008.



[Figure 2.10](#) shows the current in ground node C for the push-pull driver with power termination. Whenever there is a state transition, there is a crowbar current. Also, the steady state current changes at the ground node. When there is a logic high, steady state ground current is low and vice versa. The currents shown in [Figure 2.9](#) and [Figure 2.10](#) have some DC value, and they do not go all the way to zero, because simulations include some associated circuits aside from the final stage that have some DC currents.

Figure 2.10. Power termination: Current in node C

Source: V. Pandit and M.J. Choi, “Power Integrity for Single Ended Systems,” IBIS Summit, June 2008.

2008.

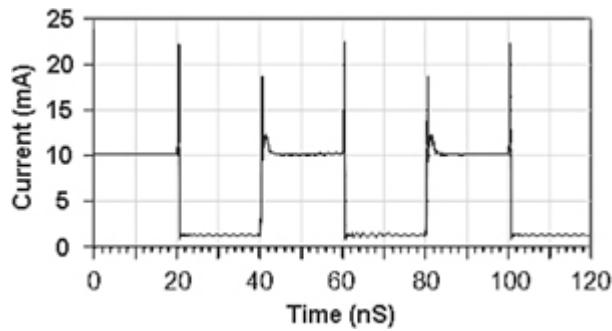


Figure 2.11 shows the current from node D to node B for a push-pull driver with power termination. At logic state low, the current enters the node B from the node D. At logic state high there is no current flow from the node D to the node B. At each state transition, there is a crowbar current.

Figure 2.11. Power termination: Current from node D to node B

Source: V. Pandit and M.J. Choi, “Power Integrity for Single Ended Systems,” IBIS Summit, June 2008.

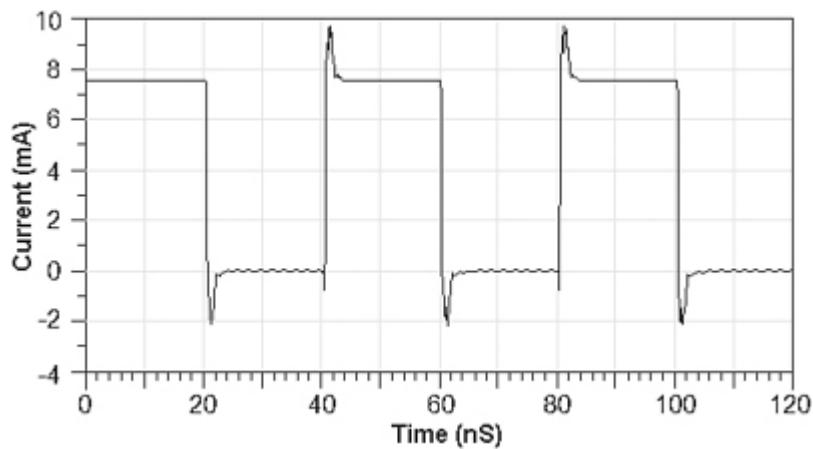


Table 2.2 summarizes the current flows in logic low and logic high states for the push-pull driver with power termination. In general, a push-pull driver with power termination at the receiver shows more overshoot in a signal level than a push-pull driver with CTT at the receiver. However, power termination has less power consumption compared with CTT. The current profiles at the power/ground nodes are significantly different for the two termination schemes.

Table 2.2. Currents for a Push-Pull Driver with Power Termination

Currents For	Power Node	Ground Node	Output Node
Logic low	Low	High	Enters node B

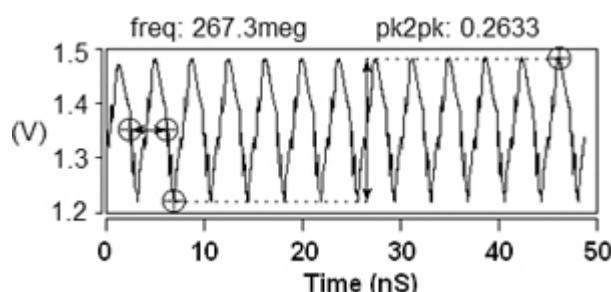
			from the power node of receiver
Logic high	Low	Low	No current flow from node D to node B

2.1.5. Noise for Push-Pull Driver

Figure 2.12 shows an example of the simulated voltage noise for the single-ended interface at the driver power node [3]. It has a push-pull driver with CTT. The logic state high is the data pattern 1 and low is the data pattern 0. This noise is produced when the multiple buffers for a single-ended interface are switching at the pattern 1100 for 1066Mbps data rate. When the logic state is switched from 1 to 0 and vice versa, there is a current spike in the power and ground. It produces noise at the driver power/ground nodes. The noise frequency is 267MHz and its amplitude is 260mV.

Figure 2.12. Noise profile for a single-ended driver

Source: V. Pandit, M.J. Choi, and W.H. Ryu, “Power Integrity for I/O Interfaces,” Tutorial, EPEP, 2008 © [2008] IEEE



The performance of the single-ended buffer is susceptible to this power/ground noise. At the driver, the noise on the PDN couples with the signal (PD to signal coupling). It produces timing delay or jitter. When the signal travels through a package and a PCB, it is referenced to the power or ground. If the referencing is not so solid, and there are return path discontinuities, the signal quality is affected. The interconnect structure from driver to receiver determines the PD to signal coupling.

Compared with differential signaling, single-ended signaling has advantage in its simplicity of manufacturing process and geometrical constraints. Simultaneous switching noise combined with crosstalk makes single-ended signaling less attractive than differential signaling at higher speeds. Nevertheless, because of cheaper manufacturing costs and a well-established ecosystem, data rates of some single-ended systems are

pushed beyond a couple of Gbits/second. One good example of pushing its capability far beyond what had been predicted a decade ago is the DDR memory channel. To assess genuine signaling impact at higher data rates, signal and power integrity co-analysis is needed with cosimulations. It gives information not only on signal integrity and power integrity, but also on the interaction between the two.

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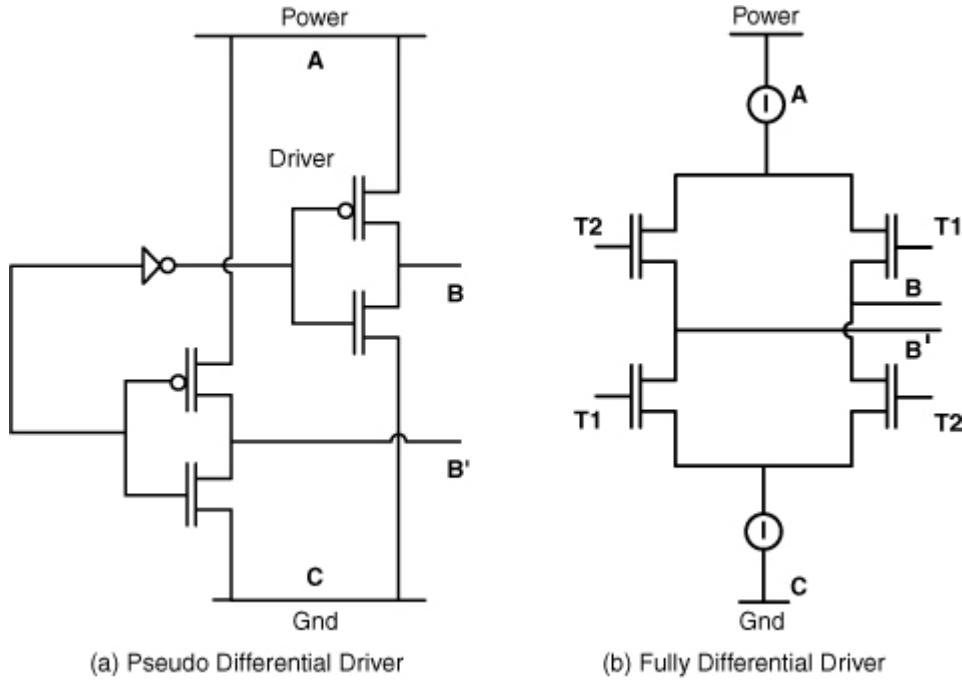
2.2. Differential Drivers and Receivers

A differential system comprises a driver, a transmission line pair, and a receiver. For a single-ended input or output buffer, there is only one dedicated terminal referenced to the common ground or power. For a differential input or output buffer, there are two dedicated terminals, separate from the common power or ground [2]. The differential signaling requires two pins per driver whereas single-ended signaling requires one pin per driver. At the differential driver or differential receiver, the signal is referenced from one signal to the other and not referenced to the common ground or power. However, in the transmission line pair, the signal will be referenced to the other line or to the ground or both depending on the geometry. For all practical applications, even with tight coupling, the return current flows through the reference planes due to the geometry.

In the following section, only conceptual representation of the differential drivers and receivers is shown. The actual implementation may be different. I/O Buffer Information Specification (IBIS) modeling cookbook [2] classifies the differential drivers as pseudo differential, half-differential, and fully differential. A pseudo differential driver is also known as a complementary driver. Also, a half-differential and a fully differential driver are also known as just “differential” drivers. In this chapter, terminology similar to that in IBIS modeling cookbook is used.

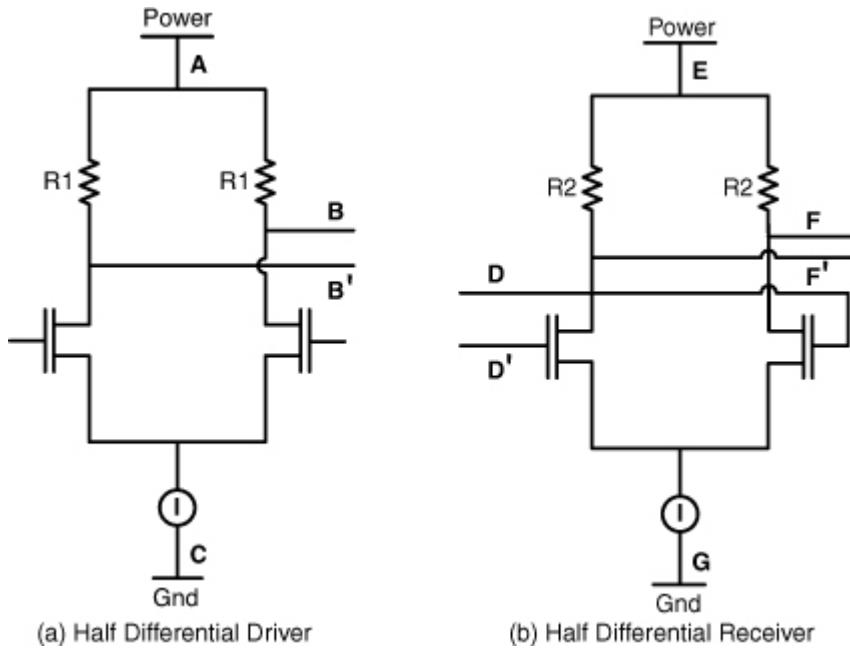
Figure 2.13 shows a pseudo differential driver and a fully differential driver [2]. A pseudo-differential driver comprises two single-ended drivers. There are two output terminals B and B'. It is essentially a voltage mode driver, and the output swing is determined by the supply voltage. There is a differential load between these output terminals, at the receiver. It needs an external low voltage supply for the low swing output. Reference [4] shows techniques to improve the performance of the voltage mode differential driver.

Figure 2.13. Pseudo differential and fully differential drivers



The implementation for fully and half differential driver shown in [Figure 2.13](#) and [Figure 2.14](#) considers the current steering or current mode topology. As shown in the figure, in a fully differential driver, there are two current sources, one connected to the power and the other to the ground. When the transistors T1 are turned on, the transistors T2 are turned off, and vice versa. When transistors T1 are turned on, the current flows from the power supply through the top current source to the output terminal B. This type of fully differential driver is connected to a differential termination, that is, termination between two differential signals. The return current comes to terminal B' and goes to the ground through the bottom transistor T1 and bottom current source. Similarly, when the T2 transistors are turned on, the current will exit through the output terminal B' to the differential termination. Then it enters back in to the terminal B and goes to the ground through the bottom transistor T2 and bottom current source. The advantage of the fully differential driver is that the current in the power node is near constant, and the rate of change of the current is small. It is less susceptible to power or ground variations.

Figure 2.14. Half differential driver and receiver



The half differential driver and receiver are shown in Figure 2.14 [2]. In a half differential driver, there is only one current source near the power or ground terminal. The other current source is typically replaced by resistor terminations. As shown in Figure 2.14, the current source is connected to the ground node C. The outputs of the two transistors are B and B'. They are terminated to the power node A by resistors. For the half differential receiver, the inputs are D and D' and are differential in nature. The current source is connected to ground node G. The output is at the nodes F and F'.

The fully differential driver has two current sources compared to one current source in a half differential driver. The power consumption may or may not be the same depending on how much current is sourced. A half differential driver can use terminations and can have enhanced performance compared to a fully differential driver.

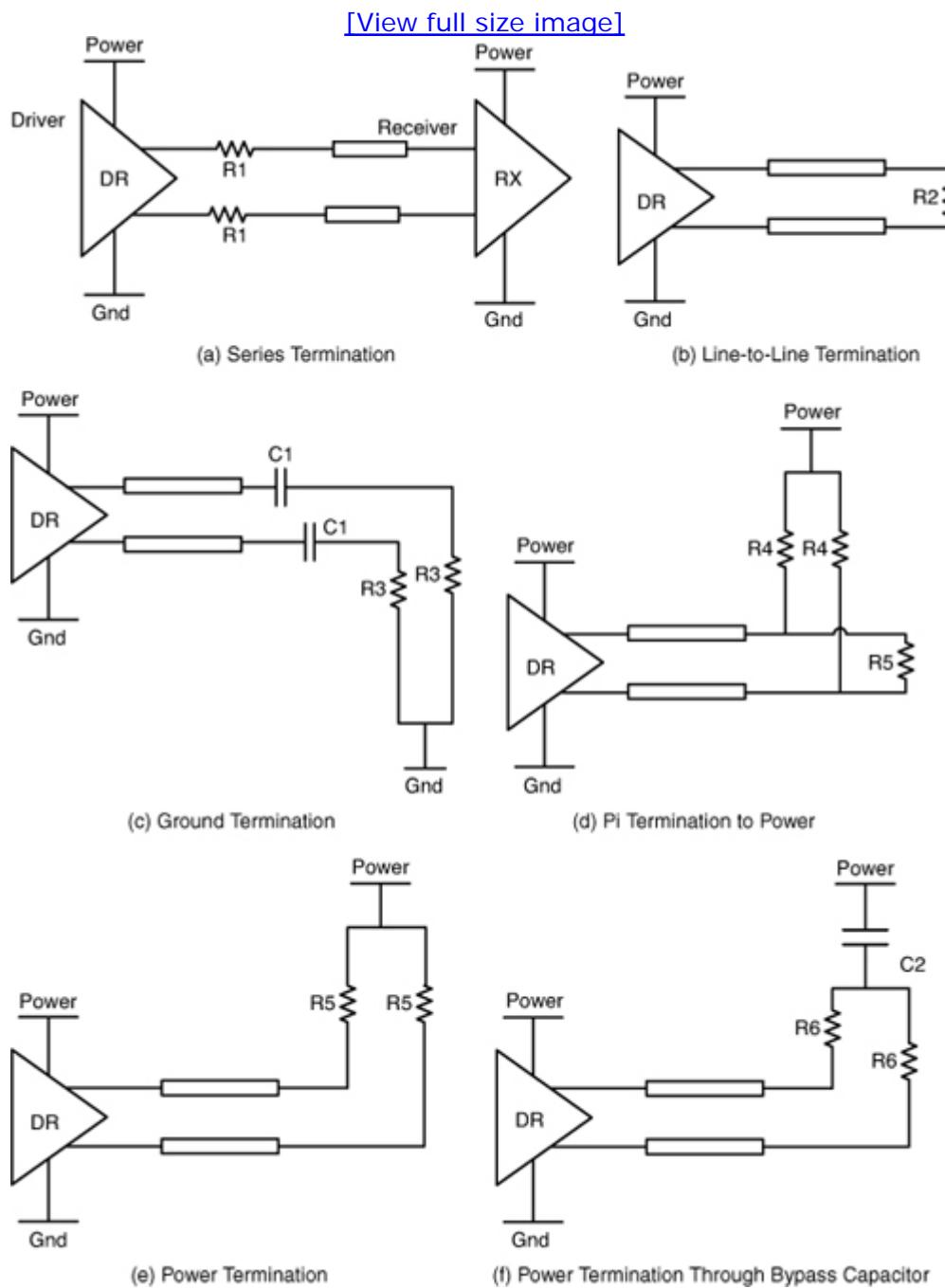
2.2.1. Termination Schemes for Differential System

The termination scheme for differential signaling is also an important factor in determining signal quality. The challenges introduced in the differential terminations are balanced termination design and power consumption control. Tolerance of components and power consumption of a different termination scheme should be carefully considered to achieve the design goal.

Figure 2.15 shows different termination schemes for a differential link [5, 6]. Series termination in Figure 2.15(a) is used for a point-to-point, low-speed and low-power system. It is used for a low-impedance driver, and a series resistor compensates the difference between transmission line characteristic impedance and output impedance of the driver. For this scheme, the signal integrity is modestly reserved. Figure 2.15(b) shows

line-to-line termination at the receiver; however, with this scheme common mode noise may be an issue with any imbalance in differential pair. Ground or power termination in [Figure 2.15\(c\)](#), [Figure 2.15\(d\)](#), and [Figure 2.15\(e\)](#) show good signal integrity quality at a high speed, but additional resistors are required that increase the cost of the system. In particular, power termination through a bypass capacitor in [Figure 2.15\(f\)](#) is a popular choice for clock differential signal termination because it wastes little power. However, too big of a bypass capacitor takes a long time to charge up, and a too small bypass capacitor is not effective enough for low-frequency noise bypass. Therefore, careful optimization of the value of the bypass capacitor and charging circuits is needed to get the most benefit of the scheme.

Figure 2.15. Termination schemes for differential link

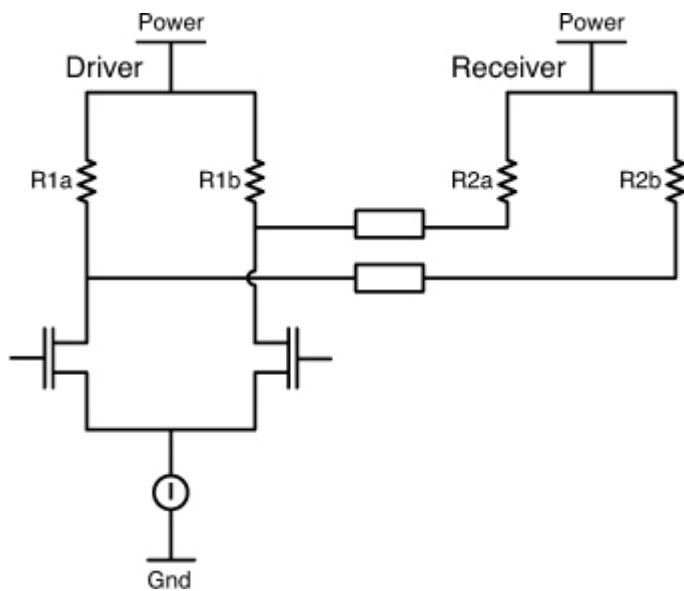


Intentional bias or mismatched differential signals create a common mode signal, which is the major sources of Electromagnetic Interference (EMI). Common mode rejection ratio (CMRR), which is the ratio of a differential gain over a common mode gain, is an important factor when evaluating a differential buffer. It is usually frequency-dependent; therefore, its frequency domain characteristic should be well examined. A common mode of differential signals can occur because of a signal trace routing mismatch and termination mismatch. Termination mismatch often comes from tolerance of the termination components.

2.2.2. Current Profiles in Half Differential Driver

A typical example of a half differential driver is shown in [Figure 2.16 \[5\]](#). There are two output terminals B and B', which have transmission lines connected to them. The far end of transmission lines are terminated to a power node (at the receiver) through resistors R2.

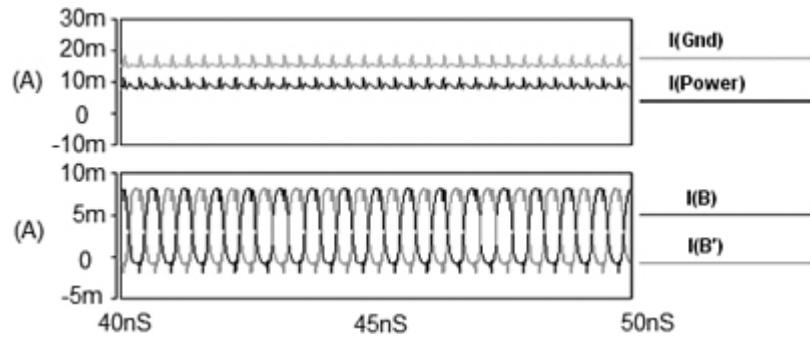
Figure 2.16. Half differential driver with power termination



[Figure 2.17](#) shows current profiles in power and ground nodes at the driver and currents in the transmission lines [5]. If there is a differential line-to-line termination at the far end, then the transmission line currents would be equal and opposite. However, because the termination is to the power node at the receiver, there is a DC current flowing in the transmission line. Because of this, the summation of currents in the transmission line is not zero but produces a net DC current.

Figure 2.17. Half differential driver currents for normal operation

Source: V. Pandit and M. Mirmak, “Differential System Design and Power Delivery,” IBIS Summit, Feb., 2006.

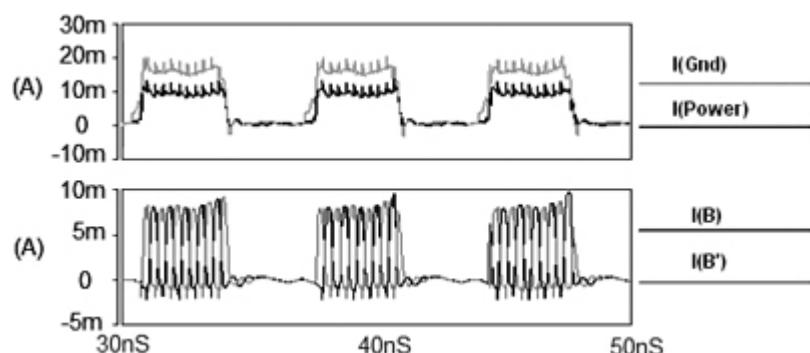


When the left transistor is on, the transistor at the right is off. The current flows from the R1a resistor from the driver power and also from the R2b resistor from the receiver power node. These two currents are added, and the summation is equal to the current sourced from the current source I. Similarly, there are two currents when the transistor at left is off and the other one at the right is on. In both cases, the current from the driver power node is added to the far end current from the receiver power node and flows through the ground node at the driver. Thus, the current in power node is smaller than the current in the ground, as shown in the figure. These currents are plotted in the normal operation of the driver.

The half differential driver may be powered off to save power, in certain architectural modes. It is then powered on when the data transmission is required. There is some latency involved between the power on event and the data transmission. An example of a power on/off scenario is shown in Figure 2.18 [5]. The currents in the driver power, ground, and transmission lines are shown. When the driver is powered off, there is no current in the transmission line, in the power, or in the ground node at the driver. When it is powered on, the normal operation current flows as described in the previous section. Again, when it is powered off; all the currents return to zero. The currents in the power node and the ground node follow a step, so the di/dt is produced. The di/dt for the ground is larger than that for the power. This di/dt produces voltage noise at the driver power/ground nodes.

Figure 2.18. Half differential driver current in power on/off events

Source: V. Pandit and M. Mirmak, "Differential System Design and Power Delivery," IBIS Summit, Feb., 2006

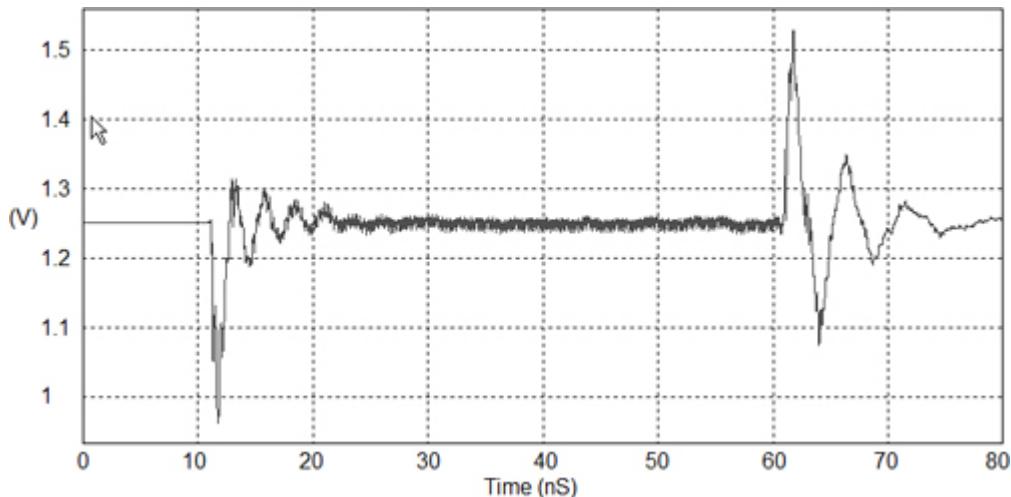


2.2.3. Noise for Half Differential Driver

A typical simulated voltage noise plot for this type of driver is shown in [Figure 2.19 \[5\]](#). Consider a differential interface with a certain number of drivers operating together. At $t=12\text{ns}$, there is a power-on condition for the driver. There is voltage droop due to sudden di/dt in the power/ground nodes. Then the voltage settles with some ringing. At the steady state, when the differential link transfers the data, there is high-frequency noise. At $t=60\text{ns}$, there is a power-off scenario. The voltage bounces to a higher voltage and then settles down. This steady state noise is much smaller than the power-on or power-off state noise.

Figure 2.19. Noise profile for half differential driver

Source: V. Pandit and M. Mirmak, “Differential System Design and Power Delivery,” IBIS Summit, Feb., 2006



[Table 2.3](#) provides characteristics of single-ended and differential signaling. For the single-ended signaling, at the driver output and the receiver input, the signal is referenced to power/ground terminal. The interconnect structure from driver to receiver can be a microstrip or stripline and return currents flow through the nearby power and/or ground reference planes. In the case of differential signaling, at the driver output and the receiver input, the signal is referenced from one terminal to the other terminal with ground as a global reference. The interconnect structure from the driver to the receiver is made primarily of a coupled line. Depending on the geometry of the structure, the coupling between the two lines is determined. If the coupling is strong and the nearby reference plane coupling is weak, then the return currents flow through the other line. However, for most of the practical package and PCB systems, the coupling between the two lines is weak and there is a strong coupling to nearby reference planes. In this scenario, the return currents still flow through the reference planes, and not through the other line.

Table 2.3. Single-Ended and Differential Link Comparisons

	Single Ended	Differential
Reference scheme at the driver/receiver	Ground and/or power	From one terminal to other terminal with ground as global reference
Return current path at the interconnect	Return currents go through nearby power/and or ground reference planes	Return current path is dependent on the geometry of the structure For typical geometries, strong return currents go through the reference planes
Higher di/dt condition state	Normal operation	Power on/off
Susceptibility to noise	More susceptible	Less susceptible
Data Rate	Low–medium	High

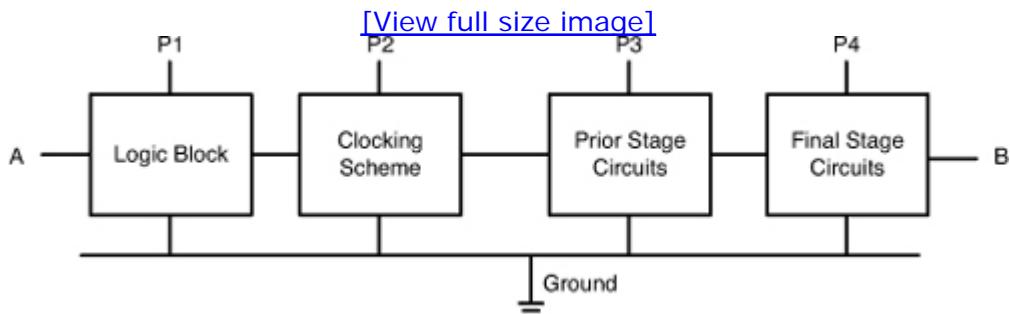
Compared to singled-ended signaling, differential signaling can operate at higher data rate at the expense of increased pin-count. Generally, differential signaling gives a superior response to single-ended signaling because of less crosstalk/power noise generation and common mode noise rejection by the receiver and coupled interconnection line. Nevertheless, a slight mismatch could introduce mode conversion from a differential mode to a common mode or a common mode to a differential mode. So, it becomes important to design circuits and transmission lines that are well balanced enough to have the received signal within the specification. The common-mode rejection ratio is an important factor to determine how much the circuit can be designed to tolerate mismatch in the differential signal.

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2.3. Prior Stages of I/O Interface

In the previous sections, the termination schemes, current profiles, and noise profiles for single-ended and differential drivers and receivers are examined. The driver and receiver circuits shown were typically for the final stage of the I/O interface. As shown in [Chapter 1, “Introduction,”](#) there are Tx and Rx high-speed I/O circuits in the prior stage of the driver and receiver. Also, there is a clocking circuitry providing the clocks to the driver and receivers. [Figure 2.20](#) shows power domains for different circuitry in the I/O interface.

Figure 2.20. Power domains for I/O interface



A generic block diagram for the transmitter and receiver paths is shown in [Figure 2.20](#). For the transmit path the data is flowing from A to B, and for the receive path it is from B to A. For the transmitter, the final stage is the driver, and the prior stage may include the predriver, equalizer, multiplexer, and so on. In the receive path, the prior stage may include a sampling amplifier, a serial-to-parallel converter, and so on. Different stage circuits may or may not be on the same power rail as the final stage circuits. Power nodes P1, P2, P3, and P4 may have the same power rail or different power rails. If all or some circuit blocks share the power rails, then the noise coupling needs to be taken into account for those blocks. As an example, the predriver and the driver final stage are at the same power rail; then while evaluating the noise, both the stages (the predriver and the driver) are considered. In another example, if the clock circuits and the final stage circuits share the same power rail, then the effect of noise from the final stage circuits on the clock circuits need to be considered. For some sensitive

clocking circuits, it may be required to utilize isolated power domains. Whether or not different circuits within the I/O interface share the same voltage domain is determined by considering various factors, including the noise sensitivity, package and board routing area, and the cost.

For an I/O interface, the current flow path needs to be examined. The current generated at the power node produces noise at the chip. This noise becomes prominent when multiple drivers and receivers are operating simultaneously. It gets coupled to the interconnect lines and affects the signal performance. These signal and power integrity effects for the interconnect system are analyzed with the electromagnetic theory, which is summarized in the next chapter.

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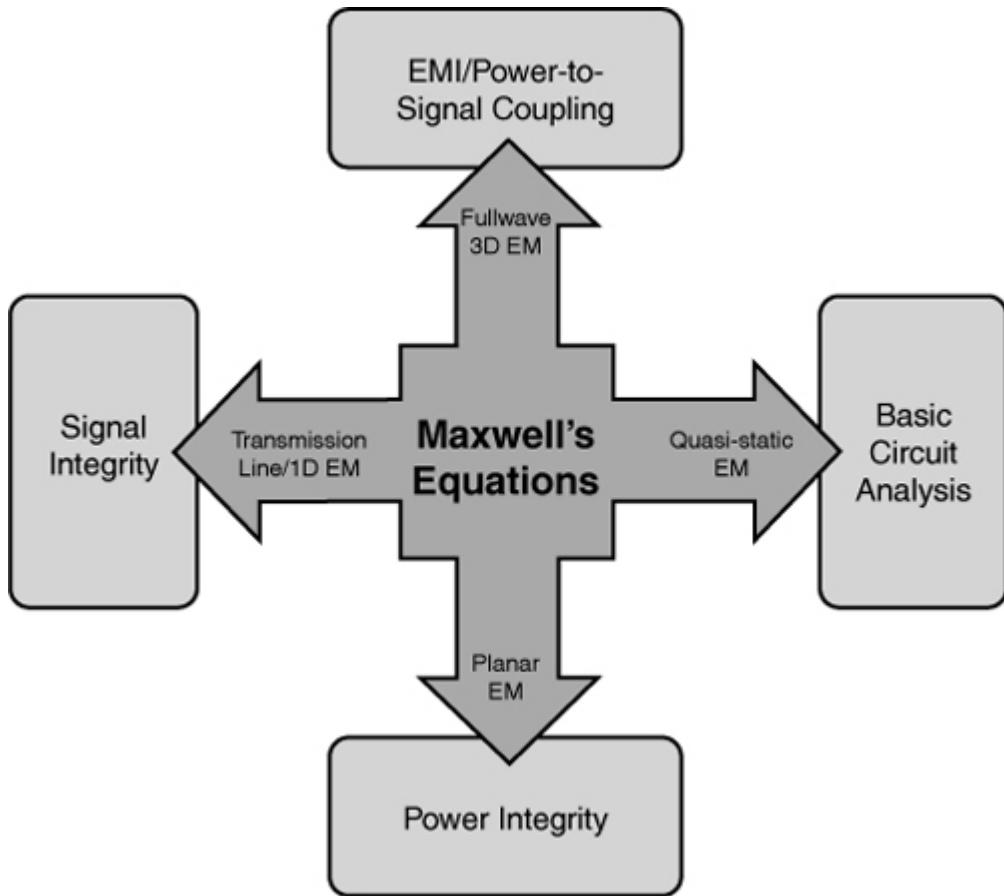
Chapter 3. Electromagnetic Effects

This chapter addresses the basic principles that underlie the co-analysis/design of power/signal integrity. The origins of Signal Integrity (SI), Power Integrity (PI), and Electromagnetic Interference (EMI) and the significance of understanding interactions between them are discussed. An overview of how you can analyze and solve issues relating to these terms is also presented.

3.1. Electromagnetic Effects on Signal/Power Integrity

In recent years, we have made impressive progress in raising data rates of I/O interfaces. System-on-chip (SoC), CPU and chipset designers, nevertheless, need to do more than simply make their systems operate under typical conditions in the laboratory. As the systems operate at 1GHz and beyond, a number of signal integrity, power integrity, and electromagnetic interference problems become exponentially more complicated and crucial to the overall system bandwidth. The problems connected with high-frequency effects, such as Inter-Symbol Interference (ISI), crosstalk, timing jitter, reflection, Simultaneous Switching Output (SSO), power/ground noise coupling to signal, and noise amplification steadily attract more attention. In turn, these problems become more critical; particularly in high-speed digital interconnect systems at multi-Gbit/sec data rates. These issues prove to be increasingly crucial in determining the processing speeds of digital systems. As shown in [Figure 3.1](#), many signal integrity, power integrity, and EMI problems are electromagnetic in nature and hence related to the electromagnetic effects.

Figure 3.1. Applied Maxwell's theory for Signal Integrity, Power Integrity, and EMI



Signal Integrity is a measure of the quality of an electrical signal. In the area of high-speed I/O signaling design, Signal Integrity has become a critical issue and poses increasing challenges to the I/O interface design engineers. Major Signal Integrity issues such as crosstalk, ISI, signal reflection, noise amplification, and so on are primarily due to transmission line effects, which usually are based on the 1-dimensional (1D) electromagnetic (EM) Maxwell's theory as depicted in [Figure 3.1](#). To answer the market demand for a better understanding of signal behavior and transmission line effects, manufacturers have designed and tuned simulation tools and testing instruments.

The preferred mode of electromagnetic signal wave propagation on a transmission line is Transverse Electromagnetic (TEM) because it comprises an extremely low loss and fast mode propagation. The TEM mode, due to perpendicular propagation of the fields with respect to the signal, usually propagates in most transmission lines except for the wave-guides where the higher modes such as Transverse Electric (TE) and Transverse Magnetic (TM) modes flow. The TEM mode has electromagnetic field variations only in the perpendicular cross-section directions, and no field variations in the z-axis or transmission line axial direction. This enables both mono-mode propagation and simplified transmission line characteristics and behavior. A transmission line can support a purely TEM mode in a homogeneous dielectric medium between a minimum of two perfect conductors. Basic circuit analysis can be done using a quasistatic electromagnetic solver. For a

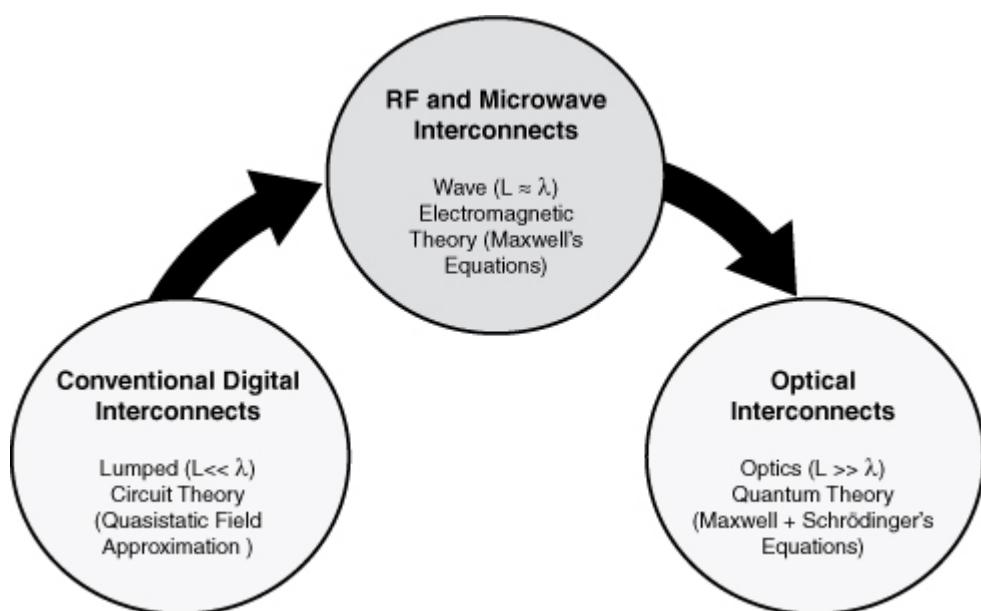
typical power integrity analysis, a planar electromagnetic solver is adequate. The planar electromagnetic solver can analyze planar structures such as power/ground plane structure and nonuniform microstrip networks. In a 3D planar EM solver, the Maxwell's equations are solved primarily for the 2D plane structures, and the electrical parameters are locally solved or projected in the third dimension. For power noise to signal coupling analysis, or EMI analysis, a full-wave 3-dimensional (3D) electromagnetic solver will be necessary. In a full-wave electromagnetic tool, the Maxwell's equations are solved for the entire geometry.

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3.2. Electromagnetic Theory

In this section, we enhance the reader's understanding of the basics of RF effects based on Maxwell's equations and electromagnetic theory. As shown in [Figure 3.2](#), for digital systems, digital interconnection is moving from low-speed lumped interconnection domain to RF and microwave interconnection domain. This frequency range is around 0.2 GHz to 10 GHz. In this range, we should consider electromagnetic phenomena for signal integrity when designing for medium line lengths, 3 mm to 3 m. It is essential to apply EM modeling, design and simulation, optimization, and characterization to high-speed digital interfaces. Moreover, we should use Radio Frequency (RF) and microwave technology for high-speed digital system design. RF effects become more visible for high-speed I/O interfaces, and RF technology is a viable alternative for improving interconnection bandwidth. After that, RF and microwave interconnection can change to optical interconnection.

Figure 3.2. Interconnect technology and analysis techniques



Because of the complexity of Maxwell's equations, numerous special techniques have been developed for solving the equations in special

situations. Three ranges in the frequency spectrum for extensive special techniques are shown in Figure 3.2. In the case of conventional digital interconnects, the special analysis techniques known as circuit theory are obtained from Maxwell's equations by applying an approximation, called the quasistatic field approximation, which is valid when $L \ll \lambda$, where λ , the wavelength, and L , the approximate dimension of interconnects, for example interconnection line, power/ground plane, and so on. As the electrical size increases, $L \approx \lambda$, inductive and conductive effects become more visible, and skin effect exists in the RF and microwave interconnects. Optical interconnect technology has been widely used for decades in long-distance ($L \gg \lambda$) and/or ultra-high performance applications such as super-computer communications, telephony, and wide area networks (WANs).

3.2.1. Maxwell's Equations

In this section, we conceptually describe equations of Maxwell's theory that underlie the interaction between power and signal integrity and how they link together to explain the origin of electromagnetic radiation such as light. The term "Maxwell's equations" refers to a set of original eight equations; however, it refers to a set of modified four equations grouped together by Heaviside, in differential formulation. In this section, we present these four equations. Later, we also present eight original equations with vector notations.

The following examples depict the four Maxwell's equations in differential form [1]. Each law is named according to the individual or individuals who originally discovered the connections that the equation represented. These are vector notations unless specified.

Equation 3.1

Faraday's law:

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

Equation 3.2

Ampere-Maxwell law:

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

Equation 3.3

Gauss' law for electricity:

$$\nabla \cdot D = \rho$$

Equation 3.4

Gauss' law for magnetism:

$$\nabla \cdot B = 0$$

Where

H is the magnetic field intensity, which Maxwell called the "magnetic intensity" (A/m).

B is the magnetic flux density (T or Wb/m^2).

E is the electric field intensity (V/m).

D is the electric flux density, called the "electric displacement" by Maxwell ($Coulombs /m^2$).

J is the electric current density comprising of conduction and convection current densities (A/m^2).

$\frac{\partial D}{\partial t}$ is the displacement current density (A / m^2) due to the motion of bound charges in dielectric medium.

$B = \mu H$ and $D = \epsilon E$ are constitutive relationships. where μ is the permeability ($Henry/m$) and ϵ is permittivity (F/m).

ρ is the free charge density, called the "quantity of free electricity" by Maxwell ($Coulombs /m^3$). ρ is a scalar quantity.

Maxwell's four equations, formulated by James Clerk Maxwell, together form a complete description of the production and interrelation of electric and magnetic fields. The statements of these four equations are

- Equation (3.1): electric fields are produced by changing magnetic fields.
- Equation (3.2): circulating magnetic fields are produced by changing electric fields and by electric currents.
- Equation (3.3): total electric flux passing through the enclosed surface is equal to the total charge within the enclosed surface.
- Equation (3.4): The total flux through a closed surface in a magnetic field must be zero; law of conservative of magnetic flux or Gauss's law for magneto-static field.

Equations (3.1) and (3.2) express that a changing electric field generates a magnetic field; in turn, that change in the magnetic field generates an electric field. We can conclude that the electromagnetic field will propagate spontaneously through regions of total vacuum in the form of a wave of E and H fields; working with/against each other, as shown in [Figure 3.3](#) and

Figure 3.4. The eight original Maxwell's equations can be written in modern vector notation as follows [2]:

(A) **The law of total currents:** Total current is the summation of conduction, convection, and displacement currents. \mathbf{J} is the conduction current plus convection current densities. $\frac{\partial \mathbf{D}}{\partial t}$ is the displacement current density:

Equation 3.5

$$\mathbf{J}_{tot} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}$$

(B) **The equation of magnetic flux:** \mathbf{B} can be expressed as the curl of the vector field \mathbf{A} defined as the vector magnetic potential. It is similar to the introduction to the scalar electric potential φ in equation (3.8):

Equation 3.6

$$\mathbf{B} = \nabla \times \mathbf{A}$$

(C) **Ampère's circuital law:** The circulation of magnetic field intensity \mathbf{H} around any closed path is equal to the free space current flowing through the surface bounded by the path:

Equation 3.7

$$\nabla \times \mathbf{H} = \mathbf{J}_{tot}$$

(D) The electromotive force created by convection, induction, and static electricity. (This is in effect the *Lorentz force*.):

Equation 3.8

$$\mathbf{E} = \mu \mathbf{v} \times \mathbf{H} - \frac{\partial \mathbf{A}}{\partial t} - \nabla \varphi$$

Here, φ refers to the electrostatic potential energy, and \mathbf{v} is the instantaneous velocity of the particle. φ is scalar potential and \mathbf{A} is vector potential.

(E) **The electric elasticity equation:** The electric flux density \mathbf{D} is proportional to the electric field intensity \mathbf{E} with permittivity ϵ of a medium:

Equation 3.9

$$D = \epsilon E$$

(F) **Ohm's law:** It is the point form of Ohmic's law. The potential difference across an ideal conductor is proportional to the current through it:

Equation 3.10

$$J = \sigma E$$

(G) **Gauss's law:** This relates an electric charge contained within a closed Gaussian surface to the surrounding electric field:

Equation 3.11

$$\nabla \cdot D = \rho$$

(H) **Equation of continuity:** The principle of conservation of an electric charge must be satisfied at all times and under any circumstances:

Equation 3.12

$$\nabla \cdot J = -\frac{\partial \rho}{\partial t}$$

Figure 3.3. Transverse Electromagnetic (TEM) wave propagation

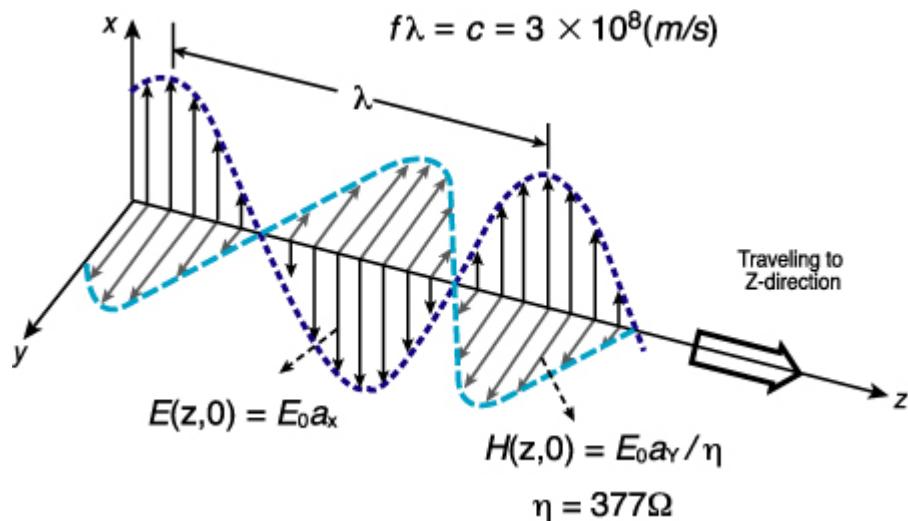
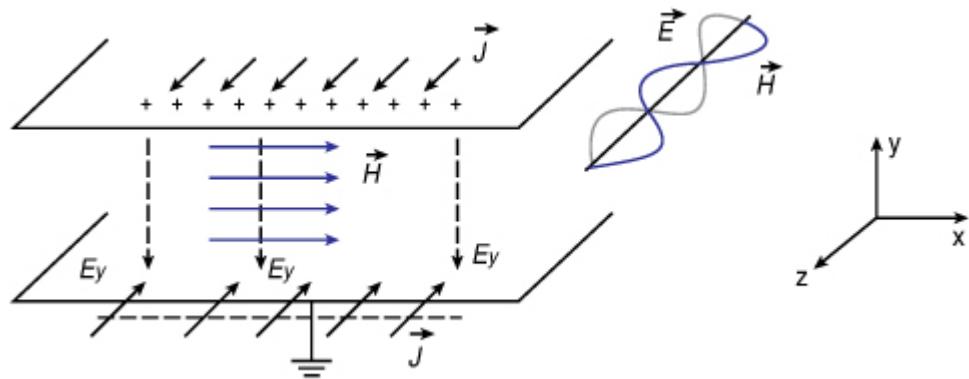


Figure 3.4. Electromagnetic wave in a parallel plate waveguide



This equation relates the net flow of current to the rate of decrease of charge.

The Maxwell's equations described in equations (3.1) through (3.4), with the constitutive relations formulate a minimum complete set of electromagnetic behavior.

Figure 3.3 shows that electromagnetic waves are formed when an electric field couples with a magnetic field. The magnetic and electric fields of an electromagnetic wave are perpendicular to each other and to the direction of the wave. A changing E produces B and a changing B produces E . In the air, electromagnetic fields are oscillating and regenerating, and electromagnetic waves are propagating at the speed of light.

To drive a wave equation, we start with Maxwell's equations and take the curl of Faraday's law in equation (3.1). By using the vector identity, we derive a wave equation for the E field as shown in equation (3.13). Similarly, taking the curl of the Ampère-Maxwell equation (3.2) gives a wave equation of the H field in equation (3.14). You can easily show that an identical equation exists for B . A more general derivation yields the 3D version. For a source-free region, the following wave equations are applicable:

Equation 3.13

$$\nabla^2 E = \mu\sigma \frac{\partial E}{\partial t} + \mu\epsilon \frac{\partial^2 E}{\partial t^2}$$

Equation 3.14

$$\nabla^2 H = \mu\sigma \frac{\partial H}{\partial t} + \mu\epsilon \frac{\partial^2 H}{\partial t^2}$$

Power/ground plane noise and its coupling onto signal trace are the most difficult EM effects to be modeled in system signaling analysis because of the complexity of the power/ground distribution system. Transient currents

drawn by a large number of devices (logic, clocks, drivers) switching simultaneously can cause voltage fluctuations between power and ground planes, SSO, or Delta-I noise, or power fluctuation/ground bounce. SSO would slow down the signals due to an imperfect return path constituted by the power/ground distribution system. It would also cause a logic error when it couples to quiet signal nets or disturbs the data in the latch.

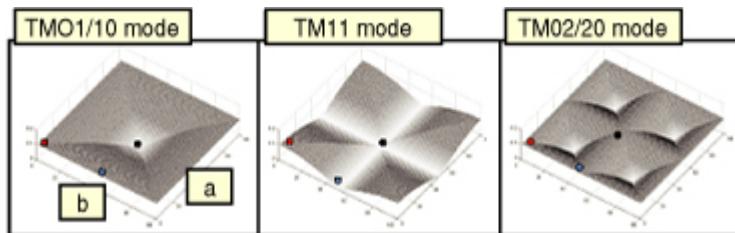
Maxwell's equations govern the propagation of electromagnetic fields. The electromagnetic wave equation is a second-order partial differential equation that describes the propagation of electromagnetic waves through a medium or in a vacuum. A pair of closely spaced parallel planes behaves much like an ideal resonant cavity with two PEC (perfect electric conductor) and four PMC (perfect magnetic conductor) boundaries. The following equation shows the resonant frequencies of a power/ground plane:

Equation 3.15

$$(f_r)_{mn} = \frac{1}{2\pi\sqrt{\mu_0\epsilon_0\epsilon_r}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}$$

where m and n are mode numbers equal to 0, 1, 2, . . . and a and b are the dimensions of the plane length and width, as shown in [Figure 3.5](#).

Figure 3.5. Poles and zeros of power/ground fields distribution



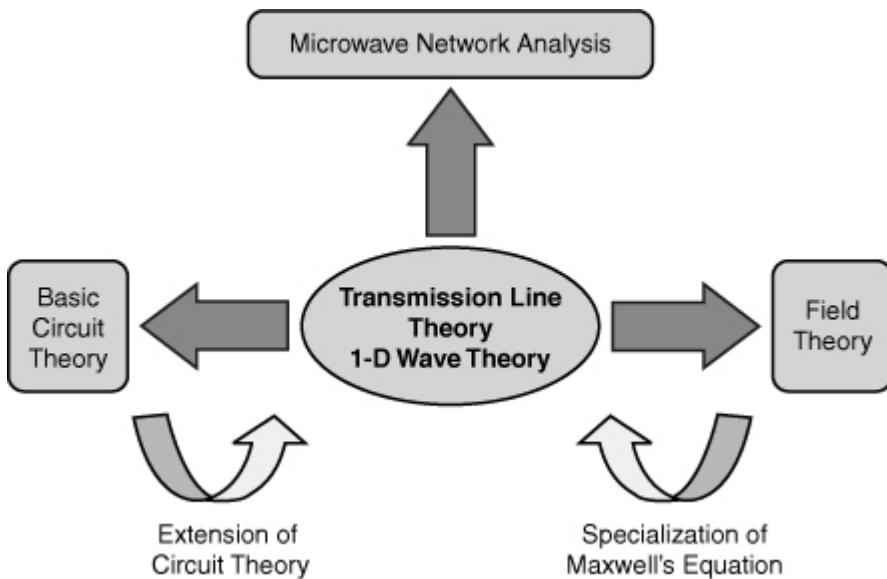
Designing a robust power distribution network for high-speed I/O signaling has become a challenging task. With equation (3.15), the location of poles and zeros, as shown in [Figure 3.5](#), can be predicted at the different resonant modes. Based on the location of the poles and zeros, the magnitude response of the power and ground plane can be quickly understood. A power/ground distribution plane on the package and PCB is a major noise source and a coupling structure as the impedance magnitude of the plane determines the fluctuations in the power/ground plane. Power/ground distribution networks necessitate reduction of these undesired noise levels, especially at some sensitive parts of I/O interfaces such as the reference transition area and chip area with high-speed I/O circuitry. In general, it is crucial to mitigate the resonance voltage fluctuations of all critical hot spot regions (poles) of a power/ground plane by adding decoupling capacitors.

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3.3. Transmission Line Theory

In many ways, the Transmission Line Theory bridges the concept between field analysis and circuit theory, underlies the channel resonance of power/ground planes and signal traces, and is significant in signal and power integrity modeling and simulation. As you can see in [Figure 3.6](#), the phenomena of wave propagation on transmission lines may be approached from an extension of the circuit theory or from the specialization of Maxwell's equations. We describe both viewpoints and show how the field theory approach is differentiated from the lumped circuit theory approach, and describe 1D transmission line equations, called Telegrapher's equations [3].

Figure 3.6. Transmission Line Theory: 1 dimensional electromagnetic



As shown in [Table 3.1](#), the major deviation from the circuit theory with the transmission line distributed network is the positional dependence of voltage and current. We must consider it in terms of the position and time to understand the transmission line behavior. This positional dependence is added when the assumption of the size of the circuit being small is compared to the signaling wavelength. The RLC lumped elements describe

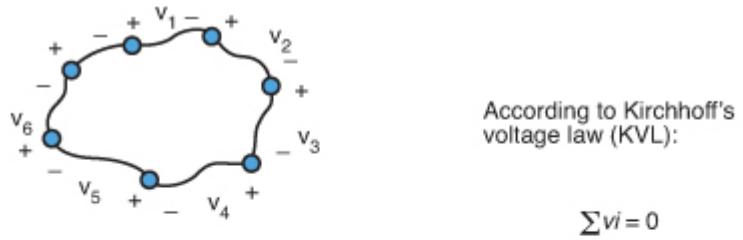
the behavior of the charging and discharging mechanism whereas the characteristic constants such as characteristic impedance, attenuation constant, and phase constant describe the behavior of the wave propagation mechanism. The Vector Network Analyzer (VNA) is widely used to characterize the behavior of transmission line.

Table 3.1. Transmission Line Theory Versus Lumped Circuit Theory

	Lumped Circuit Theory	Transmission Line Theory
Voltage and Current Equation	$V(t) = V_0 \cos(\omega t + \phi)$ $Z_{in} = \frac{V(t)}{I(t)}$, where ...	$V(t) = V_0^+ \cos(\omega t - \beta z + \varphi^+) + V_0^- \cos(\omega t + \beta z + \varphi^-)$ $Z_0 = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-}$, where ...
Operation	Time-varying Voltage, Current as a function of time	Traveling Voltage and Current Wave as a function of both location and time
Describing Elements	R, L, C	Z_0 (impedance), propagation constant ($\gamma = \alpha + j\beta$)
Measurement	RLC meter	Time-Domain Reflectometer (TDR), Vector Network Analyzer (VNA)

In circuit analysis, the RLC of an interconnect system are lumped together based on quasistatic EM theory; as shown in [Figure 3.1](#). An interconnect system can be modeled by a transmission line including inductive and conductive effects, based on specialized 1D Maxwell's theory; that is, it can be modeled as an electric circuit (combination of paths, each containing one or more circuit elements) if $\lambda = c/f \gg$ physical dimensions of the power/ground plane and signal trace. For any lumped circuit, Kirchhoff's Voltage Law (KVL) states that the algebraic sum of all voltages around any closed path in a circuit at any time equals zero, as shown in [Figure 3.7](#). No time-varying magnetic flux through the interconnect loop or the electrically short-loop is necessary to satisfy KVL. Otherwise, there would be an induced voltage (or noise) based on Faraday's law, which states the algebraic sum of the branch voltages around a loop cannot be zero. To analyze the interconnect network, we have to use a distributed model rather than a lumped model. Antennas are designed to pick up electromagnetic waves, but regular interconnect circuits often do so undesirably.

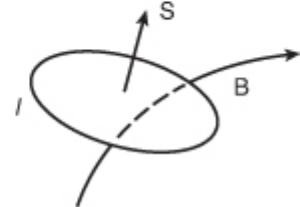
Figure 3.7. Kirchhoff's voltage law in electromagnetic theory



From Faraday's Law,

$$\sum vi = \oint E \cdot dl = \int_S \nabla \times E \cdot dS = -\frac{\partial}{\partial t} \int B \cdot dS$$

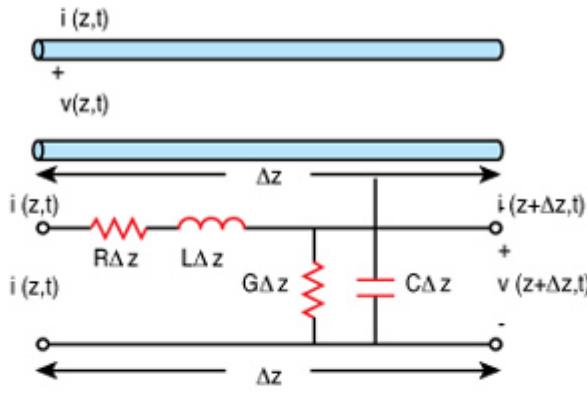
Then, in the case of $l \ll \lambda$ or time invariant fields,
this satisfies the KVL ($\sum vi = 0$)



Both electric and magnetic fields are present in the transmission lines. These fields are perpendicular to each other and to the direction of wave propagation for TEM mode waves, which is the simplest mode, and is assumed for most transmission line simulators (except for microstrip lines, which assume quasi-TEM, which is an approximated equivalent for transient response calculations). When an electric potential difference is established between two conductors, an electric field will exist between them. This implies that an equivalent circuit model must contain a distributed capacitor. In addition, a magnetic field is induced by current flowing on the line. This implies an equivalent circuit model must contain a distributed inductor. Thus, as Figure 3.8 shows, a transmission line is a distributed parameter network where voltages and currents can vary in magnitude and phase over its length [3].

Figure 3.8. Transmission line modeling (Distributed RLGC versus Lumped RLGC)

[\[View full size image\]](#)



- Two or more metal for TEM mode \Rightarrow Transmission Line
- Cross-sectional dimension $\ll \lambda$, electrical length $\sim \lambda$
 - Per-unit-length Capacitance (C) [pF/cm]
 - Per-unit-length Inductance (L) [nF/cm]
 - Per-unit-length (Series) Resistance (R) [Ω/cm]
 - Per-unit-length (Parallel) Conductance (G) [S/cm]
- If electrical length of transmission line $\ll \lambda$, we can extract lumped RLGC from

$$Z_{in_short} = R + j\omega L \Rightarrow R + \text{Re}[Z_{in_short}], L = \frac{\text{Im}[Z_{in_short}]}{\omega}$$

$$Z_{in_open} = \frac{1}{Z_{in_open}} = G + j\omega C \Rightarrow G = \text{Re}[Z_{in_open}], C = \frac{\text{Re}[Z_{in_open}]}{\omega}$$

We can drive the following equations, based on Kirchhoff's voltage law equation (3.16) and Kirchhoff's current law equation (3.17).

Equation 3.16

$$v(z,t) - R \Delta z i(z,t) - L \Delta z \frac{\partial i(z,t)}{\partial t} - v(z + \Delta z, t) = 0$$

Equation 3.17

$$i(z,t) - G \Delta z v(z + \Delta z, t) - C \Delta z \frac{\partial v(z + \Delta z, t)}{\partial t} - i(z + \Delta z, t) = 0$$

When a transmission line is not electrically short, by using (3.16) and (3.17) in the limit as $\Delta z \rightarrow 0$, Telegrapher's differential equations can be found as follows:

Equation 3.18

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L \frac{\partial i(z,t)}{\partial t}$$

Equation 3.19

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C \frac{\partial v(z,t)}{\partial t}$$

If harmonic time dependence is assumed, Telegrapher's equations are given by the following:

Equation 3.20

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z)$$

Equation 3.21

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z)$$

By applying (3.20) and (3.21), we can derive voltage and current wave equations as the following:

Equation 3.22

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0$$

Equation 3.23

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0$$

where $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$, γ : propagation constant [m^{-1}] α : attenuation constant [neper/m] (1 neper=8.686 dB) β : phase constant [rad/m].

In the physics of wave propagation, a plane wave is a constant-frequency wave whose wavefronts (surfaces of the constant phase) are infinite parallel planes of constant amplitude normal to the phase velocity vector. The Helmholtz equations, which yield the necessary plane wave solutions as shown in equations (3.13) and (3.14) can also be written in terms of the voltage (V) of equation (3.22) and current (I) of equation (3.23).

The familiar plane wave solutions to these wave equations (3.22) and (3.23) are in terms of both forward and backward traveling voltage and current waves given by the following:

Equation 3.24

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}$$

Equation 3.25

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}$$

Characteristic impedance is the ratio of the voltage and current waves at any one position on the transmission line:

Equation 3.26

$$Z_0[\Omega] = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Propagation velocity is the speed with which signals are transmitted through the transmission line in its surrounding medium:

Equation 3.27

$$v_p[m/s] = \frac{\omega [rad/s]}{\beta [rad/m]} = \lambda [m] \cdot f[s^{-1}] \quad \left(\xrightarrow{\text{Lossless}} \frac{1}{\sqrt{LC}} \right)$$

The input impedance Z_{in} of a transmission line is the ratio of V/I:

Equation 3.28

$$Z_{in} = \frac{V_1}{I_1} = \frac{V_1^+ + V_1^-}{I_1^+ - I_1^-}$$

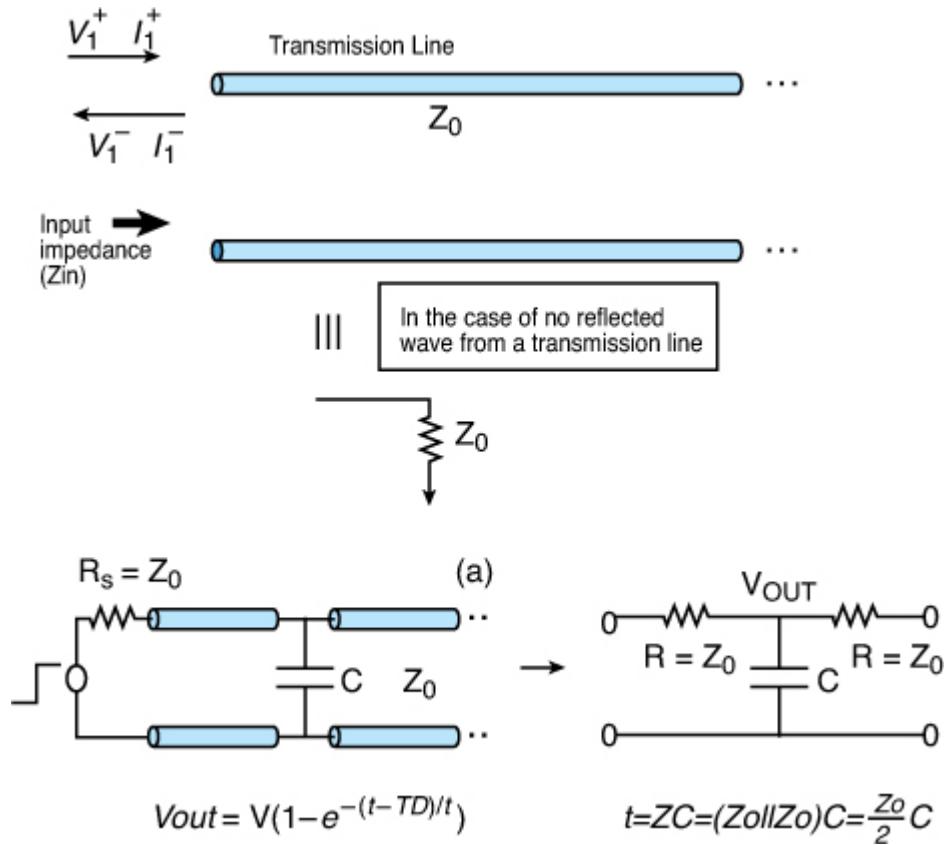
If there is no reflected wave from transmission line ($V_1^- = I_1^- = 0$), then we can simplify (3.28) as follows:

Equation 3.29

$$Z_{in} = \frac{V_1}{I_1} = \frac{V_1^+}{I_1^+} = Z_0$$

The input impedance (Z_{in}) approaches the characteristic impedance ($Z_0[\Omega]$) when no reflection from the transmission line exists, as [Figure 3.9 \(a\)](#) depicts. Similarly, to calculate the time constant (τ) of the transmission line, we can assume Z_0 transmission line as $R = Z_0$, as [Figure 3.9 \(b\)](#) reveals.

Figure 3.9. Lumped model approximation for a transmission line



By solving equations (3.24), (3.25), and (3.26) for the reflected and incident voltage wave co-efficient, we can derive the ratio of voltage wave and current wave, which is the impedance when we look toward the load end of the transmission line at a distance l from the load Z_L :

Equation 3.30

$$Z_i = Z_0 \frac{Z_L + jZ_0 \tan \gamma l}{Z_0 + jZ_L \tan \gamma l}$$

In Figure 3.10, we see that the input impedance of the transmission line with an open-ended termination is $Z_{\text{in_open}} = -jZ_0 \cot \gamma l$ whereas the input impedance of the transmission line with a short-ended termination is $Z_{\text{in_short}} = -jZ_0 \tan \gamma l$. When the line is a quarter-wavelength long, the input impedance of a lossless transmission line transforms from open to short or from short to open. Because it has the effect of transforming the load impedance, also depending on the characteristic impedance (Z_0) of the transmission line, such a line is known as a quarter-wave transformer. For high-speed chip-to-chip interfaces, the effect becomes more visible as frequency increases. The impedance of a loading device is predominated by its parasitic capacitance. Even though it has well terminated at low

frequency, due to I/O capacitance effect and the channel parasitics the channel, impedance transformation effect cannot be avoided in a high-speed interface. This may cause channel resonance problem and amplifying power/ground and crosstalk noise, as Figure 3.11 indicates.

Figure 3.10. (a) Finite transmission line terminated with load impedance Z_L . Impedance transformation of a transmission line with (b) a short-ended termination ($Z_L=0$) and (c) an open-ended termination ($Z_L=\infty$)

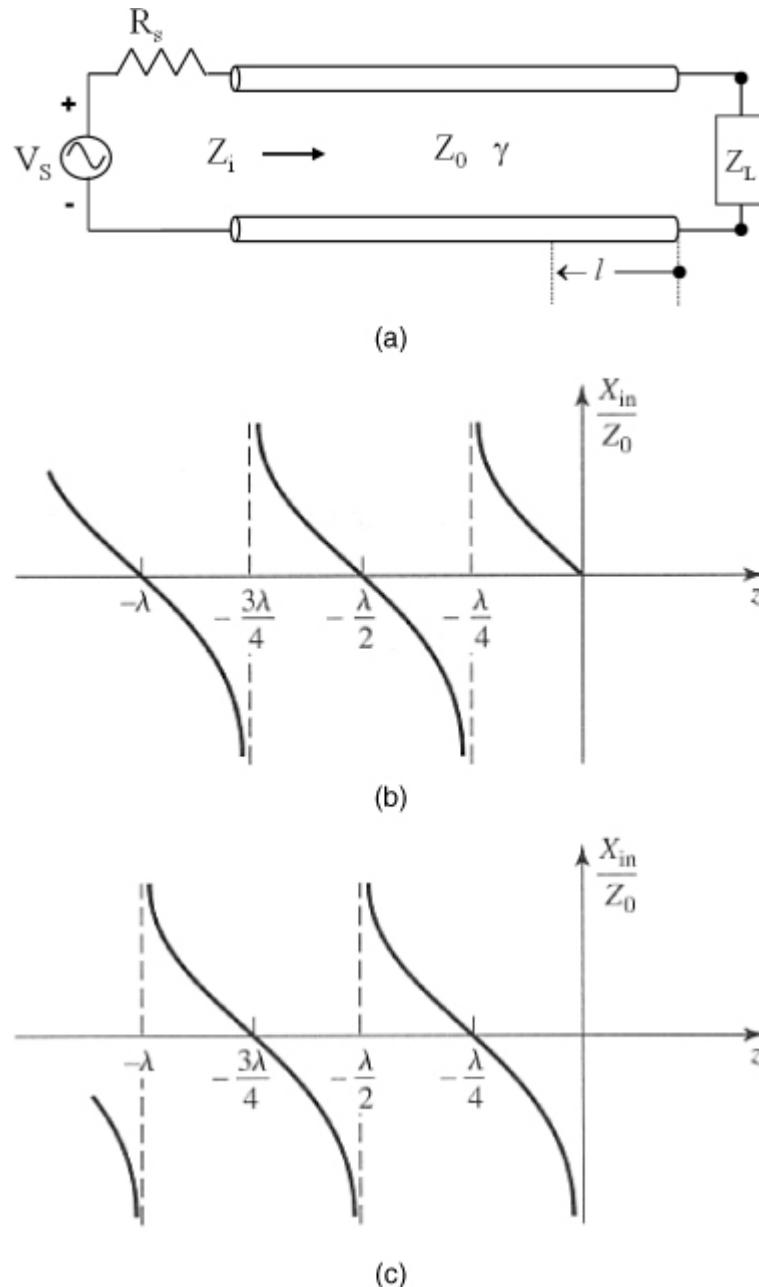


Figure 3.11. A voltage transfer function variation due to the channel impedance transformation effect (Resonant mode: An odd multiple of one-quarter wavelength $\lambda/4$)

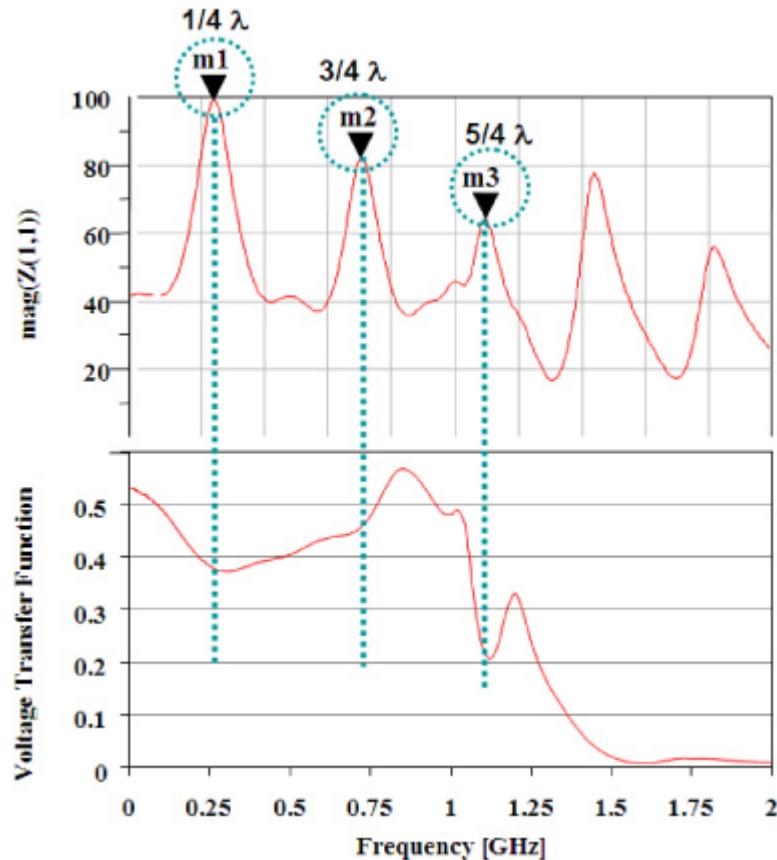


Table 3.2 depicts a number of types of impedance with their equations, definitions, and applications.

Table 3.2. Various Types of Impedance

Type of Impedance	Equation	Definition	Application
Intrinsic Impedance (η)	$\eta = \sqrt{\frac{\mu}{\epsilon}}$	It is the function of the material properties of the medium and is equal to the wave impedance for plane waves.	Radiated emission, plane wave, free space
Wave Impedance (Z_w)	$Z_w = \frac{E_t}{H_t}$	The ratio of transverse electric and magnetic fields. TEM, TM, and TE waves each have different wave impedances that may depend on the type of the	Power integrity, power/ground plane noise, waveguides

		line or guide, the material, and the operating frequency.	
Characteristic Impedance (Z_0)	$Z_0 = \frac{V^+}{I^+} = -\frac{V^-}{I^-}$	The ratio of V/I for a traveling wave on a transmission line. It is the function of the geometry and the material properties of the medium. Z_0 for TEM wave is unique.	Signal integrity, transmission line, signal reflection, impedance discontinuities
Self Impedance (Z_{self})	$Z_{self} = \left. \frac{V}{I} \right _{(all\ other\ ports= open)}$	The ratio of V/I for circuitry that is seen looking into an arbitrary port when all other ports are open.	Power integrity, characteristic impedance of power delivery network
Input Impedance (Z_{in})	$Z_{input} = \left. \frac{V}{I} \right _{(all\ other\ ports= short)}$	The ratio of V/I for circuitry that is seen looking into an arbitrary port when all other ports are short.	Lumped circuit, characteristic impedance of transmission line with no reflection

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3.4. Interconnection Network Parameters: Z,Y,S and ABCD

The performance of interconnect systems can be evaluated using formula-based calculations, waveform-level simulation, or through hardware measurements. In this section, we focus on the basic principles of RF and microwave network theory to help us understand the limiting factors for the signal/power design. This particular theory can be applied in S-parameter-based interconnects modeling and characterization discussed in [Chapter 9](#), “Measurement Techniques.” We first consider an arbitrary N-port interconnection network, as shown in [Figure 3.12](#). At the n^{th} terminal plane, total voltage and current are given by the following:

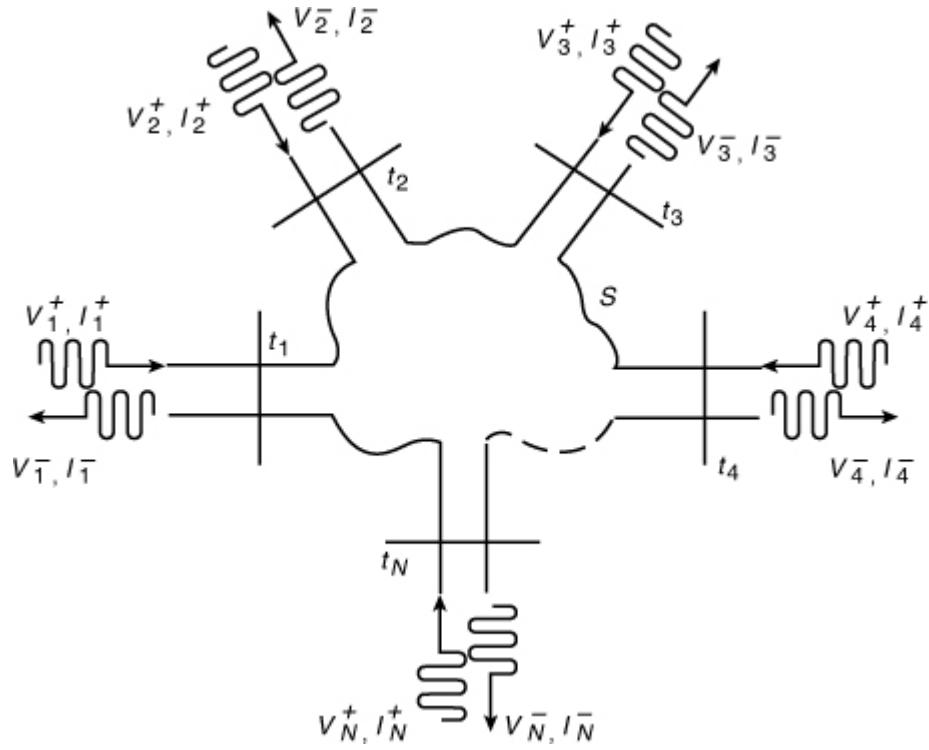
Equation 3.31

$$V_n = V_n^+ + V_n^-$$

Equation 3.32

$$I_n = I_n^+ + I_n^-$$

Figure 3.12. An arbitrary N-port interconnection network



3.4.1. Impedance Matrix [Z]

The impedance matrix (Z) of the interconnection network then relates these voltages and currents:

Equation 3.33

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1N} \\ Z_{21} & \cdots & Z_{2N} \\ \vdots & & \ddots & \\ Z_{N1} & \cdots & Z_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}$$

$$[V] = [Z][I]$$

Equation 3.34

$$Z_{ij} = \frac{V_i}{I_j} \Big|_{I_k = 0 \ (k \neq j)}$$

Equation (3.34) shows that Z_{ij} can be found by driving port j with the current I_j , open-circuiting all other ports, and measuring the open-circuit voltage at port i . Because the parameters are independent of the port impedance, the Z -parameters prove extremely useful for FD analysis on the interconnect network with arbitrary loads and power and ground planes. We discuss this in Chapter 5, "Frequency Domain Analysis." Z_{ii} is the input

impedance seen looking into port i when all other ports are open-circuited, and Z_{ij} is the transfer impedance from port j to i when all other ports are open-circuited.

3.4.2. Admittance Matrix [Y]

Similar to the Z-parameters, the admittance matrix [Y] is defined as follows:

Equation 3.35

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1N} \\ Y_{21} & \cdots & Y_{2N} \\ \vdots & & \ddots & \\ Y_{N1} & \cdots & Y_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix}$$

$$[I] = [Y][V]$$

Equation 3.36

$$Y_{ij} = \left. \frac{I_i}{V_j} \right|_{V_k=0 \text{ for } k \neq j}$$

Equation (3.36) depicts that Y_{ij} can be found by driving port j with the voltage V_j , short-circuiting all other ports, and measuring the short-circuit current at port i. Similar to the impedance parameters, Y_{ii} is the input admittance seen looking into port i when all other ports are short-circuited. In addition, Y_{ij} is the transfer admittance between ports j and i when all other ports are short-circuited; that is $V_k=0$ for $k \neq j$. Similar to Z parameters, Y parameters are also independent of reference impedance of the port.

3.4.3. The Scattering Matrix [S]

Scattering parameters or S-parameters describe the electrical behaviors of linear electrical networks when undergoing various steady state stimuli by electrical signals. The parameters are useful for electrical engineering, electronics engineering, and communication systems design. As frequency increases, the impedance and admittance matrix become somewhat of an abstraction because the parameters cannot show the reflected and the transmitted voltage and current waves separately. However, the scattering matrix shows the information about the reflected and the transmitted voltage and current waves, so it is convenient to analyze high-speed

interconnection networks for the reflection and the insertion loss of traces, the isolation and the coupling between traces, and so on.

The scattering matrix relates the voltage waves incident on the ports to those reflected from the ports. Scattering parameters can be measured with a vector network analyzer. The scattering matrix or [S] matrix is defined in relation to these incidents and reflected voltage waves as:

Equation 3.37

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & S_{22} & \cdots & S_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ S_{N1} & S_{N2} & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix}$$

$$[V^-] = [S][V^+]$$

Equation 3.38

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+ = 0 \text{ for } k \neq j}$$

Equation (3.38) means that S_{ij} is found by driving port j with an incident wave of voltage V_j^+ , and measuring the reflected wave amplitude, V_i^+ , coming out of port I when all other port except the jth port are matched. An important point to understand about S-parameters is that the reflection coefficient looking into port k is not equal to S_{kk} , unless all other ports are matched. Similarly, the insertion coefficient from j to i is different from S_{ij} , unless all other ports are matched. We discuss this in the following section.

Return loss (RL) at port j is defined (in dB) as follows:

Equation 3.39

$$RL = -20 \log |S_{jj}| \text{ [dB]}$$

If matched load ($S_{jj} = 0$), return loss is 0dB, that indicates there is no reflected power. By contrast, if total reflection is equal to 1 (open or short), then return loss is 0dB, which is a total reflection.

Insertion loss (IL) from port j to i is defined (in dB) as shown in the following equation:

Equation 3.40

$$IL = -20 \log |S_{ij}| \text{ [dB]}$$

If amplitude is reduced by 70.7%, then the insertion loss is 3dB.

Coupling and isolation [dB] between port i and j are defined as shown in the following equations:

Equation 3.41

$$\text{Isolation} = -20 \log |S_{ij}| \text{ [dB]}$$

Equation 3.42

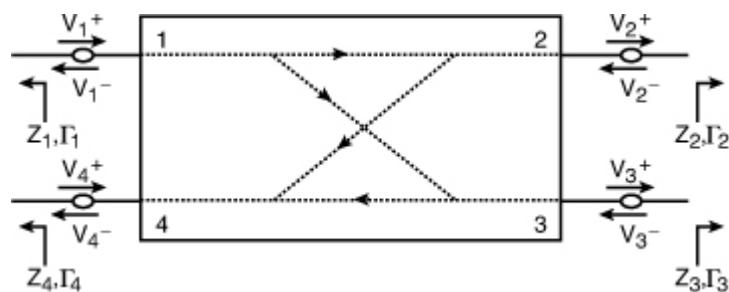
$$\text{Coupling} = -20 \log |S_{ij}| \text{ [dB]}$$

3.4.4. The Scattering Matrix [S] with Arbitrary Loads

The scattering parameters with arbitrary loads have been widely used to characterize a nonideal power/ground I/O signaling system for signal/power integrity cosimulation. Typically, power/ground plane impedance is much smaller than signal transmission line impedance. With Touchstone® 2.0b as a revision to the conventional Touchstone, network scattering parameters describe both power planes and signal lines with an arbitrary reference impedance [4].

We begin by considering a reciprocal ($S_{ij}=S_{ji}$) and matched ($S_{ii}=0$) 4-ports interconnect system with arbitrary load impedance, as shown in Figure 3.13, where V_n^+ is the amplitude of the wave incident on port n, and V_n^- is the amplitude of the wave reflected from port n.

Figure 3.13. An arbitrary four-port interconnection network



In the case of interconnect network, we can solve the independent equations of incident and reflect wave such as $[V_n^-] = [S][V_n^+]$ and $V_n^+ = \Gamma_n V_n^-$ (Γ_n : a load-sided reflection coefficient at the port n) and obtain the following:

Equation 3.43

$$S'_{11} = \frac{V_1^-}{V_1^+} = S_{21}S'_{21} + S_{31}S'_{31} + S_{41}S'_{41}$$

Equation 3.44

$$S'_{31} = \frac{V_1^-}{V_1^+} = \frac{(S_{31} + S_{41}S_{43}\Gamma_4)(1 - S_{42}^2\Gamma_2\Gamma_4) + \Gamma_2(S_{32} + S_{42}S_{43}\Gamma_4)(S_{21} + S_{41}S_{42}\Gamma_4)}{(1 - S_{43}^2\Gamma_3\Gamma_4)(1 - S_{42}^2\Gamma_2\Gamma_4) - (S_{32} + S_{42}S_{43}\Gamma_4)^2\Gamma_2\Gamma_3}$$

Equation 3.45

$$S'_{41} = \frac{V_1^-}{V_1^+} = \frac{(S_{41} + S_{31}S_{43}\Gamma_3)(1 - S_{32}^2\Gamma_2\Gamma_3) - \Gamma_2(S_{42} + S_{32}S_{43}\Gamma_3)(S_{21} + S_{31}S_{32}\Gamma_3)}{(1 - S_{43}^2\Gamma_3\Gamma_4)(1 - S_{32}^2\Gamma_2\Gamma_3) - (S_{42} + S_{32}S_{43}\Gamma_3)^2\Gamma_2\Gamma_4}$$

Equation 3.46

$$S'_{11} = \frac{V_1^-}{V_1^+} = S_{21}S'_{21} + S_{31}S'_{31} + S_{41}S'_{41}$$

where S'_{21} and S'_{31} are insertion coefficients and far-end coupling coefficients of port 2 and 3; when all other port are terminated with arbitrary load impedance. Equations (3.45) and (3.46) depict near-end coupling and return coefficients S'_{41} , S'_{11} respectively when all other ports except ports 1 and 4 are terminated with arbitrary load impedance. The preceding equations show that S-parameters (S'_{21} , S'_{31} , S'_{41} , and S'_{11}) with arbitrary load impedance are functions of reflection coefficients (Γ_2 , Γ_3 , and Γ_4) and well-matched S-parameters (S_{21} , S_{31} , S_{32} , S_{42} , S_{43} , and S_{41}).

Similarly, we can derive S-parameters with arbitrary load impedance, S'_{42} , S'_{33} , S'_{22} , S'_{33} , and S'_{32} , using the independent equations of incident and a reflected wave such as $[V_n^-] = [S][V_n^+]$ and $V_n^+ = \Gamma_n V_n^-$ (Γ_n : a load-sided reflection coefficient at the port n).

Equation 3.47

$$S'_{42} = \frac{V_4^-}{V_2^+} = \frac{S_{42} + S_{21}S_{41}\Gamma_1}{1 - S_{41}^2\Gamma_1\Gamma_4}$$

Equation 3.48

$$S'_{33} = \frac{V_3^-}{V_3^+} = S_{31}^2\Gamma_1 + (S_{43} + S_{21}S_{41}\Gamma_1) \frac{S_{42} + S_{21}S_{41}\Gamma_1}{1 - S_{41}^2\Gamma_1\Gamma_4} \Gamma_4$$

Equation 3.49

$$S'_{22} = \frac{V_2^-}{V_2^+} = S_{21}^2\Gamma_1 + \frac{(S_{42} + S_{21}S_{41}\Gamma_1)^2}{1 - S_{41}^2\Gamma_1\Gamma_4} \Gamma_4$$

Equation 3.50

$$S'_{33} = \frac{V_3^-}{V_3^+} = S_{31}^2\Gamma_1 + \frac{(S_{43} + S_{31}S_{41}\Gamma_1)^2}{1 - S_{41}^2\Gamma_1\Gamma_4} \Gamma_4$$

Equation 3.51

$$S'_{32} = \frac{V_3^-}{V_2^+} = S_{32} \left\{ 1 + \frac{\Gamma_1(S_{21} + S_{42}S_{41}\Gamma_4) + \Gamma_4(S_{42} + S_{21}S_{41}\Gamma_1)}{1 - S_{41}^2\Gamma_1\Gamma_4} \right\}$$

Also, as shown in equations from (3.43) to (3.51), we see that preceding equations show that S-parameters (S'_{42} , S'_{33} , S'_{22} , S'_{33} , and S'_{32}) with arbitrary load impedance are functions of reflection coefficients (Γ_1 , Γ_3 , and Γ_4) and well-matched S-parameters (S_{42} , S_{21} , S_{41} , S_{31} , S_{43} , and S_{32}).

3.4.5. Relation Between Scattering Matrix [S] and Y/Z/ABCD Matrix

[S] matrix can be determined from the [Z] or [Y]. Assuming that Z_0 (characteristic impedance) are identical and for convenience, and we set $Z_{0n}=1$, then the total voltage and current at the nth port are $V_n = V_n^+ + V_n^-$ and $I_n = I_n^+ - I_n^- = V_n^+ - V_n^-$.

From the definition of [Z] matrix

Equation 3.52

$$[V] = [Z][I] = [Z]([V^+] - [V^-]) = [V^+] + [V^-]$$

Equation 3.53

$$([Z] + [U])[V^-] = ([Z] - [U])[V^+]$$

Where, $[U]$: unit matrix:

$$\text{Using def of } [S] \text{ matrix } [V^-] = [S][V^+] \rightarrow [S] = [V^-][V^+]^{-1}$$

Consequently, we can derive

Equation 3.54

$$[S] = [V^-][V^+]^{-1} = ([Z] + [U])^{-1}([Z] - [U])$$

In addition, $[Z]$ is equal to $[Y]^{-1}$:

Equation 3.55

$$[S] = ([Y]^{-1} + [U])^{-1}([Y]^{-1} - [U])$$

For the relation between S-parameters and the Transmission Matrix (ABCD), the relation between the two-port S-parameters and Transmission (ABCD) Matrix is shown in equations (3.45) to (3.48). From the definition of the S-parameters and ABCD parameters

Equation 3.56

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}$$

Equation 3.57

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$

$$\begin{bmatrix} I_k^+ \\ I_k^- \end{bmatrix} = \frac{1}{Z_0} \begin{bmatrix} V_k^+ \\ V_k^- \end{bmatrix}, \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} I_1^+ - I_1^- \\ I_2^- - I_2^+ \end{bmatrix}$$

Here, using these relations, we can derive the equations as follows:

Equation 3.58

$$V_1 = AV_2^- + B \cdot \frac{V_2^-}{Z_0}$$

Equation 3.59

$$I_1 = CV_2^- + D \cdot \frac{V_2^-}{Z_0}$$

Equation (3.58) and (3.59) can be divided by V_1^+ :

Equation 3.60

$$S_{11} = \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+=0} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D}$$

Equation 3.61

$$S_{21} = \left. \frac{V_2^-}{V_1^+} \right|_{V_2^+=0} = \frac{2}{A + B/Z_0 + CZ_0 + D}$$

Similarly, equation (3.58) and (3.59) can be divided by V_2^+ , and then also derive the following equations:

Equation 3.62

$$S_{22} = \left. \frac{V_2^-}{V_2^+} \right|_{V_1^+=0} = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D}$$

Equation 3.63

$$S_{12} = \left. \frac{V_1^-}{V_2^+} \right|_{V_1^+=0} = \frac{2 \cdot (AD - BC)}{A + B/Z_0 + CZ_0 + D}$$

Table 3.3 summarizes conversions between N-port network parameters such as S-parameter, Z-parameter, and Y-parameter.

Table 3.3. Microwave Network Parameters Conversions

$[S] \leftrightarrow [Z], [Y]$	$[S] = \frac{1}{Z_0}([Z] + [U])^{-1}([Z] - [U])$	$[S] = \frac{1}{Z_0}([Y]^{-1} + [U])^{-1}([Y]^{-1} - [U])$
$[Z] \leftrightarrow [S], [Y]$	$[Z] = Z_0([U] + [S])$ $([U] - [S])^{-1}$	$[Z] = [Y]^{-1}$
$[Y] \leftrightarrow [Z], [S]$	$[Y] = \frac{1}{Z_0}([U] + [S])^{-1}([U] - [S])$	$[Y] = [Z]^{-1}$

$[U]$: unit matrix, Z^0 (characteristic impedance)

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3.5. LTI System

A linear system is a system for which the superposition property holds true with the system input/output responses. A Linear Time Invariant (LTI) system is a linear system with no parameters changing with time. Most passive electrical components we deal with are LTI. Electromagnetic systems represented by S, Y, or Z parameters are LTI systems; however, time domain simulation of EM LTI systems with nonlinear driver models often shows nonlinear behavior. Most nonlinear responses probed at the LTI system with nonlinear driver models evolve from numerical errors and inaccuracies. Real component measurements are inherently subject to external perturbations and noises. repeatable and accurate measurement technique is crucial in LTI component measurement.

3.5.1. Reciprocal Network

In frequency domain passive component transfer function measurement, such as the S, Y, or Z parameter measurement, if the network is made of isotropic and passive material, the measurement should be symmetric ($S_{ij} = S_{ji}$). Anisotropic components have asymmetric S, Y, or Z parameters. An example of anisotropic components is a component with ferrite material. Usually circulator isolators are made from ferrite. RF amplifiers are usually not reciprocal. Unless required for a particular purpose, most common high-speed channels do not usually use ferrite material. Measured or simulated S parameters of reciprocal channels could be slightly asymmetric because of measurement error or numerical errors; however, huge asymmetry means the data is invalid.

3.5.2. Parameter Conversion Singularity

Sometimes when S-parameters are converted to Y/Z parameters, if ports are shorted at a particular frequency, parameter conversion singularity occurs. A simple example is a series inductor with two ports. Conversion of an ideal two-port inductor S-parameters to the Y-parameters results in singularity at the DC. To avoid the singularity, a small loss can be added to each port to introduce interport loss. This numerically avoids singularity while keeping the component meaningful. Similar conversion singularity

occurs for an ideal capacitor with two ports when an S-parameters are converted to Z-parameters, because at the DC the S-parameter becomes an unitary matrix, $Z = Z_0([U] - [S])^{-1}([U] + [S])$.

3.5.3. Stability

A stable high-speed channel system is a system with Bounded Input Bounded Output (BIBO). Otherwise, the system is unstable [5]. Time domain simulation of a high-speed channel with EM-modeled components sometimes shows nonconverging behavior with bounded input. Frequently, the nonconverging output responses are ascribed to either nonpassive characteristics of EM components or numerical computation errors. To root-cause the nonconvergence, passivity of the EM modeled components should be checked. As long as the components are strictly passive and the simulator can accommodate a proper convolution algorithm without numerical computation difficulties, the entire system simulation must be stable.

3.5.4. Passivity

A passive system is a system unable to generate energy [5]. System interconnect components, such as interconnects and packages in digital and analog systems, are passive. Passive systems are guaranteed to be stable. Stable systems, however, are not necessarily passive. Passivity is of particular interest in electromagnetic systems because time domain stability of those systems is rather easily implemented by enforcing passivity on the systems.

S, Y, or Z parameters in a frequency domain are the most frequently used forms of transfer functions to represent passive system. Behavior of a system can be fully described by one of the three parameters. S-parameters can be transformed to Y or Z parameters without losing the system behavior information, and the reverse is true as well. Passivity can be easily checked by examining one of the parameters. However, handling S-parameters with certain assumptions constitutes an easier way to check passivity. Because all the energy coming out of the system should be at least equal or smaller than the energy going in, for N port system,

Equation 3.64

$$\sum_{i=1}^N |S_{ij}|^2 \leq 1, \text{ for all } j,$$

Equation 3.65

$$\text{and } \sum_{j=1}^N |S_{ij}|^2 \leq 1, \text{ for all } i,$$

if the system can be assumed to be reciprocal, which is true for isotropic material, the matrix can be assumed to be symmetric, and only one of (3.64) or (3.65) need to be sufficed.

Fixing the S-parameters for passivity is more complicated than checking the passivity with the S-parameters. Fixing the passivity with S-parameters leaves one less equation than unknown variables that it is hard to obtain systematic algorithm. On the other hand, using Y or Z parameters gives a more systematic approach when tested with the Sylvester test or Eigenvalue check. Y-parameters are used here to define a passivity fix algorithm, and also using Z-parameters follows the same algorithms.

A network with an admittance matrix is passive only if the following two conditions are met:

(1) $Y(s^*) = Y(s)^*$, where ' $*$ ' is the complex conjugate operator.

(2) $Y(s)$ is a positive real matrix. That is, $x^*(Y(s) + Y^t(s^*))x > 0$ for vector x .

To test positive realness of a matrix, the Sylvester test can be used. It is stated in the Sylvester-Principal minors test that a Hermitian matrix M is a positive definite only if each of its leading principle minors is strictly positive.

Equation 3.66

$$\text{Minor}(i) = \det \begin{pmatrix} Y_{1,1} & \cdots & Y_{1,i} \\ \vdots & & \vdots \\ Y_{i,1} & \cdots & Y_{i,i} \end{pmatrix}$$

So for k by k matrix, $\text{Minor}(1) \dots \text{Minor}(k)$ should be all positive for the matrix to be positive real.

At the same time, because ports are exchangeable, (3.67) can be represented as (3.68).

Equation 3.67

$$Y = \begin{bmatrix} Y_{1,1} & \cdots & Y_{1,k} \\ \vdots & Y_{i,j} & \vdots \\ Y_{k,1} & \cdots & Y_{k,k} \end{bmatrix}, k \text{ by } k \text{ admittance matrix}$$

Equation 3.68

$$Y = \begin{bmatrix} Y_{1,j} & \cdots & Y_{1,k} \\ \vdots & Y_{1,1} & \vdots \\ Y_{k,1} & \cdots & Y_{k,k} \end{bmatrix}$$

all diagonal elements $\text{real}(Y_{i,i})$ should be greater than zero, and off diagonal elements $\text{real}(Y_{i,j})_{i \neq j}$ should be in the particular range to make the whole matrix passive.

For 2×2 admittance matrix, if $Y_{21} = Y_{12}$, when diagonal elements are decided according to the restriction, Y_{21} has a particular range that makes the whole matrix positive real.

$$-\sqrt{\text{real}(Y_{11}) * \text{real}(Y_{22})} < \text{real}(Y_{21}) < \sqrt{\text{real}(Y_{11}) * \text{real}(Y_{22})}$$

Fixing passivity could cause a huge unwanted variation in transformed parameters, therefore the transformed parameters need to be checked with the original parameters.

3.5.5. Causality

In a causal system, at one instance of time the response is dependent on the input at the instance of time or at the past instance of time [5]. The cause of noncausality primarily evolves from the phase relationship of the dielectric constant. An electrical signal or signals must obey the relationship between the real and imaginary part of the network parameters to keep the causality so that it can contain physical meaning. It is known that the real and imaginary part of a system transfer function should be related by the Kramers-Kronig dispersion. The Hilbert transformation [7] can equally enforce the Kramers-Kronig dispersion [6]. In a passive high-speed channel, the speedy way to check for causality is to examine the S-parameter Smith Chart. If the data rotates clockwise, it has positive group delay; implying it to be causal. On the other hand, if the data rotates counterclockwise, this implies it is noncausal.

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Chapter 4. System Interconnects

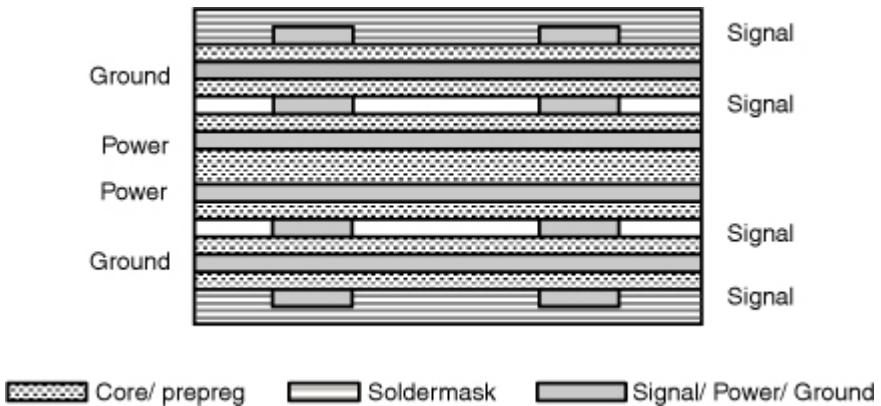
This chapter gives an overview of the Power Distribution Networks (PDN) and signal distribution networks for the digital electronic systems. The basic building blocks of the system are Printed Circuit Board (PCB), package, and on-chip networks. The PCB and package PDN have power/ground planes and various PDN capacitors. The on-chip PDN is composed of the power/ground grid and on-chip capacitors. This chapter describes different components of PDN and signal networks. The effects of different types of capacitors on self-impedance of the PDN are analyzed; signal routing schemes such as microstrip lines, striplines, and coupled lines are described in detail; analytical expressions for these routing schemes are provided; and interaction between power/ground and signal interconnect structures at various components is described.

4.1. PCB Technology

The printed circuit board provides electrical connections to signals coming from Integrated Circuits (ICs) and also provides power to different ICs. The PCB layers can be arranged in a multilayer stackup [1]. The total number of layers on the PCB is determined by the complexity of the PCB design, the signal routing requirements, total power/ground planes, and also the cost-constraints. Multilayer stackups are used for the PCB to route all the signals and their reference planes. PCB stackup influences signal integrity, power integrity, EMC, and their interactions [2].

There are many ways in which multiple layer stackups can be designed. An example of an eight layer stackup is shown in [Figure 4.1](#). There are conductor layers such as signal, power plane, and ground plane. Prepreg or core layers are between the conductor layers. Outermost signal layers are covered with the soldermask.

Figure 4.1. Eight layer PCB stackup



Prepreg is a fiberglass fabric that is pre-impregnated with resin. The core and prepreg may alternate for the inner layers, and prepreg is used on outer layers. The prepreg material is cured during the fabrication process. The core material is cured epoxy resin material that has copper foils bonded to both sides of the material. Depending on the complexity of the PCB, the stackup layer count is determined. For high-speed signals, a ground plane is placed in close proximity to a signal to maintain a good return path. The higher the number of layers, the higher is the manufacturing cost. In view of this, it may or may not be possible to have dedicated planes for particular power and ground domains. For more complex designs, the number of layers can be higher, such as 20 layers, or even more.

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4.2. Package Types

In the semiconductor manufacturing process, wafers are produced. The wafers are cut into numerous pieces carrying the same integrated circuit, each known as a die. The integrated circuit chip or the die is mounted on a package. The package provides electrical and mechanical connection to the chip and interfaces the chip with the PCB. Examples of packages include Dual In Line Package (DIP), Pin Grid Array (PGA), Small Outline Package (SOP), Quad Flat Pack (QFP), and Ball Grid Array (BGA), and so on [3, 4, 5]. DIP and PGA packages are insertion mount packages. For the PGA package arrays of pins are inserted to the PCB or to the socket, which is mounted on the PCB [6].

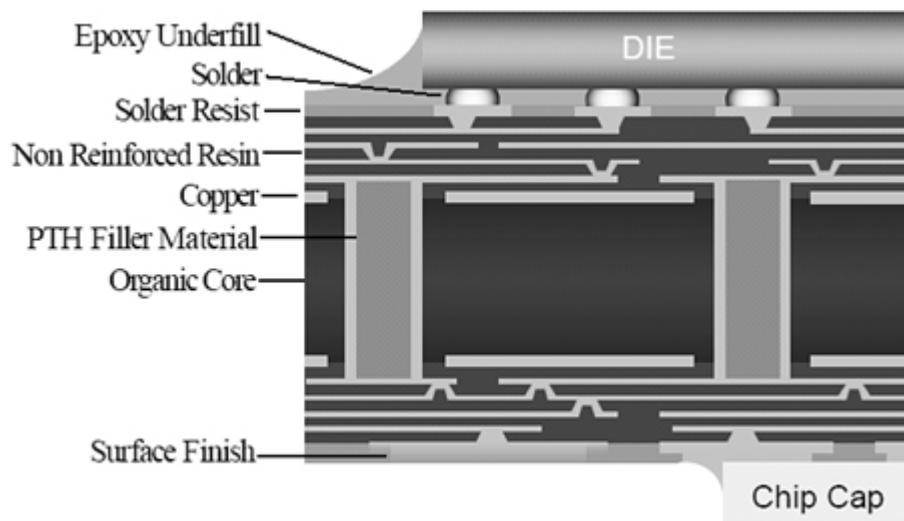
SOP, QFP, and BGA are surface mount packages. For the SOP package, the package pins are soldered to the PCB surface, and the PCB holes are not required [7]. The parasitic inductance for a SOP package is dependent on the geometry, such as the lead width, space, and pitch. For a BGA type package, there are solder balls for the connection to the PCB instead of the pins [8, 9]. These solder balls are arranged in an array fashion. The PCB has copper pads at the same geometry locations. The BGA package provides a lower inductance path from the package to the PCB, compared to the leaded package. The BGA packages are popular for high-density pin-outs. The J-STD-012 standard describes the Chip Scale Package (CSP) details. The CSP is a direct surface mountable package, and the package size does not exceed 1.2 times the size of the die [10]. The Land Grid Array (LGA) package has a similar grid array for connection to the board, as that for BGA, but it does not have solderballs.

In the wirebond package [4], there is a wire from the package to the bonding pad on the die. There is an inductance associated with this wire, which may degrade signal integrity for high-speed interfaces. BGA type packages are available in both wirebond and flip-chip technologies. In the flip-chip design, the die is flipped and the bumps are connected to the package top layer [11]. There are no wires in the flip-chip design. A flip-chip type of package does not require peripheral space for the wirebond. The die is connected to the package substrate at the bumps, without any need of trace connections. After the bump, the signals are routed in the package on different layers.

Packages also can be single layer or multilayer, depending on the complexity of the design and routing requirements. They have substrate technology similar to that for PCB, but the thicknesses and dielectric materials may vary. Figure 4.2 shows an example of a twelve-layer package cross-section. There is a core material at the center of the package and is surrounded by routing layers.

Figure 4.2. 12-layer package cross-section example

Sources: M. Manusharow, A. Hasan, T.W. Chao, and M. Guzy, “Dual die Pentium D package technology development,” Electronic Components and Technology Conference, 2006. Proceedings. 56th, pp 7. © [2006] IEEE.



Packages are sometimes attached to an additional connection mechanism, such as a socket, as shown in Figure 4.3. The figure shows an example of the LGA socket assembly. The components shown from the top are heat sink, thermal conductive film, package, LGA socket, PCB, and mechanical support for the PCB. Routing in the socket mostly introduces inductive coupling between vertical routings from the package to the board. The current loop in the socket interconnects becomes the significant source of crosstalks between signals and powers, especially in high-speed applications, such as CPU sockets [12, 13]. To minimize the crosstalks, a fine adjustment of pins according to their switching timing is required with the given physical specification of the socket. For example, location of one group of signals adjacent to the other groups of signals can be optimized by considering their active and inactive status and state of operation.

Figure 4.3. The schematic diagram of LGA socket assembly

Source: S. Yang, J. Wu, and M.G. Pecht, “Reliability Assessment of Land Grid Array Sockets Subjected to Mixed Flowing Gas Environment,” *Reliability, IEEE Transactions*, Vol.58, No.4, pp 634–640, Dec. 2009 © [2009].

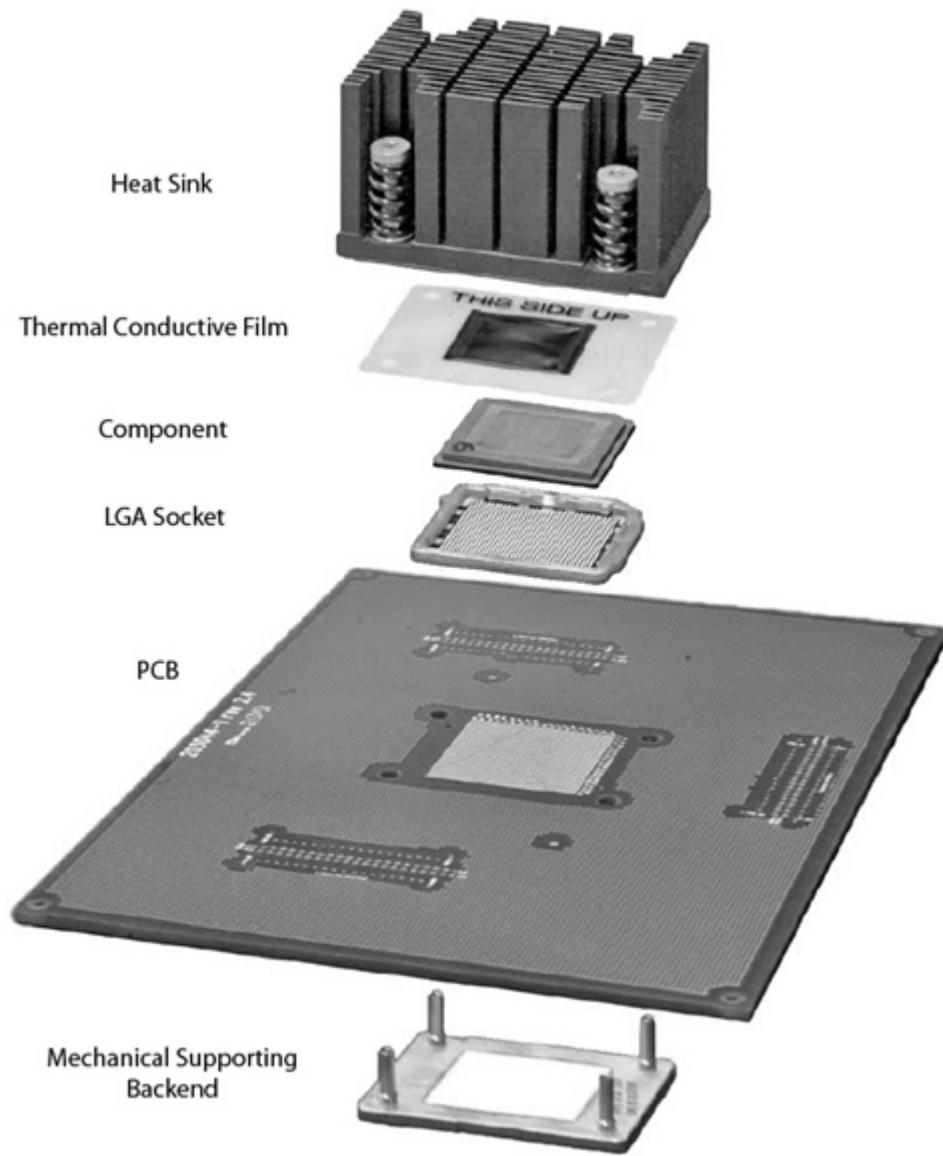
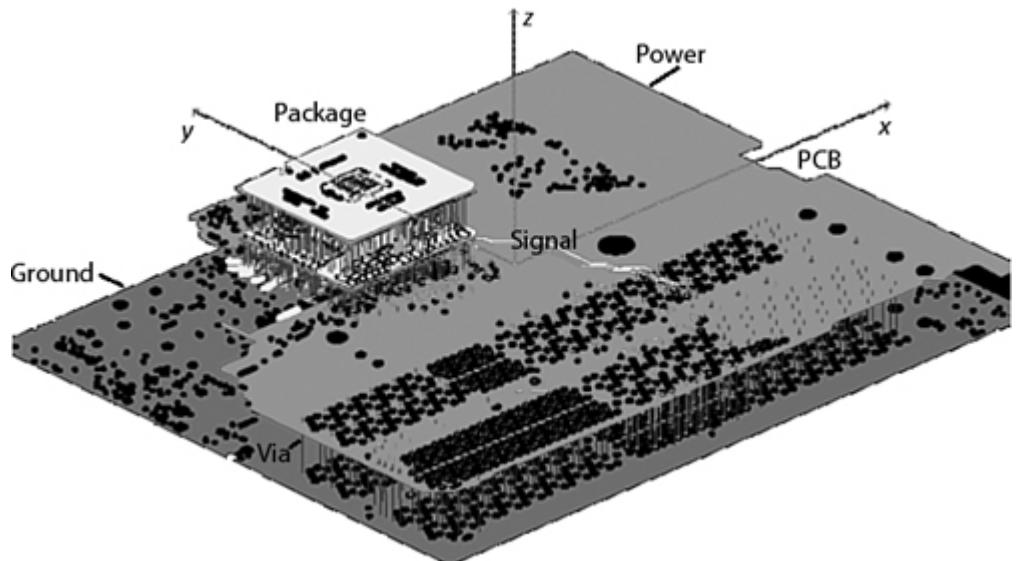


Figure 4.4 shows a modeling example of a package mounted on the PCB. It shows a multilayer package and a multilayer PCB. Power and ground planes on the PCB are demonstrated with a few signal lines. Modeling the package and the PCB together has an advantage over modeling them separately because modeling together includes electromagnetic interaction of the package and the PCB at the bottom layer of the package and the top layer of the PCB. Usually the impact of including the interaction is relatively small for a low-speed channel. However, the interaction can provide a fair amount of impact if the referencing change and domain division and union occur at the interface for high-speed channel. Also ever-increasing computational resources and speed grant enough reasons to consider macromodeling of the package and the PCB together as a viable choice.

Figure 4.4. PDN design example

Source: M. J. Choi, and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



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4.3. Power Distribution Network

This section describes the power distribution network for the PCB, package, and on-chip interconnect system.

4.3.1. PCB PDN

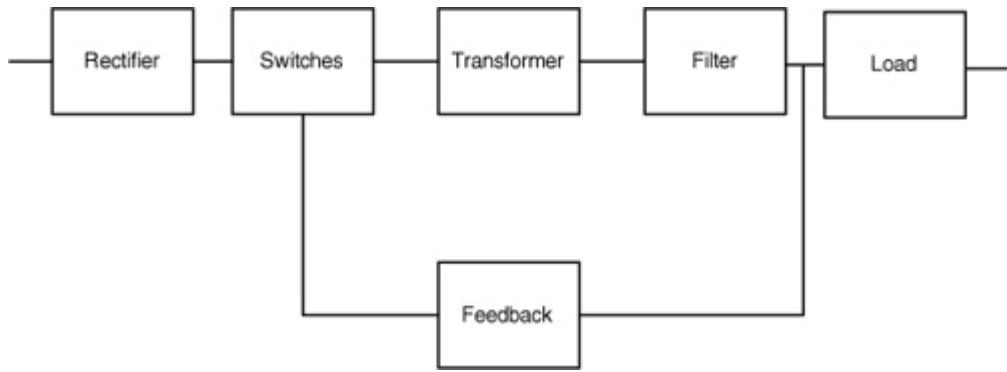
AC power from the outlet is converted to the DC supply by an AC/DC converter. This converter may be a standalone power supply or a part of the PCB. There may be a few DC output levels from the power supply. When the DC power arrives at the PCB, typically it is regulated through the Voltage Regulator (VR) or DC/DC converter. The function of the VR is to provide a steady supply at the desired DC level. The VR circuits can be mounted on the PCB or on a module known as Voltage Regulator Module (VRM). The DC power from the VR is routed through the PCB and fed to the chip. The routing may be on different layers of the PCB dependent on the stackup. When circuits start operating, the current flows through the PDN. It produces voltage fluctuations due to change in the current in the PDN. There are different decoupling capacitors on the PCB to smoothen out these fluctuations.

4.3.1.1. Power Supply

For a personal computer type of system, the AC/DC converter is typically standalone. It is also called a “sliver box” or a “power supply.” For a set-top box type of application, it may be integrated with the PCB. There are universal power supplies that can have 120V or 240V as input AC voltage. There are two types of power supplies: linear power supply and Switched Mode Power Supply (SMPS). A linear power supply uses a transformer to lower voltage and a rectifier to convert AC to DC, with pulsation occurring at line frequency (60Hz or 50Hz). In modern computer systems and set-top boxes, SMPS are common. [Figure 4.5](#) shows a block diagram of SMPS power supply.

Figure 4.5. Switched mode power supply

[\[View full size image\]](#)

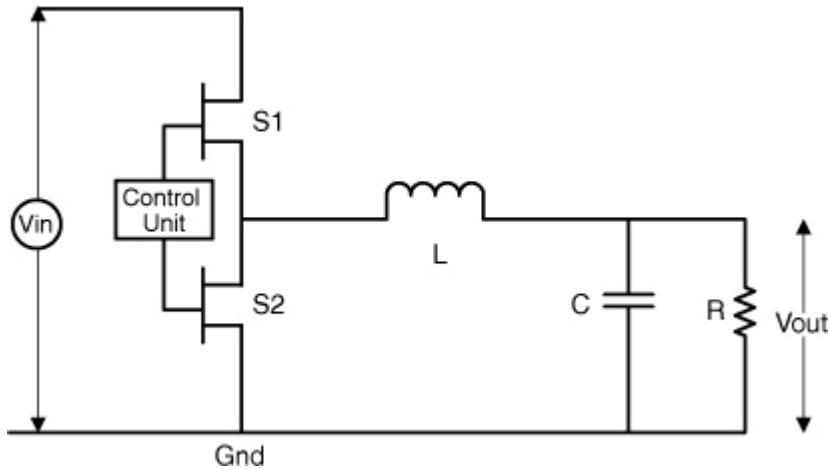


In SMPS, AC is first converted to DC and then the DC voltage in turn fed to switches with much higher frequency than the AC line frequency. In the next stage, it is fed to the step-down transformer. Then it is filtered out at the output stage. There is a feedback loop from the output of the filter to the control of the switches. SMPS has a better efficiency than that for linear power supply. SMPS produces ripple voltage at the switching frequency, which may cause ElectroMagnetic Interference (EMI) issues. The SMPS switching frequency is 100s of KHz or a few MHz range, whereas for the linear power supply the operating frequency range is the line frequency (around 60Hz). As a result, the isolation transformer or ripple filtering components are more bulky for linear power supply compared to those for SMPS.

4.3.1.2. DC/DC Converter

A typical computer system or set-top box system uses circuits that operate on different DC voltages. From the power supply a few DC voltages are available. Those DC voltages are converted to different levels using DC to DC converters. There are two types of DC/DC converters: linear and switched. The linear converter has lower efficiency, and the converted voltage is lower than the input voltage. The linear converter can be used for low power applications. The switched converter with FET switches has higher efficiency, and it can be used in step-up as well as step-down configurations. A step-down switched DC/DC converter is referred to as a buck converter and a step-up DC/DC converter as a boost converter. [Figure 4.6](#) shows a schematic diagram of the synchronous buck converter [14].

Figure 4.6. Buck converter



The incoming DC waveform V_{in} is chopped with the N-channel FET switches S_1 and S_2 . The current increases in the inductor L when the top FET S_1 is on and decreases when the top FET S_1 is off. When the primary switch S_1 is on, S_2 is off; and vice versa. When S_1 is off, there is a time gap before S_2 is on. This time gap is designed for avoiding a condition when both switches S_1 and S_2 are momentarily on. Because when both the transistor switches are on, there is a shoot-through current. After this time interval S_2 is on, and S_1 is off. The bottom FET S_2 is used to improve the efficiency of the converter. When S_2 is on, there is a R_{on} resistance for S_2 that is in mΩ range. The control unit circuitry synchronizes the switches. The ratio of V_{out} to V_{in} is equal to the duty cycle of the switches,

Equation 4.1

$$V_{out} = \frac{T_{on}}{T_p} V_{in}$$

where T_{on} is on the interval (when S_1 is on) and T_p is the total period.

VR tolerance is typically a low-frequency component. The VR tolerance is composed of DC error and VR ripple. VR ripple is due to switching frequency, passive filtering components, and load. It is typically in few hundreds of kHz range, but as the VR technology advances, it may get into the MHz range as well. There are various losses in the VR designs, which include the various components including the upper FET, lower FET, inductor, output capacitor, and PCB. Loss in the PCB needs to be extracted using an electromagnetic simulation tool.

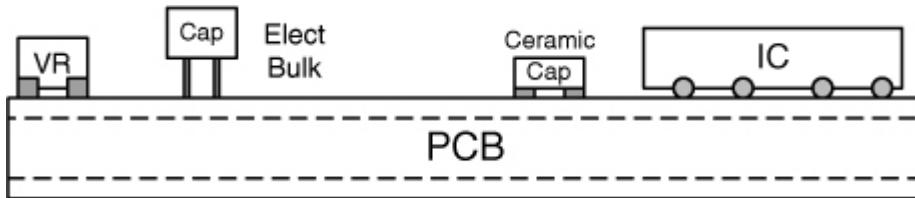
4.3.1.3. PCB Capacitors

PCB capacitors are useful for improving power integrity, signal integrity, and EMC. In PDN applications, the capacitors can be used to reduce the impedance of the PDN at the device. The target impedance of the PDN is

the ratio of allowed voltage tolerance and the switching current. The bulk capacitors are used for low frequency decoupling, whereas ceramic capacitors are used for medium frequency decoupling [15]. For signal integrity applications, the capacitors are used wherever there are reference transitions. For EMC applications, the capacitors are used to mitigate the PDN resonance effects, at different locations on the PCB.

Bulk capacitors are effective up to hundreds of kHz to a few MHz. Typical types of bulk capacitors are electrolytic or polymer. Figure 4.7 shows a cross-sectional view of a PCB with a VR, an electrolytic bulk cap, and a ceramic cap. It shows only the conceptual view; there are a few bulk and multiple ceramic capacitors placed on the PCB. Generally, low-frequency PCB PDN noise is mitigated by bulk decoupling capacitors.

Figure 4.7. PCB capacitors



EIA standard 198-1-F describes four different dielectric classes of ceramic capacitors [16]. The dielectric material is categorized into different classes. The capacitance variation to voltage and temperature is minimal for class 1 dielectrics and maximum for class 4 dielectrics. Class 1 capacitors are used where the tight tolerance is required. In class 1 dielectric, the common materials are C0G or NPO. Typically, the capacitors with this dielectric material have lower capacitance, in the range from pF to tens of nF, depending on the size. Capacitors with class 2 through 4 dielectric materials typically have higher tolerances. One popular example of class 2 dielectric material is X7R. The capacitors with this dielectric material have capacitance in the range of 100s of pF to 10s of uF, depending on the size. The class 2 and class 3 dielectric differ in temperature characteristics. Examples of class 3 dielectrics are Y5V and Z5U. Class 4 dielectric is limited to capacitors using barrier layer type construction.

Capacitor has parasitics such as inductance and resistance [17]. A simple one-stage model with these parasitics is shown in Figure 4.8. The impedance Z of the capacitor is given by

Equation 4.2

$$Z = R + \frac{1}{j\omega C} + j\omega L$$

where

R = Equivalent Series Resistance (ESR),

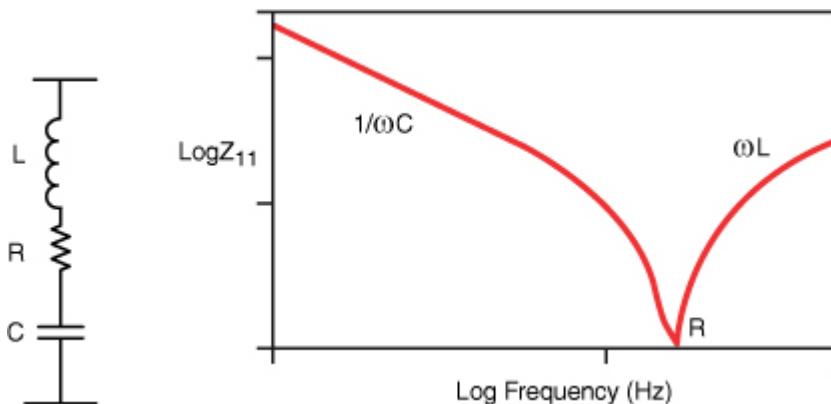
L = Equivalent Series Inductance (ESL),

C = is capacitance

$\omega = 2\pi f$

f = frequency

Figure 4.8. Simplified capacitor model



The impedance curve is capacitive in the beginning and then it becomes inductive. At the Series Resonance Frequency (SRF), the impedance is purely resistive. Above the SRF, the impedance response becomes inductive. The SRF is given by equation (4.3)

Equation 4.3

$$SRF = \frac{1}{2\pi\sqrt{LC}}$$

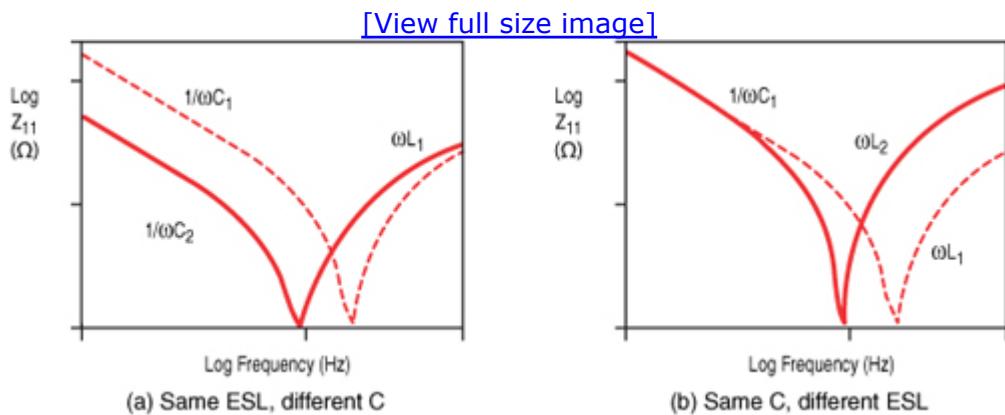
Both bulk capacitors and ceramic capacitors exhibit these ESR and ESL parasitics. [Figure 4.9](#) shows a simplified diagram of monolithic ceramic capacitor construction. Typically, monolithic ceramic capacitors have ceramic sheets and electrodes painted to the sheets with a paint having fine metal particles. The alternative electrodes exit from the opposite side and are terminated.

Figure 4.9. Ceramic capacitor construction



ESL of the ceramic capacitor is usually a function of the size of the capacitor [18]. There are different ceramic capacitor package sizes. Capacitor package examples in decreasing order of sizes are 2220, 1812, 1210, 1206, 0805, 0603, 0402, and 0201. In general, 0402 implies the length of 0.04 inch and width of 0.02 inch. Figure 4.10(a) shows the Z_{11} for different capacitors with the same ESL value. As the capacitance value increases from C_1 to C_2 , the impedance decreases. The high-frequency performance is limited by the ESL of the capacitor that is typically fixed for the size. For a given size, the highest capacitor value can be selected. The higher the size, the higher is the ESL of the capacitor, and this ESL is frequency-dependent. For the given length to width ratio, as the thickness increases, the ESL increases. For the same length, as the width increases, inductance decreases. As shown in Figure 4.10(b), as the inductance increases from L_1 to L_2 , the high-frequency impedance increases. ESR of the capacitor is the function of the geometry (plate length, width, thickness) and the resistivity of the material.

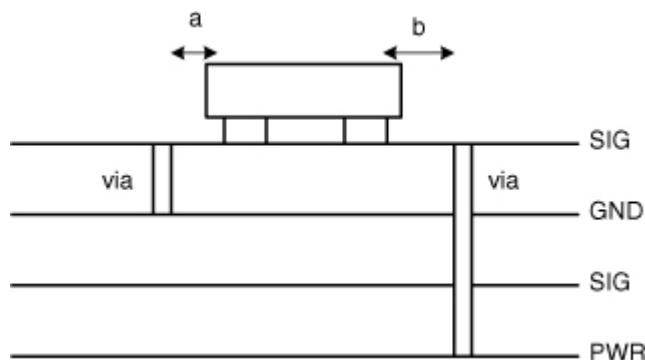
Figure 4.10. Z11 for the capacitor



The single stage model may not be adequate to capture the high-frequency effects, due to complexity in the capacitor structure. In that case a multistage model (higher order model) is used. While characterizing the capacitors, the mounting of the capacitor is also considered. Capacitor mounting plays an important role in overall loop inductance. If capacitor is not mounted properly, the inductance can increase. There are capacitor pads on the PCB where the capacitor is soldered. There are vias connected to these pads that go to power and ground planes. If the vias are connected by traces to the pads, there is increased inductance. Figure 4.11 shows that the pads and vias are separated by length a and b . This distance needs to be minimized to reduce the inductance. If the vias are within the pads or close to the pads, the inductance is reduced. The width of the trace connecting the vias to the pads needs to be such that it exhibits smaller inductance. Also, the total vertical distance of the power/ground via is an important consideration. If the capacitor height from the power/ground

planes is larger, there is increased inductance. Figure 4.11 shows an example where the ground via is on the adjacent layer and the power via is landing on the 4th layer. To reduce this inductance, the power/ground planes should be closer to the layer where the capacitor is mounted. Overall, to reduce the loop inductance, three things need to be considered: ESL of the capacitor, mounting pad and via placement, and capacitor height over the power/ground planes.

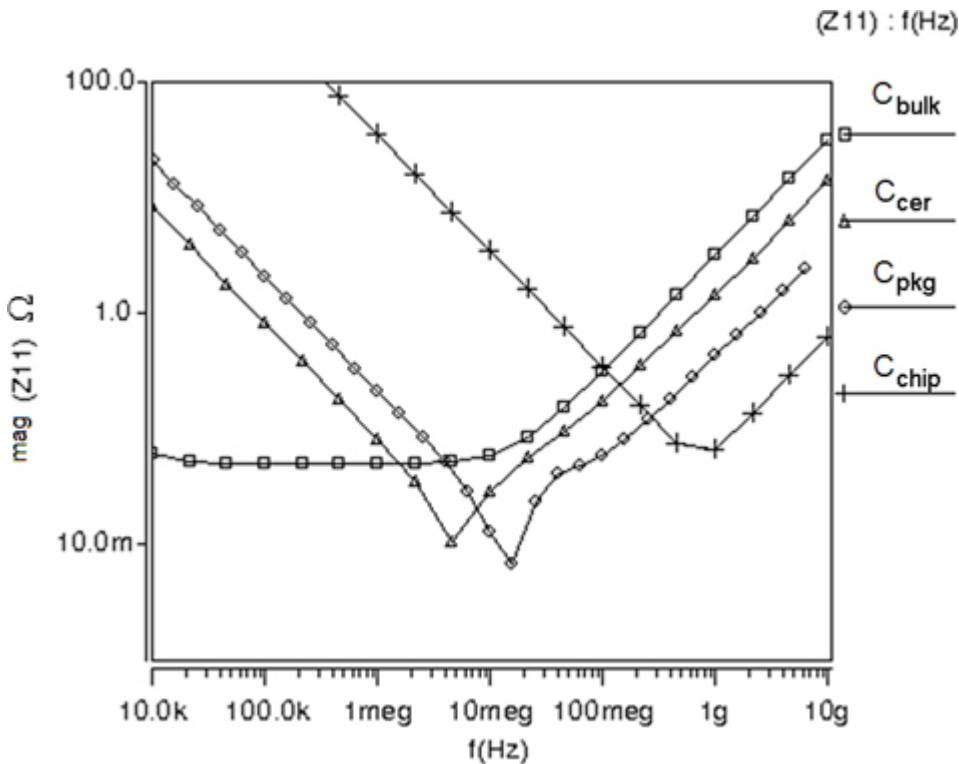
Figure 4.11. Capacitor mounting and associated inductances



In Figure 4.12, the impedance response of the typical bulk capacitor (C_{bulk}) and ceramic capacitor (C_{cer}) is shown, with a single stage RLC model. The package capacitor and chip capacitor response is also shown in the Figure 4.12 [18,19]. The package capacitor used is a reverse geometry capacitor. Its SRF is higher than that of the ceramic capacitor. The chip capacitor is assumed to have some routing inductance due to power grid.

Figure 4.12. Self-impedance of different capacitors

Source: V. Pandit, M.J. Choi, and W. H. Ryu, “Power Integrity for I/O Interfaces,” EPEP 2008, Tutorial. © [2008] IEEE.



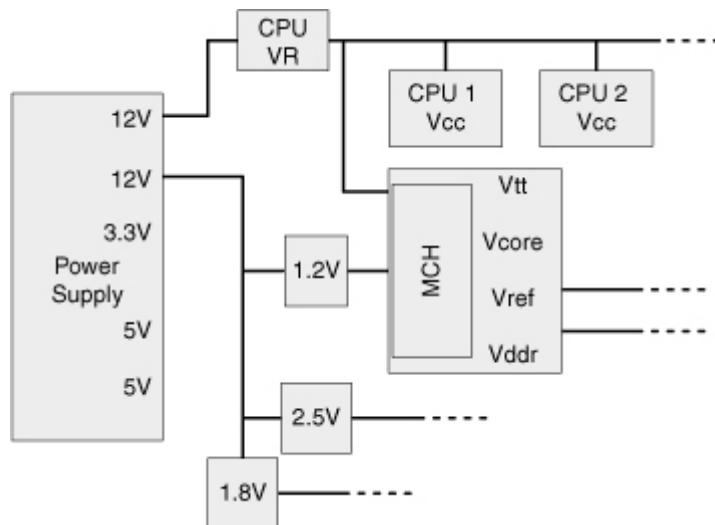
The power supply or VR cause conducted and radiated emissions. Typical switched VR frequency is hundreds of kHz, and newer VRs switch at MHz range frequencies. Various types of filtering techniques are used to alleviate the emissions. They include decoupling capacitors, LC filters, and also ferrites [20]. Inductors are used as power line choke and also in DC/DC converters. Inductors can have two types of cores on which the wires are wound: air core and ferrite core. Ferrites are ferrimagnetic materials that exhibit variable impedance for different frequencies. Ferrite beads can be used for attenuating a particular range of frequencies. Ferrites can be characterized as electrical entities with nonreciprocal network behavior. Ferrite materials are solid ceramics with crystal structures. They are typically stoichiometric mixtures of certain metal oxides. Ferrites have a higher relative permeability and a higher dielectric constant (>10 or so). They also have a specific resistivity greater than those of metals.

4.3.1.4. PCB Power/Ground Planes

The best way to keep the inductance and resistance low for PDN is to use solid and uninterrupted power and ground planes. However, in reality, PCB power distribution networks often have different domains and many layers of conductors because of different voltage levels, different frequencies of operation, and different signaling schemes. Figure 4.13 shows an example of a partial power delivery network diagram with different voltage levels and currents requirements. The power supply has different outputs such as 12v, 3.3v, and 5v. These outputs are converted into different DC levels with the VRMs. Different voltage and current requirements for the processors and chipset (MCH) are shown in the figure. Predicting the power and signal

integrity performance in multilayer, irregular shaped PDN with multiple power domains gets more difficult because it requires rigorous EM modeling and simulation to analyze the complex PDN. Recent advancement of planar circuit modeling algorithms and software made it possible to quickly assess the effectiveness of the power ground planes. To check the isolation of one domain from another domain, the impedance parameter is analyzed. When these domains merged together at one particular point in the channel, special attention should be given to the noise isolation of each domain. Especially, digital, RF, and analog domains should be effectively isolated to prevent one from interfering with another domain.

Figure 4.13. PCB power delivery example—shown partial diagram



If there are different power domains on the adjacent layers, there will be coupling between the two domains. To reduce this vertical coupling, the two different power planes on those adjacent layers are routed in such a way that they are not on top of each other. Each power plane pertaining to different power domain needs to have an adjacent ground plane. If a section of the power plane does not have a solid ground reference on the adjacent layer, enough ground shapes on the coplanar layer and adequate bypassing need to be considered.

The following section presents the different approaches for power/ground plane modeling. The self-impedance of the PDN is analyzed. One-dimensional (1-D), 2-D, and 3-D approaches are discussed. As the complexity of the power/ground plane increases, a more accurate model is required.

Simplified Plane Model

Figure 4.14 shows a power/ground plane with length a , width b , and thickness h . Due to the thickness of the dielectric, there is capacitance associated with the plane. The capacitance and inductance per unit length is

given by

Equation 4.4

$$C = \frac{\epsilon b}{h}$$

Equation 4.5

$$L = \frac{\mu h}{b}$$

where

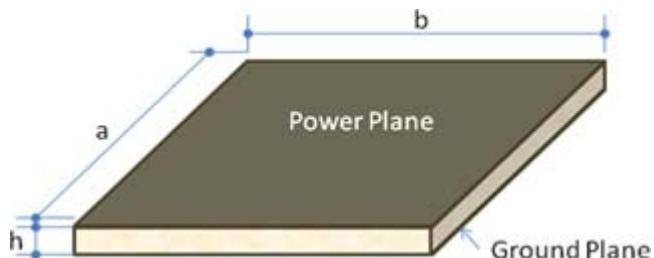
ϵ = Permittivity (F/m)

μ = Permeability (H/m)

a, b = length and width of the plane (m)

h = thickness of the dielectric (m)

Figure 4.14. Power and ground plane cavity



As the thickness of the dielectric increases, the capacitance decreases. Tighter h serves two purposes. One, it gives higher capacitance, which is effective at higher frequencies. Secondly, it reduces the self-inductance resulting in lower loop inductance. The overall plane capacitance is relatively low in value compared with separate component decoupling capacitors. The plane capacitance has lower parasitic inductance hence it becomes effective at high frequencies. Looking from the die, this capacitance may be overshadowed by the on-chip decoupling capacitor that typically may be much more than this plane capacitance.

A simple plane RLC model can be approximated as series R and L with shunt C. This particular model is of the first order and is similar to the transmission line model described in [Chapter 3, "Electromagnetic Effects."](#)

Equation 4.6

$$Z_i = Z_0 \frac{Z_L + jZ_0 \tan \gamma l}{Z_0 + jZ_L \tan \gamma l}$$

where

Z_i = Input impedance

Z_L = Load impedance

Z_0 = Characteristics impedance

γ = Propagation constant

l = Length

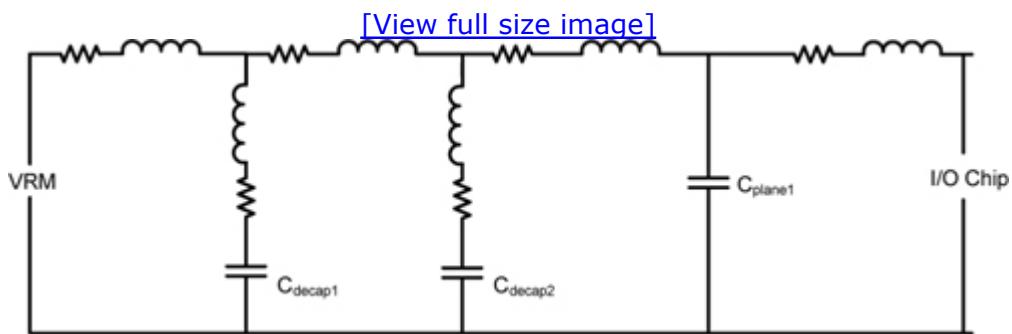
For the open boundary case, Z_L is near infinity.

Equation 4.7

$Z_{in_open} = -jZ_0 \cot \gamma l$ as plane is open boundary.

Figure 4.15 shows the simplified 1D model for the PCB PDN including VR, decoupling capacitors, and the power/ground plane [21]. As shown in the figure, there is a bulk cap C_{decap1} , ceramic cap C_{decap2} , and plane cap C_{plane1} . There are plane inductances and resistances between different sections of the plane.

Figure 4.15. Simplified PCB PDN model



This 1D PCB PDN model is an equivalent model and shows the path from the VR to the I/O chip. More accurate 2D models can be created for PCB power/ground planes, as shown in reference [22]. In this type of model, the R, L, and C are distributed in x and y directions. The associated capacitance and the velocity of the wave can be given by the following formulae:

Equation 4.8

$$C_a = \frac{\epsilon}{h}$$

Equation 4.9

$$v_r = \frac{C_{light}}{\sqrt{\epsilon_r}}$$

where

C_a = Capacitance per unit area (F/m^2)

V_r = Velocity of the wave traveling between power/ground plane (m/s)

C_{light} = Velocity of wave in free space (m/s)

ϵ_r = Dielectric constant of the material between power/ground planes

As shown in equation (3.27), for a lossless transmission line, the velocity of propagation is $1/(LC)^{1/2}$ where L is inductance/unit length and C is capacitance/unit length. A similar concept can be applied to the power/ground plane with C_a is capacitance per unit area and L_a is inductance per unit area

Equation 4.10

$$L_a = \frac{1}{C_a v_r^2}$$

where L_a is also known as spreading inductance (Henries/square.)

The spreading inductance is inductance on the plane from the IC chip to the decoupling capacitor, which provides high-frequency currents to the chip [22]. The spreading inductance is proportional to the separation of the planes. Depending on the position on the planes, this inductance changes. Spreading inductance and plane capacitance play important role at high frequencies.

EM Based Model

The PCB has power and ground planes that can be characterized using electromagnetic cavity formulations. The plane capacitance and spreading inductance effects are already taken into effect in the electromagnetic (EM) based models. [Figure 4.14](#) shows the power and ground plane similar to cavity form. Its dimension is length a and width b . The height of the dielectric material between power and ground plane is h .

The resonance due to this cavity is a function of dielectric constant, plane thickness, and the size of the plane [23].

Equation 4.11

$$(f_r)_{mn} = \frac{1}{2\pi\sqrt{\mu_0\epsilon_0\epsilon_r}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 + \left(\frac{p\pi}{h}\right)^2}$$

where

f_r = Resonance frequency (Hz)

μ_0 = Permeability of the air (A/m)

ϵ_0 = Permittivity of the air (F/m)

ϵ_r = Dielectric constant of the material between power and ground

m , n , and p = Mode numbers

a , b , and h = Length, width and height of the plane (m)

If $h/b \ll 1$, the vertical resonance can be neglected, therefore, the last term $\left(\frac{p\pi}{h}\right)$ can be neglected.

The Z_{ij} , the transfer impedance, is discussed in reference [24, 25, 26]. It is assumed that at higher frequencies, $h >$ skin depth, and Z_{ij} is given by

Equation 4.12

$$Z_{ii} = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{j\omega\mu h \chi_{mn}^2}{ab \left(k_{xm}^2 + k_{yn}^2 - k^2 \right)} \cdot \cos^2(k_{yn} T_{yi}) \cos^2(k_{xm} T_{xi}) \sin^2\left(k_{yn} \frac{L_{yi}}{2}\right) \sin^2\left(k_{xm} \frac{L_{xi}}{2}\right)$$

where

m, n = indices of cavity modes in x and y direction

$$\chi_{mn}^2 = 1 \text{ for } m = 0 \text{ and } n = 0$$

$$= 2 \text{ for } m = 0 \text{ or } n = 0$$

$$= 4 \text{ for } m \neq 0 \text{ and } n \neq 0$$

T_{xi}, T_{yi} = Coordinates of the center of the i^{th} port in x and y direction

L_{xi}, L_{yi} = Dimensions of i^{th} port in x and y direction (<wavelength)

$$K_{xm} = \frac{m\pi}{a}$$

$$K_{yn} = \frac{n\pi}{b}$$

$$k = \omega\sqrt{\mu\epsilon}$$

The previous equation assumes that the structure has no losses. In reality, with the PCB power ground planes, there are various losses due to dielectric and conductor. The quality factor for a microwave resonator is

Equation 4.13

$$\frac{1}{Q} \approx \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_r}$$

where Q = Overall quality factor, Q_c is the quality factor for conduction loss, Q_d is the quality factor for dielectric loss, and Q_r is the quality factor for radiation loss.

Equation 4.14

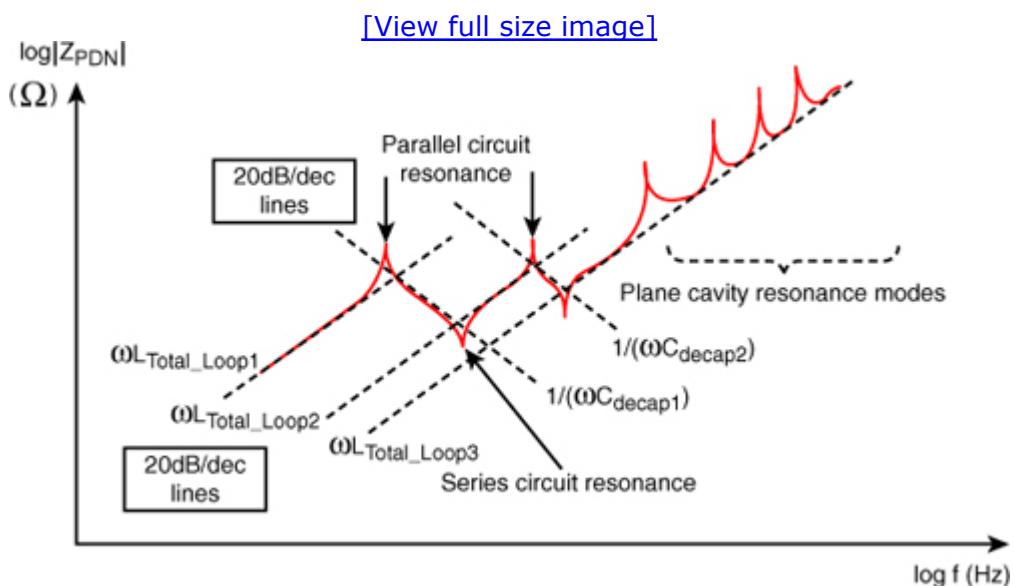
$$Q_c \approx h\sqrt{\pi h \mu \sigma}$$

Equation 4.15

$$Q_d = \frac{1}{\tan \delta}$$

The typical cavity resonance is shown in Figure 4.16. It shows the response of the PCB PDN that also has decoupling capacitors. The first inductive curve $\omega L_{\text{Total_Loop}1}$ is from the VR loop inductance. Then there is a low frequency capacitor $C_{\text{decap}1}$ (bulk capacitor) that produces a capacitive curve. The second inductive curve $\omega L_{\text{Total_Loop}2}$ is from the ESL of the bulk cap and mounting inductance. After that, the ceramic capacitor $C_{\text{decap}2}$ produces a capacitive curve. As frequency increases, the plane cavity resonance is visible.

Figure 4.16. Self-impedance plot for PCB PDN



4.3.1.5. Impact of Vias

In multilayer PCBs or packages, complex power and ground planes are often placed in different layers. To maintain the electrical connection, they should be connected with vias. Here, via is a pad with a plated hole for electrical connections between conductor traces on different layers. PTH, which is basically a Plated Through Hole from top to bottom on the board, is a type of a via used as an electrical interconnection between conductive patterns on top and bottom layers. There are two other types of vias: buried and blind. A buried via connects two or more inner layers and cannot be seen from the top or bottom of the board, whereas a blind via starts from top or bottom but does not completely pass through the board. To illustrate the effect of vias on the impedance, a simple experiment is shown. Figures 4.17 and 4.18 show a hypothetical rectangular power ground plane pair with vias. The top plane is the power plane and the bottom plane is the ground plane. Ground vias are explicitly shown. The power-ground plane of Figure 4.17 is modified by the inclusion of three ground vias at its center.

Figure 4.17. A power-ground plane pair

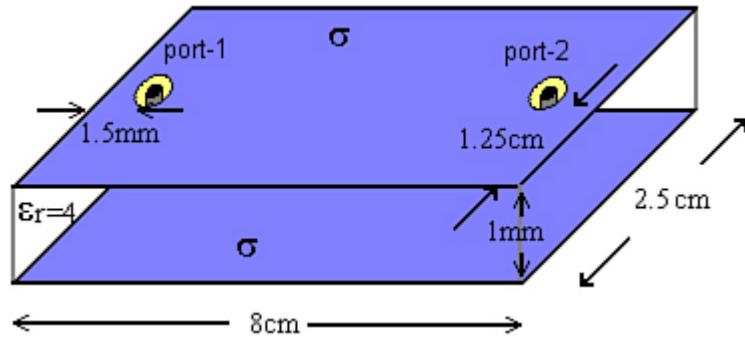
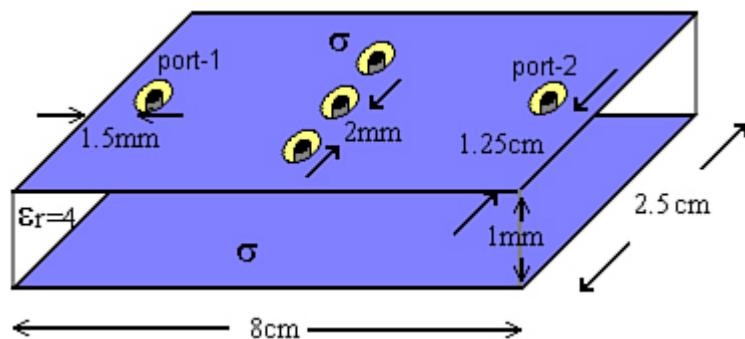


Figure 4.18. Modified power-ground plane pair



As shown in Figures 4.19 and 4.20, the impedance profile is changed quite significantly due to vias. The Y axis shows impedance amplitude in Ohms. More vias push away resonances to higher frequencies, for structures shown in Figures 4.17 and 4.18. The general rule of thumb for better signal referencing is to place power or ground vias within one-quarter wavelength of the maximum frequency of interest for nearby signal vias.

Figure 4.19. Z11 profile for structure in Figure 4.17

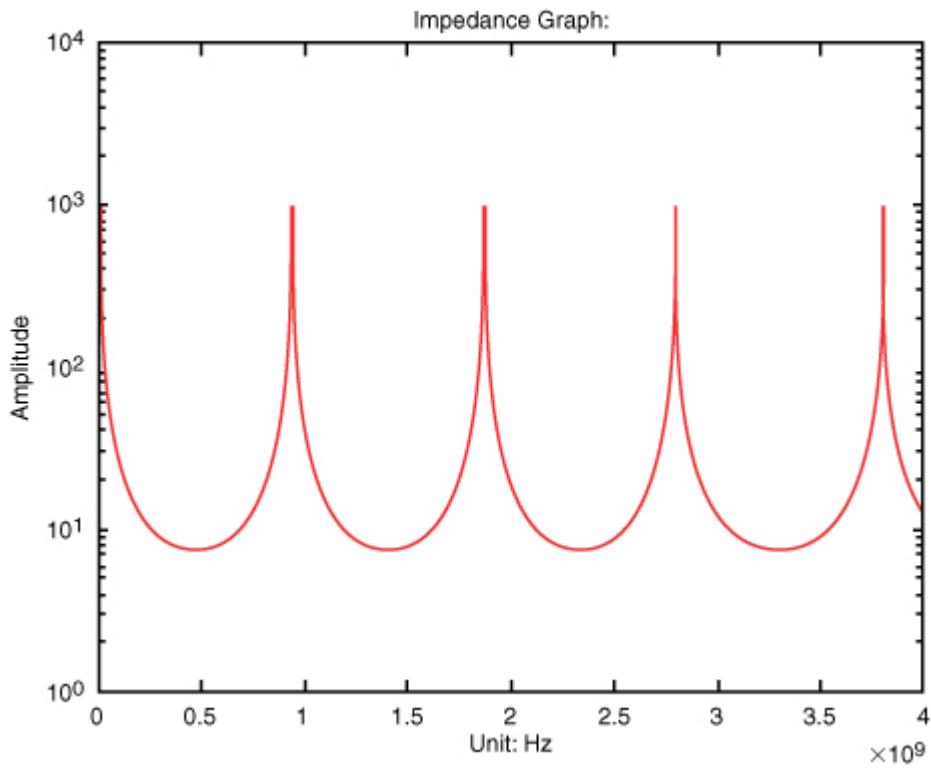


Figure 4.20. Z11 profile for structure in Figure 4.18

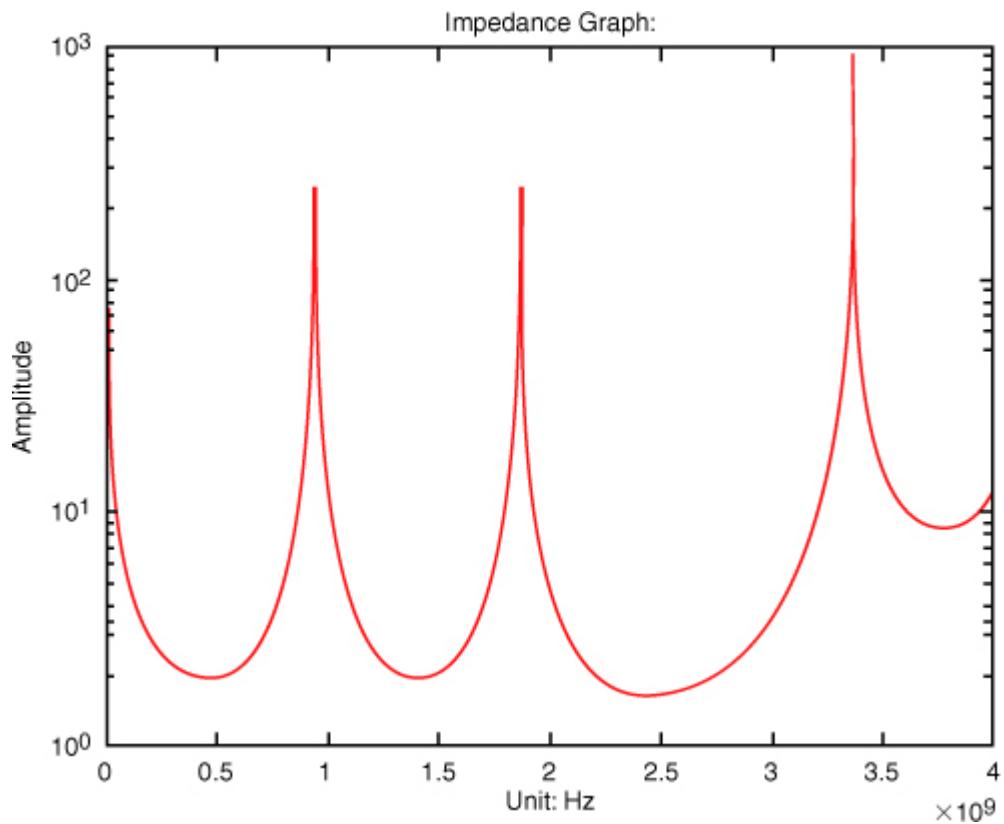


Figure 4.21 depicts hypothetical 8cm by 4cm power-ground plane with 2mm gap in the center of the power plane. The presence of the gap still provides capacitive coupling between the two different power domains. The transfer

impedance Z_{21} response in Figure 4.22 now shows different cavity resonances, compared with the case in Figure 4.19 for self-impedance, because of the gap in the top plane.

Figure 4.21. Power-ground plane pair with a 2-mm gap at the top (power) plane

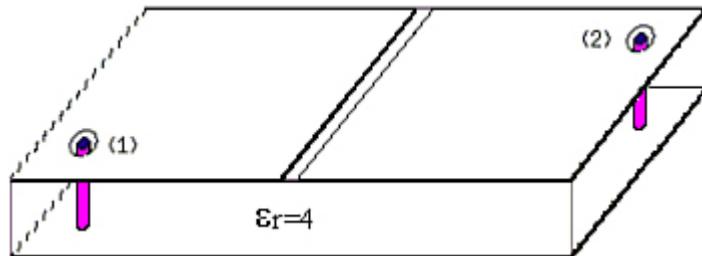
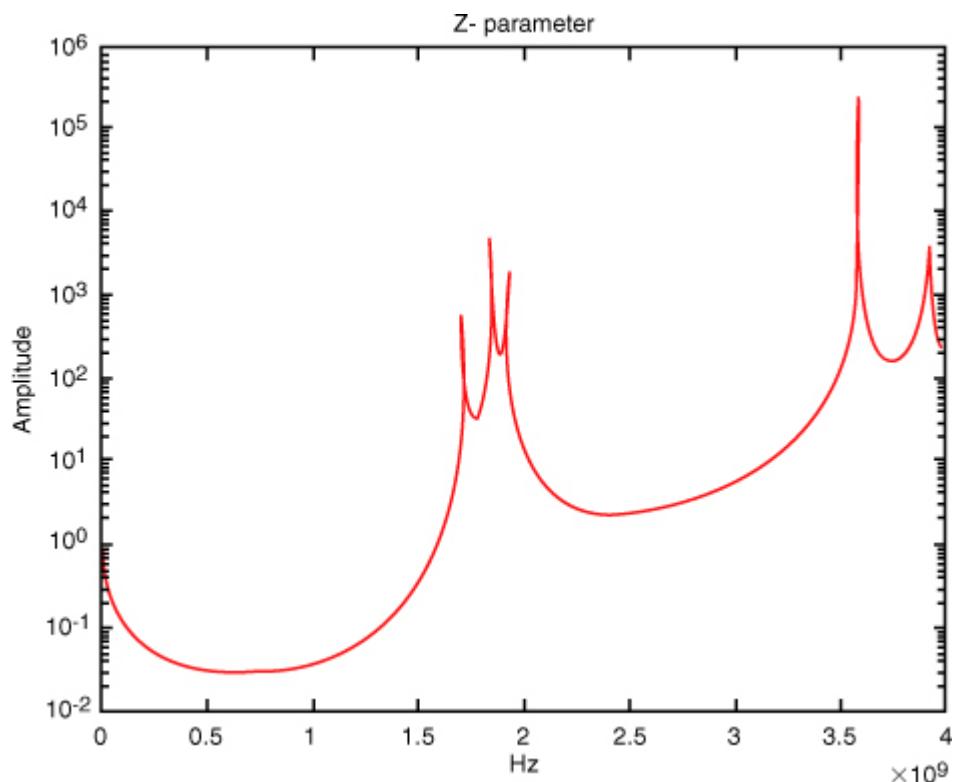


Figure 4.22. Magnitude of Z_{21} for the structure in Figure 4.21



Lots of vias scattered across PCBs act as walls that reflects back the radial waves generated in between power and ground planes. Therefore the vias reduce effective dimension of power-ground plane cavity and as a result they push away plane resonances. Use of vias for interconnection purpose impacts not only the interconnection itself but also the electromagnetic response of the power ground plane including the resonance profile. Especially the different via impedance from the connected interconnection impedances make the via an unintentional noise source. The unintended noise should be at least approximately quantified, to optimize the system,

especially in the system with high speed and tight margin budget.

4.3.1.6. Stitching Domains Together

Connecting complex power or ground planes of the same net placed in different layers together to maintain physical connectivity is often called *stitching*, which is also used to describe certain specific via usages. [Figure 4.23](#) depicts hypothetical power distribution network geometry by adding more layers and more vias for stitching purpose. Four planes are now present, each dimension 8cm by 4cm. A 2-mm gap is present all the way across the top power plane, as shown in the structure of [Figure 4.23](#). A total of 58 vias are present for stitching purpose. [Figure 4.24](#) depicts the cross-section of the four-layer board structure with via stitching conductors in the different layers. It is important to stitch the same signal reference planes in the different layers because poorly stitched reference planes tend to have long return paths and higher inductance.

Figure 4.23. Top view of a four-layer board with a 2-mm gap at the top power plane. Forty-eight vias are at the left-half plane and 10 vias are at the right-half plane. Circles denote power vias. Squares denote ground vias.

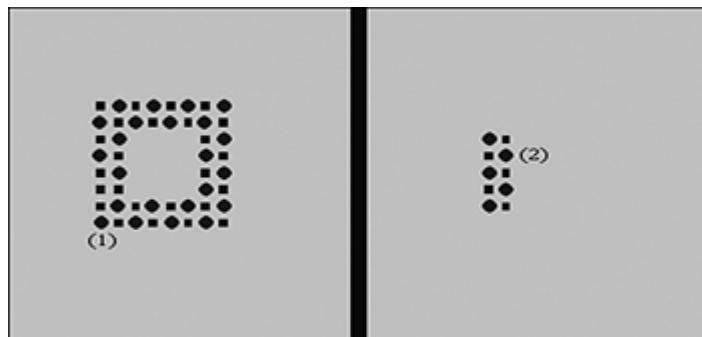


Figure 4.24. Cross-sectional view of the four-layer board, illustrating the connection of the ground (left) and power (right) vias



Physically, vias connect the two different layers, and electrical connection is also maintained at low frequency through a physical connection. However the high-frequency behavior will be highly dependent on the physical geometry, their connection mechanisms, and connection locations. In general more stitching vias are preferred for better electrical connection across wide bandwidth. On the other hand, the number of vias that can be

placed is limited by the power delivery routing and signal routing requirements. Therefore, it is important to place a limited number of stitching vias at optimal places to achieve electrically well-connected domains over wide bandwidth. Proper stitching is verified by examining the frequency domain impedance profile and time domain pulse response, and the optimization rule can be very system-specific. Though, in general, more stitching vias are recommended for the inside of the quarter wavelength region around the electrical hot spots that draw more switching currents. [Chapter 7](#), "Signal/Power Integrity Interactions," discusses in detail performance impact of the stitching vias.

4.3.2. Package Power Distribution Network

PCB PDN brings the power from the VR to the package, and the package in turns provides to the chip. For a wirebond type of package, the wirebond may be inductive at higher frequencies and may cause signal distortion. For the power delivery network, there are several wirebonds for power and ground. The net equivalent inductance is lower than that for a signal because these several wirebonds are in parallel. However, there is a much larger current in the power delivery network. That may put constraints on wirebond usage at higher speeds. The flip-chip package offers lower inductance than the wirebond package.

For a typical package, it is important to determine the required die-side connection points and board-side connection points. The flip-chip package interfaces the die with die bumps, and the wirebond package interfaces the die with bonding pads. The die bump map, or bumpout scheme, is designed in accordance with the signal integrity and power delivery performance. There are bumps required for the power, ground, and signal nets. For determining the required power/ground bumpout, both AC and DC analysis is performed. The on-chip PDN model is created with ports at bumps and the circuit locations. The IR drop is calculated in the power grid. Depending on the required IR drop, the number of power/ground bumps and bump-map is determined.

The board-side connection points of the package are package pins or package balls. There are signal, power, and ground package balls for the BGA type of package. The ball-out scheme is also determined based on the signal integrity and power delivery considerations. It includes signal pin-to-reference pin ratio (typically signal-to-ground ratio). For high-speed channels, lower signal-to-ground ratio (high number of ground pins) is required. The power distribution network for the package and that for the PCB is routed accordingly. The IR drop for the package is calculated from the package pin to the die pad on the package.

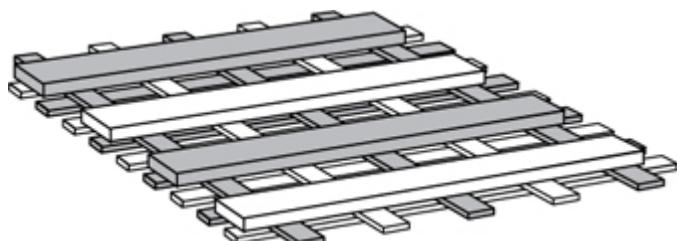
With advances in the package technology, signal and power nets can be routed in a multilayer structure. Similar to the PCB power/ground planes, the package power/ground planes also have plane capacitance and plane

inductance. The smaller vias are possible in the package, leading to the lower inductance. Package capacitors can be mounted between power and ground planes with very thin dielectric. The package capacitor can be mounted with the blind via; the opening side is connected to the capacitor terminals; and the other side is connected internally to power/ground planes. Typically, package capacitors are chosen with lower ESL values. There are different types of capacitors, such as reverse geometry or multiterminal capacitors, which exhibit lower ESL values. In the reverse geometry type of capacitor, the terminations are done at the longer size of the case, instead of the smaller size on a regular capacitor device. The regular size 0805 becomes 0508 for a reverse geometry capacitor. These are more expensive than the regular geometry capacitors and can be used for PCB as well as package applications. The advantage of these types of capacitors is that they can have multiple vias connecting to the package planes, thus further reducing the via inductance. A typical impedance plot for a reverse geometry package capacitor is shown in [Figure 4.12](#). It shows a much higher SFR frequency than that for the ceramic PCB capacitor. The package PDN capacitors are placed as close as the die-bumps or die-pads to minimize the routing inductance. The package PDN capacitor can be effective at much higher frequencies than that for the PCB PDN capacitor.

4.3.3. On-Chip Power Network

On-die PDN, or on-chip PDN, consists of power and ground interconnect and on-chip decoupling. There are different types of power and ground interconnect networks: routed network, mesh network, and grid-structured network [27]. The routed network is used for the ICs with lower complexity, where circuit blocks are connected to the routed power trunks. In the mesh network, there are power and ground lines in upper layer over the entire circuit block. The grid structured network provides robustness and is used in high-complexity ICs. Depending on the process technology power and ground, grid is routed over several interconnect metal layers. The typical nomenclature of these layers are M1, M2, and so on, where M1 is the first metal interconnect. The bumps or bonding pads are on the top metal interconnect layer. The power nodes of the I/O circuits are connected to the top bumps/bonding pads through the power grid. A typical power grid representation is shown in [Figure 4.25](#).

Figure 4.25. Typical power grid [27]



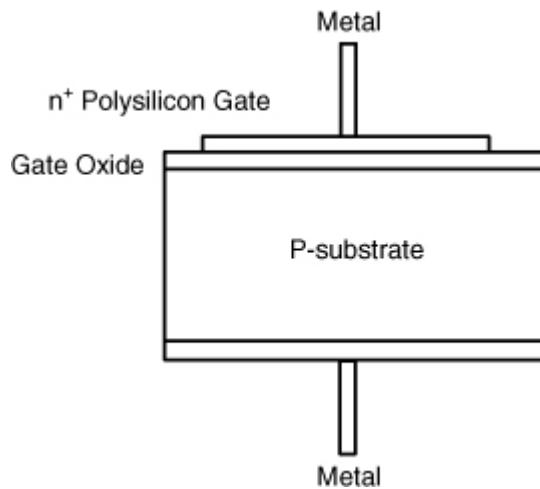
This grid is for power and ground domains. Metal layer width, thickness, and via dimensions are dependent on the silicon process. The power grid and the ground grid are represented by alternate metal lines, in [Figure 4.25](#). The higher the layer number, the wider and thicker is the grid dimension. Lower metal layers may have thinner grid interconnects. The power grid is orthogonal in alternative layers and connected with multiple vias (not shown in the figure). Power grid is an interconnect structure that connects the circuits to the package, and the parasitics elements such as grid resistance and grid capacitance need to be taken into account in the system level analysis.

On-chip capacitors have two major categories: intentional capacitors and unintentional capacitors. The intentionally designed capacitors are also known as extrinsic capacitors, and the unintentional capacitors are known as intrinsic capacitors.

4.3.3.1. Intentional Capacitors

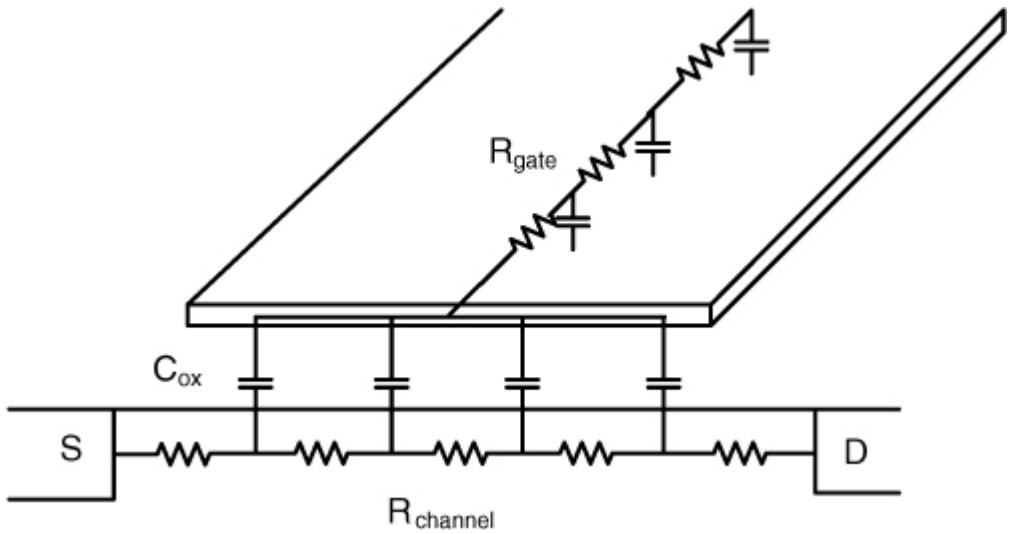
There are different types of intentional capacitors that include Polysilicon-Insulator-Polysilicon (PIP) type, Metal Oxide Semiconductor (MOS) type, and Metal Insulator Metal type, as described in reference [\[27\]](#). MOS transistor type capacitors are shown in [Figure 4.26](#).

Figure 4.26. MOS capacitor



The NMOS capacitor is shown in [Figure 4.26](#), which has a p-substrate. For the PMOS capacitor, there is an n-substrate, and for the CMOS capacitor, there are p-wells and n-wells. For the NMOS capacitor, there are different regions of operation based on the applied voltage. The parasitic resistance for a typical MOS capacitor is composed of channel resistance R_{CH} and gate resistance R_G [\[28, 29, and 30\]](#). The total resistance, R_{eq} , is shown in equation 4.16.

Figure 4.27. Channel resistance and gate resistance [30]



Equation 4.16

$$R_{eq} = R_G + R_{CH} = R_{Poly} \left(\alpha \frac{W}{L} + \beta \right) + \frac{1}{\gamma \mu_n C_{OX} (\eta V_{ter} + V_{gs} - V_T)} \frac{L}{W}$$

Equation 4.17

$$\approx \frac{1}{12} \left(R_{Poly} \left(\frac{W}{L} \right) + \frac{1}{\mu_n C_{OX} (\eta V_{ter} + V_{gs} - V_T)} \frac{L}{W} \right)$$

where

$\alpha = 1/3$ when gate terminal is brought out from one side

$\alpha = 1/12$ when gate terminal is brought out from both sides

β = External gate resistance

$\gamma = 12$, transistor is operating in the linear region ($V_{DS}=0$)

μ_n = Electron mobility:

R_{poly} = POLY sheet resistance

L = Gate length

C_{ox} = Gate oxide capacitance

W = Gate width

V_{gs} = Gate Voltage

V_T = Threshold voltage

V_{ter} = thermal voltage = kT/q ,

η = Semiconductor technology dependent constant

k = Boltzman constant, T = lattice temperature and q = charge

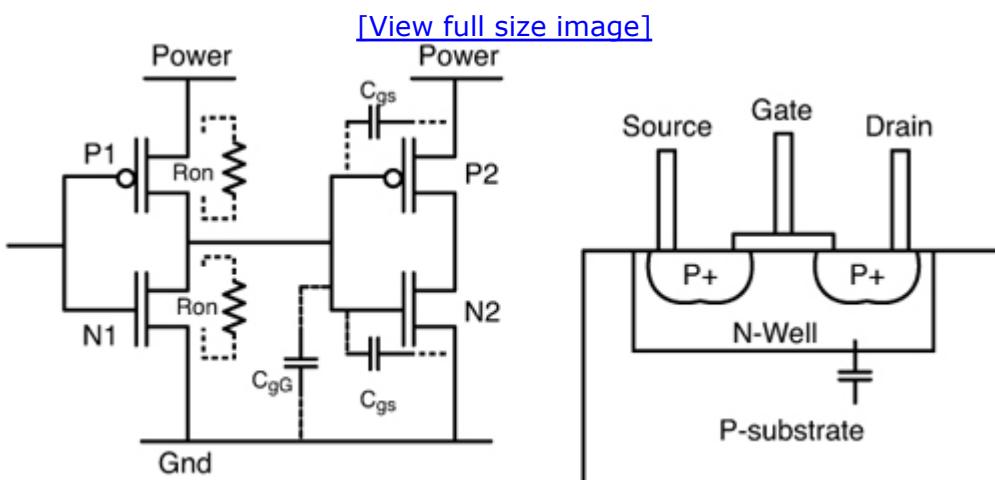
For the system-level PDN analysis, the resistance element analysis becomes an important factor.

4.3.3.2. Unintentional Capacitors

There are different types of unintentional capacitors in the silicon. [Figure 4.28](#) shows a conceptual representation of unintentional capacitors in an inverter chain [31]. P is a PMOS type transistor and N is NMOS type transistor:

- A. When P1 is on and N2 is off, there is a capacitor in that path. P1 has on resistance of R_{on} and N2 has gate to source capacitance of C_{gs} .
- B. Similarly, when P2 is off, and N1 is on, there is a capacitor C_{gs} in that path as well.
- C. Another type of capacitor is C_{gG} Cgate-global ground for N2.
- D. Also, when there is a P-channel transistor, there is a capacitance from N-well to the P-substrate.

Figure 4.28. Unintentional capacitors [31]



Typically, for the core, due to large circuit blocks, the amount of unintentional capacitance is high. Also there is series resistance associated with the unintentional capacitors that needs to be accounted for. For the I/O interface, the number of circuit blocks is much lower compared to that for the core. Hence, the amount of unintentional capacitance is much lower compared to that for the core.

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4.4. Signal Distribution Network

This section describes signal routing schemes such as microstrip lines, striplines, and coupled lines and analytical expressions for these routing schemes.

4.4.1. PCB/ Package Physical Signal Routing

As described in [Chapter 1](#), “Introduction,” there are two types of PCB signaling schemes: single-ended signaling and differential signaling. High-speed differential signaling typically uses coupled lines. PCB signals are mostly routed with microstrip and stripline because of their relatively cheap and easy structure to manufacture. Coplanar, quasi-coplanar, slotline, and other structures are used less frequently than microstrip and striplines in PCBs. However, special types of signal lines are being used increasingly to overcome geometrical routing issues and cost-saving issues.

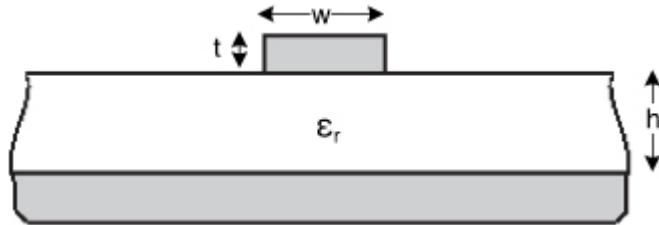
In typical digital systems up to a few GHz, the electromagnetic wave propagates in the transverse electric and magnetic (TEM) or quasi-TEM mode, which means that the electric and magnetic fields are both perpendicular to the direction of propagation along the guiding line. In this chapter we show the three common types of interconnection line structures that support TEM or quasi-TEM: stripline, co-planar waveguide, and microstrip line. In the case of a microstrip line, a TEM transmission line model approximation, as shown in [Chapter 3](#), “Electromagnetic Effects,” is found to be reasonably satisfactory when the width of the signal trace is much greater than the substrate thickness and the substrate has a high dielectric constant. And the general transmission line equations as described in the [Chapter 3](#) can be applied to uniform transmission lines—for example, stripline and co-planar waveguide.

4.4.1.1. Microstrip Line

As shown in [Figure 4.29](#), microstrip line is a popular planar guiding structure for most of the general circuitries on PCBs. Photolithography and photo-etching make manufacturing relatively easy and low cost. However, microstrip lines do not support a pure TEM wave because fields are not contained in the homogenous dielectric region, but some of the fields are in

the air and some of them are in the dielectric. This wave is called a quasi-TEM wave. Some of the fields in the air region may radiate. Nevertheless, comparatively low cost, compact size, and ease of integration with active devices make microstrip lines a good choice for integrated circuits and microwave circuits.

Figure 4.29. Microstrip line cross-section



A few parameters are easily controllable considering manufacturing processes. Characteristic impedance and effective permittivity [32] are controllable by changing the geometry of the line. Where h is the thickness of the dielectric, ϵ_r is dielectric constant, W is trace width, and t is trace thickness. The reference here can be power or ground. The formulas assume that the reference is continuous in nature.

Equation 4.18

$$Z_0 = \frac{\eta}{2\pi\sqrt{\epsilon_{re}}} \ln\left(\frac{8h}{W} + 0.25\frac{W}{h}\right) \text{ for } \frac{W}{h} \leq 1$$

Equation 4.19

$$Z_0 = \frac{\eta}{\sqrt{\epsilon_{re}}} \left\{ \frac{W}{h} + 1.393 + 0.667 \ln\left(\frac{W}{h} + 1.444\right) \right\}^{-1} \text{ for } \frac{W}{h} \geq 1$$

Here, η is 120π ohm.

The effective dielectric constant (ϵ_{re}) is a function of relative permittivity (ϵ_r), trace width (W), thickness (T), and dielectric height (h), as follows [46];

Equation 4.20

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F(W/h) - \frac{\epsilon_r - 1}{4.6} \frac{T/h}{\sqrt{W/h}}$$

Equation 4.21

$$F\left(\frac{W}{h}\right) = \left(1 + 12 \frac{h}{W}\right)^{-1/2} + 0.04 \left(1 - \frac{W}{h}\right)^2 \text{ for } \frac{W}{h} \leq 1$$

$$F\left(\frac{W}{h}\right) = \left(1 + 12 \frac{h}{W}\right)^{-1/2} \text{ for } \frac{W}{h} \geq 1$$

The effect of frequency f on an effective dielectric constant, ϵ_{re} , has been described accurately by the dispersion models given by references [47, 48, 49, 50]. The accurate expression of a relative dielectric constant with dispersion, $\epsilon_{re}(f)$ is as follows:

Equation 4.22

$$\epsilon_{re}(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{re}}{1 + \left(\frac{f}{F_{50}}\right)^m}$$

where

$$F_{50} = \frac{C \cdot \tan^{-1} \left(\epsilon_r \sqrt{\frac{\epsilon_{re} - 1}{\epsilon_r - \epsilon_{re}}} \right)}{0.75 + \left\{ 0.75 - \left(0.332 \sqrt{\frac{1}{\epsilon_r^{1.73}}} \right) \right\} \cdot \frac{W}{h}} \cdot \frac{1}{2h\pi\sqrt{\epsilon_r - \epsilon_{re}}}$$

$C = 3 \times 10^8$ m/s, and

$$m = 1 + \frac{1}{1 + \sqrt{\frac{W}{h}}} + 0.32 \cdot \left(\frac{1}{1 + \sqrt{\frac{W}{h}}} \right)^3$$

With given dielectric material, desired characteristic impedance, the ratio of line width to height can be determined from following equations:

Equation 4.23

$$\frac{W}{h} = \frac{8 \exp(A)}{\exp(2A) - 2} \text{ for } A > 1.52$$

Equation 4.24

$$\frac{W}{h} = \frac{2}{\pi} \left\{ B - 1 - \ln(2B-1) + \frac{\varepsilon_r - 1}{2\varepsilon_r} \left[\ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_r} \right] \right\} \text{ for } A < 1.52$$

where

Equation 4.25

$$A = \frac{Z_0}{60} \left\{ \frac{\varepsilon_r + 1}{2} \right\}^{1/2} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1} \left\{ 0.23 + \frac{0.11}{\varepsilon_r} \right\}$$

Equation 4.26

$$B = \frac{60\pi^2}{Z_0 \sqrt{\varepsilon_r}}$$

Signal integrity control on microstrip line in a PCB is practically limited to matching impedance control by controlling line width and height as usually other materials are already determined by the product design specifications. However, other features, such as referencing, termination, and power integrity control, all affect signal integrity to some degree.

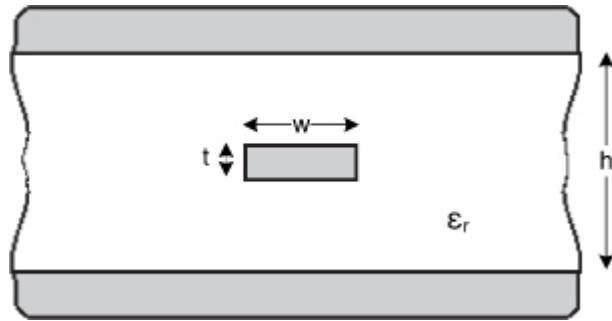
4.4.1.2. stripline

For a stripline situation as shown in [Figure 4.30](#), the signal layer is sandwiched between two reference planes. The stripline can be symmetric or asymmetric. In a symmetric stripline, the reference planes are equidistant from the signal layer, whereas in a case of asymmetric stripline, the distance of one reference plane from the signal may be different than the other. Similar to microstrip line design, geometry parameters are usually the only controllable parameters to control impedance [33, 34, 35] of the line.

Equation 4.27

$$Z_0 \sqrt{\varepsilon_r} = 30\pi \frac{K(k)}{K(k')}$$

Figure 4.30. Strip line cross-section



where

Equation 4.28

$$k = \operatorname{sech} \left(\frac{\pi W}{2b} \right), \text{ and } k' = \sqrt{1 - k^2}$$

Here, k is the complete elliptic integral of the first kind. Approximate expression for $K(k)/K(k')$ is given as

Equation 4.29

$$\frac{K(k)}{K(k')} = \frac{K(k)}{K'(k)} = \frac{1}{\pi} \ln \left(2 \frac{1 + \sqrt{k}}{1 - \sqrt{k}} \right) \text{ for } 0.5 \leq k^2 \leq 1$$

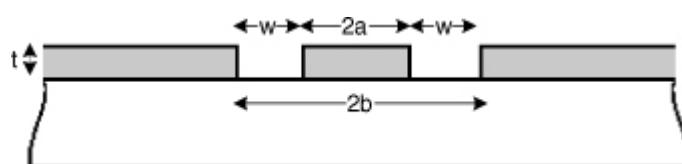
Equation 4.30

$$\frac{K(k)}{K(k')} = \frac{K(k)}{K'(k)} = \frac{\pi}{\ln \left(2 \frac{1 + \sqrt{k'}}{1 - \sqrt{k'}} \right)} \text{ for } 0 \leq k^2 \leq 0.5$$

4.4.1.3. Co-Planar Waveguide

A co-planar waveguide, as shown in [Figure 4.31](#), are often used in packages with one conductor layer. Silicon-based integrated circuits and microelctromechanical systems (MEMS) devices often use co-planar waveguides.

Figure 4.31. Co-planar waveguide



The characteristic impedance is given by [36]:

Equation 4.31

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K(k')}{K(k)}$$

Equation 4.32

$$\epsilon_{re} = 1 + \frac{\epsilon_r - 1}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}$$

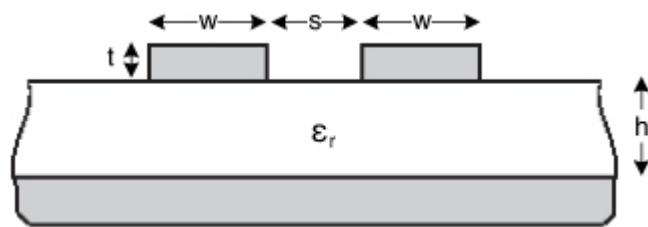
$$k = a/b, \text{ and, } k' = \sqrt{1 - k^2}$$

$$k = \sinh\left(\frac{\pi a}{2h}\right) / \sinh\left(\frac{\pi b}{2h}\right), \text{ and, } k'_1 = \sqrt{1 - k_1^2}$$

4.4.1.4. Coupled Lines

For a differential I/O interface, two coupled lines are used from transmitter to receiver. The coupling between two lines is more dependent on the distance between the two lines than other geometrical parameters. For a situation where the reference plane is far away, the coupling between the two lines is stronger than that between the signal line and reference ground. Figure 4.32 shows a coupled microstrip line [37].

Figure 4.32. Coupled microstrip line



The following equations for the quasistatic solutions provide accuracy within 1% in the range of parameters $0.1 \leq u \leq 10$, $0.1 \leq g \leq 10$, and $1 \leq \epsilon_r \leq 18$. The even mode effective dielectric constant is given by

Equation 4.33

$$\epsilon_{ree}(0) = 0.5(\epsilon_r + 1) + 0.5(\epsilon_r - 1) \cdot (1 + 10/v)^{-a_e(v) \cdot b_e(\epsilon_r)}$$

where

Equation 4.34

$$v = u \left(20 + g^2 \right) / \left(10 + g^2 \right) + g \cdot \exp(-g)$$

Equation 4.35

$$a_e(v) = 1 + \ln \left(\left(v^4 + (v/52)^2 \right) / \left(v^4 + 0.432 \right) \right) / 49 + \ln \left(1 + (v/18.1)^3 \right) / 18.7$$

Equation 4.36

$$b_e(\varepsilon_r) = 0.564 \left((\varepsilon_r - 0.9) / (\varepsilon_r + 3) \right)^{0.053}$$

$$u = W/h, \quad g = S/h$$

The quasistatic odd-mode effective dielectric constant for an infinitesimally thin conductor is similarly given by

Equation 4.37

$$\varepsilon_{re0}(0) = [0.5(\varepsilon_r + 1) + a_0(u, \varepsilon_r) - \varepsilon_{re}(0)] \cdot \exp(-c_0 g^{d_0}) + \varepsilon_{re}(0)$$

where

Equation 4.38

$$a_0(u, \varepsilon_r) = 0.7287 (\varepsilon_{re}(0) - 0.5(\varepsilon_r + 1)) \cdot (1 - \exp(-0.179u))$$

Equation 4.39

$$b_0(\varepsilon_r) = 0.747 \varepsilon_r / (0.15 + \varepsilon_r)$$

Equation 4.40

$$c_0 = b_0(\varepsilon_r) - (b_0(\varepsilon_r) - 0.207) \cdot \exp(-0.414u)$$

Equation 4.41

$$d_0 = 0.593 + 0.694 \cdot \exp(-0.562u)$$

Here, $\varepsilon_{re}(0)$ denotes the effective dielectric constant of a single microstrip with width W .

The quasistatic even-mode characteristic impedance of coupled microstrip lines is given by

Equation 4.42

$$Z_{0e}(0) = Z_0 \sqrt{\frac{\varepsilon_{re}(0)}{\varepsilon_{ree}(0)}} \frac{1}{\left(1 - (Z_0(0)/377)(\varepsilon_{re}(0))^{0.5} Q_4\right)}$$

where

Equation 4.43

$$Q_1 = 0.8695 \cdot u^{0.194}$$

Equation 4.44

$$Q_2 = 1 + 0.7519g + 0.189 \cdot g^{2.31}$$

Equation 4.45

$$Q_3 = 0.1975 + \left(16.6 + (8.4/g)^6\right)^{-0.387} + \ln\left(g^{10}/\left(1 + (g/3.4)^{10}\right)\right)/241$$

Equation 4.46

$$Q_4 = (2Q_1/Q_2) \cdot \left(\exp(-g) \cdot u^{Q_3} + (2 - \exp(-g)) \cdot u^{-Q_3}\right)^{-1}$$

The quasistatic odd-mode characteristic impedance of coupled microstrip lines is given by

Equation 4.47

$$Z_{0o}(0) = Z_0 \sqrt{\frac{\varepsilon_{re}(0)}{\varepsilon_{reo}(0)}} \frac{1}{\left(1 - (Z_0(0)/377)(\varepsilon_{re}(0))^{0.5} Q_{10}\right)}$$

where

Equation 4.48

$$Q_5 = 1.794 + 1.14 \cdot \ln\left(1 + 0.638 / \left(g + 0.517g^{2.43}\right)\right)$$

Equation 4.49

$$Q_6 = 0.2305 + \ln\left(g^{10} / \left(1 + (g / 5.8)^{10}\right)\right) / 281.3 + \ln\left(1 + 0.598g^{1.154}\right) / 5.1$$

Equation 4.50

$$Q_7 = \left(10 + 190g^2\right) / \left(1 + 82.3g^3\right)$$

Equation 4.51

$$Q_8 = \exp\left(-6.5 - 0.95 \ln(g) - (g / 0.15)^5\right)$$

Equation 4.52

$$Q_9 = \ln(Q_7) \cdot (Q_8 + 1 / 16.5)$$

Equation 4.53

$$Q_{10} = Q_2^{-1} \cdot \left(Q_2 Q_4 - Q_5 \cdot \exp\left(\ln(u) \cdot Q_6 \cdot u^{-Q_9}\right)\right)$$

Here, the odd-mode parameters are less sensitive to frequency variation than the even-mode parameters, and characteristic impedance is less sensitive to frequency variation than effective dielectric constant.

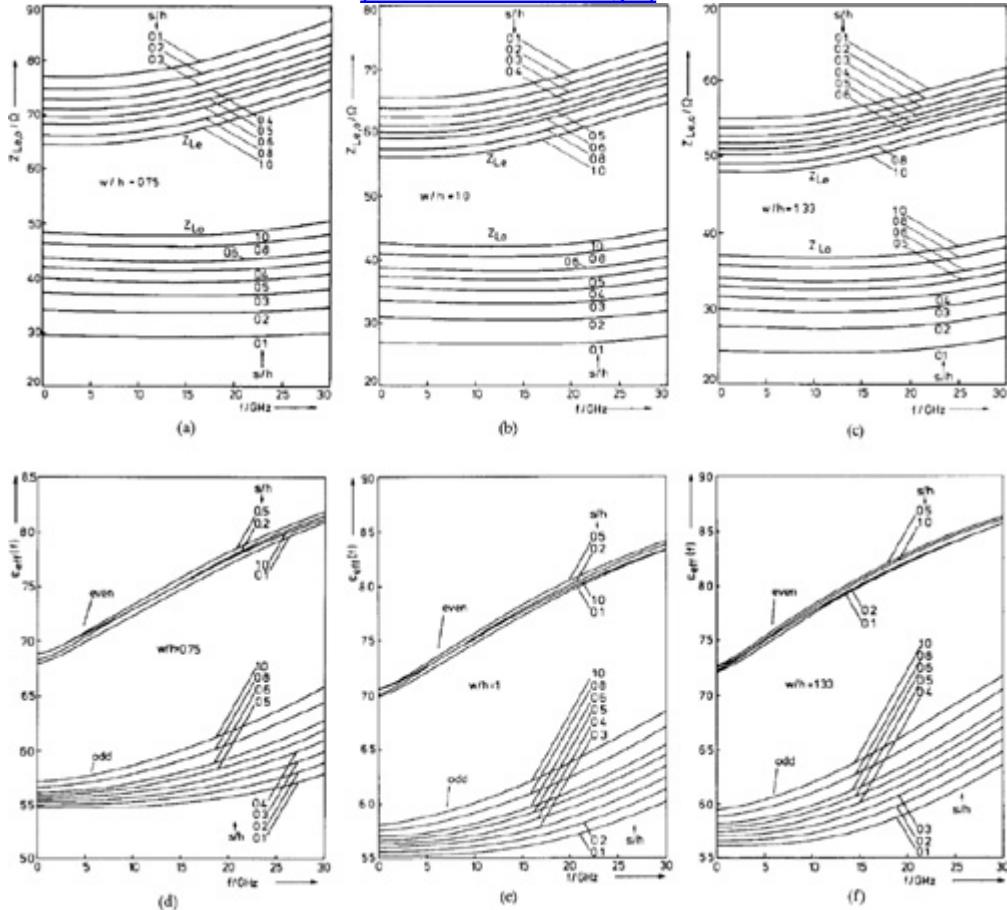
Differential signaling also suffers some amount of dispersion as in single-ended signaling. [Figure 4.33](#) shows the frequency-dependent behavior of even and odd-mode dielectric constants and characteristic impedance. This phenomenon serves as a cause of mode conversion in differential signaling.

Figure 4.33. The frequency dependent even- and odd-mode effective dielectric constants and characteristic impedances of coupled microstrip lines on a ceramic substrate (alumina, $\epsilon_r=9.70$, $h=0.64\text{mm}$). (a), (d) $w/h=0.75$. (b), (e) $w/h=1.0$. (c),

(f) w/h=1.33.

Source: M. Kirschning, and R.H. Jansen, "Accurate Wide-Range Design Equations for the Frequency-Dependent Characteristic of Parallel Coupled Microstrip Lines," *Microwave Theory and Techniques*, IEEE Transactions on Volume 32, Issue 1, Jan 1984 pp 83–90 © [1984] IEEE.

[\[View full size image\]](#)



Figures 4.34 and 4.35 show two types of coupled striplines. In the first type, the two lines are on the same plane. In the second type, they are in a different plane. This type is also known as broadside stripline. The choices of stripline depend on the application and signal integrity requirements. To match the propagation delay, care has to be taken to route the two coupled lines in an identical fashion. Even with this routing, there may be skew between the two broadside coupled lines because of the manufacturing difference between the dielectric constant of different layers, especially at higher speeds.

Figure 4.34. Coupled stripline

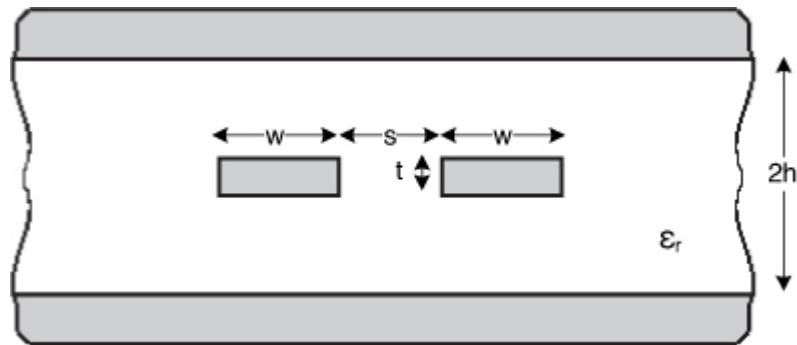
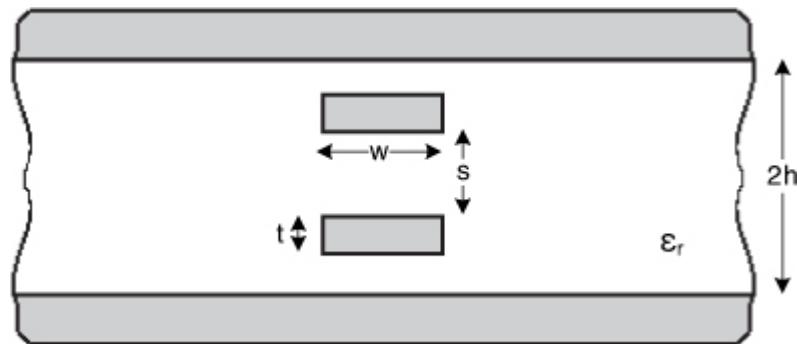


Figure 4.35. Coupled stripline—broadside



The solutions of the above equations for microstrip line, stripline, and coupled line are closer to the TEM approximation. In other words, we can easily predict the characteristic constants of the uniform TEM transmission lines using a 2-D EM modeler. Using a 3-D full-wave EM field solver, however, electromagnetic interference (EMI) and interconnects coupling (signal-to-signal & power-to-signal)—due to discontinuous reference for the IO signaling interfaces—are predicted and analyzed.

4.4.2. Package Signal Distribution Network

Package signal distribution provides signal routes from on-die circuits to the socket or PCB. With increasing speed, smaller size, and cost-saving features, package signal routing occupies a bigger portion in the entire system budget. Especially, mobile devices with higher integration use more of the packaging features to increase its efficiencies in power and device density. Formerly ignored delay and dispersion characteristics should be fully optimized to achieve maximum performance with given materials. Figure 4.36 shows an example of the assembly of different components from die to PCB level.

Figure 4.36. Cross-sectional view of core, package, socket, and PCB

Sources: M. Manusharow, A. Hasan, T.W. Chao, and M. Guzy, “Dual die Pentium D package technology development,” Electronic Components and Technology Conference, 2006. Proceedings. 56th, pp 7. © [2006] IEEE.

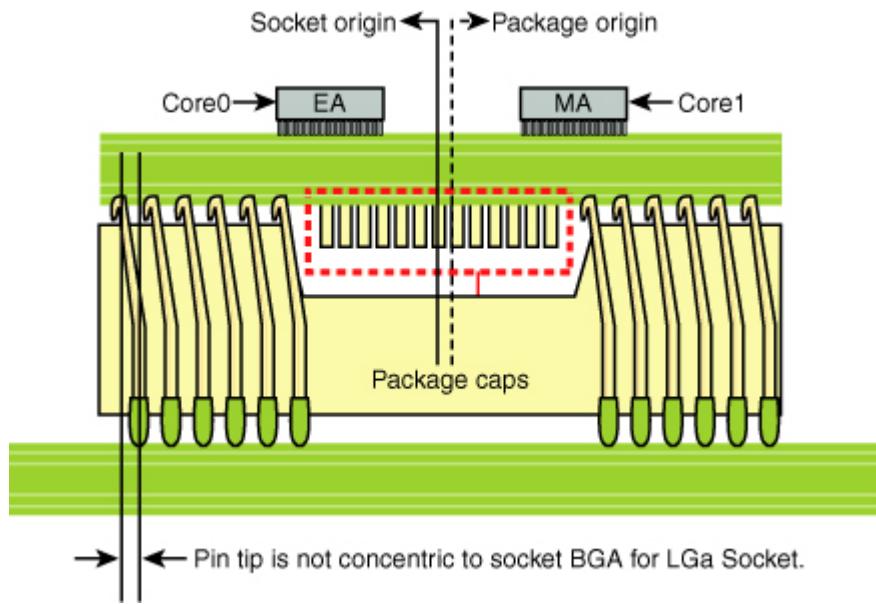
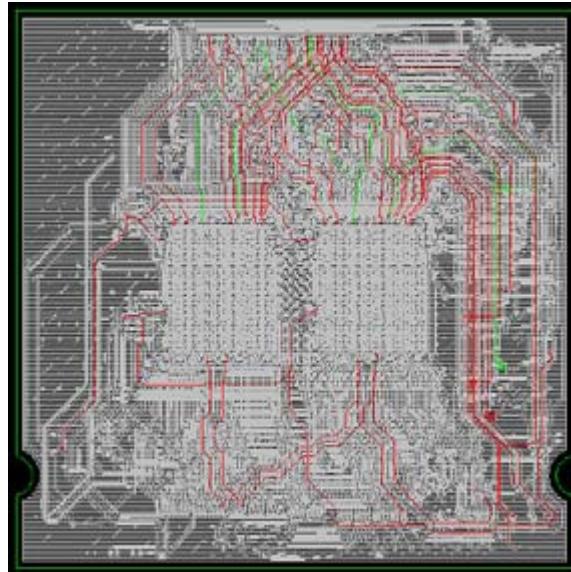


Figure 4.37 shows an example of transmission line routing on a package. Even though package signal distribution follows the same configurations as in a PCB, smaller dimensions and tolerance should be carefully considered.

Figure 4.37. Package substrate signal routing for dual die package

Sources: M. Manusharow, A. Hasan, T.W. Chao, and M. Guzy, “Dual die Pentium D package technology development,” Electronic Components and Technology Conference, 2006. Proceedings. 56th, pp 7. © 2006 IEEE.



For the microstrip implementation on a package, due to routing constraints not all signals can land on the top layer. Therefore some signals may land on internal layers and be routed for a small distance before they can come back on the top layer. The microstrip implementation is typically single referenced. For a single-referenced implementation, the power or ground

reference is maintained on all the sections of the package routing. The stripline implementation can be single referenced or dual referenced. For a dual-referenced stripline implementation, the signals are sandwiched between power and ground reference layers.

4.4.3. PCB/Package Material Properties

Material properties of the PCB and package are important in the system design. The conductivity, permittivity, and permeability are important material properties of the PCB materials [38].

4.4.3.1. Electrical Properties of Metal

A PCB has metallic signal traces and power/ground plane shapes. Static conductivity σ_s (S/m) of the signal layer and power/ground planes is used to calculate the DC drop, also called IR drop. It is defined by the equation

Equation 4.54

$$\sigma_s = -q_{ve} \cdot EM$$

where

q_{ve} = Electron charge density C/m³

EM = Electron Mobility m²/(V-s)

As the frequency of the signal increases, the current is crowded along the surface of the metal, due to magnetic fields. The skin depth is the distance the wave travels in lossy medium to reduce its value to 1/e, where e = 2.717. For a conductor with conductivity σ_s and permeability μ , the skin depth (δ) at a frequency of interest (f) is defined as

Equation 4.55

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

In copper, the skin depth at various frequencies and frequency ranges of concern from different levels of interconnection line are shown in [Figure 4.38](#).

Figure 4.38. Skin depth for copper

Frequency	Skin depth (μm)
1MHz	66
10MHz	21
100MHz	6.6
1GHz	2.1
10Ghz	0.66

PCB interconnection
Package interconnection
On-chip interconnection

There is an increase in the apparent resistance that opposes the current flow; this effect is called the skin effect. Typically the dominant loss contribution changes from conductor loss to dielectric loss as the frequency goes higher. Dielectric loss becomes a critical factor in determining the performance of interconnection lines in the multi-GHz signaling. The following section describes electrical loss properties of dielectric materials.

4.4.3.2. Electrical Properties of Dielectrics

When an electric field is applied to a dielectric medium, the flux density is different than that for the free space. It is related by a constitutive relationship $D = \epsilon E$, where ϵ is the permittivity of the medium. The dielectric constant is the real part of the permittivity, and loss tangent is pertaining to the imaginary part [38]. The dispersion equation of permittivity is defined as

Equation 4.56

$$\epsilon = \epsilon' - j\epsilon''$$

As the dielectric medium is subjected to the AC variation of the electric field, there are dipoles formed within the medium that oscillate as long as the electric field is present. The physical meaning of this displacement current is that a changing electric field makes a changing magnetic field. These oscillations produce a loss in the medium, which is called a dielectric loss.

From Equation 3.7,

Equation 4.57

$$\nabla \times H = J_{tot} = J_i + J_c + J_d$$

where

J_i = Impressed (source) current density

$$J_c = \text{Conduction current density} = \sigma_s E$$

$$J_d = \text{Displacement current density} = j\omega\epsilon E = j\omega(\epsilon' - j\epsilon'')E$$

$$J_{ce} = \text{Equivalent Conduction current density} = (\sigma_s + \omega\epsilon'') E = \sigma_e E$$

$$\sigma_e = \text{Equivalent conductivity} = (\sigma_s + \omega\epsilon'')$$

Equation 4.58

$$\nabla \times H = J_i + j\omega\epsilon'(1 - \tan \partial_e)E$$

Equation 4.59

$$\tan \partial_e = \text{Loss tangent} = \frac{\sigma_s}{\omega\epsilon'} + \frac{\epsilon''}{\epsilon'}$$

Its physical meaning is that it is a phasor relationship between effective conductive current density and displacement current densities. For dielectric materials, σ_s is low, and $\tan \partial_e$ is equal to ϵ''/ϵ' . Permeability of most dielectric material is similar to the free space permeability and equal to $4\pi \times 10^{-7}$ H/m.

4.4.3.3. Frequency-Dependent Parameters of Microstrip Line

Material characteristic parameters are frequency-dependent. For an application with short bandwidth, frequency-independent material parameters are adequate. However, for a wide bandwidth, high-speed application, it becomes significant to include frequency-dependent characteristic of materials. Frequency-dependent material parameters and frequency-dependent transmission line RLGC parameters can be extracted from frequency domain VNA measurements [39]. The use of frequency-dependent parameters makes time domain simulation more accurate because the parameters reflect the true nature of the material characteristics. It is clearly shown in Figure 4.39 that the material parameters are frequency-dependent and affect circuit parameters, as shown in Figure 4.40 [39].

Figure 4.39. Frequency-dependent material parameters

Source: Dong-Ho Han, Myoung Joon Choi, Jungwok Suk, and Woong Hwan Ryu, “Frequency-Dependent Physical-Statistical Material Property Extraction for Tabular W-element Model Based on VNA Measurements”, DesignCon, 2005.

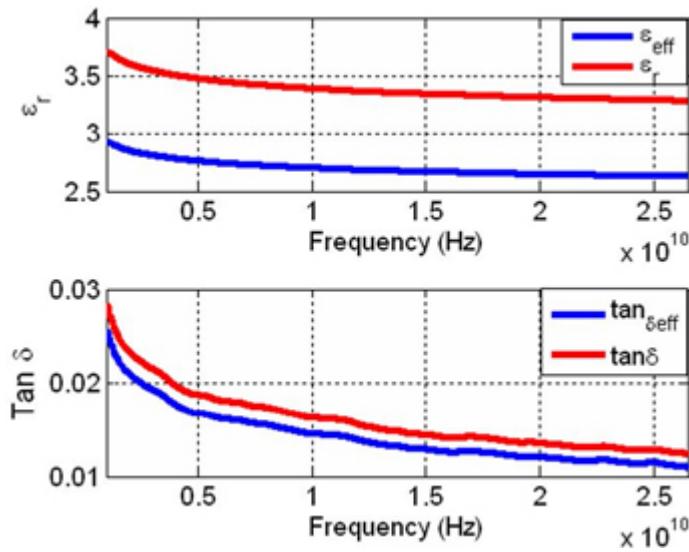
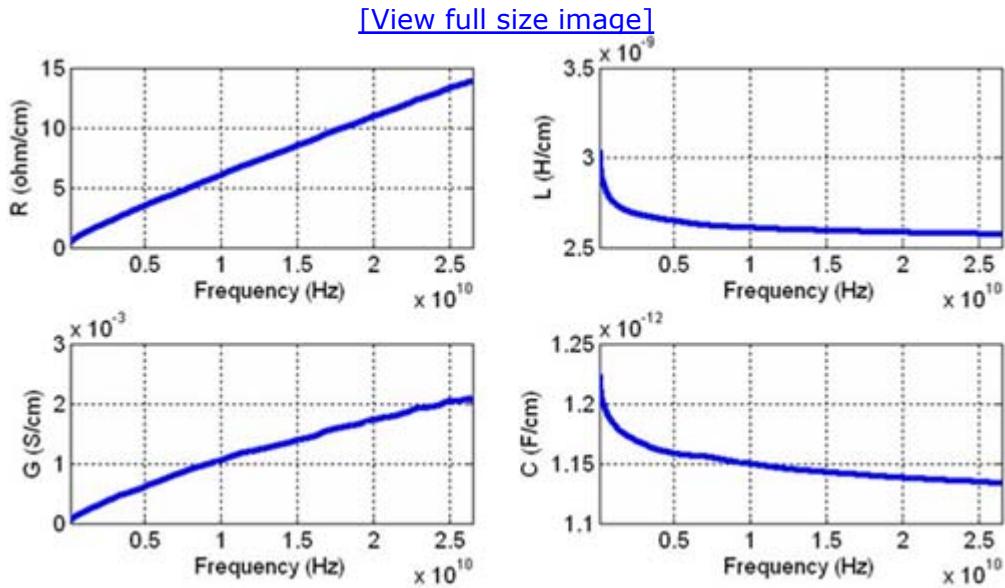


Figure 4.40. Frequency-dependent R, L, C, G of microstrip line, extracted from measured S-parameters

Source: Dong-Ho Han, Myoung Joon Choi, Jungwok Suk, and Woong Hwan Ryu, “Frequency-Dependent Physical-Statistical Material Property Extraction for Tabular W-element Model Based on VNA Measurements,” DesignCon, 2005.



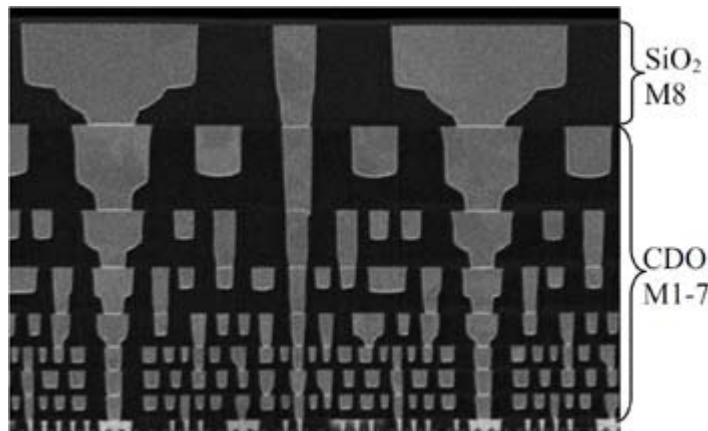
4.4.4. On-Chip Signal Network

Figure 4.41 shows an example of on-chip signal interconnects. As the on-chip transistor feature size gets smaller, the on-chip interconnection impact becomes more important. In recent high-speed designs, quite often the on-chip interconnection is becoming a limiting factor for circuit integration and performance. On-chip interconnect models are particularly becoming critical because of the lossy nature of semiconductor material and increasing frequency of operation [40]. Simulation of signal exchange through

semiconductor material requires special modeling and analysis process as the lossy material's conductivity and dielectric constant tend to require denser grid or more elements in electromagnetic modeling [41].

Figure 4.41. SEM image of 45nm interconnect stack up to Metal-8

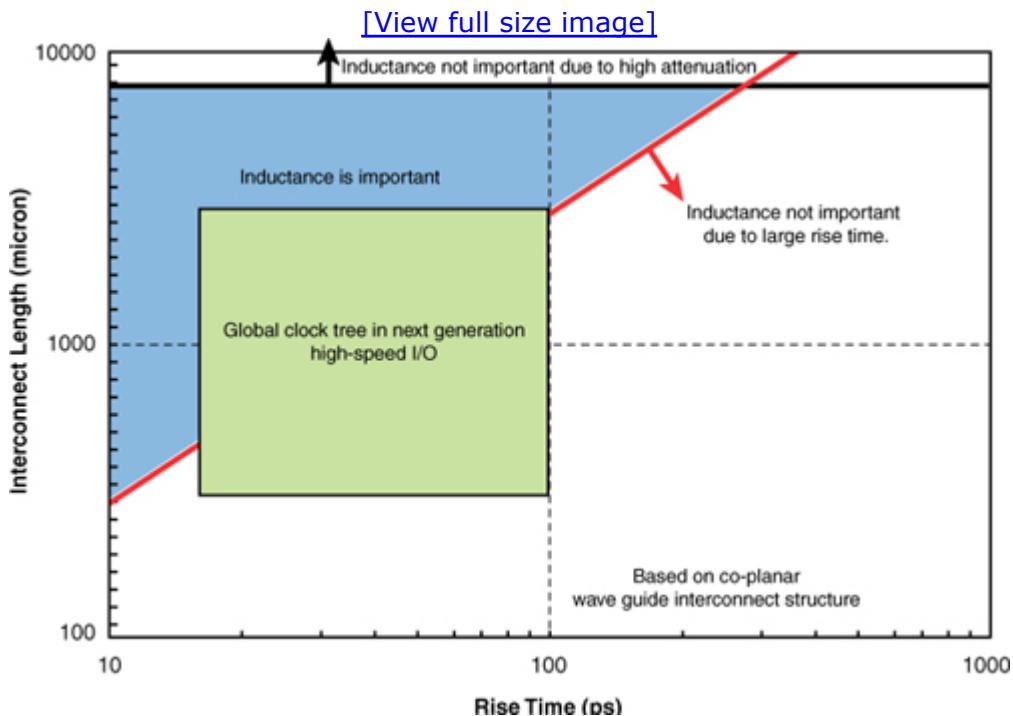
Source: D.Ingerly, S. Agraaharam, et. al., "Low-K Interconnect Stack with Thick Metal 9 Redistribution Layer and Cu Die Bump for 45nm High Volume Manufacturing," Interconnect Technology Conference, 2008. IITC 2008. International, pp 216–218, 1–4 June 2008 © [2008] IEEE.



The length of the on-chip interconnection is an important factor for deciding if rigorous parasitic extraction or electromagnetic modeling is needed. To accommodate and simplify modeling of the semiconductor, interconnection length and signal bandwidth of interest should be decided first. Figure 4.42 shows the impact of on-chip interconnect length and rise time impact on on-chip inductance. It demonstrates that the on-chip interconnect inductance should not be ignored with longer interconnect and higher bandwidth. To include inductance into the extracted model, electromagnetic modeling should be conducted. Capacitance and resistance are the fundamental parameters to incorporate into the interconnect model of the on-chip signal network. Increasingly, inductance and conductance are included in the model to conduct more accurate prediction of on-chip interconnections, especially when RLC delays are larger than RC delays. On-chip clock distribution is one of the areas that might benefit from more accurate models with inductance and conductance since on-chip clock routing tends to be long to have transmission line effects. One criterion to decide whether to include inductance into the on-chip interconnect model is provided by reference [42].

Figure 4.42. Interconnect length and rise time impact on on-chip inductance

Source: Min Wang, Ravindran Mohanavelu, and Woong Hwan Ryu, "An Optimum Clocking Design with Frequency-Tabulated W-Element Interconnect Models," DesignCon2006, Feb 2006, presentation.



Equation 4.60

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R} \sqrt{\frac{L}{C}}$$

where

t_r = Rise time of the signal at the output of the CMOS circuit driving the interconnect

R, L, C = Per-unit-length resistance, self-inductance, and coupling capacitance, respectively

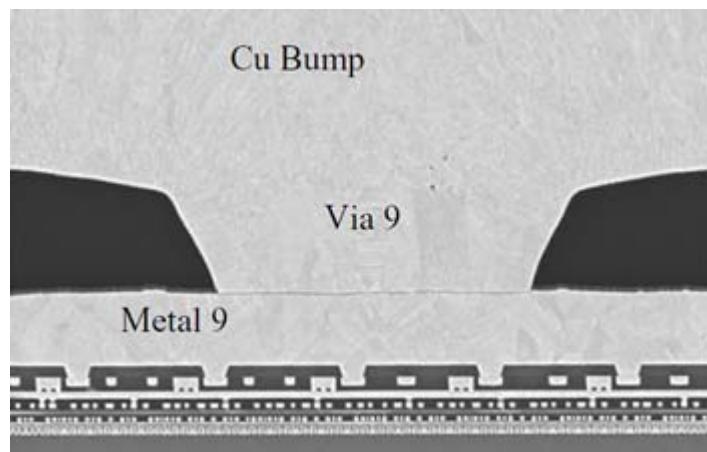
l = Physical length of the interconnection line

Figures 4.41 and 4.43 illustrate clearly the nature of on-chip interconnects. The figures show vertical on-chip interconnection. **Figure 4.43** shows an example of the bump connection to the top metal layer, through a via. The on-chip interconnections do not have solid power or ground planes as in PCBs or packages. Therefore, referencing schemes are generally different from microstrip or strip-lines because the referencing of the signal is not on dominant solid conductor planes but on neighboring narrow metal conductors. The electric and magnetic fields between on-chip signal routes cause cross-talk and dispersion, which requires different lossy material consideration. The electromagnetic impact is going to get worse with higher frequency modes. Though the dimension of the on-chip interconnection is relatively small, the increasing frequency of interest can impact signal and

power integrity. It is highly recommended to include inductance into the wide bandwidth on-chip signal and power routing analysis that suffices the relationship in equation (4.60) [43]. Chapter 9, "Measurement Techniques," describes characterization of different types of on-chip interconnect structures.

Figure 4.43. SEM image detailing the metal 9 and via 9 layers

Source: D. Ingerly, S. Agraharam, et. al., "Low-K Interconnect Stack with Thick Metal 9 Redistribution Layer and Cu Die Bump for 45nm High Volume Manufacturing," Interconnect Technology Conference, 2008. IITC 2008. International, pp 216–218, June 1–4. 2008 © [2008] IEEE.



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4.5. Interaction Between Interconnect Systems

This section describes the interaction between signal/signal and power/signal interconnects. Channel noises are categorized as three major types: Inter Symbol Interference (ISI), crosstalk, and Simultaneous Switching Output (SSO) noise. ISI is data pattern-dependent noise of a signal in which one symbol interferes with subsequent symbols. Crosstalk is an undesired signal that comes from another trace through various coupling mechanisms. As speed goes higher SSO becomes one of the most important noises, along with ISI and crosstalk. These three major types of noises are always subject to control to at least some degree. ISI can be mitigated by several different approaches. There are circuit level enablers such as adopting the equalizer, sampling the response when impulse responses of all the previous symbols crosses zero, and so on. It can also be mitigated by designing the signal interconnect to have a broadband response. Crosstalk is minimized by having the field contained near the primary transmission line as much as possible. Therefore, separating signal lines far enough, placing the reference closer, and using proper termination to reduce reflection are common solutions to the crosstalk mitigation. In addition, aggressor signal control and aggressor separation control also can mitigate crosstalk. SSO is dependent on the PDN impedance and power network-to-signal network coupling. The peak resonance impedance is dependent on on-chip capacitance and package inductance. The power-to-signal coupling is dependent on various power and signal interconnect structures. The following section describes the return paths and referencing for I/O interfaces.

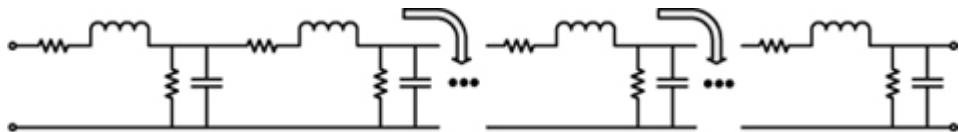
4.5.1. Reference, Ground, and Return Paths

Reference is a basis of measurement and can be ground, signal, or power. As described in [Chapter 2](#), “I/O Interfaces,” a single-ended driver has one output port and assumes a common ground and/or power connection as a reference. A differential driver has two output ports, which are different than the power or ground connection. At the driver output, one port has a second port as a reference.

The term “ground” is used in a different perspective among the system design community. For the circuit designer, ground is a zero potential node for the circuit. All the signals are typically measured with respect to their local grounds. For the package designer, the ground is the physical shape of the ground net. The chip ground bumps or ground die pads are connected to this shape. For the PCB designer, the ground is the shape for the ground net of the PCB. The package ground pins are connected to this PCB ground. On the PCB, the VRM ground is also connected to this ground net.

The current flowing on the transmission line has to return to its source. At high frequencies the transmission line tends to make a shorter return path through the capacitance than DC return path, as shown in [Figure 4.44](#). Therefore, the return path of the signal is determined by the proximity of a line to a nearby conductor with a low-impedance capacitance coupling at the particular bandwidth.

Figure 4.44. Transmission line return path



If there are power/ground plane structures with resonances, and the signal return current is going through these structures, the noise may be amplified due to the resonances. To avoid such a situation, the stackup and routing is designed in such a way that return currents do not go into the power/ground cavity structures.

4.5.2. Referencing: Single-Ended and Differential Signaling

A referencing scheme describes a way signals are arranged with proximity planes. It is particularly important in single-ended signaling, because the reference for the single-ended signal is the power or ground connection. On the PCB or the package, a ground referenced signal implies that the signal has a ground plane in close proximity. Similarly, a power referenced signal has a power plane in close proximity. A dual-referenced signal has both power and ground planes in proximity. The capacitance formed between the transmission line and the nearby conductor provides a high-frequency signal return path, so for a dual-referenced signal, return paths may exist both on power and ground planes. When the referencing scheme is changed from one to other, there is unwanted radial wave propagation. So it is recommended to have the same referencing scheme throughout the channel. However, an unintentional referencing change occurs in complex circuit board, such as signal over void, or via transition. The referencing change by the vertical structure inside of a rather flat power and ground

domain structure also works as one of the major sources of unintended radial wave propagation. It contributes to signal noise and power delivery noise when it is captured by other structures inside of the circuit board. Figures 4.45 and 4.46 show the dielectric and part of the transmission line sandwiched between the top ground plane and bottom power plane. The microstrip line above the top ground conductor is ground referenced because it runs on top of the ground plane. The transmission line sandwiched between power and ground planes have a different referencing plane depending on its proximity to the conductor plane. The central part of the transmission line in Figure 4.45(a) is ground-referenced and the central part of the transmission line in Figure 4.45(b) is power-referenced.

Figure 4.45. Referencing of transmission line

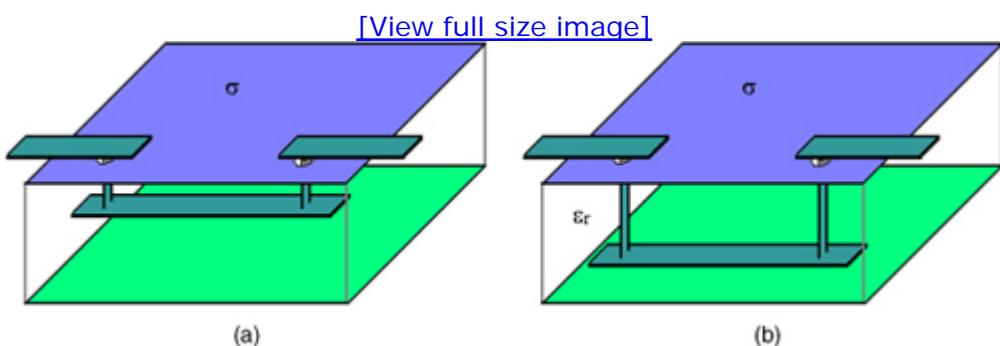
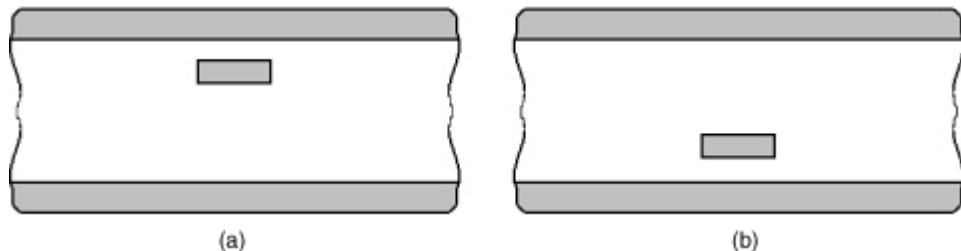


Figure 4.46. Cross-section of transmission lines in Figure 4.45



For signals in differential signaling, it can often be mistaken that the return paths are on the line with opposite polarity. The coupling from one line to the other and to the reference plane depends on the geometry and material properties. However, in many cases the real coupling between the lines with an opposite polarity signal may account for only approximately 5% to 10%. So the real return paths for differential signaling still reside in the reference plane nearby. For differential signaling, the impact of the referencing change is much smaller than that for the single-ended signaling. It is because the noise produced by this change acts as a common mode noise. Typically, differential signaling has higher common mode noise rejection.

As described earlier, uniform interconnection lines with continuous reference plane can be modeled easily using a 2D EM solver. However, for multi-Gbps data rate signaling, the referencing change impact needs to be

analyzed by a 3D EM solver. There are various scenarios for the referencing change such as a slot in the reference ground or the reference power plane, changing referencing from ground plane to power plane, or changing referencing from one power plane to other power plane. In each case, proper techniques need to be used to mitigate any potential impact. Some of them include adequate bypassing from power to ground, additional bypassing at the transition, and also via stitching. At high data rates a bypass capacitor for power/ground planes is not effective due to higher ESL and mounting inductance, so via stitching can be effective if done properly. [Chapter 7](#) illustrates the impact of stitching/decoupling on single-ended differential I/O performance.

4.5.3. Power-to-Signal Coupling

Electrically, most of the dominant PCB PDN is a resonant cavity formed by two parallel conducting plates. Signal lines are multiconductor transmission lines formed by parallel conducting wires, running parallel to the PDN planes. The combined electromagnetic field can be represented in terms of two sets of modal fields that are orthogonal.

There are different scenarios in which power nets can couple to signal nets:

- **At the interface of chip and package:** PDN impedance shows resonances in frequency domain. When buffers are switched simultaneously, there is SSO noise on the chip PDN. The coupling between power and signal nets at the interface of the chip and package affects the signal performance.
- **Package routing:** Signal bumps are connected to the package and there is a breakout region, where signals may or may not have adequate reference.

After the breakout region, the signal can be routed as microstrip or stripline. The signal line in the package may have single or dual reference structures.

- **At the pinfield or socket:** Some packages are mounted on the socket. Depending on the signal-to-ground ratio in the pinfield, there may be inadequate reference for some signals. The SSO noise is coupled to the signals.
- **PCB routing:** There may be a reference type change from the package to the PCB. As an example, the reference may be dual reference in the package and ground reference in the PCB. Also, similar to package routing, there may be reference changes within the PCB. These reference changes affect the performance of the signal.
- **Daughter-card:** If there is any daughter-card on the PCB, a connector

may be required. Signal-to-ground ratio needs to be adequate at the connector to provide a good return path. Also, the referencing needs to be continuous for high-speed signaling. If the referencing is ground reference on the PCB and power reference on the daughter-card, a reference change occurs and signal performance may be affected.

Impact of power to signal coupling is different for differential compared to single-ended systems. To evaluate the impact, accurate full-wave EM modeling of interconnect structures is required.

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4.6. Modeling Tools for the PDN and Signal Networks

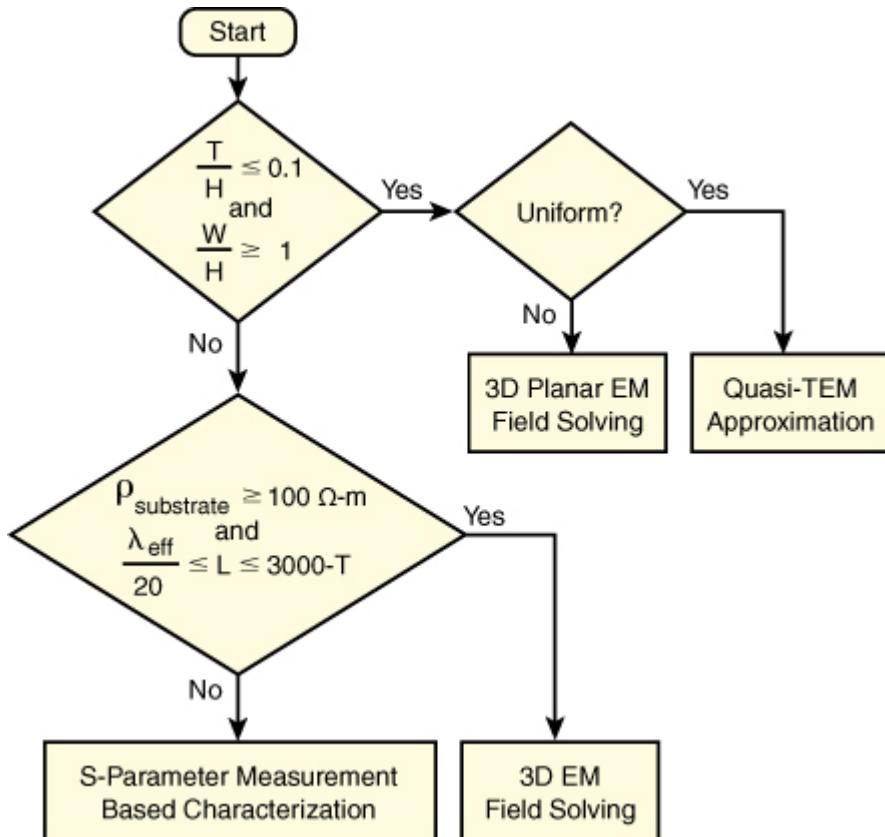
In the early years of integrated circuit digital electronics, megahertz-clock frequencies resulted in bandwidths in the order of several tens of megahertz. Thus, interconnect lengths were shorter than approximately 1/20th of the minimum signal wavelength, and the electrical behavior of the system could be described in terms of traditional lumped circuit theory. However, for today's multi-gigahertz systems, the interconnect length becomes comparable to the signal wavelength, and transmission line electromagnetic effects become important factors that impact signal integrity. Thus, the signal interconnect network and power distribution network can no longer be modeled in terms of lumped circuit theory. Furthermore, our ability to accurately calibrate and measure is becoming challenging with increased system bandwidth, reduced feature size, and increased system complexity. The necessity for electromagnetic (EM) modeling of the power and signal distribution network is apparent. Although several full-wave 3-D electromagnetic modeling approaches are available for such modeling, their simulation cost becomes prohibitive for the complex distribution networks of interest. However, these full-wave models can be simplified considerably using approximations guided by the physics of the associated electromagnetic fields in the interconnect structure. Toward this physics-based model complexity reduction, a variety of distributed electromagnetic models have been proposed over the last decade for the computer simulation of the power distribution network of high-speed digital systems during switching. For example, it has been shown that a reduced, 2D EM model may suffice for some simple power network designs. This reduced model takes advantage that the power-ground plane separation in actual boards is a negligible fraction of the wavelength and thus neglects the field variation in the direction perpendicular to the planes. This enables the reduction of a 3D vector EM problem to a 2D one without loss of accuracy. Furthermore, the reduced model can be interpreted in terms of a SPICE-compatible, distributed lumped circuit network [44, 45].

Despite its ease and computational efficiency, such a 2D approach becomes rather cumbersome when applied to complex, multilayer PCBs. Such

multilayer PCBs, especially those used with performance-driven gigahertz processors, are characterized by power distribution networks of high complexity, including planes of irregular shape, split power-ground planes, and multiple reference voltages. Added to this complexity is a high-density network of the power-ground pins and vias. This complexity introduces a variety of geometric and electromagnetic discontinuities that render the aforementioned 2D approximation of the electromagnetic fields inaccurate, especially at high frequencies. For the case, a class of locally 3D EM models are introduced that enable the proper and accurate modeling of the departure of the EM field from its 2D approximation in the vicinity of the aforementioned geometric and electrical discontinuities. The enhanced accuracy through the 3D modeling of fine features comes at the cost of increased model complexity. This type of 3D analysis is still mainly dependent on planar solutions, with considering local 3D effects and can be called as planar-3D simulation.

Both the computing time and memory required for EM simulations increase with the complexity of the circuit and the density of mesh. The 3D full-wave EM simulation takes much more time than the 2D and 3D-planar EM-field solutions. A chip-level interconnection-line simulation takes more time because of the higher aspect ratio compared to board-level and package-level interconnection lines. The aspect ratio should be less than 3000:1 for accurate and efficient simulations. For accurate and efficient simulation and design for high-speed microstrip interconnection lines, software limitation, accuracy, computing time, and memory usage should be considered. An accurate and efficient modeling flow diagram for interconnections at frequencies in the GHz range is shown in [Figure 4.47](#). For microstrip interconnection lines with a thickness (T) to height (H) ratio less than 0.1, a width (W) to height (H) ratio greater than one, and a 5% error in the difference between a 3D EM-field solver and a 3D-planar EM-field solver, it is not necessary to consider the effects of fringing fields, dispersion effects, and radiation losses. Thus a 3D-planar EM-field solver and quasi-TEM-approximation-based software tools, such as a 2D EM-field solver and a transmission-line calculation based on an analytical solution or empirical model, can produce accurate interconnection line models. This is especially true for a uniform interconnection line, where a quasi-TEM approximation (lumped circuit model) is useful in reducing computing time. On the other hand, nonuniform interconnections such as interconnects with non-continuous reference plane, impedance step lines and microstrip lines with cross-junctions and bends should be analyzed and designed using a 3D-planar or a full-wave EM-field solver. As can be seen from [Figure 4.47](#), if $T/H > 0.1$ or $W/H < 1$, a 3D full-wave solution or S-parameter measurement-based characterization is required for accurate design.

Figure 4.47. An accurate and efficient modeling flow chart for interconnection lines



Until this point, the flow chart can be applied to the PCB, package, or on-chip silicon interconnects; however, this paragraph focuses specifically on silicon interconnect lines. In the case of a relatively highly resistive substrate ($\rho_{\text{substrate}} \geq 100 \Omega\text{-m}$) such as MCMs (MultiChip Modules) and silicon chips without a highly lossy silicon effect, and for moderate length microstrip interconnection lines ($\lambda_{\text{eff}}/20 \leq L \leq 3000 \times T$, T : metal thickness), a 3D field solver is quite adequate for accurate simulation and design. For an accurate 3D full-wave simulation, a proper microstrip interconnection length is required. In other words, if the line length is less than $\lambda_{\text{eff}}/20$, the characteristic constants, especially the effective dielectric constant and loss, may not be accurately obtained. This may be because the relatively short interconnection length increases internal field error at the analysis frequency. Thus the lumped modeling approach should be adequate. For an aspect ratio greater than 3000, the interconnection line simulation takes a long time or may not be completed because of the high aspect ratio. Therefore, minimum frequencies for accurate and efficient simulation using the 3D EM-field solver can be defined by the criterion in Figure 4.47 as $\lambda_{\text{eff}}/20 \leq L \leq 3000 \times T$, where T is the metal thickness. For thick metal PCB-level and package-level interconnections, the minimum frequency is approximately 100MHz. On the other hand, for accurate and efficient modeling of chip-level interconnection lines using the 3D EM-field solver, calculations should be confined to frequencies above approximately 2GHz. Finally, predictions for characteristics of interconnection lines with high loss or high aspect ratio should be based on S-parameter

measurements.

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Chapter 5. Frequency Domain Analysis

This chapter illustrates the design techniques for power delivery networks and signal networks in the frequency domain. The first section provides the requisite background and supporting information about the frequency domain analysis for power and signal integrity applications. The subsequent sections provide detailed analysis methods for the power integrity and signal integrity using various frequency domain techniques.

The relationship between the time domain information and the frequency domain information of a certain device is complementary and requires the frequency domain analysis along with the time domain analysis to thoroughly understand the behavior and the nature of the device. This idea will be made clear as the relationship between time waveforms and their frequency domain counterpart is developed. The concepts and techniques introduced here form the backbone of the frequency domain analysis, and the subsequent sections draw upon this material. The frequency domain analysis for power integrity is elaborated with an example of the power distribution network meeting certain target impedance. Effects of different elements such as chip, package, and PCB on the impedance response are evaluated. Design techniques to determine Simultaneously Switching Output (SSO) noise impact in the frequency domain and the isolation between two domains are presented. This chapter presents a detailed analysis about the on-chip power distribution network design and characterization. It also describes the signal network performance taking into account the on-chip parasitic and terminations to the power distribution network. End-to-end signal distribution network design is presented in the frequency domain with simulations and characterization. Design techniques for determining Inter Symbol Interference (ISI) and crosstalk are also demonstrated.

5.1. Signal Spectrum

This section provides you with a general feel and insight into the signal analysis techniques. A concerted effort is made to minimize the number of equations and mathematical developments, and focus is on the physical picture behind the concepts. Detailed mathematical descriptions and proofs

can easily be obtained in the large body of technical literature devoted to these topics.

Time/frequency analysis refers to the interrelated nature of describing a waveform in either the time or frequency domain. The link is provided by the Fourier transform (and its brethren), and this section introduces the concepts of the Fourier series, Fourier transform, and Fast Fourier transform (FFT) and the analysis techniques that are enabled by these methods.

Let $x(t)$ be the waveform at a receiver. If the waveform is periodic, then it is possible to represent the waveform as a Fourier series. There are numerous versions of Fourier series (cosine, sine, and so on), but to illustrate the link between the time and frequency domain, the following form is particularly useful:

Equation 5.1

$$x(t) = D_o + \sum_{n=1}^{\infty} D_n \cos(2n\pi f_o t + \varphi_n)$$

where f_o is 1/period, and D_n and φ_n are constant coefficients, and the discrete n is referred to as harmonics. The physical interpretation is that any periodic time domain waveform can be constructed out of sinusoids of various amplitudes and phases. These sinusoids are all just a single "frequency" and make up the spectrum or frequency domain waveform. The resulting "Line" spectrum is (positive frequencies) given by

Equation 5.2

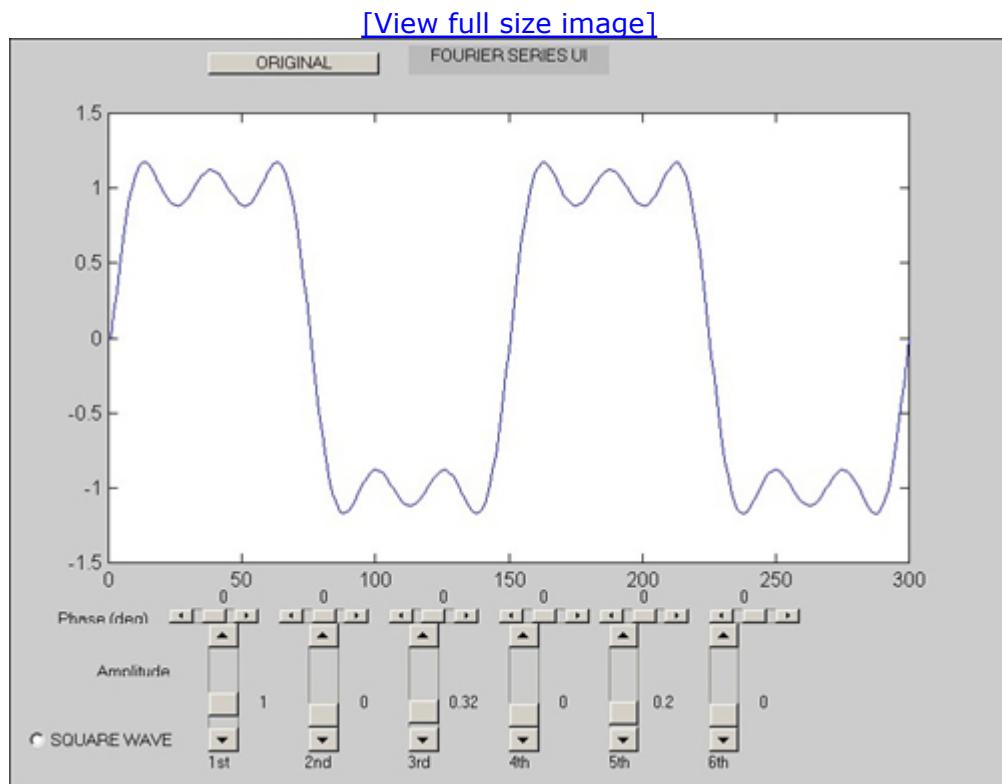
$$y(f) = \sum_{n=1}^{\infty} D_n e^{j\varphi_n} \delta(f - nf_o)$$

This equation says that the spectrum of a periodic waveform is composed of discrete frequencies (nf_o) with amplitude D_n and phase φ_n . A simple example would be if $x(t) = 0.8 * \sin(2\pi * 10 * t)$, then the spectrum would be $y(f) = 0.8 * \delta(f-10)$, and is just as we would expect; a sinusoid is composed of a single frequency component.

How does it help us to represent a waveform as a series of sinusoids? The answer is of course because of frequency domain analysis. One can now solve a problem in the frequency domain by finding the D_n , φ_n and then get back to the time domain using those coefficients. Therefore, if you can determine how a topology affects a sinusoidal waveform (attenuate or amplify and phase change) it can also be used to find the effect on a general (nonsinusoidal) periodic waveform.

The examples shown in [Figure 5.1](#), are obtained using a commercial tool that enables a user to set the amplitudes (D_n) and phases (ϕ_n) for $n=1,2,3,4,5,6$, and if a square wave is assumed, then the tool will automatically set the even harmonics amplitude to 0 and the odd harmonic ($1,3,5,7,9,11$) to their $1/n$ amplitudes. In [Figure 5.1](#), the 3rd and 5th harmonics are set to $1/3$ and $1/5$, respectively, with the even harmonics set to 0, the resulting time domain waveform is shown, which is the first three terms in a square wave series.

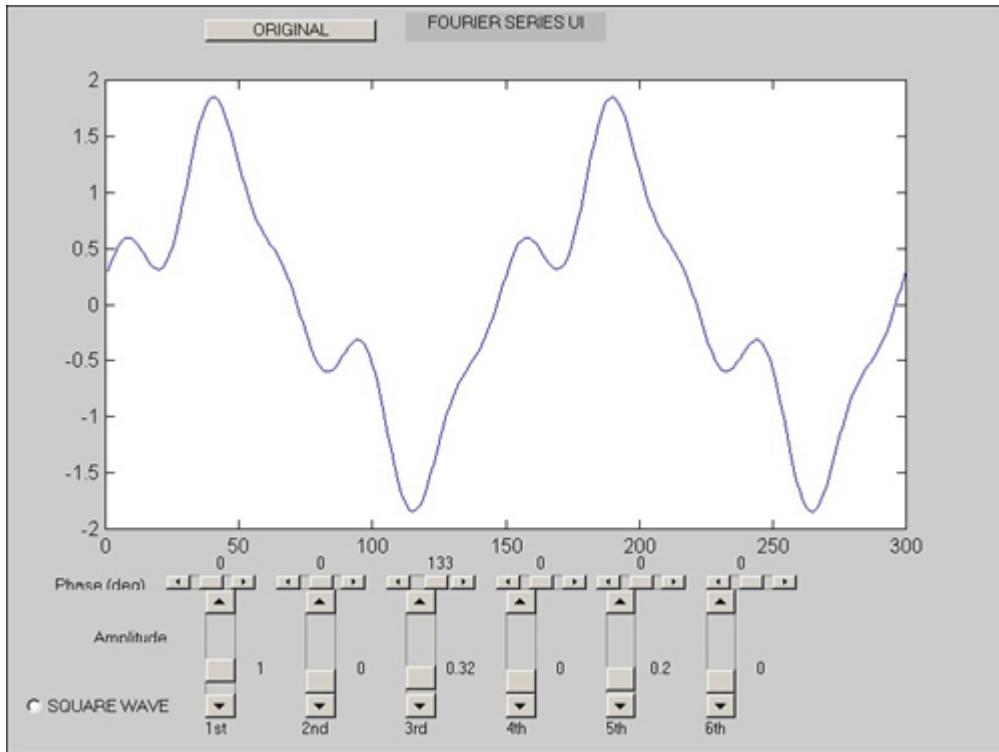
Figure 5.1. Fourier series UI. Generic tool to study Fourier series



In this example, if the phase is changed for a harmonic, the resultant waveform changes shape, even though the amplitude of the harmonic remains the same. In [Figure 5.2](#), the third harmonic has a phase deviation of 133 degrees; the resultant time domain waveform shows huge ledges. This illustrates of the importance of the phase information you can obtain in frequency domain analysis; even though the amplitude is unchanged, the phase deviation can still greatly impact signal quality.

Figure 5.2. Phase deviation (3rd harmonic) impact on a Square Wave

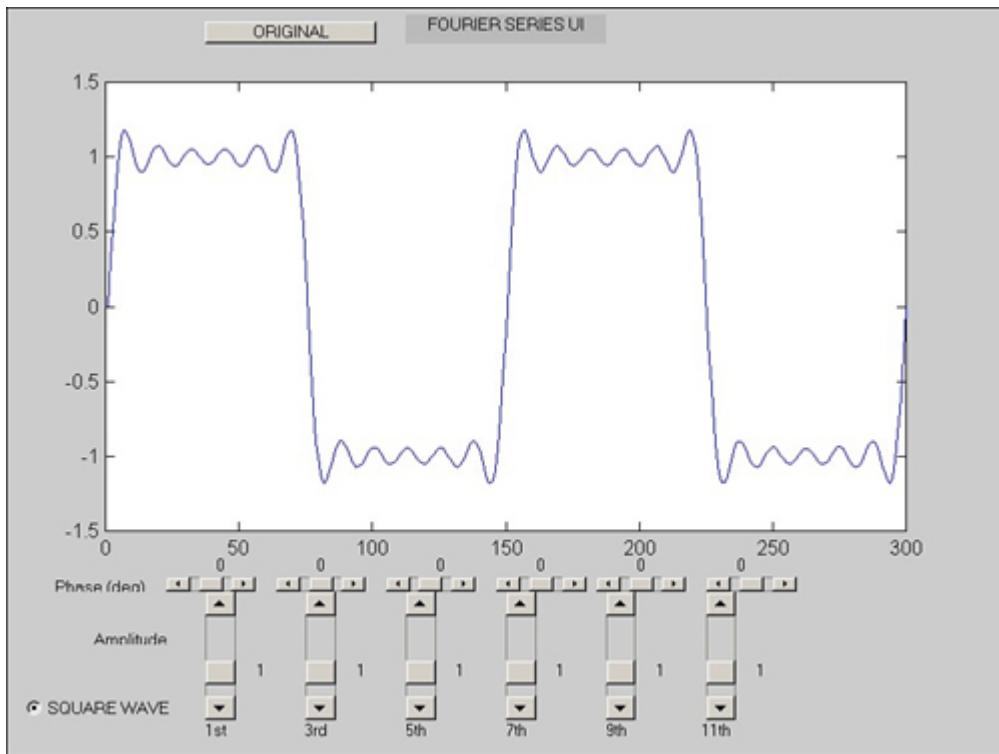
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As mentioned earlier, the tool also has the Square Wave feature, which changes the slider bars (amplitude, phase) to be just the odd harmonics, with implied square wave weighting. This feature is shown in [Figure 5.3](#). This also illustrates the ideas behind bandwidth and edge rate, as we increase the bandwidth (5 harmonics to 11 harmonics) the edge rate increases. This can also illustrate the reverse effect (low pass filtering/capacitive loading), where the edge rate decreases as the bandwidth is lowered (11 harmonics down to 5 harmonics). This is directly related to the frequency domain analysis performed for signal integrity. A transfer function is obtained in the frequency domain, which weights (multiplied) the amplitude and phase of the input waveform to obtain the spectrum of the output waveform. This is exactly what is shown in [Figure 5.3](#), where we see the transfer function is weighting the amplitude by all 1s and the phase is being shifted by 0° . This is the case of the perfect transfer function ($\text{OUTPUT} = \text{INPUT}$).

Figure 5.3. Square Wave, using 11 harmonics (Note the Square Wave option is active.)

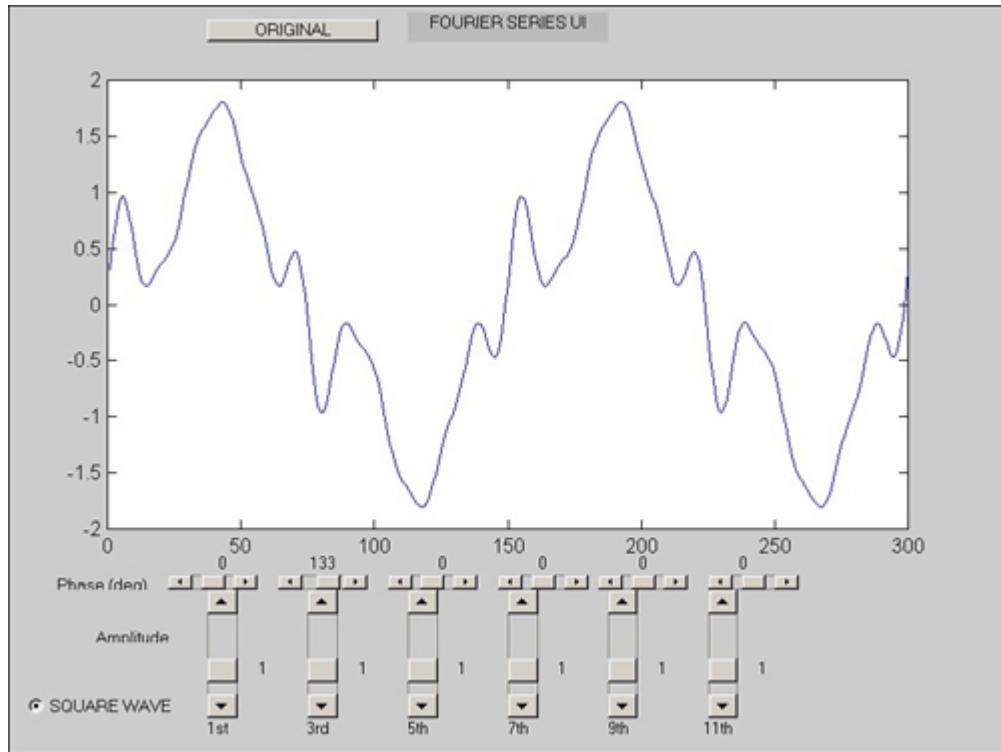
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Again, deviations from the perfect transfer function can be observed. In Figure 5.4, the third harmonic is shifted by 133 degrees (same as in Figure 5.2) with the resultant time domain waveform shown. Note that the waveform is quite different than the 5th harmonic case (Figure 5.2), which is due to the expanded bandwidth. As before, the amplitudes still have the “perfect” transfer function (all 1s), and major signal quality issues can still arise.

Figure 5.4. Square Wave with phase deviation in the 3rd harmonic

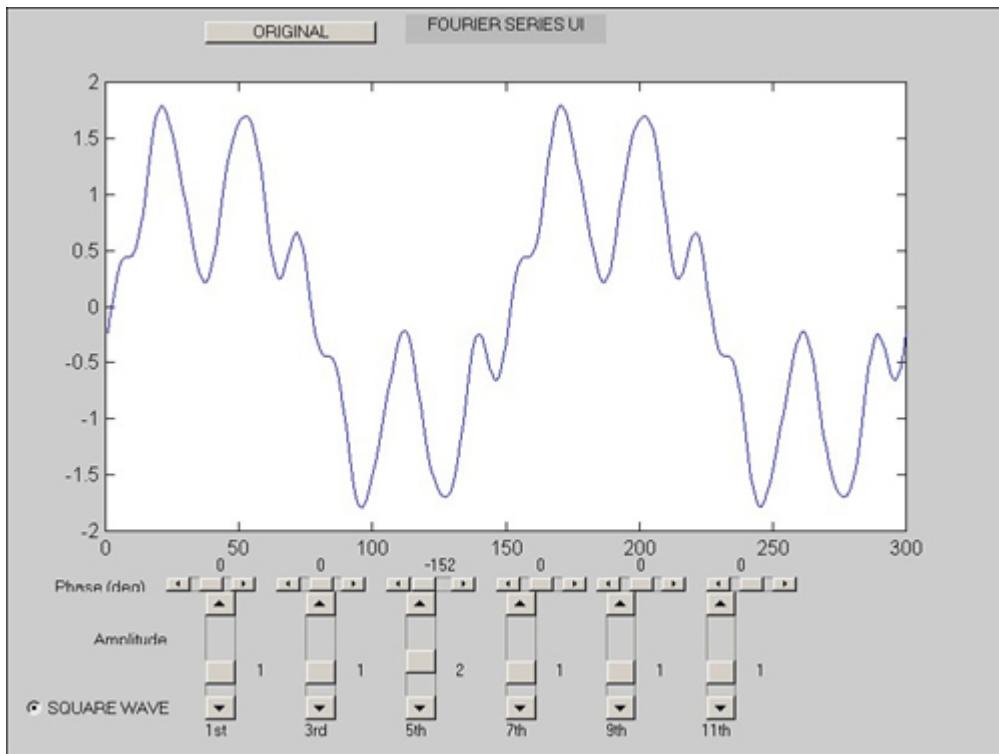
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The final example for the Fourier series shows a case where the transfer function has a resonance. In [Figure 5.5](#), the 5th harmonic in this square wave is multiplied by 2; this would be a resonance condition (pole in the frequency domain). Also, note the phase is also shifted in this example. The time domain waveform shows a large amount of ringing at the 5th harmonic (as expected).

Figure 5.5. Square Wave with phase and amplitude deviation in the 5th harmonic

[\[View full size image\]](#)



The Fourier series as explained before is useful for a general understanding of the frequency domain concepts but is not the entire picture. The Fourier transform provides the rest of the picture and enables the spectrum to be filled in between the harmonics and removes the restriction of a periodic waveform.

5.1.1. Fourier Transform Interpretation

Fourier transform establishes the conceptual link between the time and frequency domain. The Fourier series is applied for periodic (infinite extent) waveforms, but the ideas behind the Fourier series can be generalized to become a Fourier transform. This is done by allowing for a continuum of frequencies (not just harmonics) and moving from a series representation to an integral representation. The Fourier transform is applicable to large subset of waveforms and does not require periodicity. The Fourier transform of a time domain waveform results in a spectrum once again, and this spectrum now contains a continuum of frequencies, all with amplitude and phase "coefficients," just like the Fourier series. The spectrum of a Fourier transform is continuous (continuum of frequencies) as compared to the "line" spectrum of a Fourier series. Note that if the waveform is periodic, a Fourier transform yields a line spectrum identical to that of the corresponding Fourier series.

The physical interpretation of the Fourier series spectrums versus a Fourier transform spectrum is as follows: Fourier series produces "lines" (infinite spectral resolution), because the waveform is periodic and infinite. As you truncate an infinite waveform, the lines begin to broaden and produce the

Fourier transform spectrums. As the truncation is made more and more severe, the broadening is increased until the point that a delta function (time domain), which is the most truncated time domain waveform, produces an infinitely broad spectrum. (All frequencies are needed.)

This is the essence of the uncertainty principle in time-frequency analysis. Also, it is one of the reasons why we do frequency domain analysis in the first place and follow it with time domain (transient) simulations as well. This is because a time domain response provides an excellent resolution in the time domain, which as explained earlier, would be difficult to obtain in the frequency domain (need a lot of frequency points). The converse is also true; a frequency domain response provides perfect resolution in the frequency domain, whereas a time domain waveform would take a prohibitive amount of time to simulate at that resolution.

For real-world applications a continuum of frequencies is impossible; therefore, it is necessary to discretize the frequencies (just like we do in the time domain with a time step). This results in a Discrete Fourier Transform (DFT) and a special form of the DFT is the Fast Fourier Transform (FFT).

The important concept to remember is that the time steps (in the time domain) are inversely related to the frequency steps in the frequency domain. This is another statement of the uncertainty principle. The frequency resolution can still be improved (even with a small time step), by increasing the number of points, by zero padding, or simulating a longer time domain response.

5.1.2. Important Properties of the Fourier Transform

This section lists some of the important properties of the Fourier transform; note that this information can be found in numerous textbooks along with additional properties and transform pairs.

5.1.2.1. Interpreting and Using Frequency Domain Representations of Waveforms

A spectrum $y(f)$ is in general a complex (real and imaginary). The common plot of a spectrum is the power spectral density (PSD) which is $20 * \log(\text{abs}(y(f)))$. This plot gives information only for the magnitude of the spectrum, however, the phase portion is also important. The Fourier transform of a real valued (typical) time domain waveform produces a spectrum with negative frequency components ($y(f) = y(-f)^*$). A common practice is to display only the positive frequencies. It is important to include the negative frequencies when computing the inverse Fourier transform.

5.1.2.2. Key Properties of Fourier Transforms (of Interest in

SI)

- Convolution in time domain is multiplication in frequency domain :: $x(t) * z(t) = X(f)Z(f)$
- Linearity :: $ax(t) + bz(t) = aX(f) + bZ(f)$
- Time delay/Phase shift :: $x(t-a) = X(f)\exp(-j2\pi f \cdot a)$
- Rectangular waveform in time domain is sinc function in frequency domain (and vice versa)
- Triangular waveform in time domain is sinc^2 function in frequency domain
- Trapezoidal waveform is corresponding to $\text{sinc}(A)*\text{sinc}(B)$
- Impulse in time domain is a flat spectrum (-inf to inf) in freq.
- Impulse in freq domain is infinite sinusoid in time domain.
- Impulse train in time domain is impulse train in frequency domain (used with convolution delta functions).

5.1.2.3. Fourier Transform Examples and Interpretation

The power spectral density (PSD) is the common means of displaying spectrum magnitudes. The PSD of random bit patterns are shown in [Figure 5.6](#), where various (random) 100-bit sequences of perfect square pulses are Fourier transformed. This plot is overlayed with the theoretical, $\text{sinc}(F*T/2)$ ($F=\text{Freq}$, $T=\text{bit period}$) PSD along with certain deterministic cases (Fastest 101010101..., $\frac{1}{2}$ Fastest 11001100... and slowest 0000000...11111....). The respective time domain waveforms can be seen in [Figure 5.7](#), where top to bottom plots are the slowest, $\frac{1}{2}$ fastest, fastest, and then one random bit pattern. The PSD in [Figure 5.6](#) is for a 33MHz (max freq) bus, where the odd harmonics are seen to be maximal points and the even harmonics are nulls. This plot illustrates the need for frequency domain analysis to “fill” in the spectral coverage that time domain bit patterns leave out, when they are not exhaustively simulated. Also of importance is the edge rate was not included in this example.

Figure 5.6. PSD of random bit patterns (Square Wave)

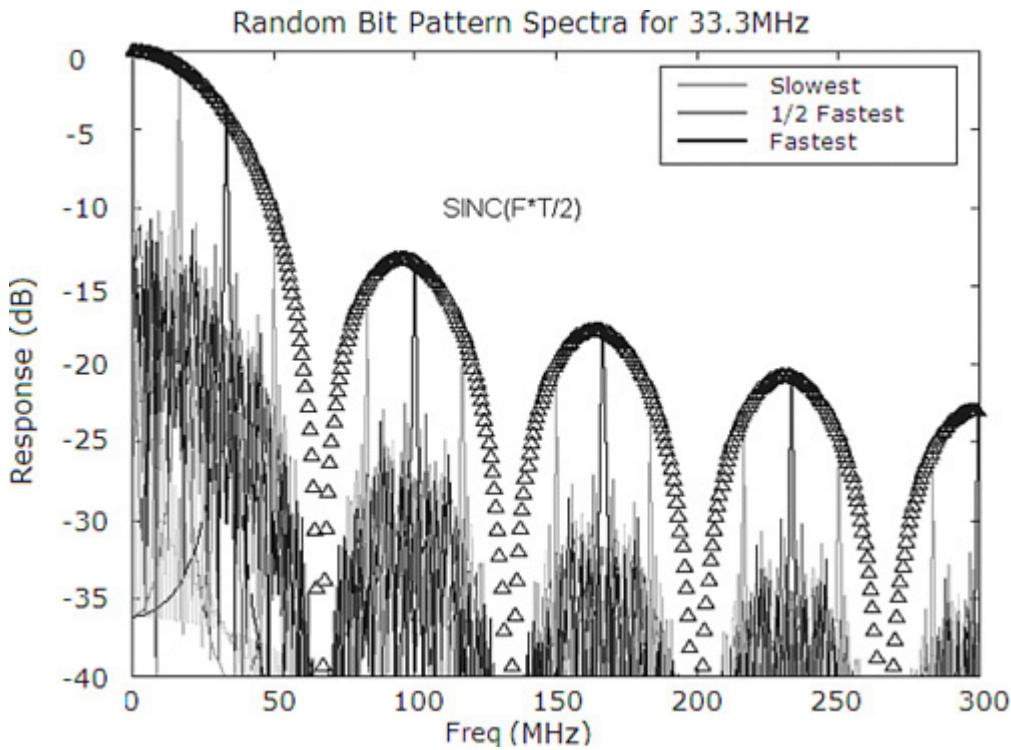
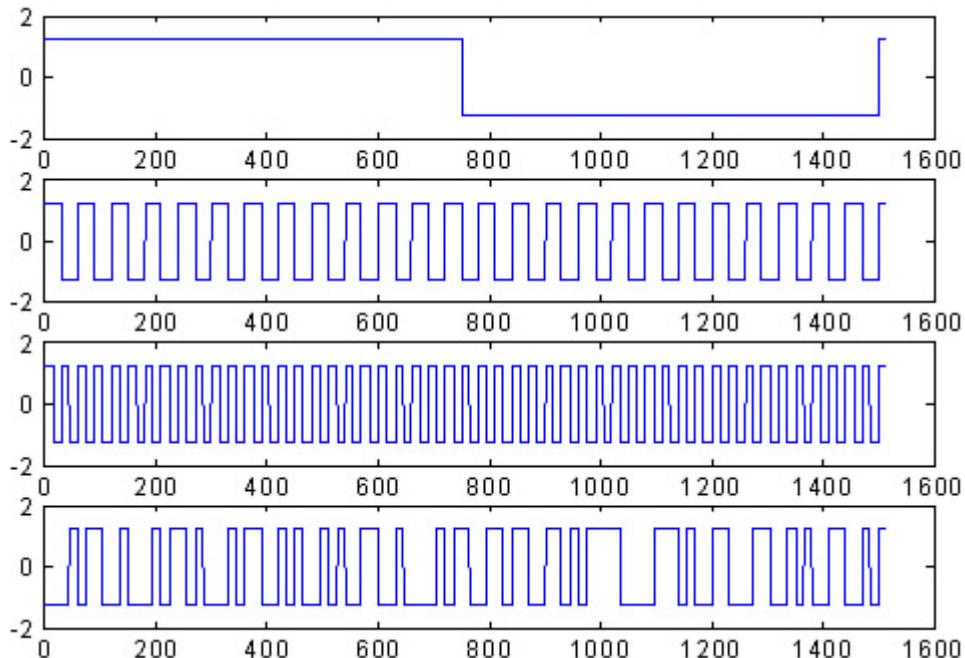


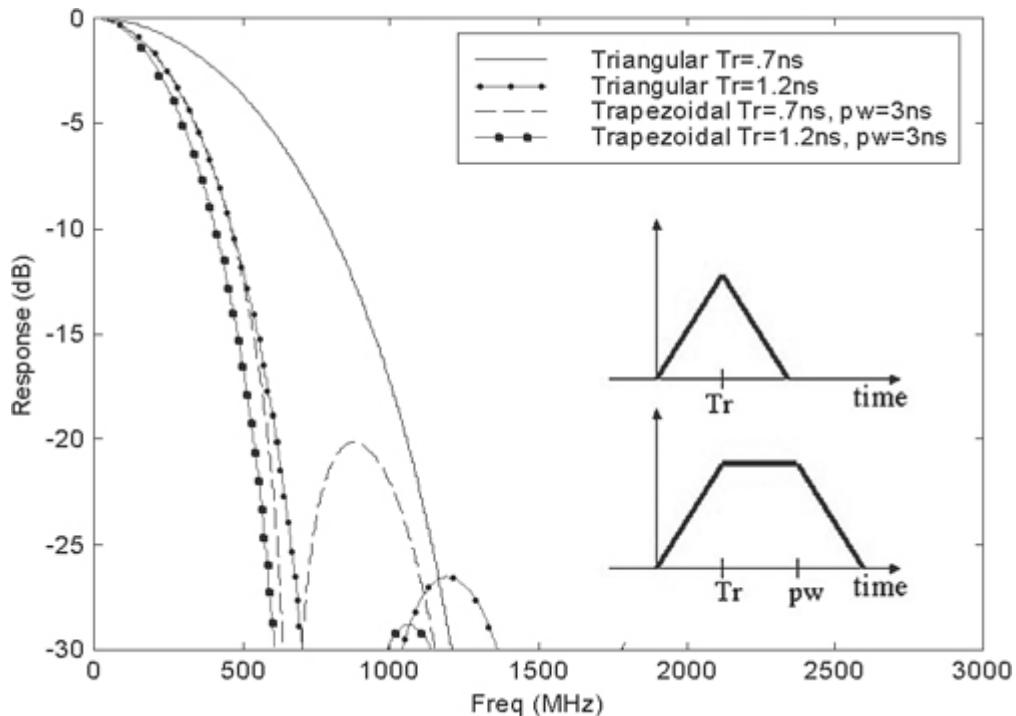
Figure 5.7. Time domain waveforms for random bit pattern example



The following examples look into the relationship of edge rate and bandwidth. The general concept that the edge rate is related to bandwidth was discussed in the Fourier series section, where it was shown that a larger bandwidth signal resulted in faster edge rates. The following analysis is performed using the Fourier transform on just a single pulse (not periodic wave). In Figure 5.8, the PSD for two triangular pulses (in the time domain) are shown in the solid lines, and two trapezoidal pulses in the dashed lines.

The rise time (edge rate) was varied to show the impact in the frequency domain. The faster the edge rate, the larger the bandwidth, as seen with the 0.7ns rise time versus the 1.2ns rise time.

Figure 5.8. PSD of various pulse shapes



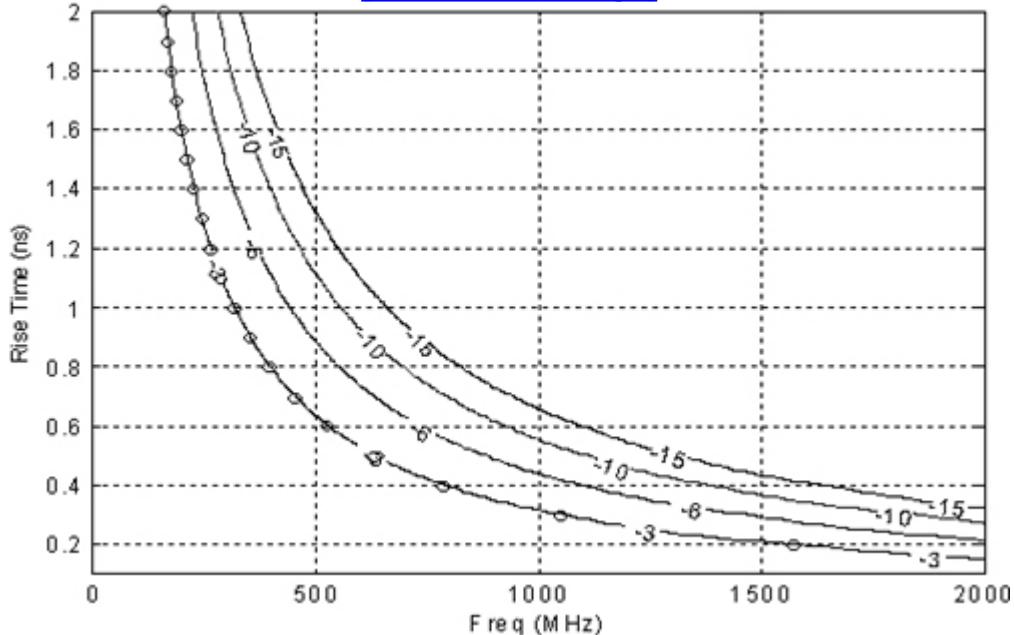
The trapezoidal waveform though does not require the same amount of bandwidth that the triangular wave requires. This can be seen from the mathematical descriptions of the spectrums. From the properties of the Fourier transform, the triangular pulse is corresponding to $\text{sinc}(\text{Tr}) * \text{sinc}(\text{Tr})$ (not exact equations just to show relationship), whereas the trapezoidal pulse is corresponding to $\text{sinc}(\text{Tr}) * \text{sinc}(\text{pw})$, where $\text{pw} > \text{Tr}$, therefore the $\text{sinc}(\text{pw})$ term modulates the $\text{sinc}(\text{Tr})$ and reduces (because $\text{pw} > \text{Tr}$) the bandwidth.

Also of importance is that the amplitude of the time domain waveforms does not impact the Fourier transforms (linearity), other than the amplitude of the transform.

The analysis on the pulse spectrums can be extended by sweeping the rise time for the triangular waveform. In [Figure 5.9](#), the rise times are swept from 0.1ns to 2.0ns, with the resulting PSD dB contours shown. The rule of thumb for edge rate to bandwidth is $1/(\pi * \text{rise time})$ and we see that this correlates to the 3dB points of this waveform. We also observe the dependence on rise time (Tr) changes significantly as the rise time goes below 1ns, as expected.

Figure 5.9. dB contours of PSD for triangular pulses with various rise times, overlayed with the $1/(\pi \times \text{Tr})$ approximation

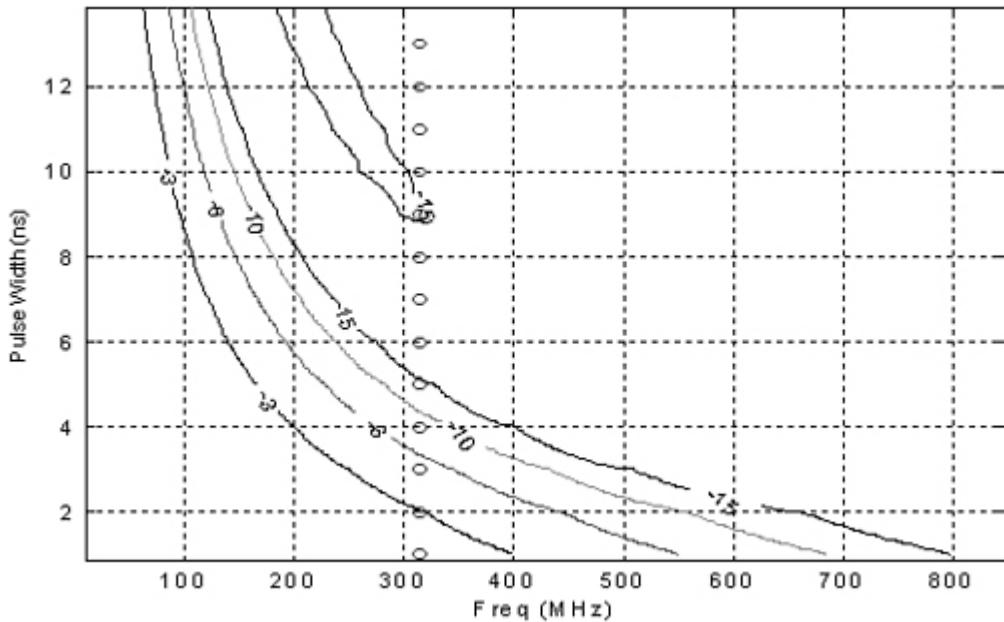
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The dependence on pulse width (pw) is shown in [Figure 5.10](#), where a nominal rise time of 1ns is assumed for all cases as the pulse width is swept from 2ns (triangular) to 14ns. We observe that the pulse width decreases the bandwidth of the pulse and that the 2ns pulse width correlates to the triangular wave, as expected. The other observation is that the first sidelobe becomes more and more important as the pulse width is increased, this is physically the effect of the edge rate and tends to create a need for a higher effective bandwidth (more in line with the triangular pulse) to capture the sidelobe.

Figure 5.10. dB contours of PSD for trapezoidal pulses with various pulse widths ($Tr = 1\text{ns}$), overlaid with the $1/(n \times Tr)$ approximation

[\[View full size image\]](#)



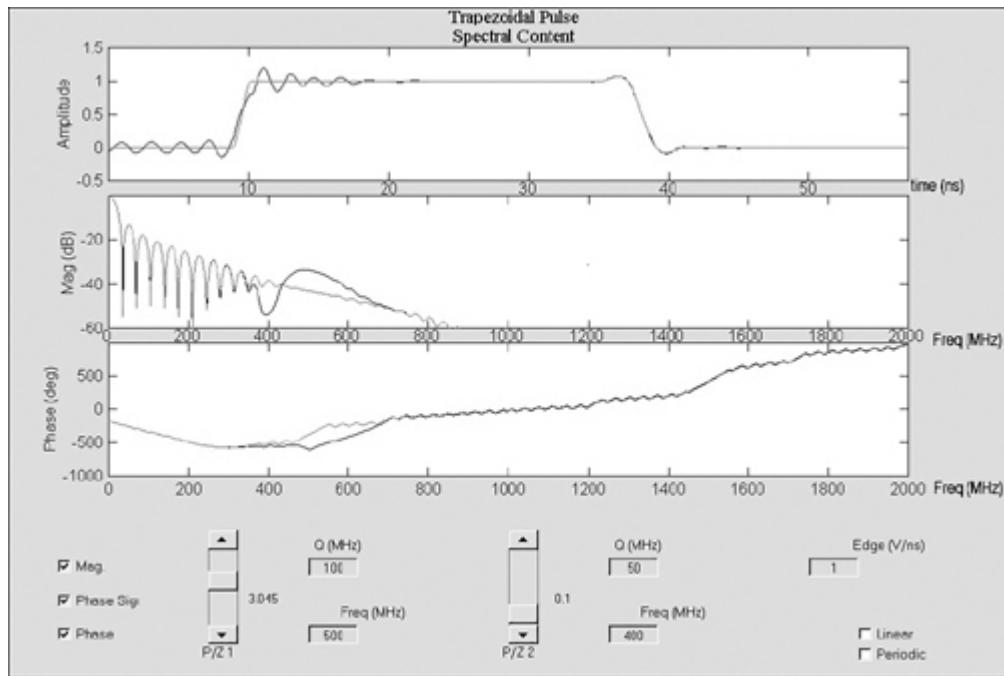
From these plots various metrics can be defined to determine a frequency domain specification. For example, if a 1ns risetime (convert to slew rate if necessary) is required at a receiver, the channel must pass at least 600MHz to meet a -10dB specification, provided that the driver can transmit a 1ns risetime waveform. The frequency domain response of the channel would then be used to ensure the proper bandwidth is available (and well behaved).

5.1.2.4. Trapezoidal Pulse Fourier Transform Tool

To study the relationship between the time and frequency domain, a generic software tool has been created that provides an interactive environment to explore these concepts. [Figure 5.11](#) shows the basic interface, where three large plots show the time, magnitude (Freq), and phase (Freq) plots for a given signal. The user can add up to two poles/zeros and observe the effects in the time and frequency domains as compared to the ideal case. This tool can be thought of as representing the transfer function of the system, with the driver and the receiver side curves. However, when applying deviations to the phase and magnitude, a causal relationship is not enforced.

Figure 5.11. Software tool for Fourier transform concepts

[\[View full size image\]](#)



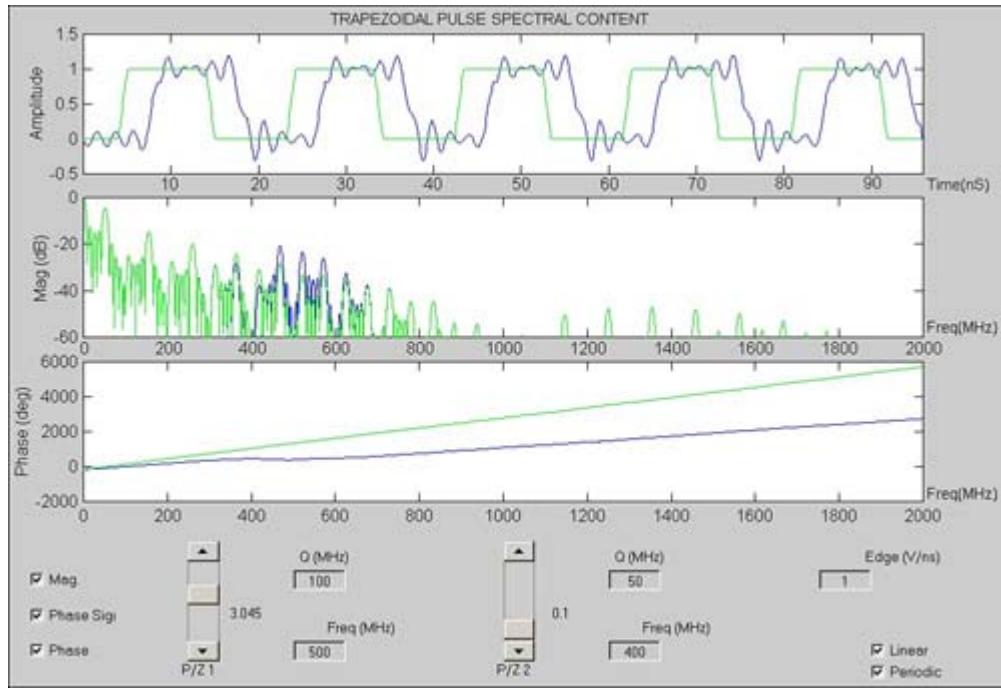
In this example, a pole is added at 500MHz with a Q (width) of 100MHz and a relative amplitude of 3.045; also a zero is added at 400MHz with a Q of 50MHz; the effects on a 1V/ns edge are shown. Also, note that the falling edge is 0.5V/ns. The effects on the rising edge are significant, where as the falling edge does not require the bandwidth that the leading edge does and is not impacted as much.

This example represents the type of information obtained in the frequency domain (the bottom two plots) and how it can be interpreted.

A similar example can be observed (same poles/zeros) when the waveform has been extended (periodically). Note that the spectrum is now much more complicated and Inter Symbol Interference can now play a major role. Figure 5.12 shows the properties of the Fourier transform—pulse train.

Figure 5.12. The properties of the Fourier series for pulse train

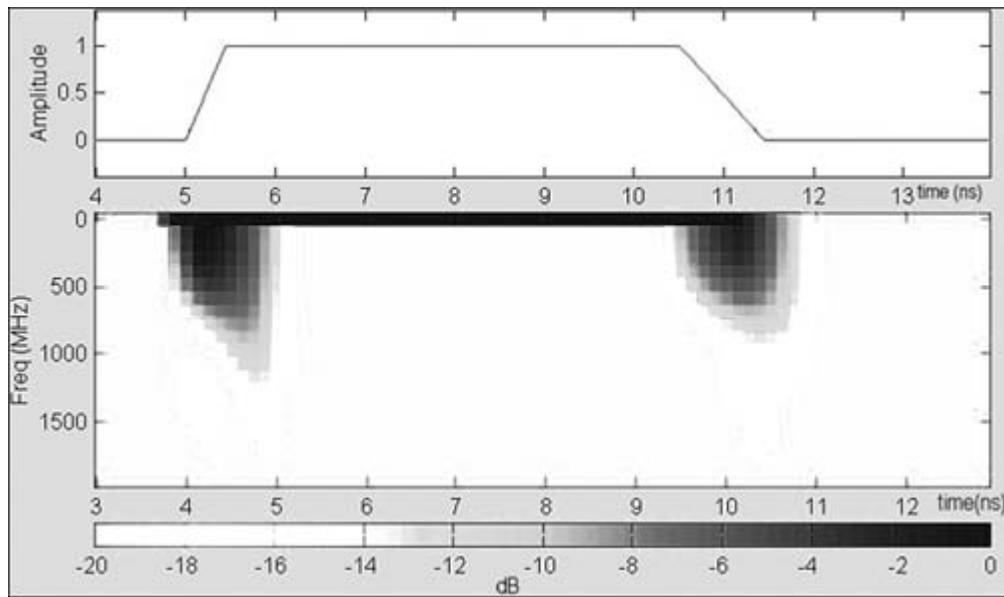
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This brings up an important concept for the interpretation of spectrum. It was shown earlier how pulse width modulates the spectrum. The example in [Figure 5.12](#) is similar to a pulse train, which also modulates the spectrum. The time domain waveforms with edges (transitions) followed by a DC level in between, could be thought of as sending a burst of frequencies (edge) followed by DC.; However, when we perform a Fourier transform on the entire pulse (or bit pattern), we apparently lose the spectral content for the individual edges. This can be visualized in [Figure 5.13](#), where a short time-interval Fourier transform was performed on the time pulse above it. We see that the leading edge (0.5ns risetime) produces localized burst high frequencies. When this is compared to the falling edge (1.0ns falltime) we see the reduced spectral content. Note that the pulse width did not lower the bandwidth (as predicted in [Figure 5.10](#)), whereas a composite Fourier transform would have lowered it.

Figure 5.13. Short time Fourier transform of a pulse

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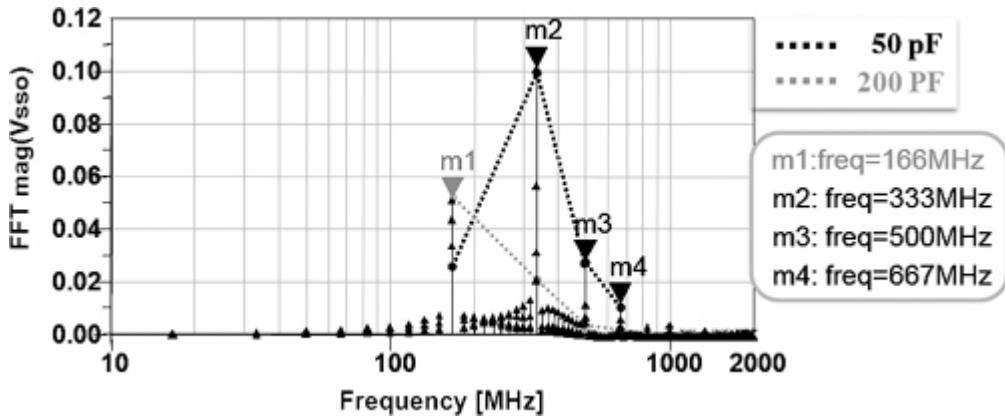


As we modulate (convolve) waveforms, the edge contribution is apparently reduced. This is actually not the case, it is just a result of the modulating waveform emphasizing a certain region (lower frequencies) and this must be accounted for. This impacts the specifications and simulation methodologies needed to correctly interpret the spectra.

5.1.3. FFT of Power Noise

In [Chapter 2](#), “I/O Interfaces,” current profiles in the PDN for various single-ended and differential systems are shown. This current goes through the PDN that may have resonances in the impedance response. As a result, the noise is produced in the PDN. [Figure 5.14](#) shows one example of the PDN noise of which the FFT is taken. It demonstrates the SSO noise spectrum of DDR333 with a pattern 101010. The major frequency components are 333MHz as the second harmonic of the data signal, 167MHz being the fundamental frequency, 500MHz as the third harmonic, and 666MHz as the fourth harmonic. Similarly for the DDR800, we could expect that the major components are 400MHz, 800MHz, 1200MHz, and 1600MHz, respectively. [Figure 5.14](#) shows two cases of on-chip decoupling capacitors: 50pF/IO and 200pF/IO. Various frequency components are visible in the frequency domain FFT plot. For 200pF/IO, the major component seen is at 167MHz. For 50pF/IO, the major component seen is at 333MHz; however, there are also other components such as 500MHz and 667MHz. For higher on-chip capacitance, the impedance at higher frequency is low, and hence, in turn, the power noise at the higher frequency is low. Therefore, for 200pF/IO case, the prominent frequency seen is 167MHz, and other frequencies have low magnitude. The intent of this graph is to show various frequency components in the power noise. In comparison with the dark dotted line of the 50-pF decoupling capacitor per each buffer, the light dotted line represents that the on-die decoupling capacitor is effective for high-frequency noise reduction.

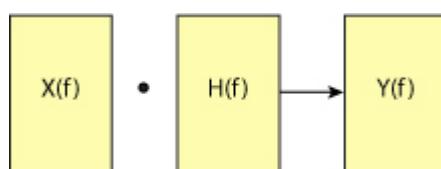
Figure 5.14. FFT of PDN noise (measured)



5.1.4. Convolution and Filtering

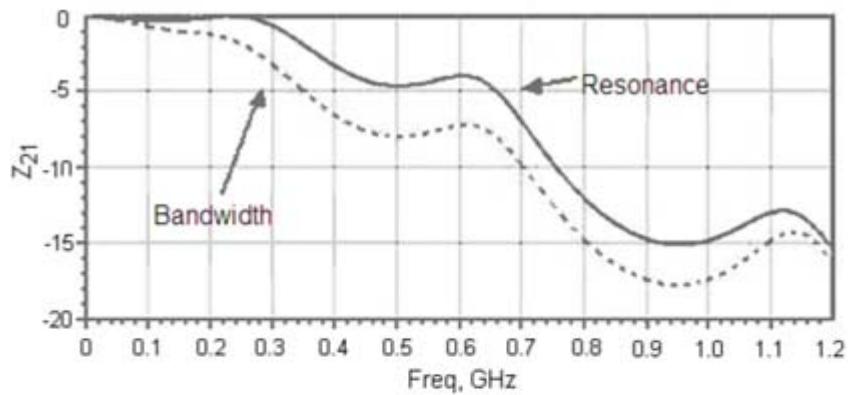
Consider that when the time domain input waveform $x(t)$ passes through a system with transfer function $h(t)$, it results in the time domain output waveform $y(t)$. These $x(t)$ and $h(t)$ time domain functions are integrable with Fourier transforms resulting in $X(f)$ and $H(f)$. The functions $X(f)$ and $H(f)$ are frequency domain representations of the input waveform and transfer function, respectively. The Fourier transform of the convolution is $Y(f) = F\{x(t) * h(t)\}$, where F is the Fourier operator and $Y(f)$ is output waveform in frequency domain (see [Figure 5.15](#)). $Y(f)$ is the product of Fourier transforms $X(f)$ and $H(f)$, thus, $Y(f) = X(f) H(f)$.

Figure 5.15. Signal and system frequency response

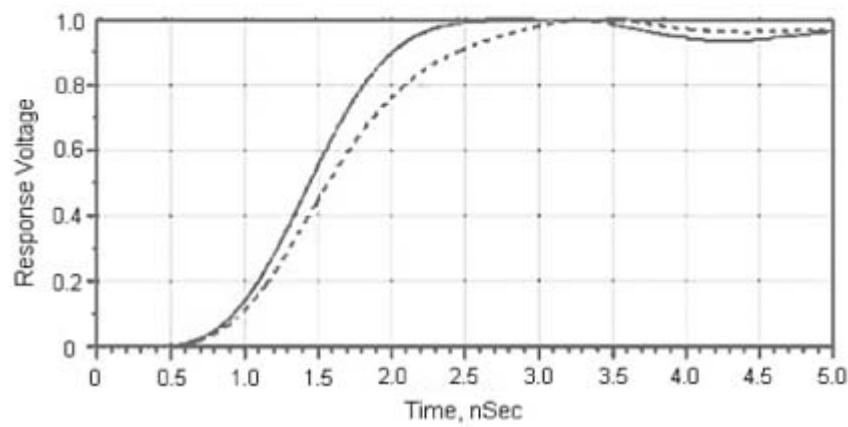


It is important to realize that filtering is also a convolution. An example is shown in [Figure 5.16](#), where a step response is convolved with the transfer function of a channel. The upper plot shows the transfer function $H(f)$, which is obtained in the frequency domain, for two cases of a topology. The lower plot is the time domain waveform of the transfer function convolved with a step response. Mathematically, this is the output waveform $y(t) = \text{IFFT}\{X(f)H(f)\}$, where $X(f) = 1/(j*2\pi f)$ and $H(f)$ is the transfer function. It shows that a larger bandwidth transfer function produces a faster edge rate. Note this can also be viewed from the filtering standpoint, in that $H(f)$ is the low-pass filter response.

Figure 5.16. Convolution example



(a) Magnitude of frequency domain transfer impedance



(b) Convolved time domain step response

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5.2. Signal and Power Integrity Applications

Frequency domain techniques can be effectively used in signal and power integrity applications. Scattering parameters are commonly used for the frequency domain analysis. Electromagnetic simulation tools have S-parameters as output, for signal nets and for power nets. S-parameters can be converted into Y- or Z-parameters as discussed in [Chapter 3](#), "Electromagnetic Effects." The following section lists the commonly used S- and Z-parameters for signal and power integrity analysis:

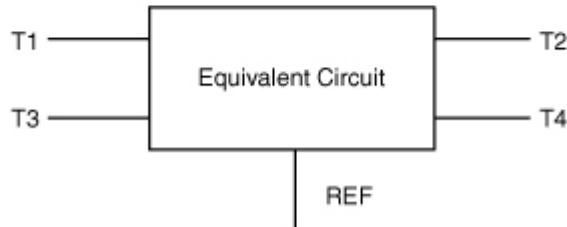
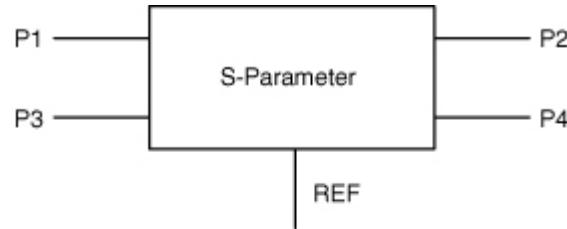
- **Self-impedance of the power net:** Z_{11} represent the self-impedance of the power net, which is the primary design parameter for PDN design in the frequency domain. It is corresponding to the PDN noise in the time domain.
- **Coupling from other power nodes:** If two different ports connect to the same power domain at different locations, Z_{21} represents the transfer impedance of the power net. It is an indicator of coupling from power node 1 to power node 2. This coupling factor can be used in SSO analysis.
- **SSO in frequency domain:** Typically, the SSO is the time domain phenomenon, however, it can also be analyzed in the frequency domain. Z_{Tot} is the total impedance for a node on a distributed PDN. It accounts for self-impedance Z_{11} and the summation of transfer impedances Z_{21} from the neighboring nodes. This is useful for determining the SSO impact in the frequency domain. One of the assumptions is that the amplitude and phase of the currents on different nodes are similar.
- **Coupling between two power domains:** If the port 1 connects to one power domain and port 2 connects to other power domain, the coupling between them is determined by the voltage transfer function Z_{21} / Z_{11} . It is corresponding to the domain-to-domain noise coupling in the time domain.

- **Power-to-signal coupling:** If the port 1 connects to power net and port 2 connects to signal net, transfer impedance Z_{21} describes the coupling from the power to the signal net. Power-to-signal coupling can be determined at different locations such as a chip location or PCB location.
- **Return loss:** If the port 1 connects to the signal net, the return loss of a signal net is characterized by S_{11} . It is corresponding to the reflection coefficient at port 1.
- **Insertion loss:** For a signal net, if the port 1 connects to the driver end and port 2 connects to the receiver end, the insertion loss of the signal net is S_{21} .
- **Crosstalk:** Transfer impedance (Z_{12}) is an indicator for crosstalk between two signal nets. It is especially true for signaling schemes where the current is flowing on the transmission line to the far end. The voltage coupled to adjacent signal net due to the current in a given signal net is determined with Z_{12} . Consider that the nets A and B are routed from the driver to receiver. Port 1 is connected to the net A and port 2 is connected to the net B. For the near end crosstalk, port 1 and 2 are on the same side (for example, driver side). For the far end crosstalk, port 1 is on one side (for example, driver side) and the port 2 is on the other side (for example, receiver side).
- **ISI:** Voltage transfer function is an indicator of an ISI. It is determined by Z_{21} / Z_{11} , where port 1 connects to the driver side signal net and port 2 connects to receiver side of the same signal net. Typically it is recommended to have a flat voltage transfer function in the given frequency range of operation.

5.2.1. S-Parameters with Global and Local Ground

For a signal or a power port, there is a positive and a negative terminal. In some simulators, all the negative terminals connect to a certain reference point. These simulators have separate ports for signal and local ground, as shown in Figure 5.17.

Figure 5.17. S-parameter model with local ground ports

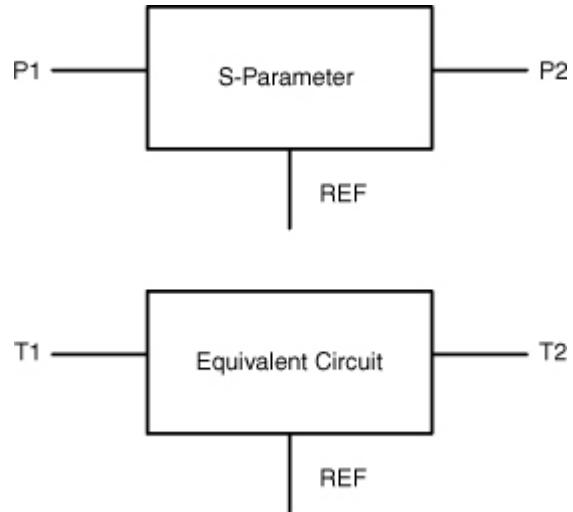


There is a signal at port P1 with its reference at port P3. At the far end, the signal is at port P2 with its reference at port P4. For example, this network is generated for a signal net on the PCB from the driver end (port P1) to the receiver end (port P2). This signal is referenced to the ground. Port P3 is connected to the local ground near port P1, and port P4 is connected to the local ground near port P2. All the negative terminals of ports P1 through P4 are connected to the reference terminal. The resultant S-parameters for this net have four ports and a reference node.

When the equivalent circuit is created, it will have four terminals, T1 through T4, corresponding to P1 through P4, along with a reference node. This reference is typically connected to the global ground of the circuit simulator. The global ground is a reference point for all voltage measurement in the system that it becomes ideal sink for all currents. In this type of S-parameters, the voltage variations between different grounds (driver side ground and receiver side ground) can be analyzed.

Often, the delta variation between a signal or power port and its reference node is adequate for the analysis. In the lab, when measurements are performed, they always reference to a local ground. For the second type of S-parameters, there are only terminals for signal or power nets, as shown in [Figure 5.18](#).

Figure 5.18. S-parameters model without local ground ports



In this example, the negative terminal of the port is connected to a closest point on the return path. The positive terminal of port P1 is connected to signal (driver end), and the negative terminal connected to the local ground, where the positive terminal of port P3 was connected before. Similarly, the negative terminal of port P2 connected to the local ground, where positive terminal of port P4 connected before. The resultant S-parameters have only two ports with a reference node. The equivalent circuit has two terminals with a reference node. In this type of S-parameters, the reference node is arbitrary and does not have any physical meaning. The advantage of this type of S-parameters is that it has a lower number of ports. The disadvantage is that it cannot measure the response from one local ground node to the other local ground node.

When using different types of S-parameters in a circuit simulator, proper care has to be taken to connect the local ground ports, if any, and the reference ports [1]. Consider that there are two different types of S-parameters to be used in a system simulation. The first one is, for example, for the on-chip PDN and has the power ports and local ground ports, with a reference node, as shown in [Figure 5.17](#). Second set of S-parameters, for example, is for the package PDN, which has only power terminals with a reference node, as shown in [Figure 5.18](#). When using these two different types of S-parameters, one cannot connect all the local ground ports from the on-chip PDN S-parameters to the reference node of the package PDN [2]. It will imply that all the local ground terminals for the on-chip PDN are shorted, which is not accurate. One of the ways to make the models compatible is to regenerate S-parameters of the on-chip PDN with only power ports. It can be done by taking the S-parameter model for the on-chip PDN and redefining the ports. For example, the on-chip model with ports P1, P2, P3, and P4 is converted to the newer model with ports P1 and P2, whereas the negative terminals of ports P1 and P2 are connected to local grounds. The newly generated S-parameters have a reference node that can be connected to the reference node of the package S-parameters.

S-parameters can be expressed in the Touchstone® format. S-parameters have the port impedance, but Y- and Z-parameters are independent of port impedance. For the signal net, the typical port impedance is 50Ω . This 50Ω is typical for RF designs, and the traces on the PCB are typically designed to have a 50Ω characteristic impedance. For the power net, the characteristic impedance is much lower than 50Ω . In the Touchstone® 1.0 format, only one value of port impedance can be used for all the ports; however, for Touchstone® 2.0, different port impedances can be used for different ports [3].

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5.3. Power Distribution Network Design in Frequency Domain

The important design parameter for the power distribution network design in frequency domain is the self-impedance or Z_{11} .

Equation 5.3

$$Z_{11} = \frac{V\Delta v}{I_{\max} - I_{\min}} \quad [4], \text{ with other ports open}$$

Where Z_{11} = Self-impedance

V = Power supply voltage

Δv = % Ripple

$I_{\max} - I_{\min}$ = Transient current

Z_{11} is a single port parameter and shows the relationship between the resultant voltage at the PDN port due to the input current at that port. Input current for the PDN is transient in nature and may contain different frequency components. It depends on the circuit blocks on the power domain. As shown in Chapter 2, the I/O interface has different circuit blocks such as

- **Logic circuits:** The interface with the core.
- **High speed I/O circuits:** These circuits include clocking circuits and circuits for prior to final stage.
- **Final stage circuits:** Comprise driver and receiver circuits.

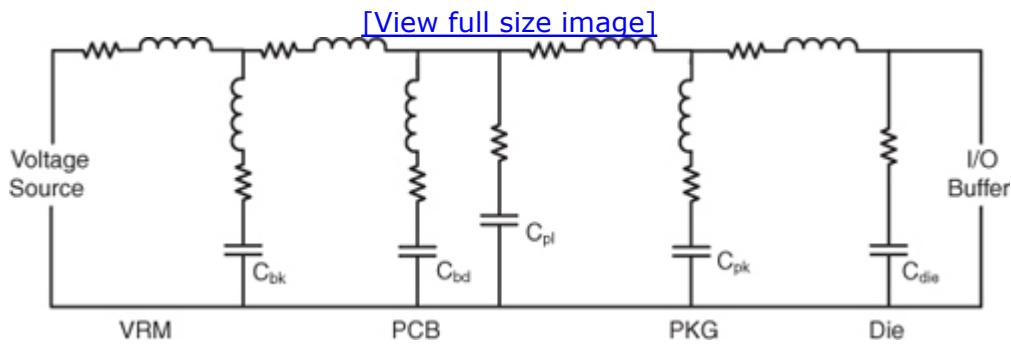
For an I/O interface, the designer may choose to have only one power domain for all these blocks. If some blocks are sensitive to noise, the designer may choose to have separate power domains for those blocks. It

depends on the cost-performance trade-off because a different domain implies that there will be a different regulator and different routing schemes. In some applications, there may be the same domain on the PCB but separated out through a filter before going to the package.

5.3.1. Impedance Response Z_{11}

As shown in the [Chapter 3](#), there are different peaks due to the resonances in the power deliver network. A simplified RLC network of the entire power delivery network is shown in [Figure 5.19](#).

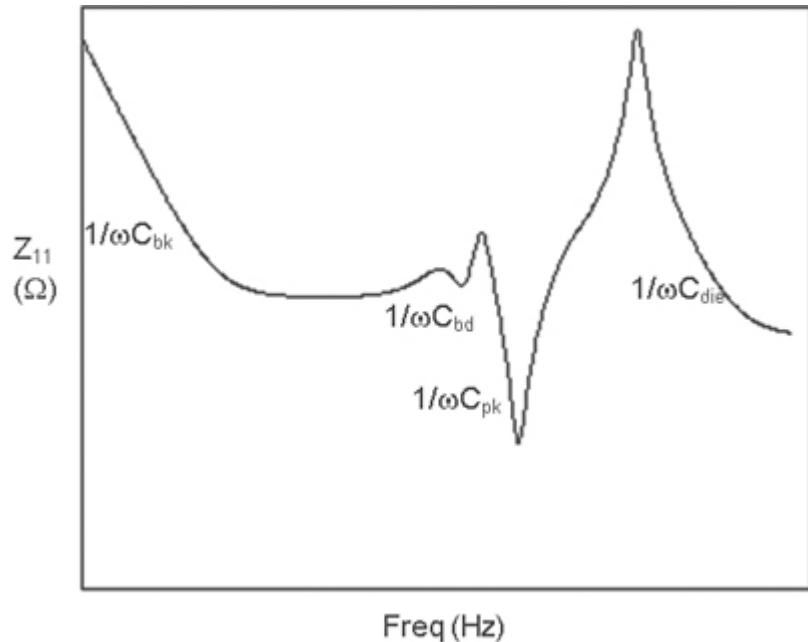
Figure 5.19. Simplified power delivery network



There is a voltage source and corresponding inductance. Then on the PCB there is a bulk capacitor C_{bk} and a ceramic capacitor C_{bd} . Then there is a package capacitor C_{pk} . C_{pl} illustrates the plane-to-plane decoupling capacitor on the board and package. Then there is on-chip capacitor C_{die} . There are resistances and inductances in between the capacitors. This inductance is similar to spreading inductance of the plane, as described in [Chapter 4](#), "System Interconnects."

[Figure 5.20](#) shows the Z_{11} plot looking from the die of the I/O buffer. This plot is generic in nature and in the preceding network; only 1 bulk capacitor, 1 edge capacitor, and 1 package capacitor is used for illustration purposes. This is the open circuit response probed at the die. Three resonant peaks are shown in the figure. Voltage source is not used, so the impedance is very high at the DC point.

Figure 5.20. Self-impedance of the PDN



Effective frequency range of board edge capacitor is from 1MHz to tens of MHz. The first slope is due to the bulk capacitor C_{bk} , which is effective in the kHz to MHz range. It has a flat response at low frequencies. The effective frequency range of the board ceramic (edge) capacitor is from 1MHz to tens of MHz, and the package capacitor is from tens of MHz to a few hundreds MHz. The chip capacitor can be effective all the way to a very high frequency range. The first resonant peak is due to the board inductance and the board ceramic capacitor C_{bd} . The second resonant peak is due to the board and package inductance and the package capacitor C_{pk} . The package inductance in this case is from the package BGAs (connection point to the board) to the package capacitor. The third and prominent peak is due to the package inductance and die capacitance. This inductance is from the package capacitor to the die. With proper design and decoupling capacitor optimization, these peaks can be reduced or shifted.

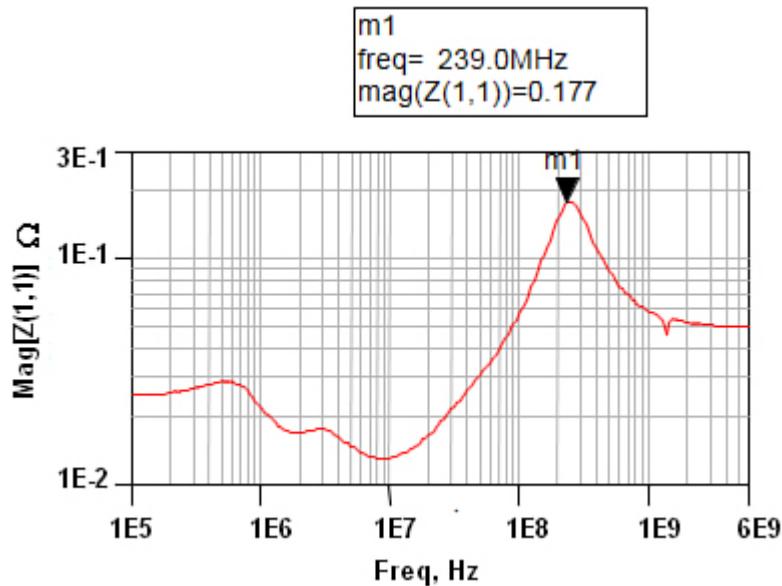
C_{pl} , the plane capacitance, is low in value and is effective for high frequencies. In the preceding network, the impedance is probed at the die location, and the C_{pl} is separated inductively from the die. Also, there is the C_{die} that has much more value than C_{pl} . Therefore the effect of this C_{pl} capacitor is overshadowed when looking from the die. However, if we probe only the impedance on the board or package, the effect of C_{pl} will be more vivid. When 3D or planar 3D electromagnetic models are used for the board and package, the effects of C_{pl} and spreading inductance are captured accurately.

When the voltage source or VRM is used, the low frequency impedance is short circuit or very low. With multiple bulk and ceramic capacitors, the first two peaks can be reduced substantially. Consider that with the optimized

capacitors on the PCB, package and die, the impedance response looking from the die is as shown in [Figure 5.21](#). The maximum impedance at the resonance is about 0.18Ω [5]. For this simulation, planar 3D electromagnetic models for the package and PCB PDN are used.

Figure 5.21. Z_{11} of the optimized PDN

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



5.3.2. Impedance Targets for I/O Interface

To determine the impedance target, it is important to evaluate the time domain response to different excitations. The noise is simulated at the die location when different excitations are subjected to the preceding power delivery network. In the frequency domain, the following PDN impedance formula can be used:

Equation 5.4

$$Z_{11}(f) = \frac{V(f)}{I(f)} \text{ (all other ports open)}$$

Where the following are the function of frequency

$Z_{11}(f)$ = Impedance

$V(f)$ = Voltage noise

$I(f)$ = Current

Equation (5.4) also can be written as

Equation 5.5

$$v(t) = \text{Inv.FFT}(Z_{11}(f) \times I(f))$$

In the preceding equation, the phase and amplitude of the impedance and current need to be considered. When there is only one frequency at 240MHz, 1A peak-to-peak current produces 180mV peak-to-peak noise, as Z_{11} at that frequency is about $180\text{m}\Omega$. If the nominal voltage is 1.5V, the 180mV peak to peak will be $\pm 6\%$. In other words, if the required tolerance is $\pm 6\%$ for 1.5V nominal voltage, then at 240MHz the impedance requirement is about $180\text{m}\Omega$ (assuming 1A of current at that frequency). However, the currents in PDN are more complex in nature, as shown in Chapter 2. In view of this, the impedance target needs to be calculated taking into account the overall spectrum. The impedance target can be frequency-dependent; however, looking into the chip, the worst-case target impedance is calculated and can be applied to the wide band of frequencies.

There are different methods to achieve the target impedance on the PCB. In the Deep V method, the same capacitor type is used in multiple numbers to achieve a deep V shape [6]. In a second type of method to achieve target impedance, about three capacitors are used per decade of frequencies. In the third method, known as Frequency Dependent Target Impedance Method (FDTIM), the capacitors are selected at each value to achieve a flat line at target impedance. For the core circuits, the PCB capacitors may be high in number [6], however for the I/O interfaces, the PCB capacitor number is lower than that for the core. The impedance target at the chip or die can be achieved with co-analysis of the PCB, the package, and the chip PD network.

The PDN impedance target depends on the required voltage tolerance and current in the power domain. If only the final stage circuits are connected to the power domain under design, the current in that domain is computed by taking into account the possible activity for all the drivers and receivers in the final stage. If there is more than one stage connected to the same power domain, the combination of all the currents and their worst-case activity need to be considered.

5.3.2.1. Single-Ended Driver

As shown in Chapter 2 for a single-ended driver, current in the power and ground varies in accordance with the bit pattern. The pattern can match the PDN resonance pattern at the highest peak, which is in the 100s of MHz range. Suppose the maximum data rate is 1600MT/s, and there is a half rate clock (800MHz), then the pattern 1111000011110000 has frequency of 200MHz. It is close to the resonance frequency of the PDN described in the

previous section. To determine the impedance target of the single-ended system, the worst-case pattern is considered. The current in the power domain may have different frequency contents [7]. The current is determined in the PDN for the entire interface, and its FFT is taken. From the FFT, the spectral contents are identified. The impedance target is determined based on the energy at particular frequency.

In an alternative approach, a preliminary power delivery network is constructed. The current profile is determined for the entire bus when all the bits are switching simultaneously at the resonance frequency. Then this current is subjected to the simple power delivery network model, and the noise is determined. If the noise level is higher than expected, some key elements such as an on-die capacitor is changed in the simple power distribution network model. In some iterations, the desired amount of noise is obtained, and the impedance target is determined. In general, the impedance is highest at the chip-package resonance frequency, so the impedance target has to be met at that frequency.

5.3.2.2. Differential Driver

For a differential system, there are different types of differential drivers, such as pseudo differential and half differential, as shown in [Chapter 2](#). For both of these driver types, the PDN current is typically at high frequencies for normal operation. There is little variation in the current depending on the data pattern. However, whenever there is a “power on” for a differential bus, there is a big step for the current [8]. After this step, there is a normal operation current. For determining the impedance target for a differential system, two scenarios need to be considered. First is the normal operation condition. In this condition, the bus runs at a normal operation and has a PDN current at the bus operation frequency, say 2.5GHz. The PDN impedance at 2.5GHz needs to be considered. In the second scenario, the bus is powering on or off. In this scenario, there is a DC step of current. There is droop when the buffers are powered on, and there is a bounce when the buffers are powered off. This droop or bounce magnitude is dependent on the amplitude of the Z_{11} at the PDN resonance. After the droop or bounce, there is a ringing before the noise settles down. This ringing frequency is dependent on the resonance frequency of Z_{11} .

5.3.2.3. Prior Stages

Clocking circuits are part of high-speed I/O circuits for single-ended and differential system. The different clocking schemes such as Phase Locked Loop (PLL) or Delay Locked Loop (DLL) can be used. The current in the power domain for those schemes depends on whether the clock is single-ended or differential. The current varies in the PDN of the clock circuits according to the topology. Although final stage driver circuits may switch at different data rates, clocking circuits have only specific data rates.

Other examples of high speed I/O circuits before the final stage are a phase interpolator, a parallel to serial converter, a predriver, depending on the interface. The change in current in the power domain for these circuits may or may not be data-dependent. There is also logic block in the I/O interface, which communicates with the processing unit. The activity for the logic associated with this block is determined to get the current in the power domain.

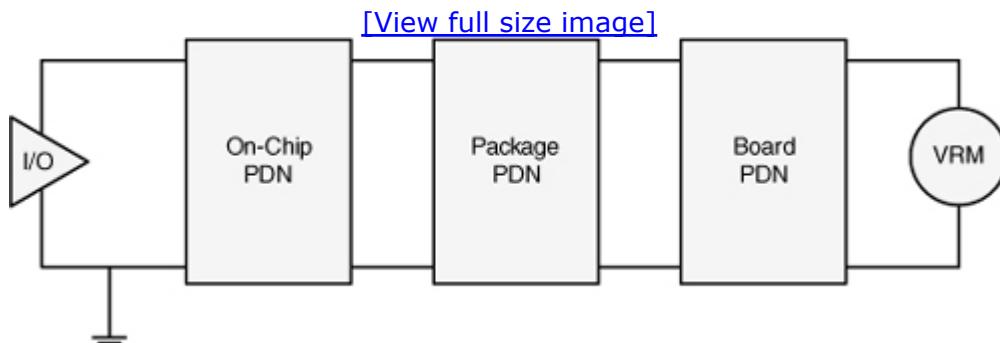
If the final stage and other stages are on the same power domain, then the current profile in power domain may have a variety of different frequencies. Consider a PDN comprising of a PCB, a package, and a single-node die model. The target impedance, looking from the die location, serves as a preliminary design target. In the single-node die model, all the current is injected into one node, and the voltage noise is determined. In a distributed die model, there is a variation from node to node at different locations of the die.

As shown in subsequent sections, different PDN elements such as the PCB, package, and die influence different frequency range. For individual components, the target impedance needs to be maintained only for the frequency range within which the component can have an effect. As an example, the PCB can influence only up to a few tens of MHz, so the target impedance for the PCB components needs to be maintained within a few tens of MHz of frequency. Beyond that frequency, it may exceed the target impedance, but there are other considerations, such as EMI mitigation.

5.3.3. PDN Design Example

Consider that the impedance target for an I/O interface is determined to be $200\text{m}\Omega$ at the die location. This is much higher than typically required for the core PDN. However, I/O interfaces have much lower current than that for the core. The overall PDN design methodology is similar, but the amount of decoupling may be different. In this example, the final stage driver and some other stages like the predriver are on the same power domain under consideration. As shown in [Figure 5.22](#), the power distribution network comprises the chip, package, and board networks [5].

Figure 5.22. Power delivery network

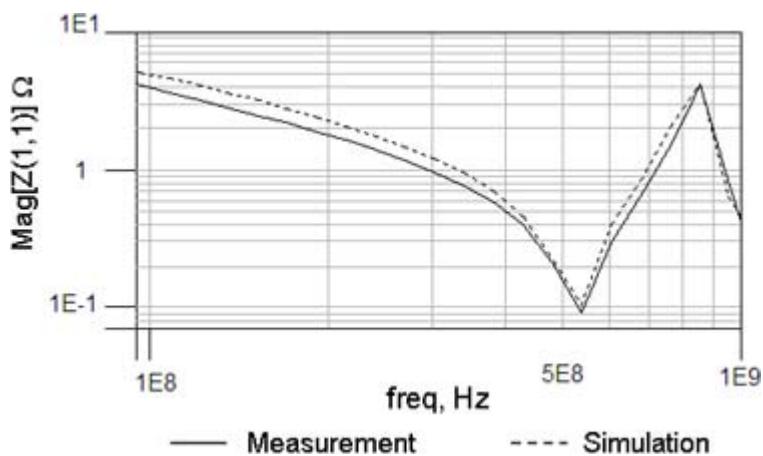


5.3.3.1. Package and PCB PDN

The board and package power distribution networks are modeled using 3D or planar 3D electromagnetic solvers, and S-parameters are extracted. Then, the S-parameters are converted into Z-parameters and plotted for impedance response. The plane-to-plane capacitance and plane inductance is taken into account as the model is an electromagnetic based model. The package Z-parameters response is shown in Figure 5.23.

Figure 5.23. Package PDN: Z_{11} simulation and correlation

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, Md. and R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009, Presentation.



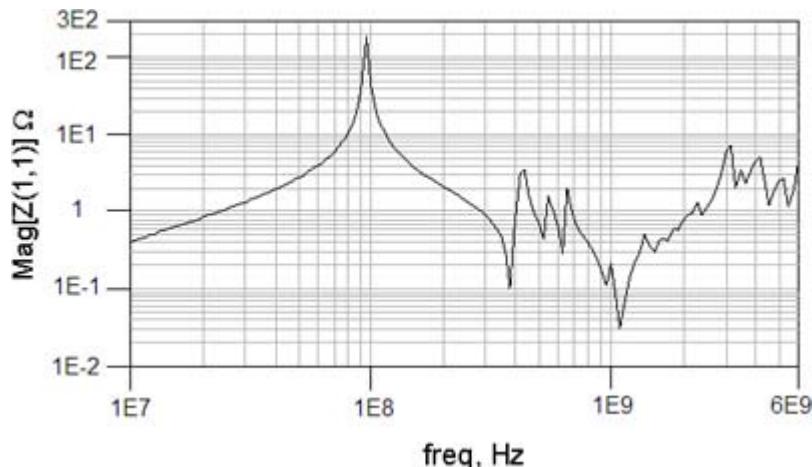
The plot shown in the graph is for the Z_{11} simulated and measured at the package bump location of the power distribution network. The simulator used is a planar 3D electromagnetic simulator. The measurements are done with Vector Network Analyzer using a two-port method [9]. The simulations correlate well with the measurements. This Z_{11} is for a pair of power and ground bumps, and the curve is becoming inductive at 500MHz and again capacitive above 900 MHz. When considering the entire interface for simulations, all the die side bumps are considered as a lumped port. It exhibits lower inductance than that for 1 bump.

Figure 5.24 shows the Z_{11} response at the package bump when the package and PCB are analyzed together. Similar to the package, the PCB is modeled with the planar 3D electromagnetic simulator. It has two ports: the package side BGA and the VRM port. For the first port, the package BGA side power distribution ports on the board are lumped into one port. The VRM bulk capacitor is modeled when extracting the S-parameters for the board. Then, the S-parameters of the board are cascaded with that for the package. There is no other decoupling capacitor than the VRM capacitor.

The self-impedance of the package bump side port shows that for most of the frequencies above 10MHz, the impedance target of 200mΩ is exceeded.

Figure 5.24. Simulated Z_{11} with PCB and the package, no capacitors

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



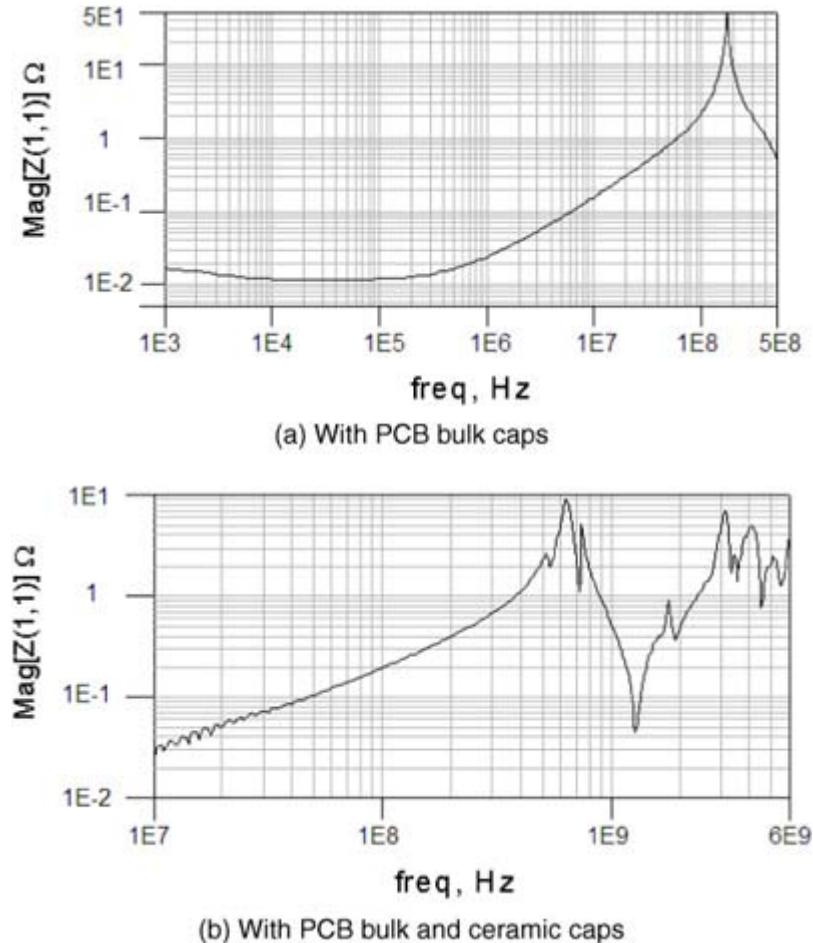
5.3.3.2. PDN Co-Design: PCB, Package and Chip

The design target of 200mΩ needs to be achieved over a wide frequency range. Different decoupling solutions affect different frequency range. The response of the PCB and package PDN, looking from the package bump port shows that the target is not met at many frequencies. In the PDN co-design approach, the PCB, the package, and later the chip simulated simultaneously and decoupling solutions are optimized [5]. First, the decoupling capacitors are placed on the PCB and optimized for the desired frequency response. Bulk capacitors are effective in low frequency from kHz to several MHz, as shown in [Figure 5.25a](#). This impedance is simulated from the package bump side for the cascaded package and board power distribution network. Then the high-frequency ceramic capacitors are placed on the board near the package. Their effective frequency is a few 10s of MHz. With the bulk capacitors and ceramic capacitors on the board, the target impedance is met in the 80MHz of frequency range, as shown in [Figure 5.25b](#). This impedance is simulated at the package bump side in the cascaded package and PCB network. PCB PDN decoupling cannot support high-speed I/O currents, with faster rise times. For that, package level decoupling or chip level decoupling is required.

Figure 5.25. Simulated Z_{11} with PCB + PKG a) bulk caps; b) bulk caps + edge caps

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO

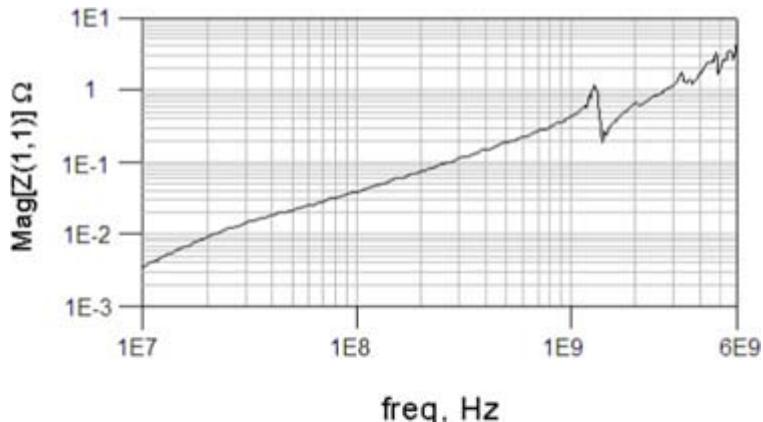
Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



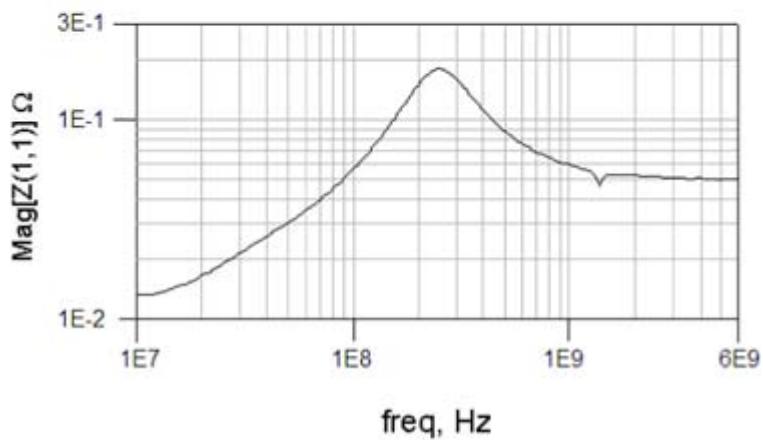
Next, the package capacitors are placed, and the impedance is simulated at the package bump location. The resultant plot is shown in Figure 5.26a. The package capacitors are placed as close as possible to the die bump, so as to minimize the inductance path from the die bump to the package capacitors. The target impedance is met in the frequency range of a few 100s of MHz. Above this frequency range only the chip capacitors are effective. With the chip capacitors, the target impedance of 200mΩ is met over the wide frequency range, as shown in Figure 5.26b. There is a resonance at around 240MHz, at which the impedance is maximum.

Figure 5.26. Simulated Z_{11} with (a) PCB and PKG caps, (b) PCB, PKG, and chip caps

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



(a) With PCB and package caps



(b) With PCB, package, and chip caps

The on-chip PDN model used is shown in Figure 5.27. The on-chip decoupling capacitor is C_{die} and its series resistance is R_{die} . R_{leak} is the leakage resistance for that domain. From the bump to circuit location, there is a power grid with parasitic resistances R_s and inductance L_s . The sensitivity of C_{die}/R_{die} is shown in the Figure 5.28.

Figure 5.27. On-chip PDN model

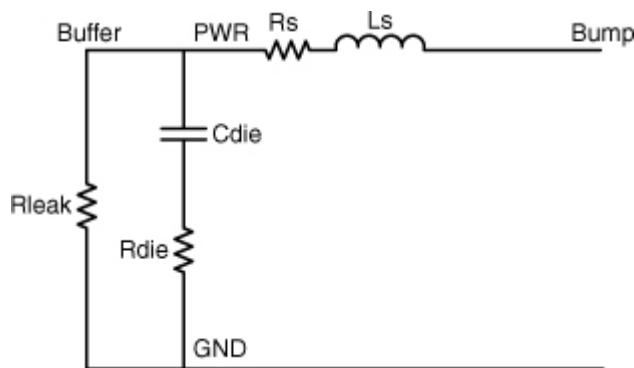
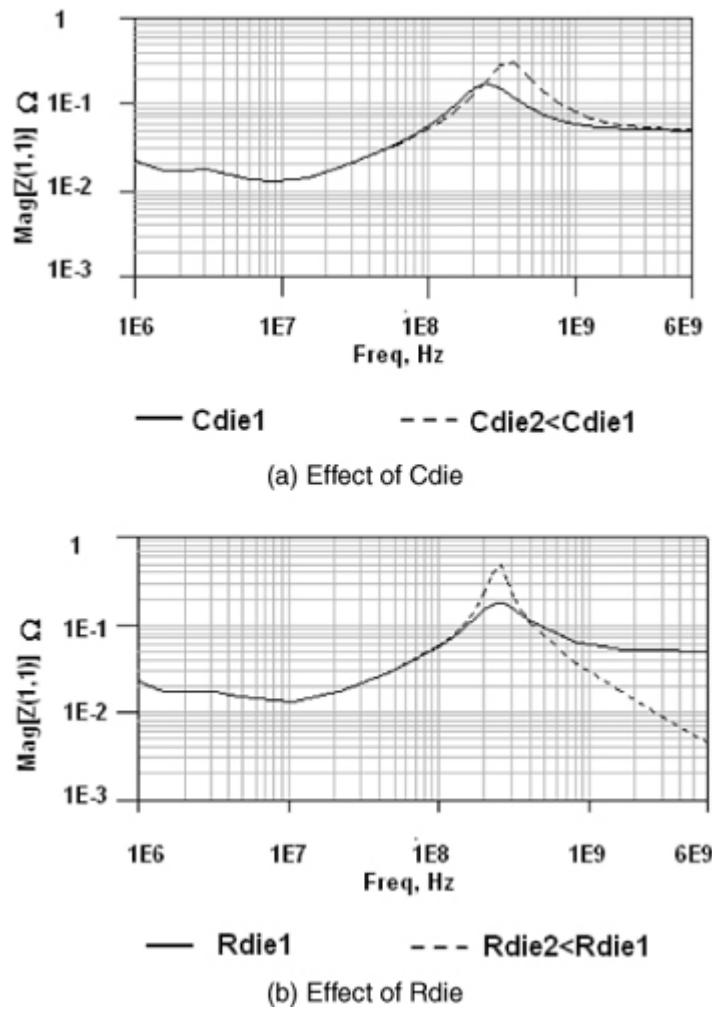


Figure 5.28. Effect of on-chip PD elements on Z_{11} (simulated)

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009, Presentation.



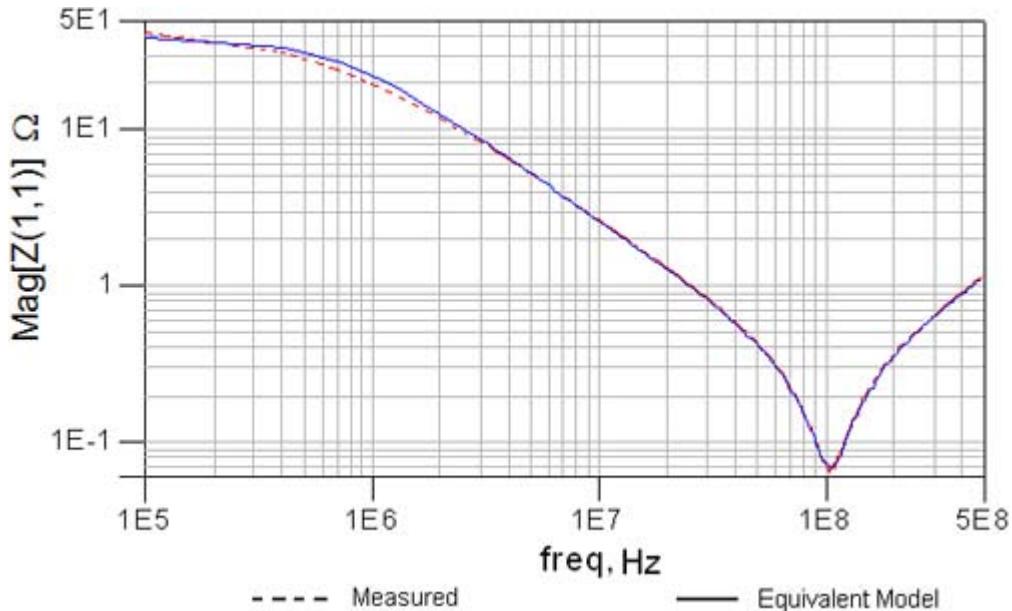
If C_{die} is lowered, the resonance peak increases and shifts toward the right. If R_{die} is reduced, the resonant peak increases, but the high frequency ($>1\text{GHz}$) impedance is lowered. There is a trade-off for the Z_{11} response for high frequency and for low frequency.

5.3.4. On-Chip Power Delivery: Modeling and Characterization

As shown in [Chapter 4](#), the on-chip power delivery network is composed of the power grid, intentional capacitors, and unintentional or intrinsic capacitors. It is difficult to characterize the power delivery network from the die side because there are no access points on the die. Typically, the die mounted in the package is taken, and VNA measurements are done on the package pins. The package capacitors are removed. The package parasitics are de-embedded and the on-chip model can be determined. [Figure 5.29](#) shows the Z_{11} measurement for the package pin and its equivalent model simulations [5].

Figure 5.29. Z_{11} for chip and package

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009



The equivalent model topology is shown in Figure 5.27. In this case, R_s is combination of the grid resistance and package resistance. Similarly, L_s is a combination of grid inductance and package inductance. In the above approach, it is difficult to separate out the R_{die} and R_s from the measured data. Similarly, due to the intentional chip capacitors, the amount of power grid capacitor is difficult to estimate. So, with this approach, the power grid parasitics cannot be easily extracted from the measurement. Also, the C_{die} is a combination of the intentional C_{die} and intrinsic C_{die} . With the measurements described in Figure 5.29, the total C_{die} can be determined.

To characterize the on-chip power delivery network with power grid parasitics, a special test vehicle can be designed. There are intentional on-chip capacitors and intrinsic on-chip capacitors. Power grid capacitance is one of the components of the intrinsic on-chip capacitance; the other components are primarily due to circuits as described in Chapter 4. With this test vehicle, the power grid model and the on-chip intentional decoupling capacitor model can be extracted.

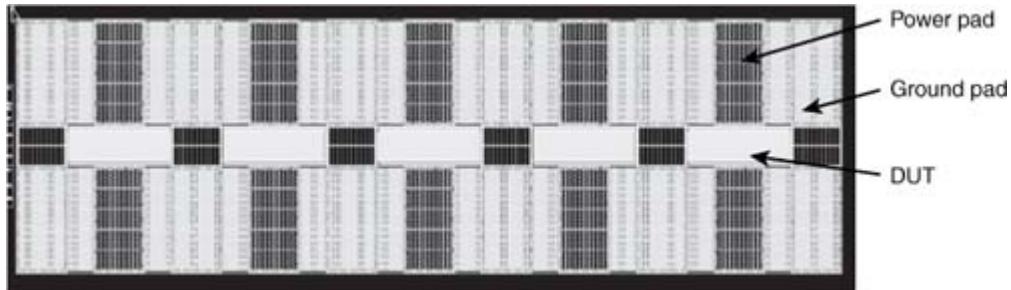
5.3.4.1. Test Vehicle for On-Chip PDN

The on-chip PDN is composed of the power grid and decoupling capacitors. The following section presents a methodology for determining the on-chip PDN models with the test chip. A special test structure is designed to measure the S-parameter response for the on-chip PDN [10]. It has pad

rows for measurement and the device under test, as shown in Figure 5.30.

Figure 5.30. Test Chip: Pad-row with the DUT

Source: V. Pandit, W. H. Ryu, S. Ramanujam, K. Pushparaj, and F. Fattouh, "Simulation and Characterization of GHz on-chip Power Delivery Network," DesignCon 2008.



There are two rows of the pad, and in each row, there are power pads and ground pads. Power pads are surrounded by the ground pads on both sides. All the ground pads are connected together; however, the power pads are isolated from each other. Also, there is a ground shield placed between the power pad and the ground pad. With this arrangement, the noise and extraneous effects are minimized during the VNA measurements up to 10GHz and beyond.

There are different configurations of the test vehicle with the same pad-row structure. In each type, the DUT is different, as described here:

- **Pad-row with the open circuit power grid:** For this structure, the DUT is only a multilayer power grid. This grid is not connected to any capacitor. The size is very small ($<200 \times 200\text{um}$).
- **Pad-row with short circuit power grid:** For this structure, the DUT is a power grid with the power and ground nets of the grid shorted on the lower metal layers.
- **Pad-row with the intentional capacitor:** For this structure, the DUT is a power grid with the intentional capacitor connected at the lower metal layers.

For all the three structures, VNA measurements are performed up to 40GHz. The power and ground pads are used for the VNA measurements. For the open circuit grid, the S-parameter is S_{open} and for short circuit grid, it is S_{short} . With these two measurements, the 2×2 matrix for the power grid S-parameters is constructed. The power grid is assumed to be a symmetric and reciprocal network: $S_{11\text{grid}} = S_{22\text{grid}}$ and $S_{21\text{grid}} = S_{12\text{grid}}$.

Equation 5.6a

$$S_{11grid} = \frac{S_{open} + S_{short}}{2 + S_{open} - S_{short}}$$

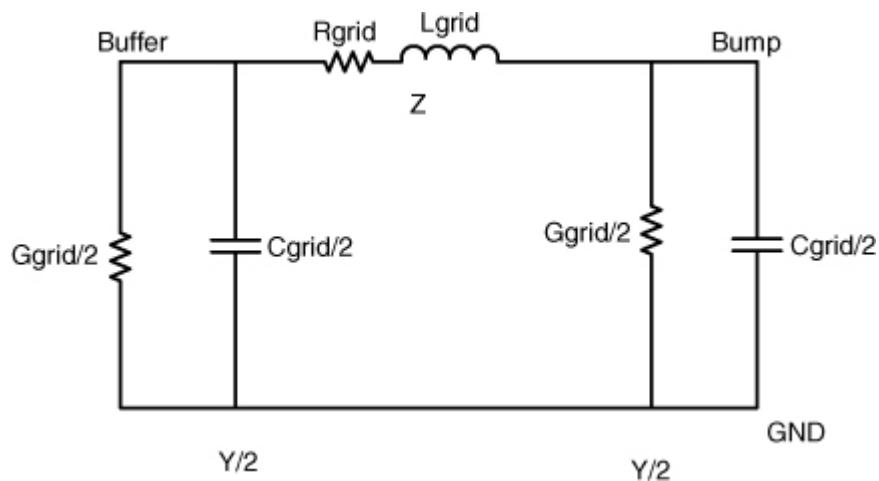
Equation 5.6b

$$S_{21grid} = \sqrt{(S_{11grid} - 1) \times (S_{11grid} - S_{open})}$$

5.3.4.2. 2D TLM Empirical On-Chip PD Modeling Method

From the open circuit power grid structure, the capacitance and conductance of the grid are extracted, whereas from the short circuit power grid structure, the resistance and inductance of the grid are extracted. A simple RLGC model is created with these extractions, as shown in Figure 5.31. This model is similar to the transmission line model, and the power grid can be constructed as a 2-dimensional transmission line matrix (2D TLM).

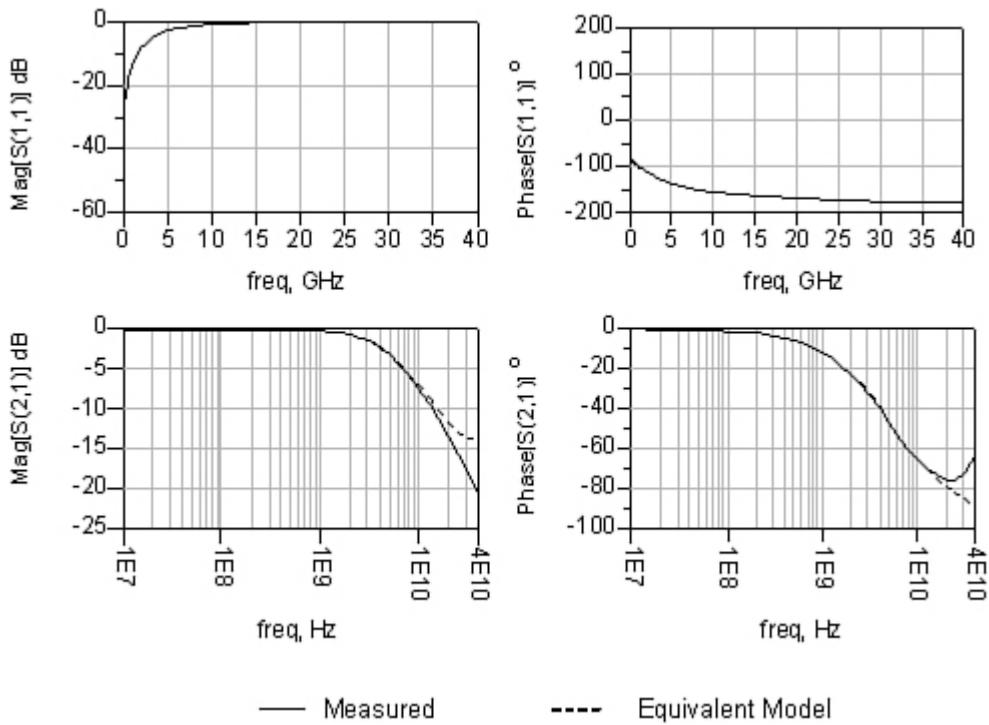
Figure 5.31. RLGC model for power grid



Based on the design of the power grid, initial power grid parameters are determined. The S-parameter response of the power grid are plotted and compared against the measurements. The different parameters are tweaked to fit the response. The final model shows a good correlation to the measured S-parameters up to 10GHz of frequency, as shown in Figure 5.32. Above that frequency, the lumped approximation is not valid.

Figure 5.32. S-parameters for the power grid

Source: V. Pandit, W. H. Ryu, S. Ramanujam, K. Pushparaj, and F. Fattouh, "Simulation and Characterization of GHz on-chip Power Delivery Network," DesignCon 2008.



5.3.4.3. On-Chip Capacitor Model Extraction

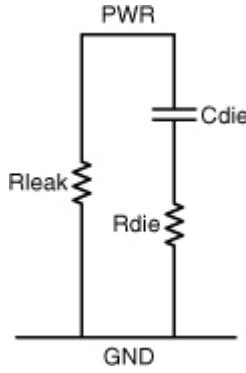
The third type of structure in the test vehicle has an open circuit power grid and the on-chip intentional decoupling capacitor. This is the intentional capacitor that is designed with the transistor circuits. The measurements are done on this structure with the VNA. The decoupling capacitor is connected to the power grid, which in turn is connected to the pad. The S-parameters measured for the power grid + capacitor structure are S_{11tot} . With a 2×2 S-parameter matrix of the power grid, the S_{11} of the decoupling capacitor is computed as $S_{11decap}$:

Equation 5.7

$$S_{11decap} = \frac{S_{11tot} - S_{11grid}}{\left(S_{21grid}\right)^2 - \left(S_{11grid}\right)^2 + S_{11grid}S_{11tot}}$$

A simple model of the transistor type on-die decoupling capacitor is created, as shown in [Figure 5.33](#). It has the intentional capacitor C_{die} , its parasitic resistance R_{die} , and the leakage resistance R_{leak} .

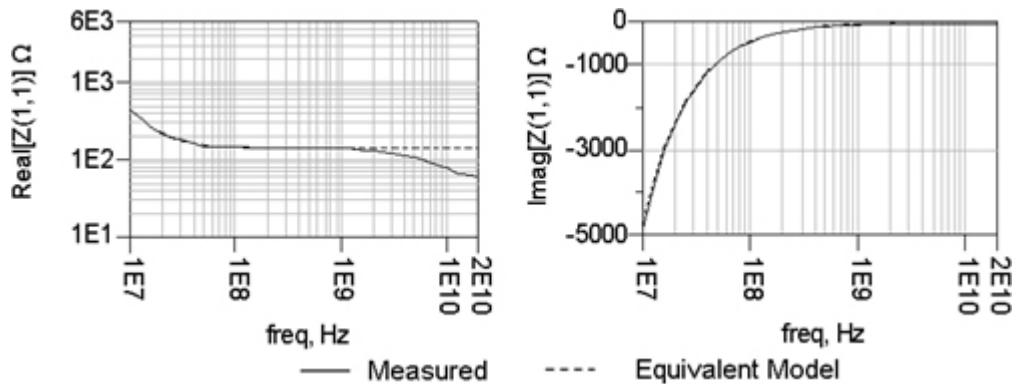
Figure 5.33. Equivalent on-chip capacitor model



Based on the design information, the initial parameters for this model are determined. These variables are changed to fit the curve for S_{11} . As shown in Figure 5.34, it shows a good correlation up to a few GHz range.

Figure 5.34. Z_{11} for on-chip capacitor

Source: V. Pandit, W. H. Ryu, S. Ramanujam, K. Pushparaj, and F. Fattouh, "Simulation and Characterization of GHz on-chip Power Delivery Network," DesignCon 2008.

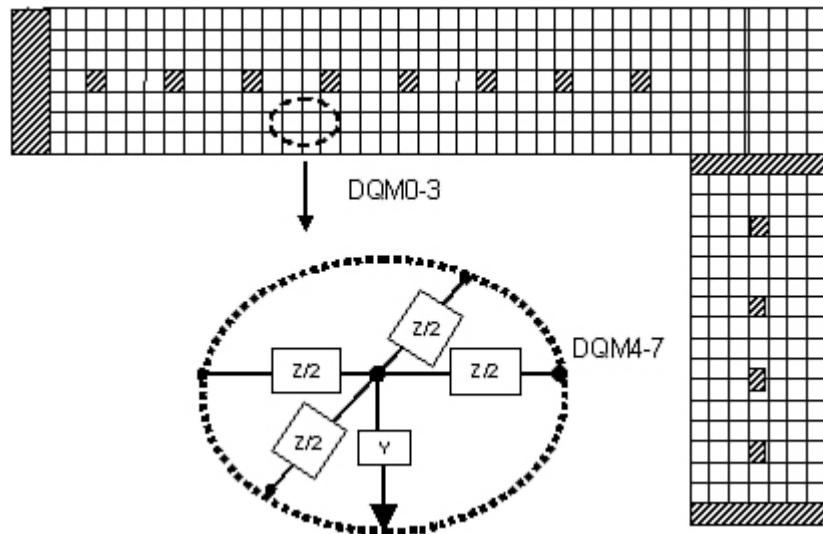


5.3.4.4. Modeling and Correlation for On-Chip PDN of the I/O Interface

As discussed in the previous section, the 2D TLM method for on-chip die model includes the power grid model and decoupling capacitor model. This method can be applied to the on-chip PDN model for the entire interface [11, 12]. Figure 5.35 shows the on-chip geometry for the I/O interface.

Figure 5.35. On-chip geometry for I/O interface

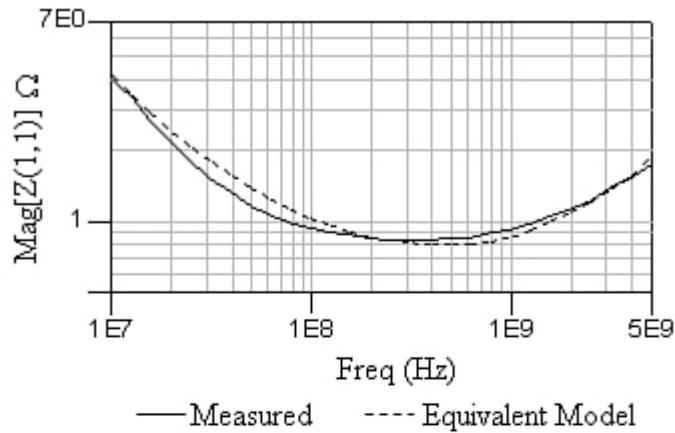
Source: V. Pandit and W. H. Ryu, "Multi-GHz Modeling and Characterization of On-chip Power Delivery Network," EPEP 2008, Poster Presentation. © [2008] IEEE.



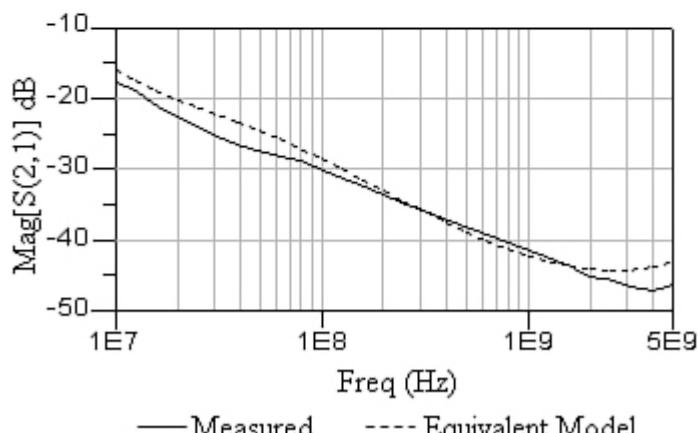
It has different DQ Modules (DQM) as shown. The entire section is divided into different unit cells. Each unit cell is assigned a 2D TLM model as discussed in the earlier section. The unit cells are filled for the entire geometry. The on-wafer probing is performed with the VNA at the bump location. The different PDN bumps are probed and the self-impedance and insertion loss are plotted. The equivalent model with the 2D TLM method shows a good correlation with the measurements, as shown in Figure 5.36.

Figure 5.36. Self-impedance and insertion loss for the on-chip PDN

Source: V. Pandit, and W. H. Ryu, “Multi-GHz Modeling and Characterization of On-chip Power Delivery Network,” EPEP 2008, Poster Presentation. © [2008] IEEE.



(a) Self-impedance



(b) Insertion loss

Note that the self-impedance plot shows the resistance of the network at about 800mOhm. As described in earlier sections, it is a combination of the grid resistance and the series resistance with the on-chip capacitors. Beyond 100MHz the impedance stays flat for a few hundred MHz and then becomes inductive. The insertion loss is measured and simulated from a bump to another bump for the power distribution network. It shows 15dB of insertion loss at 10MHz. It implies that, from one bump to another bump, there is loss of signal at a high frequency. There are a couple of things to be noted. First, the insertion loss is S_{21} , and dependent on the 50-Ohms port impedance. For the power distribution network, the port impedance may be different, and the voltage transfer function needs to be plotted. Second, the bumps may have higher insertion loss dependent on the on-chip routing. The power bumps are typically shorted on the package, so when the package is connected, this insertion loss for the same bumps will be lower. However, this plot is for correlation purposes of the on-chip PDN model and shows a good correlation.

5.3.4.5. EM Modeling of On-Chip PDN

As described in Chapter 3, "Electromagnetic Effects," the electromagnetic

modeling is essential to predict the parasitics of the interconnect structures. It is also applicable for the on-chip power grid. A methodology is developed utilizing quasi-static approximations and is correlated with the on-chip measurements [13].

As described in [Figure 5.30](#), a test vehicle has been created to measure the parasitics of the power delivery network of the silicon. A similar power grid was analyzed by the proposed electromagnetic engine, and results were compared with the measurements. As shown in [Figure 5.37](#) and [Figure 5.38](#), simulated results show good correlation with the measurements in the frequency range up to 5GHz.

Figure 5.37. Power grid impedance correlation

Source: L. Proekt and V. Pandit, “Multi-GHz On-Chip Power Delivery Modeling Method,” DesignCon, 2010.

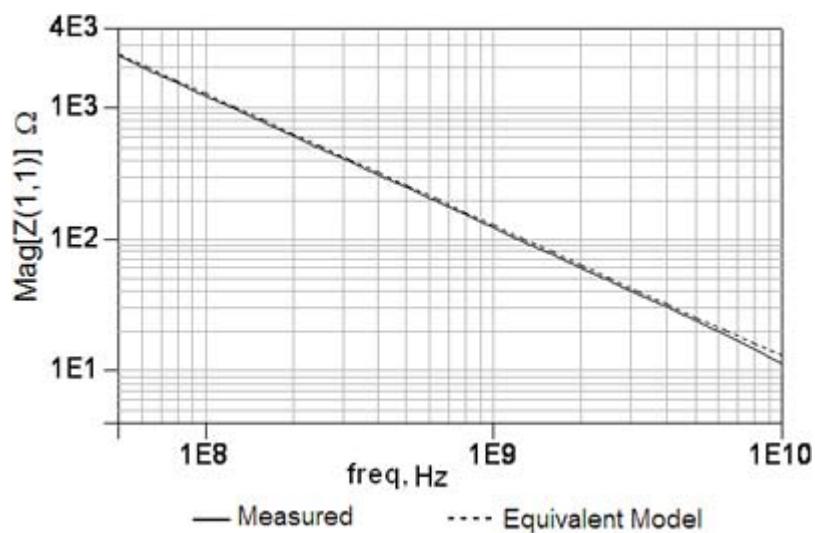
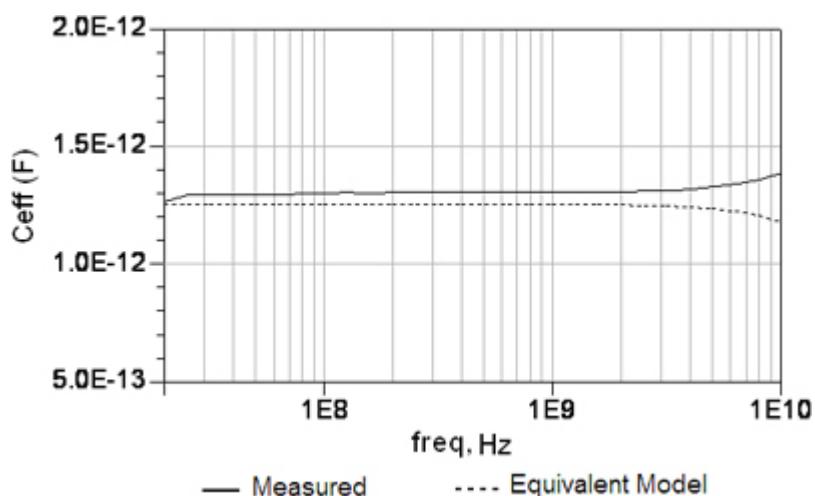


Figure 5.38. Power grid capacitance correlation

Source: L. Proekt and V. Pandit, “Multi-GHz On-Chip Power Delivery Modeling Method,” DesignCon, 2010.



The equivalent model is from the quasi-static EM solver with RC netlist as output. Inductive effects are neglected for the power grid. Beyond 5GHz, inductive effects become noticeable. It was concluded that for the given structure and power grid geometry, the RC model for the power grid is reasonably accurate up to 5GHz of frequency.

5.3.5. Insertion Loss and Voltage Transfer Function

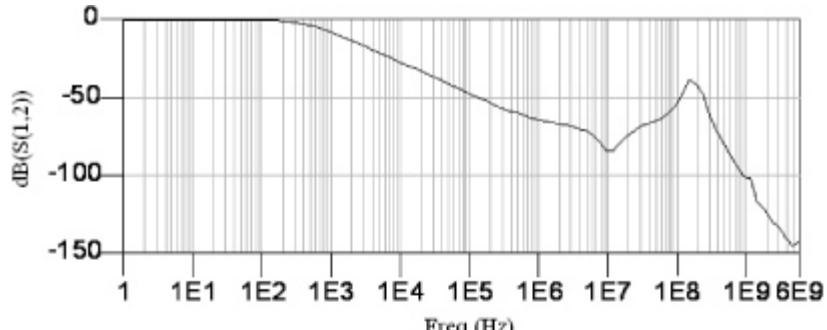
For a signal net, the port impedance of 50Ω for the S-parameter model accurately describes the properties of the net because the typical characteristic impedance of the signal trace is 50Ω . For example, consider that a signal net has 50Ω characteristic impedance. Its S-parameters with 50Ω port impedance show the insertion loss of 3dB at 1GHz. Because the characteristic impedance and port impedance are the same, there will be 3dB loss at 1GHz.

The characteristic impedance of a power net is much lower than 50Ω . Due to resonances in the power net, the impedance may be different at different frequencies. If the S-parameters are generated with 50Ω port impedance, the characteristic impedance and port impedance are not the same for this power net. In view of this, S_{21} will not accurately represent the insertion loss for that power network.

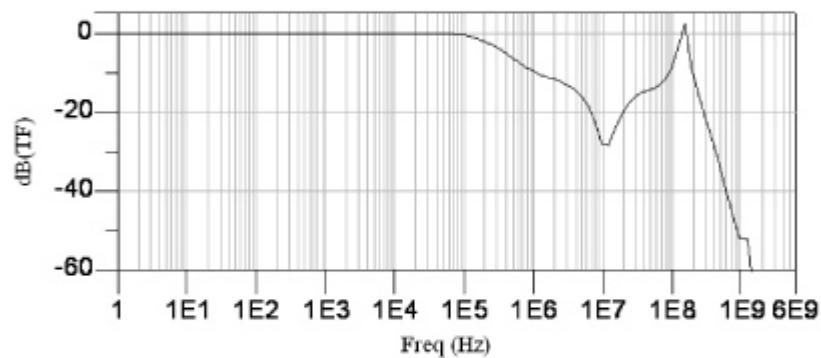
Consider an example in which there are two on-chip power domains that are separated on the board through a filter [14]. Figure 5.39a shows the insertion loss S_{21} from domain 1 to 2. This plot of the S-parameters is with the 50Ω port impedance. It shows that there is an isolation of 40dB around 100MHz. If the impedance parameters such as self- and transfer impedances are plotted, as shown in Figure 5.39c, it shows resonances around 100MHz of frequency. Figure 5.39b shows the voltage transfer function.

Figure 5.39. Voltage transfer function

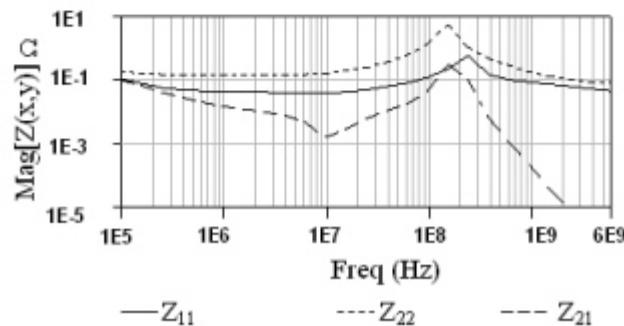
Source M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



(a) Insertion loss



(b) Voltage transfer function



(c) Self-impedance and transfer impedance

The voltage transfer function from port 1 to port 2 is defined as Z_{21} / Z_{11} where Z_{21} is the transfer impedance from port 1 to 2, and Z_{11} is the self-impedance of port 1. Due to the transfer impedance $Z_{21} > Z_{11}$ at some frequencies, the voltage transfer function exceeds 0dB, indicating there is no isolation, but the gain. Because it is a voltage transfer function, it still holds the energy conservation principle. This phenomenon is occurring due to noise transfer (Z_{21}) and its voltage amplification (Z_{11}) due to resonance.

The characteristic impedance of the power delivery network is much lower than 50Ω; therefore, the S_{21} may not represent the isolation between the domains. Also, because of the resonance in the PDN, the noise voltage transferred may get amplified. In view of this, the voltage transfer function is an important parameter to analyze the isolation between the power

domains.

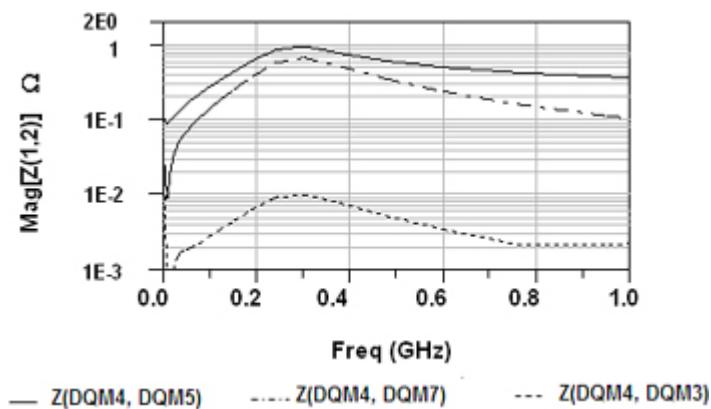
5.3.6. SSO in Frequency Domain

SSO occurs when a number of buffers switch simultaneously. Consider that buffer A is switching with other neighboring buffers. When buffer A is switching, there is a noise produced at the power node. When other neighboring buffers are also switching, the noise level at the power node of buffer A is increased due to noise coupling. The extent of this coupling can be analyzed in frequency domain. This coupling is a function of frequency. It is dependent on the layout of the on-chip PDN.

In the following section, an example of determining SSO in frequency domain is presented [5]. Consider the chip area of $X \times Y$, as shown in Figure 5.35. There are different modules represented by DQM n where n varies from 0 to 7. For this analysis, a distributed on-chip PDN model is considered, along with the package and board PDN models. All these are cascaded together and the resultant model has ports at the chip level corresponding to each DQ module. These ports are for the PDN network, as the coupling from one power node to the other node is analyzed. The victim node is the power node of DQM4. Figure 5.40 shows the transfer impedance from power nodes of different DQM n to DQM4.

Figure 5.40. Coupling from power nets of other modules to DQ4-module

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



The plot shows the transfer impedance from DQM5 to DQM4, which is noted as $Z(DQM4, DQM5)$. It shows frequency variations in amplitude implying that the coupling from the power node of DQM5 to that for DQM4 is different at different frequencies. $Z(DQM4, DQM7)$ shows lower values than that for $Z(DQM4, DQM5)$, implying that the coupling from DQM7 is lower than that from DQM5. In this way, the coupling from different nodes in PDN can be analyzed to the victim DQM4.

To determine the SSO impact, the total impedance at the DQM4 needs to be considered. It is a summation of self-impedance and transfer impedance from all other modules.

Equation 5.8

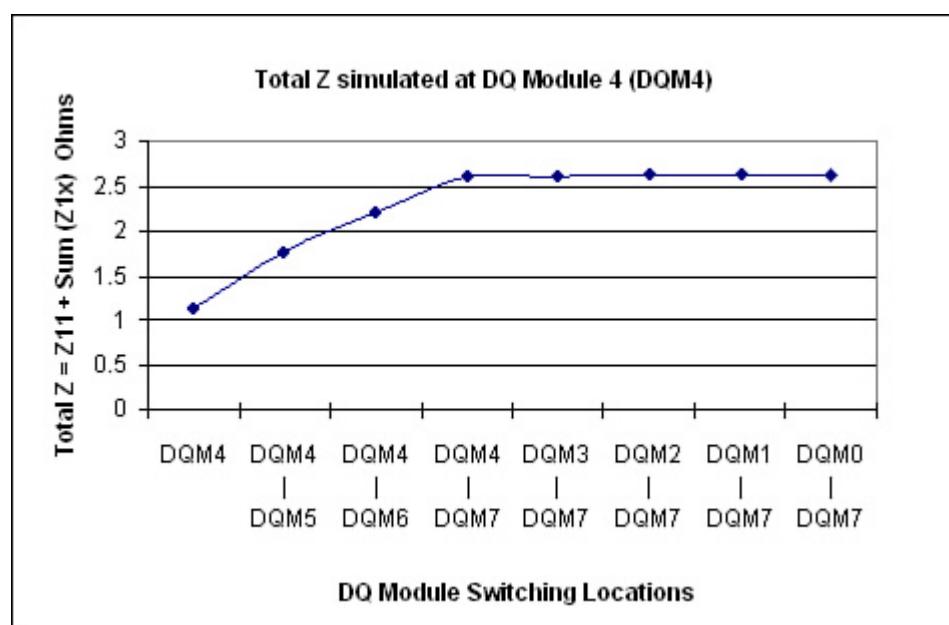
$$Z_{tot}(DQM4) = Z_{11}(DQM4) + Z_{12}(DQM4, DQM5) + Z_{12}(DQM4, DQM6) + \dots$$

$$Z_{tot}(DQM4) = Z_{11}(DQM4) + \sum Z_{12}(DQM4, DQMn)$$

Figure 5.41 shows the summation of self- and transfer impedances at DQM4. The first data point on the x-axis is the DQM4 only. It shows the Z_{11} of the DQM4. The second data point is for $Z_{11}(DQM4) + Z_{12}(DQM4, DQM5)$, and so on. The total Z for DQM4 increases with two modules (DQM4-M5), three modules (DQM4, DQM5, DQM6), and four modules (DQM4, DQM5, DQM6, DQM7). As seen from the plot, the SSO coupling gets saturated after DQM7. The coupling from DQM3 through DQM0 is quite lower and Z_{12} is smaller. It is totally dependent on the on-chip power delivery routing and the floor plan arrangements. This analysis and SSO saturation shows that the coupling from neighboring buffers to the victim buffer is different dependent on the electrical parasitics. The distributed on-chip models are required to determine the coupling and its impact.

Figure 5.41. Total impedance (self + transfer)

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009.



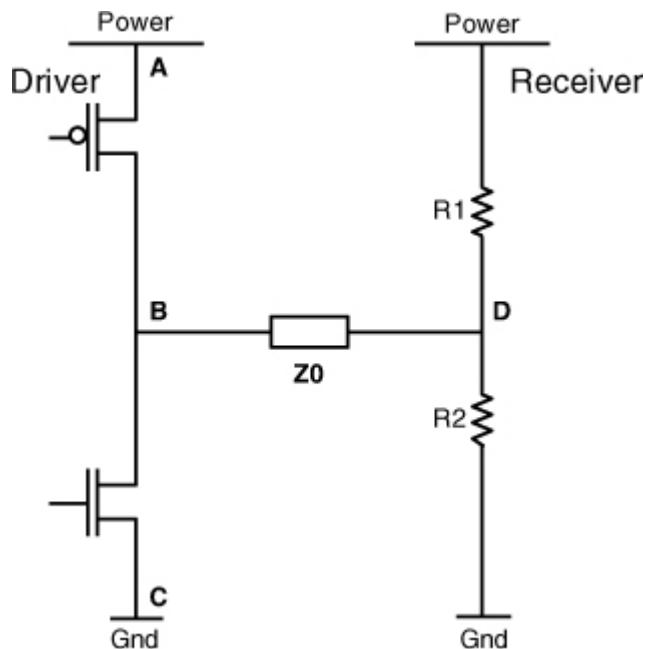
This SSO response in the frequency domain is analyzed assuming that all the modules will have the same phase and amplitude for the switching

currents. In some interfaces it may be different depending on the architecture.

5.3.7. Power-to-Signal Coupling

Power noise can couple to signal at different locations in the channel. In this section, one example is shown where the coupling is from the chip [5]. It is an active noise coupling when the circuitry is functional. Consider a single-ended interface with the center tap termination, as shown in [Figure 5.42](#).

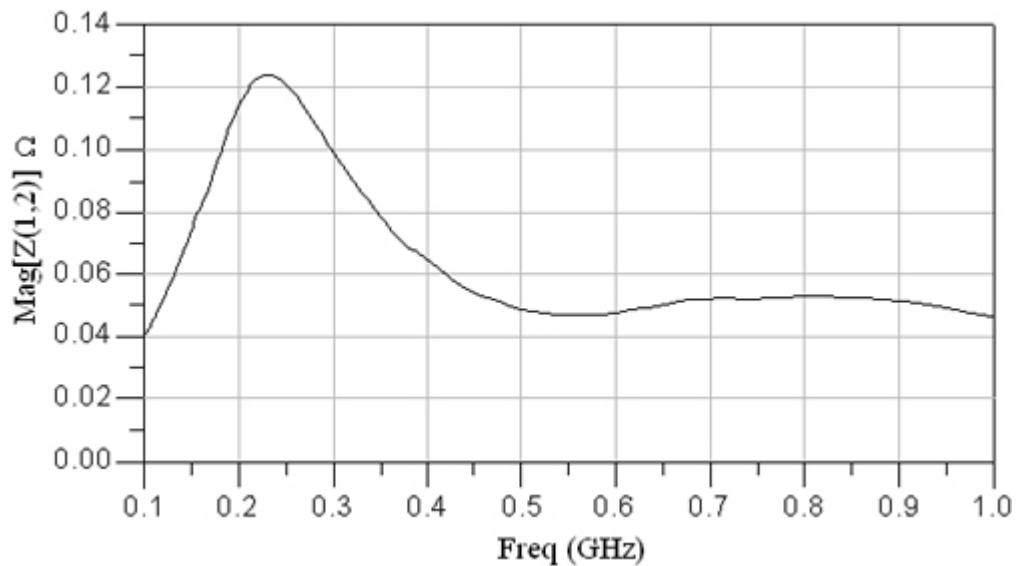
Figure 5.42. Single-ended driver with the channel



Power nets and signal nets are modeled using package, PCB, and the on-chip model described in earlier sections. For determining the power-to-signal coupling at the chip level, the transfer impedance is simulated from point A to point B. When the top driver is switching, there is an effective resistance R_{on} from the power net to the signal net. The entire channel with the power net, signal net, effective R_{on} , and far-end ODT is simulated, and transfer impedance is probed, as shown in [Figure 5.43](#).

Figure 5.43. Simulated power-to-signal coupling at the chip

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



There is a resonance above 200MHz in this coupling plot. It implies that at different frequencies, the noise coupling from power to signal is different. This affects the timing performance of the signal nets.

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5.4. Signal Network Design in Frequency Domain

As the I/O interface data rate increases, high-frequency phenomena such as channel resonance, ISI, crosstalk, SSO, and power/ground noise coupling onto signal network become critical in determining its performance. Thus, to predict the channel performance, to minimize the high-frequency phenomena, and consequently to optimize the channel signal integrity; analysis techniques in the Frequency Domain (FD) are essential.

In addition, as the system interfaces become more complex and global competition demands shorter time to market, the large number of Time Domain (TD) simulation matrices relating to system signal integrity should be reduced by using frequency domain analysis. However, with channels of any complexity, there is not a direct correlation between FD and TD analysis. This raises the question of why we should consider FD analysis. This was addressed in the opening section: Simulations are faster, nonoverlapping coverage, increased understanding of channel (debug), and arguably a more fundamental/robust optimization. The advantages and uniqueness of FD analysis easily makes it a must-have in High Volume Manufacturing (HVM) channel analysis and design. This section describes the methods and techniques of combining FD analysis with TD HVM analysis. The resultant method is an excellent choice for system level signal integrity analysis.

Three major advantages of performing FD analysis are [15]

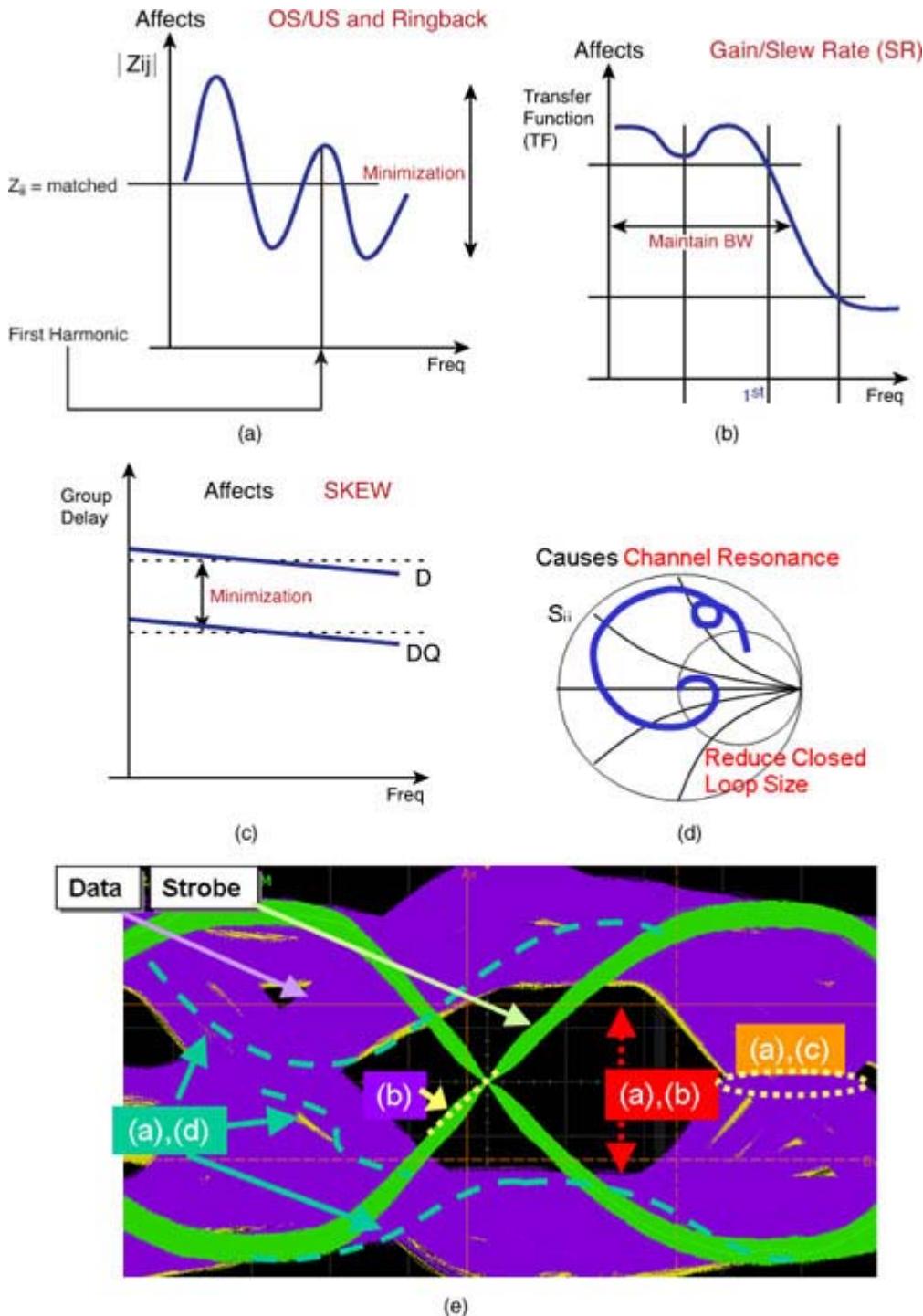
- Any channel resonance that depends on the electrical delay of each bus can be alleviated using appropriate resistors or low-Q microstrip lines.
- An optimum topology that provides excellent signal quality and appropriate gain can be selected before a series of TD simulations.
- The TD matrix size can be reduced through FD sensitivity analysis.

5.4.1. Frequency Domain Optimization

In an high-frequency system, noises can be easily coupled and amplified due to the resonance effect on victim trace. Alleviating the channel resonance effect is essential to mitigate its system risk for high-speed interfaces, in particular the single-ended interfaces. The FD optimization procedure has been proposed in reference [16] to mitigate resonance risk as follows: The first step is to decide the uncontrollable parameters and realistic ranges for the controllable parameters. The controllable parameters are parameters that the designer can change; for example, trace lengths and impedance, on-chip termination, receiver loading capacitance, and so on. On the other hand, uncontrollable parameters are parameters that are set by the board vendor or by feedback from the PCB designer; for example, dielectric height and constant, limited signal trace width and spacing because of the limited layout space, and so on. The second step is to set our goals such as FD fluctuation minimization and resonance alleviation, as shown in Figure 5.44a, and equalized channel response up to a 1st harmonic of its operating frequency, as shown in Figure 5.44b. Accordingly, a smaller return loss and coupling coefficients of systems at the frequencies of resonance will be key to reduce crosstalk and power coupling noise impact. As impedance magnitude fluctuation in the FD response increases, overshoot (OS), undershoot (US), and ringback increase due to reflected, crosstalk, and PDN coupling noise. In addition, the possibility of a signal ledge on the rising edge increases due to nonharmonic resonance, as shown in Figures 5.44d and e.

Figure 5.44. Resonance factors in FD and corresponding TD parameters [15]

[\[View full size image\]](#)



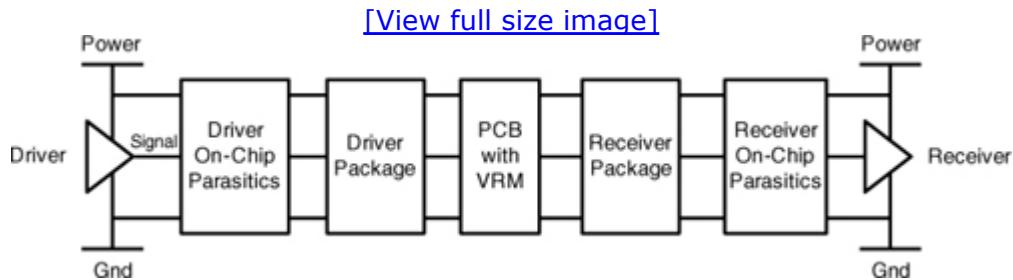
Optimization of the electrical channel performance in FD needs an understanding of the 1:1 correspondence between TD and FD parameters, as seen in [Figure 5.44](#). Simple effects such as slew-rate loss in TD eye-diagrams can be easily attributed to third harmonic damping in FD (loss of gain at these harmonics for deterministic signals such as clock or strobe). Small voltage swing in a TD eye-diagram is attributed to a small gain at the 1st harmonic of the spectral content in the FD. As shown in [Figure 5.44d](#), more complex effects such as harmonic and nonharmonic resonance in FD can lead to standing wave in pre-burst and within burst and ledges on the rising/falling edges of the signals depending on the Q of the pole/zero, its frequency, and bandwidth. ISI effects can be easily seen in the FD as a

large delta of voltage gain variations in the main harmonic frequency range of the different data patterns of the TD signal (that is, in the frequency range of the slowest 111000 to the fastest: 101010). Also, Figure 5.44c shows the group delay plot. Large group delay can lead to large jitter, that is, skew between different patterns. All these resonance factors in FD and their corresponding TD parameters are shown in Figure 5.44.

5.4.2. Simulation and Correlation of Signal Network

For the frequency domain analysis of the signal network, the end-to-end effects of the signal channel are considered. The passive channel components are modeled along with the terminations. A typical block diagram of the channel is shown in Figure 5.45.

Figure 5.45. End-to-end signal network



In a conventional Signal Integrity (SI) analysis, 2D transmission line models are used that may not be adequate for high-speed interfaces. At higher speeds, the 3D effects become important. The coupling effects from the power delivery network, from adjacent signal lines, and from the on-die terminations need to be accounted for. If there is any resonance at a frequency of interest, it needs to be avoided. Typical resonance occurs at $\lambda/4$ or $\lambda/2$, where λ is the wavelength corresponding to frequency of interest. When different elements of the channel are connected together, there may be reflections at the interfaces. The individual segment of an element or combinations of the segments should not correspond to $\lambda/4$ or $\lambda/2$ length. On-chip elements also play an important role. For some interfaces, there is on-die termination to the PDN. This termination can alter the overall frequency response.

The end-to-end signal network in Figure 5.45 is composed of different elements such as on-chip parasitics, a package, and a PCB. The chip may be mounted on the socket. A VRM is situated on the PCB. In designing the frequency response of the signal network, the package and board sections can be modeled with planar 3D or full-wave 3D electromagnetic solvers. On-chip parameters including on-die terminations are used, and the frequency response is determined. Because the on-chip elements, such as pad capacitance and on-die terminations, are connected to the power

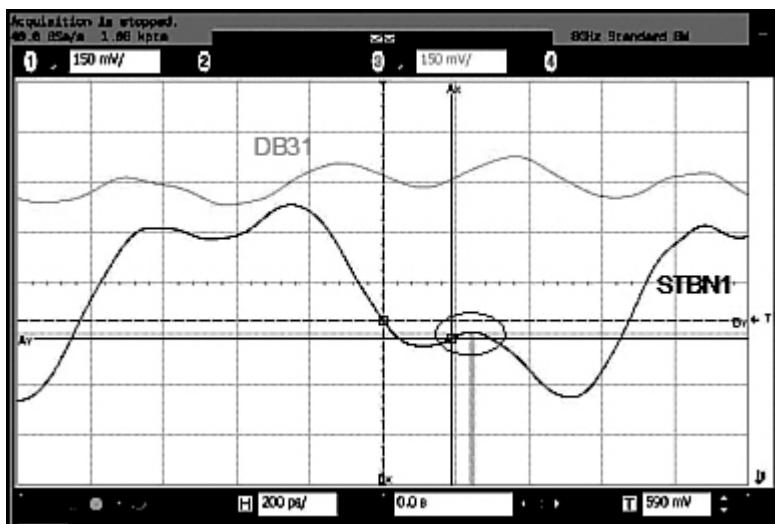
network, power nets are also included along with the signal nets. As discussed in an earlier section, the primary frequency domain parameters for the signal network design are S_{21} for insertion loss, Z_{11} for resonance, Z_{21} for crosstalk, and voltage transfer function for ISI.

5.4.3. Case Study: Crosstalk Amplification by Resonance

In the following section, a case study is presented for interaction between signal nets in the presence of the on-chip elements and the PDN. The signal-to-signal coupling impact is analyzed and mitigated with frequency domain analysis. It has been observed in the lab that there is a third harmonic resonance at 2GHz, as shown in Figure 5.46.

Figure 5.46. Victim bit and strobe oscillations

Source: V. Pandit and W. H. Ryu, "Crosstalk Amplification by Resonance," DesignCon 2009.



In the root-cause analysis process, the following items are determined:

1. Source of the noise
2. Coupling mechanism
3. Resonant structure that amplifies the noise (voltage amplification)

The source of the noise can be from the PDN (such as SSO) or from other signal channels (such as crosstalk), and the coupling mechanism is due to interconnect. Resonant structure is typically for the signal channel. In Chapter 7, "Signal/Power Integrity Interactions," PDN noise and its impact on the signal channel will be discussed. In the case study presented in the following section, it is shown that the crosstalk is a primary noise source,

and it gets amplified due to the channel resonance [17]. This example shows signal-to-signal coupling; however, these signal channels are connected to the PDN for on-die terminations and pad capacitance. I/O device pad capacitance (C_{pad}) consists of all the capacitance seen from the pad due to the I/O circuits, protecting devices, and interconnects.

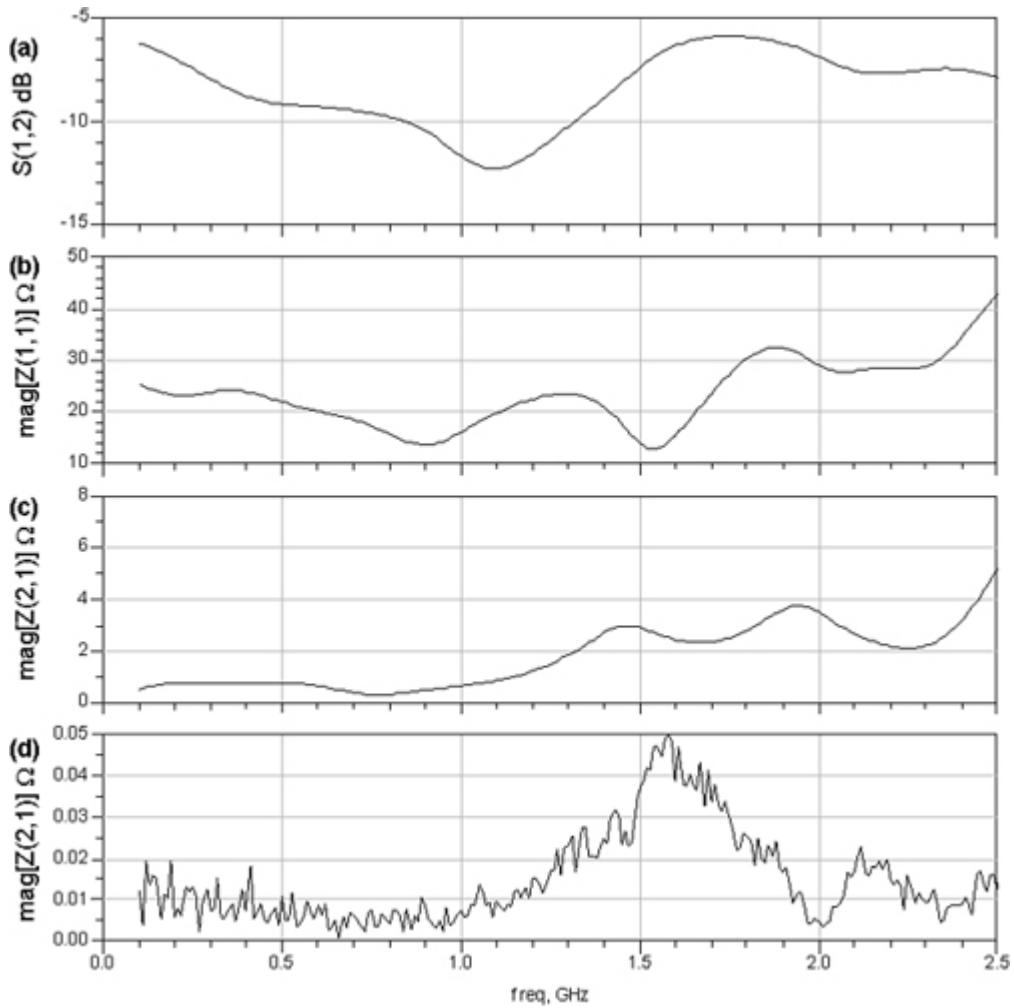
Vector Network Analyzer (VNA) measurements are performed on the PCB at the driver and receive side to identify the root-cause of the problem, as shown in [Figure 5.47](#). The following measurements are taken:

- a. S_{12} from the driver to receiver.
- b. Self-impedance of the worst case bit: Z_{11} at the driver side interconnect.
- c. Crosstalk: transfer impedance Z_{21} from neighboring channel to the worst-case channel.
- d. Power-to-signal coupling: Transfer impedance Z_{21} from the power net-driver side to the signal net-receiver side. All these measurements are done on the back side of the PCB where the package is connected.

Figure 5.47. VNA measurements on PCB

Source: V. Pandit and W. H. Ryu, “Crosstalk Amplification by Resonance,” DesignCon 2009.

[\[View full size image\]](#)



These measurements are taken when the system is active, so the on-chip elements are enabled. Figure 5.47d shows the transfer impedance of the PDN to the worst-case signal net, which implies the coupling between PDN and signal net. It is low, so the possibility of the PDN to signal coupling is eliminated. Figure 5.47b shows the self-impedance of the worst-case bit. It shows resonance around 2GHz, which is the 3rd harmonic of the bus operating frequency. Also, Figure 5.47c shows the transfer impedance from the neighboring bit. This corresponds to the crosstalk to the worst-case bit from the adjacent bit. This also shows a resonance peak at around 2GHz. The crosstalk is the noise source in this case, which has a resonant peak at around 2GHz. This noise gets coupled to the worst-case signal net, which in turn also has 2GHz resonance. Hence, this noise gets amplified due to that resonance of the worst-case bit. Note that the noise amplification is voltage amplification. The total power is conserved and there is no power amplification.

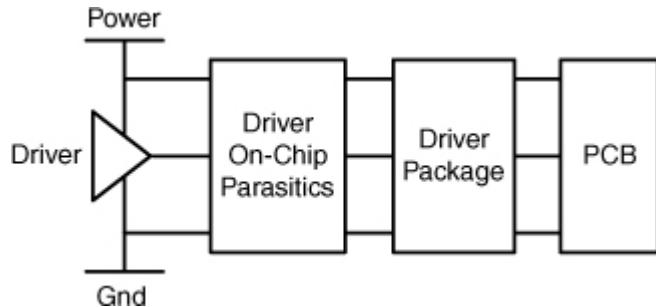
5.4.3.1. Model Correlation

The on-chip parasitics may vary in the manufacturing process. If the entire end-to-end channel is correlated, there will be many on-chip variables, driver side, and receiver side. Therefore, the characterization is done in two

steps [17]. First, the frequency domain analysis for the driver and PCB section is performed and correlation is done with the measurements. After this characterization, the entire channel model is put together and correlated with measurements.

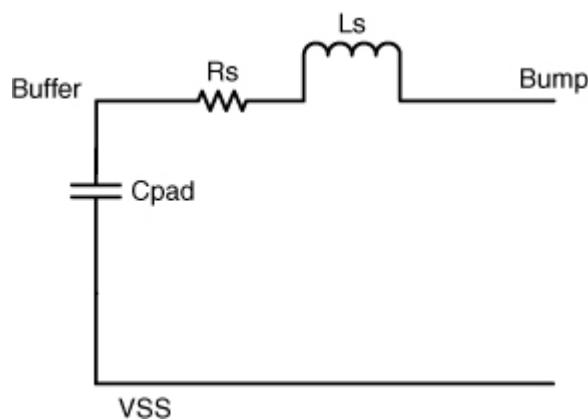
For the analysis and measurement of the first step, the receiver package is removed. The remaining part of the channel has an on-chip section of the driver, the driver package, and the PCB, as shown in [Figure 5.48](#).

Figure 5.48. Driver and PCBs signal network



The package and board sections are passive and include the signal nets and power net. The on-chip parasitics for the signal net include the on-chip pad capacitance for the buffer (C_{pad}), on-chip routing inductance (L_s), and on-chip routing resistance (R_s). [Figure 5.49](#) shows a simple lumped model for the on-chip parasitics of the signal network.

Figure 5.49. On-chip parasitics for the driver signal net



This on-chip model is combined with the planar 3D EM models of the package and board signal network. Measurements are performed with the VNA at the PCB, with the system active. Thus the on-chip elements are enabled. For correlation purposes two measurements are taken:

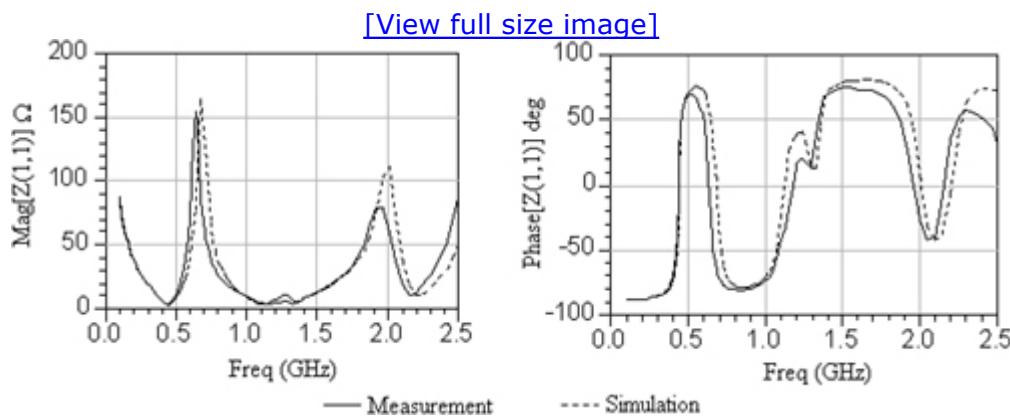
- Self-impedance of the channel looking from drivers

- Insertion loss for the channel

When the on-chip elements are included, the designed values and manufactured values can be different after the chip is produced. The on-chip model parameters are optimized within the given range, so as to match the measured response. Figure 5.50 shows a good correlation of the channel model with measurements. Self impedance is measured at the PCB at the back side of the driver package BGA. The self-impedance plot shows resonances at 2GHz that is the 3rd harmonic of the operating frequency.

Figure 5.50. Self-impedance correlation for driver + board

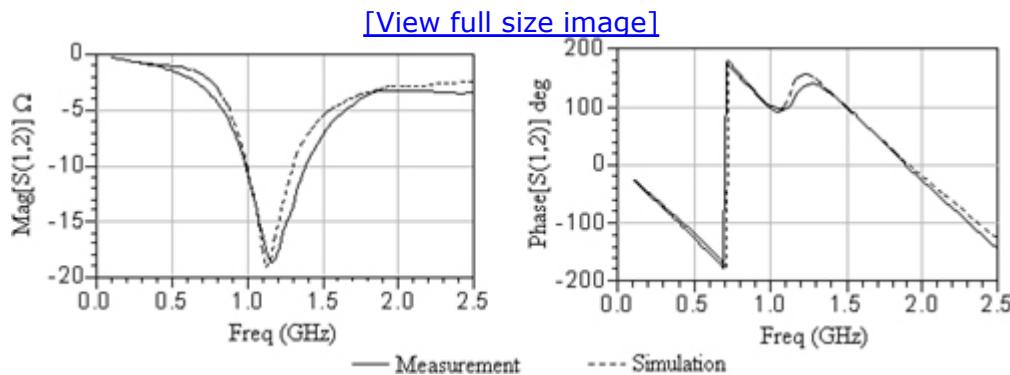
Source: V. Pandit and W. H. Ryu, “Crosstalk Amplification by Resonance,” DesignCon 2009.



Insertion loss is measured on the PCB from the driver side to the receiver side. The insertion loss plot shows the resonance at about 1.2GHz. The simulated results correlate well with the measurements, as shown in Figure 5.51.

Figure 5.51. Insertion loss correlation for driver + board

Source: V. Pandit and W. H. Ryu, “Crosstalk Amplification by Resonance,” DesignCon 2009.



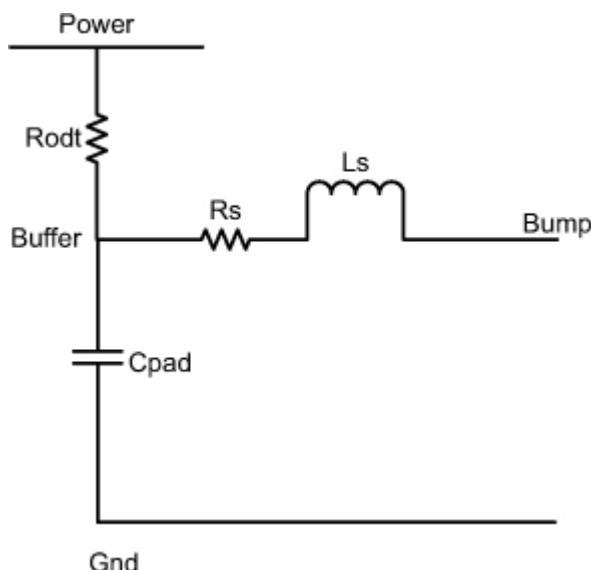
As previously discussed, models of the on-chip driver section, driver package section, and PCB section correlate well with the measurements.

There is a resonance near the 3rd harmonic. It indicates that there must be a resonant length of the signal channel in this section. Next, the receiver section is included in the model, and measurements are performed for the entire channel.

5.4.3.2. Self-Impedance and Insertion Loss for the Entire Channel

The receiver section is composed of the receiver package and the on-chip receiver model. The receiver package is modeled in the planar 3D EM simulator with including signal nets and power nets. It includes the effects of reference transition, stitching, and PDN-to-signal coupling. A lumped on-chip model is used for the receiver signal network, as shown in Figure 5.52.

Figure 5.52. On-chip parasitic model for the receiver signal net

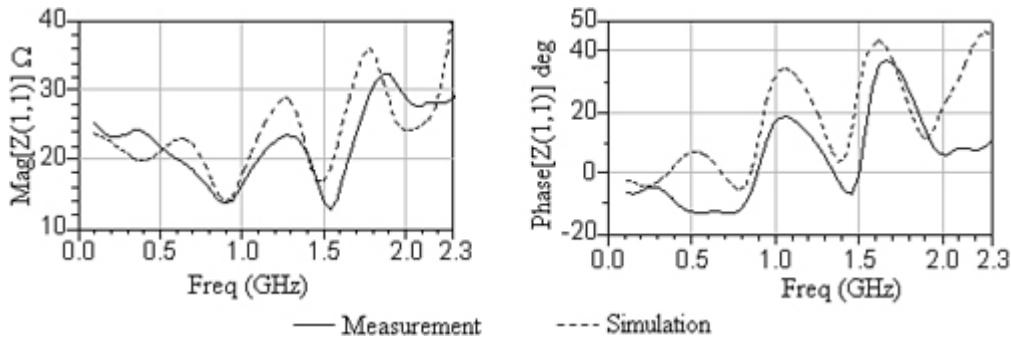


The receiver on-chip model is composed of the on-chip routing resistance R_s , routing inductance L_s , receiver pad capacitance C_{pad} , and on-die termination R_{odt} . The measurements are performed for the entire channel. The self impedance is probed at the PCB at the driver side, with the far end ODT active. The receiver on-chip parasitics are optimized in a given range so as to correlate the measured data, as shown in Figure 5.53.

Figure 5.53. Self-impedance correlation with entire channel

Source: V. Pandit and W. H. Ryu, "Crosstalk Amplification by Resonance," DesignCon 2009.

[\[View full size image\]](#)

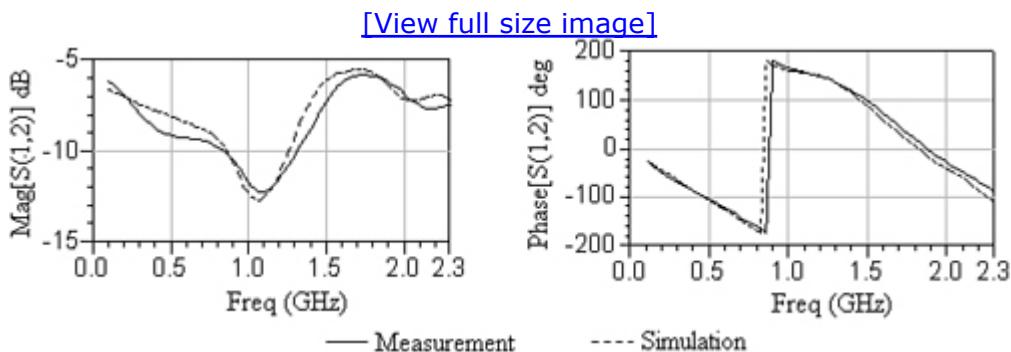


Simulation shows a reasonably good correlation with the measurements. There is a resonance near 2GHz, the 3rd harmonic of the bus operating frequency. This indicates that if there is any voltage noise at this frequency on the signal line, it will get amplified at that frequency.

Figure 5.54 shows the insertion loss correlation with the entire channel. It is probed at the PCB from the driver side to the receiver side with the far end ODT active. It indicates that there is a resonance near 1GHz, but at the frequency of concern, that is, at the 3rd harmonic of operating frequency, it has a flat response.

Figure 5.54. Insertion loss correlation for the entire channel

Source: V. Pandit and W. H. Ryu, “Crosstalk Amplification by Resonance,” DesignCon 2009.

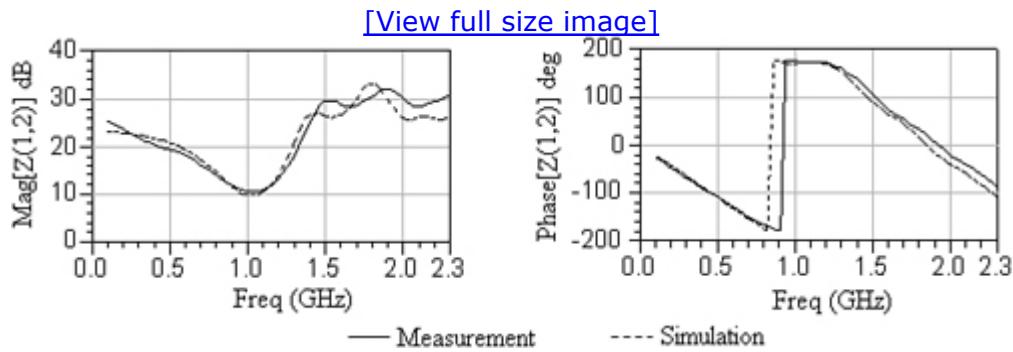


5.4.3.3. Voltage Transfer Function for the Victim Bit

Figure 5.55 shows the transfer impedance Z_{21} correlation for the entire channel. It is probed on the PCB from the driver side to the receiver side on the same net. It shows a good correlation with the simulations. This transfer impedance has near 25Ω value at the DC or low frequency, due to the on-die terminations. The impedance value decreases to 10Ω at about 1GHz and then goes back to $25-30\Omega$ above 1.5GHz. This plot illustrates the voltage generated at the receiver end of the channel due to current at the driver end of the channel.

Figure 5.55. Transfer impedance correlation for the victim bit

Source: V. Pandit and W. H. Ryu, "Crosstalk Amplification by Resonance," DesignCon 2009.

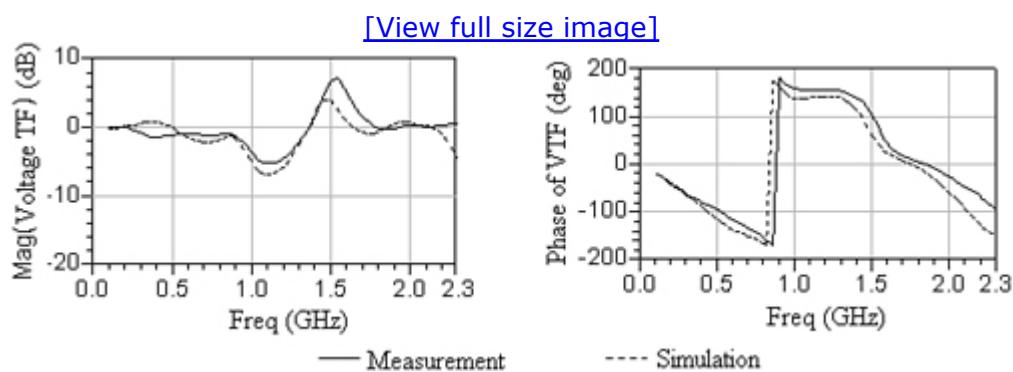


In the previous correlations, one signal net of the victim bit is modeled and measured for self-impedance and transfer impedance. The voltage transfer function is computed by Z_{21}/Z_{11} , where port 1 is at the driver end and port 2 is at the receiver end on the same signal net.

Voltage transfer function is an indicator of the ISI. Typically, it is expected to have a flat transfer function within the signal operation frequency. If the transfer function has a higher magnitude at a lower frequency compared to that at a higher frequency of operation of the interface, then the low frequency pattern has higher swing than the high-frequency pattern. In that case, there is likelihood that there are more ISI effects on the channel performance. For the above signal net, the voltage transfer function is fairly flat over the frequency of the operation (see [Figure 5.56](#)). The value exceeds 0dB above 1.3GHz, indicating that due to the resonance effects, the voltage is amplified.

Figure 5.56. Voltage transfer function for the victim bit

Source: V. Pandit and W. H. Ryu, "Crosstalk Amplification by Resonance," DesignCon 2009, Presentation.



5.4.3.4. Far-End Crosstalk

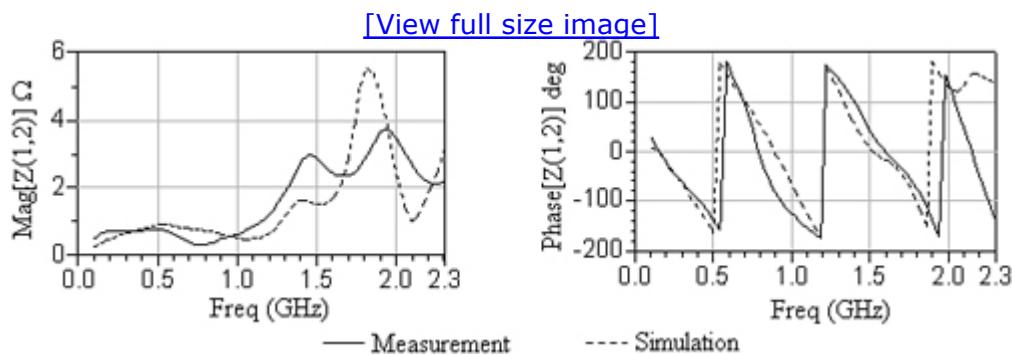
To determine the effect of crosstalk in the frequency domain, the transfer impedance from the adjacent net is simulated and measured. For this

simulation, the 3D electromagnetic models are created with the coupling effects from the adjacent nets. Similar to the victim bit, the on-chip elements, package, and board sections are modeled for the adjacent net.

For near-end crosstalk, the transfer impedance from the driver side aggressor to the driver side victim bit is simulated. Similarly, for the far-end crosstalk, the transfer impedance from the driver side aggressor to the receiver side victim bit is simulated. [Figure 5.57](#) shows the far-end crosstalk.

Figure 5.57. Far-end crosstalk correlation

Source: V. Pandit and W. H. Ryu, “Crosstalk Amplification by Resonance,” DesignCon 2009, Presentation.



The simulations show a similar trend with measurements, in the frequency of resonance. The discrepancy in amplitude may be coming from the aggressor bit on-chip parasitics. Optimization of the on-chip parasitics for the victim bit is described in the previous section, and the same on-chip parasitics are used for the aggressor bit, but they may be different than those for the victim bit. The resonance near 2GHz indicates that there is a crosstalk coupling at the 3rd harmonic of the bus operating frequency. In the previous section, it was shown that the self-impedance of the victim bit also has a resonance near 2GHz. Therefore, the noise is coupled from the aggressor to the victim bit at the 3rd harmonic of the bus operating frequency and is amplified due to resonance (voltage amplification). This phenomenon is called crosstalk amplification due to resonance. It may result in lowering the system margin. To avoid this effect, the resonance needs to be shifted at different frequency than the 3rd harmonic frequency of 2GHz.

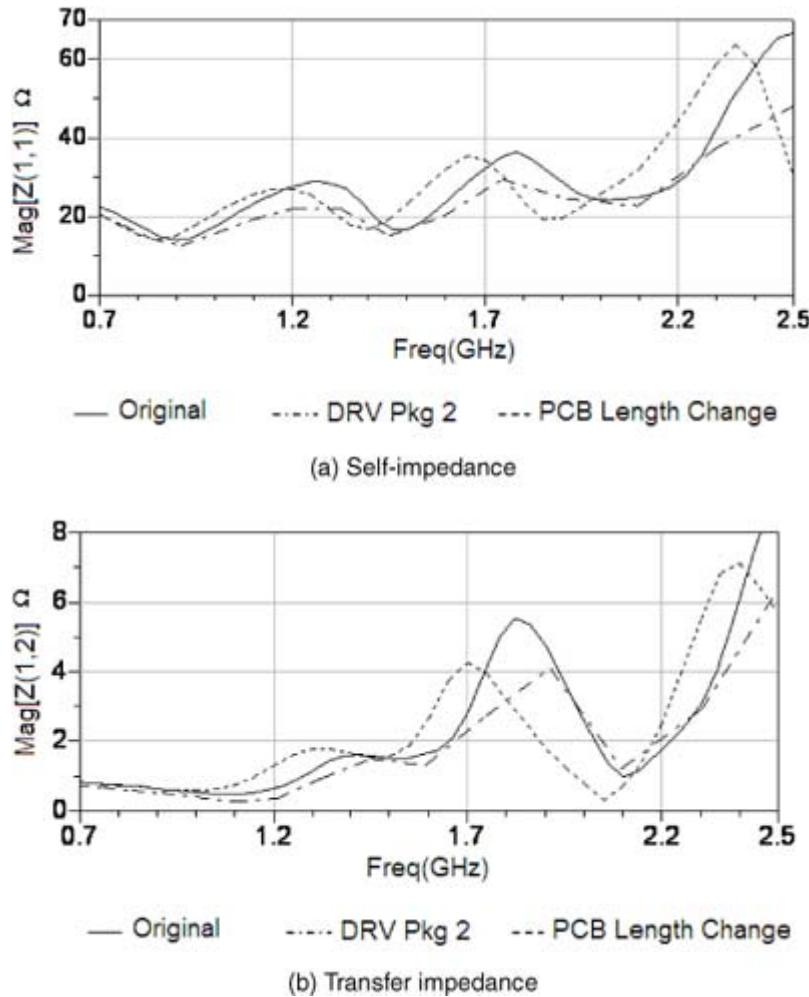
5.4.3.5. Self-Impedance and Transfer Impedance with Different Enablers

To shift the resonance, different enablers are studied. One of the enablers is a different package technology for the drive, and the other enabler is the PCB trace length change. [Figure 5.58](#) shows the self-impedance of the

victim bit and transfer impedance from neighboring bit to the victim bit.

Figure 5.58. Self-impedance and transfer impedance with different enablers

Source: V. Pandit and W. H. Ryu, "Crosstalk Amplification by Resonance," DesignCon 2009.



Both self-impedance and transfer impedance show that the resonance is shifted to the left for the enabler with the PCB length change. Therefore, the PCB length is the major factor in the overall channel for having the resonances near the 3rd harmonic resonance of the bus operation frequency. These resonances are seen for both self-impedance and transfer impedance. When these resonances are shifted to lower frequencies, the noise coupling near 2GHz (3rd harmonic of 667MHz) will not be amplified as much. This enabler will resolve the low margin issue for the victim bit.

In the design phase, the 3D EM models of signal network taking into account on-chip elements and power network, are required to be generated. It is necessary to observe the resonances in self-impedance and transfer impedance (indicating crosstalk) plots and avoid potential crosstalk amplification and power noise coupling issues.

5.4.4. Differential Signaling in Frequency Domain

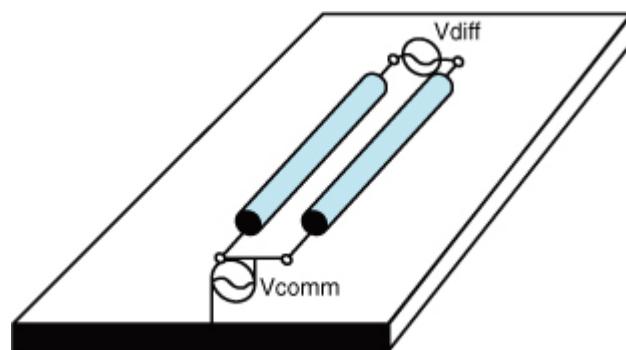
In the previous sections, simulation and characterization of single-ended channel in frequency domain is described. The differential signaling effects can be quantified with mixed mode S-parameters. Mixed mode S-parameters provide the ratios of mode conversion between differential and common mode. Differential mode is what a designer wants to achieve with the differential signaling scheme, but a certain amount of common mode will always be present in a real system. Common mode effects come from various sources such as imbalanced passive interconnections, different loading conditions, and differential buffer mismatch. The common mode becomes the source of the EMI, although the radiated emissions are usually smaller with differential signaling than that due to single-ended signaling. Equation (5.9) shows differential two-port S-parameters converted from a four-port single-ended S-parameters. The mode *dd* represents differential-to-differential, *dc* represents common-to-differential, *cd* represents differential-to-common, and *cc* represents common-to-common mode conversion.

Equation 5.9

$$S_{mm} = \begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} = \begin{bmatrix} S_{d1d1} & S_{d1d2} & S_{d1c1} & S_{d1c2} \\ S_{d2d1} & S_{d2d2} & S_{d2c1} & S_{d2c2} \\ S_{c1d1} & S_{c1d2} & S_{c1c1} & S_{c1c2} \\ S_{c2d1} & S_{c2d2} & S_{c2c1} & S_{c2c2} \end{bmatrix}$$

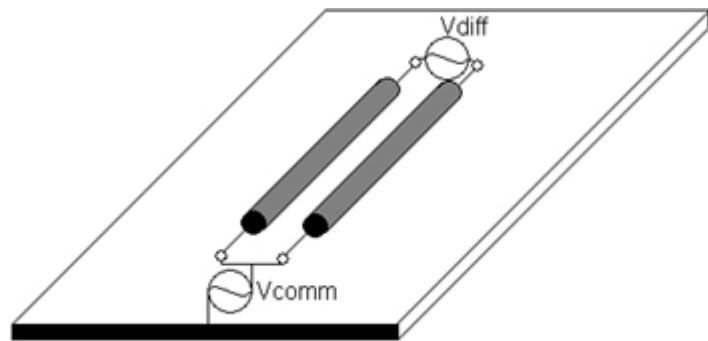
S_{dd} in Figure 5.59 indicates a differential to differential conversion, which is usually the intended response for a designer of the differential channel.

Figure 5.59. Differential to differential mode conversion of differential signaling channel



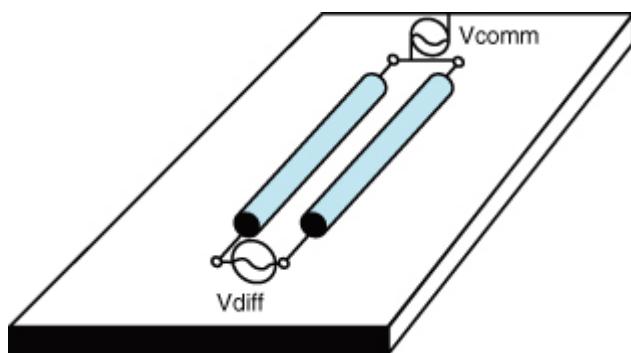
As shown in Figure 5.60, S_{dc} indicates a common-to-differential mode conversion. Bigger S_{dc} means more reception of external signals and noise, which means the lines are more susceptible to noise.

Figure 5.60. Common to differential mode conversion of differential signaling channel



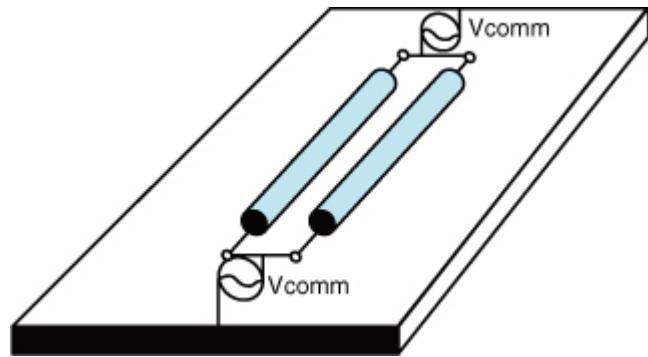
S_{cd} in Figure 5.61 indicates differential-to-common mode conversion. It is often used as a measure of signal radiation. The converted common mode often translates into noises to the receiver. It also acts as a source of radiation. Common Mode Rejection Ratio (CMRR) is the measure of rejected common mode signal in the differential amplifier. Here, common mode signal is rather described simply as a signal common to both input nodes. S_{dc} and S_{cd} both usually occur because of interconnect length mismatch and/or unbalanced buffers.

Figure 5.61. Differential-to-common mode conversion of differential signaling channel



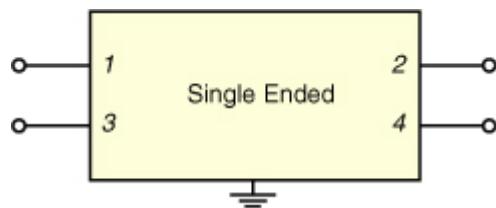
S_{cc} in Figure 5.62 indicates common mode-to-common mode conversion. Less than perfect S_{cc} means a variation of a common mode in the receiver signal and the reference.

Figure 5.62. Common-to-common mode conversion of differential signaling channel



Standard single-ended measurement of the S-parameters for a four-port system is described in [Figure 5.63](#). This system can be described as in equation (5.10) with the S-parameter description.

Figure 5.63. Four-port single-ended device under test

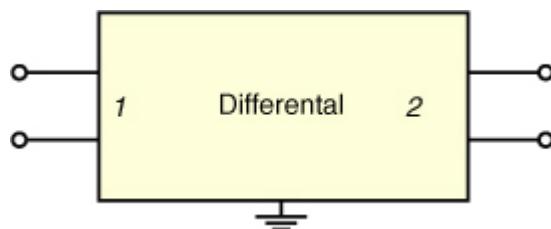


Equation 5.10

$$B = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = SA$$

The four-port single-ended system S-parameters can be converted to a differential system mixed mode S-parameters with the S-parameter conversion equations. Equations (5.11) and (5.12) describe differential and common mode conversion using the single-ended mode in equation (5.10).

Figure 5.64. Two-port differential system derived from a four-port single-ended system



Equation 5.11

$$a_{d1} = \frac{(a_1 - a_3)}{\sqrt{2}}, \quad a_{c1} = \frac{(a_1 + a_3)}{\sqrt{2}}, \quad b_{d1} = \frac{(b_1 - b_3)}{\sqrt{2}}, \quad b_{c1} = \frac{(b_1 + b_3)}{\sqrt{2}}$$

Equation 5.12

$$a_{d2} = \frac{(a_2 - a_4)}{\sqrt{2}}, \quad a_{c2} = \frac{(a_2 + a_4)}{\sqrt{2}}, \quad b_{d2} = \frac{(b_2 - b_4)}{\sqrt{2}}, \quad b_{c2} = \frac{(b_2 + b_4)}{\sqrt{2}}$$

Mixed mode S-parameter relationship (5.13) follows a similar relationship in (5.10). The resulting mixed mode S-parameter has modes conversions as in (5.14).

Equation 5.13

$$B_{mm} = S_{mm} A_{mm}$$

Equation 5.14

$$S_{mm} = \left[\begin{array}{c|c} S_{dd} & S_{dc} \\ \hline S_{cd} & S_{cc} \end{array} \right] = \left[\begin{array}{cc|cc} S_{d1d1} & S_{d1d2} & S_{d1c1} & S_{d1c2} \\ S_{d2d1} & S_{d2d2} & S_{d2c1} & S_{d2c2} \\ \hline S_{c1d1} & S_{c1d2} & S_{c1c1} & S_{c1c2} \\ S_{c2d1} & S_{c2d2} & S_{c2c1} & S_{c2c2} \end{array} \right]$$

Formulating the four-port single-ended-to-mixed mode matrix conversion involves a conversion matrix M , as shown in (5.15), (5.16), and (5.17).

Equation 5.15

$$A_{mm} = MA = \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}$$

Equation 5.16

$$B_{mm} = MB = \begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}$$

Equation 5.17

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}, M^{-1} = \frac{M^*}{|M|} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix}$$

A generalized relationship between the conversion matrix and S-parameters is derived from (5.18), resulting in the relationship (5.19).

Equation 5.18

$$B_{mm} = MB = MSA = MSM^{-1}A_{mm} = S_{mm}A_{mm}$$

Equation 5.19

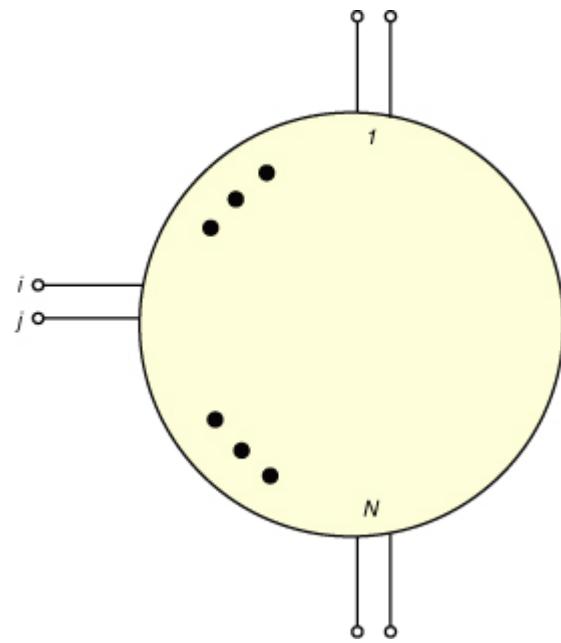
$$S_{mm} = MSM^{-1}$$

If the system is extended to multi-pair differential lines as in Figure 5.65, the conversion matrix M becomes as shown in (5.20).

Equation 5.20

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & \dots & 0 & \dots & \dots & 0 & \dots & 0 \\ \vdots & \ddots & & & & \vdots & \ddots & \vdots \\ 0 & & C_{ki} & & & -C_{kj} & & 0 \\ \vdots & & & \ddots & \ddots & \ddots & & \vdots \\ \vdots & & & \ddots & \ddots & \ddots & & \vdots \\ 0 & & C_{N+k,i} & & & C_{N+k,j} & & 0 \\ \vdots & & \ddots & & & \ddots & & \vdots \\ 0 & \dots & 0 & \dots & \dots & 0 & \dots & 0 \end{bmatrix}$$

Figure 5.65. N-port differential system



where $C_{x,y}$ has value 1 at row x and column y , N is the number of differential ports, k is the k -th port in the differential system. The i and j are the i -th port and j -th port in the single-ended system.

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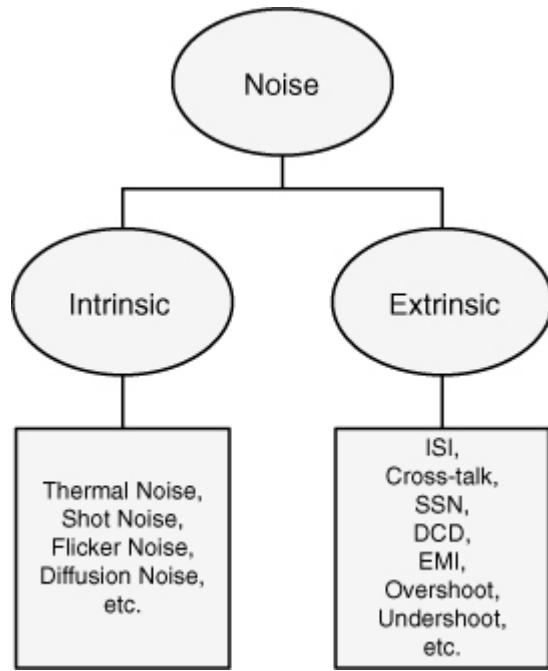
Chapter 6. Time Domain Analysis

Time domain has always been a straightforward and natural domain for measurement, simulation, and analysis of time-dependent signals. Even though frequency domain information of the same signals provides complementary information of the signals analyzed, time domain information is an essential measure of system performance. Especially, simulation of passive components with active devices is inherently more convenient to run in the time domain. This chapter illustrates a time domain gauge for design and optimization of components and systems, along with time domain methodologies using various techniques.

6.1. Time Domain Modeling and Simulation

Time domain simulations for power and signal integrity analysis determine the noise and signal quality. Even though it is difficult to define noise for all applications of engineering, noise is readily defined in the IEEE standard as unwanted disturbances superposed upon a useful signal that tends to obscure its information content [1]. Noise can be categorized in different ways to help analyze the impact on the system. However, in terms of its origination, it is customary to categorize it as intrinsic and extrinsic noise, as shown in [Figure 6.1](#). Intrinsic noise refers to the noise generated inside of the electrical device because of its inherent material nature at its particle level. Typically, it stems from randomly moving electrons inside of the device. Thermal noise, shot noise, flicker noise, and diffusion noise, and all other noises related to the inherent nature of the device fall under intrinsic noise category. Extrinsic noise refers to the noise generated by design aspects external to the intrinsic nature of the device. Inter Symbol Interference (ISI), crosstalk, Simultaneous Switching Output (SSO) noise, duty cycle distortion, Electro-Magnetic Interference (EMI), overshoot, undershoot, and all other device design related noises are extrinsic noises.

Figure 6.1. Classification of noise



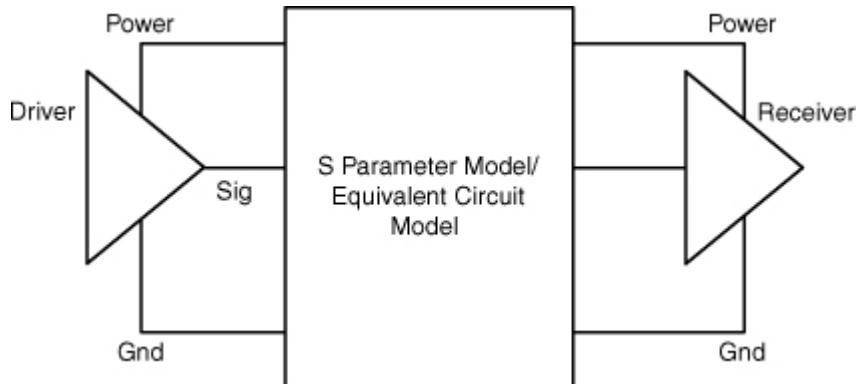
Thorough signal integrity time domain analysis typically requires an investigation of several of extrinsic noise figures classified in [Figure 6.1](#). Power integrity time domain analysis typically requires an investigation of peak-to-peak noise specification because the performance of the power delivery network depends on the capability to maintain a certain voltage level within a specified tolerance. Signal integrity time domain analysis requires investigation of an eye diagram and signal behavior metrics to identify various performance limiting factors. Time domain simulation of power integrity and signal integrity requires modeling of both passive and I/O buffer components. Passive components are modeled by electromagnetic modeling software using various techniques. Active components such as the I/O buffer should be modeled carefully to include all the parasitic impacts stemming from transistor implementation. The active components then should be used either directly or indirectly by conversion to a behavioral model.

6.1.1. Transient Simulations

Most of electromagnetic modeling software can generate frequency domain S-parameters, for signal and power delivery networks. Even though time domain electromagnetic simulation of signal and power delivery network with active components is occasionally used, utilization of frequency domain transfer function in a SPICE-compatible simulator is favored in many simulation situations because of its flexibility and compatibility with buffer models. [Figure 6.2](#) shows generic block diagram for the signal/power integrity time domain simulations. Some of the SPICE-compatible simulators provide S-parameter import capability to expedite the use of frequency domain data in the time domain. If a SPICE-compatible simulator of the choice does not provide the capability, the frequency domain data

should be converted to equivalent circuits using a broadband vector-fitting technique. There have been a number of issues about the conversion of frequency domain data-to-time domain because of passivity, interpolation, extrapolation, and convolution. However, recent advancements in numerical error correction techniques have made SPICE-compatible simulators more robust that reasonable accuracy and stability can be achieved.

Figure 6.2. SPICE-compatible time domain transient simulation



There are different types of the time domain simulation flows and S-parameter models depending on the application. Ideal power and ground represent constant supply voltage, whereas nonideal power and ground represents power/ground nets with parasitics producing noise in the power nets. For conventional signal integrity-only simulations, ideal power and ground are considered. For signal and power integrity co-simulations, nonideal power and ground nets with their coupling to signal nets are included in the S-parameter based model. For power noise simulations for earlier stages such as internal clocks, there are no signals, so only non-ideal power nets are adequate in the S-parameter based model.

6.1.2. Buffer Modeling

A buffer transistor level model describes electrical properties of the device. To protect the intellectual property such as full schematic and manufacturing process information, behavioral models are commonly used to describe devices using electrical parameters as seen at their terminals, as in a black box model. There are different ways of achieving the goal of concealing proprietary information while having it behave almost precisely in the way the original model would behave. IBIS, Verilog-A, Behavioral SPICE, and using Voltage-Controlled-Resistor (VCR) are all good ways of achieving that goal. IBIS has most certainly been a popular choice for the behavioral model, but recently Verilog-A and behavioral SPICE got some traction because of their flexibility.

6.1.2.1. IBIS and VCR Models

I/O Buffer Information Specification (IBIS) is a standard for describing the analog behavior of the buffers of digital devices using plain text formatted data [2]. Figure 6.3 shows the block diagram of the CMOS Buffer. A basic IBIS model consists of four I-V curves, two ramps, buffer capacitance, and packaging parasitic parameters for each buffer on a chip, as shown in Figure 6.4. IBIS standard 4.1 and later versions support Verilog-AMS and VHDL-AMS. IBIS 4.2 and later versions support Verilog-A as well.

Figure 6.3. CMOS buffer block diagram compatible with IBIS

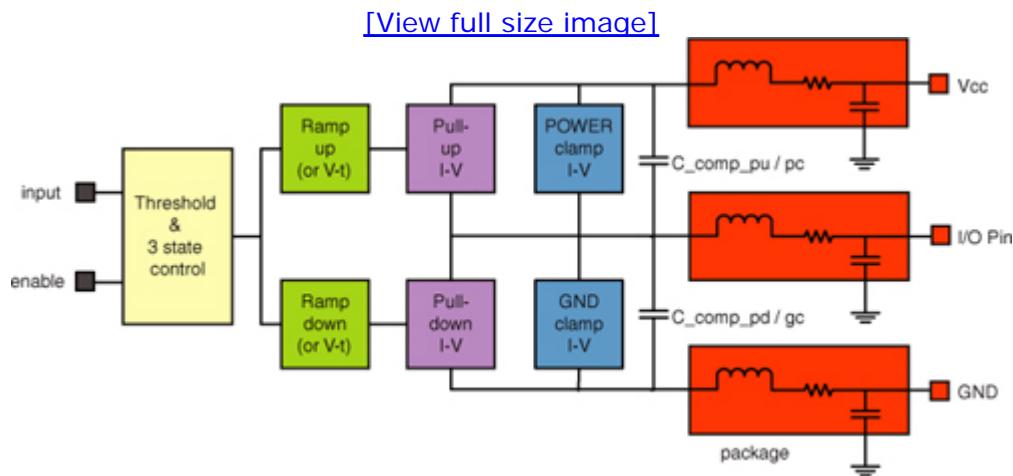
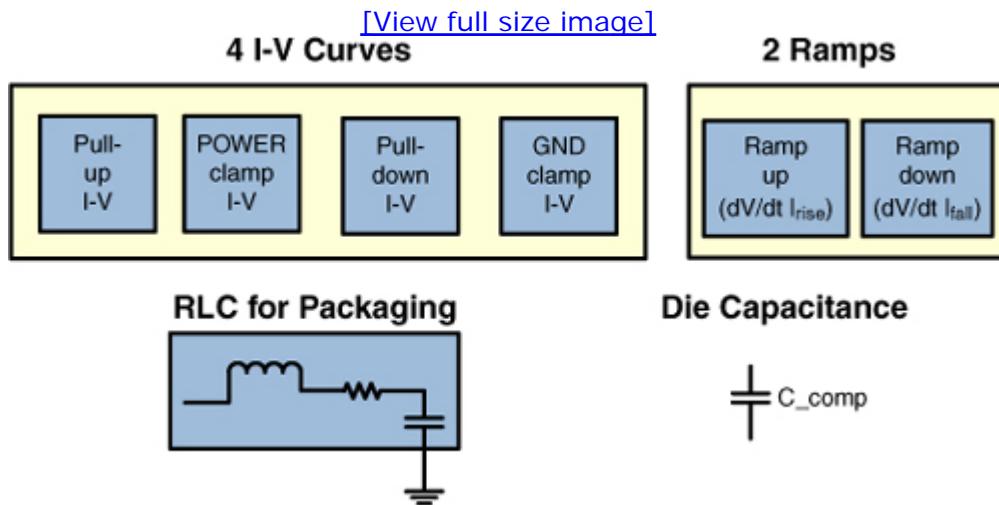


Figure 6.4. Building components of basic IBIS model

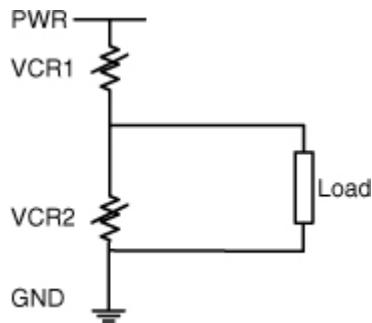


The IBIS model has been mainly used for signal integrity analysis. Power integrity analysis supports has been added recently in IBIS version 5.0. Tables for effective currents in pull-up/pull-down nodes are supported in the newer standard for better power integrity simulation. In earlier versions, such as 4.2, the power node information can be implemented using supporting language such as Verilog-A.

Another alternative to the IBIS model is using the VCR, which is an element

used to control the current flow through the power node and ground node by measuring V-R curves, as shown in [Figure 6.5](#). The VCR model makes the power integrity simulation possible by using the two currents to describe $I_{cc}(t)$ for the power and ground node. It is an effective way to describe nonlinear behavior of a transistor model. VCR is a voltage-dependent current source in its nature. It can take advantage of the flexibility of the voltage-dependent current source implementation by using a polynomial function description of the behavior or by using the piecewise linear function description of the behavior. The flexibility to describe nonlinear behavior of transistor models is an essential ingredient in the behavior model implementation. Other alternatives, such as Verilog-A or other language-based behavior description, are also successful ways to replace conventional IBIS models. VCR models or other alternative representation of buffer models are important components for power delivery simulations and SI-PI co-simulations because they provide relatively accurate power node simulation capability while expediting the simulation time.

Figure 6.5. VCR driver models



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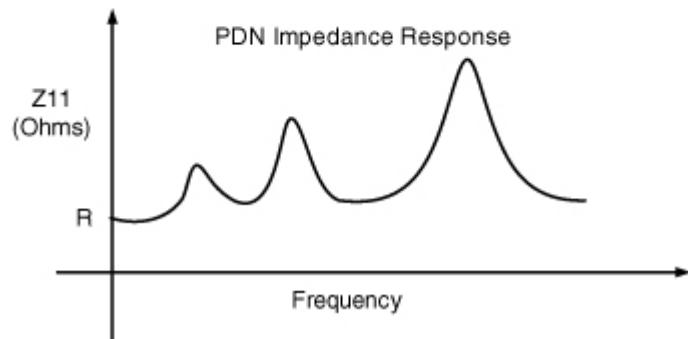
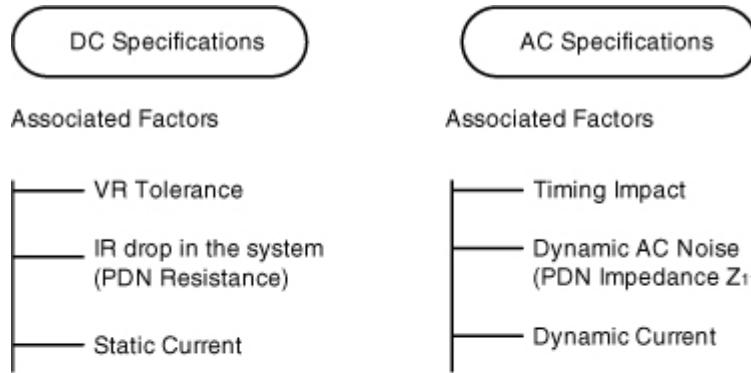
6.2. Simulation for Optimization

This section covers Power Distribution Network (PDN) time domain specifications, and controllable parameters for optimization, including geometry and material, passive components in system boards, and on-chip design variables.

6.2.1. Power Delivery Time Domain Specification

Major power delivery time domain specifications are composed of the peak-to-peak noise limit and the steady state noise limit. [Figure 6.6](#) shows the different factors associated with DC and AC specifications. To meet the target peak-to-peak specification, a range of design and optimization should be performed. With the progress in process technology, the power supply voltage and noise limit are becoming smaller. For the DC analysis, VRM tolerances and the IR drop in the system need to be considered. The PDN resistance in the power grid, package and the PCB influences the DC specifications. The current used in calculating the DC specification is the steady state current.

Figure 6.6. PDN DC, AC specifications and impedance response

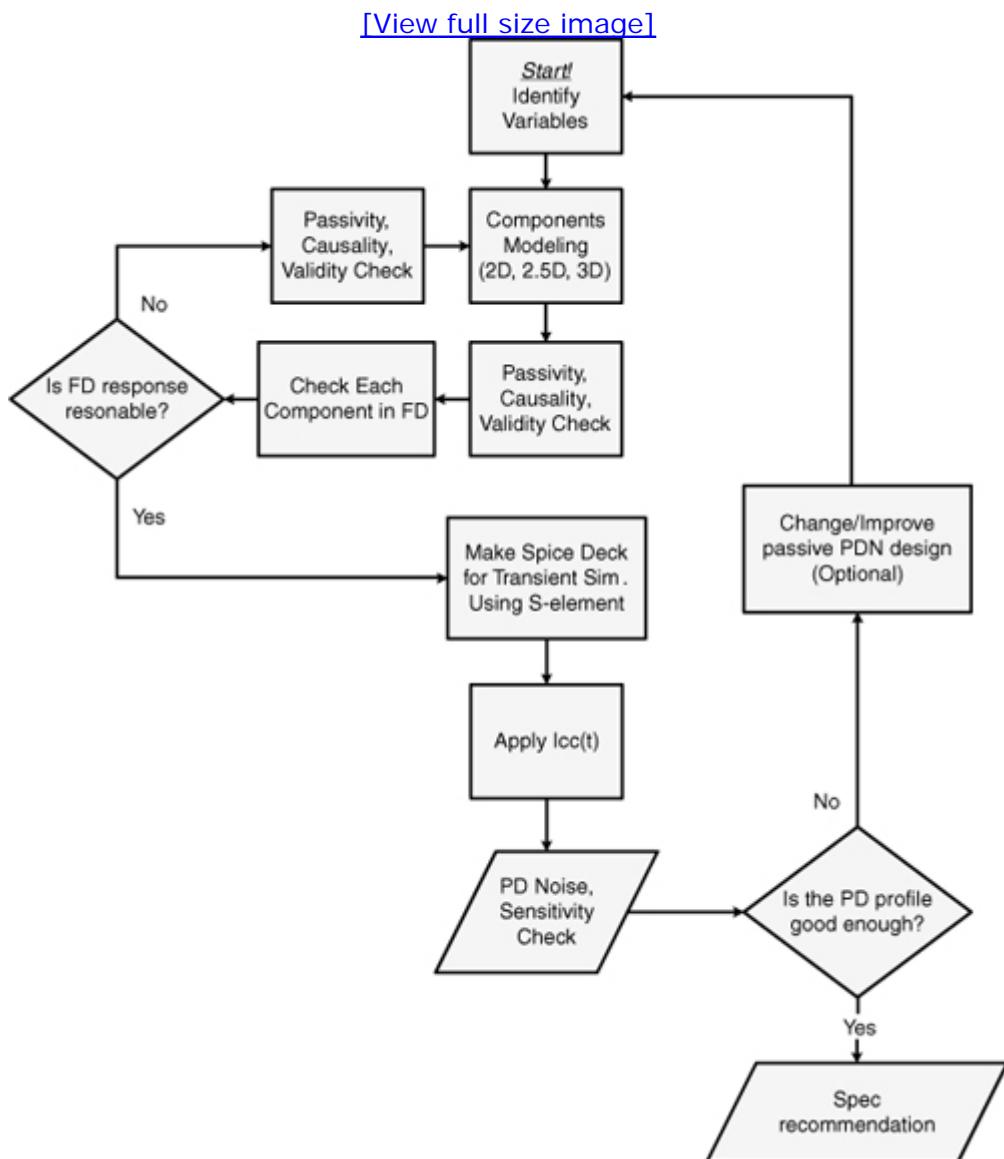


The AC specification is related to the timing performance of the I/O interface. In the AC timing spreadsheet a certain timing budget is allocated to the noise induced timing variations. For the AC transient analysis, S-parameter based models for the on-chip, package, and PCB networks are required. With the S-parameter models, the PDN impedance Z_{11} can be determined. Simulating to measure peak-to-peak noise at a certain location of the PDN requires preplanned electromagnetic modeling with a port on the location to make the signal observable. Active dynamic currents to simulate the peak-to-peak noise are obtained from I/O buffer transistor level simulations or measurements. As the current draw by the active buffers essentially becomes the major source of PDN noise, an accurate description of the buffer model with the current draw from the PDN is critical for PDN analysis. [Chapter 2, “I/O Interfaces,”](#) describes current flow paths for I/O interfaces. For PDN noise simulations, transistor models, behavioral models, or current sources $I_{cc}(t)$ can be used. Other than DC and AC specifications, there are also the minimum and maximum voltages for circuit operation are specified.

Assuming the power delivery peak-to-peak noise is the major parameter that indicates the performance and quality of the PDN, the optimization flow, as shown in [Figure 6.7](#), describes the conventional iterative methods of improving the PDN performance. It starts with identification of controllable parameters in the passive PDN. Usually decoupling capacitors, stitching vias, and other geometrical variations become controllable parameters of choice. The component modeling uses electromagnetic simulation software and then the resulting transfer functions are checked for passivity and causality. When it is proven that the transfer functions are

reasonable, time domain $I_{cc}(t)$ injection simulation is performed to catch peak-to-peak noise and the sensitivity of the noise to the controllable design parameters. If the noise is within the specification with enough tolerance, the optimization of the PDN ends. This algorithm is employed commonly to achieve the goal with little complexity. However, the lack of a systematic approach to the geometry change makes it difficult to be time-efficient. More refined approach can employ optimization algorithm, such as genetic algorithm and particle swarm optimization. More efficient PDN optimization still needs more research to be faster and more effective enough to meet the fast design cycle of low power, low cost devices.

Figure 6.7. Conventional PDN optimization flow



6.2.2. Controllable Design Variables for Optimization

Optimization of a system requires identification of parameters, components,

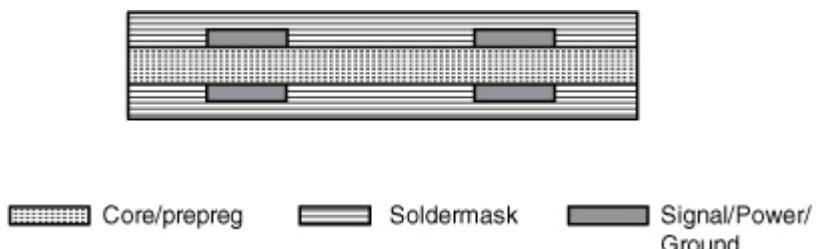
geometry, and system architectures that can be effectively controlled to affect system behavior. In many product development cases, cost constraints limit the range and choices of adjustable parameters. Therefore, it is always necessary to assess cost constraints and resources availability before engaging in optimization process.

6.2.2.1. Geometry and Material

Geometry is one of the most effective and important factors to control the performance of signal and power integrity. Stackup of a PCB or a package is a critical factor because it impacts various aspects, such as, signal integrity, power integrity, and cost-effectiveness.

If a PCB has a two-layer stackup, as shown in the [Figure 6.8](#), only two routing layers are separated by the core material. The routing layers may have signal, power, and ground shapes. The return path for the two-layer PCB may be on the adjacent ground layer or may be on the ground shape next to the signal on the same layer (coplanar). Reference discontinuities may affect signal integrity. Also, the power planes will be discontinuous, so the impedance response may show many resonances. Because of these effects, EMI performance is also affected. This type of stackup may be used in systems with fewer chips and low-speed interfaces.

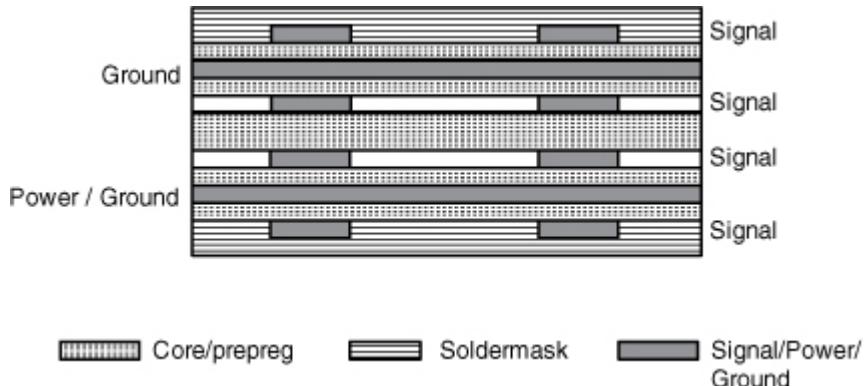
Figure 6.8. Two layer stackup



For high-speed interfaces, solid reference planes are required to maintain return paths. [Figure 6.9](#) shows a six-layer stackup example of the PCB. It has a solid ground plane on Layer 2 and power planes on Layer 5. There are also some ground shapes on Layer 5. Signals on the top layer have ground reference, and signals on the bottom layer have power reference. The distance from signal to reference is small (for example, 4 mils), so there is a good return path at high frequencies, because of the strong electromagnetic coupling. For high-speed signals, a continuous reference needs to be maintained from driver to receiver, and reference change needs to be avoided. For low-speed signals, reference transition from ground reference to power reference may work with adequate stitching decoupling capacitors. Major high-speed signals can be routed on inner layers (such as Layer 3) to avoid the EMI. For this type of six-layer stackup, power to ground coupling will be weak as their separation distance becomes larger. However, there will be power/ground shapes on other layers that need to

be stitched to power and ground planes with stitching vias.

Figure 6.9. Six layer stackup example



For complex PCBs, the layer-count may go as high as 20 or even higher. It depends on the number of integrated circuit chips and interfaces, power/ground shape requirements, and high-speed signal routing requirements. Reducing layers of the package or PCB leads to cost-saving in most cases. However reducing the number of layers could also mean a sacrifice in signal and power integrity because some routing might not have a referencing mechanism that could be achieved with the stackup with higher layers. For example, reducing the number of layers for a particular package could lead to dual referencing of a certain routing that could be single referencing with the original stackup. In many cases, having additional layers for signal reference domain means improved signal integrity. Also for power integrity, it is advantageous to have solid power and ground planes. Stackup impact on signal integrity, power integrity, and cost of the stackup should be included in the study of the sensitivity of the channel components.

Usually the stackup, as shown in [Figure 6.8](#) and [Figure 6.9](#), and material for the package and board are predetermined and do not change in the debugging phase unless significant Return on Investment (ROI) is gained as a result of the stackup and material change. Therefore, after the stackup is determined, designers are usually left with limited choices such as the line width and separation for signals and shapes for powers and grounds. That is, the lateral dimension change is more common than vertical dimension change. Surface roughness is also a factor to consider when it starts becoming comparable to the skin depth at the frequency of interest. Frequency-dependent material characteristics are explained in [Chapter 4](#), "System Interconnects."

6.2.2.2. Passive Components on PCB and Package

Passive components are used in the construction of a system board. Many R, L, C components are used along with packages, connectors, and sockets. All these passive components can be candidate variables. However, for

power delivery, system impact-sensitive components such as decoupling capacitors and filters are usually selected for effective variables for optimization.

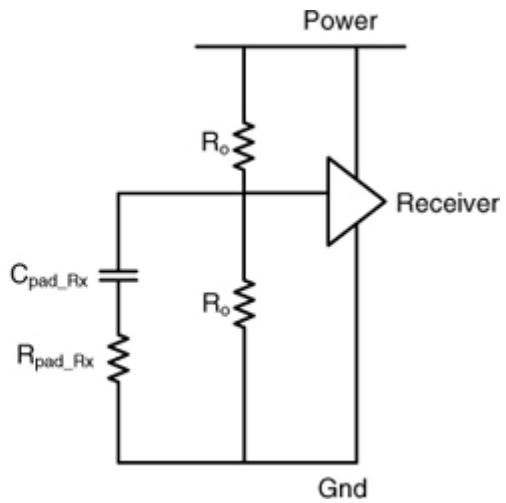
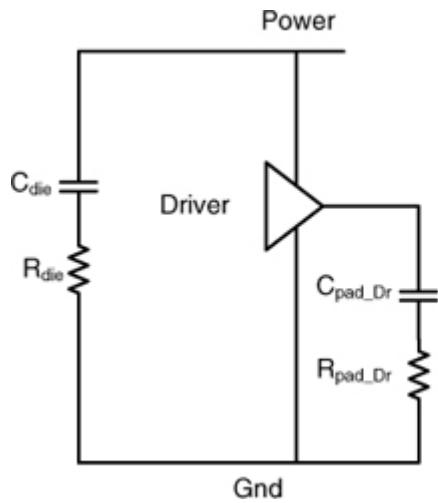
As shown in [Chapter 5](#), “Frequency Domain Analysis,” self-impedance of the PDN is a primary design parameter, and with different combinations of capacitors and filters the required impedance can be achieved, with given stackup and plane-shape geometry. It is required to optimize the power delivery performance using the minimum number of capacitors and filters. The lower the number of passive components, the lower will be the cost of the board.

6.2.2.3. On-Chip Design Variables

On-chip parameters, including the buffer circuit parameters, affect the receiver eye margin. Their sensitivity varies according to their process variation and connected networks. [Figure 6.10](#) shows some examples of on-chip design variables. Usual influencing factors in this category are the I/O pad capacitance C_{pad} , signal pad resistance R_{pad} , on-chip power delivery capacitance C_{die} , and on-chip power delivery resistance R_{die} . Slew rate, buffer output impedance Z_{out} , on-die terminations R_o , and equalizer are all critically sensitive parameters that decide the quality of data transmission. The on-chip PDN elements (C_{die} , R_{die}) play an important role in noise performance at the driver chip. PDN on-die parameters are sensitive parameters to SSO control. It is almost always desirable to put more C_{die} but cost sensitivity should be considered as the C_{die} consumes a considerable chip area. Powergrid serves as a distributed network of resistance and capacitance that interfaces to the package at one end and to the circuits (buffers, C_{die} , and so on) at the other end. Inductance of the powergrid is usually not considered unless the bandwidth surpasses the electromagnetically important frequency when the distance of one node of the powergrid to another node of the power-grid is comparable to one tenth of the wavelength. Process, Voltage, and Temperature (PVT) variation is a crucial factor that should be considered not only in buffer design but also in the SI, PI simulations and analysis. PVT corner condition should be considered as one of the parameters to tune the entire system performance.

Figure 6.10. On-chip design variables

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6.3. PDN Noise Simulations

For an I/O interface design there is a noise specification on the power domain. This noise specification is tolerance from the nominal voltage. The given circuits must operate within the specified tolerance. There are different components of the noise: voltage regulator tolerance, IR drop, and AC noise due to switching of the interface. The following sections address each of the topics in detail.

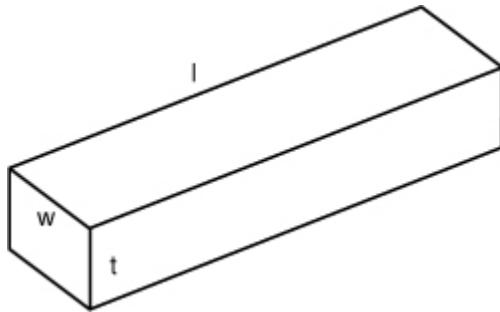
6.3.1. VR Tolerance and IR Drop

A Voltage Regulator (VR) can be mounted on a PCB or on a separate VR Module (VRM). There are different types of VRs or DC to DC converters as described in [Chapter 4](#). The DC and low frequency voltage tolerance includes [3]

- Initial DC output voltage set-point error
- Output ripple dependent on the VR switching frequency
- Noise due to load changes

These components are useful while designing the VR. IR drop is a DC loss due to resistance in the power distribution network. The following section describes analytical formulae for determining the resistance for 3D objects and planes. These formulae are based on regular structures, but in reality the structures may be irregular or discontinuous. For that, the commercial software tools are used. [Figure 6.11](#) shows the 3D metal object, for which the resistance will be examined [4].

Figure 6.11. 3D object and resistivity



Consider a metallic conductor with the length l , width w , and thickness t . From equation (3.10), ; It is rewritten as shown in [Equation 6.1](#).

Equation 6.1

$$E = J\rho$$

where J is the current density in A/m^2 , E is the electric field intensity in V/m , σ is conductivity in S/m , and ρ is resistivity in $\Omega\cdot\text{m}$.

ρ can be defined in terms of geometry and resistance R , as shown in [equation 6.2](#).

Equation 6.2

$$\rho = \frac{Rwt}{l}$$

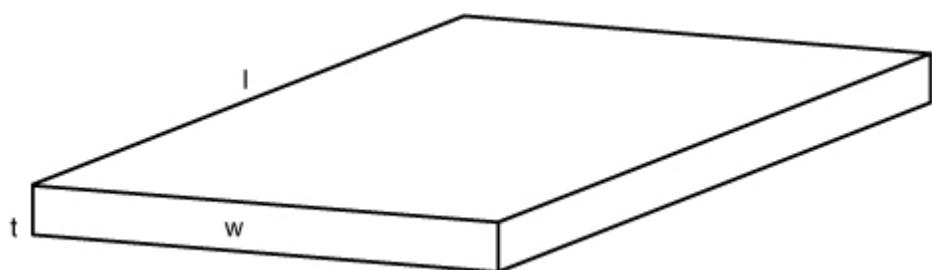
Resistance R can be described in terms of ρ as shown in [equation 6.3](#).

Equation 6.3

$$R = \frac{\rho l}{tw}$$

For the interconnect system, sheet resistance is specified, which is a resistance per unit thickness. [Figure 6.12](#) shows a planar structure for which the surface resistivity is described.

Figure 6.12. Planar structure and sheet resistance



Sheet resistance R_s is applicable for a two dimensional plane, where the assumption here is that the current flows parallel to the plane and not perpendicular to it. Typically it is specified by the Ω/square , which implies that it is the resistance between the opposite edges of the unit square. The resistance R can be calculated from the sheet resistance as shown in equation 6.4.

Equation 6.4

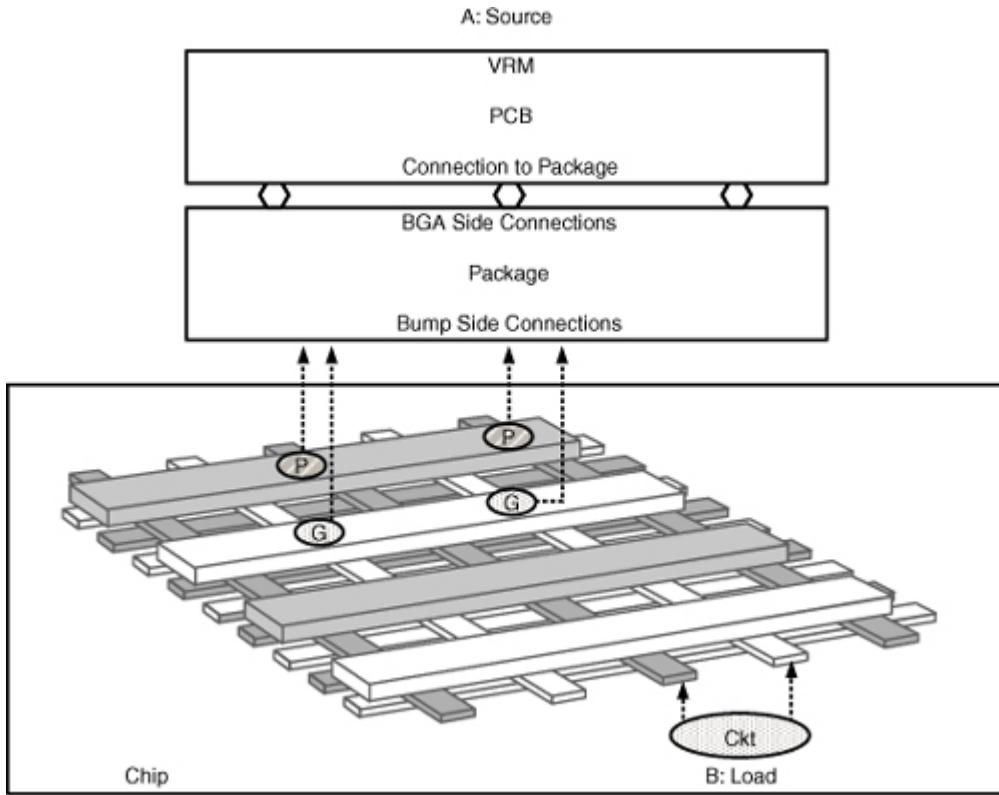
$$R = R_s \frac{l}{w}$$

IR drop is calculated on the PCB, package, and the powergrid. There is a budget for the DC operating value for the circuits. The overall resistance path is shown in Figure 6.13. The voltage regulator is mounted on the PCB at point A in the figure, and the circuit load is located at point B at lower-level metal layers in the chip. From the source VRM, voltage travels to the package and then to the chip. Typically, PCB and packages have power and ground planes. Due to the resistivity of the material, there is voltage drop in the PCB and package. There may be discontinuities and irregular power/ground shapes in the PCB/package layouts. Depending on the IR drop, the required power/ground shapes are determined in the package and PCB. The IR drop on the PCB and package can be lowered by having solid power/ground planes and adding multiple stitching vias.

Figure 6.13. PDN paths for IR drop calculations

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.

[\[View full size image\]](#)



As described in [Chapter 4](#), die pads or die bumps interface with the package. [Figure 6.13](#) shows a configuration in which the package has die bumps. On-chip IR drop is calculated from the top metal layer bumps to the bottom metal layer buffers. IR drop is a major design criterion for determining the number of power/ground bumps. As shown in [Figure 6.13](#), the power grid and ground grid is alternating. There are bumps P connected to power grid and bumps G connected to ground grid. The figure shows a part of the total number of bumps, and these bumps connect to the package. From these bumps, the voltage travels on the grid to the circuits located at point B. If the IR drop in the grid is higher, redesigning of the grid is necessary, or adding more bumps closer to the circuit location B is required.

6.3.2. AC Noise Analysis

For an I/O interface, the current profiles for the power domain are determined. All the circuits on that power domain contribute to the current profiles. The worst-case loading condition is determined based on the architecture of the interface. The PDN model is composed of the board, package, and die networks.

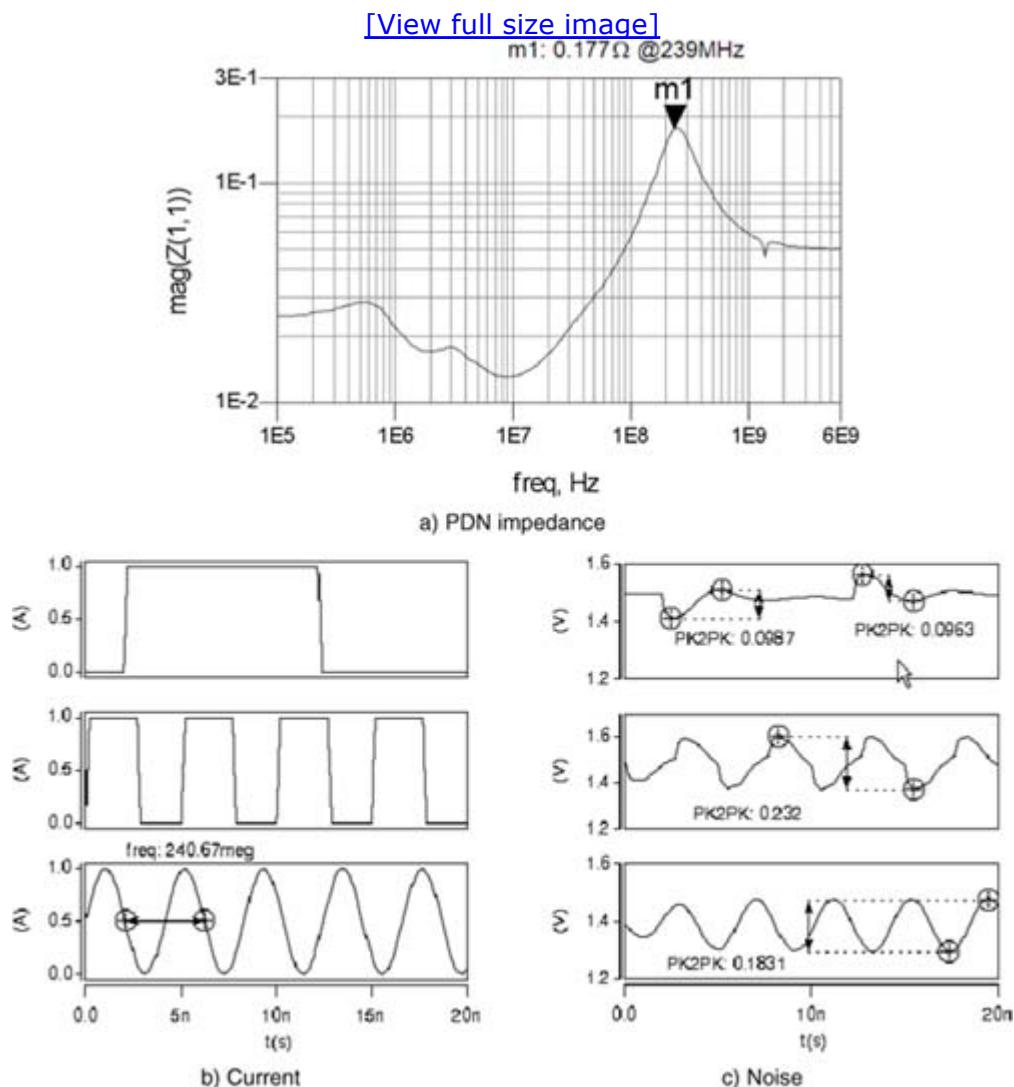
6.3.2.1. Supply Droop and Resonance

The noise is simulated at the die location when different excitations are subjected to the power delivery network having impedance response, as shown in [Figure 6.14\(a\)](#). If there is the circuit activity in the die in which

there is a big step of 1A, then there is a droop (voltage drop) of about 98mV, as shown in Figure 6.14. When the current level comes down to 0 again in a step, there is a bounce of about 96mV. This noise level depends on the ramp rate. The first droop is pertaining to the peak resonance at 240MHz. If the Z_{11} response is of high Q or there is high current, then there will be oscillations after the first droop at 240MHz. Because there is no sustained energy at this frequency, the oscillations will die down. Also, if simulations are done long enough, there is a second droop corresponding to mid-frequency resonance and a third droop corresponding to low frequency resonance [5]. This is typical for the core circuits when there is state change; the DC current level changes with high di/dt , and stays at the high level after that.

Figure 6.14. PDN response to different excitation

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



In the second example shown in Figure 6.14, the excitation is a pulse having a frequency of 240MHz and amplitude of 1A. The noise level changes

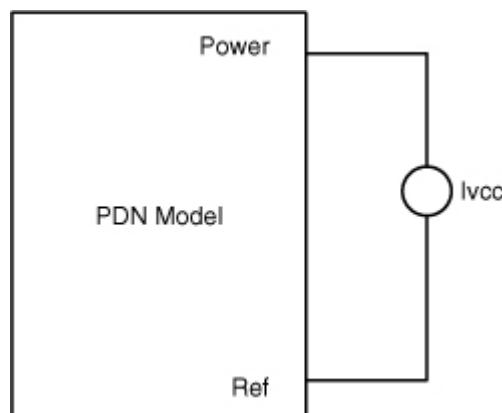
to 232mV peak to peak. The noise level depends on the ramp rate and pulse repetition frequency. To illustrate the effect of the ramp rate, the pulse rise time is reduced such that it is a sine wave pulse at 240MHz with 1A amplitude. The noise level then reduces to 183mV peak to peak.

For the single-ended I/O interface, the data pattern may match with the highest resonance frequency. In that case, there is a sustained energy at that frequency, and the amplitude might increase after the first droop. It is the worst-case loading condition for the PDN. For differential circuits, when they are powered on, there is a step change in terms of DC current, and then there is high-frequency current riding on that. For the differential interface, the worst-case loading condition is when the interface is powered on or off, and only one buffer or a group of buffers are active.

6.3.3. Internal Circuits

As described in [Chapter 2](#), “I/O Interfaces,” the designer may choose to have separate power domains if the previous stage circuits are more sensitive to noise and isolation from the final stage circuits is required. There are clocking circuits and predriver circuits that may or may not be on the same power rail as the final stage circuits. While simulating the noise for the earlier stage circuits, the current is flowing only within the PDN and not going externally through the transmission line. In that case, the current from power to ground can be injected on the die nodes of the PDN model, as shown in [Figure 6.15](#), and the noise simulations are performed. The PDN model is S-parameter-based or an equivalent circuit model.

Figure 6.15. Noise simulation for intermediate stages



As described in [Chapter 5](#), “Frequency Domain Analysis,” the S-parameters for the PDN model may include power nodes and an arbitrary reference node. All the parasitics in the power and ground paths are accurately captured. The transfer function between the power node and local ground node is the same as that between the power node and arbitrary reference node. There is an option of grounding the arbitrary reference node in the system-level simulations. The voltage difference between the power node

and arbitrary reference node is probed in the noise simulations, for determining the noise from the power node to the local ground node.

6.3.4. Final Stage Circuits

While simulating the noise for the final stage circuits, the transmission lines need to be considered in the simulations. [Figure 6.16](#) shows a conceptual block diagram. The simulation setup is similar to that previously described, but for final stage circuits, the current in the PDN is also dependent on the far-end terminations. At the driver side, there are currents in the power I_{VCC} and in the ground I_{VSS} , which are generated with circuit simulations with proper far-end terminations. The PDN model can be the S-parameter model or the equivalent circuit model. It has a driver power port and receiver power port. There is a transmission line $Tline$ that connects to the terminations at the far end. In the example shown in [Figure 6.16](#), there is a center tap termination at the far end. For PDN noise analysis, the worst-case condition is the SSO condition when all the buffers switching occurs at the same time. This depends on the architecture of the interface, and there may be some delay between different buffers. [Figure 6.17](#) shows the power noise coupling mechanism at different stages.

Figure 6.16. Noise simulation for final stage

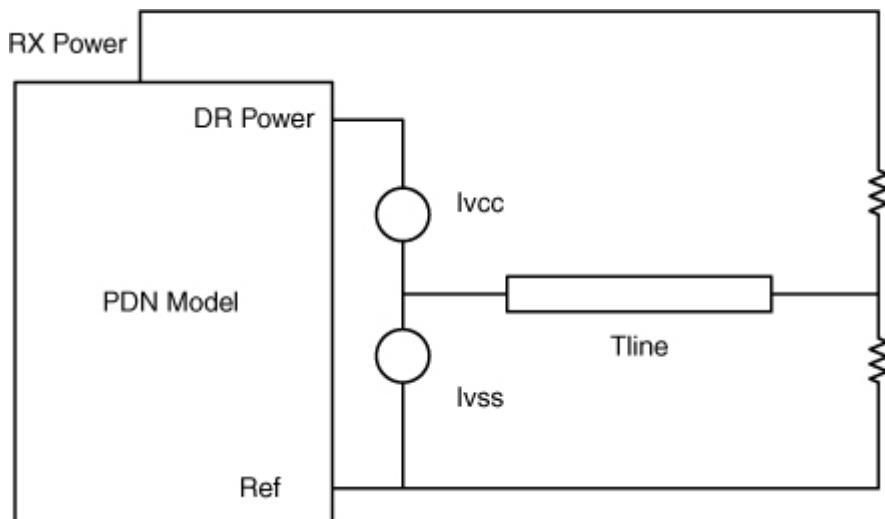
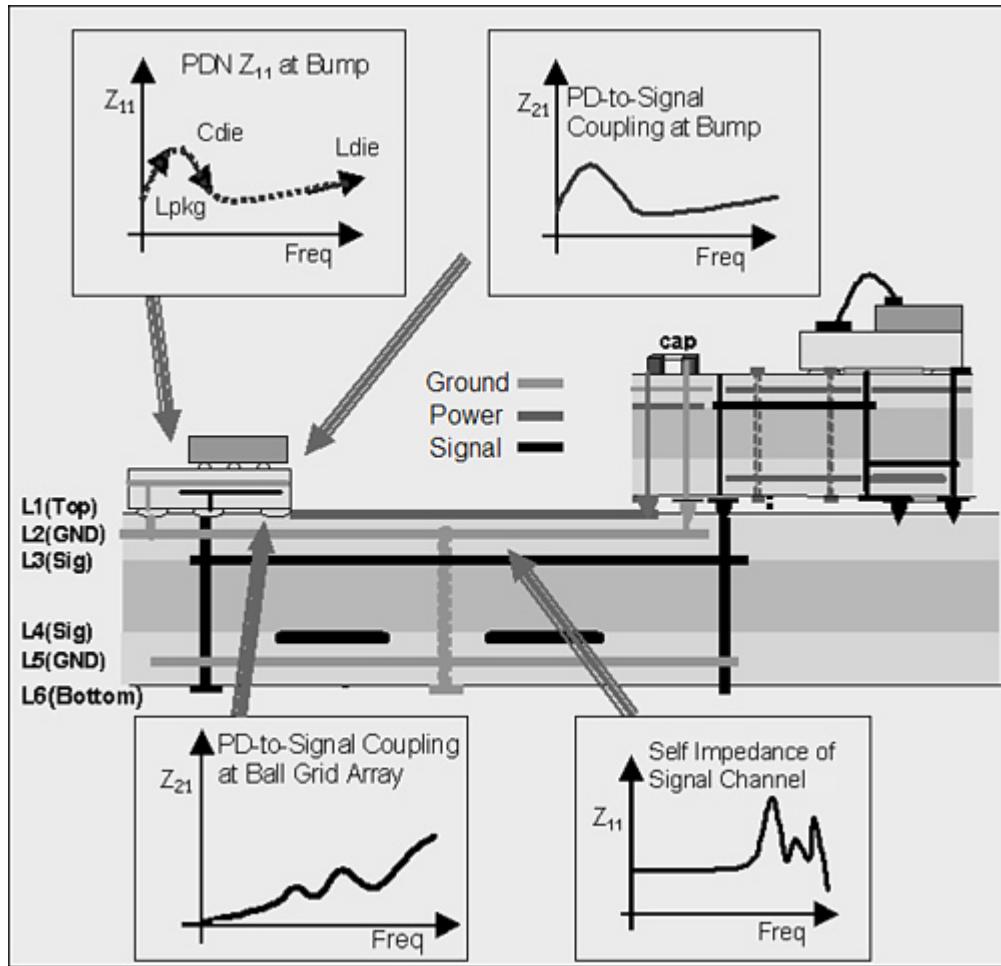


Figure 6.17. Power noise coupling at various stages



In the example, a six-layer PCB is shown with the layer function information. The driver chip is mounted on the PCB, and the receiver chip is mounted on the daughter card. There are different levels of noise coupling to signal.

First is the noise coupling at the driver chip: For the PDN at the driver chip, there is self-impedance Z_{11} at the bump, which varies with the frequency.

Depending on the activity of the chip, the noise will be produced. The resonance is produced due to L_{pkg} (package inductance) and C_{die} (die capacitance). At higher frequencies, the Z_{11} increases linearly due to L_{die} (die power grid inductance). There is power noise to signal coupling at the chip (bump) that can be determined with the transfer impedance Z_{21} , where port 1 is power port and port 2 is signal port. As shown in the figure, Z_{21} at the bump follows the Z_{11} .

At the package-PCB interface, signal travels from the chip to the package, and then from the package to the PCB. The ball-out of the driver plays an important role in the power noise coupling to the signal at the interface of the package to the PCB. This power-to-signal coupling is determined by the transfer impedance Z_{21} at the ball grid array. Also, there may be signal-to-

signal coupling (crosstalk) depending on the adjacency of different pins. As shown in the figure, the Z_{21} at the package to the PCB interface inductively increases with frequency, and there are some resonances.

On the PCB, when the signal travels on the PCB, it goes through different reference transitions and vias and travels through transmission lines. There is a power noise coupling to signal due to this interconnect structures. Also, the transmission line has resonances in self- impedance due to the interconnect lengths between discontinuities of the channel. In the figure, it is shown as self-impedance of the signal channel. If any of the noise frequency is corresponding to the resonance of the self-impedance, then that noise will get amplified.

If the goal of the time domain simulation is to determine the noise impact at the driver chip, then the transmission line model can be connected externally. If the PDN-to-signal net coupling at the chip needs to be considered, then the PDN model needs to have both power and signal nets with coupling included between those nets. For signal and power integrity co-analysis this type of model is required. In general, this chapter focuses on the noise coupling at the driver chip including self- impedance and transfer impedance impact.

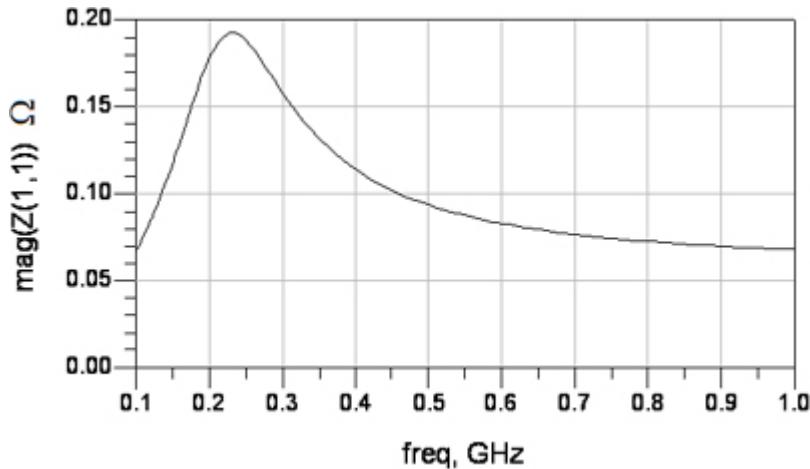
More extensive analysis of the noise coupling due to other elements such as transition from the package to the board, and the board level coupling are discussed in [Chapter 7](#), "Signal/Power Integrity Interactions," and [Chapter 8](#), "Signal/Power Integrity Co-Analysis." For low-speed systems and shorter interconnects (depending on the frequency), considering only the noise coupling at the driver chip is adequate. The transmission line effects at those mid-frequencies are not prominent. The jitter impact at these frequencies is mainly due to the noise coupling at the chip level. As the frequency goes higher and interconnect electrically becomes longer, the effects of other types of coupling (power-to-signal coupling at the PCB) need to be considered. The signal resonance issue comes into picture, and the power supply noise voltage can get amplified due to this resonance. In this case, the jitter and voltage margin impact is prominently due to interconnect-level coupling. For this type of analysis, comprehensive models for the signal and power nets are required.

6.3.5. Single-Ended Systems

Consider an example of the PDN design discussed in [Chapter 5](#), "Frequency Domain Analysis," that is used for the final stage of the single-ended system. The self- impedance plot is shown in [Figure 6.18](#).

Figure 6.18. Simulated self-impedance at the chip location

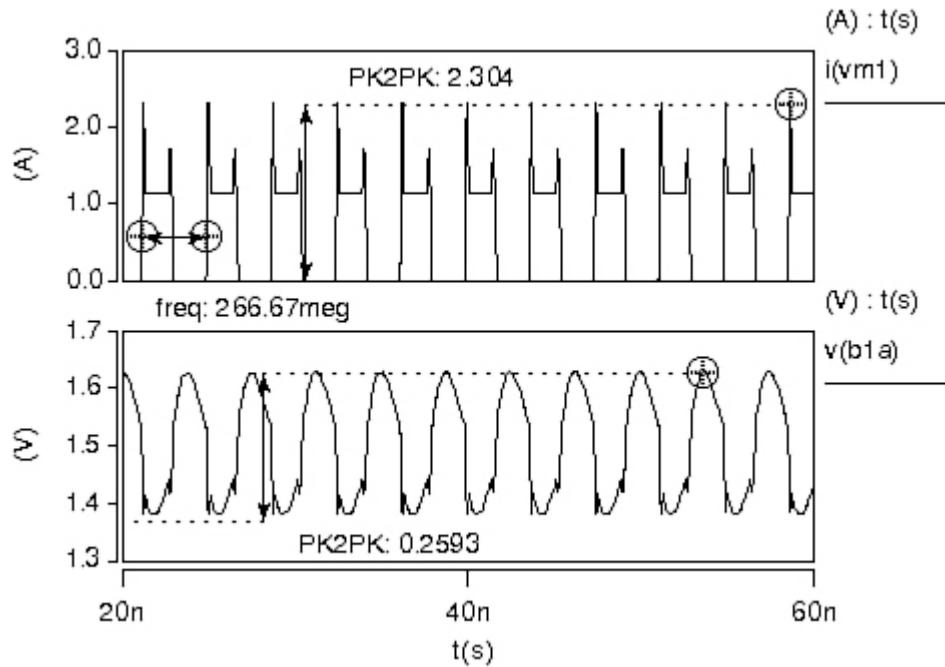
Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009.



First, a single node die model is used for the entire interface. A configuration similar to [Figure 6.16](#) is used for connecting the current profiles. The simplified current in the power node and resultant noise is shown in [Figure 6.19](#).

Figure 6.19. Simulated noise at the driver

Source: V. Pandit and M. J. Choi, "Linearity Indicator with SI/PI Analysis," IBIS Summit, 2010.



The self-impedance plot shows the resonance peak at about 250MHz. To get the worst-case noise, the current needs to switch at or near 250MHz of frequency. The current shown has a frequency of 267MHz that can be achieved for a 11001100 pattern at 1067MT/s, and a 1010 pattern at 533MT/s interface speed [6, 7]. Different frequency components can be obtained by varying the pattern. The data pattern can be varied to change the frequency of the current excitations. The peak-to-peak noise waveform follows the signature of the impedance profile as the frequency varies.

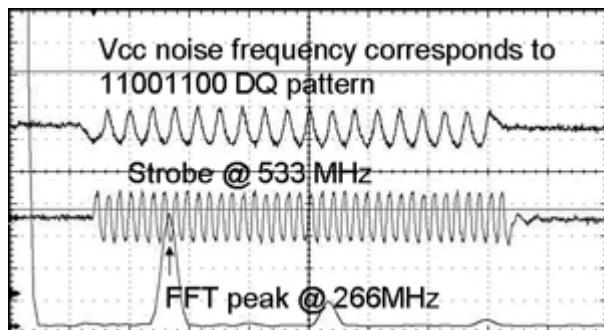
6.3.5.1. Correlation with Measurements

Due to the package and board parasitics, the PDN noise waveform on-chip is distorted when it travels on the package and board. Due to the decoupling capacitors some frequency components get filtered out. Therefore, measuring the PDN noise on-board may not indicate the noise level at the chip.

On-chip measurements are performed for the system, the simulation results of which were shown in [Figure 6.19](#). To measure the noise level at the die of the drivers, a special structure is designed [7]. It has measuring probes at the lower metal layers of the silicon. The data bus activity is started and patterns are varied. For the 1067 MT/s rate, the 1100 pattern produces 267MHz, as shown in [Figure 6.20](#). The entire interface is switching with this pattern, and the on-chip noise measurements are performed.

Figure 6.20. Screen capture of pico-probing measurements

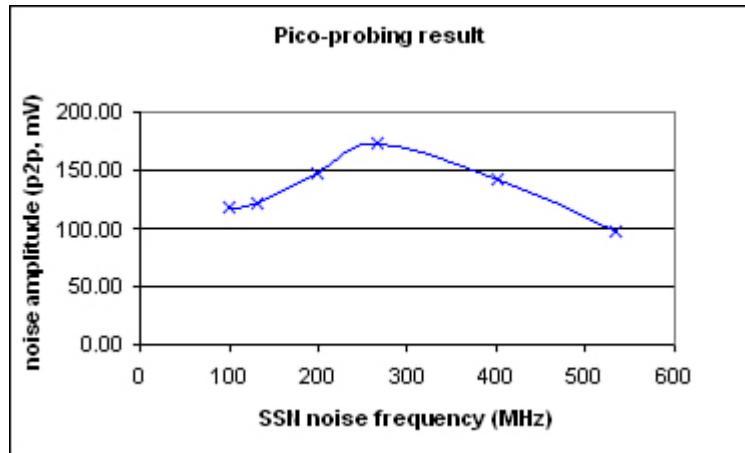
Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



The top plot shows the noise at the power node, which has 266MHz frequency. The FFT of this is taken, and clearly there is a major frequency component at 266MHz. The middle plot shows the strobe that switches at a fixed frequency of 533MHz. Pico-probing calibration is performed, and the resulting value is noted to be around 180mV. Similarly, the data rate is varied, and peak-to-peak noise is determined for different frequencies. For the 1067MT/s data rate, the frequency points are 533MHz for 1010 pattern, 267MHz for 1100 pattern, and 133MHz for 11110000 pattern. Similarly with the 800MT/s data rate, noise for 100MHz, 200MHz, and 400MHz is obtained. [Figure 6.21](#) shows the peak-to-peak noise-versus-frequency plot, with the pico-probing measurements.

Figure 6.21. Measured on-chip SSO noise amplitude versus frequency

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



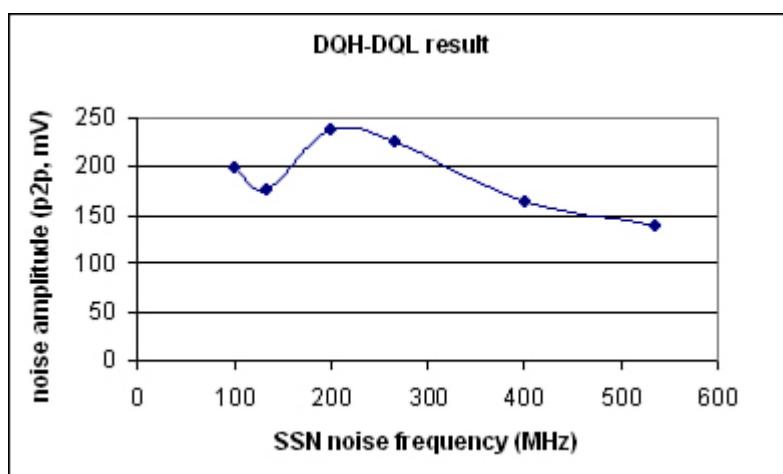
The noise plot shows that the signature is similar to that for the frequency domain self-impedance response shown in [Figure 6.19](#).

6.3.5.2. Noise Measurements at the Receiver

For the same interface, the noise at the driver can also be measured on the PCB with special techniques. The receive side noise is measured and on-chip noise for the driver is projected. The DQH-DQL method is described in [Chapter 9](#), "Measurement Techniques." In this method, the interface is switching with the SSO pattern. One data bit is kept high (DQH) and other low (DQL). The neighboring bits of the victim bits are kept off to avoid the crosstalk effects. The difference between the DQH and DQL is corresponding to the on-chip noise. There is a transfer function that needs to be applied to this because the measurements are at the receiver, and there are some losses. [Figure 6.22](#) shows the plot of projected noise at the driver against the frequency [7].

Figure 6.22. Projected on-chip noise at driver with DQH-DQL approach

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009.

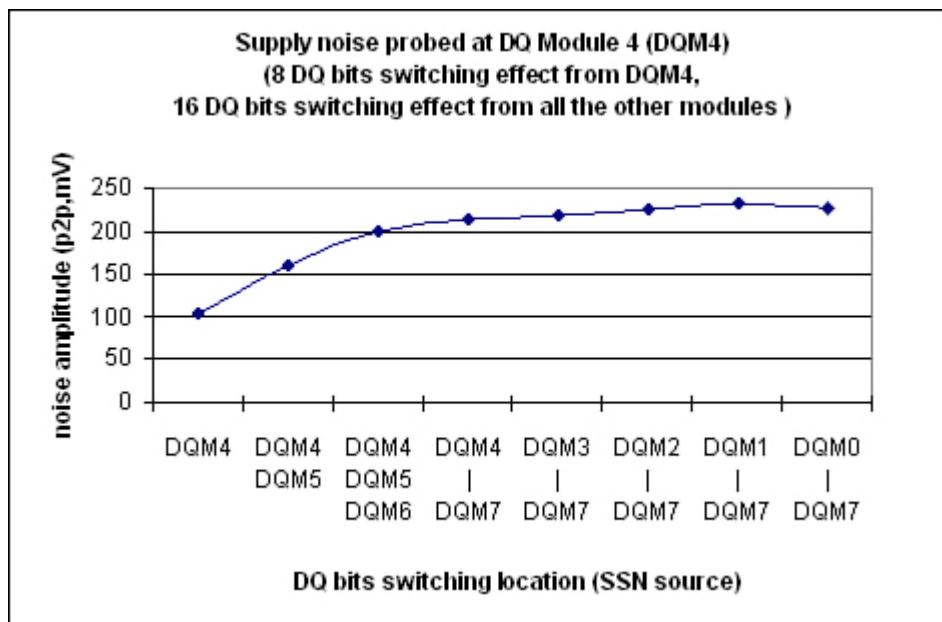


This plot is similar to the on-chip noise measurement plot, as shown in [Figure 6.20](#). The signature of the noise is similar to that for the self-impedance plot. [Chapter 9](#) shows the details of the DQH-DQL method. There are some constraints on this method. The two lines DQH and DQL should have similar noise profiles when switched low. Sometimes, the noise on a particular line gets influenced by neighboring lines due to crosstalk or power/ground plane coupling. In that case, the profile may be different. So the care must be taken to avoid crosstalk and coupling from other shapes.

In [Chapter 5](#), the concept of total Z and SSO in frequency domain is described. The same interface for which the total Z is shown in [Figure 5.41](#), is used for the time-domain correlation. The noise contribution of the individual DQ module (DQM) is determined by switching on one module at a time and measuring noise with the DQH-DQL method. The measurements are performed for DQM4. There are 16 bits in each module, but for avoiding crosstalk and far end PDN coupling, only 8 bits are switched in DQM4. Out of the remaining 8 unswitched bits, one is DQH and the other is DQL. The noise for DQM4 is plotted, as shown in the first point on the x-axis of [Figure 6.23](#). It shows around 110mV of noise due to DQM4 switching.

Figure 6.23. SSO impact of the neighboring modules

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



With DQM4 switching, DQM5 (all 16 bits) is switched and noise at DQM4 is measured. It is the second point on the x-axis. The noise increased from 110mV to 160mV. When DQM6 was also added to it, the noise at DQM4 increased to 200mV. This clearly shows the contributions of the SSO. When DQM7 is added, the point on the x-axis is DQM3-DQM7, and the

corresponding noise is about 215mV. Next, few points on the x-axis are when DQM3, DQM2, DQM1 and DQM0 switching bits are added. The SSO noise measured at DQM4 is shown on the y-axis. It does not increase significantly after DQM7, implying that the SSO is saturated after DQM7. This SSO measurement correlates with the frequency domain SSO response for the same system analyzed in [Figure 5.41](#).

This SSO saturation in the previous example indicates that as the distance from the aggressor module to the victim module increases, the coupling may be reduced. This is dependent on various factors, such as the on-chip power grid design and on-chip decoupling capacitor placement. For the previous example, it indicates that the noise from the data modules DQM0 through DQM3 does not couple significantly into data module DQM4. If a single node on-chip model is used, this effect cannot be captured. This necessitates the use of distributed on-chip model for PDN analysis.

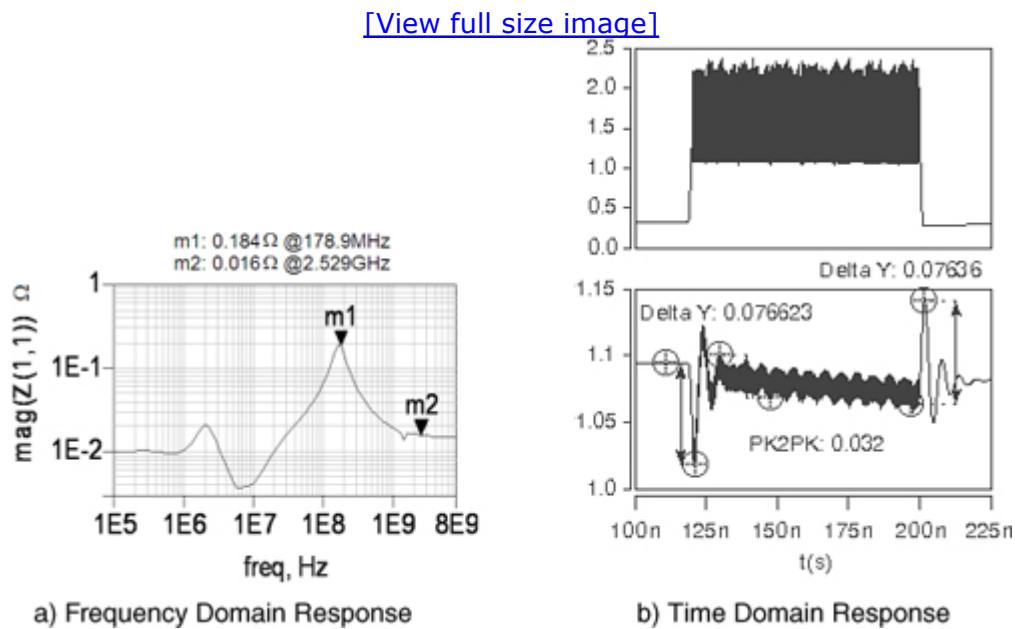
6.3.6. Differential Systems

Differential I/O interfaces have a clocking stage, a high-speed I/O stage, and the final stage circuits, as discussed in [Chapter 1](#), “Introduction.” The noise simulations for the internal stages other than the final stages are done based on the block diagram, as shown in [Figure 6.15](#). As discussed in [Chapter 2](#), “I/O Interfaces,” the final stage of the differential circuit has a current profile at the bus operating speed [8]. During the power on and power off state of the buffer, there is a big surge in power current. A configuration similar to [Figure 6.16](#) is used for the time domain analysis.

For the PDN of the differential interface, frequency domain analysis is performed, and the resonance frequency is determined. [Figure 6.24\(a\)](#) shows an impedance plot at the power node of the differential driver [9]. The basic clock frequency for the bus operation is at 2.5GHz. There is a resonance in the PDN and the peak resonance frequency is 178 MHz with impedance of 0.184Ω . At 2.5GHz, the impedance is $16m\Omega$. [Figure 6.24\(b\)](#) shows the time domain analysis for the differential interface. The current profile is shown in the top plot. At the power on of the interface, there is a big di/dt at around 120ns. Due to this di/dt , there is a voltage droop of 76mV. Then, there is a normal operation condition up to 200ns, with steady state noise of 32mV. After that, there is a power-off scenario with a current variation from the steady state. There is a voltage bounce of around 76mV. After the droop, the waveform oscillates at the resonance frequency. The amplitude of the first droop is dependent on the amplitude of the peak resonance impedance. The oscillations settle down after some time. At the steady state condition, the amplitude is dependent on the impedance at 2.5GHz, that is, the fundamental frequency. Similar to the droop, voltage bounce is also corresponding to the resonance frequency and amplitude.

Figure 6.24. Impedance and noise for differential driver

Source: M. J. Choi and V. Pandit, "SI/PI Co-analysis for I/O Interfaces," IBIS Summit, July 2009.

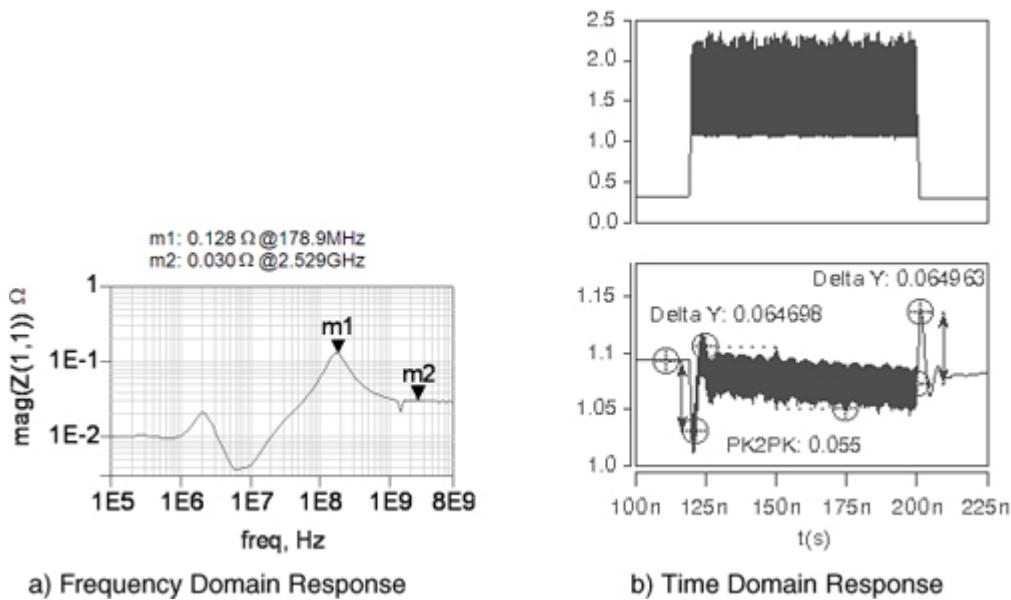


To reduce the noise magnitude, the PDN components can be varied or the di/dt conditions can be changed. With a C_{die} increase, the peak resonance impedance will be lowered, as discussed in [Chapter 5](#), "Frequency Domain Analysis." With an R_{die} increase, the impedance at the resonance can be damped. [Figure 6.25\(a\)](#) shows an impedance plot with the higher R_{die} . The peak resonance impedance is changed from 0.184Ω to 0.128Ω . As a result, the droop reduces to 64mV, as shown in [Figure 6.25\(b\)](#). However, the impedance at the fundamental frequency of 2.5G increases to $30m\Omega$, increasing the noise level in a steady state to 55mV. With a higher R_{die} , even though the droop and bounce levels are reduced, the steady state noise increases.

Figure 6.25. Impedance and noise with higher r_{die}

Source: M. J. Choi and V. Pandit, "SI/PI Co-analysis for I/O Interfaces," IBIS Summit, July 2009.

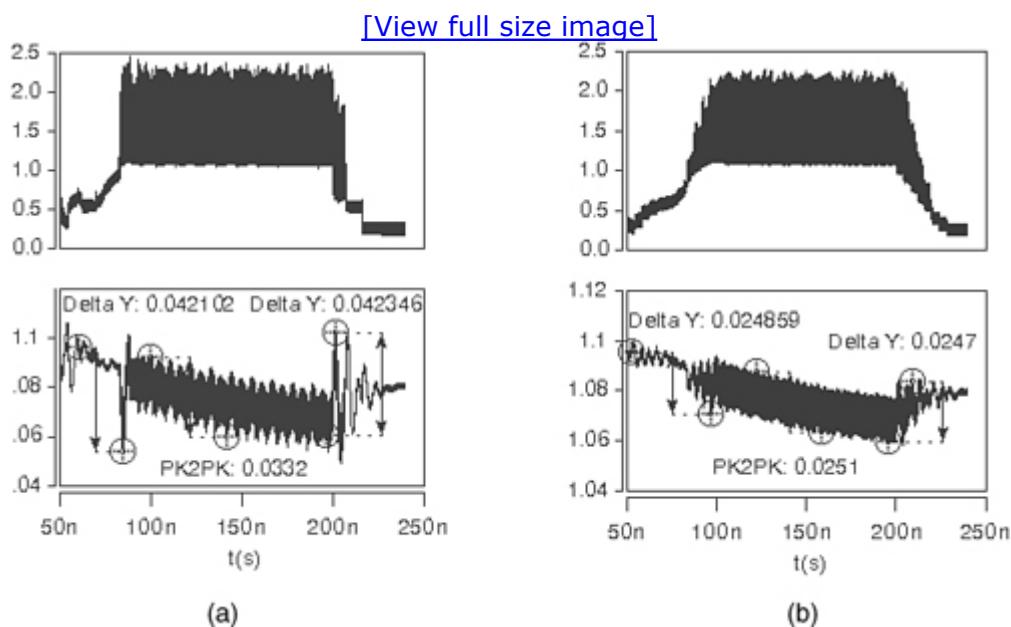
[\[View full size image\]](#)



For a differential interface, another way to reduce the power-on noise is to reduce the di/dt with architectural controls. One of the examples of architectural controls is that the power on delay is introduced in different circuits. As a result, the ramp rate of the power on current is reduced. Figure 6.26(a) and Figure 6.26(b) show the current profiles and different techniques for architectural controls. The power on and power off ramp rate is slowed down with different architectural options. The corresponding power-on droop and bounce gets reduced significantly.

Figure 6.26. Architectural controls to reduce di/dt and noise

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



For a differential interface, if multiple stages (driver, predriver, clocking, and so on) are on the same power domain, then the current profiles for the

different stages need to be added. In that case, all the different frequency components are considered for performing the time domain simulations.

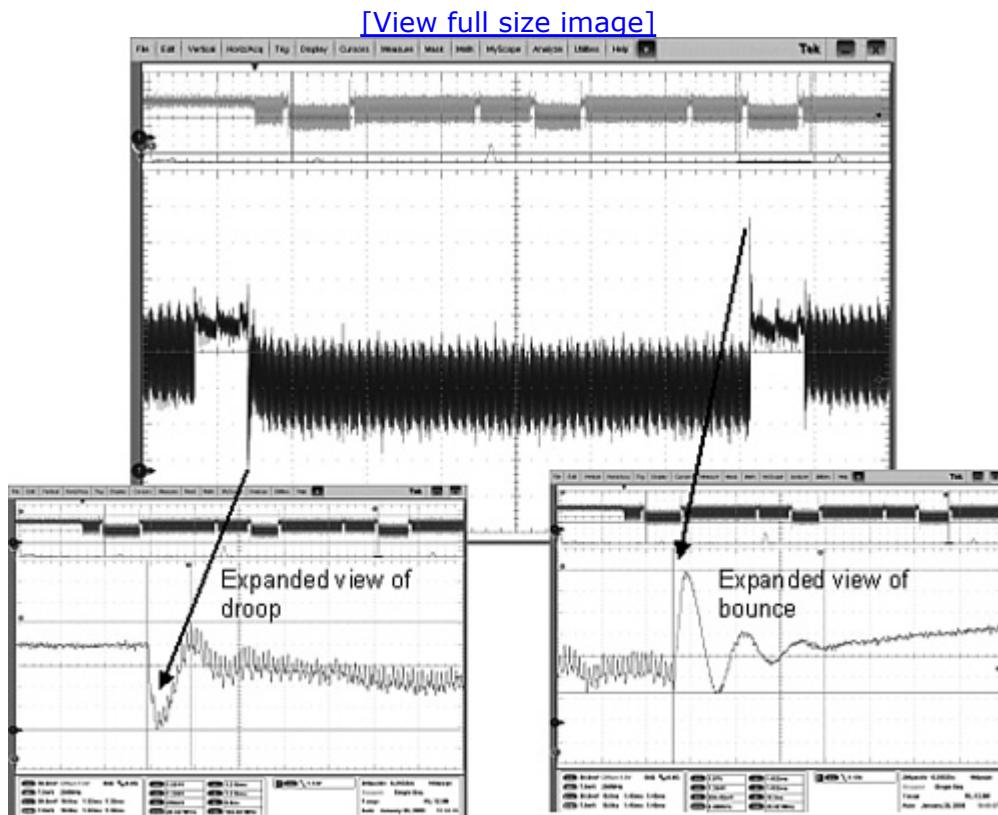
6.3.7. Logic Stage

For the logic stage noise simulations, it is required to get the $I_{cc}(t)$ profiles to simulate the power delivery noise impact. The Value Change Dump (VCD)-based activity levels are determined and the dynamic current is extracted [11]. The logic stage circuits may consume certain current in a particular state, and when the state changes the current may change significantly.

Consider an example where the current changes from low to high for the logic circuitry. The captured noise waveforms are shown in Figure 6.27 [10].

Figure 6.27. Measured noise for logic circuitry with pico probing

Source: J. Delino, T. Pham, and F. Fattouh, “Di/Dt Mitigation Method in Power Delivery Design and Analysis,” Design Automation Conference 2009.



In this example, when there is a state change, there is a big voltage droop. As shown in an earlier section, the droop amplitude is dependent on the peak resonance amplitude of the PDN. There is also a ringing of the noise waveform after the droop, and that frequency is the PDN resonance frequency. The logic state circuitry is switching at a high frequency after

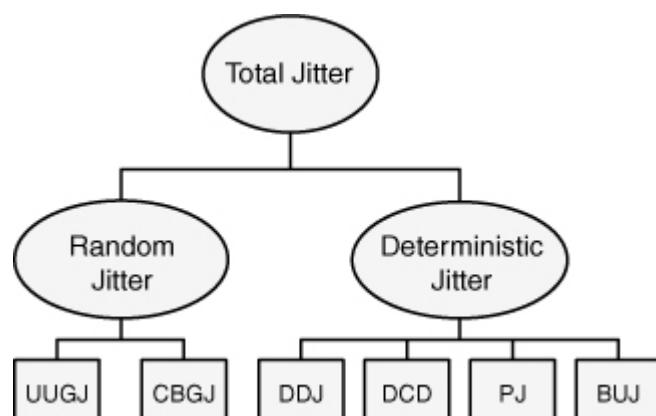
power on, and there is a high-frequency noise. Similarly there is a bounce after the state change when the current goes down. The noise produced is dependent on di/dt conditions for state-change events.

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6.4. Jitter Impact for Time Domain Analysis

Jitter is a timing variation of the signal in the system from the ideal signal due to both intrinsic and extrinsic noise. If intrinsic noise is a source of the jitter, it is also classified as Random Jitter (RJ). If the jitter is caused by design parameters that are predictable, it is classified as Deterministic Jitter (DJ). Total Jitter (TJ) is composed of RJ and DJ. [Figure 6.28](#) shows different types of jitter. Uncorrelated Unbounded Gaussian Jitter (UUGJ) and Correlated Bounded Gaussian Jitter (CBGJ) are part of random jitter. UUGJ is part of intrinsic noise because it results from the intrinsic nature of the material properties. UUGJ has a Gaussian distribution and the amplitude grows as time goes on. CBGJ has a Gaussian distribution but the amplitude is bounded. Transmitted signal amplitude shows a CBGJ characteristic. Four types of jitters are part of deterministic jitter. Data Dependent Jitter (DDJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Bounded Uncorrelated Jitter (BUJ) are part of DJ. DDJ is jitter-dependent on data pattern and the transfer function of the system. It is caused by the dispersion or limited bandwidth of the system channel. The jitter induced due to ISI is DDJ. DCD is the mean deviation of the clock signal from an ideal clock signal. Typically, rise and fall time mismatch causes DCD. PJ is repeating jitter with a periodic attribute. It is commonly related to ground bounce caused by the SSO. BUJ is a non-Gaussian jitter that does not typically belong to any of the categories of DJ and RJ previously described. The amount of these jitters in a channel demonstrates the quality and behavior of the channel.

Figure 6.28. Classification of jitter

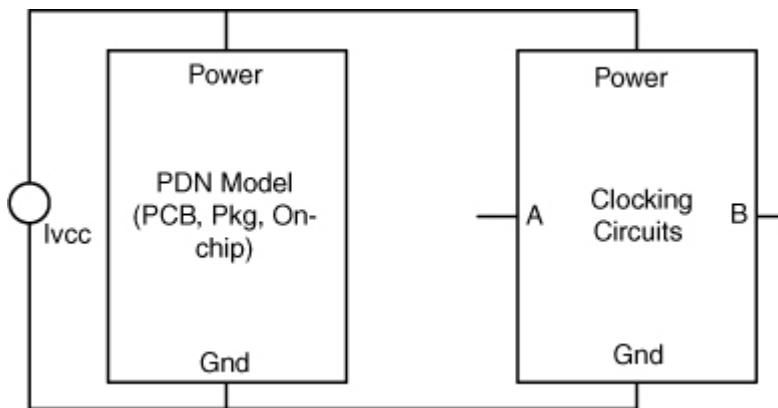


Jitter impact due to PDN noise is deterministic jitter. PDN fluctuation causes modulation of a buffer output signal that consequently contributes to the signal jitter. In this chapter, impact of PDN noise at the chip is analyzed without taking into account crosstalk or ISI.

6.4.1. Jitter Impact Due to PDN Noise

For the I/O interface stages other than the final stage, the noise produced in the PDN is subject to the circuits on that stage. There is a timing delay associated with this noise based on the circuit characteristics. [Figure 6.29](#) shows a block diagram for the jitter evaluation for the internal stage circuits such as clocking circuits.

Figure 6.29. Block diagram for clocking circuit jitter evaluation

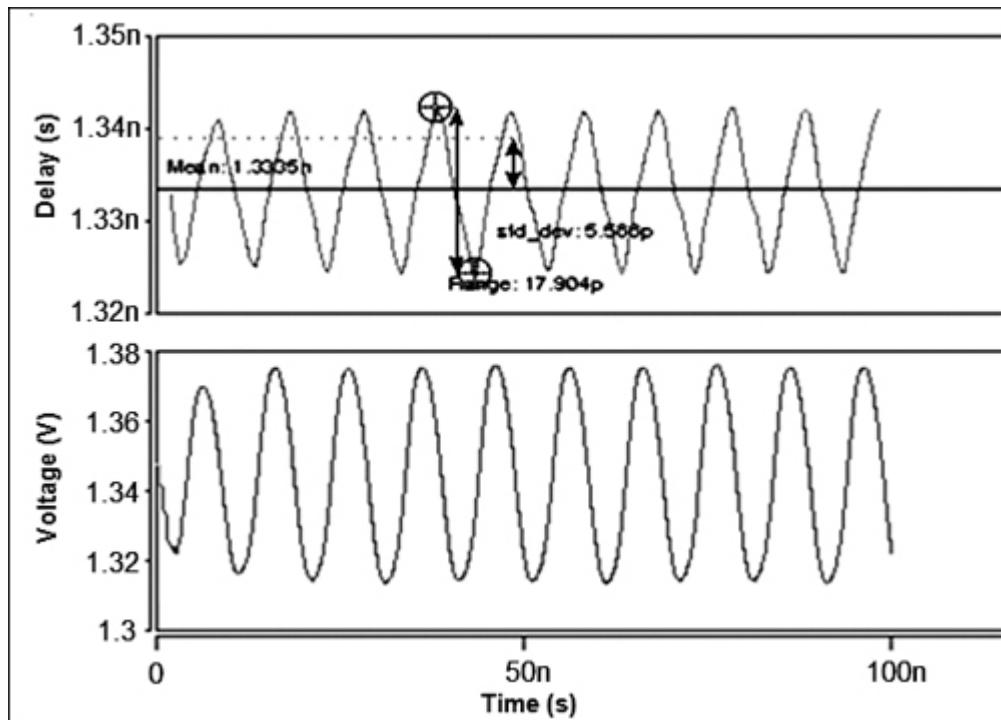


The power and ground nodes for the one clocking circuit are connected to the PDN model's power and ground nodes. Here the PDN model used comprises the PCB, package, and on-chip PDN, thus having all the parasitic elements. The current I_{VCC} is the total current for that power domain based on the activity for all circuits on that domain. The clocking circuit connected to the PDN model is the circuit in one path from A to B where jitter needs to be evaluated. Point A is near the core, and point B is near the final stage of the I/O. The current I_{VCC} on that domain produces the noise, and the jitter is introduced between points A and B.

This type of jitter impact can be in the Tx clock path or Rx clock path. An example of peak-to-peak jitter is shown in [Figure 6.30](#). The bottom plot shows the PDN voltage variations. The top plot shows the peak-to-peak jitter impact of about 17.9ps.

Figure 6.30. PDN noise and jitter impact for the clocking circuits

Source: V. Pandit and W. H. Ryu, "Power Integrity for I/O Interfaces," EPEP 2008, Tutorial. © [2008] IEEE.



6.4.2. Jitter Due to the SSO

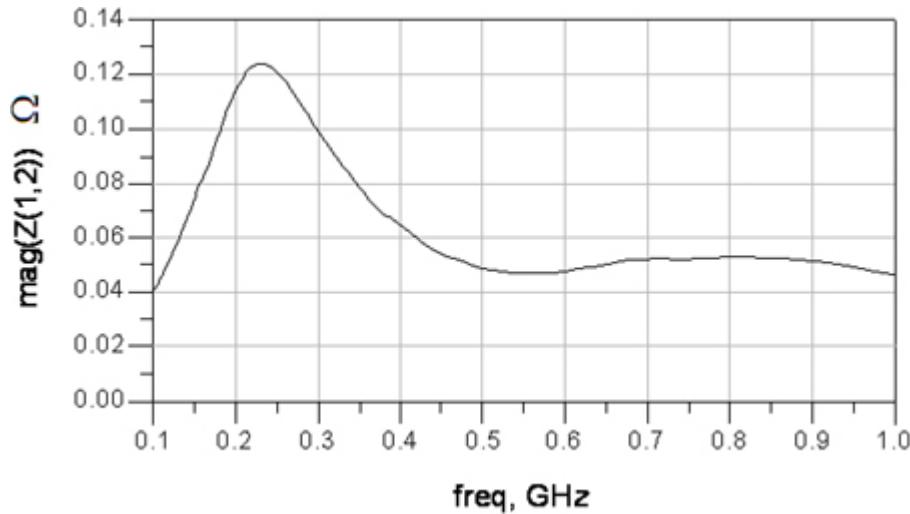
This section covers the power noise at the driver and its effect on the timing at the receiver. Both single-ended and differential SSO impact is evaluated in terms of jitter. [Chapter 8](#), “Signal/Power Integrity Co-Analysis,” addresses the other elements that affect the timing such as ISI and crosstalk and their interaction with the SSO noise. To evaluate the SSO-only jitter impact, the crosstalk is avoided by not transmitting the data on the neighboring transmission lines. Two cases are simulated for the jitter first without the SSO noise and second with the SSO noise. The difference in jitter impact due to these cases is attributed to the SSO noise at the driver.

6.4.2.1. Single-Ended System

As shown in [Chapter 5](#), for the CMOS push-pull driver, the SSO noise generated at the power node couples to the signal node. The Z_{12} transfer impedance is shown in [Figure 6.31](#), where port 2 is the power port and port 1 is the signal port.

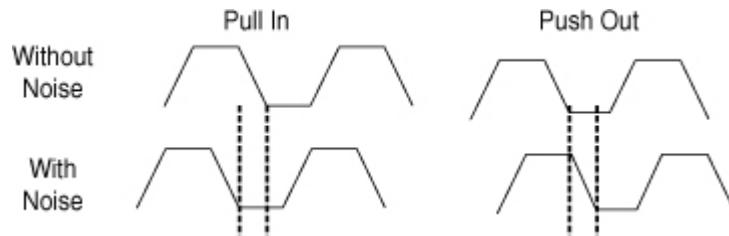
Figure 6.31. PDN to signal coupling at the chip

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



The noise on the PDN due to the simultaneously switching of the buffers introduces the timing delay, which has frequency-dependent variations. This timing delay can be pull-in or push-out, as shown in the Figure 6.32.

Figure 6.32. SSO pull in and push out



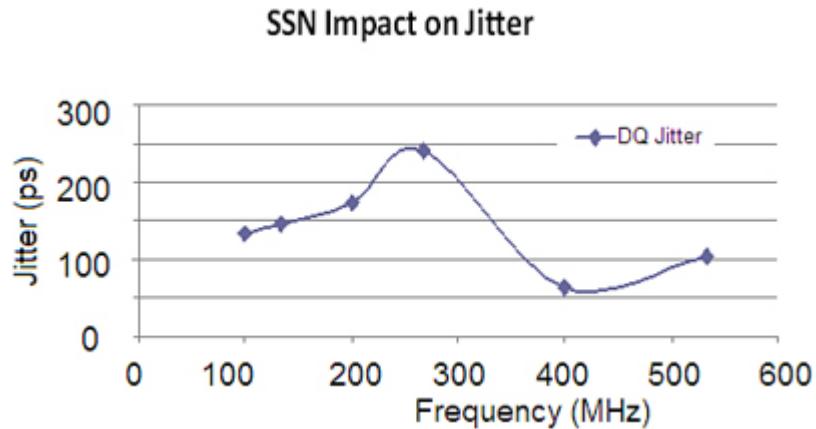
The SSO push out occurs when there is a voltage droop or reduced voltage. Due to lower voltage for the CMOS driver, the gate-to-source current decreases and propagation delay increases resulting in a push out. Similarly, due to increased voltage (bounce), the propagation delay decreases or pull in occurs. Due to the pull in and push out, the total eye width is reduced.

Data Line Jitter

Figure 6.33 shows the simulated jitter in the DQ data lines due to SSO [7]. For simulating the jitter introduced in DQ data lines, first the SSO power noise simulations are performed as described in the earlier section. Different noise signatures are obtained by varying the data pattern from 100MHz to 533MHz frequencies. The noise is injected in the 3D EM model of the channel. This channel model is end-to-end with the on-chip components, package, mother-board, and terminations. The total DQ jitter with the SSO noise is plotted against the frequency as shown in the figure.

Figure 6.33. Simulated jitter for the data line

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009, presentation.

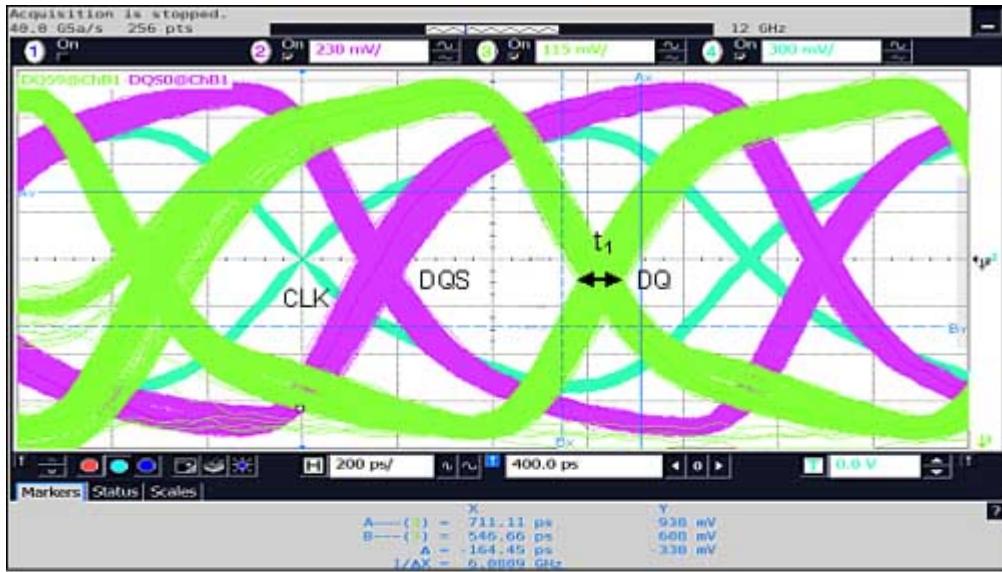


To correlate this jitter with the measurements, the measured eye diagram is plotted for a DQ data line. The data line is switching a 1010 pattern at the maximum frequency of the data rate (1067MP/s). The 7 data bits in that byte are kept quiet to avoid crosstalk due to the neighboring bits. All other bits in other modules are switching the SSO pattern. [Figure 6.34\(a\)](#) shows the measured eye diagram for DQ bit without the SSO, and [Figure 6.34\(b\)](#) shows the eye diagram with the SSO pattern. The SSO pattern in this case is 1100 for the data rate. The DQ and DQS waveforms are triggered on the system clock. The jitter due to the SSO can be determined by $t_2 - t_1$.

Figure 6.34. Measured DQ jitter without and with the SSO noise for 1100 pattern

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009, presentation

[\[View full size image\]](#)



(a) Without SSO



(b) With SSO

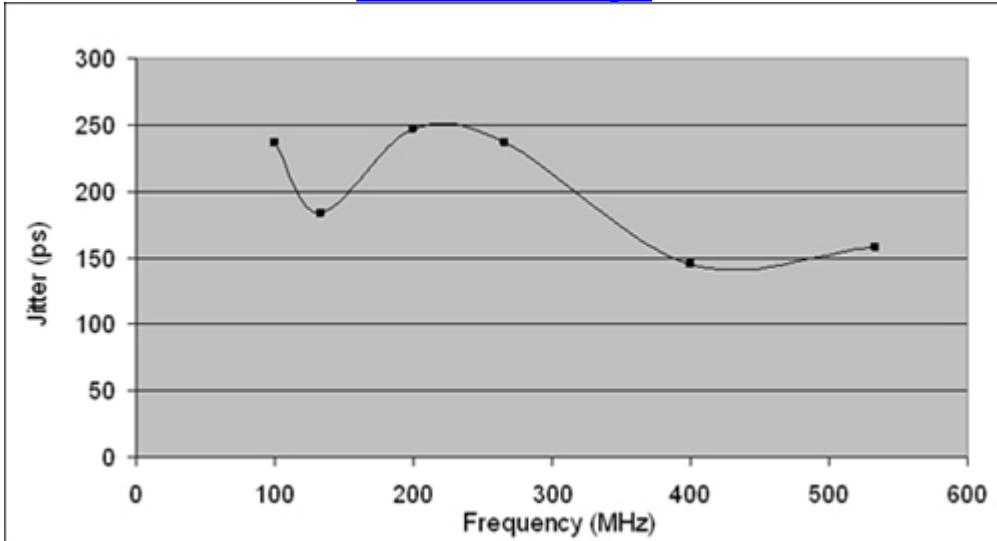
The same procedure is then repeated with the different data patterns for the SSO bits, such as 1010, 1100, and 11110000, to get the frequency response. Then, the eye width without the SSO is subtracted to that with the SSO noise. In all the measurements, the data line for which the jitter is measured is switching the 1010 pattern, even though the SSO bits are having different patterns. The result is the frequency dependent eye width degradation due to the SSO, as different frequencies.

Figure 6.35 shows the DQ jitter with the SSO, and it shows a close correspondence to the simulated DQ jitter. This jitter has a similar signature to the PDN to signal coupling, as shown in Figure 6.31.

Figure 6.35. Measured DQ jitter

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.

[\[View full size image\]](#)



Setup/Hold Time Jitter

Source synchronous interfaces have a clock or strobe with the data. Figure 6.36 shows the conceptual representation for the setup-hold times. The DQ data are sampled on the DQS strobe edge. The setup time is from the beginning of the data valid window to the strobe edge, and the hold time is from the strobe edge to the end of the data valid window. Typically the strobe and the data buffers are on the same power domain. The SSO noise affects both the data and strobe. There is a jitter introduced on the data and strobe due to the SSO. As a result there is a net degradation to the available data valid window. Figure 6.37 shows the measured timing window degradation due to the SSO noise [7].

Figure 6.36. Setup and hold time

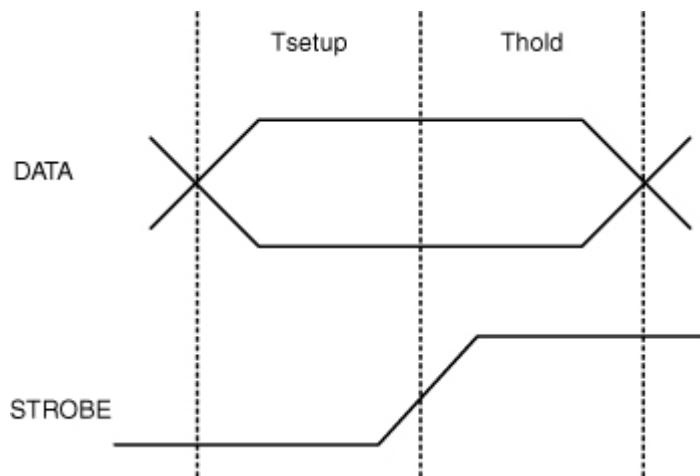
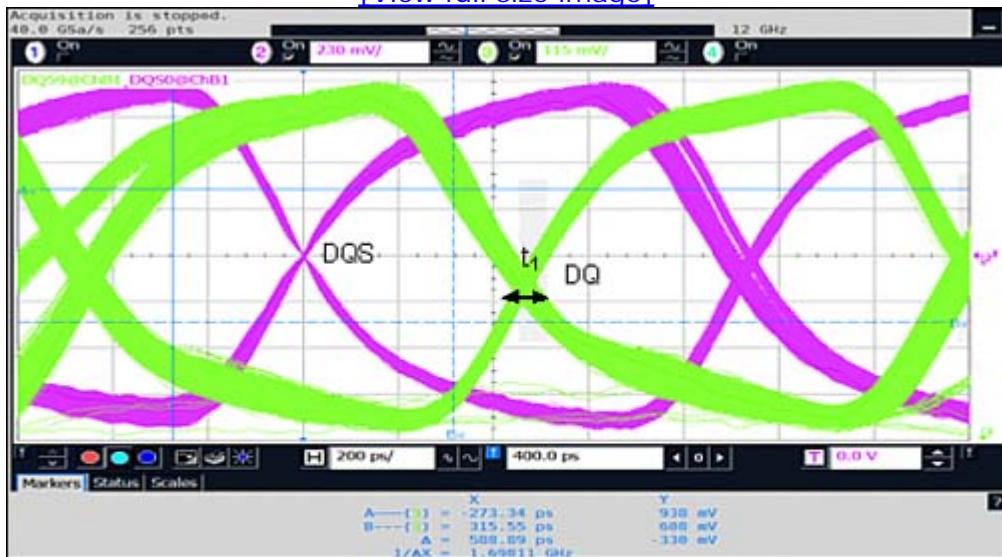


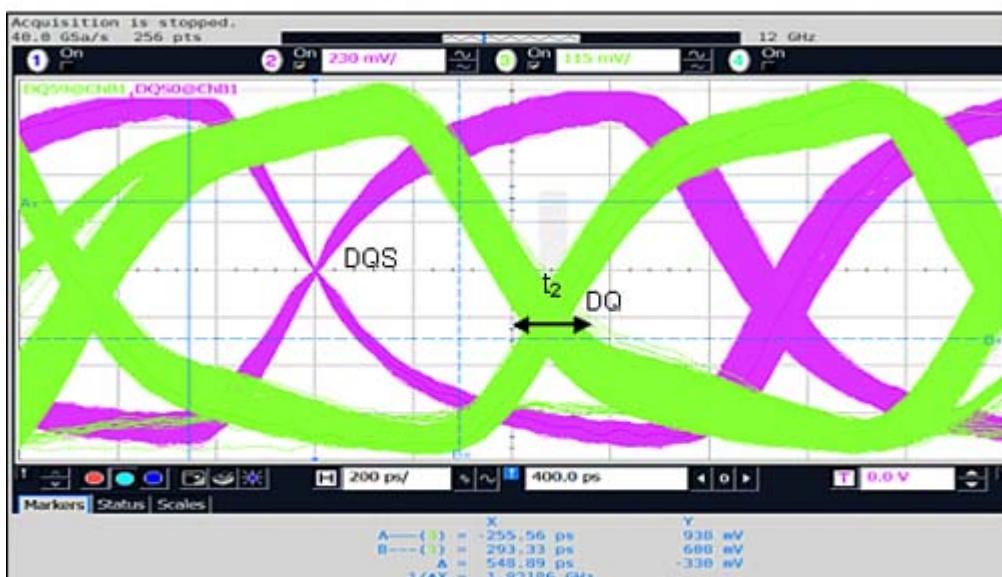
Figure 6.37. Setup/hold time without and with SSO noise for 1100 pattern

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO

[View full size image]



(a) Without SSO



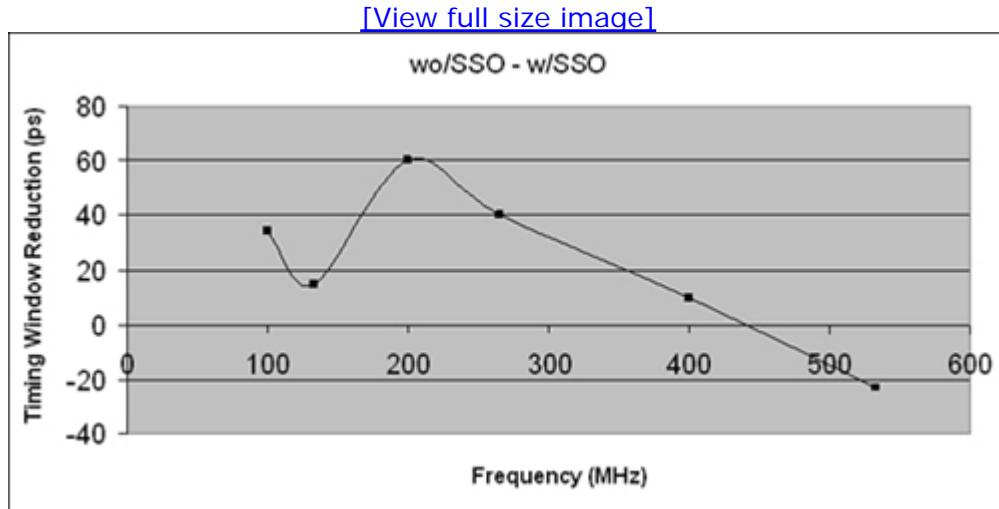
(b) With SSO

A similar setup is used as that for DQ jitter measurements. All the SSO bits at the driver are switching at the same pattern 1100, for the 1067MT/s data rate. At the receiver end, crosstalk bits are turned off. Two measurements are taken: one with the SSO and the other without the SSO, as shown in Figure 6.38. For both measurements, the victim bit is toggling a pattern of 1010. The DQ is now triggered on DQS and the timing window is captured. With the SSO there is some degradation in the timing window. It can be determined by measuring the difference in the timing window or by determining $t_2 - t_1$. Next, the SSO data pattern is changed and the entire procedure is repeated for the 1010, 1100, and 11110000 SSO data patterns. The difference between the timing window without the SSO and that with the SSO is plotted, as shown in Figure 6.38. Different frequency

components are evaluated.

Figure 6.38. Timing Window reduction due to the SSO

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, "SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity," DesignCon 2009.



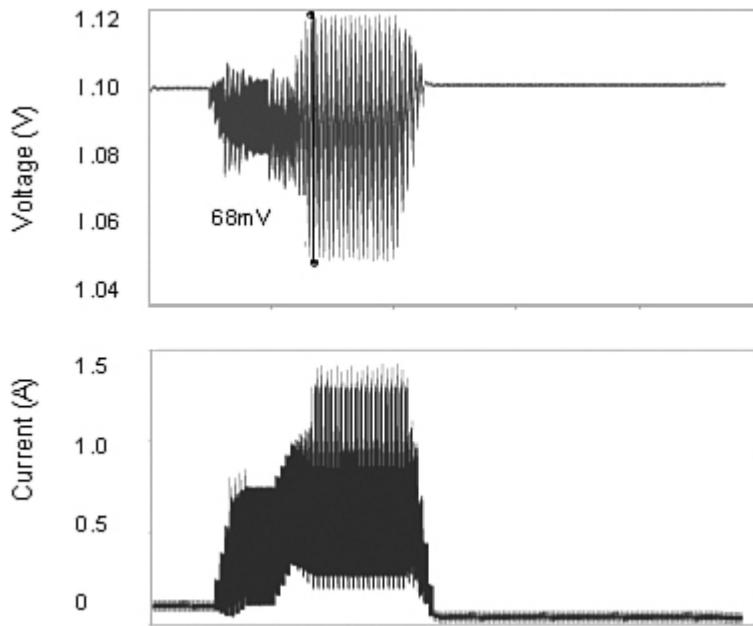
This jitter waveform signature corresponds to the PD-to signal coupling signature, as shown in Figure 6.31. It shows a negative timing window reduction due to the SSO at higher frequencies. It may be due to interaction of the ISI and SSO noise phases.

6.4.2.2. Differential System

As described in the earlier section, the final stage of the differential driver has high-frequency components in the $I_{cc}(t)$ profile of the power domain. If the driver is powering on, there is an initial DC step, and then there is a high-frequency current with a certain DC level. If there are prior-stage circuits on the same domain, the total $I_{cc}(t)$ needs to be captured. Figure 6.39 shows an example of the $I_{cc}(t)$ for the entire interface when all the drivers, receivers, and other stages are on the same domain and active simultaneously. The noise produced is about 68mV [9].

Figure 6.39. $I_{cc}(t)$ current and noise for the differential interface

Source: M. J. Choi and V. Pandit, "SI/PI Co-analysis for I/O Interfaces," IBIS Summit, July 2009.

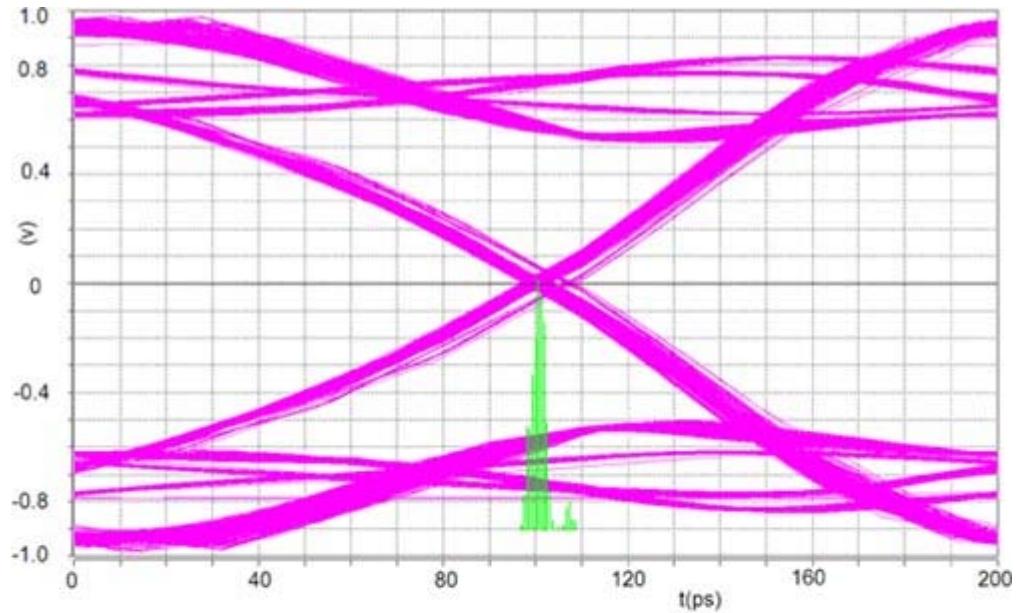


The jitter of the differential system at the receiver is evaluated in simulations. First, only the differential driver is transmitting the signal without any other driver/receiver active. The resultant jitter is simulated and is due to the ISI, as shown in Figure 6.40(a). For this simulation, the neighboring bits are not transmitting, so there is no crosstalk noise.

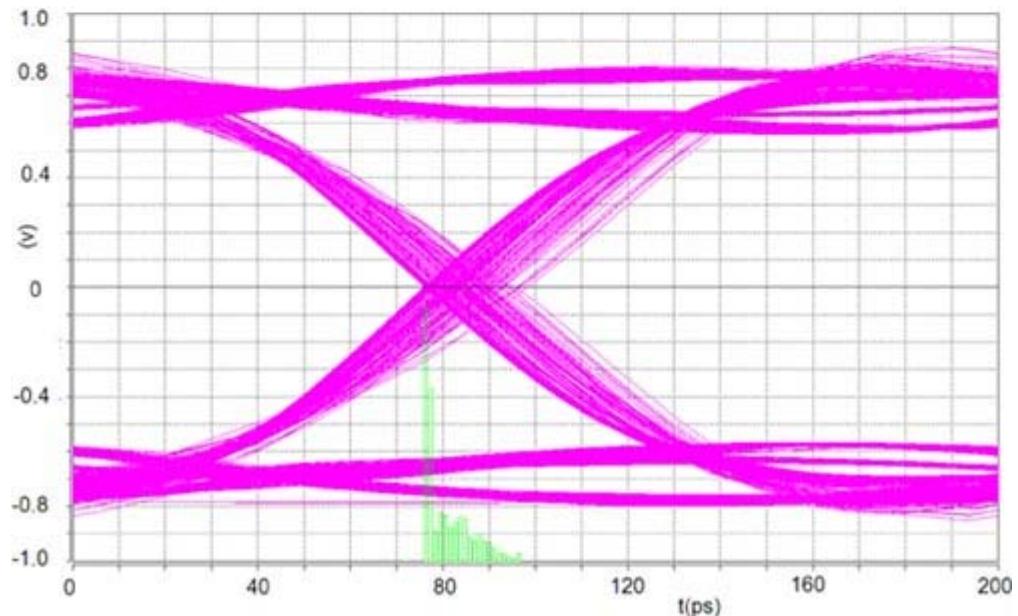
Figure 6.40. Differential eye margin (a) without SSO and (b) with SSO

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

[\[View full size image\]](#)



(a) Without SSO



(b) With SSO

Next, the current $I_{cc}(t)$ previously shown is injected in the power node of that driver. This replicates the entire interface being active. The purpose of the simulation is to determine the jitter impact due to the SSO noise. In this simulation, no neighboring transmission lines are used to avoid crosstalk. Because of the $I_{cc}(t)$, the noise is produced in the driver power node. The jitter at the receiver is simulated, as shown in Figure 6.40(b). The EYE margin without and with the SSO noise is measured, and the difference is 10ps.

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Chapter 7. Signal/Power Integrity Interactions

As the Printed Circuit Board (PCB) interconnection density and channel data rate increasingly intensify, various 3D electromagnetic effects, crosstalk, and discontinuity-induced ISI represent an even more significant role for both signal channels and power distribution networks. In particular, noise coupling between signal trace and power delivery network constitutes a key issue and performance limiter for the high-speed I/O interface, which must be addressed appropriately. Understanding these combined signal integrity and power integrity issues in the era of gigahertz data rate requires advanced co-design methodology for signal integrity and power integrity analysis. In this chapter, we describe power/signal integrity interaction mechanism, including power noise coupling onto signal trace and noise amplified through signal resonance.

The first part of this chapter demonstrates root-cause analysis through two case studies: investigations of a memory double data rate (DDR) control bus resonance problem and DDR Vref bus noise issue. With traditional signal integrity simulations that consider an ideal power delivery system, these issues may not be observable until the post-silicon validation stage. With the co-design methodology, however, as root-causes of these issues are identified, more cost-effective resolutions become apparent at the presilicon design stage. Design guidelines, which were summarized from the two case studies regarding noise coupling by 3D effect and resonant structure follow:

- Plane coupling noise is limited to be a small fraction of the signal voltage swing at the transition layer.
- To reduce plane-signal coupling, it is recommended that no reference layer change occurs unless absolutely required.
- The stitching distance has to be much shorter than the wavelength of the third harmonic of maximum digital frequency.
- Signal resonances need to be alleviated by keeping out critical lengths

such as half and quarter wavelength at frequencies of interest. Cavity resonances also need to be mitigated by close spacing between power and ground planes.

The latter part of the chapter discusses the effects of referencing and stitching for the single-ended interface by evaluating power-to-signal transfer impedance. Then, for the differential interface, the effects of different types of stitching schemes are evaluated for ISI and crosstalk. Finally, EMI trade-off for different power plane structures is addressed.

7.1. Background

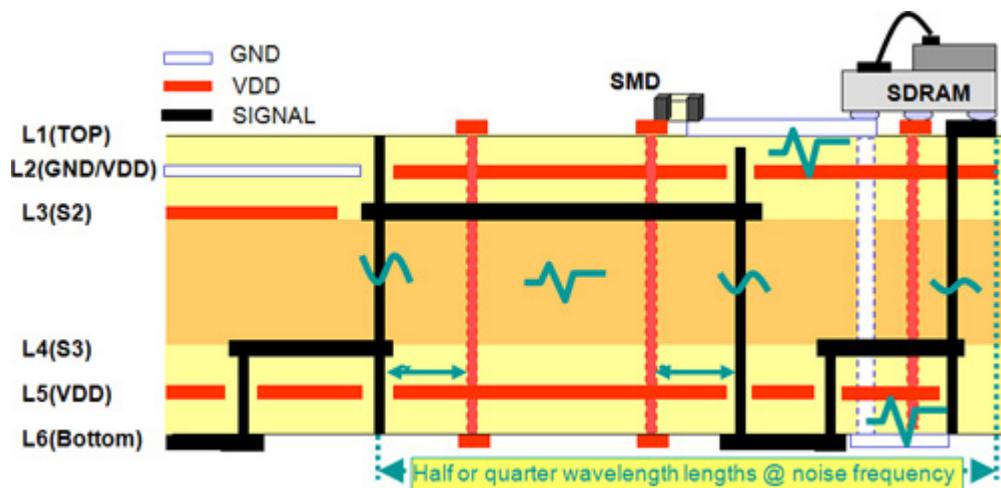
As data rate exceeds multi-GHz bandwidth, even at board level, faster signal transitions are required. Such signals can generate larger common mode noise including crosstalk, simultaneous switching output noise (SSO), signal reflection, and plane noise-induced signal resonance. In multi-GHz bandwidth interconnect systems, such as multiprocessor computer systems; it is essential to predict signal resonance effects induced by power-ground plane noise. Conventional design flow separates the design of the power network and signal network but does not predict interactions between the two. A new co-design methodology has been proposed that simultaneously considers signal routing and power network design under integrity constraints [1]. The key part of this approach, a simple yet accurate power network estimation formula, decides the minimum number of power nets needed to satisfy both the power and signal integrity constraints prior to a detailed layout. This chapter describes a systematic approach to determine the interaction between power and signal networks, at the interconnect level. It is necessary to develop co-modeling and co-simulation methodology of signal integrity and power integrity, a one-pass solution to the co-design of power and signal networks in the sense that no iteration between them is required to meet design closure

As shown in [Figure 7.1](#), SSO comes from the chip and propagates through the power-ground plane. The noise is coupled onto the resonant structure on the signal trace through the reference transition. As the data rate goes higher, the coupling coefficient between the plane and the signal generally increases. Chips, packages, and boards have been designed separately for a number of years. However, as the electrical length of the 3D structure grows, accurate 3D Electro-Magnetic (EM) modeling is required. Rising interconnect density and high-speed interfaces running at the GHz level prompt a shift to co-design, which comes at an added expense. Although it is difficult to obtain the appropriate pinouts across chips, packages, and boards, managing signal integrity and power distribution across those elements proves even more difficult. Consequences may include problems with resonance, signal crosstalk, impedance discontinuity, and reference transitions. In extreme cases, signal resonance due to power noise, has caused the failure of systems, forcing re-spins and even resulting in

negative financial impact for some companies. To mitigate these effects, expensive redesigns of power-ground systems and signal referencing may be required, with increased layers in packages or boards, or with an excessive number of stitching vias. A ground (or power) stitching via may be placed next to a signal net as it passes from one layer to another and provides a ground (or power) reference to that signal.

Figure 7.1. Interaction between power-ground planes and signal trace

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.

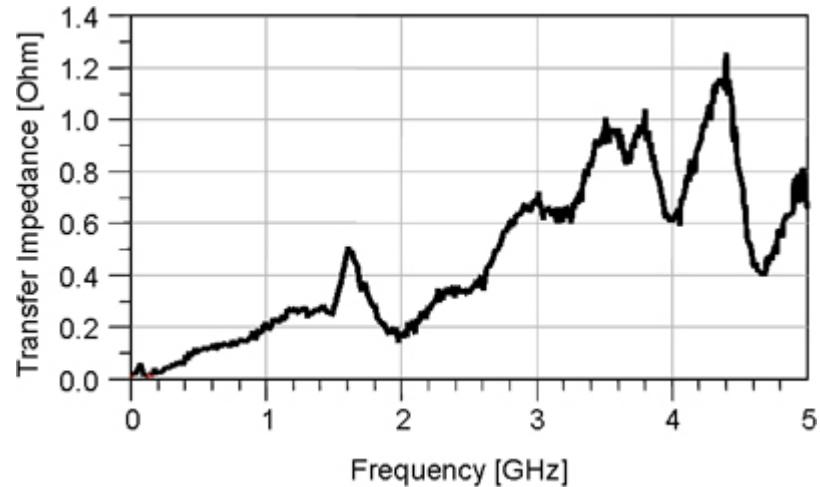


In high-speed systems, the system SSO causes various problems, such as logic failure, EMI, timing delay, low voltage margin, and skew. As the previous paragraph describes, when the SSO is generated, it could significantly be coupled onto signal traces, causing severe resonance problems. As Figure 7.2 shows, Vector Network Analyzer (VNA) data with two stitching vias at a distance of 100mils from signal via transition, show large plane-to-signal coupling in the GHz interface. It is necessary to model the coupling between the plane SSO noise and interconnection lines in multilayer boards. An increase in board and package complexity and density results in signal traces with more vias, more segments, and many more discontinuities as they traverse through the board and package. When most of the routings in board and package designs are contained on only one or two layers, cross-sectional geometries and general design rules yield acceptable performance. However, when trace routings have significant lengths on many layers, a trace-path can easily contain four to eight vias, and 2D channel modeling exposes its limitations. Even worse, ever-increasing edge rates enable signals to “see” the increased number of discontinuities; the primary reason 3D modeling becomes important for high-speed system interconnects. In some ways, 3D modeling extends the frequency range across that with more accurate models. Several papers describe the SSO coupling mechanism through the signal via exchanging

reference planes in a multilayer board [2, 3].

Figure 7.2. Measured plane-to-signal transfer impedance

Source: W. H. Ryu, M. Wang, "A Co-design Methodology of Signal Integrity and Power Integrity," DesignCon 2006.



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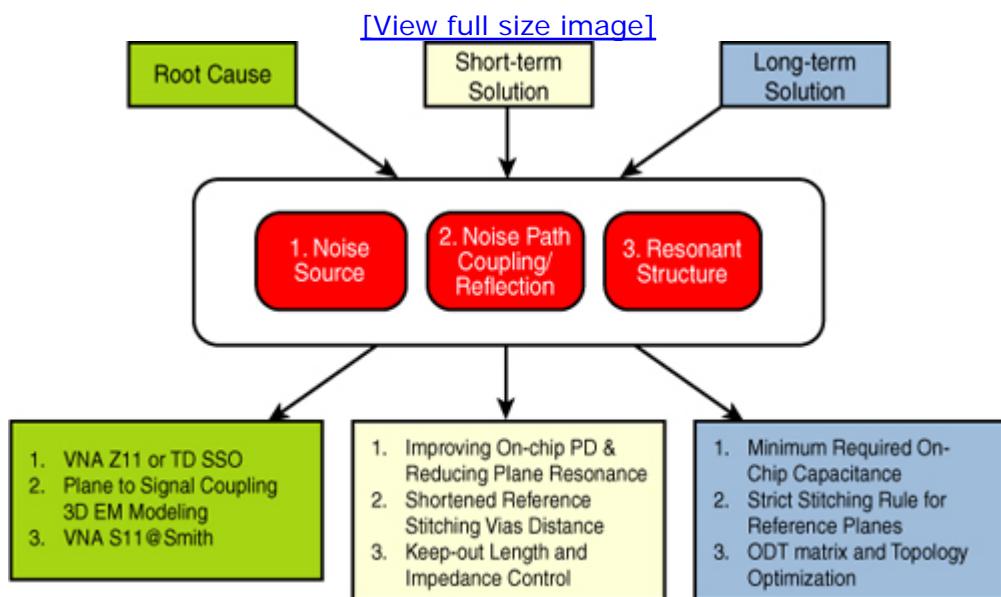
7.2. Root Cause Analysis

As shown in Figure 7.3, in signal-power integrity co-design for multi-GHz bandwidth interface, the following three mechanisms need to be considered:

- Noise sources, that is, ISI, crosstalk, power/ground noise (SSO)
- Noise coupling path between signal and signal or plane and signal trace
- Resonance on victim trace and cavity

Figure 7.3. Approach to indentifying root cause and solutions of noise amplification through channel resonance

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



Accordingly, there are three major steps to investigate plane noise-induced signal resonance problems: First, root-causing the issue through VNA and TDR measurements and 3D EM analysis; second, determining short-term cost-effective solution investigation; and third, conducting a long-term

solution study. In terms of root-cause study, the first step is to identify the noise source, for example crosstalk noise, SSO noise, and signal reflection noise. This can be accomplished through EM modeling and VNA plane input impedance (Z_{11}) measurements and system validation with various signal patterns. VNA data can also be used to get an accurate 3D EM model through a correlation study. The second step is to determine the noise coupling path. If the noise comes from a power-ground plane, noise coupling mechanism needs to be identified with not only VNA plane-to-signal coupling measurements but also well-correlated 3D EM modeling; including PCB, package, and chip-level power-signal interactions. The final step is to investigate the resonant structure on the signal trace by using VNA return loss (S_{11}) data at the Smith chart and empirical material property, based on frequency-domain simulation.

The typical short-term solutions to alleviate plane noise induced signal resonance would be adding an on-chip decoupling capacitor, replacing the plane shape, reducing stitching via distance, and controlling resonant trace lengths and trace impedance. For the long-term solutions, minimum requirement of on-chip decoupling capacitance, design rule of stitching via for transition layers, and optimum on-chip termination matrix and topology need to be developed, based on co-simulation of power-signal integrity. In this chapter, we describe a robust design guideline to achieve the following conditions:

- Plane noise specification is required to be less than $\pm 3\%$ of the signal voltage swing at the transition layer.
- No reference layer change is permitted unless absolutely necessary.
- Resonance needs to be alleviated by keeping out critical lengths such as half and quarter wavelength at frequencies of interest. The stitching distance has to be much shorter than the wavelength of the third harmonic of maximum digital frequency.

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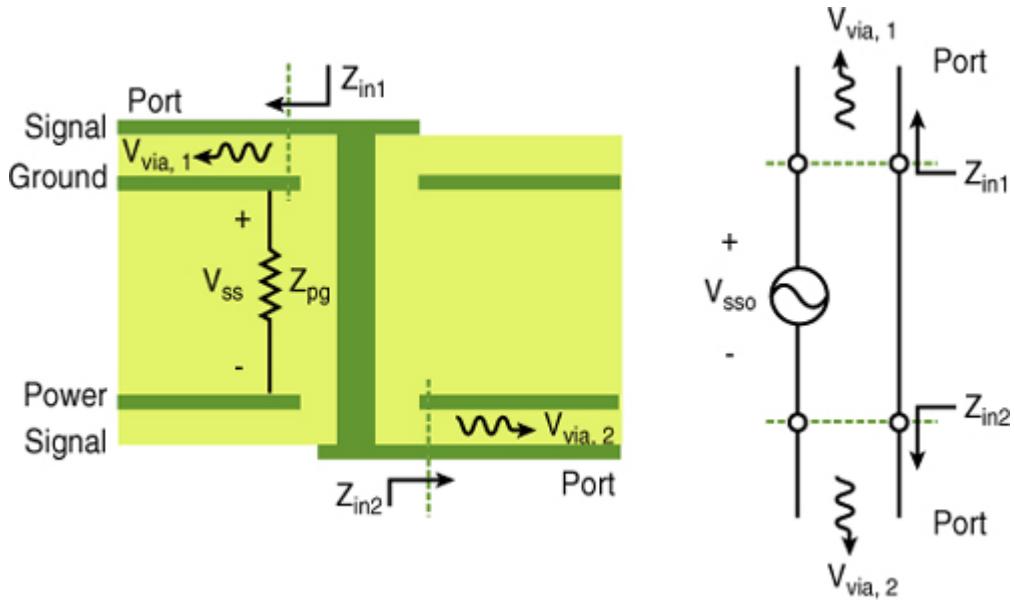
7.3. SSO Coupling Mechanism

A high-frequency signal trace must have its reference plane to guarantee the return current path. In other words, as frequency goes higher it is essential to minimize the RF inductive effect and plane noise coupling to improve the bandwidth of the signal interconnection line. In a multilayer board, the ground plane and the power plane can be used as a reference for the signal line. Therefore, it is possible for signal traces to route on different layers of a module. For example, interconnects for multibit data signals in a memory module can take the different layers on the module. Various line segments are required to connect a signal net in the multilayer module. The signal line structures are divided by whether they consist of a stripline or a microstrip line, and whether they change the reference plane. The SSO generated by the current consumption of the driver chips is coupled to signal through the following two coupling mechanisms [3, 4].

Figure 7.4 shows the first SSO coupling mechanism through the reference changing via in a typical six-layer memory module. As the memory module requires multiple layers to route effectively many signal lines in a limited space, the reference changing via is used to transit the signal. The signal reference changes from ground plane to power plane or from power plane to ground plane. Through-hole signal vias that penetrate power/ground plane pairs could cause noise coupling between signal and power/ground planes. When driver chips consume a large number of instant currents, the SSO generated near the reference changing via has a relation with power/ground cavity impedance near the via, which is frequency-dependant [4, 5]. The higher the power/ground cavity impedance, Z_{pg} , the higher the SSO voltage, V_{SSO} . In addition, V_{via1} and V_{via2} , the SSO voltages coupled to each port of signal line, are proportional to input impedances of two transmission lines. They are obtained as equations (7.1) and (7.2).

Figure 7.4. SSO coupling through the reference changing via in typical six-layer PCB

[\[View full size image\]](#)



Equation 7.1

$$V_{via1} = \frac{Z_{in1}}{Z_{in1} + Z_{in2}} \cdot V_{SSO}$$

Equation 7.2

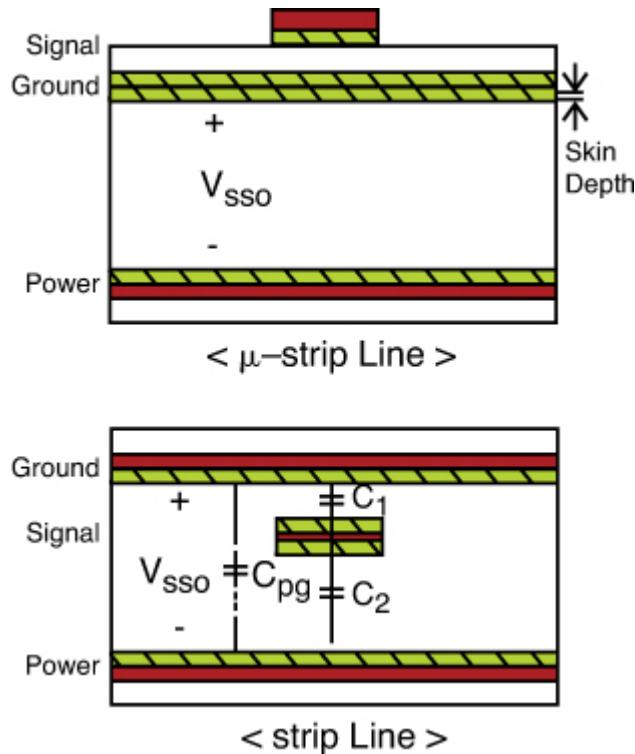
$$V_{via2} = \frac{Z_{in2}}{Z_{in1} + Z_{in2}} \cdot V_{SSO}$$

If input impedances, Z_{in1} and Z_{in2} , of two transmission lines are 60 Ohm, one-half of V_{SSO} is coupled to the signal.

The second coupling mechanism is the SSO coupling to signal through the trace between the power and ground plane, as shown in [Figure 7.5](#). If the thickness of the power or ground plane is not smaller than the skin depth, the SSO is not coupled to a microstrip line located out of the power/ground plane pair. Consider that power or ground plane thickness is 18 μm and the skin depth is about 18 μm at 10MHz; there is no coupling for the SSO over about 10MHz. On the other hand, when a signal trace is located between the power and ground plane, the SSO is capacitively or inductively coupled to the signal trace. However, the SSO coupling to the trace is much smaller than that, compared to the reference changing via. The SSO coupling to signal by the two mechanisms previously mentioned affects signal integrity in high-speed PCBs and modules. To understand SSO coupling and amplification mechanism, it will be required to translate SSO noise into receiver voltage and timing impact. Similarly signal-to-signal interaction through via reference transition becomes more important in the high-speed I/O interfaces. When there is a transition of a signal via between two

reference planes, a plane wave is launched into the cavity between those two planes. That plane wave can be “shorted out” by nearby stitching vias if the two planes are ground planes. However, if there are other signal vias near that plane wave launch point, there is strong coupling into those vias, and it constitutes a major source of crosstalk, especially for thick boards with long vias.

Figure 7.5. SSO coupling through a trace in typical six-layer memory module



The following sections describe two case studies: a DDR2-800 control bus resonance problem and a DDR2-667 Vref bus noise issue. DDR2 is a double data rate synchronous dynamic random access memory interface. DDR2-800 and DDR2-667 are running at 800MT/s and 667MT/s, respectively. DDR2-800 control bus is running at 200MHz. Both problems were approached from three key aspects: Noise source, noise coupling path, and noise excitation structure. With traditional signal integrity simulations that consider an ideal power delivery system, these issues may not be observable until the post-silicon validation stage. With the combined signal/power integrity analysis, however, as root-causes of these issues are identified, cost-effective resolutions become apparent at the pre-silicon design stage. Design guidelines can be drawn from the two case studies regarding noise sources, 3D electromagnetic coupling paths, and resonance effects. The same principles can be extended for higher frequency interfaces.

The underlying mechanism of the control resonance issue has been

diagnosed as follows: First, the source of a significant amount of noise at 900 MHz is the simultaneous switching of data signals. Second, the noise coupling path between the power/ground planes and control signal trace is mainly three transitions of reference planes. Third, the noise becomes excited due to the 900 MHz resonant structure on control tree topology. There is one-half wavelength resonance between SDRAM devices and one-quarter wavelength resonances between T-junction to SDRAM device.

The second case of the Vref noise issue on DDR2-667 displays a similar mechanism, although the resonance frequency is 1GHz, which is the third harmonic of the data signal frequency 333 MHz, rather than 900 MHz. The proposed root cause approach for signal/power integrity combination effect starts from frequency-domain analysis with S-parameters and impedance profiles, then establishes on-die models with lab measurements, and finally confirms results with time-domain signal integrity simulations. All theoretical analyses have been verified through VNA and TDR measurements and combined signal/power integrity analysis with full-wave 3D or planar 3D EM simulation tools.

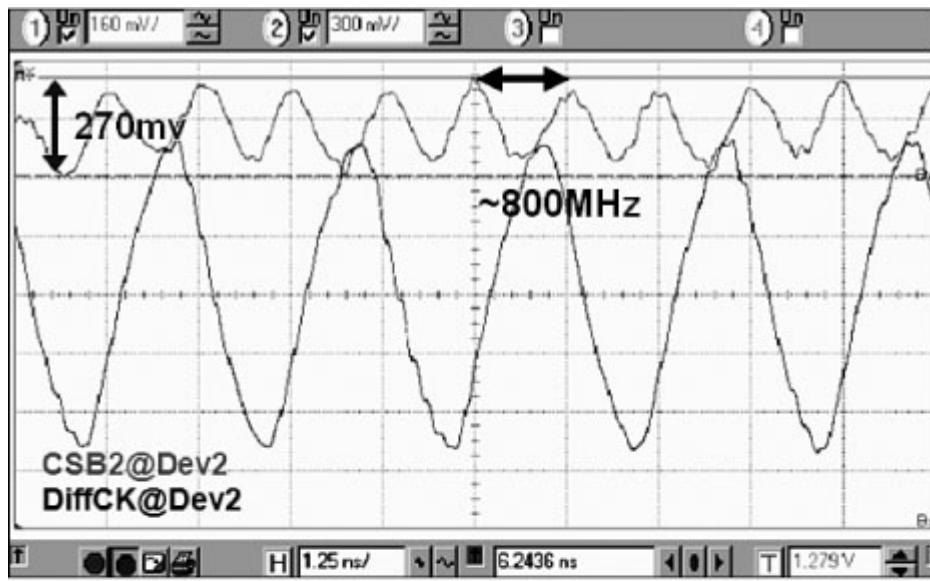
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7.4. Case Study I: DDR2 800 Control Signal

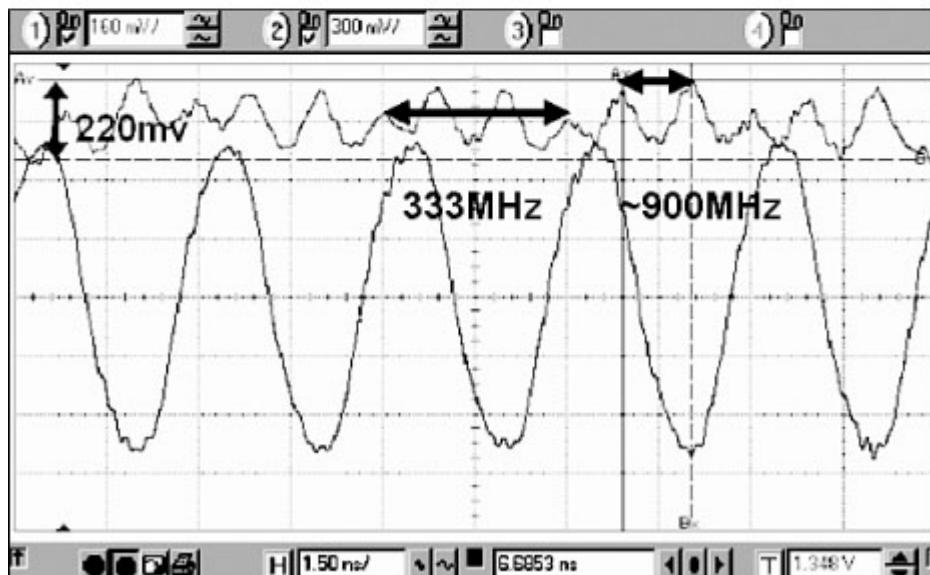
The study investigated root-cause of the resonance problem on DDR2-800 Dual In-line Memory Module (DIMM). It has 400-MHz clock signals and 200-MHz control signals. Cost-effective short-term and long-term solutions are proposed to resolve the problem. As shown in [Figure 7.6](#), resonance noises at 800 MHz and 900 MHz were observed on DDR2-800 and DDR2-667 control networks during the memory device write mode, respectively. The second harmonic frequency of 800 MT/s and the third harmonic frequency of 667 MT/s are 800 MHz and 900MHz, respectively. The peak to peak noise was 270mV for DDR2-800 and 220mV for DDR2-667. The resonance degrades the timing margin by around 270ps according to [Figure 7.7](#). In this example, the setup and hold window of the Chip Select (CS) signal had more than 250ps at Vref uncertainty introduced due to the memory device data driving SSO even without considering any changes to slew rate derating.

Figure 7.6. Resonance on the control trace

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” Design-Con 2006.



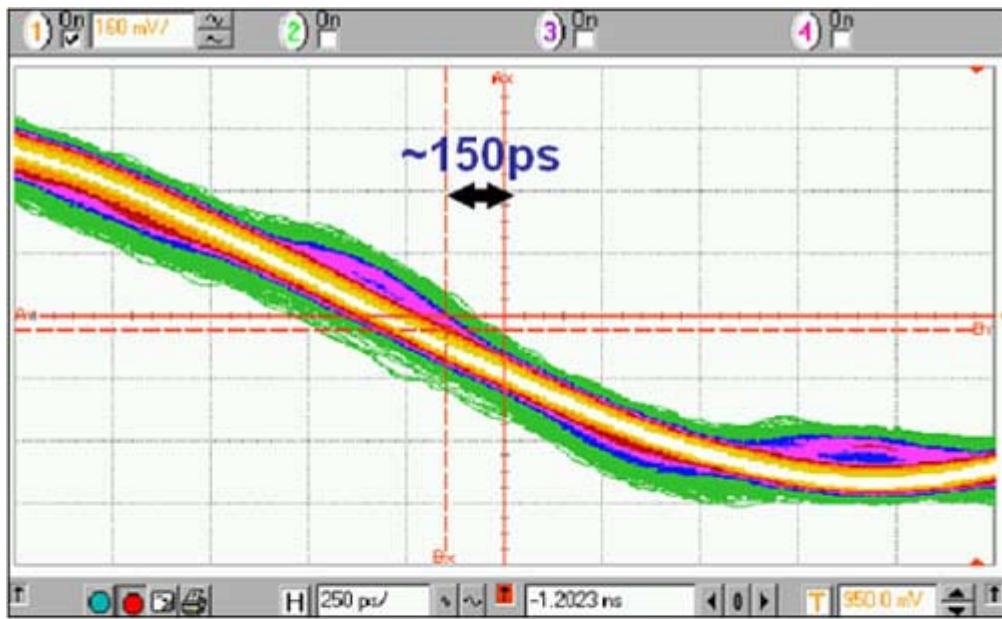
(a) DDR800



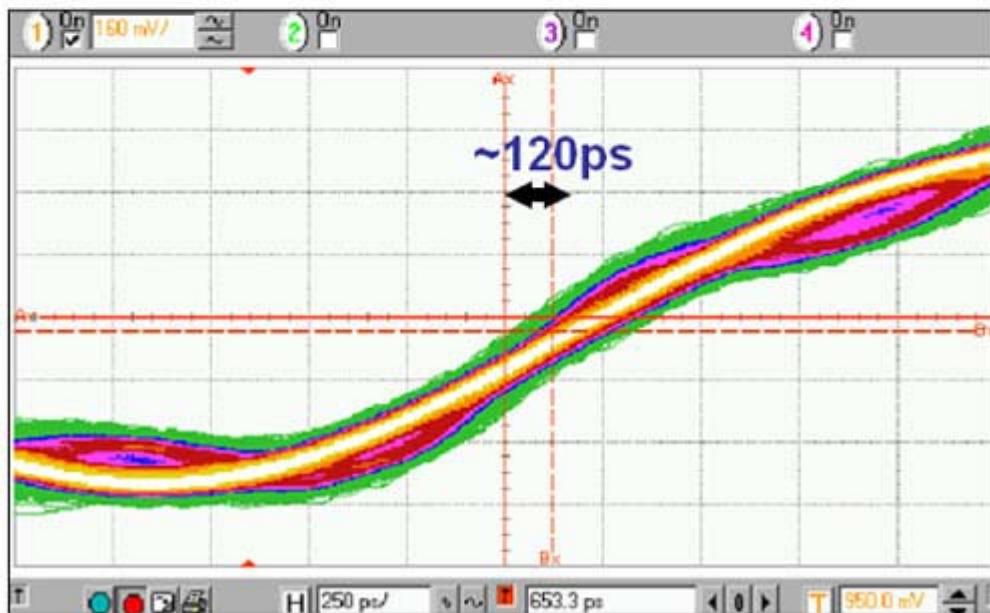
(b) DDR667

Figure 7.7. Margin loss of around 270ps due to power noise induced signal resonance

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



(a) Setup margin loss



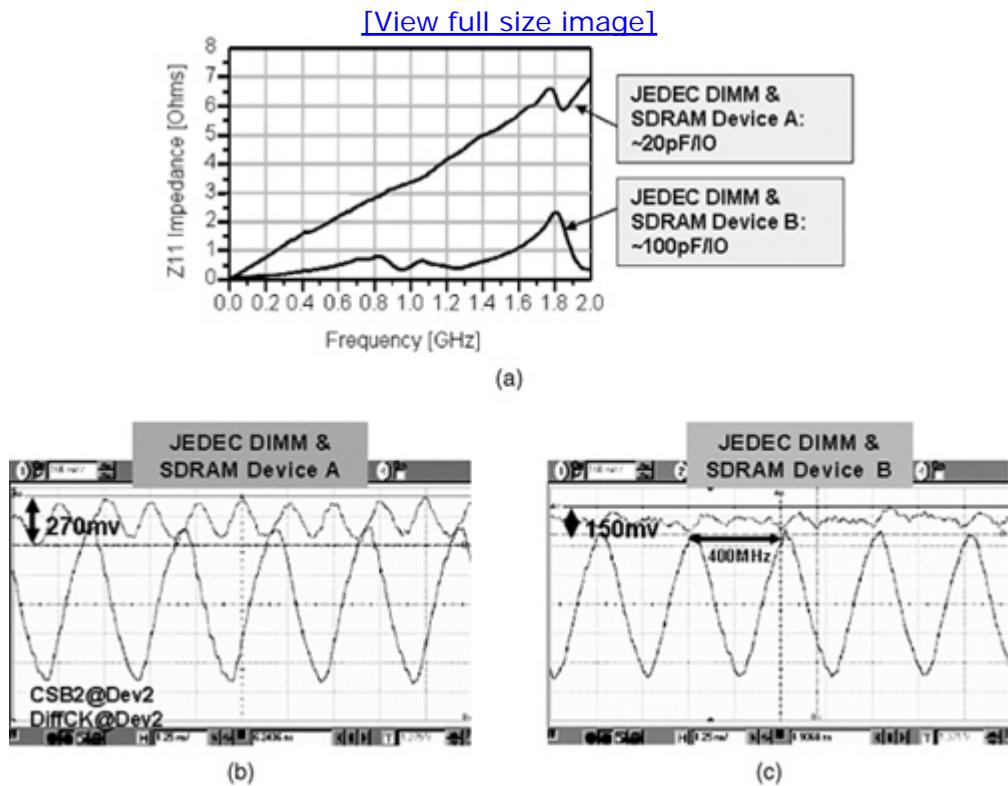
(b) Hold margin loss

7.4.1. Noise Source

Based on the time-domain waveform capture in Figure 7.8 and noise spectrum analysis, the noise magnitude is dependent on the data switching pattern and the plane impedance. The noise has a frequency of around 800MHz, the second harmonic of DDR2-800. The second harmonic noise normally evolves from the SSO generated by data switching.

Figure 7.8. SSO noise source comparison between SDRAM device A and SDRAM device B: (a) Measured Z11 at SDRAM package ball; (b) and (c) Control signal resonance at 800MHz induced by 800MT/s data of SDRAM device A and SDRAM device B.

Source: W. H. Ryu and M. Wang, "A Co-design Methodology of Signal Integrity and Power Integrity," DesignCon 2006.

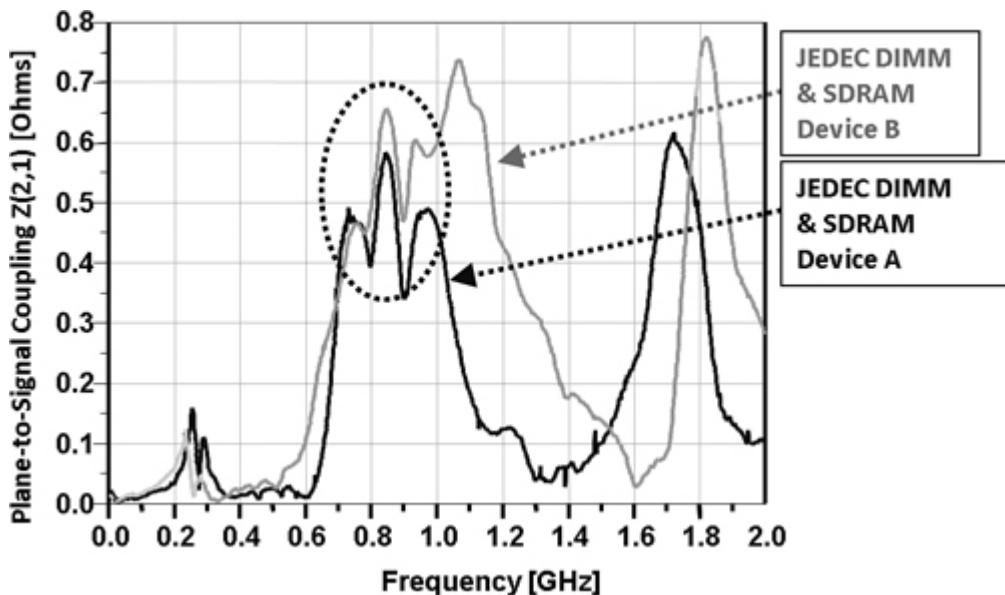


7.4.2. Coupling Mechanism

Figure 7.9 shows plane-to-signal coupling impedance measured by using 2-port VNA. Large coupling coefficients are observed between 700MHz and 1GHz; due to imperfect stitches between reference layers. The coefficient of JEDEC DIMM and SDRAM device A appear comparable to that of JEDEC DIMM and SDRAM device B up to 800MHz, due to a similar DIMM board design. However, the discrepancy between SDRAM device A and SDRAM device B increases over 1GHz, because on-chip parasitic impact becomes more significant. The second harmonic frequency noise of DDR2-800 and the third harmonic frequency noise of DDR2-667 are easily coupled onto signal trace through the coupling structures.

Figure 7.9. Measured plane-to-signal coupling of JEDEC DIMMs with SDRAM device A versus device B

Source: W. H. Ryu and M. Wang, "A Co-design Methodology of Signal Integrity and Power Integrity," DesignCon 2006.



7.4.3. Resonant Structure on Control Networks

The final point to understand the resonance mechanism involves the resonant structure on the signal trace. As shown in Figure 7.10, both SDRAM device A and SDRAM device B mounted on the JEDEC DIMM have the same resonant frequency, around 900MHz. Extensive simulation and TDR measurement data on DIMM have shown the resonance is caused by a half wavelength mode between two branches, as shown in Figure 7.11.

Figure 7.10. Measured resonance on control trace of (a) SDRAM device A ($M1 = \sim 900\text{MHz}$) and (b) SDRAM device B ($M2 = \sim 900\text{MHz}$) on the JEDEC DIMM

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” Design-Con 2006.

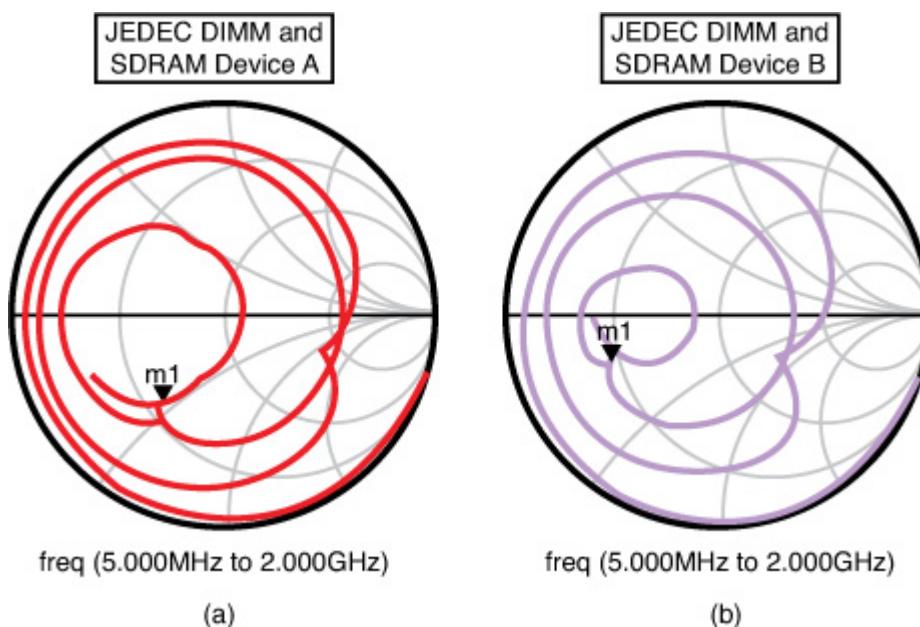
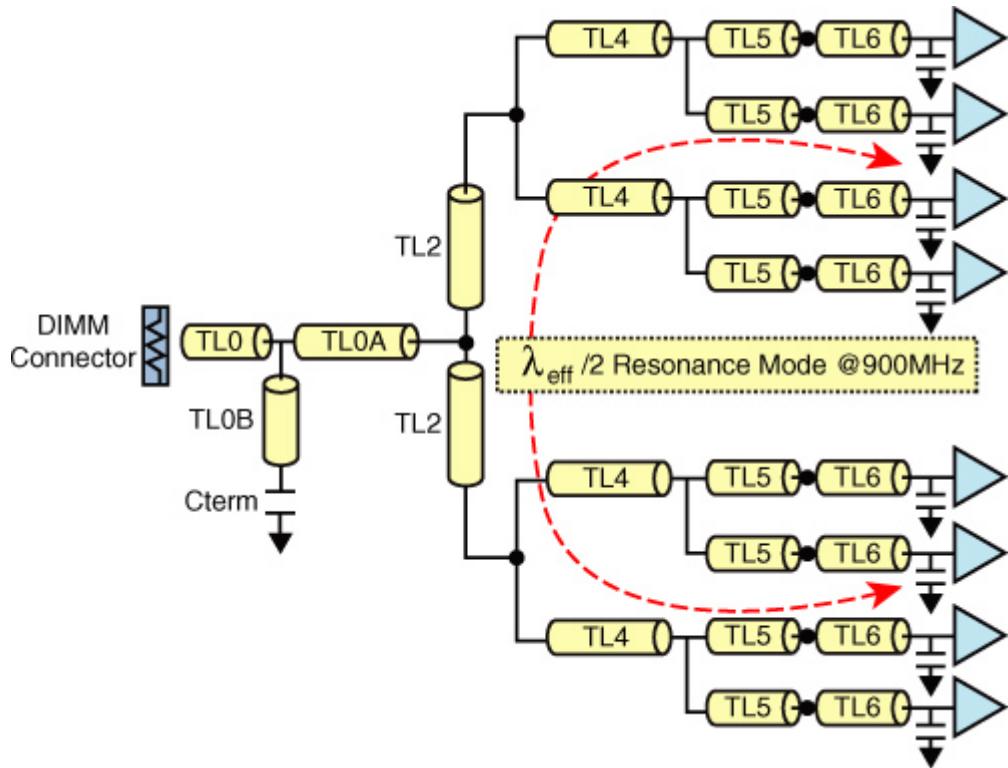


Figure 7.11. Resonant structure on control network

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” Design-Con 2006.



In summary, SSO noise between 800MHz and 900MHz, the second and the third harmonic components of DDR800 and DDR667, respectively, was coupled onto the signal trace by way of the through-hole via and imperfect referencing. Unfortunately, the signal trace has a resonant structure, which causes 800~900 MHz standing wave on the signal trace. Finally, this degrades the timing margin around 270ps for setup and hold time.

7.4.4. Proposed Solutions

To fix the noise amplification problem due to resonance, we recommend short-term solutions as follows. First, plane noise specification requires less than $\pm 3\%$ of the signal voltage swing at the transition layer. Adding an on-chip decoupling capacitor with more than 100pF per IO onto SDRAM device B is required to reduce high-frequency noise from the SDRAM devices. Second, to reduce plane-signal coupling, it is recommended that no reference layer change occurs, unless absolutely required. The stitching distance has to be much shorter than the wavelength of the third harmonic of the maximum digital frequency, and multiple vias help isolate signal trace from the plane noise, as shown in Figure 7.12. Third, the resonance needs to be alleviated by keeping out critical lengths such as half and quarter wavelengths at frequencies of interest. A series resistive terminator on the

resonance path can help alleviate resonance. Another sometimes helpful way to dampen the resonance effects is that you can use lossy transmission lines, that is, narrow traces, lossy dielectric, and so on. This dampens the reflections in the time domain or lowers the Q-factor of the resonances in the frequency domain. Fourth, extremely close spacing between the power and ground planes can mitigate cavity resonances. Plane capacitance goes up, plane inductance goes down, and plane resistance stays the same, so consequently Q-factor is greatly reduced. This effect becomes especially pronounced when dielectric thickness drops below 1mil. Radiation can also be reduced a lot.

Figure 7.12. Via shielding effect: electric field intensity at 1GHz

[View full size image]

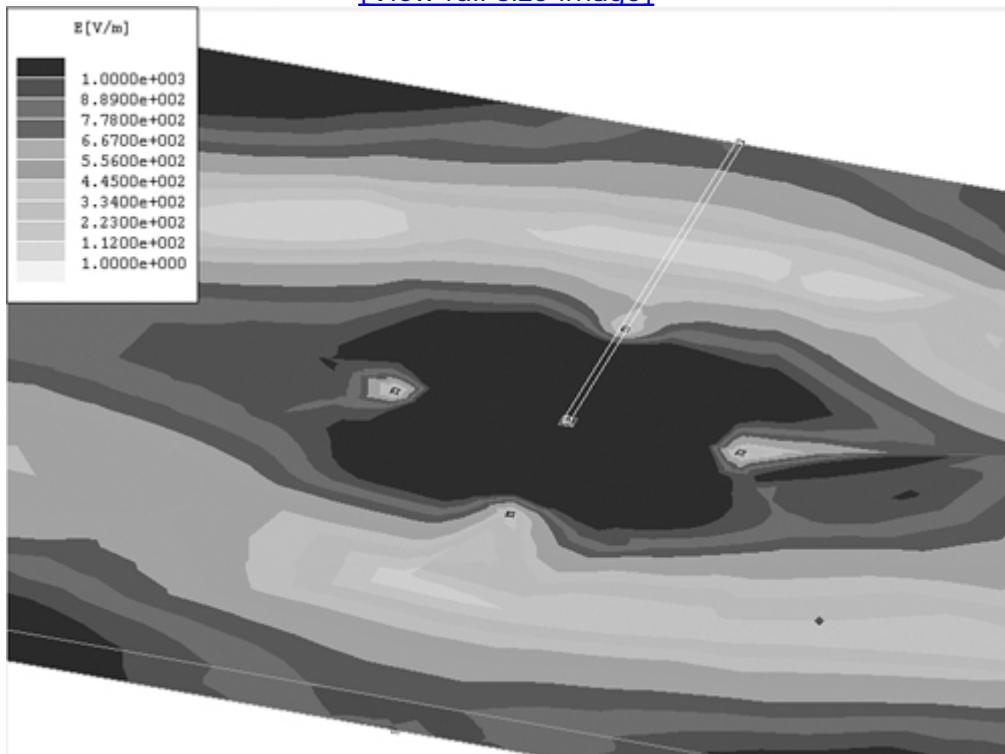


Figure 7.12 shows the via shielding effect at 1GHz frequency. More vias are added in two different ground planes. In comparison with single stitching, four ground via stitching improves planes-to-signal coupling by more than 30%. The insertion loss of the trace is also reduced by half. Although shortening the stitching via distance is more critical than its orientation, the via positioning that is parallel to the shorter plane edge is the preferred orientation for placement.

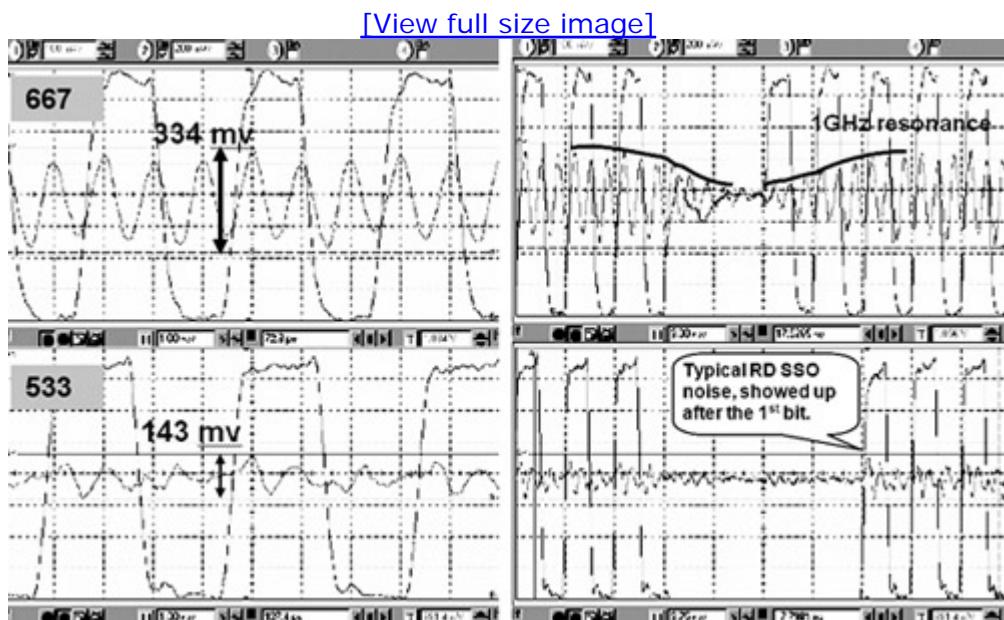
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7.5. Case Study II: DDR2 667 Vref Bus

A case study on the Vref resonance issue of DDR2 667 MT/s bus is described in this section. In the DDR2 platform under this case study, a significant amount of noise was captured on the Vref bus on the DIMM card, as shown in [Figure 7.13](#). On the DDR2 interface, Vref is a reference voltage level generated on the motherboard side and supplied to all SDRAM devices to maintain data signals near their switching level. As the data transfer rate of the DDR interface increases from one generation to another, available voltage margins for data signals decrease significantly. A clean Vref signal has become critical for normal operation of the DDR interface. Moreover, when defining the roadmap for next-generation memory technology, how well local Vref noise is controlled and minimized has become a significant factor.

Figure 7.13. Time domain measurement shows 1GHz resonance on Vref bus

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



When the DDR2 interface operated at a 533 MT/s data rate with the worst-case SSO pattern 1010, 143 mV peak-to-peak Vref noise was observed. However, when it operated at the 667 MT/s data rate, 334 mV peak-to-peak Vref noise was observed. In the 533 MT/s case, the noise has a typical SSO appearance, whereas in the 667 MHz case, the noise waveform is much smoother and shows a frequency around 1GHz. It was also observed that the noise level was the highest on device 0, the first device on the DIMM card, and reduced to a lower level on other devices (device 1 to device 8). Three factors have been investigated to identify the root cause: noise source, noise coupling mechanism, and resonance structure. A combination of planar 3D EM simulation and lab VNA measurement was used in this analysis.

7.5.1. Noise Source

Based on the time-domain waveform capture on [Figure 7.13](#), the noise magnitude is dependent on the data switching pattern. The noise has a frequency of 1GHz, the third harmonic of the fundamental data frequency. DDR2 667 MT/s has a fundamental data frequency of 333MHz. It is relatively easy to draw a conclusion that the root cause of the noise is the simultaneous switching output noise of SDRAM buffers in their write cycle on the DIMM card.

7.5.2. Coupling Mechanism

Extensive simulation and measurement data on this case study has shown the SSO noise was coupled from the power and ground planes to the Vref trace due to through-hole vias and reference plane change, as shown in [Figure 7.4](#). Previous work [3] has proved the coupling mechanism between switching noise on power and ground to signal trace analytically and experimentally. For this case study, there are two dominant coupling mechanisms: coupling induced at signal discontinuities due to layer transition and direct SSO coupling. Coupling can be increased due to cavity and signal resonances.

7.5.3. Resonance Structure

The next important consideration is to identify the resonance structure. The magnitude of SSO noise itself is much smaller than the noise observed on the Vref trace. The SSO noise shape is also not as smooth as the Vref noise. Noise magnitude becomes amplified with a certain resonance structure. As illustrated in [Figure 7.14](#), the distributed decoupling scheme was used on the Vref trace design to minimize the capacitor ESL and make the Vref track the midpoint of the signal voltage swing. The standing wave (also called stationary wave) phenomena occurs in all the Vref trace segments between two decoupling capacitors, which form electric walls on both sides, as shown in [Figure 7.15](#). Depending on the physical trace length between the

adjacent capacitors and other all inductance components contributing to the electrical length, the structure is subjected to resonance at certain frequencies.

Figure 7.14. Resonance structure of the Vref bus

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.

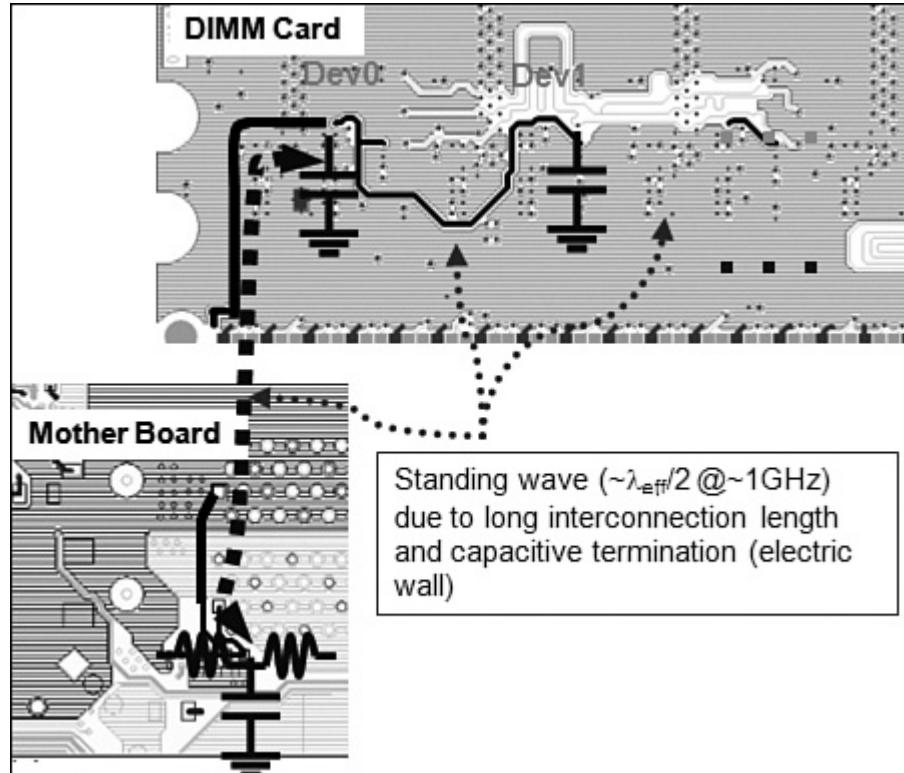
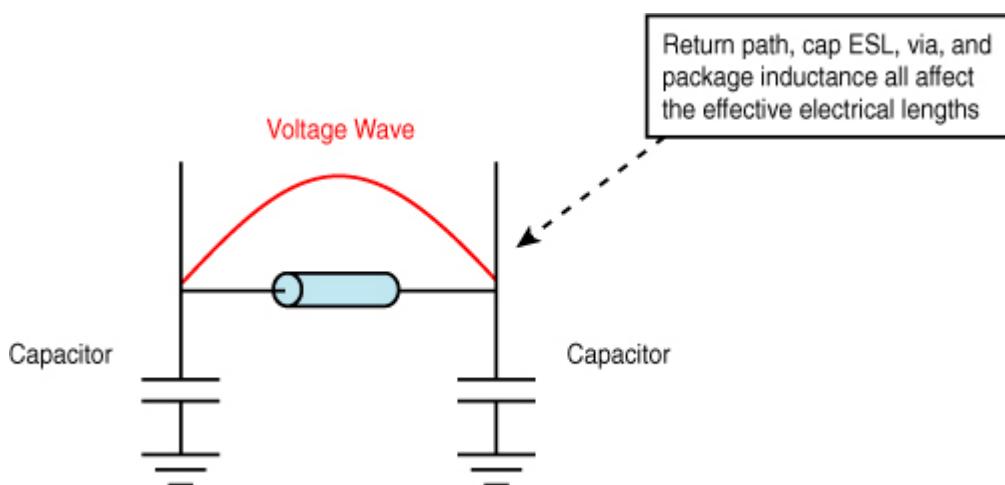


Figure 7.15. Resonance structure of the Vref bus

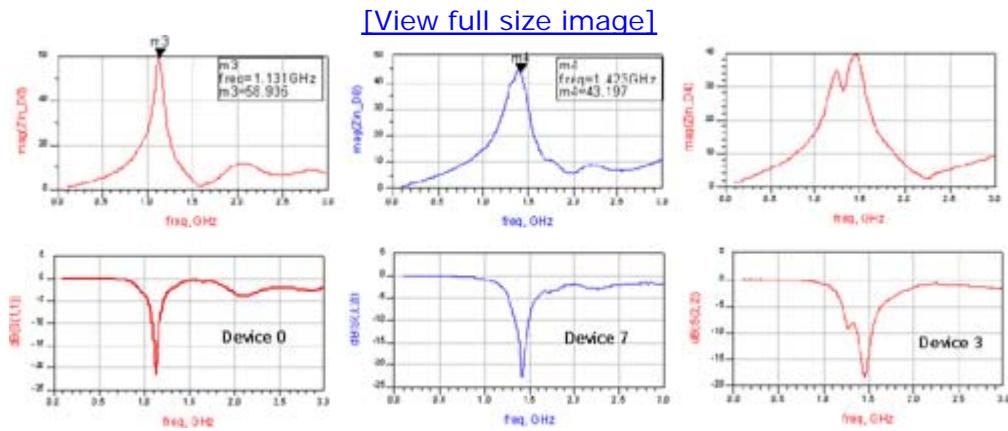


In this case, the first device (device 0) has the longest Vref trace routing between the motherboard bypass capacitor to the DIMM bypass capacitor, which should have a relatively low resonance frequency. The other eight

devices (devices 1 through 8) have shorter routing between the bypass capacitors, which should have relatively high resonance frequency. According to [Figure 7.16](#), VNA measurements of return loss S_{11} and input impedance Z_{11} at Vref pins show that the resonance frequency at device 0 is around 1.1GHz, and device 7 and device 3 around 1.4 to 1.5 GHz.

Figure 7.16. VNA measurements of S11 and Z11 indicate resonance frequencies at different device locations

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” Design-Con 2006.



This data explains the reason why the 667 MT/s data rate leads to a higher noise level and why the device 0 location has a much higher noise level. First, at the data rate of 667 MT/s, the base frequency is 333MHz and the third harmonics is 1GHz, extremely close to the resonance frequency of Vref trace, whereas at 533 MT/s, the third harmonics of the base frequency is only 800MHz. Second, the device 0 location has the lowest resonance frequency because it has the longest trace length between the bypass capacitors. In short, the analysis shows the root cause of this Vref noise issue as the third harmonic resonance of data signals when DRAM devices are in write mode.

7.5.4. Proposed Solutions

After identifying the root cause of the Vref noise issue, we propose a set of solutions. Three options exist for resolving the problem: eliminating the noise capturing path with SSO noise reduction (which is a separate topic), changing the resonance structure, and adding on-die or off-die filters.

The majority of the solutions have been verified with planar 3D EM time-domain and frequency-domain simulations, which share the same electrical models. Due to many unknown parameters, such as the actual capacitor ESL, DRAM on-die model, and so on, building an accurate baseline planar 3D EM model proved to be a challenging task. Lab VNA measurements were

used extensively to calibrate the simulation model at different device locations. Good correlations between simulation and lab measurements were established under two different conditions. This effort was later recognized as the key step for this case study. [Figure 7.16](#) and [Figure 7.17](#) show good correlations between the simulated and measured S_{11} parameter under a base condition. [Figure 7.18](#) and [Figure 7.19](#) show good correlations between simulation and measured S_{11} when an additional bypass capacitor was added at the edge finger location near the DIMM connector. Note that adding an additional bypass capacitor affects only the resonance frequency of device 0 and has virtually no impact on other devices (device 1 through 8). This confirms the analysis on the resonance structure in the previous section.

Figure 7.17. Simulated S_{11} parameters on Vref trace at devices 0, 3, and 7 under base conditions

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” Design-Con 2006.

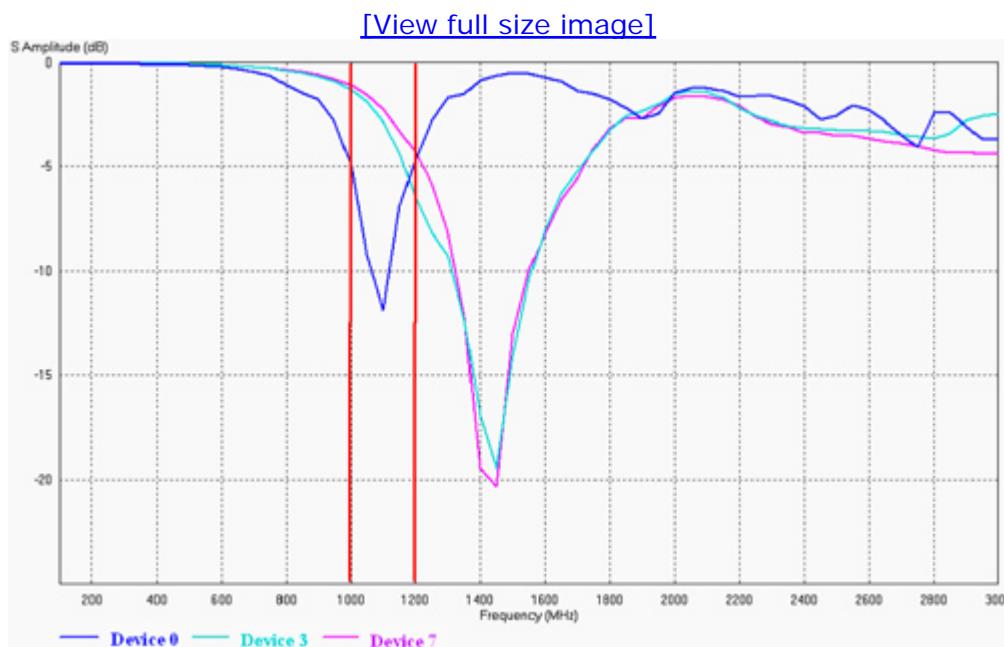


Figure 7.18. Simulated S_{11} parameters on Vref trace at devices 0, 3, and 7 after adding a bypass capacitor at edge finger location

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” Design-Con 2006.

[\[View full size image\]](#)

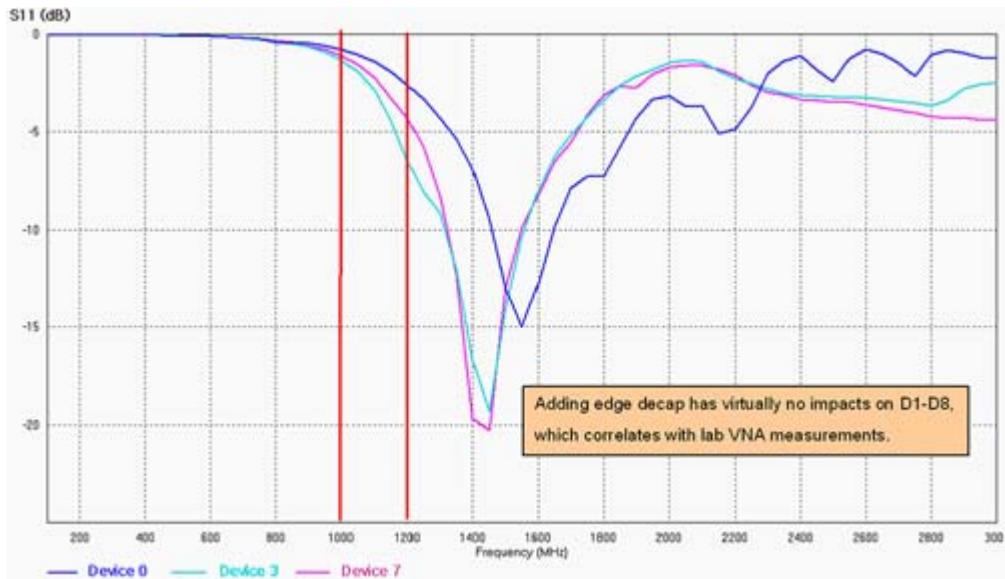
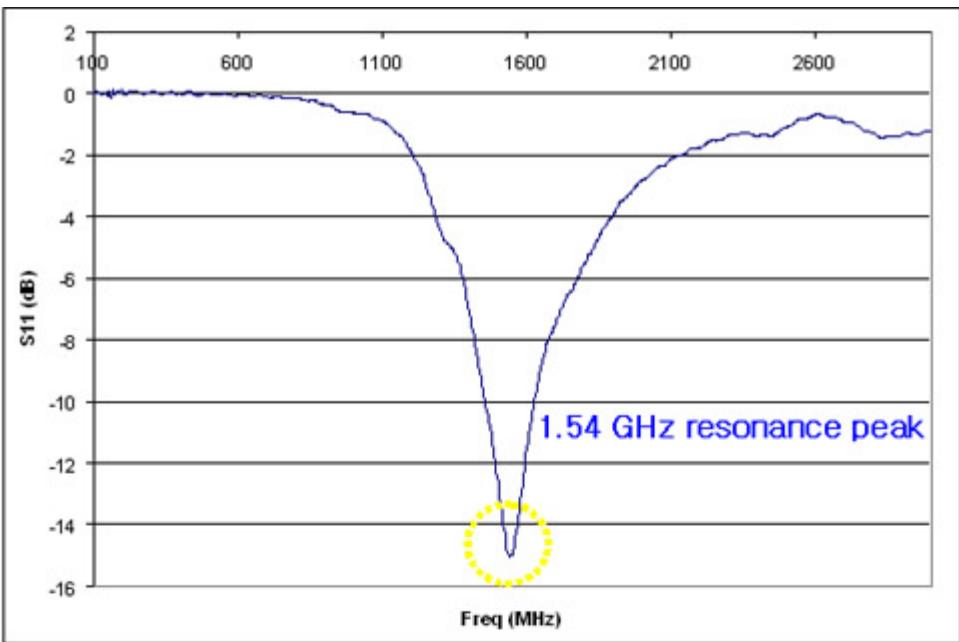


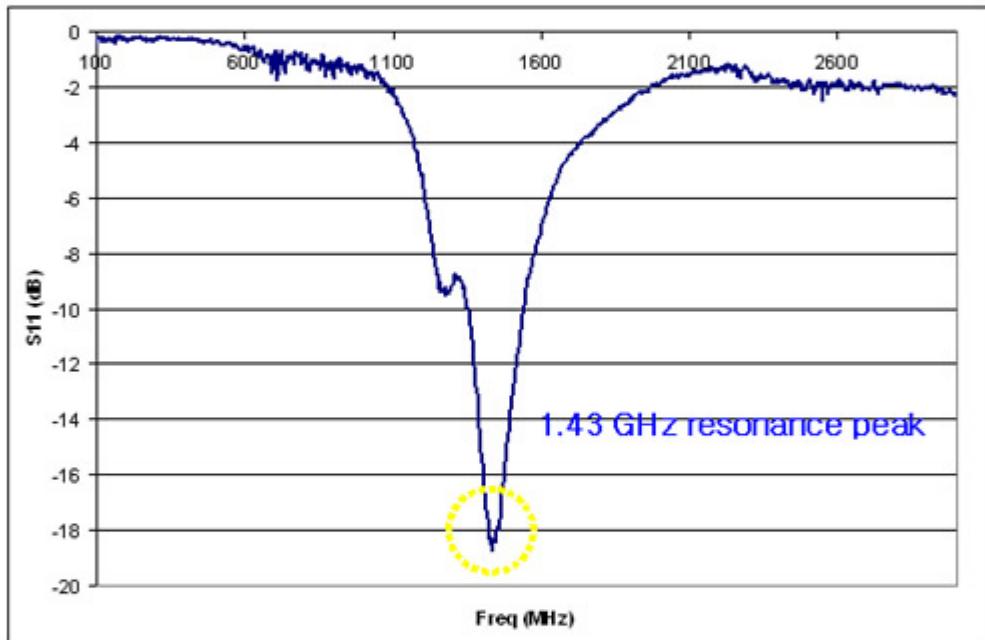
Figure 7.19. Measured S_{11} parameters on Vref trace at devices 0, 3, and 7 after adding a decoupling capacitor at edge finger location

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.

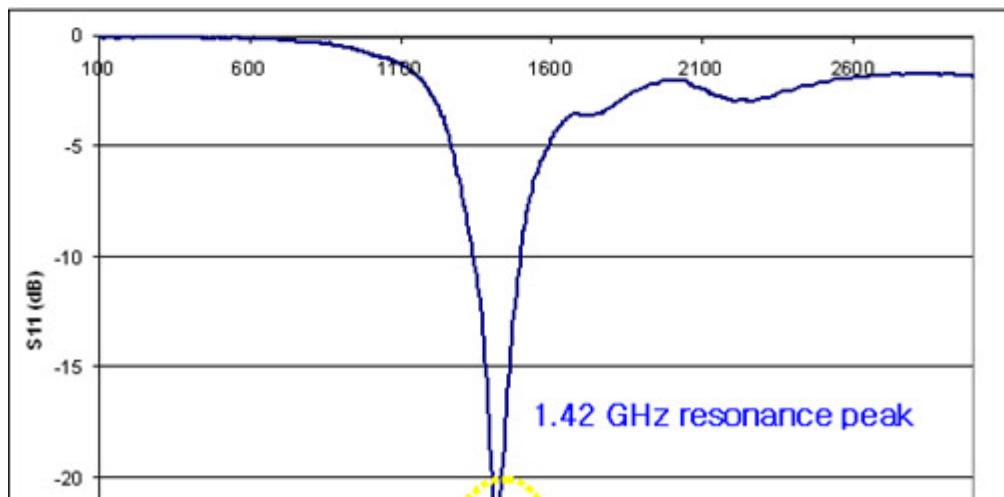
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(a) Device 0



(b) Device 3

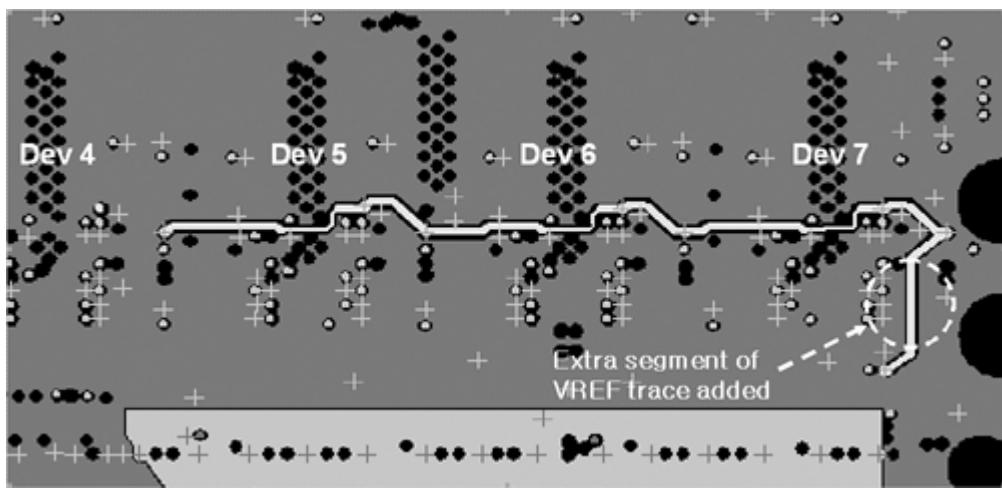


To minimize the noise coupling due to transition vias, the same reference plane (either power or ground plane) needs to be maintained along the Vref trace, including both motherboard and DIMM segments. In addition, the number of transition vias going through the power and ground planes should be reduced as much as possible.

To change the resonance structure, additional bypass capacitors need to be added to shift the resonance frequency higher, especially at the first device location where the Vref trace is longer. In general, the Vref trace needs to be routed as short as possible to shift the resonance frequency higher. The reduction of the return path will also help change the resonance frequency. More decoupling capacitors (power-to-ground) and stitching vias (power-to-power and ground-to-ground) are required to improve the return path and reduce the electrical length of the Vref trace. The effectiveness of the decoupling capacitor reduces as frequency goes higher, due to ESL and mounting inductance. At higher frequencies, stitching vias are preferred over decoupling capacitors. The simulation also shows that adding an additional Vref trace segment and a bypass capacitor after the end device can help alleviate the noise at the last device, as shown in [Figure 7.20](#). It adds a T-junction to the end device, which appears at all other device locations and reduces noise level due to energy splitting.

Figure 7.20. Additional Vref trace segment added at the end device location

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



With these changes, planar 3D EM simulations based on the models, which correlate to the lab VNA measurements, have demonstrated 62%~87% reduction of noise on the Vref trace, as shown in [Figure 7.21](#) and [Figure 7.22](#).

Figure 7.21. Time-domain simulation of Vref noise with original

board layout

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.

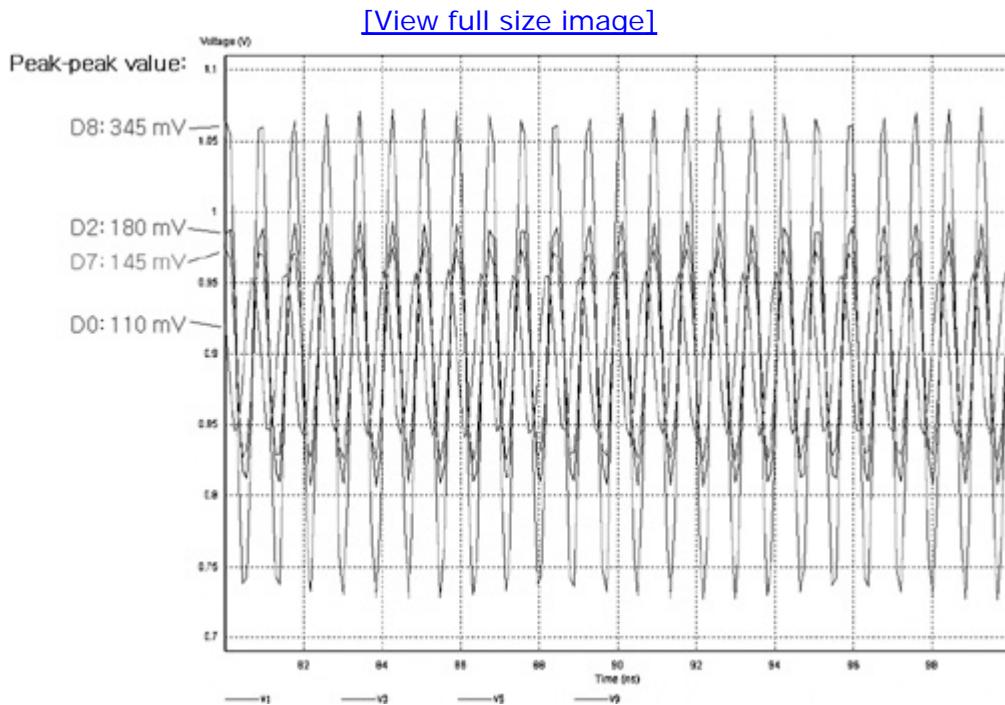
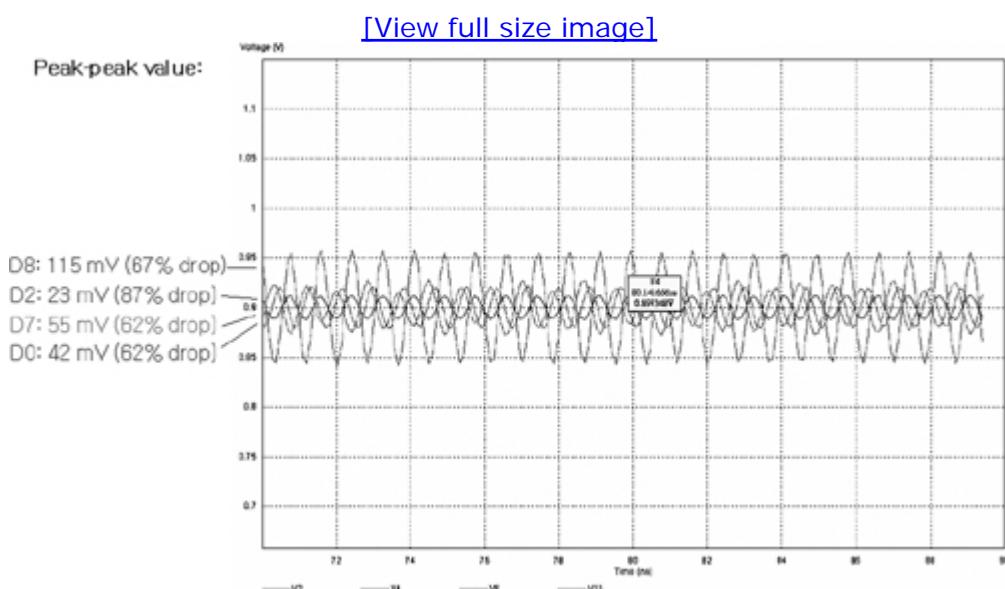


Figure 7.22. Time-domain simulation of Vref noise after eliminating reference plane change, adding an additional stub at end device, and adding a decoupling capacitor at connector pin location

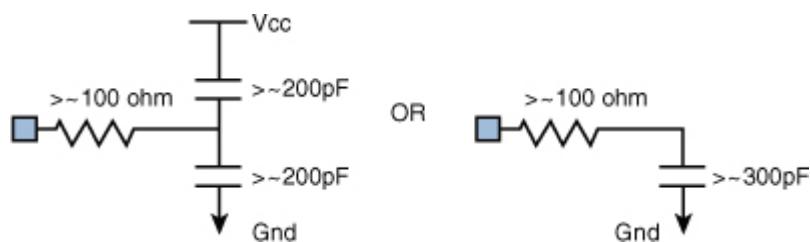
Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



Some additional solutions have also been proposed. An on-die RC low-pass filter can be used to minimize the local Vref noise at a pad location. A series resistor of around 100Ohms can be used. Either a couple hundred pF pull-up and pull-down capacitors or only one pull-down capacitor can be used, as shown in [Figure 7.23](#). The planar 3D frequency domain simulation shows that the pad location is isolated from the Vref noise on the board by adding an on-die filter. Specific R and C values should be determined, based on the value of the existing decoupling capacitor between the power and ground. If the power and ground noises are in phase, both pull-up and pull-down caps are required. If the power and ground noises are 180 degree out of phase, only a pull-down cap is required.

Figure 7.23. On-die filters for Vref signal

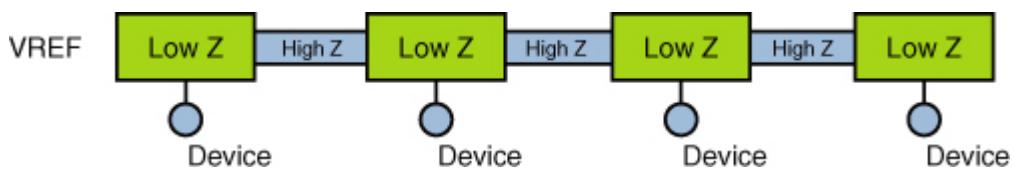
Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



If an on-die filter is not available, or a clean Vref signal is desired on board to reduce its impact on other signal traces, an off-die RC low-pass filter or stepped-impedance transmission line low-pass filter can be used. [Figure 7.24](#) shows the idea of using a stepped-impedance transmission line low-pass filter for Vref routing. The signal trace can be routed by connecting wide (low Z_0) and narrow (high Z_0) segments repetitively. Equivalent to a low-pass LC network, the stepped-impedance structure can help eliminate high-frequency noise and increase isolation between devices on Vref signal.

Figure 7.24. Off-die stepped impedance filters for Vref signal

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



Appropriately designed on-die and off-die RC or LC low-pass filters will remove high-frequency noise from a Vref signal. On-die filters remove high frequency noise at the pad location, whereas off-die filters remove noise on the trace.

We emphasize that as frequency increases, DIMM geometric dimensions and between-device distance become a significant fraction of a wavelength, which makes a Vref trace more vulnerable to the SSO noise resonance and Vref noise control more challenging. The use of distributed decoupling capacitors will not be sufficient for a higher data rate DDR interface.

Understanding combined signal-power integrity issues in the era of gigahertz data rates requires an advanced co-design methodology for signal integrity and power integrity analysis. This section has explored a robust co-design methodology with two case studies, namely DDR2-800 control bus and DDR2-667 Vref bus resonance. With the proposed co-design methodology, the complicated power induced resonance problems have been root-caused and consequently, cost-effective solutions, and design guidelines have been identified for the presilicon design stage. Similar principles of signal/power integrity co-analysis can be applied to higher data rate memory devices.

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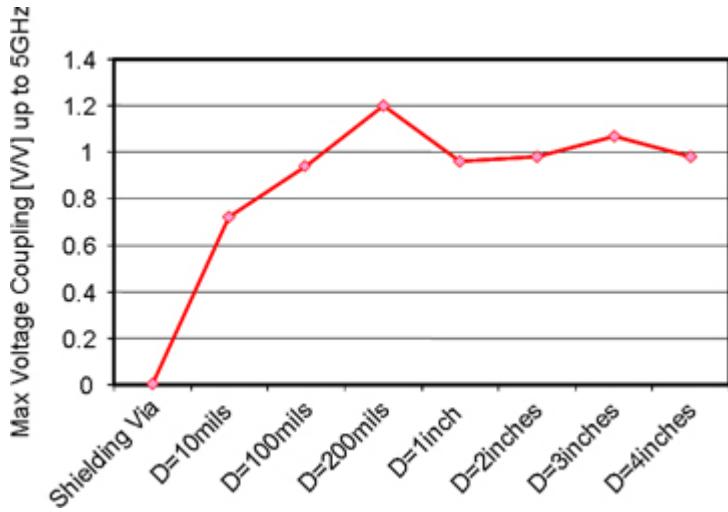
7.6. Referencing/Stitching/Decoupling Effects—Single-Ended Interface

Platform stitching vias and decoupling capacitors; also called stitching decoupling capacitors, are used when a critical signal transitions between reference planes. The stitching decoupling capacitors are then connected between the power and ground planes near the critical trace effectively tying the two planes together. The stitching decoupling capacitors have been proved to be critical design components for a single-ended interface to facilitate the return current path and minimize noise coupling from the power plane to signal trace. A simpler or better functionality can be obtained by ground-to-ground and power-to-power stitching via [6, 8].

Figure 7.25 shows the maximum voltage transfer ratios from the plane-to-signal trace with various stitching via distances. The maximum voltage transfer ratio has been extracted up to 5GHz based on full-wave 3D electromagnetic simulation. This demonstrates the significance of stitching vias for high-speed single-ended buses and that the tightened stitching distance rule is required for the multi-GHz interfaces. As high-speed interfaces are adopted more often, a link-level impact assessment and design guidelines for the plane stitching vias and decoupling capacitors are highly desirable for SI engineers and platform designers. Looser stitching/decoupling requirement means spacious board routing, lower cost, and reduced design effort, but its exact indication on platform signal integrity design is unclear. This section attempts to address this question.

Figure 7.25. Maximum voltage transfer ratio from plane-to-signal trace with various stitch distances

Source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.



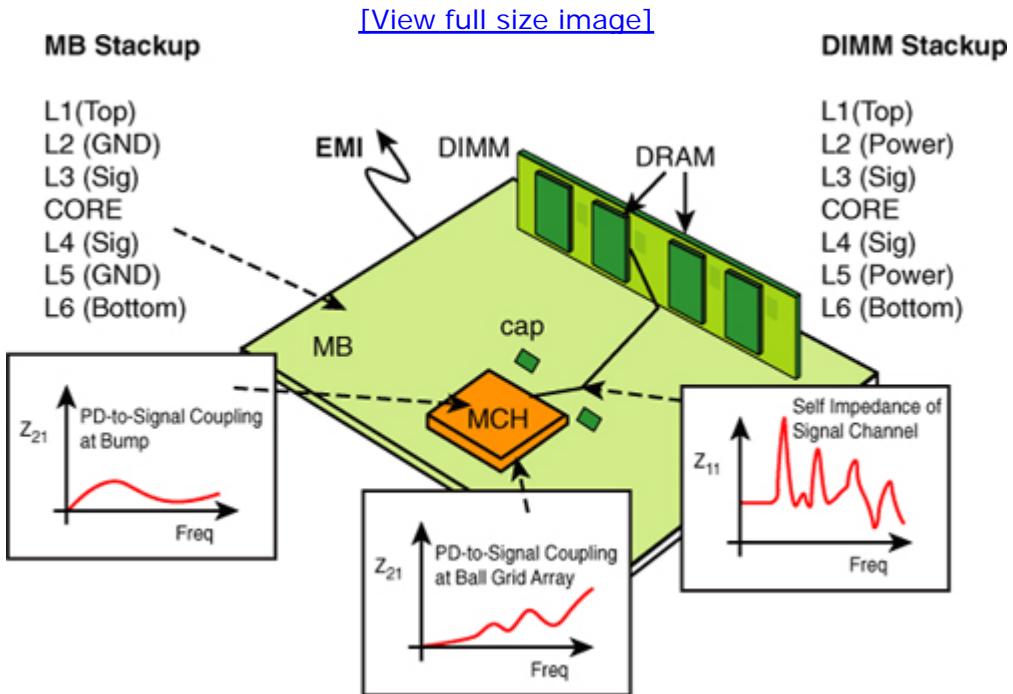
A typical DDR address, command, and control interface uses ground referencing on the controller package (MCH) and power referencing on the DIMM for the signal traces. The motherboard (MB) may use either ground or power referencing, or even both power and ground referencing. A key concern is the power noise induced on the signal trace due to the reference transition: either from the ground reference on the package to power reference on the MB, or from the ground reference on the MB to the power reference on the DIMM.

Simultaneous switching noise output (SSO) is the degradation of the voltage supply due to several I/O buffers switching simultaneously. Many papers have been written about this topic, including reference [10], which identifies and differentiates the different current loops present in a signaling system. The focus of the SSO work is typically in the hundreds of MHz range where the peak impedance of the power delivery network occurs due to the resonant interaction between the on-silicon decoupling capacitance and the package inductance. Extending the SSO analysis to explicitly consider the noise that propagates to the power and ground planes of the package and motherboard reveal additional coupling to signals that must be considered [11]. This is distinguished from adjacent signal crosstalk because this can be a long range effect where the coupling is through the proximity of the power/ground structures instead of through overlapping electromagnetic fields between adjacent signal lines. At resonant frequencies of the power/ground structures, noise on those structures couple strongly into the signal lines.

Plane-to-signal coupling increases as the data rate goes higher, especially in the multi-GHz regime. An accurate prediction of the coupling between power/ground SSO and interconnect lines in multilayer boards is required to achieve optimum power and signal distribution. Several papers have described the SSO coupling mechanism through the signal vias changing reference planes in a multilayer board [3, 8]. Figure 7.26 shows an example of a signal and power distribution scheme in DDR address/control signal networks. Typically power noise comes from the MCH chip and propagates

through the power-ground planes, and the noise is coupled onto the signal trace through the vias at a reference transition, located at the DIMM connector in this configuration. Minimizing reference discontinuities, by adding stitching decoupling capacitors, mitigate the effect of power network-to-signal coupling and radiated emission.

Figure 7.26. A signal-power distribution scheme; this depicts power network-to-signal coupling and EMI issues on DDR address/control signal networks



To investigate power noise-induced signal trace resonance on the multi-GHz bandwidth channels, three parameters need to be considered: plane self-impedance (Z_{11}) between power and ground reference planes, noise coupling coefficient (Z_{21}) from the reference planes to the signal trace at the reference transition region, and channel impedance profile (resonance behavior) of the channel [3].

Figure 7.27 shows some examples of vector network analyzer measurement data of power-ground self-impedance (Z_{11}) and coupling transfer impedance (Z_{21}). According to the Z-parameter data in Figure 7.27 (a) and (b), power-ground plane impedance correlates with power-to-signal coupling. The higher the power/ground impedance, the higher the noise coupled to the signal. However, there is strong noise coupling into the signals in the range of 2GHz, due to a potential resonance on the signal lines despite relatively low power/ground self-impedance.

Figure 7.27. Ground referenced (Case A) versus power

referenced (Case B) MB (a) Magnitude of power-ground self-impedance (Z_{11}) (b) Magnitude of coupling impedance (Z_{21})

Edward K. Chan, Mauro Lai, Myoung Joon Choi, and Woong Hwan Ryu, “Concurrent Analysis of Signal-Power Integrity and EMC for High-Speed Signaling Systems,” IEEE EMC © [2007] IEEE.

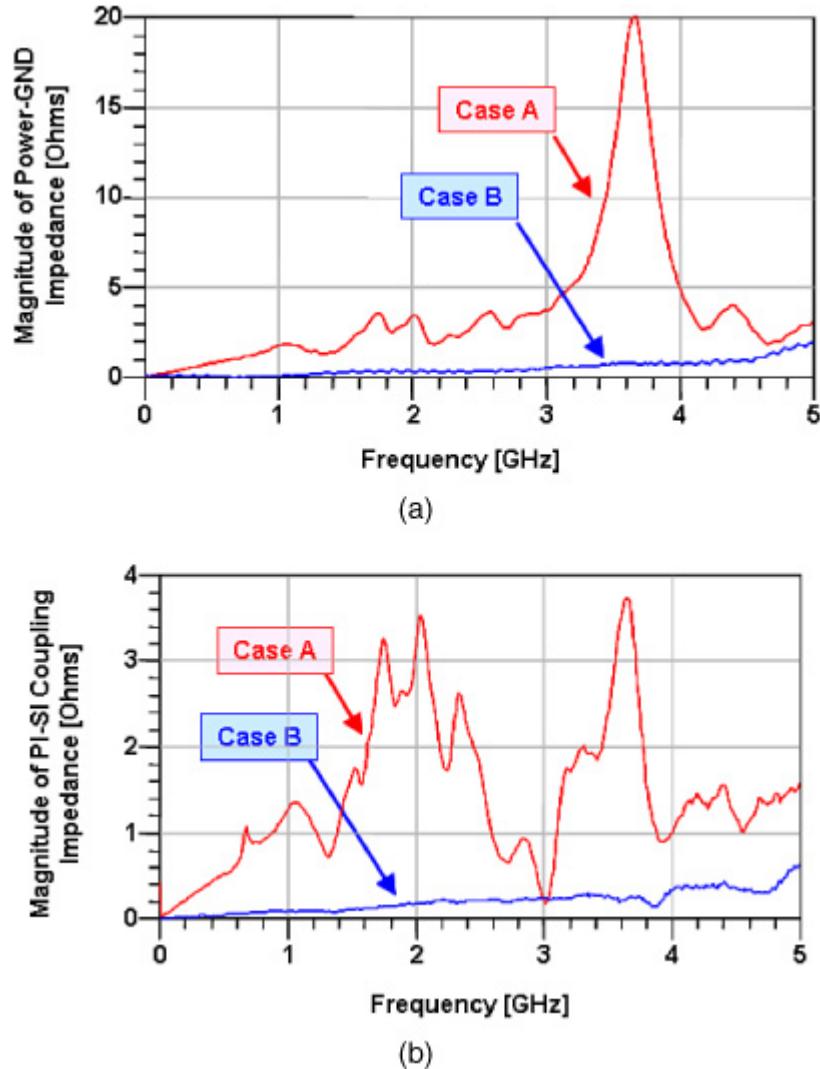


Figure 7.27 also compares ground referencing (Case A) against power referencing (Case B) on the MB. In Case A, the power/ground ports where the measurement is made are at the DIMM connector. At this point, the reference transition from ground on the MB to power on the DIMM occurs. In Case B, the power/ground port is at the MCH side, where there is a transition from ground reference on the MCH to power reference on the MB. The signal port is always at the SDRAM on the DIMM.

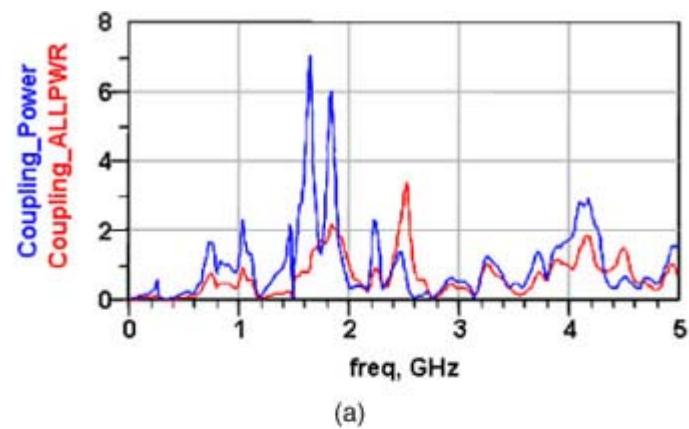
The larger power/ground impedance in Case A results in higher power noise coupling onto the signal trace. Power referencing on the MB (Case B) helps alleviate risk because, in a typical system, more stitching decoupling capacitors are at the MCH side, compared to the DIMM side. Having the entire channel from the MCH to the MB to the DIMM power referenced

would be the best solution for the long term, but it does run into stringent practical limitations in a low-cost MCH package and MB stackups. In addition, radiated emission from the power planes carved into the MB needs to be resolved.

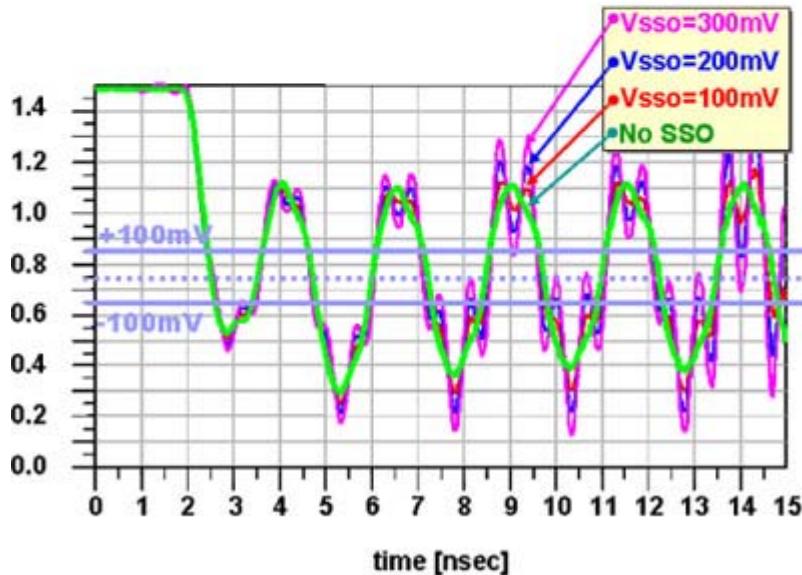
Figure 7.28 shows the simulated system-level Z-parameter results of a DDR address/control network based on full-wave EM modeling, including MCH, MB, and DIMM. It depicts power noise induced trace resonance at 1.6GHz frequency. Frequency domain coupling coefficient (Z_{21}) and time domain waveform with sinusoidal power noise injected at 1.6GHz are shown in Figure 7.28 (a) and (b), respectively. The time domain waveform exhibits ringback violation if the coupled noise is large enough.

Figure 7.28. Power noise induced trace resonance at 1.6GHz (a) FD response—coupling between PD noise and signal trace (b) TD response

Edward K. Chan, Mauro Lai, Myoung Joon Choi, and Woong Hwan Ryu, “Concurrent Analysis of Signal-Power Integrity and EMC for High-Speed Signaling Systems,” IEEE EMC © [2007] IEEE.



(a)



(b)

Through the concurrent signal/power integrity analysis, long-term and short-term solutions can be identified to mitigate any potential signal resonance effect due to power noise coupling, resulting in achieving the best platform referencing strategy. The proposed methodology covered several issues: first, identification of the noise source, for example crosstalk, SSO, and signal reflections, through extensive experiments in the time domain and frequency domains. The second issue involved identification of the coupling mechanisms including MB, package, DIMM, and chip-level power-signal interactions. The third issue included the analysis of power/ground structures, using full-wave EM field solvers. The final issue covered was the determination of a system impact based on system-level SI analysis with stimuli at the frequencies of resonance.

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7.7. Stitching Effects—Differential Interface [9]

Platform stitching vias and stitching capacitors have been proved to be critical design components for single-ended interfaces to facilitate the return current path and minimize noise coupling from the power plane to signal trace. The previous two case studies demonstrated the significant importance of stitching via for high speed single-ended buses, and tightened stitching distance rule is required for the multi-GHz interfaces. As high-speed differential interfaces are adopted more often, a link-level impact assessment and design guidelines for plane stitching vias and decaps are highly desirable for SI engineers and platform designers. A looser stitching/decoupling requirement means spacious board routing, lower cost, and reduced design effort, but its exact indication on platform signal integrity design is unclear.

In this section, differential eye diagram margins are compared for channels with different stitching/decoupling strategies on 5 to 6.4Gbps high-speed links. Mode conversion from common-mode to differential-mode was also analyzed with system-level simulations by injecting common-mode noise at the driver circuit side. Link-level time domain analysis well correlates the frequency domain measurement and simulation results. The following list depicts different purposes of each test structures as illustrated in [Figure 7.29](#):

- Case 1: Microstrip, 2 stitching vias at a distance of 200mils
- Case 2: Microstrip, 1 stitching vias at a distance of 200mils
- Case 3: Microstrip, 2 stitching vias at a distance of 100mils
- Case 4: Microstrip, 1 stitching vias at a distance of 100mils
- Case 5: Microstrip, no stitching vias. (Practically, there is one at a distance of 500mil.)
- Case 6: Stripline, 2 stitching vias at a distance of 200mils
- Case 7: Stripline, 1 stitching vias at a distance of 200mils

Case 8: Stripline, 2 stitching vias at a distance of 100mils

Case 9: Stripline, 1 stitching via at a distance of 100mils

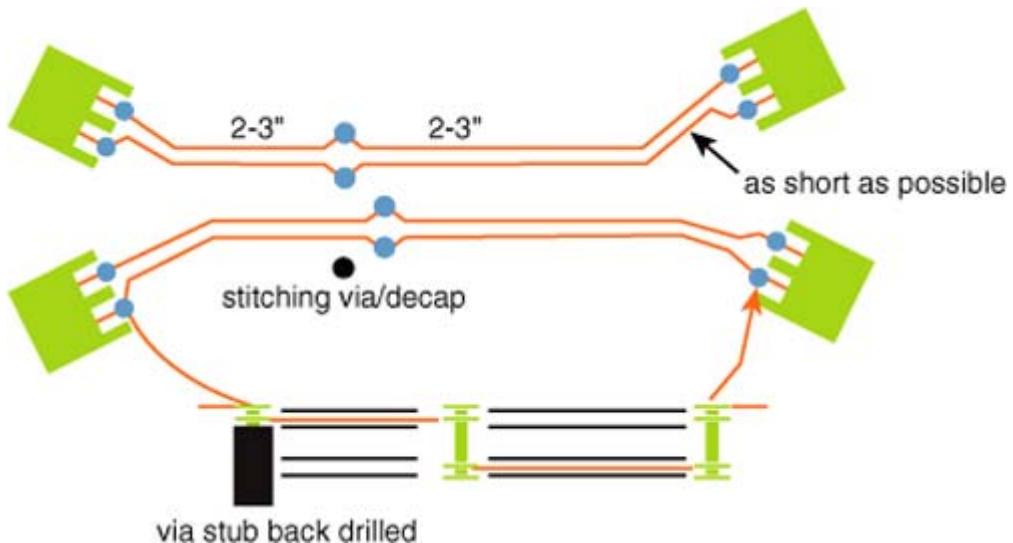
Case 10: Stripline, no stitching vias. (Practically, there is one at a distance of 500mils.)

Case 11: Microstrip, 2 stitching or decoupling capacitors at a distance of 200mils

Case 12: Microstrip, 2 stitching or decoupling capacitors at a distance of 100mils

Figure 7.29. Stitching via/cap test board setup

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.



For case 11 and 12, the characteristics with no stitching caps are taken before the capacitors are installed. Both TDR/TDT and VNA measurements are performed on these test structures to measure transmission, reflection, and far-end crosstalk. Having both microstrip and stripline structures covered different platform flavors.

Four differential pico-probes were placed at the launching structures to take the TDR and TDT measurement. During the TDR measurement, one of the four probes was connected to the TDR source, and the other three were terminated with the SMA 50-ohm loads. During the TDT measurement, the through port was connected to the TDT. Therefore, only two probes were connected to the SMA 50-ohm load.

Figure 7.30 through Figure 7.33 show the responses of the stripline (with stitching vias) TDR/TDT measurements. Figure 7.30 and Figure 7.32 show that stitching vias and their distance to transition location play an important

role on signaling characteristics. As expected, no stitching via case has the highest common mode FEXT and common mode ISI. The second highest is the 1 via at a distance of 200mils, which has a loose stitching design. The third highest is between two stitching vias 200mils away and one stitching via 100mils away. Finally, the lowest common mode FEXT and ISI corresponds to the case with tightest stitching design, 2 stitching vias at a distance of 100 mils. Based on the covered area of the crosstalk curve (that is, coupled energy from one trace to another), an approximate increase factor of 1.5 to 2 on common-mode FEXT was observed between 2 stitching via within 100 mil distance versus 500 mil distance from the signal transition location. Furthermore, two vias 200 mils away show comparable performance as one via 100 mils away.

Figure 7.30. TDR (ISI) common mode measurement for stripline with stitching via.

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

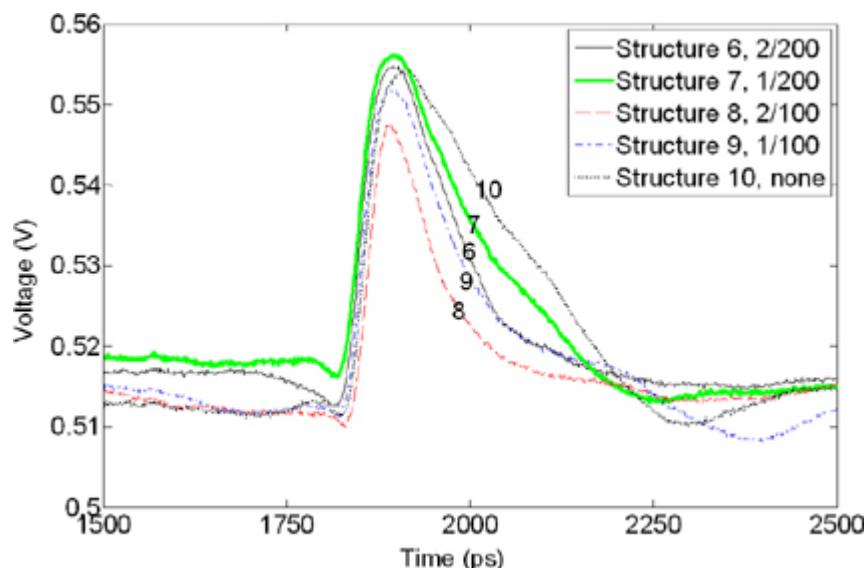


Figure 7.31. TDR (ISI) differential mode measurement for stripline with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

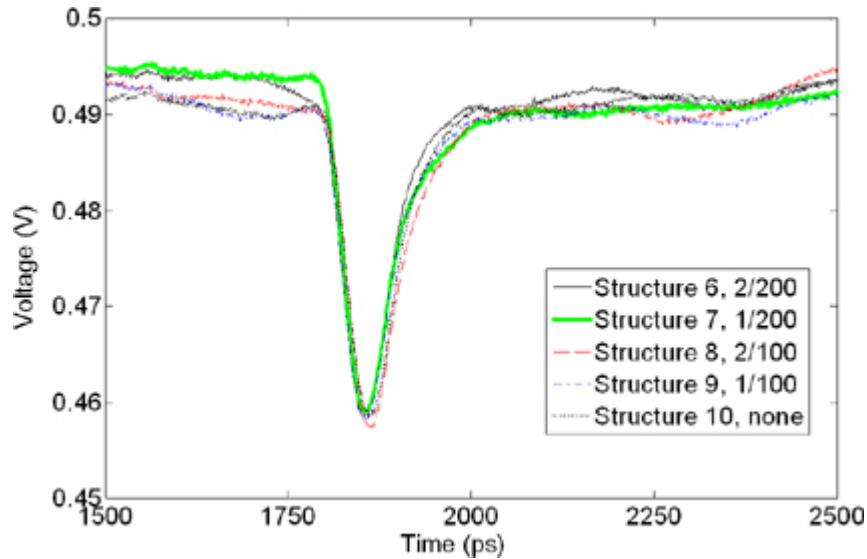


Figure 7.32. FEXT common mode measurement for stripline with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

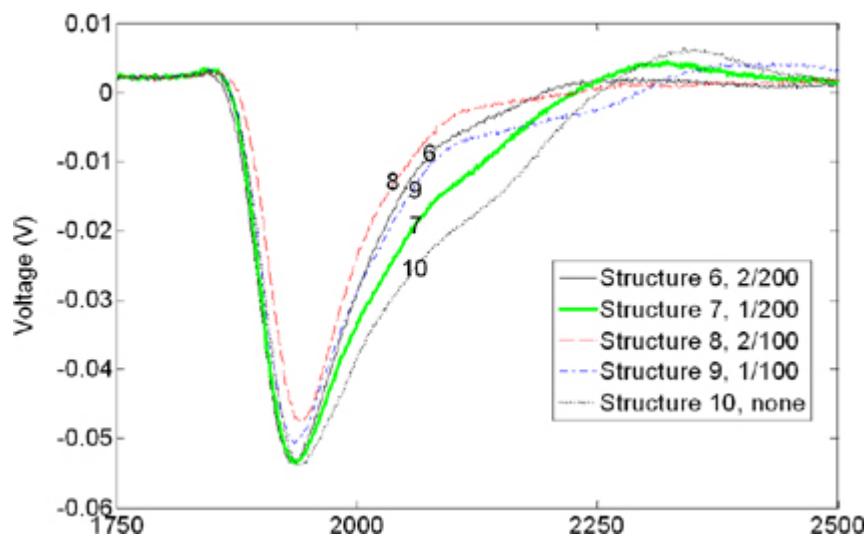
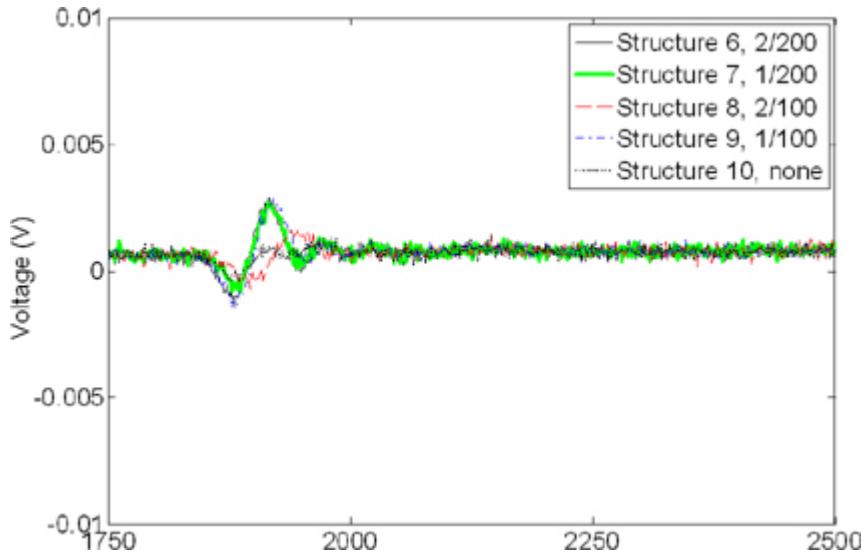


Figure 7.33. FEXT differential mode measurement for stripline with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.



On the contrary, [Figure 7.31](#) and [Figure 7.33](#) show that stitching vias and their distance to transition location have little or no impact on differential mode FEXT and ISI. Correlation between the FEXT/ISI levels and stitching condition cannot be readily found.

[Figure 7.34](#) through [Figure 7.37](#) show the responses of the microstrip (with stitching vias) TDR/TDT measurements, which has the same trend of stripline data, except the microstrip line has the higher FEXT overall due to nonhomogenous media. [Figure 7.34](#) and [Figure 7.36](#) show that stitching vias and their distance to transition location play an important role on signaling characteristics. As expected, no stitching via case has the highest common mode FEXT and common mode ISI; the second highest is the 1 via at a distance of 200 mils, which has a loose stitching design. The third highest is between two stitching vias 200mils away and one stitching via 100mils away. Finally, the lowest common mode FEXT and ISI corresponds to the case with the tightest stitching design, 2 stitching vias at a distance of 100 mils.

Figure 7.34. TDR common mode measurement for microstrip with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

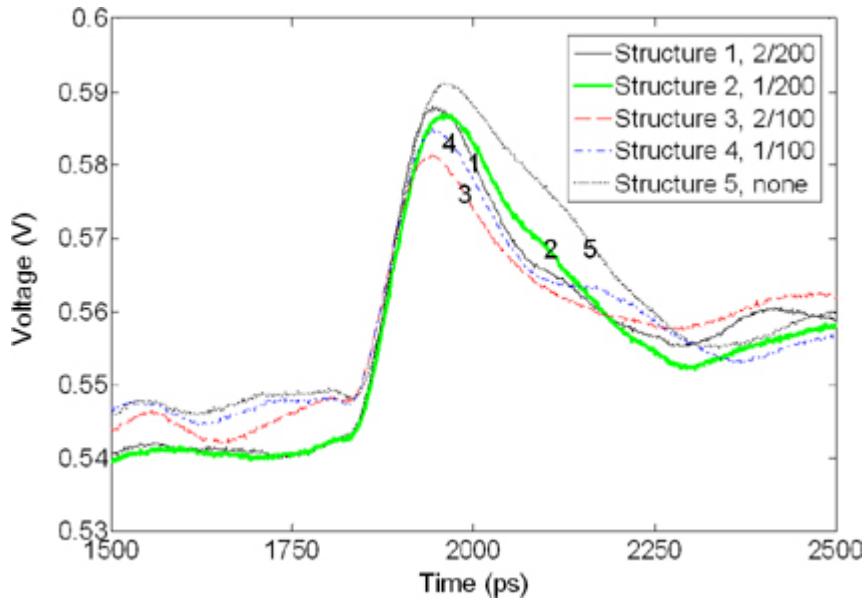


Figure 7.35. TDR differential mode measurement for microstrip with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

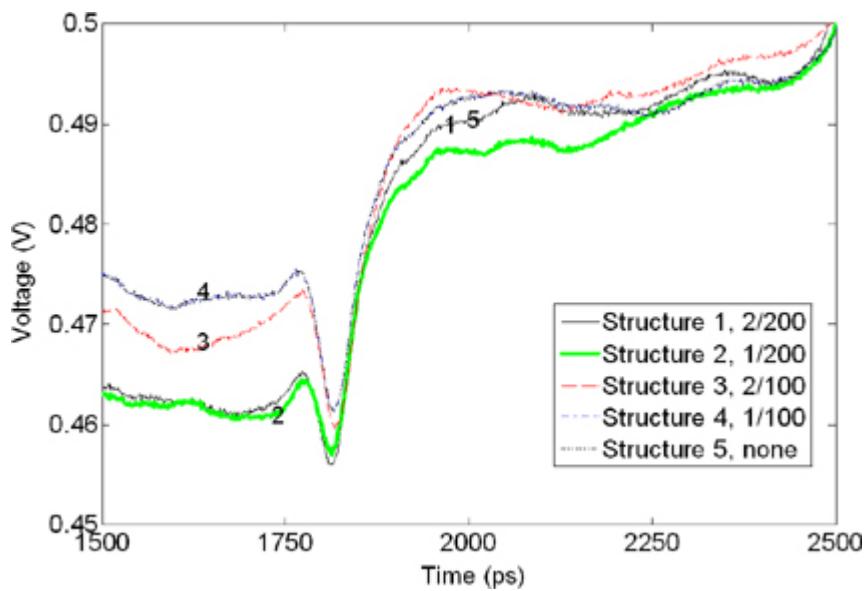


Figure 7.36. TDT common mode measurement for microstrip with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

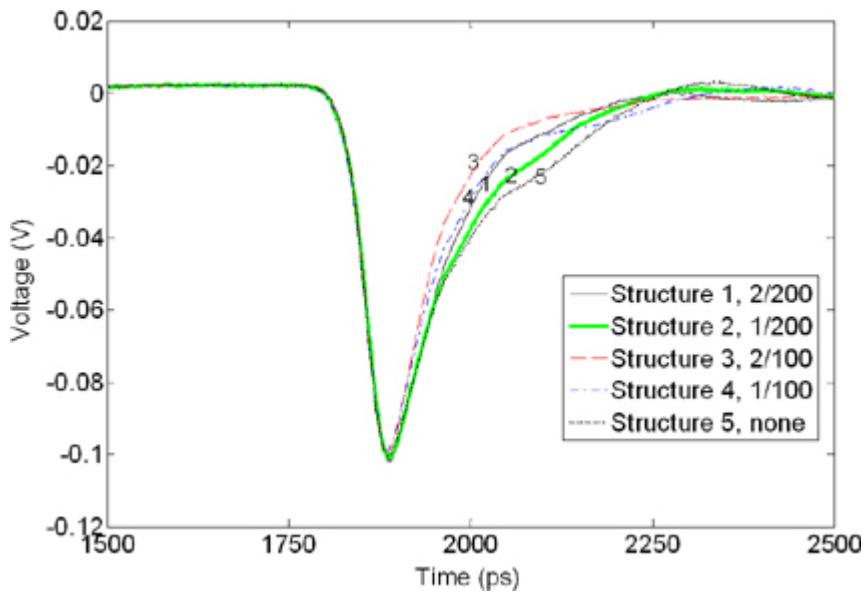


Figure 7.37. TDT differential mode measurement for microstrip with stitching vias

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

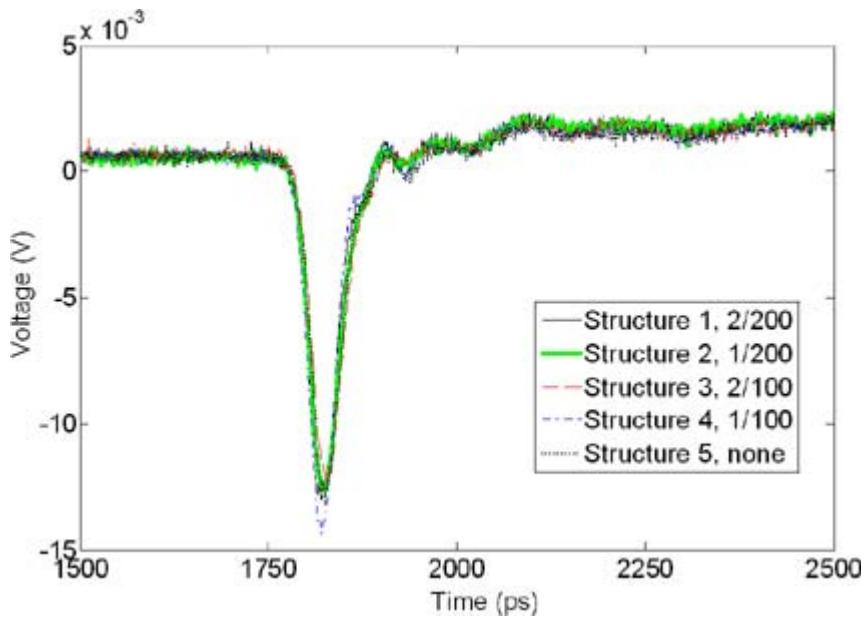


Figure 7.35 and Figure 7.37, on the contrary, show that stitching vias and their distance to transition location have little or no impact on differential mode FEXT and ISI. Correlation between the FEXT/ISI levels and stitching condition can hardly be found.

Figure 7.38 through Figure 7.41 show the responses of the microstrip (with stitching caps) TDR/T measurements. Neither common mode nor differential mode response correlates with stitching conditions of the decoupling capacitors. As frequency increases, the effectiveness of stitching caps is

significantly reduced due to equivalent serial inductance of the capacitors.

Figure 7.38. TDR common mode measurement for microstrip with stitching caps

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

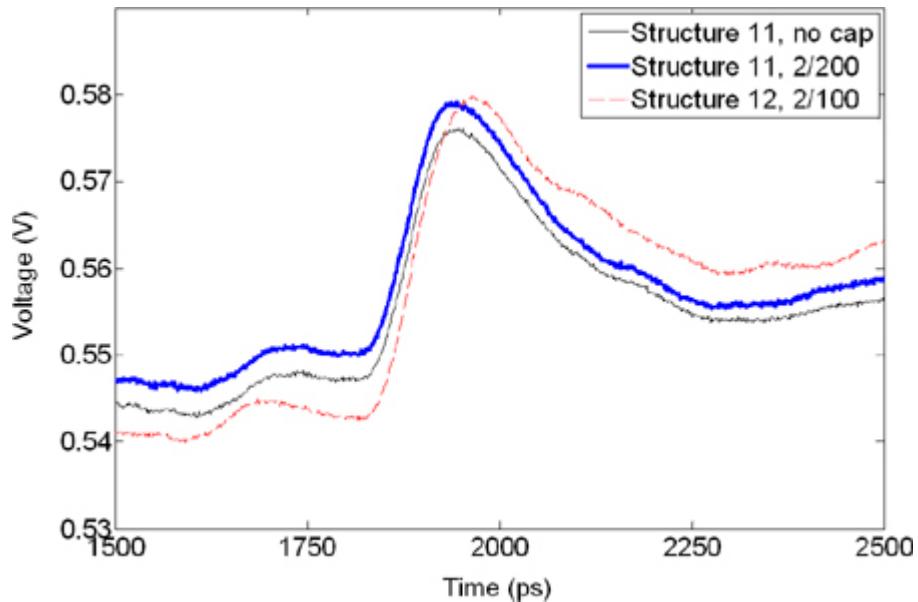


Figure 7.39. TDR differential mode measurement for microstrip with stitching caps

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

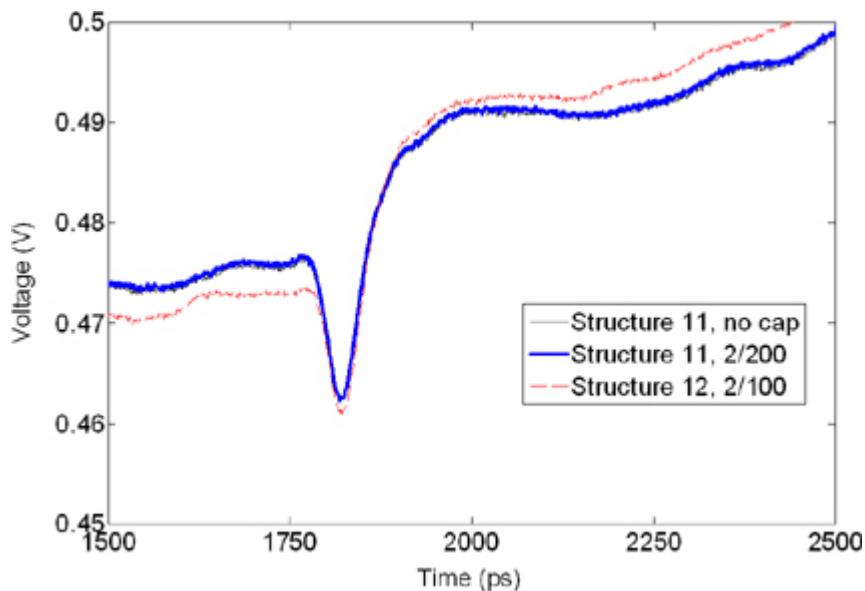


Figure 7.40. TDT differential mode measurement for microstrip with stitching caps

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

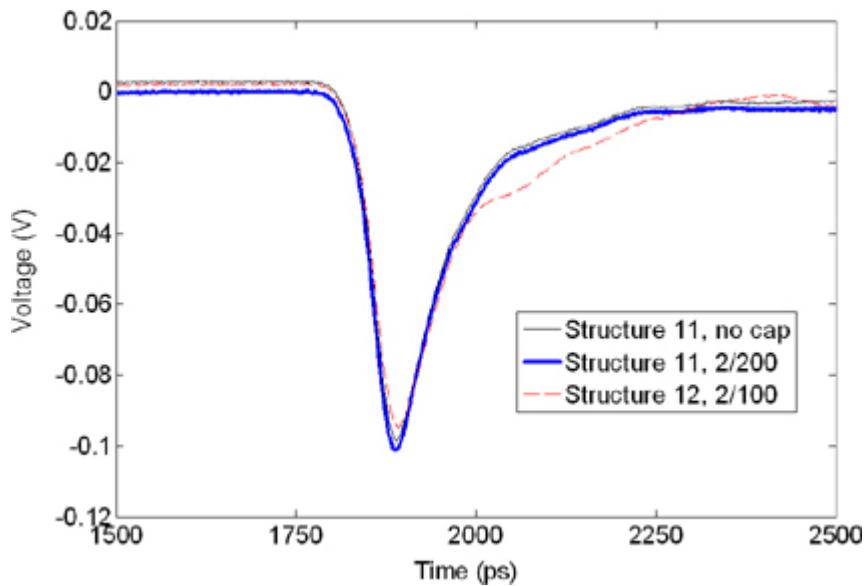
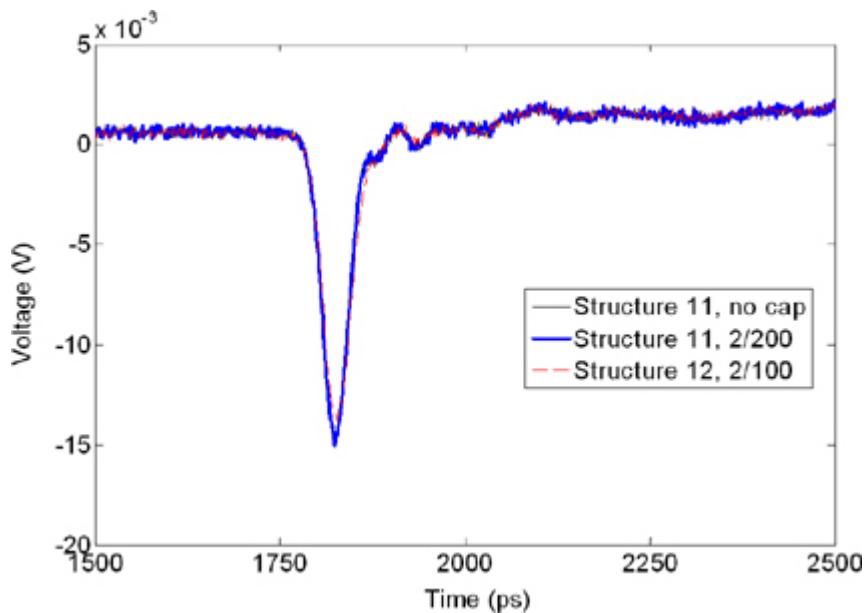


Figure 7.41. TDT differential mode measurement for microstrip with stitching caps

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.



7.7.1. VNA Measurement Results

To fully capture the frequency-dependent characteristics, VNA measurements were also performed. Due to equipment limitation, 4-port measurements were conducted and the other 4 ports for each structure were terminated with 500Ω SMA resistors.

[Figure 7.42](#) through [Figure 7.44](#) show the VNA data on FEXT. [Figure 7.42](#) shows that for the microstrip with the stitching via case, common-to-common mode FEXT level will follow the ranking of stitching condition, especially at the frequency of interest (below 5GHz), whereas differential-to-differential mode FEXT level is insensitive to the stitching condition. Similarly, [Figure 7.43](#) shows that for stripline with stitching via case, the common-to-common mode FEXT level will follow the ranking of the stitching condition whereas the differential-to-differential mode does not. The only difference here is that the stripline interconnect shows a much lower FEXT level. [Figure 7.44](#) shows that the stitching caps do not help the microstrip common mode or differential mode FEXT, correlating to the TDT data in last section. Overall, the VNA data matches TDR/TDT data very well.

Figure 7.42. VNA measurement for microstrip with stitching vias

Source: M. Wang and W. H. Ryu, “System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links,” 57th ECTC © [2007] IEEE.

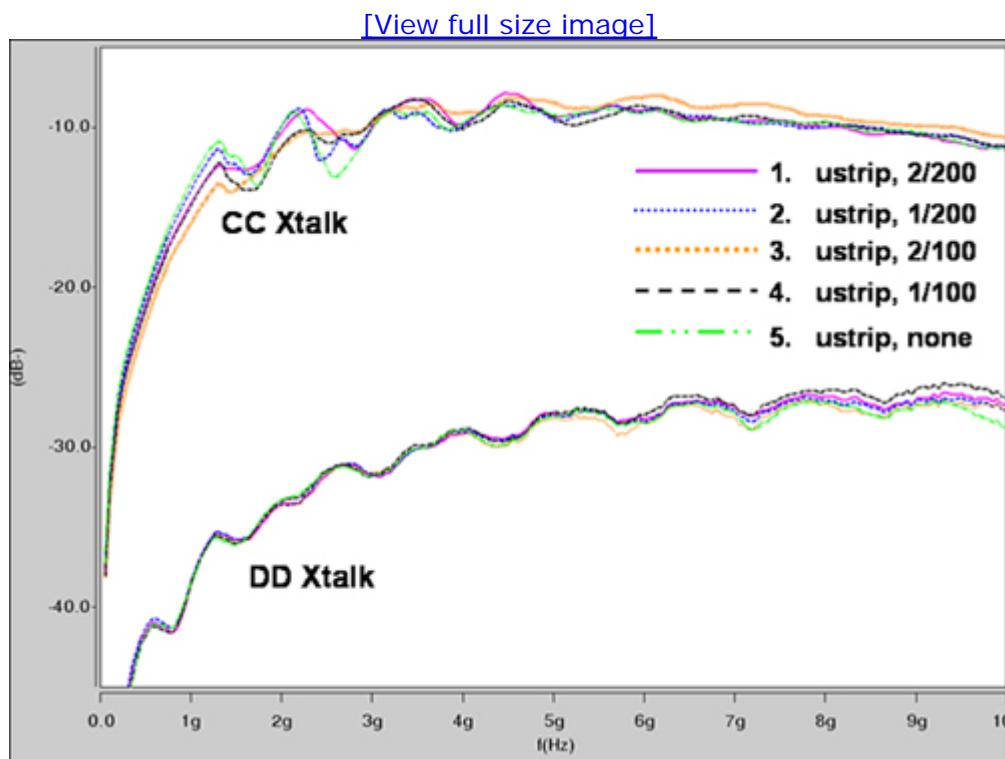


Figure 7.43. VNA measurement for stripline with stitching vias

Source: M. Wang and W. H. Ryu, “System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links,” 57th ECTC © [2007] IEEE.

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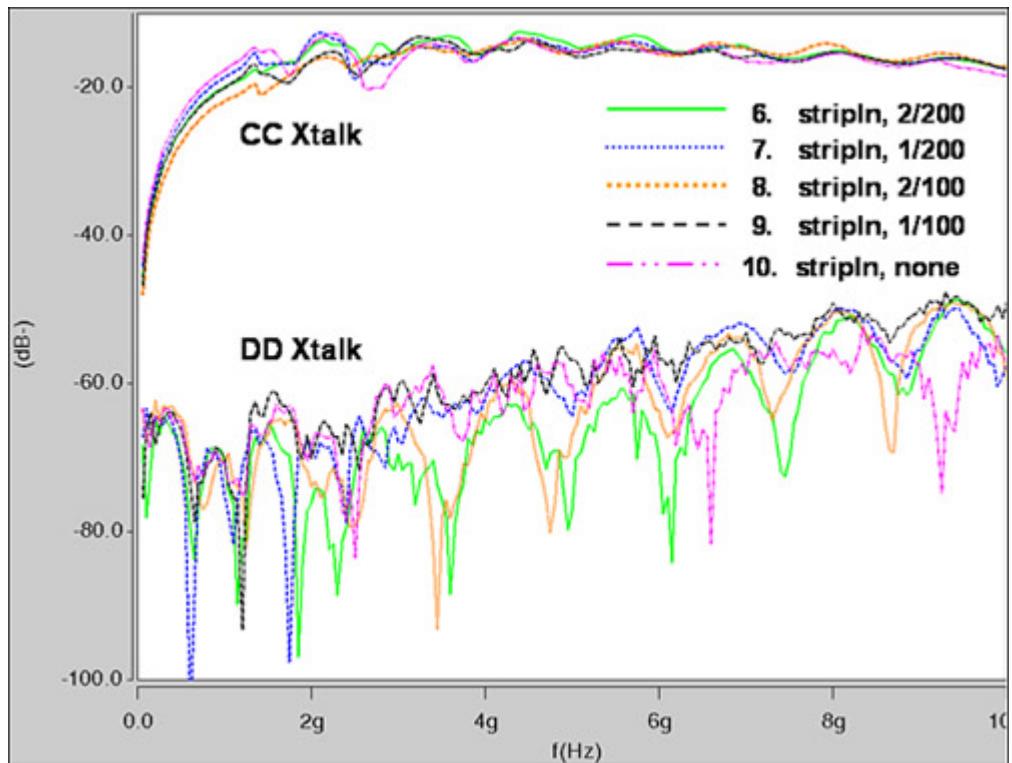
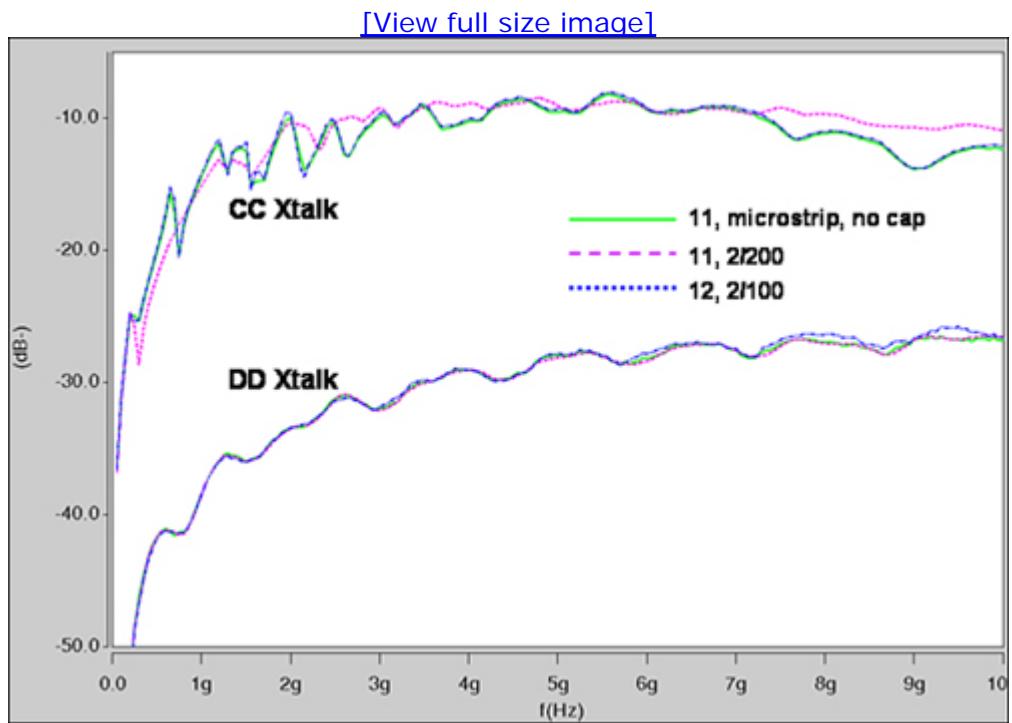


Figure 7.44. VNA measurement for microstrip with stitching caps

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.



7.7.2. Modeling and Measurement Correlations

In engineering practice, due to cost and schedule concerns, the 3D EM solver approach is used more widely than the test board approach. Here, these structures were also modeled with a 3D full-wave EM solver. [Figure 7.45](#) and [Figure 7.46](#) show the simulated common mode TDR and TDT responses, based on the generated 3D models. As expected, both common mode ISI and FEXT followed the stitching condition rank very well, which indicates a good correlation between the test board TDR/VNA measurement and a 3D full wave computational modeling. It should be noted that the absolute magnitudes of the TDR/TDT response are not the same as the test board measurement; due to the simplification of the modeled test structure and measurement and modeling errors.

Figure 7.45. Simulated common mode TDT response based on 3D EM models

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

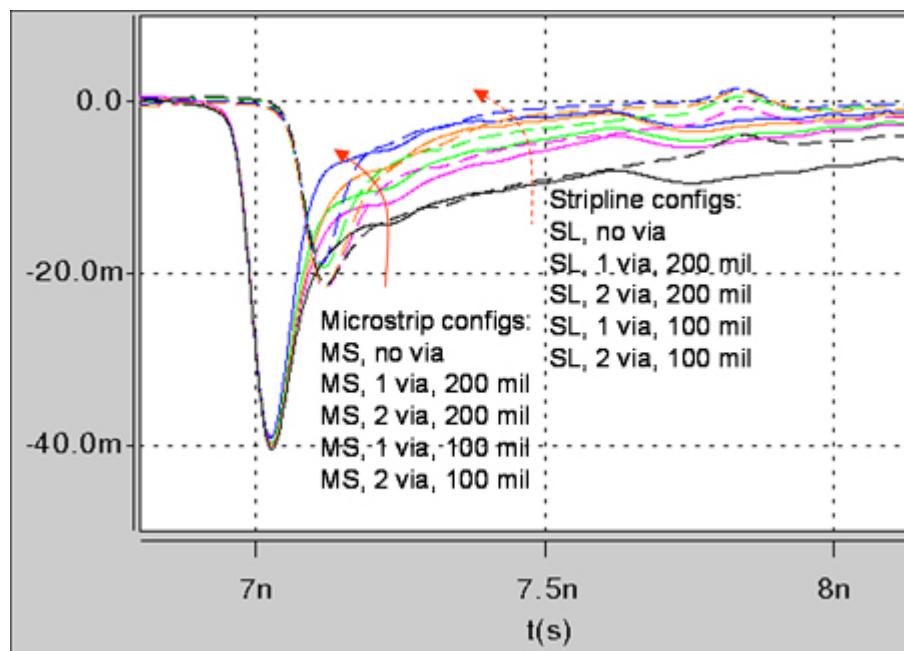
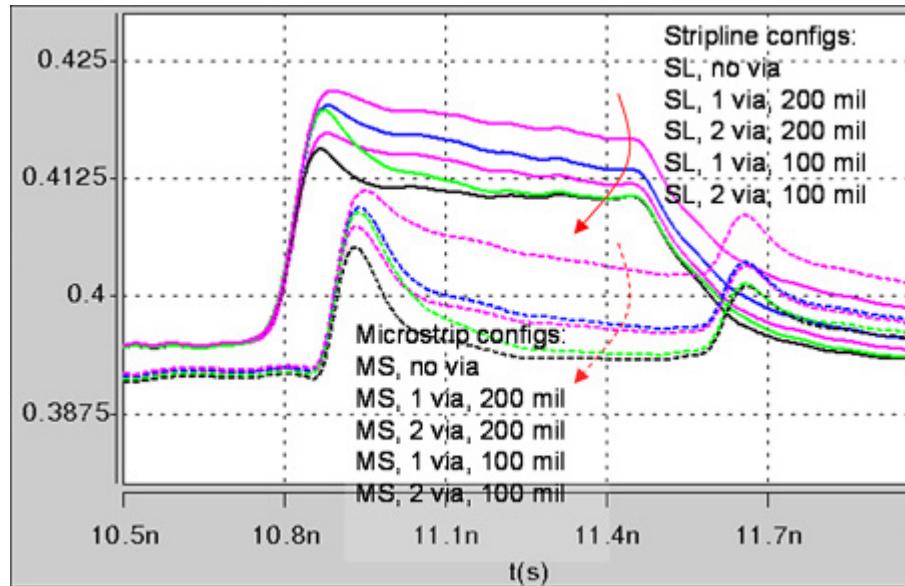


Figure 7.46. Simulated common mode TDR response based on 3D EM models

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.

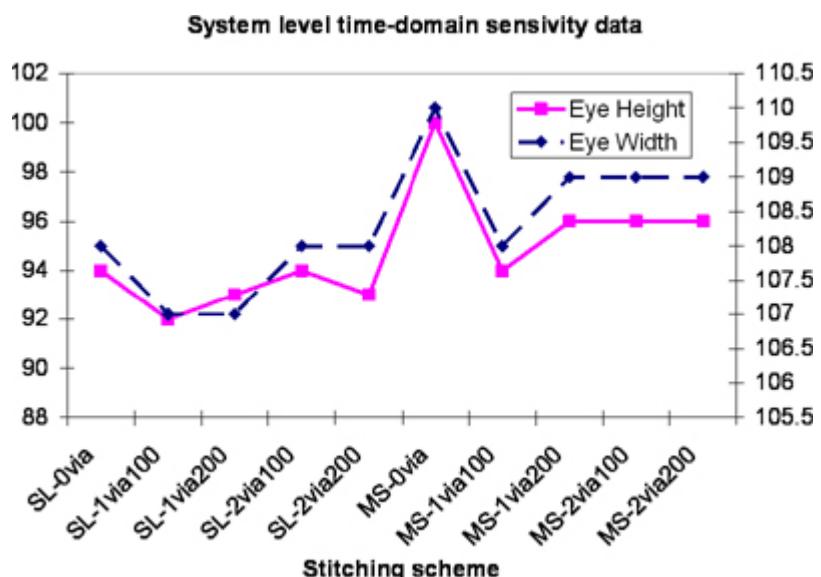


7.7.3. System-Level Impact Evaluation

A system-level simulation based on the 3D full wave EM models was performed. The 3D models were converted to equivalent spice circuits to perform time-domain analysis. Figure 7.47 shows the differential model eye diagrams for a 30-inch 5Gbps stripline link, which has a layer transition that uses one of the ten stitching via schemes in this study. The differential eye height and eye width are insensitive to the stitching scheme. Only 8ps and 4mV changes were observed, and the performance ranking is uncorrelated to the goodness of the stitching scheme.

Figure 7.47. System level simulation results on a 30-inch 5Gbps stripline system—differential mode eye diagrams

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links," 57th ECTC © [2007] IEEE.



A similar study was done on an 8-inch 6.4Gbps microstrip link, as shown in [Table 7.1](#). Two scenarios were analyzed: with and without common mode noise injection on the driver side. When injecting the common mode noise, a 25ps positive and negative buffer timing skew is added at the driver side. Both differential mode eye diagrams and common mode AC noise were compared. The key observation is that the stitching cap is not effective in terms of helping differential mode signaling or reducing common mode noise. Both system-level case studies match component level characterization and analysis very well.

Table 7.1. System Level Simulation Results on an 8-Inch 6.4Gbps Microstrip System

	No CM Injection		With CM Injection		
	DM EH (mV)	DM EW (ps)	DM EH (mV)	DM EW (ps)	AC CM (mV)
No Transition	73	100	69	98	37
2 decap, 100 mil	65	96	60	94	38
1 decap, 600 mil	65	96	61	95	41

Source: M. Wang and W. H. Ryu, "System Level Impact of Stitching Vias and Capacitors for High-Speed Differential Links,, 57th ECTC © [2007] IEEE.

In summary, this section discusses the link-level impact and design guidelines of stitching vias and stitching decoupling capacitors for high-speed differential systems. Consistent results were obtained between test board VNA/TDR characterization and 3D full-wave EM modeling. Although the number and distance of stitching vias and decoupling capacitors have little or no impact on differential mode crosstalk and ISI, their impact on common-mode crosstalk and ISI is high. Furthermore, effectiveness of stitching decoupling capacitors is low at high frequencies compared to stitching vias. Link-level time domain analysis was also performed and key conclusions were confirmed at the system level. Finally, a routing guideline for a platform design was recommended for stitching vias and caps. Here, a 100-mil stitching via distance is recommended if AC common-mode specification for I/O circuits and EMI specifications are tight. However, this rule may be significantly relaxed if AC common mode noise and its induced EMI issue is only a slight concern.

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7.8. EMI Trade-Off

Chapter 3, “Electromagnetic Effects,” described the various electromagnetic aspects of a signaling system that must be considered in detail to achieve the high speeds required in systems today and in the future. An optimized design can be achieved only by designing for power integrity, signal integrity, and EMC early in the design cycle [18].

7.8.1. Power Islands Radiation

Power plane shapes need to be carved out in the layers of the motherboard to reduce the reference plane transitions that cause noise coupling into the signals. However, these plane shapes need to be properly designed to prevent excessive radiation. Due to the noise current of switching I/O buffers, the radiation from power-ground plane resonance of multilayer PCBs can cause a large amount of emission. Although it is well known that the peak frequencies of radiated emissions are related to cavity-mode frequencies, many theories about the location and size of decoupling capacitors have been studied in relation to board size, thickness, and frequency of interest.

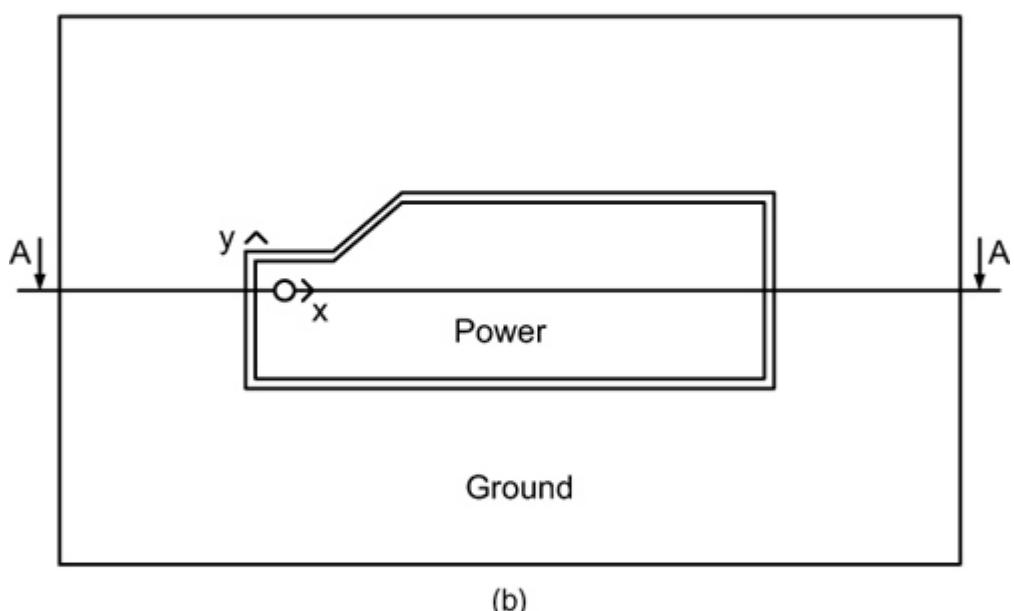
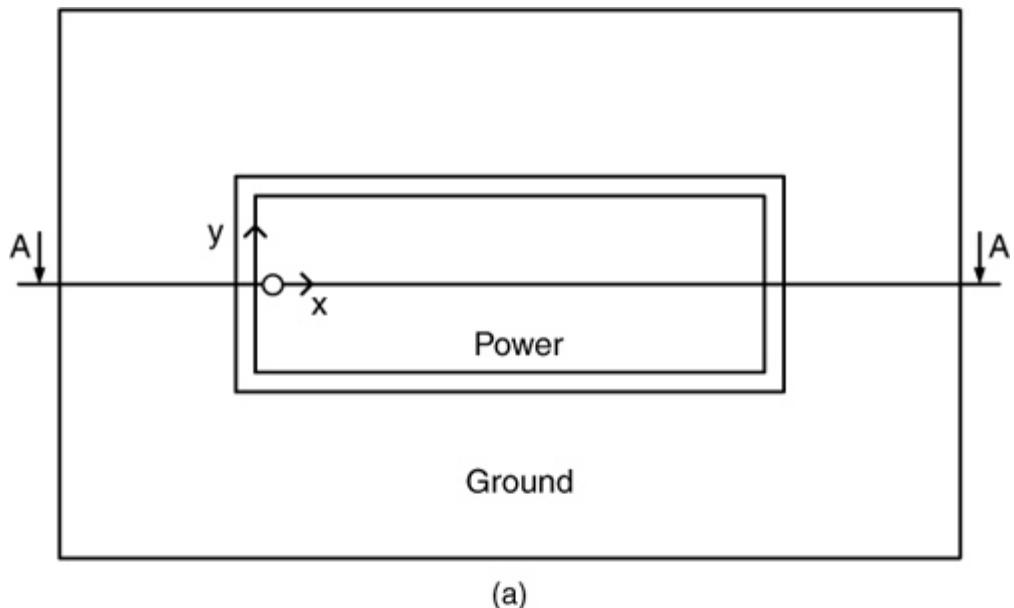
Power islands for DDR3 devices running at 1066MT/s and motherboard (MB)/DIMMs can be a source of radiation not only because of the multilayer power-ground cavity but also because of the microstrip antenna (also called patch antenna) that may be associated with the geometry [12, 13]. Edge radiated coupling phenomenon and cavity resonances can be reduced by using adequate remedies [14, 15].

The isolation between the ground and power areas shown in Figure 7.48 can be achieved by having a large gap and series impedance between the coplanar ground-power pair [16]. When far away from the cavity resonances of the power/ground pair, the coupling between the two islands is weak because the gap capacitance is extremely low, compared to the interplane capacitance. However, at frequencies where the power bus structure is resonant, it is possible to obtain relatively good coupling between planes, and the isolation can be significantly reduced. Other constraints may not allow mitigation techniques, such as having a symmetric stack up or no open edges.

Figure 7.48. Power-bus structure (geometric details) for a two- and four-power-layer board stackup

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Section A-A 2-Layers board



Section A-A 4-Layers board



(c)

The study of the radiation mitigation of a multilayer stackup with power-islands is performed starting from the analysis of cavity resonances and

radiating frequencies. [Figure 7.48 \(a\)](#) has been studied as a starting point in a two-layer configuration, whereas [Figure 7.48 \(b\)](#), which is a more complex and realistic geometry, has been studied with the four-layer stack-up configuration, as shown in [Figure 7.48 \(c\)](#).

The two conducting plates of [Figure 7.48 \(a\)](#) have width $W = 1.4$ -inch and length $L = 5.3$ -inch, conductivity $\sigma = 5.7e7$ S/m, and are separated by a dielectric of relative permittivity $\epsilon_r = 4.2$ and loss tangent $\tan \delta = 0.002$.

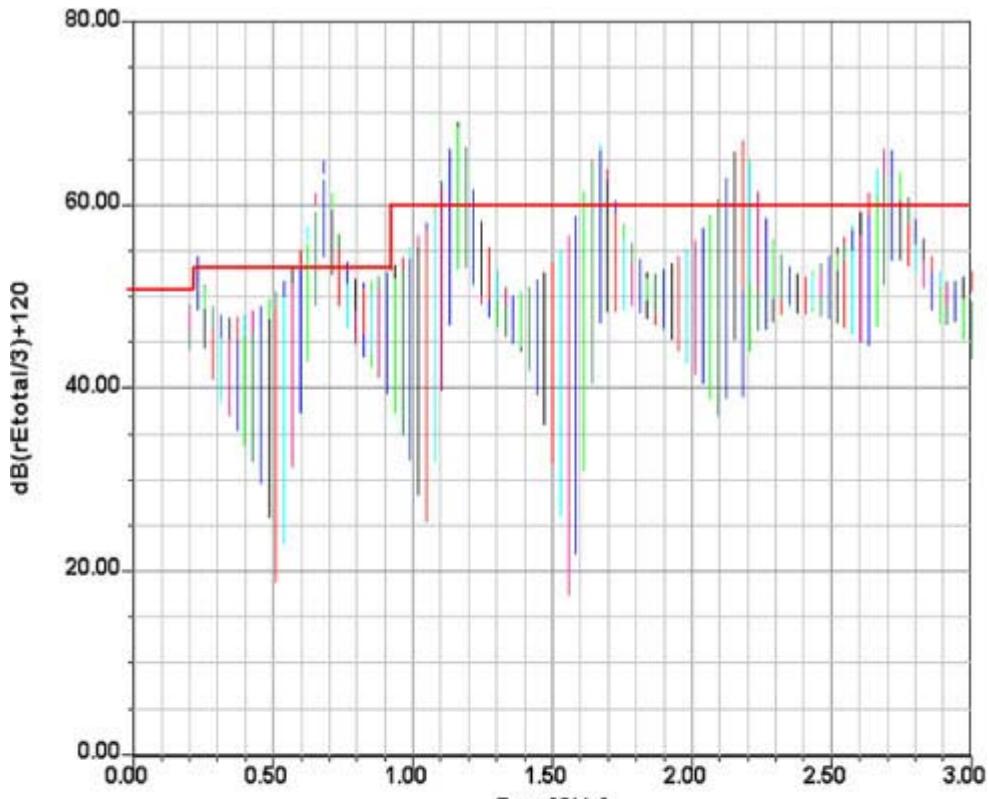
The separation distance is $h = 3.9$ mils. The plates have been excited by a voltage source $V_s = 20$ mV with a small series resistance $R_s = 50m\Omega$, representing the noise voltage due to the SSO of the memory controller on the board. The voltage source is inserted at $x = 0.1$ -inch, $y = 0$. The frequency range of interest is 200MHz to 3GHz. The ground plane dimensions are $12'' \times 13''$. A bare board analysis with no components other than the voltage source V_s provides insight about the cavity resonances and the radiation emission levels associated with them. As expected, all the peak resonances in the radiation spectrum are related to the cavity resonance frequencies of the power-bus: $f_r = 523$ MHz, 1.05MHz, 1.58GHz, 1.99GHz, 2.06GHz, 2.11GHz 2.26GHz, 2.55GHz, and 2.65GHz.

The analysis of the emission profile measured in $dB\mu V/m$ at 3 meters shows that without using any EMI precaution, this simple structure can radiate beyond the FCC Class B open-box limits. The radiation can be reduced by 3 to 10dB by using 8 to 10 decoupling capacitors ($C = 10nF$, $ESL = 0.5nH$ and $ESR = 22m\Omega$), by increasing the gap size from 16mils to 30mils, and by adding a well-connected ground filling area around the power island. [Figure 7.49](#) shows the reduction in the emission level obtained. The following table depicts a number of the before-and-after peak emissions:

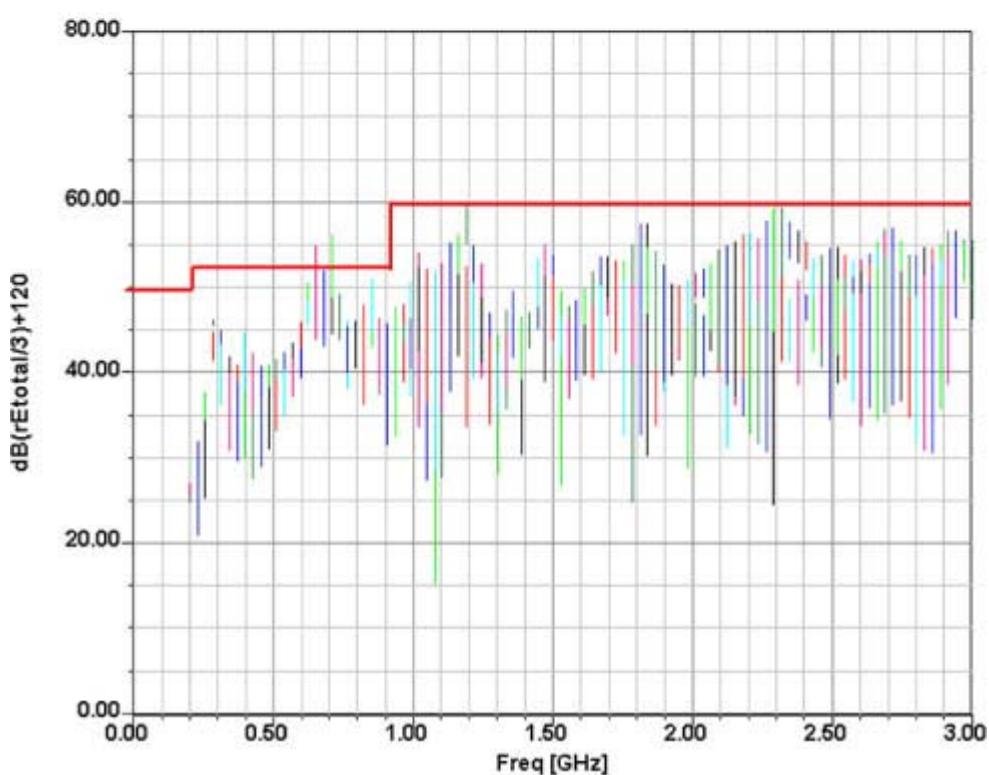
Old Values	New Values			
680 MHz	64	780 MHz	59	
1.18 GHz	69	1.2 GHz	60	
1.67 GHz	66	1.7 GHz	58	
2.18 GHz	67	2.3 GHz	60	
2.7 GHz	66	2.7 GHz	59	

Figure 7.49. 2D Finite Elements Method simulation results for rectangular two-layer bare (a) and modified (b) board

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(a)



(b)

The more complex shape in Figure 7.48 (b) has dimensions $W_1 = 1.4"$ $W_2 = 0.9"$, length $L_1 = 5.3"$, $L_2 = 4"$ (with the indexes 1 and 2 indicating the shortest and longest segments, respectively). The separation distance is

different for each of the power/ground pairs and varies from $h = 3.9\text{mils}$ to $h = 20\text{mils}$. The plates have been excited by a voltage source $V_s = 10\text{mV}$ with a small series resistance of $R_s = 50\text{m}\Omega$. The frequency range of interest in this case is 150MHz to 1.5GHz.

The ground plane extent is $12'' \times 13''$. The 3D Finite Element Method has been used to perform the simulations shown in [Figure 7.50](#). The bare board (no vias or decoupling capacitors between power and ground) emission level is above the FCC Class B open box limits. By adding ground connections, and stitching vias, and inserting an adequate number of decoupling capacitors, 22 in this case ($C = 10\text{nF}$, $\text{ESL} = 0.5\text{nH}$, $\text{ESR} = 22\text{mOhm}$), it has been possible to dramatically reduce the emission level of the board. The location of the decoupling capacitors has been based on the electric field map at the peak frequency of 1.35GHz, as shown in [Figure 7.51](#), and capacitors have been located where the electric field was denser, offering a return path to the currents. An optimization algorithm can be applied to better locate the decoupling capacitors and to automatically determine the value of the decoupling capacitors.

Figure 7.50. 3D Finite Elements Method simulation results for complex shape on four-layers boards; comparison with and without EMI mitigation

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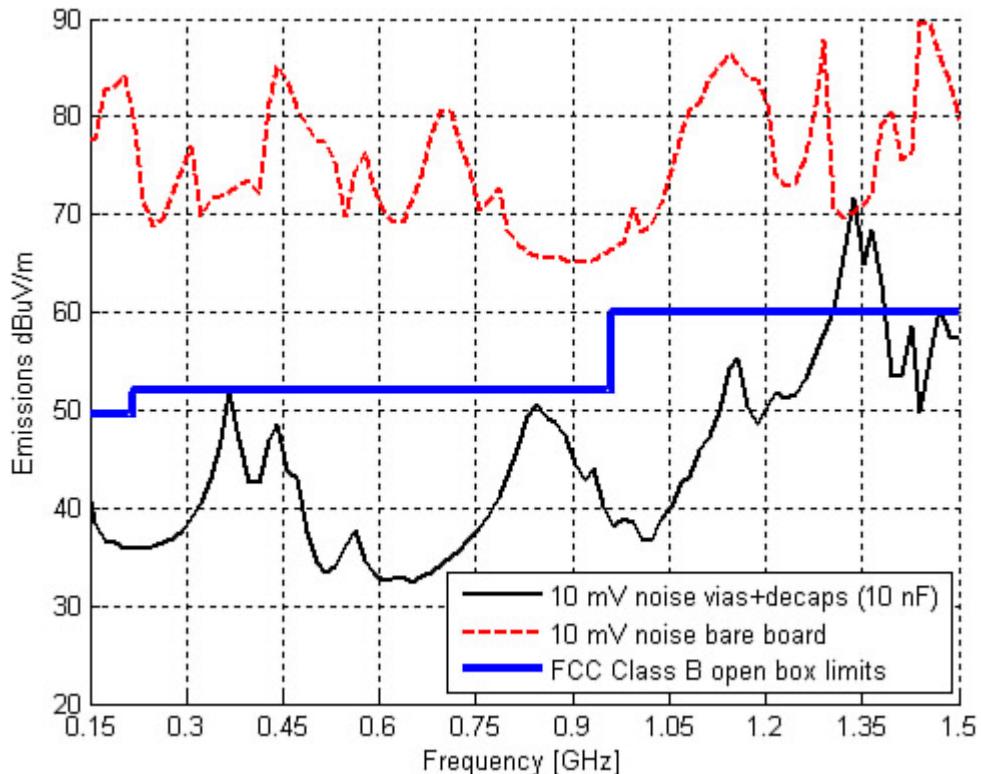
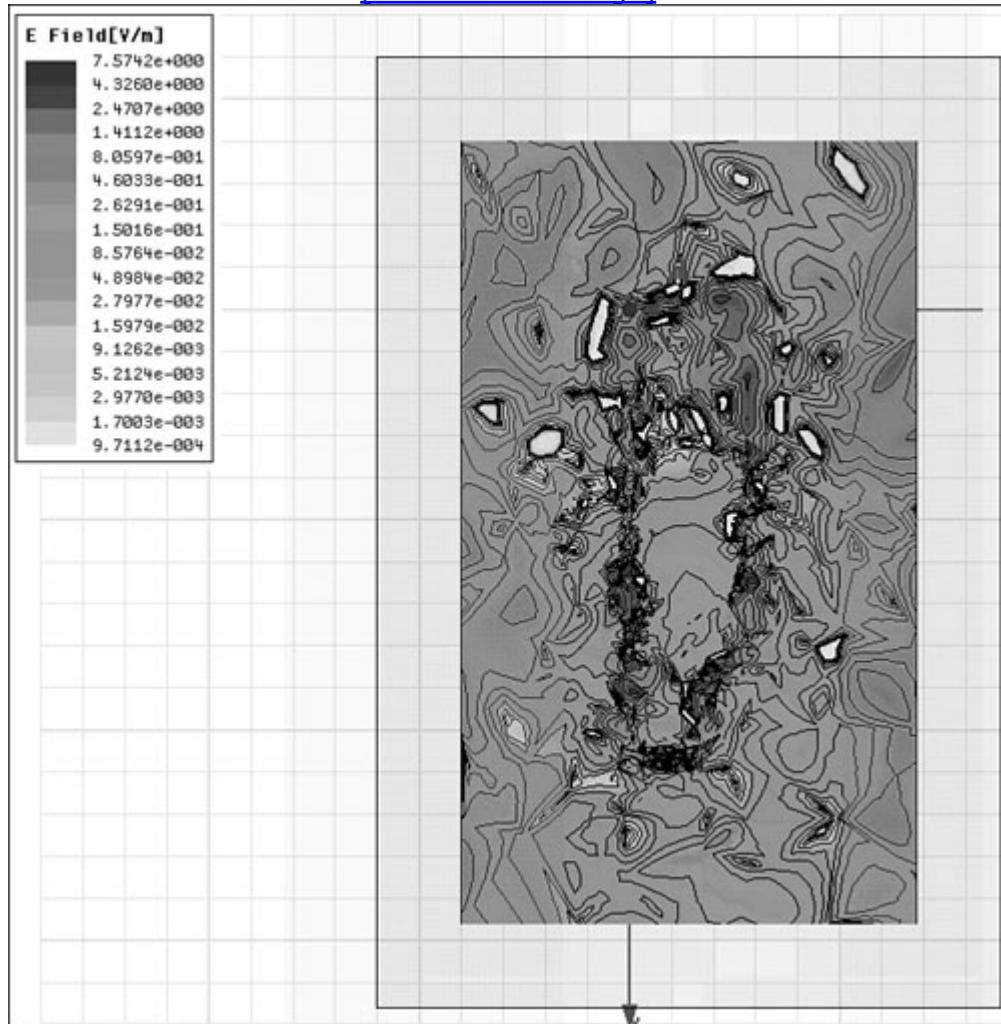


Figure 7.51. 3D Finite Elements Method simulation results for complex shape on four-layers boards showing regions of high electric fields suggesting the locations where the decoupling capacitors are needed

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EMI has to be taken into consideration early in the design process to avoid problems later. The multilayer parallel-plate configuration can be studied with a combined cavity/patch-antenna approach. By means of simulation results, it has been shown how significant the impact of radiations can be if precautions and design strategies are not taken into consideration.

Simulation investigation can provide insights about the amount and nature of the radiations. Because the radiated field is proportional to the spacing between the planes, the cavity resonance or the patch-antenna mechanism plays different roles depending on the thickness of the board [17]. Reducing emissions has a cost in terms of space allocation on the board, along with manufacturing and components costs; therefore, early stage simulations

and analysis can show if remedies are needed or not. This simulation work has shown that by considering similar structures and similar remedies, the potential gain achieved in terms of mitigation of radiation level can be quite significant.

In this chapter, we described the power delivery to signal coupling mechanisms. The power noise can be coupled to the signal traces through driver circuitry and reference transitions and can get amplified by channel resonances. The effect of stitching vias and decoupling capacitors on the signal performance was also discussed. Interconnect structures play a major role in power integrity effects on signaling performance. Identifying these power and signal integrity interaction issues at the beginning of the design process is very important, to make the noise mitigation techniques simpler, cost-effective, and more straightforward. [Chapter 8](#), “Signal/Power Integrity Co-Analysis,” explains how to translate these interaction effects into eye voltage/timing margin.

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Chapter 8. Signal/Power Integrity Co-Analysis

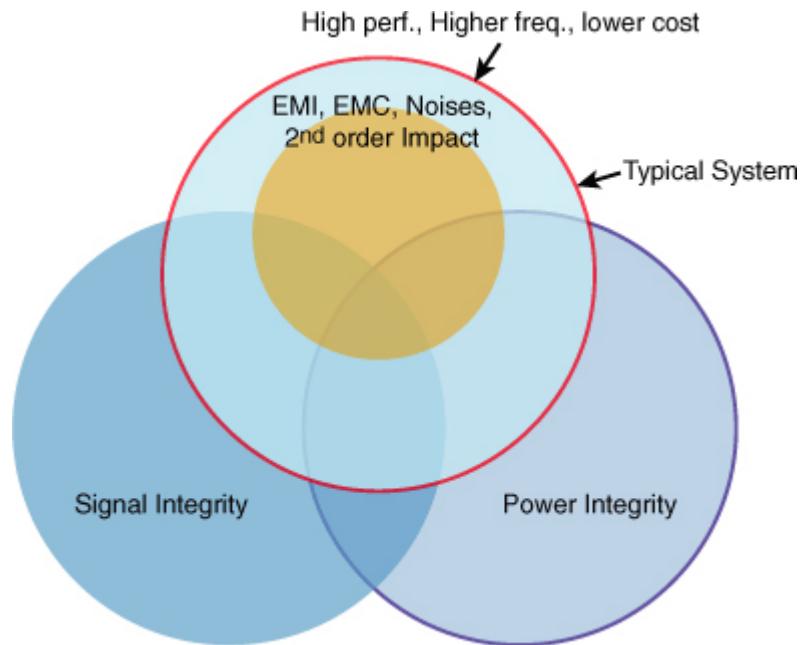
Optimizing and debugging a signal channel and associated Power Distribution Network (PDN) for the best performance is an increasingly challenging task as the digital electronics industry trend goes toward low-power, low-cost, rapid prototyping of high performance products. In particular, low-cost and low-power requirements impose more demanding signal integrity design guidelines with a tighter time domain eye margin. Until recently, signal integrity and power integrity improvement methodologies have been relying on the assumption that the linear characteristic holds for signal integrity and power integrity so that they can be isolated into two separate problems when analyzed for the channel budget. In reality, with nearby buffers switching constantly, The interaction between signal and power through Simultaneous Switching Output (SSO) noise and the buffer behavior makes the channel characteristic somewhat nonlinear. The interaction between signal network and PDN, at chip, package, and PCB, influences the eye voltage/timing margin at the receiver, which can be addressed only by analyzing signal integrity and power integrity together.

[Figure 8.1](#) shows the interaction of signal integrity, power integrity, and Electromagnetic Interference/Electromagnetic Compatibility (EMI/EMC) in a Venn diagram format [1]. Typical systems operate with moderate EMI/EMC impacts. On the other hand, systems for high performance, wide bandwidth, and lower cost tend to be vulnerable to EMI/EMC and second-order impacts from various sources, as shown in [Figure 8.1](#). Unfortunately, more and more systems are moving toward system-critical conditions. Therefore, to optimize the channel for its best performance with the allocated cost restriction and to find the controllable parameter enablers at the same time if there are any, Signal Integrity-Power Integrity (SI-PI) co-simulation, and co-analysis becomes essential methods. In this book, detailed EMI/EMC impact is not included. In [Chapter 7](#), “Signal/Power Integrity Interactions,” the power noise coupling in interconnects has been explained, along with effects of stitching vias and decoupling capacitors on the signal performance. This chapter focuses on the analysis of SI-PI combined impact, taking into effect different noise sources, such as Inter Symbol

Interference (ISI), crosstalk, and SSO—and their interactions.

Figure 8.1. Signal Integrity-Power Integrity and EMI / EMC interaction in a typical system

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



8.1. Identifying Controllable Parameters

Many parameters in the design specifications have some room for adjustment. In the Design of Experiment (DOE) [2, 3] or variables sweeps for SI-PI co-simulation to find the worst case condition of the channel, parameters that are known to impact channel responses greatly are often picked up as DOE variables or parameters to sweep. For instance, on-chip capacitance, on die termination, line length, line impedance, and other components values that can be readily adjusted are the typical candidates for DOE variables or parameters to sweep. Table 8.1 shows the controllable parameters for a typical system with a high-speed channel. Some of the parameters are predetermined because the manufacturing process parameters are fixed at a certain stage, and these parameters cannot be changed any further. Controllable parameters are parameters that the designer can still adjust within a certain range; for example, turn-on resistor (R_{on}), Slew Rate (SR), On-Die Termination (ODT), Power Delivery (PD) on-chip capacitor (C_{die}), bump-out plan, trace width and spacing between lines, pin-map plan, on-board termination (Rtt), interconnect topology, stub resistor (R_{stub}), series resistor (R_s), decoupling capacitor, referencing scheme, and so on. Realistic and realizable optimization ranges must be used for the controllable parameters in SI-PI co-simulations. On the other hand, uncontrollable parameters are parameters that are set by the board vendor or by feedback from the substrate designer; for example,

Printed Circuit Board (PCB)/package manufacturing tolerances, other passive element tolerances, silicon process variations, stack-up parameters (dielectric/conductor height and material properties) after the certain design stage, and limited signal trace width and spacing because of the limited layout space. In modeling passive components, the model parameters assume the assigned values that are samples within their variable ranges. Therefore, multiple models are generated for multiple sets of variable values.

Table 8.1. Examples of Controllable/Uncontrollable Parameters for a Typical System

Examples	SI/PI Controllable Variables	SI/PI Uncontrollable Variables
Silicon	Ron, slew rate, ODT, intentional PD cap, bumpout, I/O and EQ scheme, power grid routing	I/O count, I/O device capacitor, unintentional PD Cap, integrated passive element tolerances, silicon process variations
Package/Socket	Trace width and spacing between lines, pin-map, referencing scheme, decoupling capacitor, stackup parameters before the certain design stage	I/O pin-count, package manufacturing tolerances, passive element tolerances, stackup parameters (dielectric height and constant) after the certain design stage, limited signal trace width and spacing
PCB	Trace width and spacing between lines, Rtt, interconnect topology, Rs in memory channel, referencing scheme, decoupling capacitor, stackup parameters before the certain design stage	PCB manufacturing tolerances, passive element tolerances, stackup parameters (dielectric height and constant) after the certain design stage, limited signal trace width and spacing
DIMM/Connector	Trace width and spacing between lines, connector pin-map, Rtt, interconnect topology, stub resistor	Total I/O pin-count, PCB manufacturing tolerances, passive element tolerances, stackup parameters

	(Rstub), referencing scheme	(dielectric height and constant), limited signal trace width and spacing
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8.2. SI-PI Modeling and Simulation

Modeling and simulation only for the signal integrity involves modeling of signal nets assuming power and ground networks are ideal. On the other hand, power integrity-only modeling and simulation usually ignore the power impact to the signal and to the return path. Preparing the simulation deck for SI-PI co-simulation and co-analysis requires special handling of the modeling process because the simulation deck needs to include the interaction between signal nets and power nets. Also, it is important to model them thoroughly from the on-chip level to the board level because the noise impacts that stem from the on-chip components are getting as important as package and board level impacts. Regarding the buffer models, they should also handle power delivery behavior variation and signal behavior variation. Therefore buffer models needs more advanced models than conventional constant-power-node voltage behavioral models.

8.2.1. Modeling SI-PI Compatible Buffers

The system level simulations require end-to-end channel models with compatible buffer models. Transistor level buffer models provide a relatively accurate excitation model but it tends to slows down SPICE-compatible time domain simulations considerably. In addition, it reveals the proprietary information of the manufacturing process, which should be avoided generally. Therefore it is often desired to have SPICE-compatible behavioral models. [Figure 8.2](#) shows the types of behavioral models according to their usages. They are categorized for signal integrity-only models and models for the signal and power delivery together. Subsequently their subcategories are single-ended signaling and differential signaling buffers. One of the ways of generating a behavioral model is typically to use IBIS model methodology or Verilog-A-only methodology, or IBIS with Verilog-A methodology [1]. A commonly used IBIS model described in [Chapter 6, "Time Domain Analysis,"](#) can be used for the purposes in [Figure 8.2](#).

Figure 8.2. Buffer behavioral models for different simulation purposes

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

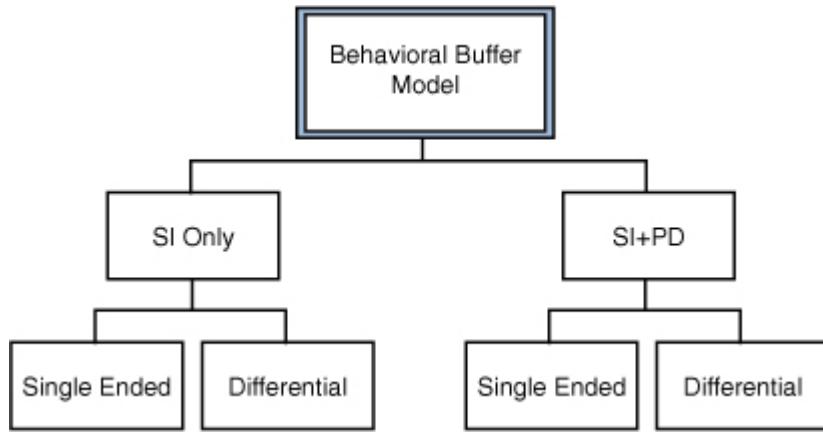


Figure 8.3 shows the construction of an SI-PI compatible behavioral model using signal integrity-only-compatible IBIS model and compensation currents. For this analysis, IBIS model version 3.2 is used, with external Verilog-A modules. Because the signal integrity-only-compatible IBIS models cannot accommodate power node variation, it is needed to compensate the missing current information with the compensation current sources, as shown in Figure 8.3. These currents are dependent on the voltage level of the power node that the currents information are supplied with in table format with different power node voltage level. Figure 8.4 approximately describes the form of an SI-PI-compatible behavioral model with the current variations according to the power node voltage variations. When the model is generated, it needs to verify the accuracy of the model by comparing the I-V, V-t characteristics of the behavioral model with those of the transistor level model. The comparison will always show mismatch to a certain degree; although the usability is dependent on the required accuracy the user needs.

Figure 8.3. Behavioral model construction for SI-PI co-simulation

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

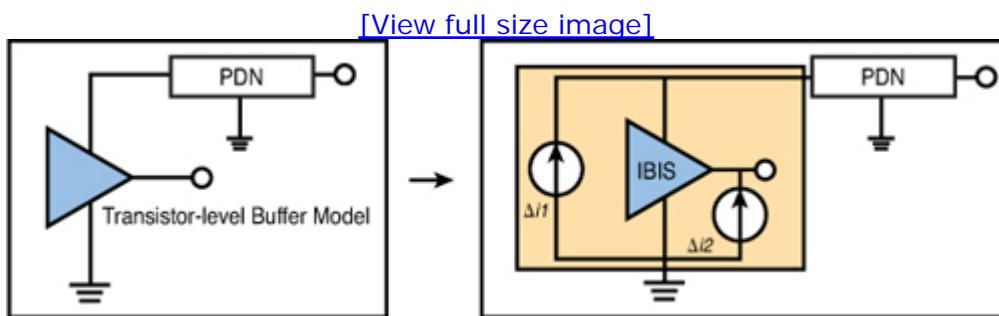
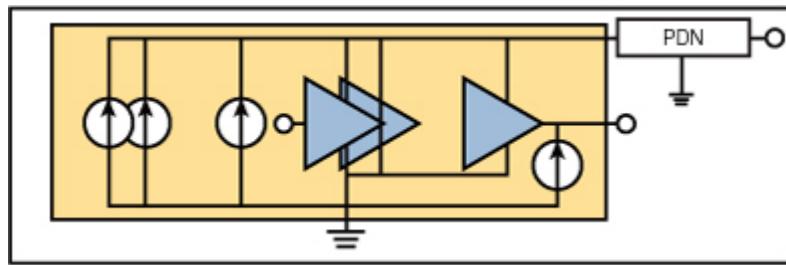


Figure 8.4. SI-PI co-simulation compatible model with variable currents with variable power node voltages

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



8.2.2. Modeling On-Chip Passive Components

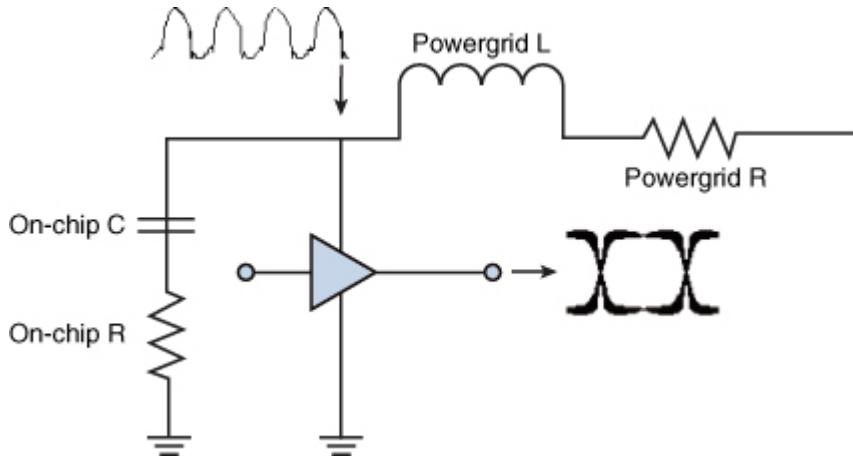
The importance of modeling on-chip passive components is bigger than ever as the impact and sensitivity of on-chip components gets bigger with advancing technology [4, 5]. Especially the on-chip interconnection impact for I/O interface cannot be ignored anymore with a tighter system budget. Figure 5.35 shows an on-chip geometry of the I/O interface.

Electromagnetic (EM) modeling tools extract resistive, capacitive, and inductive elements for the particular on-chip region. The extracted circuits can then be used with the rest of the models in SPICE-compatible simulations. For power delivery modeling, on-chip capacitor assessment is one important aspect that should be performed at the relatively early design stage because the PDN on-chip capacitor does affect the SSO. For I/O signal interconnects, the on-chip pad capacitor is sensitive; and its value should strictly be in a reasonable range for stable system performance.

On-chip level modeling is also essential for SI-PI co-simulation as the SSO is coupled through on-chip PDN to impact signal integrity. Thus, it necessitates modeling of the on-chip power grid, on-chip PDN decoupling capacitor, and its associated series parasitic resistance, as shown in Figure 8.5. However, the simple power grid model, as shown in the figure, cannot handle the buffer current $I_{cc}(t)$ of more than several buffers because current crowding at the single power node is not realistic. In reality, there are several nodes on the power grid model where different buffers are connected. Thus, to handle a higher number of $I_{cc}(t)$, the distributed power grid model should be used. An accurate on-chip PDN model including the power grid and on-chip capacitor should be included in the channel simulation.

Figure 8.5. Simplified On-chip power grid and on-chip PDN capacitor with buffer connection and PDN noise impact on eye jitter

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.



8.2.3. Modeling Off-Chip Passive Components

Off-chip level passive components include packages, sockets, PCBs, and connectors. The purpose of the SI-PI co-simulation methodology is to capture not only the direct response of signal and power networks but also the electromagnetic interaction between them. To capture the SSO and associated secondary effects, planar 3D or full-wave 3D EM modeling needs to be used for the off-chip components. Many commercially available electromagnetic modeling tools provide equivalent circuits or frequency domain transfer functions that are compatible with SPICE. The resulting output model from the modeling tools needs to be passive, causal, and SPICE-compatible to perform accurate time domain simulation.

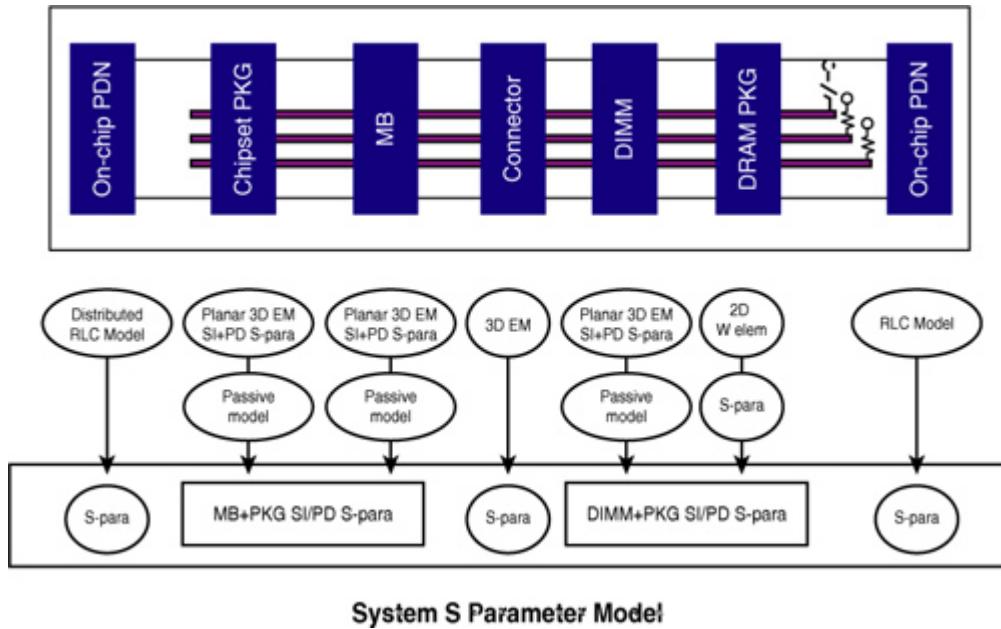
8.2.4. Model Check and Integration

The system level model is comprised of many on-chip and off-chip components. They contain on-chip transistor level buffer, on-chip power grid and decoupling capacitor, off-chip SI-PI passive elements, transmission lines, and the PD structures. Figure 8.6 shows a typical example of the passive SI-PI co-simulation channel configuration for the memory interface. It is essential to check passivity and causality for each component to guarantee time domain convergence and accuracy. Also, the number of ports should be kept as small as possible within a reasonable number to improve numerical accuracy, even though accuracy might vary from one modeling tool to the other. Considering the time domain simulation, sufficiently low-frequency data points are needed to avoid the low-frequency extrapolation error for the SPICE-compatible time domain solver.

Figure 8.6. Example of component models' connections for system channel SPICE-compatible simulation

Source: M. J. Choi and V. Pandit, "SI/PI Co-analysis for I/O Interfaces," IBIS Summit, July 2009.

[\[View full size image\]](#)



The extracted passive macromodel or passive transfer function should have a wide enough frequency bandwidth to cover the time domain buffer slew rate, switching speed, and interaction between signal paths and power delivery networks. For systems operating at a lower gigahertz range, several giga-hertz bandwidth of the model is considered to be adequate to capture signal and power integrity interactions. For systems with higher operating frequencies, resulting model bandwidth should be at least 5 times higher than the fundamental frequency to cover the impact of harmonic frequencies and electromagnetic interactions.

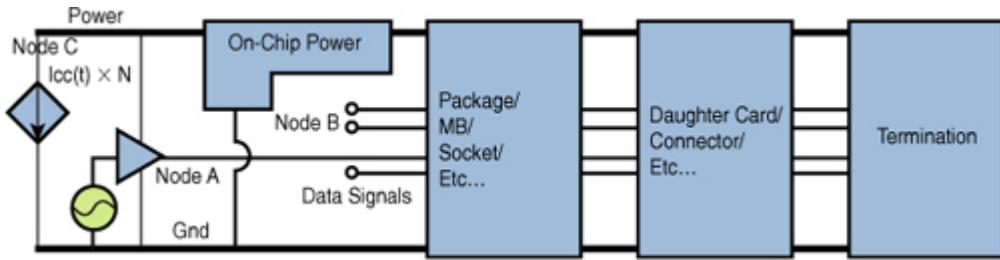
8.2.5. Construction of SI-PI Co-Simulation

Figure 8.7 shows a typical example for the SI-PI co-simulation channel configuration in a computing system. The configuration can be applied to a typical memory channel in the computer system or any other fast signaling systems. It shows an on-chip PDN, package, a motherboard (MB), a socket, a connector, and a daughter card such as a Dual In-line Memory Module (DIMM), and terminations to the signal nets. A similar configuration can be used for differential channel SI-PI analysis.

Figure 8.7. Channel for SI-PI including on-chip PDN and transistor level buffer model

Source: M. J. Choi and V. Pandit, "SI/PI Co-analysis for I/O Interfaces," IBIS Summit, July 2009.

[\[View full size image\]](#)

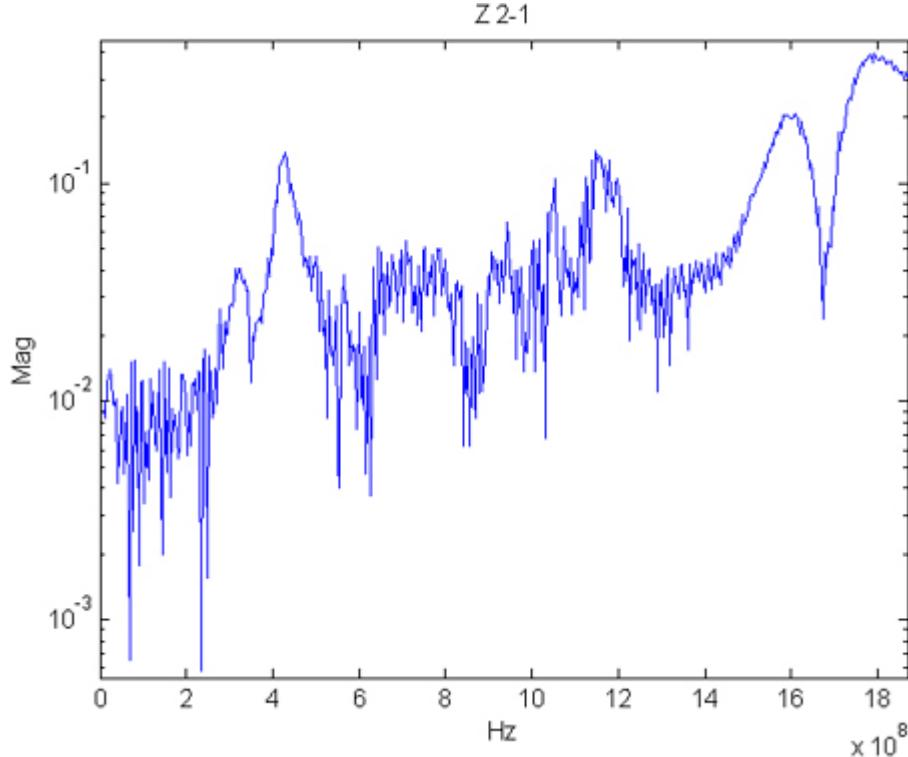


8.2.6. PDN Resonance Excitation of Driver Bit Pattern

Frequency domain spectrum of the SSO excited by buffers depends on the bit pattern of the buffers. A PDN frequency domain response shows certain resonance frequency that should be avoided. [Figure 8.8](#) shows the measured system characteristics example in terms of the Z-parameter response. The measurements are done at the PCB. Transfer impedance between PDN and signal nets shows where the resonance occurs. This resonance contributes to the interdomain energy coupling that worsens the noise coupling. The worst-case scenario for PDN is when the fundamental frequency or harmonic frequency of the bit pattern's frequency domain spectrum hits the resonance frequency of the PD to signal coupling, which often is represented with Z_{21} between PD and signal nets [6]. So the worst-case frequency domain identification of the buffer bit pattern is essential before moving on to time domain simulation. The Z_{21} resonance condition in the frequency domain provides information on what the buffer output pattern should be used to excite the system at the worst case. Low-frequency resonance at the PCB PDN is shown around 430MHz in [Figure 8.8](#). [Chapter 5](#), "Frequency Domain Analysis," illustrates that the PDN frequency domain response is governed by different components, such as the package, PCB, and chip PD routings and PD capacitors. [Chapter 5](#) shows an example of the on-chip PD resonance, and the on-chip PD to signal coupling. The resonance for the system, looking from the on-chip location, occurs at 240MHz as shown in [Figure 5.26b](#). The power-to-signal coupling at the chip also follows the PDN resonance signature, and the transfer impedance at the chip is shown in [Figure 5.43](#), which also shows a resonance at around 240MHz. The PDN resonance at the PCB location can be different than that at the chip location. The worst case patterns for the system can be decided by considering the fundamental frequency of the pattern to excite resonances of the frequency domain spectrum of the transfer function.

Figure 8.8. Measured transfer Impedance Z_{21} between PD domain and signal domain at the PCB [6]

Source: M.J. Choi, V.S. Pandit, and W.H. Ryu, "Controllable parameters identification for high speed channel through signal-power integrity combined analysis," Electronic Components and



A worst-case bit pattern for the worst PD-to-signal coupling can be obtained by checking the frequency domain Z_{21} at the resonance frequencies. For example, if the PDN resonance occurs around 250MHz for the 2Gbps data system, a bit pattern of four 0s and four 1s, as in 00001111, that has 1GHz fundamental frequency will hit the PDN resonance. Harmonic frequencies of a given bit pattern being aligned with Z_{21} resonance frequencies provide another worse situation that should be avoided. It is necessary to consider these harmonic frequencies aligned with resonance frequency to obtain the worst-case situation. The identified worst-case patterns are used in obtaining a maximum PD-to-signal coupling condition. A similar technique, based on the channel frequency domain response, can be also used for finding bit patterns that generate worst-case ISI or worst-case crosstalk.

8.2.7. Worst-Case Eye

The worst-case eye is often the most wanted system performance indicator for system margin analysis. The system shown in Figure 8.7 should be excited with the worst-case pattern to obtain the worst-case eye. However, a linear channel makes it possible to synthesize the worst-case eye from an impulse response or one-bit response, with the Peak Distortion Analysis [7]. This idea makes it possible to synthesize eyes for different patterns because eye diagrams can be constructed by superposing shifted one-bit response. Figure 8.9 shows such a response for a memory system without the crosstalk and with the worst case crosstalk considering all possible phases between victim bit and aggressors. The linearity assumption breaks down

because the power supply variation modulates buffer output pad responses in a nonlinear way and the passive channel responses show nonlinear characteristics. Running a full-time domain SI-PI co-simulation with the worst-case patterns can address the nonlinear channel issues while consuming the simulation time modestly. [Figure 8.10](#) shows a full-time domain simulation response measured for the same system, but without differential strobe signals.

Figure 8.9. One-bit response and worst-case eye constructed by shifting and superposing the response for the single-ended channel with u-Strip host package. Worst case eye diagram without crosstalk (outer eye) and with all phase crosstalks (inner eye).

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.

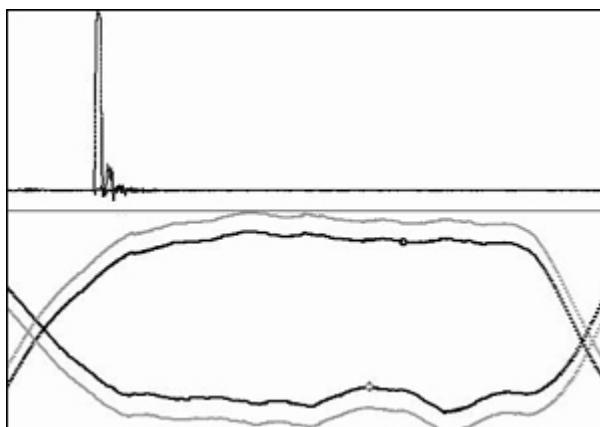


Figure 8.10. Full-time domain SI-PI co-simulation on memory channel with data lines and power delivery but without strobe signals for the system in Figure 8.9

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.

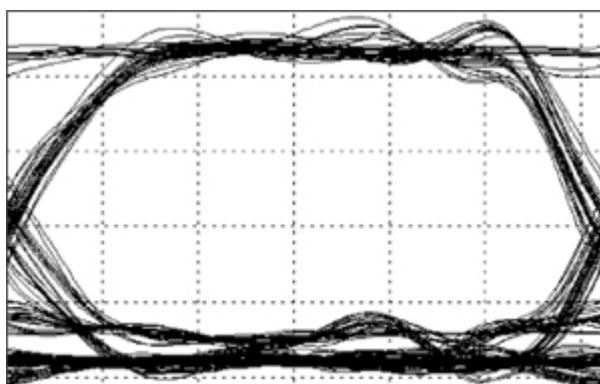
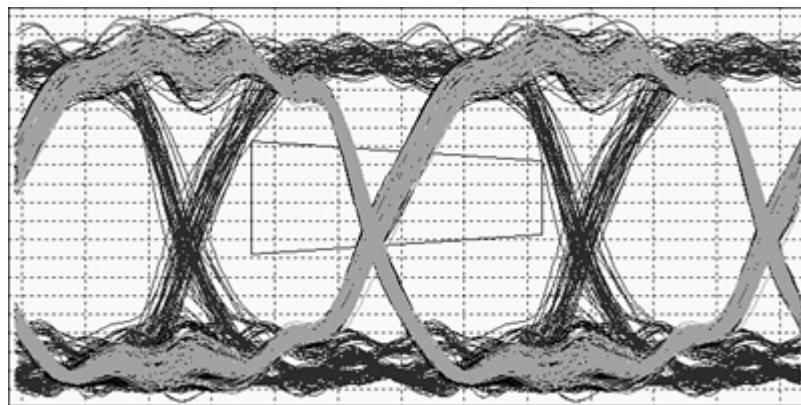


Figure 8.9, Figure 8.10, and [Figure 8.11](#) show the eye responses for the

same memory system. [Figure 8.11](#) shows the full-time domain simulation worst-case eye response including the strobe signals and power delivery networks fully engaged. The eye in the center overlapped with differential strobe signals crossing in the middle shows similar but somewhat different shapes and values from both [Figure 8.9](#) and [Figure 8.10](#) because the system includes differential strobe signal pairs. It is essential to run SI-PI co-simulation to capture the impact of different domains of signals and powers.

Figure 8.11. Full time domain SI-PI co-simulation on memory channel with data lines, strobe signals, and power delivery included signals for the system in Figure 8.9

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.



8.2.8. Running SI-PI Co-Simulation

SI-PI co-simulation puts a heavy computational burden on both modeling of components and simulation of channels. Therefore, it is crucial to clarify the objectives of running the SI-PI co-simulation in the beginning to reduce the number of runs for each case. In the following section, simulation setups are designed to expedite decomposition of noise into distinctive categories, such as ISI, crosstalk, and SSO.

For no-ISI simulation, the minimal ISI is assumed to define the case without ISI, as shown in [Figure 8.12](#), [Figure 8.13](#), and [Figure 8.14](#) [8]. The excitation is called the minimal ISI because it still is a combination of many 0 bits with a 1 bit but the ISI between 1s and 0s is minimized. In [Figure 8.12](#) only 1 bit is on for minimum interference between bits. The eye at the receiver is constructed by wrapping the lone bit waveform twice with the unit interval. [Figure 8.13](#) is another way to generate eye with minimal ISI. The delay time T_d between bits should be long enough to minimize any residue of the previous bit in the next bit excitation. A minimal ISI eye is also generated by applying a transitional waveform, as shown in [Figure 8.14](#) for a couple cycles. The delay time T_d between the bits should be long

enough to minimize any residue of the previous bit or transition in the next bit excitation, too. In this chapter, detailed analysis is presented on response decomposition. In order to identify the margin degradation due to only the ISI, the minimal ISI case is determined. This test case is useful also for response decomposition of other test scenarios. It is to be noted that the bit patterns shown in Figures 8.12 to 8.14 will produce minimal ISI, say up to several GHz. However, beyond these frequencies, such as 10GHz and beyond, even a lone bit pattern can produce a significant ISI due to channel losses. The Worst-case ISI, Crosstalk, and SSO bit patterns are defined by using PDA [7] or by identifying the frequency domain resonances or both. Minimal Crosstalk or minimal SSO refers to the no forced stimulus attached for Node B or Node C, respectively in Figure 8.7, because there are always secondary effects affecting those nodes through coupling even though there is no forced stimulus for those nodes.

Figure 8.12. A lone bit excitation of ISI node for minimal ISI eye construction by wrapping the waveform twice in time domain for the UI

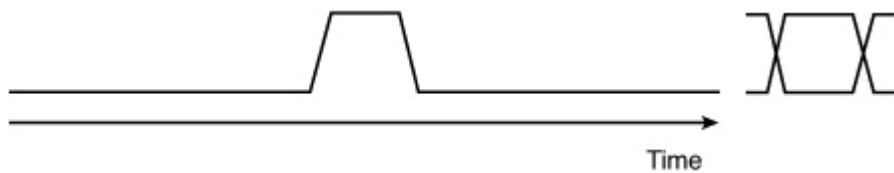


Figure 8.13. Delayed bits excitation of ISI node for minimal ISI eye construction

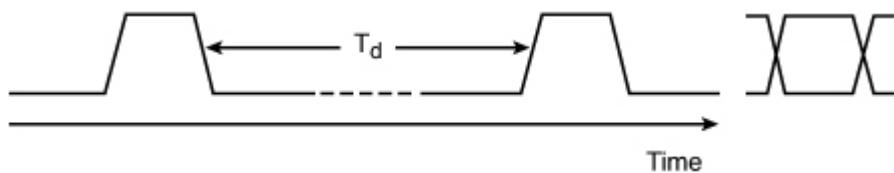
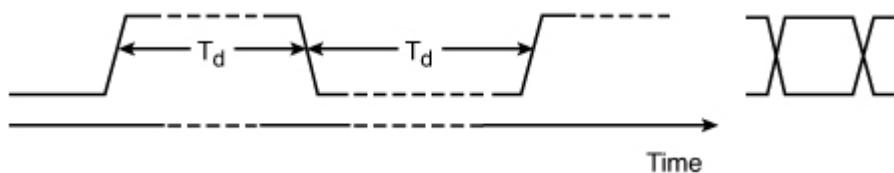


Figure 8.14. Delayed transition excitation of ISI node for minimal ISI eye construction



The following cases are to be run to accommodate noise profiling or the response decomposition of the received signal later in the analysis process.

8.2.8.1. Case for ISI and Minimal ISI

A simulation deck similar to [Figure 8.15](#) can be used for the case to see an eye diagram at the receiver for the minimal ISI or for the eye diagram with ISI. All the crosstalk buffers are turned off and only one victim buffer is on. The victim bit is applied with a lone bit, as shown in [Figure 8.12](#), or delayed bits, as shown in [Figure 8.13](#) or in [Figure 8.14](#) for a minimal ISI case. The received eye represents the eye at the receiver with a minimum ISI. The worst case ISI pattern consists of various bit patterns, as shown in [Figure 8.16](#). It is applied to the victim bit in [Figure 8.15](#), and the eye with ISI but with minimal impact of crosstalk or SSO is obtained. So the comparison between the eye with ISI and the eye without ISI shows clearly the contribution of ISI to the eye.

Figure 8.15. SPICE Deck for ISI or one-bit excitation

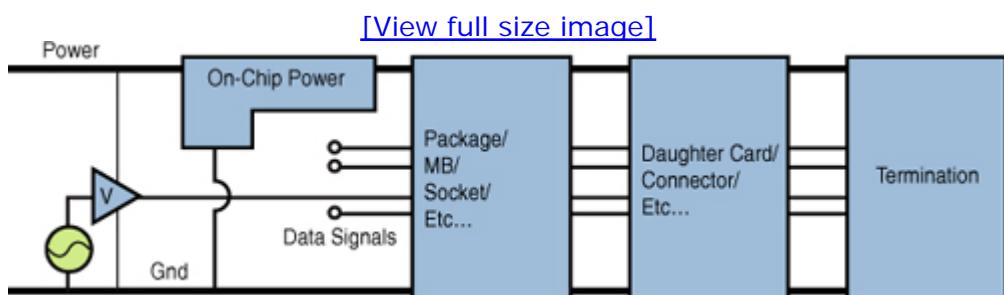
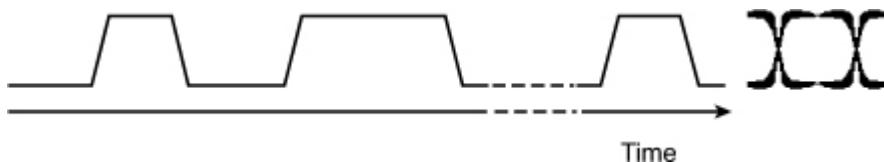


Figure 8.16. Random bit pattern for ISI



In summary, the following two cases for receiver eyes are obtained from the setting in [Figure 8.15](#):

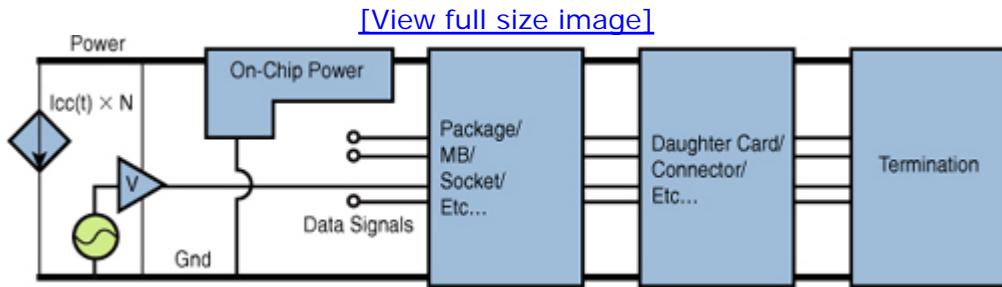
- Eye with minimal ISI, crosstalk, or SSO
- Eye with ISI but without crosstalk or SSO

8.2.8.2. Case for ISI and SSO

Simulation with $I_{cc}(t)$ activated with bit patterns, as in [Figure 8.17](#), simulates a system with the SSO. While keeping the victim buffer without ISI or SSO by using the same method in [Figures 8.12, 8.13, 8.14](#), and [8.16](#), the following two cases for receiver eyes are obtained:

- Eye with the SSO but with minimal ISI or minimal crosstalk
- Eye with the SSO and ISI but with minimal crosstalk

Figure 8.17. SPICE deck for ISI and SSO simulation

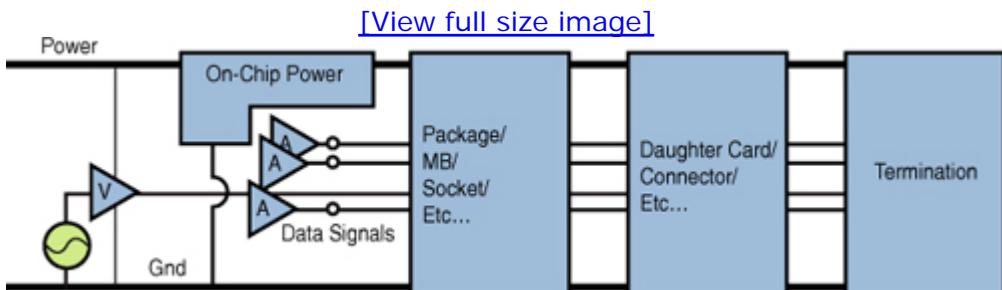


8.2.8.3. Case for ISI and Crosstalk

Simulation with other aggressor buffers activated with bit patterns as in [Figure 8.18](#) simulates a system with crosstalk. While keeping the victim buffer with ISI or minimal ISI by using the same method in [Figures 8.12, 8.13, 8.14, and 8.16](#), the following two cases for receiver eyes are obtained:

- Eye with crosstalk but with minimal SSO or minimal ISI
- Eye with crosstalk and ISI but with minimal SSO

Figure 8.18. SPICE deck for ISI and crosstalk simulation



8.2.8.4. Case for ISI, SSO, and Crosstalk

Simulation with other aggressor buffers activated with bit patterns and with $I_{cc}(t)$ attached as in [Figure 8.19](#) simulates a system with crosstalk and the SSO. While keeping the victim buffer with ISI or minimal ISI by using the same method in [Figures 8.12, 8.13, 8.14, and 8.16](#), the following two cases for the receiver eyes are obtained:

- Eye with crosstalk and SSO but with minimal ISI
- Eye with crosstalk, SSO, and ISI

Figure 8.19. SPICE deck for ISI, crosstalk, and SSO simulation

[\[View full size image\]](#)

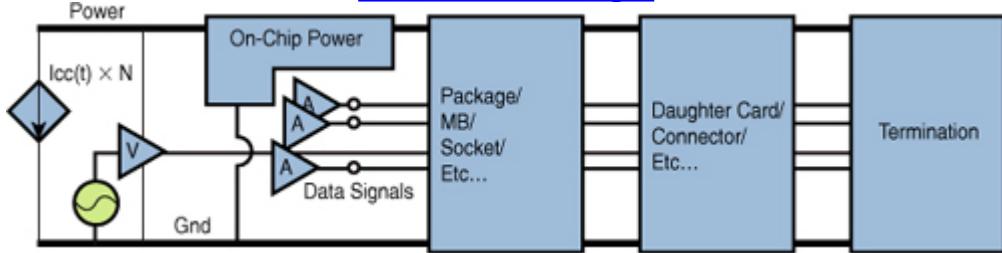


Table 8.2 shows the SI-PI co-simulation cases to accommodate response decomposition for the particular simulation condition. Comparison between cases reveals the contribution of the impact from each noise category or each noise category with secondary noise interactions. For example, comparison between the eye of case #8 and the eye of case #6 shows the impact of SSO with the second order ISI and crosstalk interaction. Comparison between the eye of case #8 and the eye of case #4 shows the impact of the crosstalk with the second order ISI and SSO interaction. Comparison between the eye of case #8 and the eye of case #7 shows the impact of ISI with the second order crosstalk and SSO interaction. The comparison between Case#3 and Case#1, Case #5 and Case#1, and Case#2 and Case #1 show the first order impact of the SSO, crosstalk, and ISI, respectively. In general, you want the second order impact is required to be included in the analysis, however, the decomposition shows a better picture of the noise interaction mechanisms. In summary, running and comparing cases #1, #2, #3, and #5 reveals the first order impact of the ISI, SSO, and crosstalk. Running and comparing cases #4, #6, #7, and #8 reveals the second order impact due to interactions. Running and comparing all of them can show how linear the channel is in terms of noises interactions.

Table 8.2. SI-PI Co-Simulation Cases for Response Decomposition

Forced Stimulus Setups for SI-PI Co-simulation				
	Case #	ISI	Crosstalk	SSO
ISI	1	Minimal	Minimal	Minimal
	2	Yes	Minimal	Minimal
SSO, ISI	3	Minimal	Minimal	Yes
	4	Yes	Minimal	Yes
Crosstalk, ISI	5	Minimal	Yes	Minimal
	6	Yes	Yes	Minimal
Crosstalk, ISI, SSO	7	Minimal	Yes	Yes
	8	Yes	Yes	Yes

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8.3. SI-PI Co-Analysis

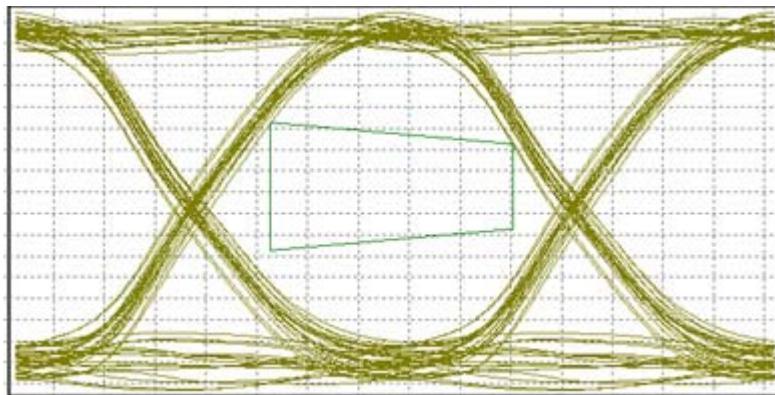
The simulations performed for the SI-PI combined effects need to be analyzed for the purpose of optimization. One of the best ways to analyze the simulation is to analyze margins and noises. The following section shows how the parameters are used for optimization, and the noise is measured and analyzed for system performance.

8.3.1. Time Domain Analysis

The time domain eye diagram is an excellent measure for system performance. It shows the margin for the system as in [Figure 8.20](#). With proper simulation settings, as shown in [Table 8.2](#), the measured eye diagrams can be analyzed to identify the noise from different mechanisms.

Figure 8.20. Eye diagram with a mask

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



8.3.1.1. Optimization Using Sweep Parameters and Noise Decomposition

SI-PI co-simulation analysis is a valuable tool when referencing scheme impact should be analyzed. A memory channel with controller package signal lines designed as stripline sometimes use different referencing depending on the mechanical and electrical routing limits. Signal integrity-

only or power integrity-only simulation can hardly reveal the power domain referencing impact to the signals. Therefore SI-PI co-simulation is used to assess the referencing scheme. Intuitively it is suspected that ground single referencing would be better than ground and power dual referencing for the particular component because of the coupling from the power to the signal. Going in further into the simulation to prove the intuition, the cases in [Table 8.2](#) can be compared to properly measure the impact of ISI, crosstalk, and SSO.

The bit pattern shown in [Figure 8.21](#) is obtained in the receiver ISI node, and the corresponding eye, jitter measurement, and power node variations are shown in [Figure 8.22](#), [Figure 8.23](#), and [Figure 8.24](#), respectively. [Figure 8.25](#) shows the channel performance with an on-chip power delivery capacitor and two different types of packages as sweep variables. The eye diagram unit interval is 750pS, and the power reference voltage is at 1.5V. Here, package #1 uses dual-referenced strip-lines, and package #2 uses single-referenced striplines. Package #2 with single referencing shows better performance with an on-die capacitor sweep than package #1 with dual referencing.

Figure 8.21. Bit pattern received at the receiver for ISI node

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

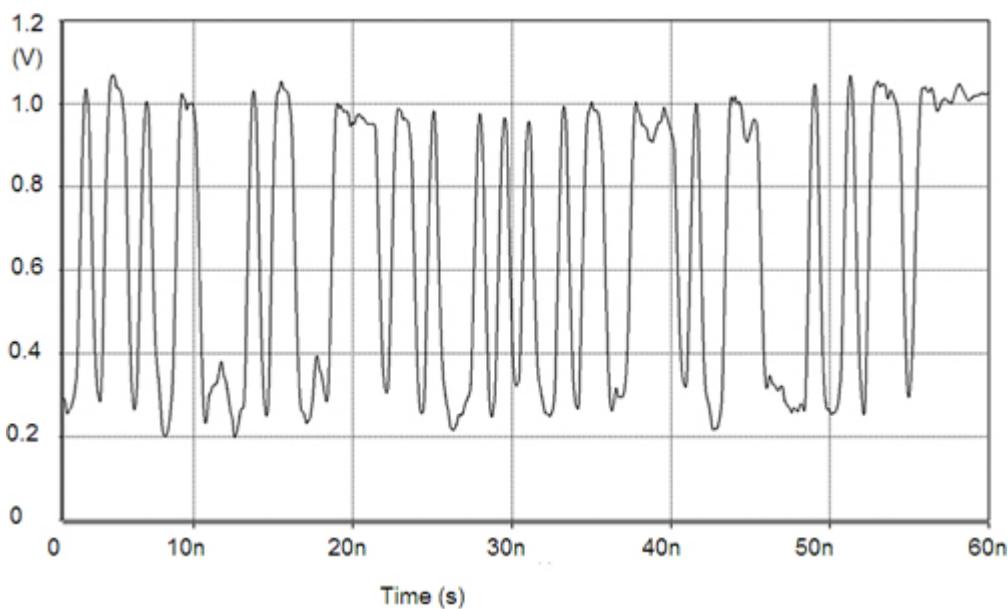


Figure 8.22. Eye diagram measured at the receiver node

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

[\[View full size image\]](#)

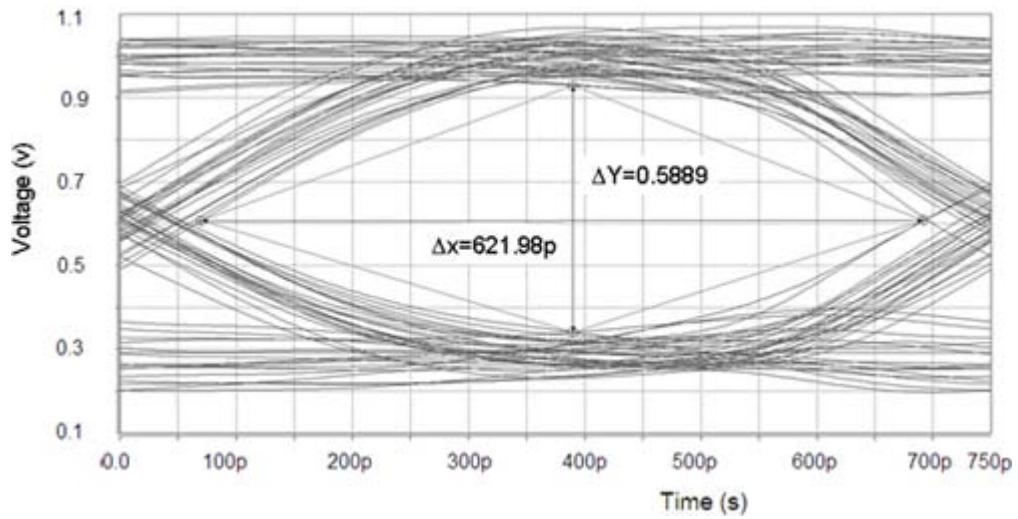


Figure 8.23. Shifted eye for jitter measurement

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

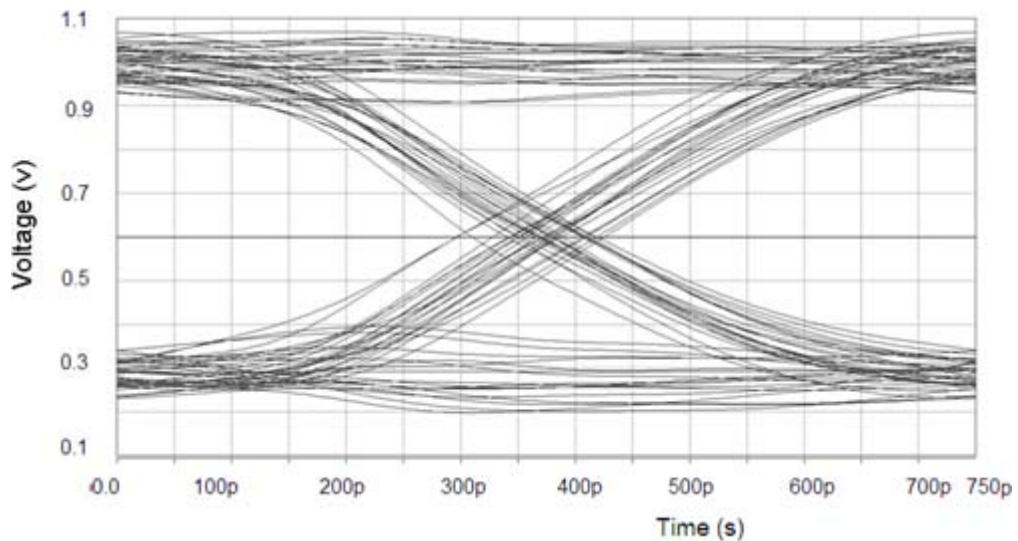


Figure 8.24. Power node variation measurement at the receiver

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

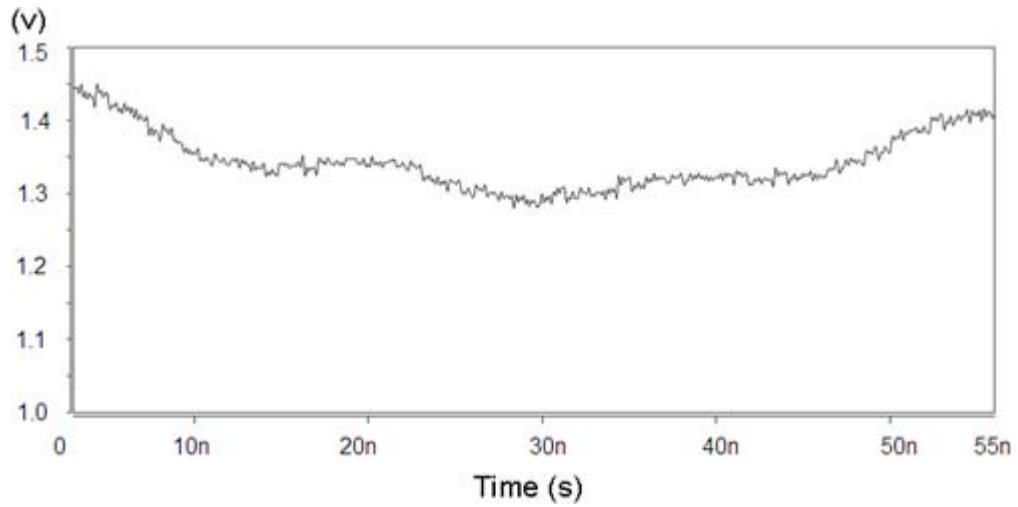


Figure 8.25. Eye Width for different packages and different on-chip capacitor values. Package #1 uses dual referencing. Package #2 uses single referencing.

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

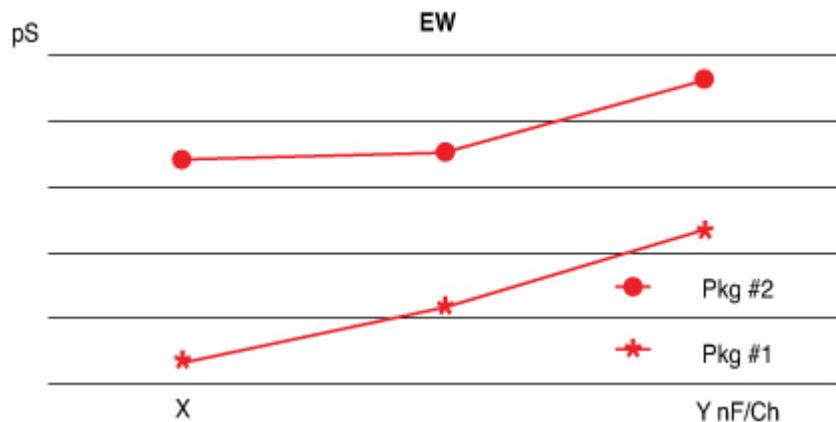
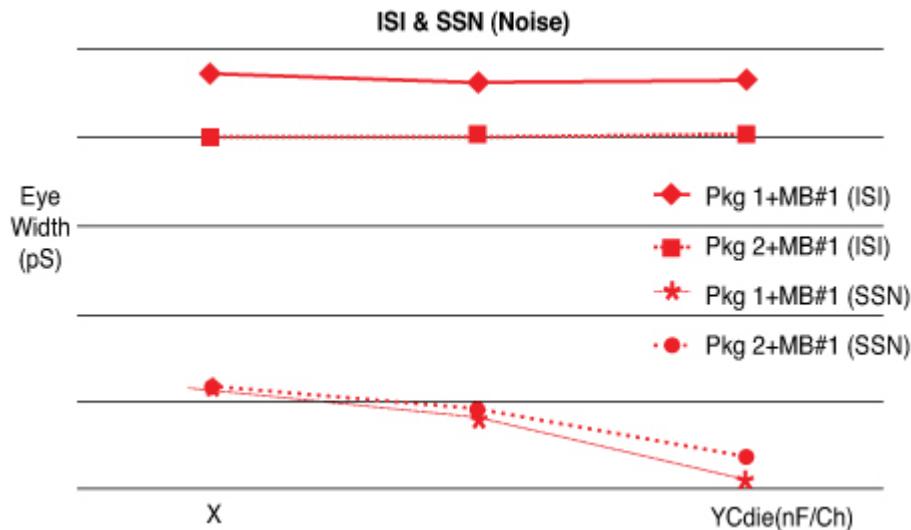


Figure 8.26 shows the result of the response decomposition of the system used in Figure 8.25. Figure 8.26 shows the inside story of why package #2 has superior performance. Even though the SSO stays similar for the system with two different packages, the ISI from package #1 is a lot bigger than the ISI with package #2. However, the ISI does not change much with the change of the on-chip capacitor value. Even though the SSO is smaller than the ISI, the SSO is effectively reduced with an increase of on-chip capacitor. It shows that the increased on-chip capacitor reduces the SSO further for package #1 than that for package #2. Looking back, the overall eye in Figure 8.25 again shows that using package #1 might be inferior to using package #2 at the XnF/Ch on-chip capacitor, but it can close the gap by increasing the capacitor to YnF/Ch . Figure 8.26 particularly shows the gap is closed because of the SSO reduction by increasing the chip capacitor. Therefore, the selection of components is dependent on the cost of the components and the on-chip capacitor values that can be achieved. For example, if package #2 is too expensive, the designer can go with package

#1 with an increased on-chip capacitor to Y_nF/Ch to match the performance. This decomposition shows the characteristics behind the overall channel performance and decision making based on the obtained data. Knowing the details of channel performance by investigating the noise contribution makes it easier to optimize the channel.

Figure 8.26. Noise profile after response decomposition

Source: M. J. Choi and V. Pandit, "SI/PI Co-analysis for I/O Interfaces," IBIS Summit, July 2009.



8.3.1.2. Simple Comparison of Eye

An example of an eye diagram for a typical high-speed DDR channel is shown in [Figure 8.27](#). The channel is comprised of seven coupled lines with PDN. The eye diagram with minimal SSO and minimal crosstalk is shown clearly with less degradation than the eye diagram with crosstalk and minimal SSO or the eye diagram with crosstalk and SSO. As crosstalk affects the channel, the receiver eye in [Figure 8.28](#) shows a 70mV reduction in the eye height and a 78pS reduction in the eye width compared to the eye diagram with minimal crosstalk and minimal SSO in [Figure 8.27](#). When other switching buffers are present nearby as shown in [Figure 8.29](#), the eye gets reduced further with 101mV and 79pS reduction in eye height and eye width. It clearly shows the impact of the crosstalk and SSO.

Figure 8.27. Eye measured with minimal SSO and minimal crosstalk. Eye height of 475mV and EW of 693pS

Source: M.J. Choi; V. Pandit, W.R. Ryu, "Controllable parameters identification for high speed channel through signal-power integrity combined analysis," Electronic Components and Technology Conference, May 2008, © [2008] IEEE.

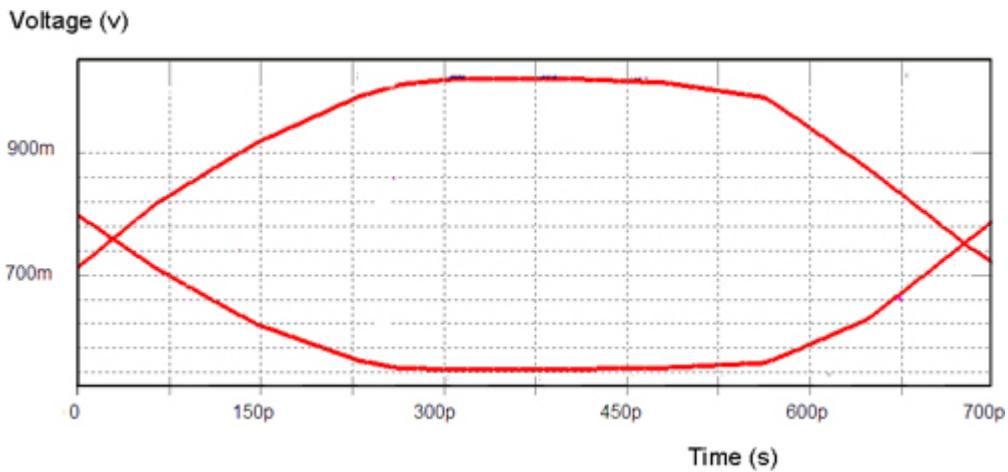


Figure 8.28. Eye measured with crosstalk and minimal SSO. Eye height of 405mV and eye width of 615pS.

Source: M. J. Choi; V. Pandit, W.R. Ryu, "Controllable parameters identification for high speed channel through signal-power integrity combined analysis," Electronic Components and Technology Conference, May 2008, © [2008] IEEE.

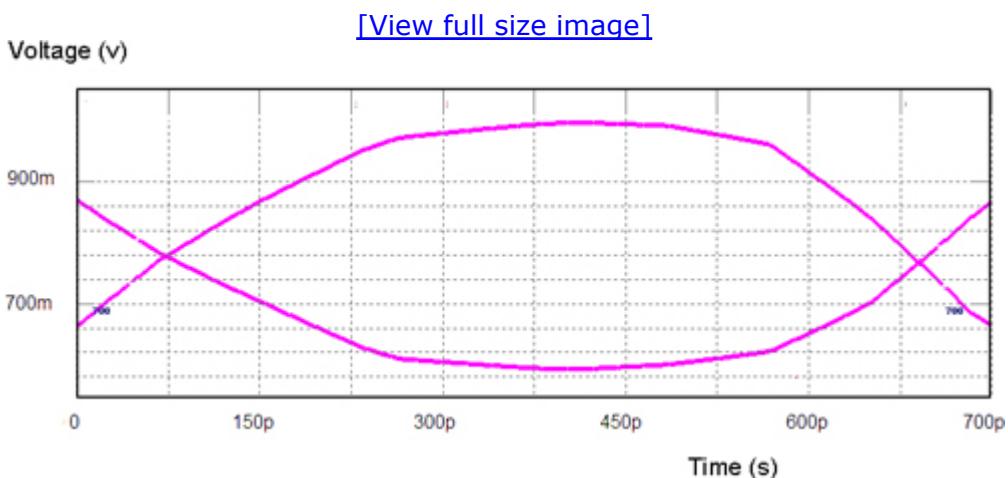


Figure 8.29. Eye with SSO and crosstalk. Eye height of 304mV and eye width of 536pS.

Source: M. J. Choi; V. Pandit, W.R. Ryu, "Controllable parameters identification for high speed channel through signal-power integrity combined analysis," Electronic Components and Technology Conference, May 2008, © [2008] IEEE.

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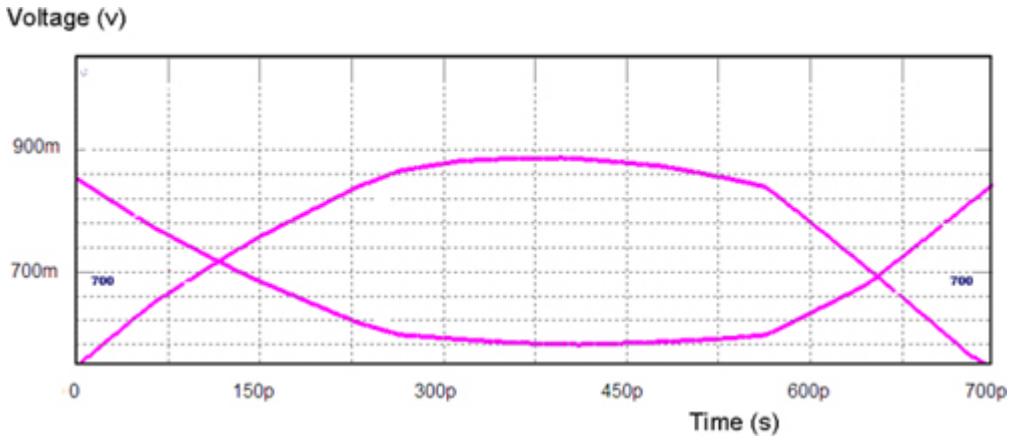


Figure 8.29 shows an example of the eye measurement at the receiver in a typical high-speed computer memory channel. The correlation process between the simulation and measurement for the response decomposition is difficult because of the measurement setup complexity and response decomposition difficulties in measurements. However, the eye with all crosstalk and SSO active as shown in Figure 8.29 can be directly compared with the measured eye.

Figure 8.30 shows an active system for the SI-PI correlation. Figure 8.31 shows a correlation of the lone bit simulation with the measurement. It shows a good agreement except for a dip in the simulated eye because of the different daughter card model in the simulation causing the dip. In general, a meticulous modeling of components leads to a good agreement between the simulation and the measurement. Figure 8.32 shows an example of the measured eye in the active system with a strobe signal as a triggering signal.

Figure 8.30. Active system for SI-PI correlation

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



Figure 8.31. Eye with SSO

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

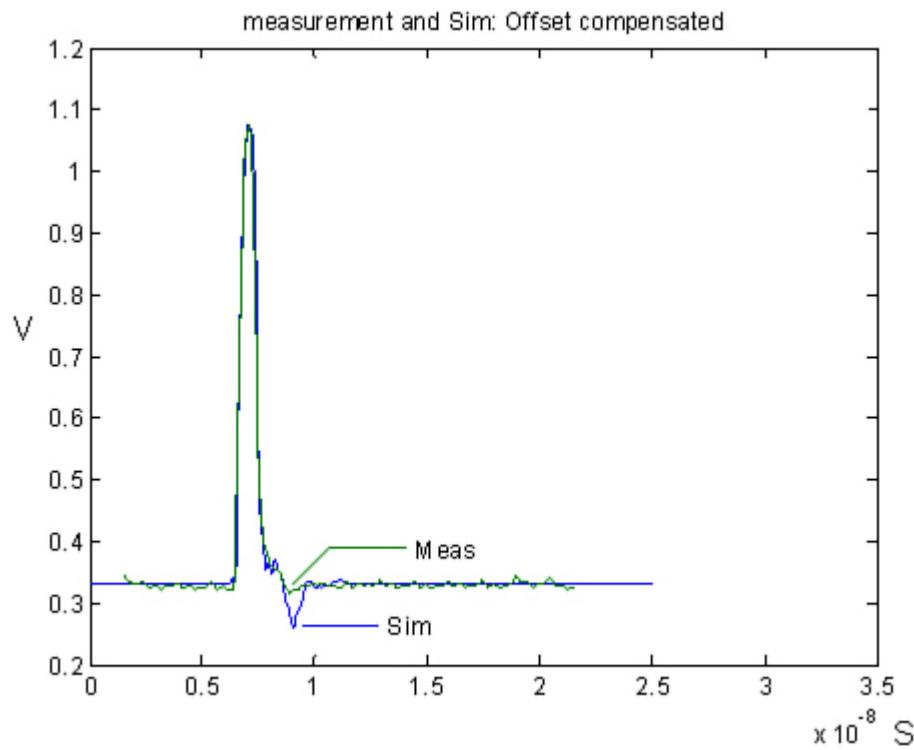
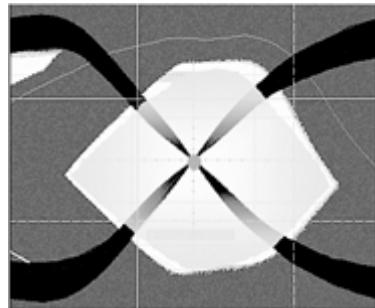


Figure 8.32. Example of measured eye with SSO and Xtalk

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.



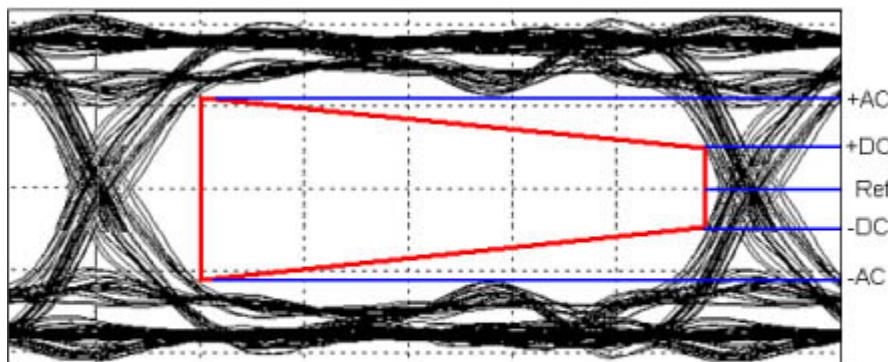
8.3.2. Eye Diagram Analysis

With SI-PI co-simulation and co-analysis the eye diagrams are obtained. In the previous sections, eye-height and eye-widths are calculated from the eye-diagrams. For some interfaces, the eye margins are calculated with respect to the “eye-mask,” which is a shape that defines the specification based on the interface and standard. Eye diagram calculation scheme for a typical high performance memory channel is shown in Figure 8.33. It is typical to use the isosceles trapezoid as the aperture type AC/DC calculation for the memory channel data lines. The isosceles trapezoid uses $\pm DC$ and $\pm AC$ levels as the first and the last crossing points, respectively. For the noise decomposition the width of the aperture, and the MH or the ML in Figure 8.33, can be used instead of the eye width and the eye height. In some systems it is more accurate to use the aperture width, the MH or the

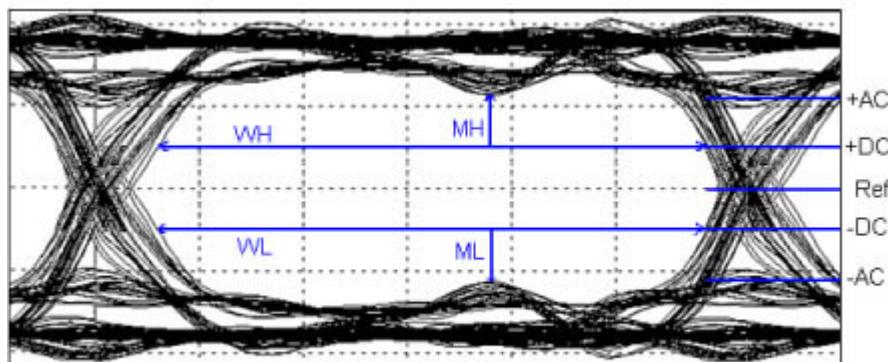
ML for eye analysis calculation because the drastic change in the eye shapes from one measurement to the other measurement makes the biggest eye opening calculation unreasonable. Different eye analysis schemes can be applied for the calculation of noise decomposition, but it is advised to keep the method rather consistent to obtain consistent time domain behavior trend.

Figure 8.33. Eye diagram measurement scheme example

Source: M. J. Choi and V. Pandit, "SI/PI Co-Analysis and Linearity Indicator," IBIS Summit, Feb. 2010.



(a) Aperture calculation using AC/DC specification



(b) Eye height calculation

8.3.3. Linear Interaction Indicator

The assumption that signal integrity and power integrity can be isolated into two separate problems and the design spec budget can be treated separately is effective only when the system in consideration is linear enough that the nonlinear impact can be discarded without costing any margin budget loss. However, the presence of simultaneously switching buffers and nonlinear buffer modulation impact due to the power node variations provides enough nonlinearity that cannot be considered minor in many systems. It becomes more critical when the system pushes for low-cost, low-power design. In this book, the Linear Interaction (LI) indicator is defined as the ratio of the sum of the isolated noises over all the noises

together; the first order considers the impact of each noise source when it is acting alone without other noises present, and the second order considers the impact of each noise source while other noises sources are active. Because ISI, crosstalk, and SSO are the three major categories of noises that are used to explain degradation in the eye, the LI indicator here is defined as the ratio of the sum of isolated ISI, isolated crosstalk, and isolated SSO over all the noises measured together.

There are different excitation conditions for the system, if a particular worst-case condition needs to be achieved. Following simulations are done to get the LI indicator of 1st order as the noise interactions are minimized. Here, the EH and EW can be replaced with equivalent measurements, such as MH or ML, and aperture width, as shown in [Figure 8.33](#).

- (1) Case #1 in [Table 8.2](#) without any patterns for crosstalk and SSO and with minimal ISI pattern as shown in [Figure 8.12](#), [Figure 8.13](#), and [Figure 8.14](#) generates an eye with minimal noises. The eye height and width are respectively defined as $EH_{Case\#1}$ and $EW_{Case\#1}$.
- (2) Case #2 in [Table 8.2](#) with the worst-case patterns for ISI generates worst-case eye for ISI. The SSO and crosstalk bits are turned off to minimize noise interactions. The difference in eye height and eye width from Case#1 in [Table 8.2](#) are respectively ΔEH_{ISI}^{1st} and ΔEW_{ISI}^{1st} .

Equation 8.1

$$\Delta EH_{ISI}^{1st} = EH_{Case\#1} - EH_{Case\#2}$$

Equation 8.2

$$\Delta EW_{ISI}^{1st} = EW_{Case\#1} - EW_{Case\#2}$$

- (3) Case #3 in [Table 8.2](#) with the worst-case patterns for SSO generates the worst-case eye for SSO. The minimal ISI pattern is used and crosstalk bits are turned off to minimize noise interactions. The difference in eye height and eye width from Case#1 in [Table 8.2](#) are respectively ΔEH_{SSO}^{1st} ΔEW_{SSO}^{1st} .

Equation 8.3

$$\Delta EH_{SSO}^{1st} = EH_{Case\#1} - EH_{Case\#3}$$

Equation 8.4

$$\Delta EW_{SSO}^{1st} = EW_{Case\#1} - EW_{Case\#3}$$

(4) Case #5 in [Table 8.2](#) with the worst-case patterns for crosstalk generates the worst-case eye for crosstalk. The SSO bits are turned off and minimal ISI pattern is used to minimize noise interactions. The difference in eye height and eye width from Case#1 in [Table 8.2](#) are respectively ΔEH_{Xtalk}^{1st} and ΔEW_{Xtalk}^{1st} .

Equation 8.5

$$\Delta EH_{Xtalk}^{1st} = EH_{Case\#1} - EH_{Case\#5}$$

Equation 8.6

$$\Delta EW_{Xtalk}^{1st} = EW_{Case\#1} - EW_{Case\#5}$$

Following simulations are done to get the LI indicator of the second order as the noise interactions are present in measuring each noise.

(5) Case #4 in [Table 8.2](#) with the worst-case patterns for ISI and SSO generates the worst-case eye for ISI and SSO. The difference in eye height and eye width from Case#8 that generates the worst-case eye with all noises acting together are respectively ΔEH_{Xtalk}^{2nd} and ΔEW_{Xtalk}^{2nd} .

Equation 8.7

$$\Delta EH_{Xtalk}^{2nd} = EH_{Case\#4} - EH_{Case\#8}$$

Equation 8.8

$$\Delta EW_{Xtalk}^{2nd} = EW_{Case\#4} - EW_{Case\#8}$$

(6) Case #6 in [Table 8.2](#) with the worst-case patterns for ISI and Crosstalk generates the worst-case eye for ISI and Crosstalk. The difference in eye height and eye width from Case#8 that generates the worst-case eye with all noises acting together are

respectively ΔEH_{SSO}^{2nd} and ΔEW_{SSO}^{2nd} .

Equation 8.9

$$\Delta EH_{SSO}^{2nd} = EH_{Case\#6} - EH_{Case\#8}$$

Equation 8.10

$$\Delta EW_{SSO}^{2nd} = EW_{Case\#6} - EW_{Case\#8}$$

(7) Case #7 in [Table 8.2](#) with the worst-case patterns for Crosstalk and SSO generates the worst-case eye for Crosstalk and SSO. The difference in eye height and eye width from Case#8 that generates the worst case eye with all noises acting together are respectively ΔEH_{ISI}^{2nd} and ΔEW_{ISI}^{2nd} .

Equation 8.11

$$\Delta EH_{ISI}^{2nd} = EH_{Case\#7} - EH_{Case\#8}$$

Equation 8.12

$$\Delta EW_{ISI}^{2nd} = EW_{Case\#7} - EW_{Case\#8}$$

(8) Case #8 in [Table 8.2](#) with the worst-case patterns for ISI, Crosstalk, and SSO generates the worst-case eye for all noises acting together. The degradation in eye height and eye width compared with case #1 is ΔEH_{11} and ΔEW_{11} .

Equation 8.13

$$\Delta EH_{All} = EH_{Case\#1} - EH_{Case\#8}$$

Equation 8.14

$$\Delta EW_{All} = EW_{Case\#1} - EW_{Case\#8}$$

The LI indicator for eye height and eye width of the 1st order are defined in equation [\(8.15\)](#) and [\(8.16\)](#).

Equation 8.15

$$L.I.I.{}_{EH}^{1st} = \frac{\Delta EH_{ISI}^{1st} + \Delta EH_{SSO}^{1st} + \Delta EH_{Xtalk}^{1st}}{\Delta EH_{All}}$$

Equation 8.16

$$L.I.I.{}_{EW}^{1st} = \frac{\Delta EW_{ISI}^{1st} + \Delta EW_{SSO}^{1st} + \Delta EW_{Xtalk}^{1st}}{\Delta EW_{All}}$$

The LI indicator for eye height and eye width of the 2nd order are defined in equation (8.17) and (8.18).

Equation 8.17

$$L.I.I.{}_{EH}^{2nd} = \frac{\Delta EH_{ISI}^{2nd} + \Delta EH_{SSO}^{2nd} + \Delta EH_{Xtalk}^{2nd}}{\Delta EH_{All}}$$

Equation 8.18

$$L.I.I.{}_{EW}^{2nd} = \frac{\Delta EW_{ISI}^{2nd} + \Delta EW_{SSO}^{2nd} + \Delta EW_{Xtalk}^{2nd}}{\Delta EW_{All}}$$

LI indicator usually has different values for eye height and eye width just as signal integrity analysis shows different worst-case corners for eye height and eye width. The difference between the 1st order LI indicator and 2nd order LI indicator shows how much noise interaction that boosts or reduces overall performance. If the channel is perfectly linear, the LI indicator must be 1. However, because of buffer modulation impact due to power variation, electromagnetic interactions, and the 2nd order or higher relationship between ISI, crosstalk, and SSO, each channel often shows an LI indicator of bigger or less than 1. The LI indicator less than 1 means that the noises measured all together have a bigger impact than each noise acting alone added together. It means that the noises interact together to boost their degrading impact. Therefore, the system noise tends to be underestimated if signal integrity and power integrity are analyzed separately because it misses noise interactions between signal integrity and power integrity causing bigger degradation. On the other hand, the LI indicator bigger than 1 means that each noise acting alone added together has a bigger impact than the noises measured all together. It means that the noises acting together reduce their overall impact. Therefore, the system noise tends to be overestimated if signal integrity and power integrity are analyzed separately because it misses the noise interactions between the signal integrity and power integrity causing less degradation.

The number of SSO buffers switching is varied by adding or removing the $I_{cc}(t)$. Figure 8.34 shows the impact of the number of buffers on eye height LI indicator. It is shown that as the number of buffers increase, the linearity decreases from 1. The value lower than one indicates that there is interaction between different elements, such as SSO and ISI or SSO and crosstalk. Similarly, the impact of number of buffers on eye width is evaluated. As in the previous case, the number of buffers is varied, and it is observed that the LI indicator for eye width reduces from 1. The eye width LI indicator is shown in Figure 8.35.

Figure 8.34. EH LI indicator of a typical channel calculated from SI-PI TD response breakdown

Source: M. J. Choi, V. S. Pandit, and W. H. Ryu, “Controllable parameters identification for high speed channel through signal-power integrity combined analysis,” Electronic Components and Technology Conference, 2008, pp 658-663; © [2008] IEEE.

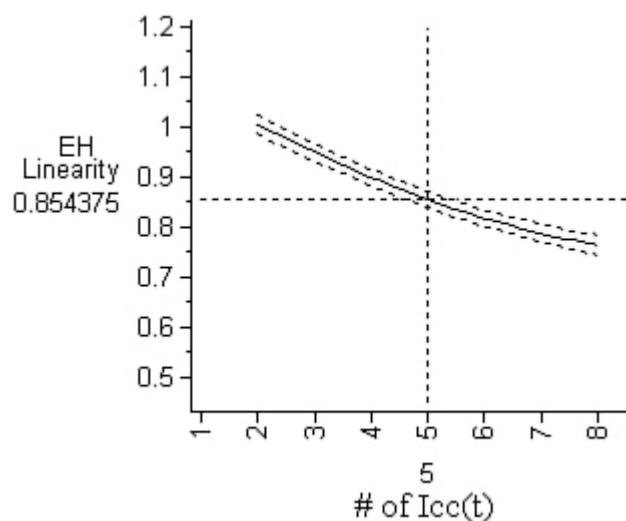
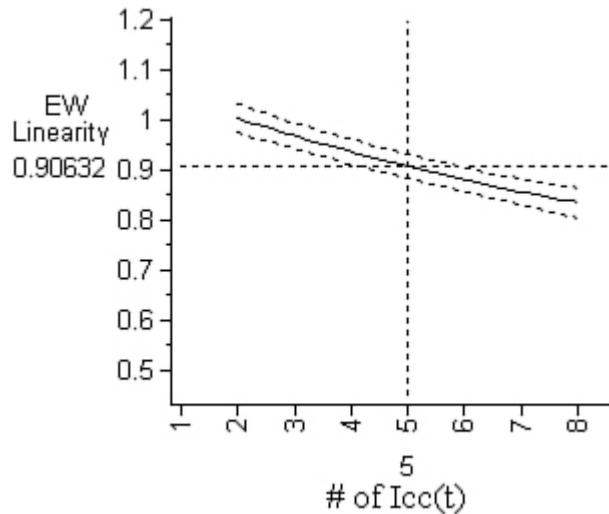


Figure 8.35. EW LI indicator of a typical channel calculated from SI-PI TD response breakdown

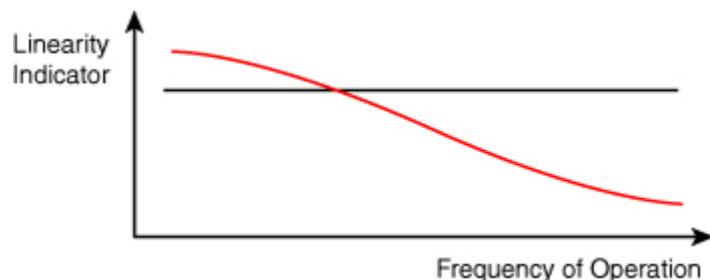
Source: M. J. Choi, V. S. Pandit, and W. H. Ryu, “Controllable parameters identification for high speed channel through signal-power integrity combined analysis,” Electronic Components and Technology Conference, 2008, pp 658-663; © [2008] IEEE.



The LI indicator less than one is due to the high order effects in the system. For a lower frequency of operation, the LI indicator may stay at 1; however, as the frequency of operation increases, the LI indicator goes down from 1, as shown in [Figure 8.36](#).

Figure 8.36. LI indicator versus frequency

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.



8.3.3.1. Single-Ended Signaling SI-PI Performance and Linearity

[Figure 8.37](#) shows a system response when the SI-PI co-simulation and co-analysis methodology applied to a single-ended signaling memory channel. Here, the SSO worst-case patterns are the same and in phase with the ISI bit worst-case patterns. Compared with the channel performance shown in [Figure 8.11](#), the response is slightly different because the host controller package uses dual-referenced strip lines whereas the system for [Figure 8.11](#) uses single-referenced microstrip lines in the host package. As per the aforementioned methodology, for [Figure 8.11](#) and [Figure 8.37](#), the measurement scheme for the aperture and the MH has been applied at the receiver’s victim bit line.

Figure 8.37. Eye diagram for time domain SI-PI co-simulation on

memory channel with data lines, strobe signals, and power delivery included signals for the system in Figure 8.9 except for the host package replaced with strip lined package

Source: M. J. Choi and V. Pandit, "SI/PI Co-Analysis and Linearity Indicator," IBIS Summit, Feb. 2010.

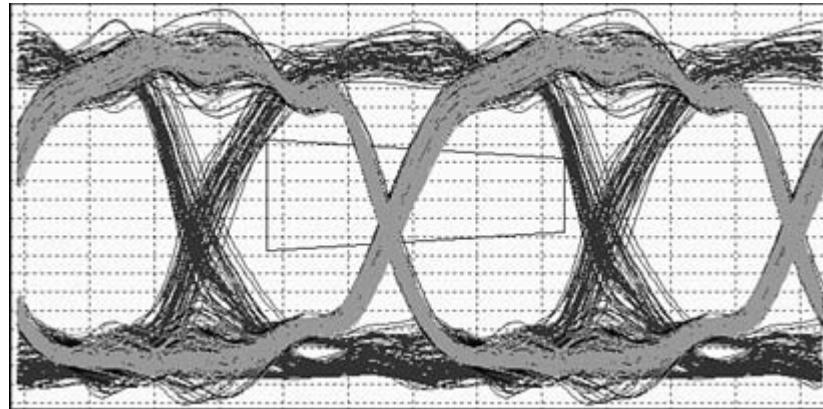


Figure 8.38 shows the noise breakdown result from applying the SI-PI co-simulation noise decomposition technique. In this particular channel, ISI is the biggest and the second biggest noise is SSO both in the 1st order and in 2nd order scenarios. The crosstalk is rated smaller than ISI or SSO. However, in general, the amount of a crosstalk can be bigger in a different system channel. Figure 8.39 shows the noise breakdown in the 2nd order noise decomposition. It is different from the 1st order, and in addition the crosstalk becomes negative, which means it widens the eye opening because of the in-phase interaction of the SSO and the crosstalk. Comparison of this crosstalk amount in Figure 8.38 and Figure 8.39 shows the amount of noises in the 1st order and 2nd order. The difference between the 1st order and the 2nd order indicates that there are certain amount of ISI, SSO, and crosstalk interactions that alter the amount of noises as the 1st order noise breakdown virtually has no interactions between noises. The change of amount of noises in the 2nd order noise breakdown in Figure 8.39 from Figure 8.38 indicates the interaction of noises needs to be considered with the co-analysis [8].

Figure 8.38. Single ended channel 1st order noise breakdown based on eye height from +DC level

Source: M. J. Choi and V. Pandit, "SI/PI Co-Analysis and Linearity Indicator," IBIS Summit, Feb. 2010.

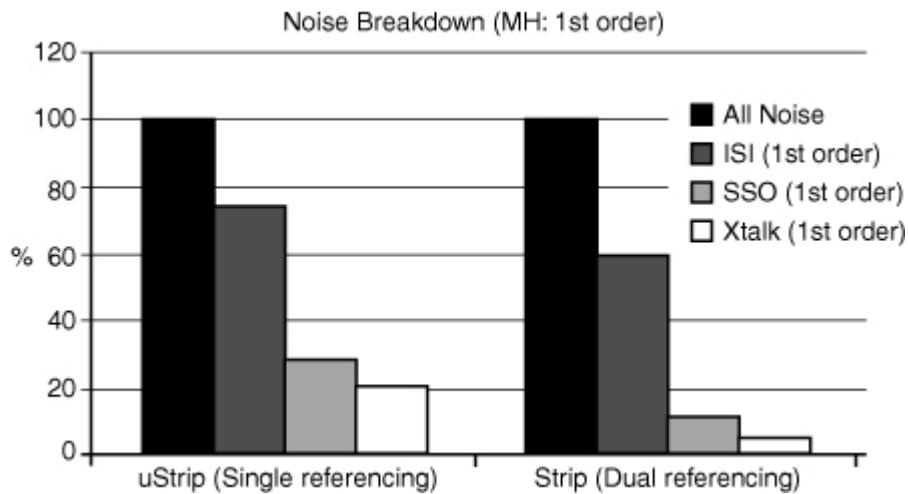
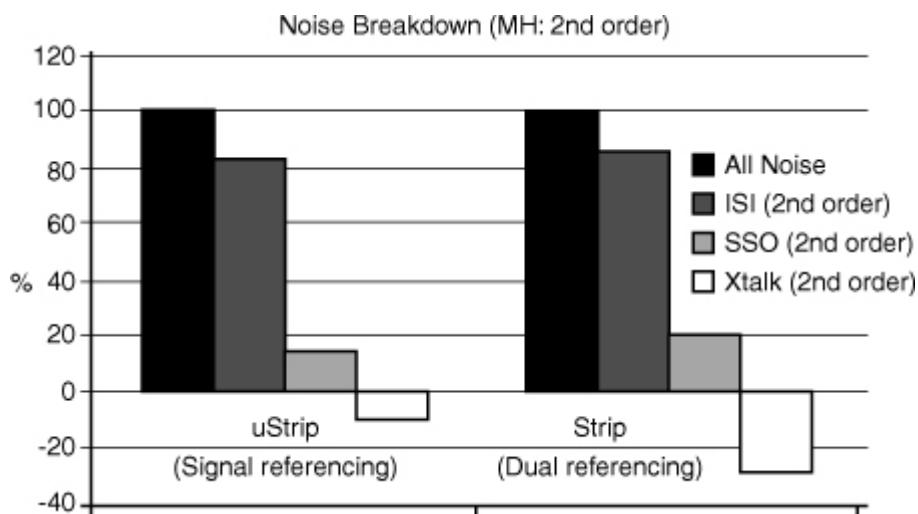


Figure 8.39. Single-ended channel 2nd order noise breakdown based on eye height from +DC level

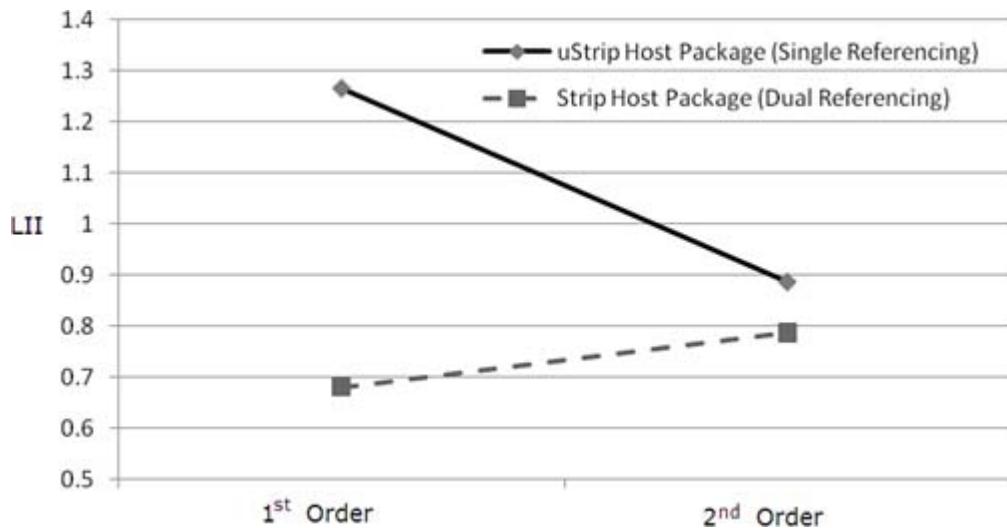
Source: M. J. Choi and V. Pandit, "SI/PI Co-Analysis and Linearity Indicator," IBIS Summit, Feb. 2010.



Investigation of the LI indicator in [Figure 8.40](#) for the systems for [Figure 8.11](#) and [Figure 8.37](#) shows the 2nd order LI is different from the 1st order LI, and it gets closer to 1. It indicates again that the interaction of noises is missing in the 1st order decomposition and clarifies that noises do interact with each other. Missing the interaction might not harm the performance margin of the end product if the margin were big enough to cover 10 to 20 percent of noise interaction shown in the 2nd order LI in [Figure 8.40](#). However, because it is hard to tell how much noise interaction is missed before running the SI-PI co-simulation, it is generally advised to run the SI-PI co-simulation in tight budget systems.

Figure 8.40. LI indicator for the systems for Figure 8.11 and Figure 8.37

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.



8.3.3.2. Differential Signaling SI-PI Performance and Linearity

SI-PI co-simulation and co-analysis methodology applied to a differential signaling channel with power delivery network shows eye response in Figure 8.41 [8]. As in the single-ended signaling example, the SSO worst-case patterns are the same and are in phase with ISI bit worst-case patterns. Compared with the channel performance for single-ended system, it shows a clearer eye, which depends on the particular system choices and designs. The system channel models for Figure 8.41 uses two differential pairs of signals and a few nearby buffers as simultaneous switching. With the aforementioned methodology applied to the system, the measurement scheme for the aperture and MH similar to Figure 8.33 has been applied at the receiver’s victim bit line for the purpose of noise decomposition.

Figure 8.41. An eye diagram at the receiver of SI-PI co-simulation for differential signaling

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.

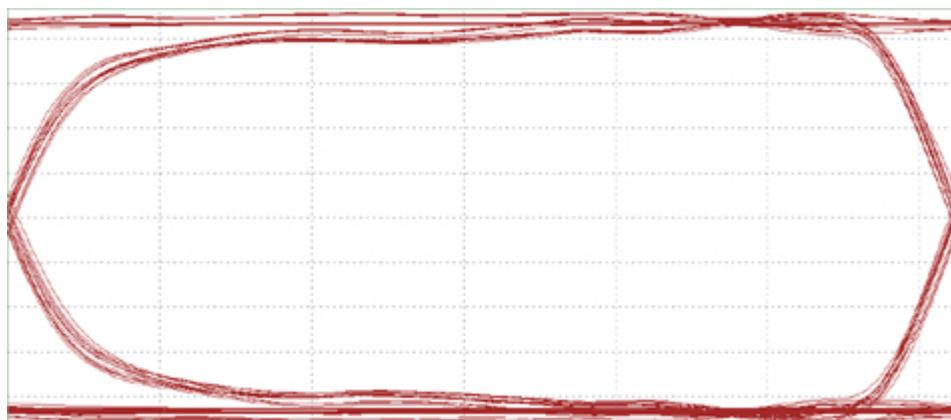


Figure 8.42 shows the 1st order noise breakdown result from applying the SI-PI co-simulation noise decomposition technique. In this particular channel, ISI is also the biggest as in the single-ended signaling example, and the second biggest noise is SSO both in the 1st order and in the 2nd order scenarios. Figure 8.43 shows the noise breakdown in the 2nd order noise decomposition. Similar to the single-ended signaling example, the 2nd order noises are different from the 1st order noises. A comparison of the noise ratio amount in Figure 8.42 and Figure 8.43 shows the interaction of noises and indicates certain amount of ISI, SSO, and crosstalk interactions alter the amount of overall noises.

Figure 8.42. Differential signaling channel 1st order noise breakdown based on eye height from +DC level

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.

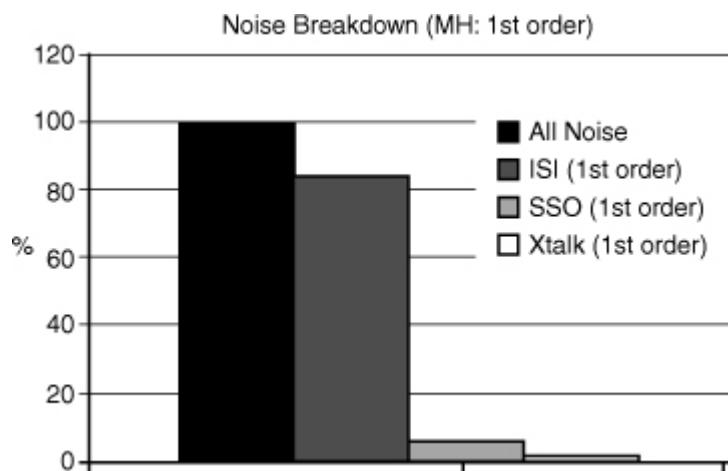
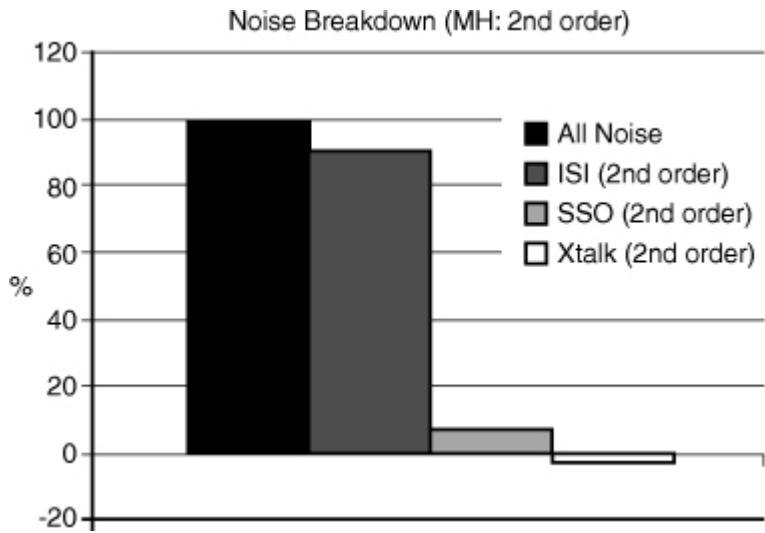


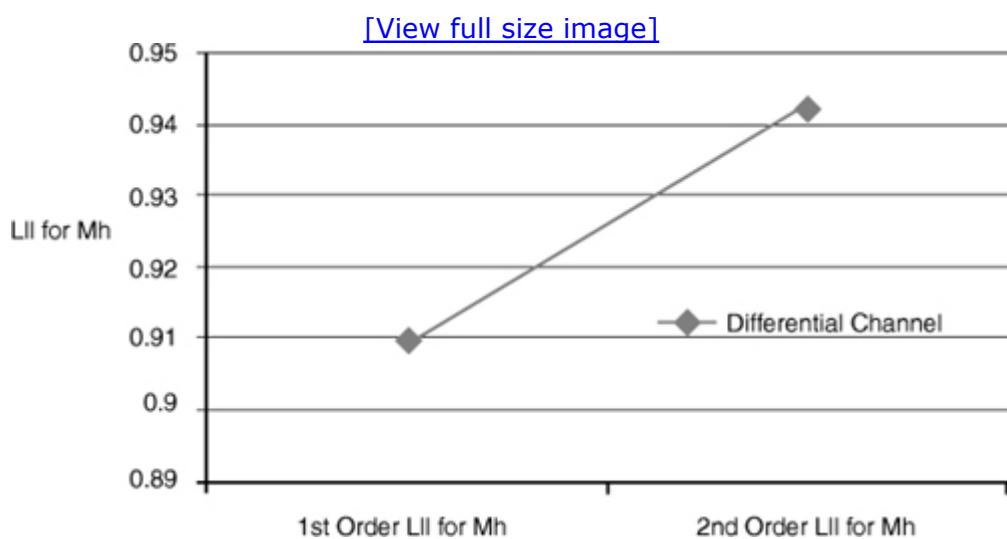
Figure 8.43. Differential signaling channel 2nd order noise breakdown based on eye height from +DC level

Source: M. J. Choi and V. Pandit, “SI/PI Co-Analysis and Linearity Indicator,” IBIS Summit, Feb. 2010.



The differential channel LI indicator in Figure 8.44 shows the first and 2nd order LI indicator is closer to 1 than those in the single-ended system [8]. Indeed, more linear behavior of differential channel can readily be expected for similar channel conditions because common mode rejection, tightly coupled lines, and differential buffers contribute to the less noisy environment and less interaction between noises for the differential channel. The differential 2nd order LI indicates that there are still some missing noise interactions, and noise might be underestimated if the channel would have analyzed signal integrity-only or power integrity-only methodologies. Missing the interaction might not harm the performance margin of the end product if the margin were big enough to cover about 6 percent of the noise interaction shown in the 2nd order LI in Figure 8.44. Particularly for the differential signaling channel, the less headroom might be needed than for the single-ended signaling channel.

Figure 8.44. LI indicator for the systems for Figure 8.41



8.3.3.3. SI-PI Linear Interaction Indicator

In the earlier sections, the L.I. indicator has been discussed and its characteristics are stated. The L.I. indicator is the ratio of summation of eye degradation due to individual ISI, crosstalk, and SSO to the eye degradation when the combined effects of ISI, crosstalk, and SSO are considered. In the previous sections signal integrity-only analysis indicated the separate analysis for ISI, separate analysis for crosstalk; and power integrity-only analysis indicated that separate analysis for the SSO.

Consider that the designer performs the signal integrity-only analysis with ISI and crosstalk together, but without the SSO. The power integrity-only analysis is done with the SSO only. Equation (8.19) is a direct indicator for the difference between the SI-PI noise and power integrity-only noise added to the signal integrity-only noise.

Equation 8.19

"SI – PI" Linear Interaction Indicator

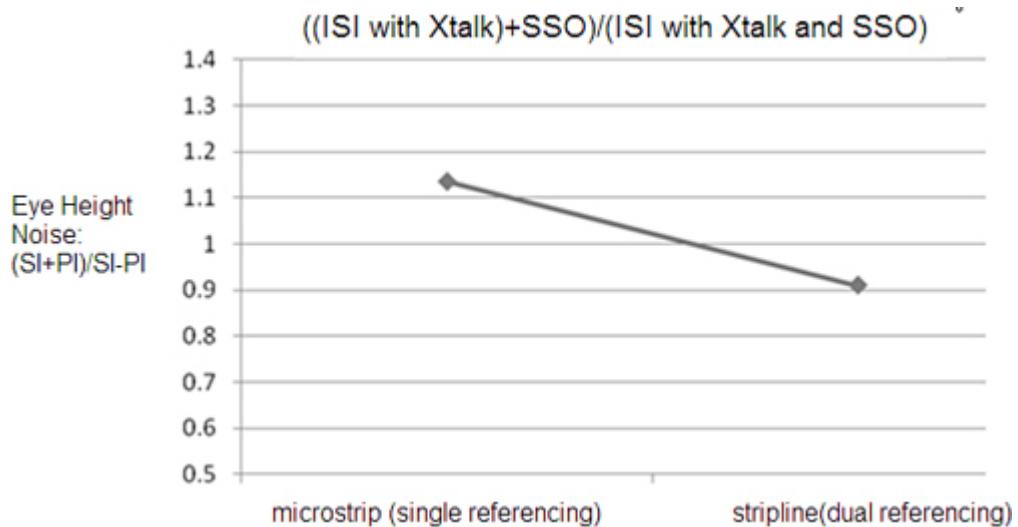
$$= \frac{\text{Signal Integrity Noise} + \text{Power Integrity Noise}}{\text{SI – PI Noise}}$$

$$\approx \frac{(EH_{\text{Case}\#1} - EH_{\text{Case}\#6}) - (EH_{\text{Case}\#1} - EH_{\text{Case}\#3})}{(EH_{\text{Case}\#1} - EH_{\text{Case}\#8})}$$

If it is less than 1, the noise measured all together in the SI-PI simulation has a bigger impact than power integrity noise acting alone added to the signal integrity noise acting alone. Therefore separate analysis of the signal and power integrity gets to underestimate the noise impact. If it is bigger than 1, separate analysis of the signal and power integrity gets to overestimate the noise impact. Figure 8.45 is the indicator plot for the eye height for the single ended system for Figure 8.11 and Figure 8.37. The channel with the microstrip line host package and the strip-line host package both are somewhat higher and lower than 1, respectively. It means that SI-PI co-simulation captures missing information if the channel was analyzed separately for signal integrity and power integrity. A similar approach can be used for eye width analysis.

Figure 8.45. Sum of signal integrity-only noise plus power integrity-only noise versus SI-PI noise

Source: M. J. Choi and V. Pandit, "SI/PI Co-Analysis and Linearity Indicator," IBIS Summit, Feb. 2010.



If equation (8.19) is applied to the differential channel, discussed in Figure 8.41, to indicate the gap between SI-PI noise and power integrity-only noise budget added to the signal integrity-only noise budget, the value is 0.99 for the particular system, which means that the SI-PI co-simulation might not be needed for the system because there is little noise interaction. In general, many well-designed differential channels do not require SI-PI co-simulation as they are quite linear in their noise interaction behavior. However, because the behavior depends on the particular channel design and LI indicator is not known until running the SI-PI co-simulation, it is always good practice to check the SI-PI performance at least once at a certain stage of product design to assess noise interactions.

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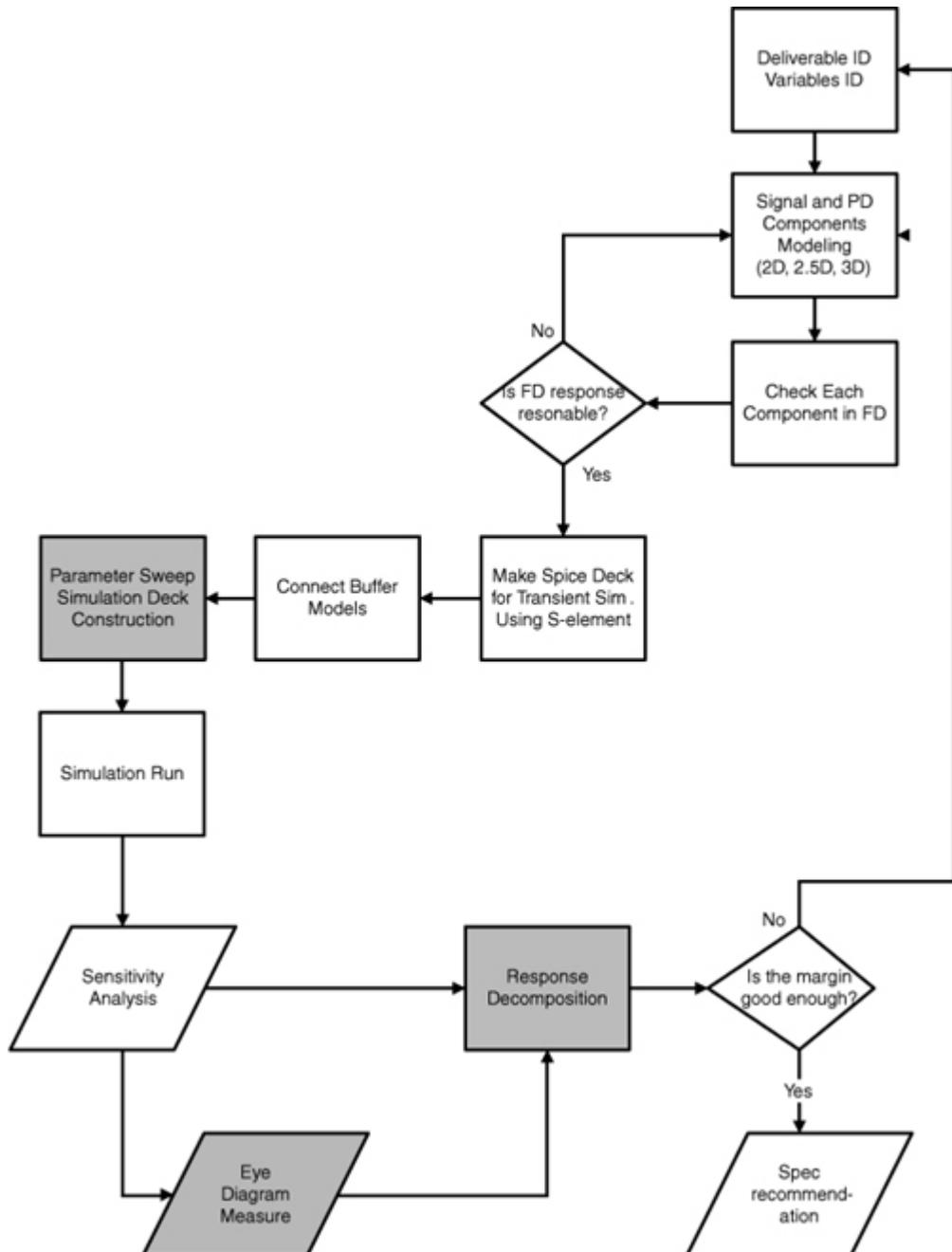
8.4. SI-PI Co-Simulation and Co-Analysis Flow: Summary

In summary, SI-PI co-simulation follows the flow described in [Figure 8.46](#). Variations in the flow can lead to more efficient but less accurate or less efficient but more accurate SI-PI co-simulation and co-analysis. The flow starts with identifying variables that might affect the system response. It is important to pre-screen simulation variables to select variables with the most sensitivity so that the optimization can be impacted significantly. Modeling of the components should include electromagnetic interactions between the signal and power because capturing interactions is the whole point of running SI-PI co-simulations. The models generated should be checked for passivity and causality to expedite smooth time domain simulation. Generating different cases of simulations can utilize Design of Experiment (DOE) commonly used in a statistical experiment or other optimization algorithms. In the end, the response decomposition helps identify noise contribution to the system, which helps further optimize and understand the system under design.

Figure 8.46. SI-PI co-simulation and co-analysis flow

Source: M. J. Choi and V. Pandit, “SI/PI Co-analysis for I/O Interfaces,” IBIS Summit, July 2009.

[\[View full size image\]](#)



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Chapter 9. Measurement Techniques

This chapter addresses frequency domain and time domain measurement techniques for power integrity and signal integrity. The measurement of S-parameters constitutes a vital component of power/signal integrity design verification for high-speed I/O interfaces. Typically, S-parameters are measured with a Vector Network Analyzer (VNA) that calculates input/output reflections and transmission by sequentially applying signals at various frequencies and recording the response of the Device Under Test (DUT). The resulting data depicts a set of measured values as a function of frequency. On the other hand, an oscilloscope, a measurement instrument used for Power Delivery Network (PDN) noise measurements and signal jitter measurements, enables voltages to be viewed in time domain. Time-Domain Reflectometry (TDR) represents a measurement technique to characterize interconnection lines by observing the reflected waveforms. Time-Domain Transmissometry (TDT) describes an analogous technique that measures the transmitted waveforms.

9.1. Frequency Domain Characterization

With a data rate of a few hundred MHz or more, the demand on an accurate broadband SPICE model and frequency-dependent transmission parameters including impedance, loss, phase velocity, distributed RLCG, mutual Lm, and mutual Cm, increases for the accurate prediction and design of signal/power integrity on chip/package/board. This section describes an accurate and efficient procedure to obtain the signal/power integrity model parameters based on VNA measurements, subsequent microwave network analysis, and equivalent circuit optimization.

9.1.1. Vector Network Analyzer (VNA)

With the push toward higher speed signaling and the need for more accurate characterization and modeling of interconnects such as cables, connectors, and printed circuit boards, the VNA is common in signal/power integrity labs [1]. In comparison with time domain (TD) measurement, the VNA brings more accuracy, dynamic range, and frequency coverage to this characterization and modeling. Even though signal integrity engineers are

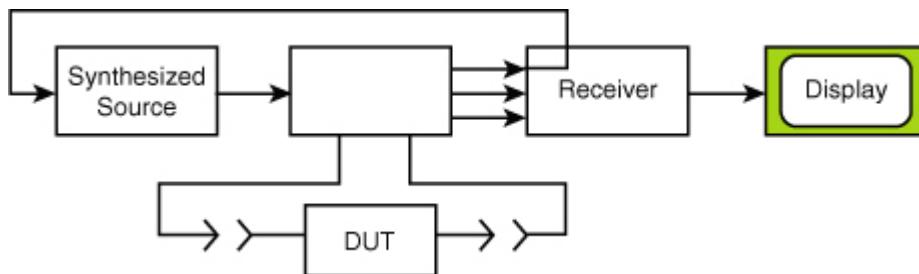
more familiar with time domain oscilloscope measurements, frequency domain VNA characterization is becoming more significant, especially at higher speeds. Depending upon the data rates and complexity of the structure, measurements and modeling can be conducted in either the frequency domain, using a VNA, or in the time domain, using a time domain reflectometer. To obtain high-quality measurements, an user needs an understanding of the instruments' architecture, calibration, and specifications such as dynamic range, accuracy, noise, and stability [1]. Several available calibration techniques permit the user to remove sources of error in making measurements.

The TDR has a broadband receiver with the choice of 12 or 18GHz 3dB bandwidths. The VNA has a selectable Intermediate Frequency (IF) bandwidth. The bandwidth can be set from 1Hz to 30KHz. This narrow bandwidth significantly reduces the noise floor, to better than -110dBm. Due to the wide band receiver of the TDR, the noise floor is higher, limiting the TDR's dynamic range to about 40dB, compared to the VNA's dynamic range of 100dB. When also considering the source power roll-off at the higher frequencies of the TDR, the TDR signal-to-noise ratio above 10GHz noticeably decreases.

As [Figure 9.1](#) shows, the VNA consists of the following components:

- **Source:** Sine wave (CW) and sweep
- **Signal Separation Device:** Power splitter, transfer switch, and directional coupler
- **Receiver:** Double conversion and three samplers
- **Display:** Error correction, trace math, formatting, scaling, marker operation, and so on

Figure 9.1. Vector Network Analyzer



[Chapter 5](#), "Frequency Domain Analysis," shows several correlation plots with the VNA measurements, both for signal and power networks. Typically for the signal and power networks, S parameters are measured and can be converted to Z-parameters. [Chapter 5](#) portrays examples of frequency domain insertion loss, voltage transfer function, and crosstalk. Self

impedance Z_{11} constitutes the major design criterion for the PDN. Later sections describe the special techniques used to measure low impedance Z_{11} .

9.1.2. Smith Chart

This section describes the Smith chart's construction and background, and summarizes practical techniques for using the chart in signal/power integrity areas. In [Chapter 7](#), "Signal/Power Integrity Interactions," we examined a way to identify any resonant structures at frequencies of noise. Root causing for a channel resonance issue, however, does not depict the only use for the Smith chart. The chart can also help signal/power integrity engineers with tasks such as optimizing for the best signal quality, resonance mitigation, noise figures, and quality factor analysis.

The Smith chart, used to draw impedance and admittance in the reflection coefficient plane, presents information such as reflection coefficient (Γ) and simultaneously provides insight to calculate impedance. The amount of reflected signal from the load depends on the degree of mismatch between the source impedance and the load impedance (Z). The following equation portrays one way to define the expression:

Equation 9.1

$$\Gamma = \frac{\bar{Z} - 1}{\bar{Z} + 1} = \Gamma_r + j\Gamma_i$$

where Γ_r , and Γ_i are real and imaginary of the reflection coefficient respectively, and the ratio of the load impedance to characteristic impedance (Z_0) is defined as $\bar{Z} = \frac{Z}{Z_0}$.

If we indicate Z as constant r circle and constant x circle in Γ plane:

Equation 9.2

$$\bar{Z} = \frac{1 + \Gamma}{1 - \Gamma} = r + jx$$

From (9.1) and (9.2)

Equation 9.3

$$r = \frac{1 - \Gamma_r^2 + \Gamma_i^2}{(1 + \Gamma_r)^2 + \Gamma_i^2}$$

Equation 9.4

$$x = \frac{2\Gamma_i^2}{(1 - \Gamma_r)^2 + \Gamma_i^2}$$

Using equations (9.3) and (9.4), we can derive the following equations (9.5) and (9.6) of a circle in Cartesian coordinates.

Equation 9.5

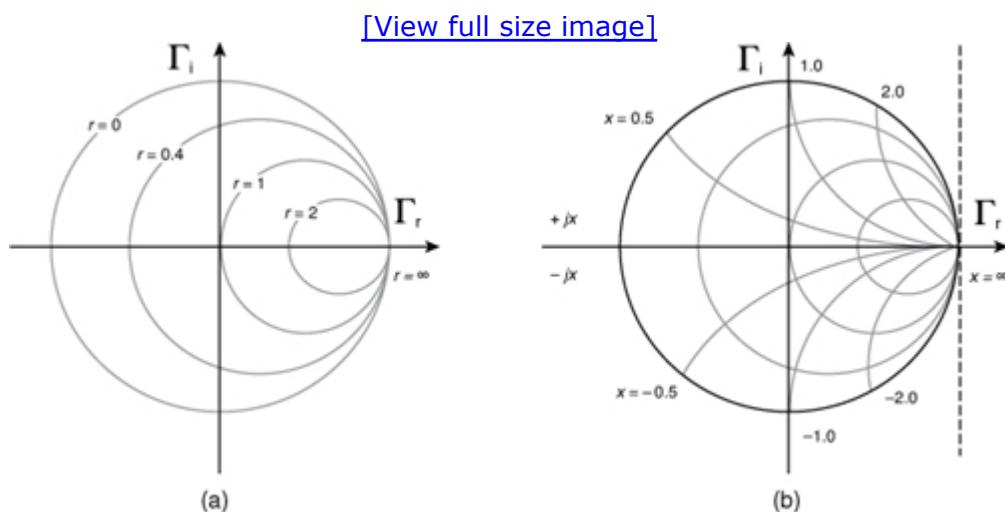
$$\left(\Gamma_r - \frac{r}{1+r}\right)^2 + \Gamma_i^2 = \left(\frac{1}{1+r}\right)^2$$

Equation 9.6

$$(\Gamma_r - 1)^2 + \left(\Gamma_i - \frac{1}{x}\right)^2 = \left(\frac{1}{x}\right)^2$$

In Figure 9.2 (a), the constant resistance circles show all the impedances characterized by a same, real impedance part value. For example, the circle, $r = 1$, centered at the coordinates $(0.5, 0)$, has a radius of 0.5. A short circuit, as a load, presents a circle centered at the coordinate $(0, 0)$ and has a radius of 1. For an open-circuit load, the circle degenerates to a single point (centered at $1, 0$ and with a radius of 0). This corresponds to a maximum reflection coefficient of 1; the point which totally reflects the entire incident.

Figure 9.2. (a) Constant resistance r-circle; (b) Constant reactance x-circle in reflection coefficient (Γ) plane



[Figure 9.2 \(b\)](#) shows the constant reactance circles, which depict all the impedances characterized by a same imaginary impedance part value x . For example, the circle $x = 1$, centered at coordinate $(1, 1)$, has a radius of 1. All circles (constant x) include the point $(1, 0)$. Differing with the real part circles, x can be positive or negative. This explains the duplicate mirrored circles at the bottom side of the complex plane. All the circle centers are placed on the vertical axis, intersecting the point 1.

9.1.3. Low-Impedance VNA Measurement for Power Delivery Network

First published at DesignCon in 1999, Novak's two-port VNA methodology provided a feasible and accurate approach for characterizing the low-impedance power delivery networks (PDN) [2]. Although this method reveals significant advantages over the simple one-port measurement, it still possessed some limitations for accuracy, mainly due to the impacts of the parasitics and discontinuities coming from the mutual inductance of probes and the inductances of power and ground vias. To minimize residual coupling through the probe-pin loops' various compensation methods have been tested and introduced [3]. By constructing a series of equivalent circuits, this section analyzes the impact of the parasitic and then develops some improvements involving probe and port arrangements, which significantly enhances the accuracy of the original Novak's two-port methodology. Both the measurements and circuit and 3-D simulations illustrated in this section validate the effectiveness of the improvements.

As processor cycle times become faster from generation to generation, the cycle time of the whole computer system, including chipset, memory chips, graphic cards and so forth, must keep pace. This continuing trend requires not only faster bus I/O circuits but also more rapid interconnect technologies. In the meantime, an ever-expanding mobile market demands the system consumes low power, which can be realized normally through lowering the system power's voltage level. For example, memory technology DDR2's voltage level measures 1.8V, whereas DDR3 is reduced to 1.5V. We expect that for the future generation of memory as DDR4, the voltage level will be reduced further to 1.2V. Similarly, the serial I/O interfaces are also being designed for low voltage levels. To meet the challenges, both these two trends require PDNs in multilayer Printed Circuit Boards (PCB) and that multilayer packages target for low impedance.

At present, abundant numerical simulation tools exist in the market, capable of simulating the characteristics of the low-impedance PDNs with sound speed and accuracy [1, 5]. However, verification by measurement lags behind, as the traditional one-port VNA method reflects severe inherent limitations for the low-impedance measurement. First, when the DUT's impedance is low, the reflection is high, whereas the accuracy of VNA is compromised at this high reflection. Second, connecting parasitics, such as

probe impedance, are in series with DUT.

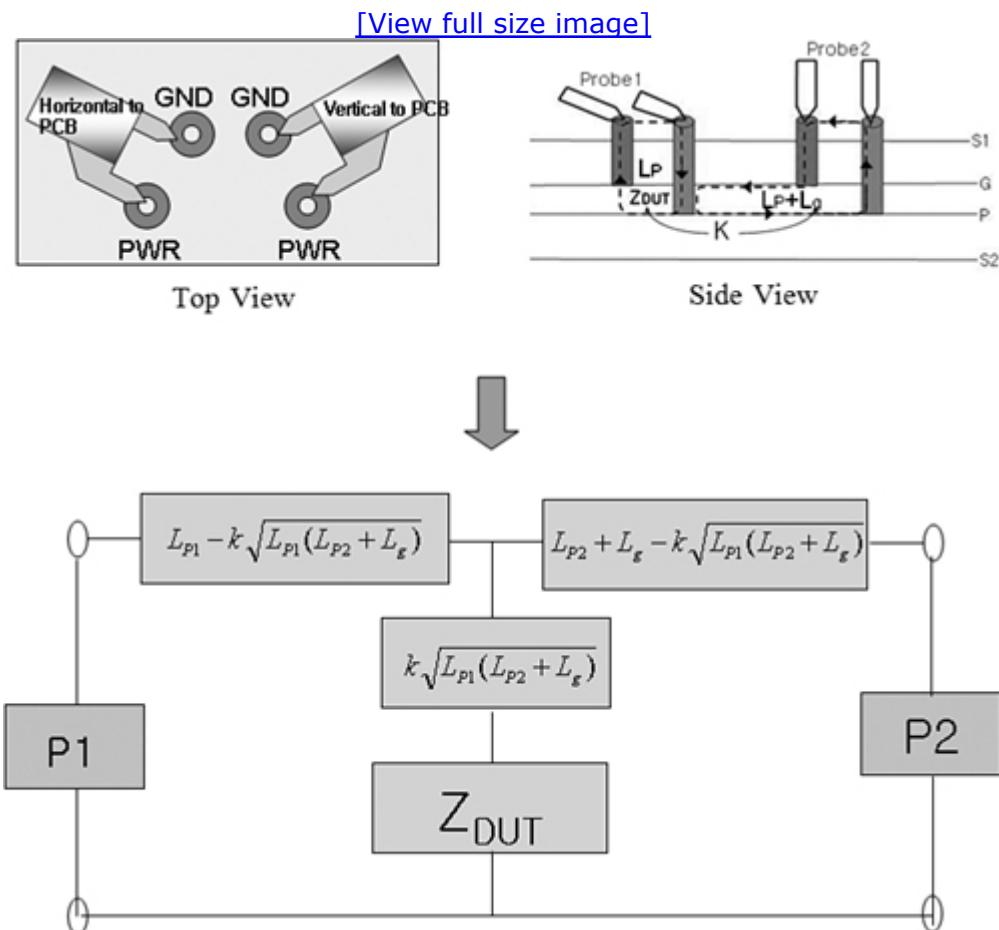
Equation 9.7

$$Z_{DUT} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} - Z_{v1}$$

Equation (9.7) illustrates the relation between the impedance of the DUT, VNA measurement result S_{11} , and probe discontinuity Z_{v1} . From equation (9.7), the user can easily understand that both these limitations work together to make it impossible for the one-port method to measure accurately impedances in the hundreds of milliohm range or lower.

In 1999, Novak [2] presented a novel two-port VNA methodology for measuring the low impedance of PDNs in his DesignCon paper. Figure 9.3 illustrates the measurement setup and the associated equivalent circuit.

Figure 9.3. Novak's two-port VNA methodology



Given the probe's parasitic impedances Z_{v1} and Z_{v2} , the two-port linear network can be characterized by a Z matrix:

Equation 9.8

$$S_{21} = \frac{2Z_{21}}{Z_0 + Z_{11} + Z_{22}} = \frac{2Z_{DUT}}{Z_0 + 2Z_V + 2Z_{DUT}}$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_{DUT} + Z_{V1} & Z_{DUT} \\ Z_{DUT} & Z_{DUT} + Z_{V2} \end{bmatrix}$$

If $Z_{V1} = Z_{V2} = Z_V$, equation (2) can be rewritten as

Equation 9.9

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_{DUT} + Z_V & Z_{DUT} \\ Z_{DUT} & Z_{DUT} + Z_V \end{bmatrix}$$

S_{21} can be derived from the Z matrix as

Equation 9.10

$$S_{21} = \frac{2Z_{21}Z_0}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} = \frac{2Z_{21}Z_0}{Z_0(Z_0 + Z_{11} + Z_{22}) + Z_{11}Z_{22} - Z_{12}Z_{21}}$$

Compared to Z_0 's 50 ohm, the item $Z_{11}Z_{22} - Z_{12}Z_{21}$ is negligible. Thus, the equation (9.10) can be reduced to

Equation 9.11

$$S_{21} = \frac{2Z_{21}}{Z_0 + Z_{11} + Z_{22}} = \frac{2Z_{DUT}}{Z_0 + 2Z_V + 2Z_{DUT}}$$

Finally,

Equation 9.12

$$Z_{DUT} = \frac{\left(Z_V + \frac{Z_0}{2}\right) \cdot S_{21}}{1 - S_{21}} \approx \frac{25S_{21}}{1 - S_{21}}$$

Equation (9.12) sheds light on the pros of the two-port VNA method. First, for the low impedance measurement, the uncertainty of S_{21} is much less than that of S_{11} . Second, the connecting discontinuities are now in series with the 50 ohm VNA reference impedance. Therefore, their impacts on the final measurement result are removed.

Compared with the simple one-port method, although the two-port VNA approach enhances measurement accuracy greatly, it may possess a number of potential limitations needing to be addressed and overcome.

The impact of the mutual inductance of the two probes causes the first limitation. With the two probes now at the same or proximate location, the impedance brought by the mutual inductance must be considered. Given the mutual inductance M , using a circuit conversion that decouples the mutual inductance from the two inductances, and following the similar steps as from equation (9.9) to equation (9.12), the mutual inductance's impact on Z_{DUT} can be written as

Equation 9.13

$$S_{21} = \frac{2Z_{21}}{Z_0 + Z_{11} + Z_{22}} = \frac{2(Z_{DUT} + j\omega M)}{Z_0 + 2Z_V + 2Z_{DUT} - 2j\omega M}$$

Equation 9.14

$$Z_{DUT} = \frac{\left(Z_V - j\omega M + \frac{Z_0}{2}\right) \cdot S_{21}}{1 - S_{21}} - j\omega M \approx \frac{25S_{21}}{1 - S_{21}} - j\omega M$$

From equation (9.14), it is evident the mutual inductance of the probes after the conversion is actually in series with Z_{DUT} . As Z_{DUT} is of low impedance, to some extent, the mutual inductance will affect the accuracy negatively. Equation (9.14) also reveals that to lower the impact of the mutual inductance, the only most effective approach is rearranging the orientation and the distance of the two probes so that the coupling of the two probes can be lowered. [Figure 9.3](#) illustrates the newly designed probe and port setup. For the purpose of mutual inductance reduction, the probes are set at 90 degrees to each other. Meanwhile, because the distance will also help in reducing the mutual inductance further, the two ports are arranged with separated power/ground pairs. When the probes are placed at the same power/ground pair and in parallel with each other, the mutual inductance approximately ranges from 5pH to 50pH.

The second limitation evolves from the impact of the power/ground vias. In multilayer printed circuit boards, power and ground planes are commonly buried inside of dielectric layers. Therefore, to access the power/ground plane pairs, a pair of power/ground vias must be used to connect the probe tips with DUT. The task of de-embedding or even reducing the power/ground vias impact is nontrivial. One popular idea in the signal integrity world is to treat the power/ground-via pair separately as one power via and one ground via. This method makes the problem unnecessarily cumbersome and simultaneously deviates from the

inductance's physical nature, as the inductance has physical meaning only if a loop is formed. Therefore, loop inductance concept is applied here to handle the power/ground-via pairs.

As Figure 9.3's side view portrays, we assume the loop inductance of the power/ground via pair associated with port1 is L_{P1} , and that associated with port2 is $L_{P2} + L_g$, where L_{P2} corresponds to the loop area of the power/ground via pair at port2, and L_g is the equivalent inductance mainly contributed by the narrow loop from probe2 to probe1 between the power/ground planes. In addition, it is reasonable to assume K is the mutual coefficient of the two loop inductances and L_{P1} is equivalent to L_{P2} ; therefore, they are represented as L_p . Similar to equations (9.13) and (9.14), Z_{DUT} can then be written as

Equation 9.15

$$S_{21} = \frac{2Z_{21}}{Z_0 + Z_{11} + Z_{22}} = \frac{2(Z_{DUT} + j\omega k \sqrt{L_p(L_p + L_g)})}{Z_0 + 2Z_{DUT} + 2j\omega(L_p + \frac{L_g}{2}) - k\sqrt{L_p(L_p + L_g)}}$$

Equation 9.16

$$Z_{DUT} = \frac{\left(j\omega(L_p + \frac{L_g}{2}) - k\sqrt{L_p(L_p + L_g)} + \frac{Z_0}{2} \right) \cdot S_{21}}{1 - S_{21}} - j\omega k \sqrt{L_p(L_p + L_g)}$$

$$\approx \frac{25S_{21}}{1 - S_{21}} - j\omega k \sqrt{L_p(L_p + L_g)} \quad \text{if } j\omega(L_p + \frac{L_g}{2}) - k\sqrt{L_p(L_p + L_g)} \ll \frac{Z_0}{2}$$

Equation (9.16) explains the impact of the power/ground vias on Z_{DUT} . For the two-port VNA methodology, the component in series with Z_{DUT} actually comprises the mutual inductance of the two loops, rather than the loop inductances themselves. Equation (9.16) also shows that by minimizing K , L_p or L_g , the power/ground via impact could be reduced. Among these three parameters, K depicts the one with the strongest sensitivity that needs to be minimized as much as possible, whereas L_g 's impact proves insignificant as it is in the square root. It is to be noted that the original two-port method Novak introduced is the special case that can also be explained by equation (9.16). With the two ports at the same location, the two loops overlap with each other, which leads to $K=1$ and $L_g=0$. Equation (9.16), then simplified as

Equation 9.17

$$Z_{DUT} \approx \frac{25S_{21}}{1-S_{21}} - j\omega L_p$$

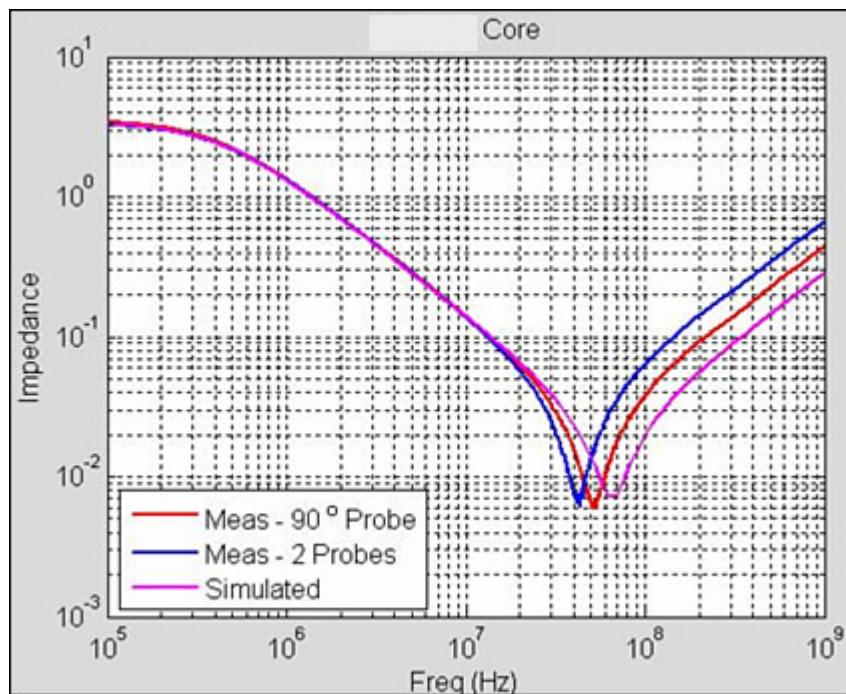
Thus, the original two-port VNA port setup introduces the error. Based on equation (9.16), we suggest two-port arrangement schemes in Figure 9.3 for the purpose of power/ground via impact reduction. The two ports could either be placed on the same side of a PCB with the loops in 90 degrees, or they could be placed on the reverse side of the PCB for a better purpose of decoupling. In summary, to lower the power/ground via impact, three steps can be adopted: First, make the power and ground vias of each port as close as possible so that the loop inductance Z_p is minimized. Second, arrange the two pairs in 90 degrees or at the reverse side of the PCB to reduce the mutual inductance. Third, keep the distance of the two pairs smaller than 500 um; that is, the least L_g is better. If L_g is too large, then

$$j\omega(L_p + \frac{L_g}{2} - k\sqrt{L_p(L_p + L_g)}) \ll \frac{Z_0}{2}$$

is broken.

Figure 9.4 shows the comparison result that indicates the new method, which as expected noticeably improves accuracy. In summary, by constructing the equivalent circuits, the negative impact of the probe mutual inductance and power/ground vias loop inductances on the accuracy of the original VNA two-port methodology is analyzed. Improved probes and ports arrangements are introduced to enhance the accuracy.

Figure 9.4. Comparison between old and new two-port VNA methods



Similar techniques can be used for on-wafer PDN VNA measurements. The

wafers are placed on the measuring structures, and power/ground nodes are probed by the VNA. Also in this case, two-probe techniques are recommended, making the probe size requirement small. If there is not enough space for putting two probes on the same bumps, then probes have to be placed on different power/ground bumps. The first probe is on power1/ground1 bumps, and the second is on power2/ground2 bumps. In this case, it is necessary that the parasitics between power1/ground1 bumps and power2/ground2 bumps are minimal.

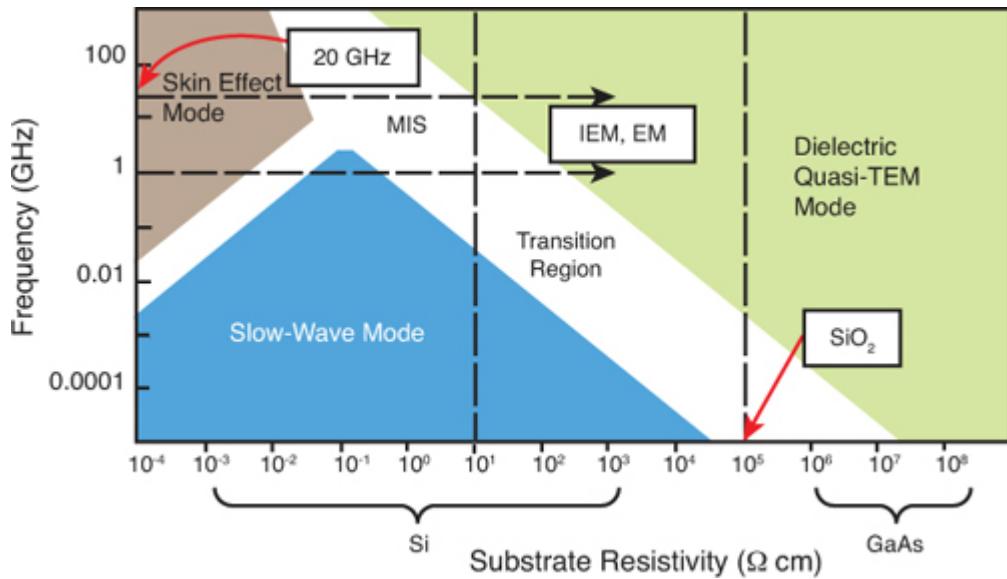
9.1.4. On-Chip Characterization

This section discusses the frequency domain characterization of the on-chip signal network and power network. Recent advances in circuit density and the speed of silicon Integrated Circuits (ICs) and System-on-Chips (SoCs) are placing increased demands on the performance of silicon interconnects. Problems associated with interconnects on silicon are inductive effects, silicon coupling and losses, common mode noise, dispersion, and electromagnetic interference (EMI). As more digital circuits are integrated on a single die, the interconnects fill an increasingly crucial role in determining the frequency limit, area, reliability, and yield of next generation ICs and SoCs. To avoid problems with the interconnects and to thereby increase the transmission bandwidth of subnanosecond digital signals, requires inductive effects to be reduced. The inductive effects need to be modeled accurately in the design phase. In particular, for efficient design and analysis of global interconnects, for example, clock, data, and power grid, precise RLC models of silicon interconnects become necessary.

Hasegawa et al. reported three fundamental modes on silicon substrate [6]. As Figure 9.5 shows, the fundamental propagation mode of the microstrip line on silicon substrate is determined by signal frequency and the resistivity of the guiding medium.

Figure 9.5. Fundamental propagation mode of silicon interconnects. [6]

[\[View full size image\]](#)



The modes are referred to as the skin-effect mode, slow-wave mode, and quasi-Transverse Electro-Magnetic (TEM) mode. When the signal frequency is high and the resistivity of the guiding medium is low, the skin-effect mode dominates. In this mode, the guiding medium behaves like a lossy conductor wall. In this range, because of the skin effect in the guiding medium, the line behaves dispersively. The slow-wave mode is important when the signal frequency is not so high and the resistivity of the guiding medium is moderate. In the slow-wave mode, the storage of electric and magnetic energy is spatially separated. The electric field does not penetrate into the guiding medium, whereas the magnetic field penetrates fully into it.

If both signal frequency and the resistivity of the guiding medium are high, the quasi-TEM mode is the dominant mode. Therefore, high resistivity is a necessary property of the guiding medium to transmit high-frequency signals with quasi-TEM mode propagation. One way to achieve this is to use low-loss dielectric layers as the guiding medium, because they have much higher resistivity than the silicon substrate. To avoid the high-frequency problems of the on-chip interconnects and therefore to increase the transmission bandwidth of subnanosecond digital signals through the interconnects, transmission line structures are required [7, 8]. In quasi-TEM transmission lines, phase velocity and impedance of the transmission line remain unchanged with frequency, thereby minimizing the signal dispersion and the impedance mismatch. Because the digital signals contain broadband frequency spectrum, the constant phase velocity and impedance are crucial properties of the future digital interconnects.

Microstrip lines have been widely used for interconnect structures of package and PCB because they are easy to fabricate and occupy a small interconnect area. However, microstrip lines exhibit frequency-dependent characteristics. By contrast, striplines and coplanar waveguides perform better, but they occupy a larger area. As Chapter 3 described, various EM-field solvers, analytical models, and empirical-solution based simulators are

available to analyze and design interconnects for chips. To reduce simulation time, calculations based on analytical models or empirical solutions, and 2D simulation tools, based on quasi-TEM approximations, are typically used. Because it is not easy to characterize the frequency dependency of material properties and quasi-TEM approximation has its limitations, it proves difficult to predict electrical characteristics accurately as a function of frequency with these methods. Modeling high-density on-chip interconnects is even more challenging, because of the high T/H ratio (metal thickness [T] relative to dielectric height [H]), and the low W/H ratio (signal line-width [W] relative to dielectric height [H]). Unlike the traditional PCB interconnects, the fringing field effects, dispersion effects, and radiation losses of microstrip on-chip interconnects are appreciable. Therefore, characteristic predictions of highly lossy or high aspect-ratio microstrip interconnects should be calibrated with either VNA S-parameter measurements or full-wave EM solver.

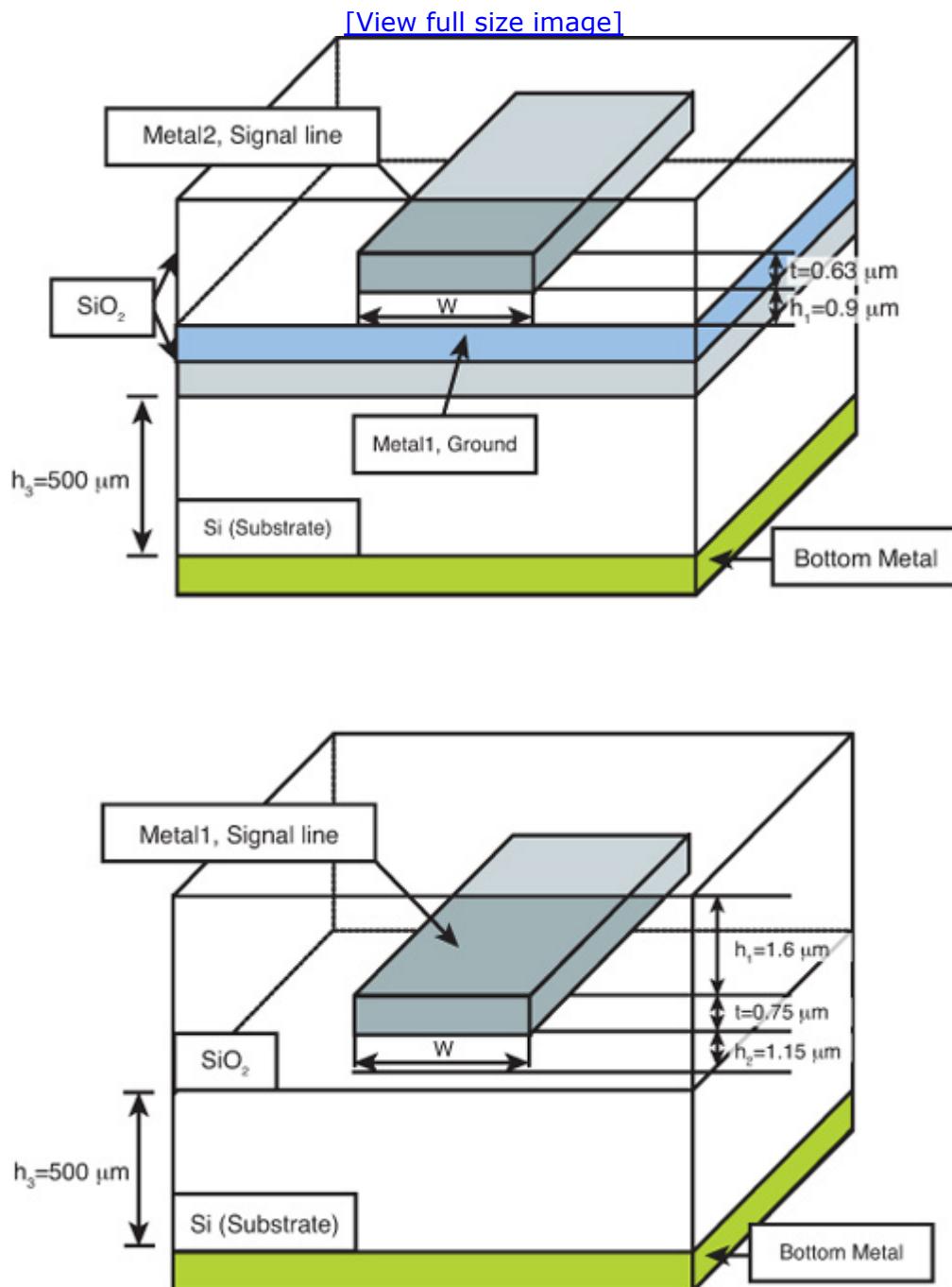
In a previous work [7], we evaluated and discussed three on-chip interconnect structures such as embedded microstrip (EM), inverted embedded microstrip (IEM), and metal-insulator-semiconductor (MIS). Using a 1-poly and 3-metal Si process, we fabricated test devices, as described in. [7] The test devices included different line structures with different sizes. The characteristic impedances and the propagation constants were extracted from the S-parameter measurement. The phase velocities and attenuation constants were derived from the extracted propagation constants. The frequency dependent model parameters of the transmission lines can be obtained by either using electromagnetic field solvers or using high-frequency measurement. For model extraction, the S-parameter measurement was proven acceptable. Analytical Telegrapher's RLCG models were suggested based on the previously reported models of microstrip lines [7, 9].

9.1.4.1. On-Chip Interconnect 2D Modeling and Correlation

To ensure the model accuracy, correlation between the lab measurement and 2D modeling result needs to be initially established. This section focuses on validating the accuracy of 2D modeling of on-die interconnects. As Figure 9.6 shows, both MIS and EM structures are studied. The lab measurement data from two other journal papers was used as the benchmark in this section [7, 9]. The detailed extraction process of the physical parameters from VNA measurement results can be found in these papers. Material properties used in the following correlation include Si dielectric constant 11.9; SiO_2 dielectric constant 4; loss tangent for SiO_2 0.0001; resistivity of silicon substrate $10 \Omega\cdot\text{cm}$, and metal conductivity 5.4×10^7 Siemens.

Figure 9.6. EM and MIS stack-ups used for Model Validation [7]

Source: W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495–503, Aug. 2000 © [2000] IEEE.



For embedded microstrip interconnect structures, [Figure 9.7](#) to [Figure 9.11](#) show the correlation between 2D modeling and measurement. According to [Figure 9.7](#), the characteristic impedance Z_0 from modeling correlates to the measurement data very well, from DC to 20GHz, with five different trace widths (3μm, 5μm, 7μm, 10μm, and 20μm). As [Figure 9.8](#) through [Figure 9.11](#) portray, exceptionally good correlations were found on resistance R and capacitance C , acceptable correlation on inductance L , whereas poor correlation on conductance G . Therefore, for embedded microstrip structure, in which case there is a thin metal layer above silicon substrate

and silicon effects are minimized, the 2D field solver accurately characterized the inductive effect but could not accurately characterize the conductive effect of silicon dioxide.

Figure 9.7. Embedded microstrip Z_0 correlation. Left: Extracted from lab measurement [7]; Right: From 2D field solver.

Source (Left): W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, “Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits,” IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495– 503, Aug. 2000 © [2000] IEEE.

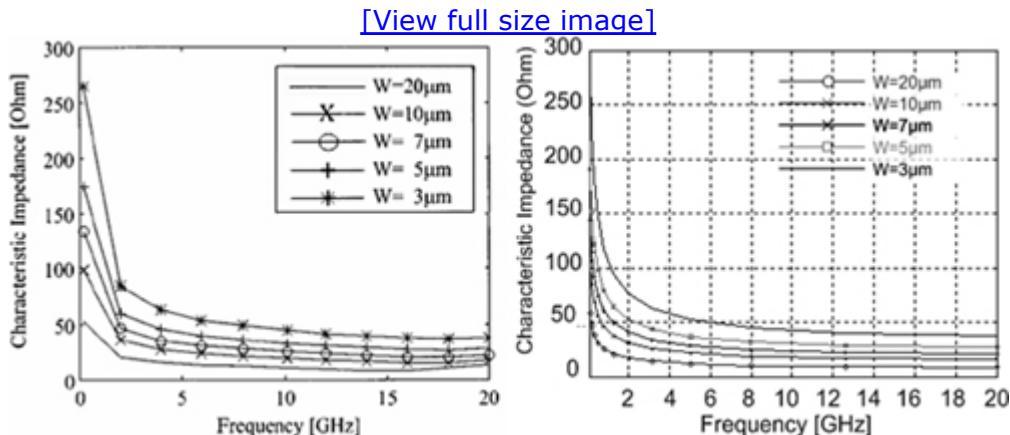


Figure 9.8. Embedded microstrip resistance correlation at 10Ghz. Left: Extracted from lab measurement [7]; Right: From 2D field solver.

Source (Left): W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, “Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits,” IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495– 503, Aug. 2000 © [2000] IEEE.

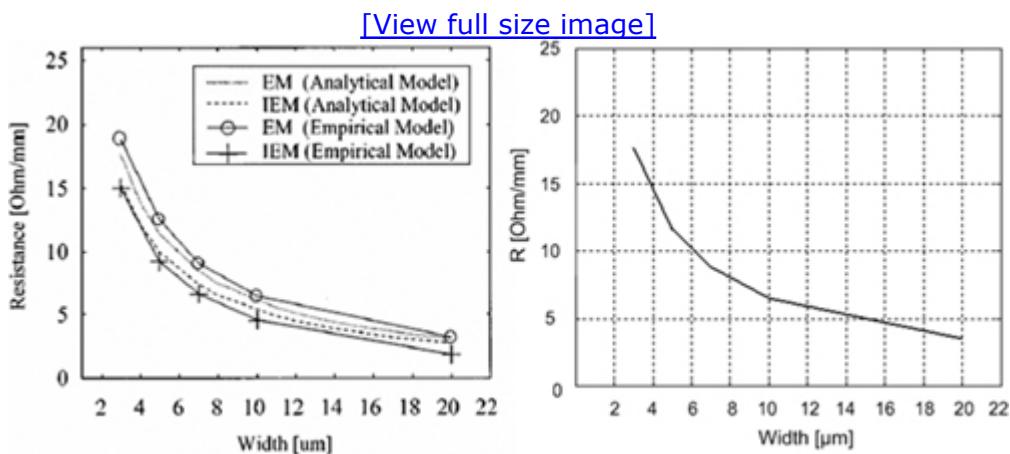


Figure 9.9. Embedded microstrip capacitance correlation at 10Ghz. Left: extracted from lab measurement [7]; Right: From 2D field solver.

Source (Left): W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495– 503, Aug. 2000 © [2000] IEEE.

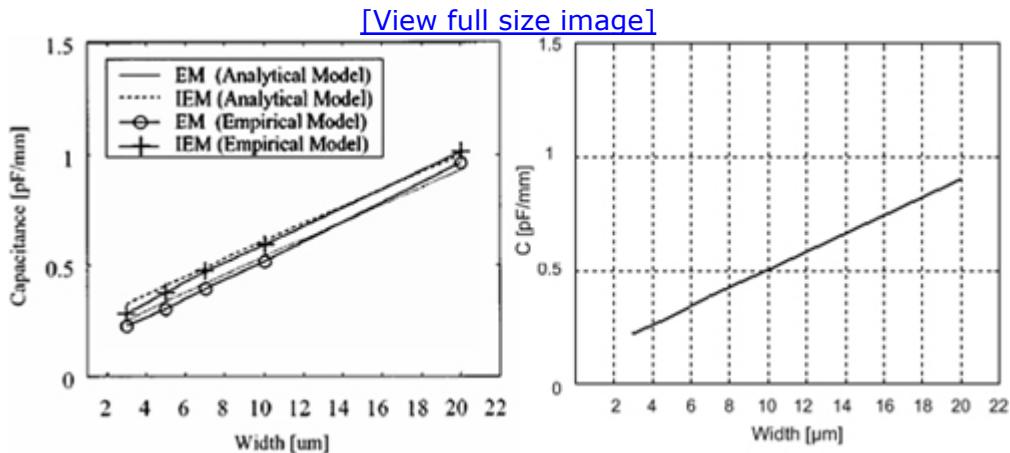


Figure 9.10. Embedded microstrip inductance correlation at 10Ghz. Left: Extracted from lab measurement [7]; Right: From 2D field solver.

Source (Left): W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495– 503, Aug. 2000 © [2000] IEEE.

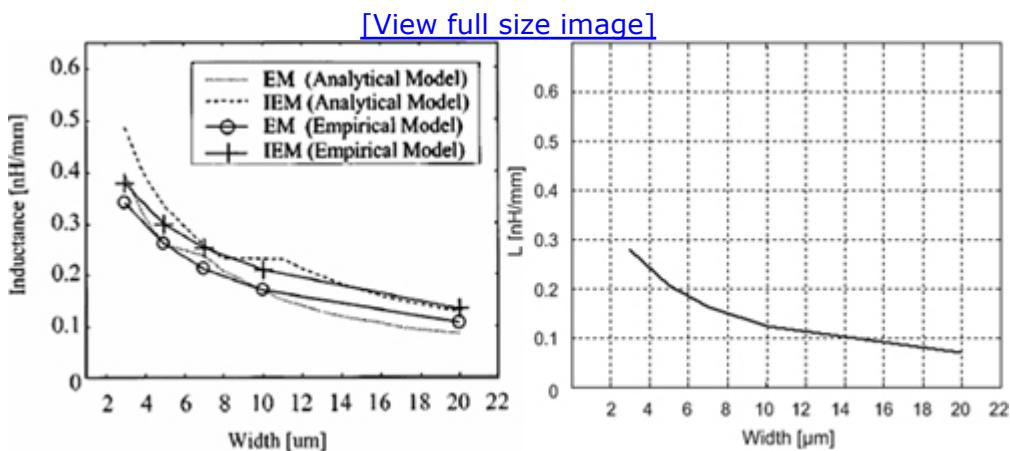
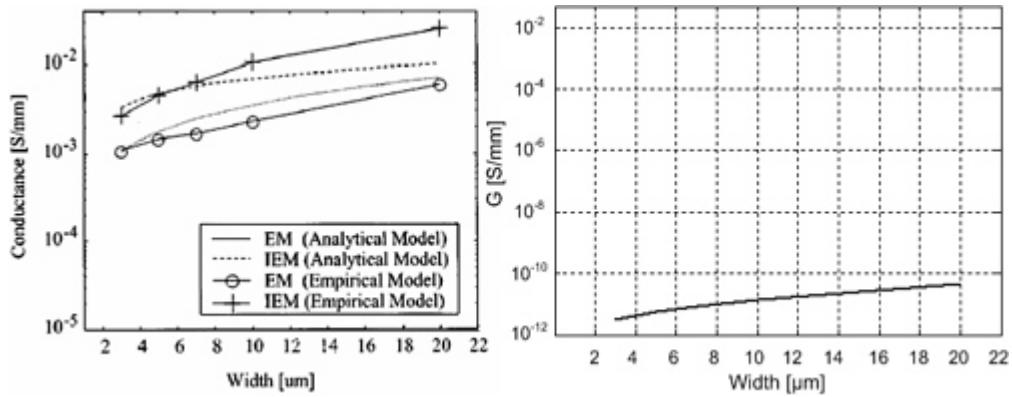


Figure 9.11. Embedded microstrip conductance correlation at 10Ghz. Left: Extracted from lab measurement [7]; Right: From 2D field solver.

Source (Left): W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495– 503, Aug. 2000 © [2000] IEEE.

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For MIS interconnect structures, correlations between 2D field solver modeling and high-frequency lab measurements are shown in [Figure 9.12](#) to [Figure 9.16](#). No ground plane is associated with the signal trace. Silicon substrate provides the current return path. As [Figure 9.12](#) depicts, the characteristic impedance Z_0 from the 2D modeling of a microstrip structure (from [6]) does not correlate well with the measurement data, from DC to 20GHz and across five different trace widths ($3\mu\text{m}$, $5\mu\text{m}$, $7\mu\text{m}$, $10\mu\text{m}$, and $20\mu\text{m}$). [Figure 9.13](#) through [Figure 9.16](#) show the correlation results for another microstrip structure (from [9]). Similarly, no good correlations were found on resistance R , capacitance C , inductance L , and conductance G . The mismatch on R , L , and C occurs because the silicon effects dominate the parasitics in this structure, and the 2D field solver does not characterize it well. It is interesting to note that the conductance miscorrelation for this case is smaller than that for the embedded microstrip case; indicating the 2D field solver underestimates the silicon dioxide loss and overestimates the silicon loss.

Figure 9.12. Microstrip structure 1 Z_0 correlation. Left: Extracted from lab measurement [9]; Right: 2D field solver.

Source (Left): Y. Eo and W.R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-parameter Measurements," IEEE Trans. Comp. Hybrid, Manuf. Technol., Vol. 16, No. 5, Aug. 1993
© [1993] IEEE.

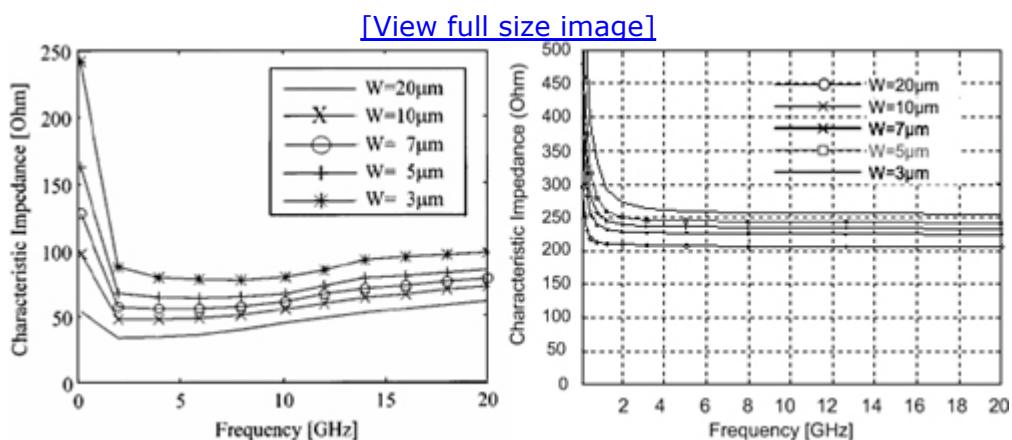
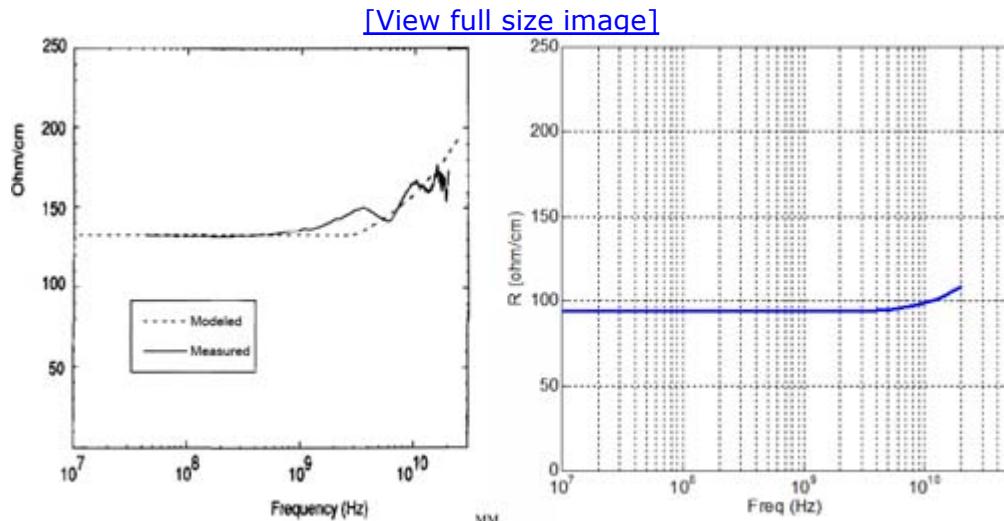


Figure 9.13. Microstrip structure 2 resistance correlation. Left: Extracted from lab measurement [9]; Right: 2D field solver.

Source (Left): Y. Eo and W.R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-parameter Measurements," IEEE Trans. Comp. Hybrid, Manuf. Technol., Vol. 16, No. 5, Aug. 1993
 © [1993] IEEE.



In summary, good correlations on RLC parameters between 2D field solver modeling and lab measurements were observed on the embedded microstrip structure but not on the MIS structure. Significant miscorrelation on G parameter was observed on both structures.

Figure 9.14. Microstrip structure 2 capacitance correlation. Left: Extracted from lab measurement [9]; Right: 2D field solver.

Source (Left): Y. Eo and W.R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-parameter Measurements," IEEE Trans. Comp. Hybrid, Manuf. Technol., Vol. 16, No. 5, Aug. 1993
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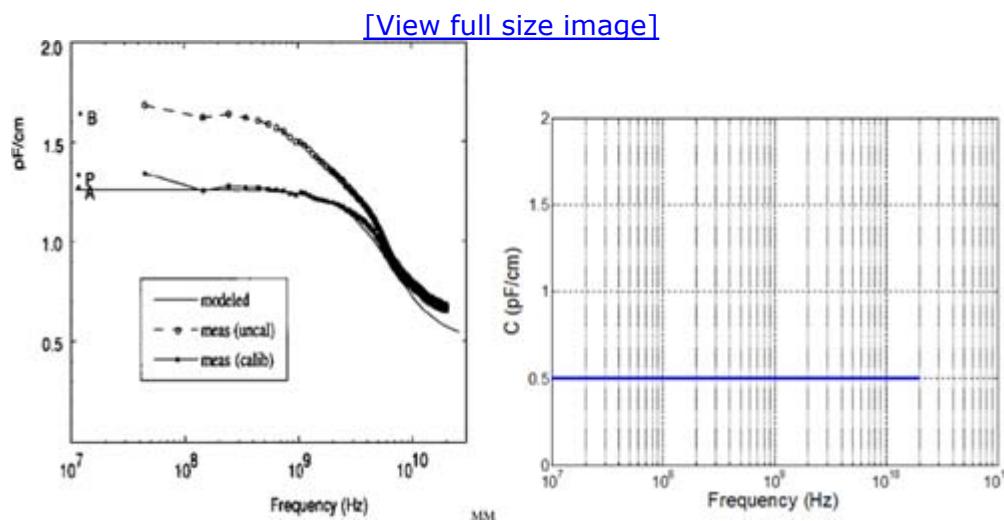


Figure 9.15. Microstrip structure 2 inductance correlation. Left:

Extracted from lab measurement [9]; Right: 2D field solver.

Source (Left): Y. Eo and W.R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-parameter Measurements," IEEE Trans. Comp. Hybrid, Manuf. Technol., Vol. 16, No. 5, Aug. 1993
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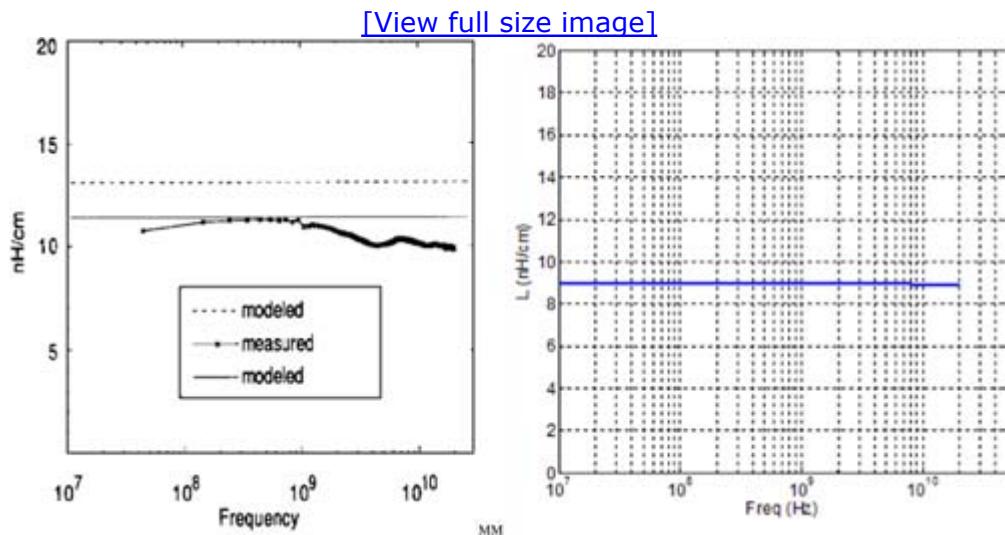
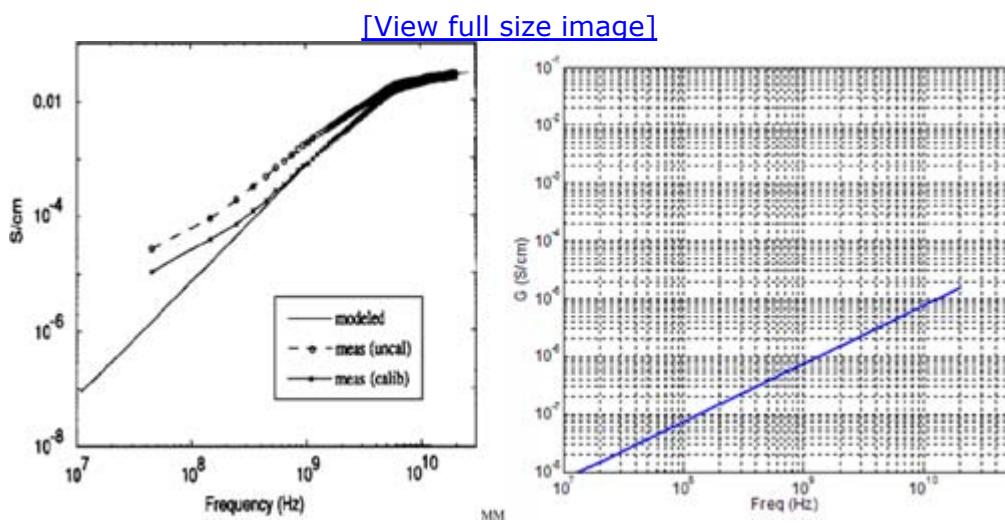


Figure 9.16. Microstrip structure 2 conductance correlation. Left: Extracted from lab measurement [9]; Right: 2D field solver.

Source (Left): Y. Eo and W.R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-parameter Measurements," IEEE Trans. Comp. Hybrid, Manuf. Technol., Vol. 16, No. 5, Aug. 1993
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9.1.4.2. On-Chip Interconnection Line Performance Versus Different Structures

There are different structures such as EM, IEM, and MIS [7]. The performance of the transmission lines are reflected in the propagation constant γ and the transmission characteristic impedance Z . The

propagation constant consists of attenuation constant and wavelength, which supply the direct physical properties of the lines. The propagation constant γ and the transmission characteristic impedance Z can be deduced from the de-embedded S'-parameters. The transmission line impedance is defined as a complex ratio of the current to the voltage waves propagating along the transmission line. Equations (9.18) and (9.19) relate the de-embedded S'-parameters to the propagation constant γ and the characteristic impedance Z , where Z_0 depicts the characteristic impedance of the probe, which is 50Ω .

Equation 9.18

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}'^2 + S_{21}'^2}{2S_{21}'} \pm K \right\}^{-1}$$

$$\text{Where, } K = \left\{ \frac{(S_{11}'^2 - S_{21}'^2 + 1)^2 - (2S_{11}')^2}{(2S_{21}')^2} \right\}^{\frac{1}{2}}$$

Equation 9.19

$$Z = Z_0^2 \left\{ \frac{(1 + S_{11}'^2)^2 - 2S_{21}'^2}{(1 - S_{11}'^2)^2 - 2S_{21}'^2} \right\}$$

The Slow Wave Factors (SWFs) and the attenuation constants were calculated from the propagation constant obtained in equation (9.18). The SWF is defined as the square root of the effective dielectric constant of the dielectric guiding medium, as equation (9.20) portrays; where λ is the wavelength at the transmission line and λ_0 is the wavelength at the free space.

Equation 9.20

$$SWF = \sqrt{\epsilon_{eff}} = \lambda / \lambda_0$$

Figure 9.17 shows the SWF of the three structures, including the MIS, the EM, and the IEM structures. The lower slow wave factor means higher phase velocity. Figure 9.17 also demonstrates the slow wave factor of the MIS structure clearly differs from that of the EM and the IEM structures. Compared to the SWF of the conventional MIS structure, the SWFs of the microstrip structures demonstrate much lower values. The phase velocities of the microstrip structures are more than 8×10^7 [m/s], whereas the phase velocity of the MIS structure is below 5×10^7 [m/s] from 200MHz to 14GHz. That means, when waves propagate along those structures, the propagation

velocities vary. Moreover, the difference in the phase velocity becomes obvious when the signal frequency exceeds 2GHz. The slow wave factor of the EM and the IEM structures remains constant at frequencies above 2GHz, indicating that the quasi-TEM mode propagation is supported. In the quasi-TEM mode propagation, phase velocity and impedance should be independent of frequency. As the previous section relates, the propagation mode is decided by the product of signal frequency and the resistivity of the guiding medium. Below 2GHz, the EM and the IEM structures also show high SWF, thereby exhibiting slow wave mode propagation. For digital signals of GHz clock frequency, the high frequency spectrum of the signal, over the frequency of $f=1/nt_r$ or $f=1/nt_f$ (t_r : rising time, t_f : falling time), typically decide waveform of the rising and falling time. Accordingly, the constant slow wave factor in the high-frequency region comprises an essential property for the GHz digital interconnect. The effect of the inductive and the conductive losses of the MIS structure substantially increases at higher frequency. Due to the leakage of the electromagnetic field into the Si substrate in the IEM structure, the phase velocity of the IEM structure is lower than that of the EM structure.

Figure 9.17. Slow wave factors (SWF) of MIS, EM, and IEM structures of a 20- μm line width

Source: W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495–503, Aug. 2000 © [2000] IEEE.

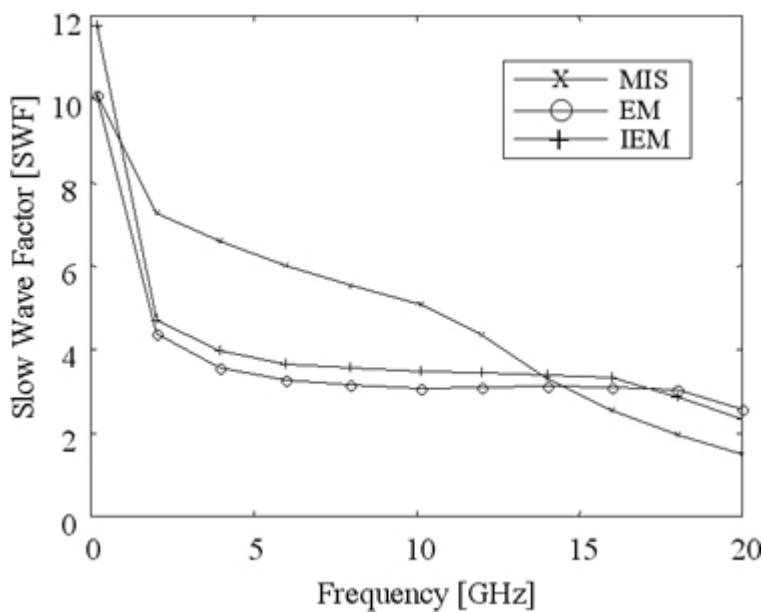


Figure 9.18 illustrates the attenuation constant of the three structures. As can be expected, the attenuation constant of the MIS structure is considerably higher than that of the EM and IEM structures at frequencies over 4GHz. In particular, the attenuation constant of the MIS interconnect line is 3dB/mm higher than those of the microstrip interconnect lines at

20GHz. Because of leakage of the electromagnetic wave into the silicon substrate, the IEM structure supports more lossy wave propagation than the EM structure. Concerning the microwave properties, the EM structure has yielded the best performance, revealing lower SWF and lower attenuation constant. Due to via holes for the ground contact, however, the EM structure has numerous discontinuities. Considering the compatibility and discontinuities of the process, the IEM structure is recommended. The attenuation at low frequency below 1GHz is negligible for all three structures.

Figure 9.18. Attenuation constants of MIS, EM, and IEM structures of a 20- μm line width

Source: W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp. 495–503, Aug. 2000 © [2000] IEEE.

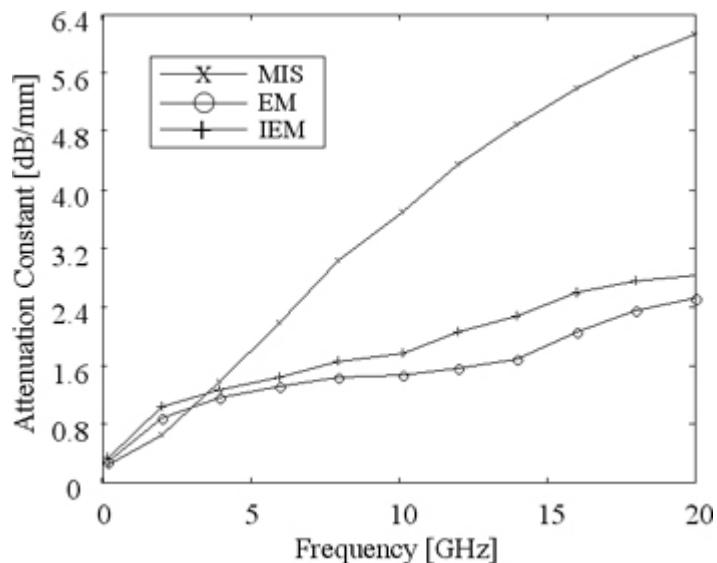
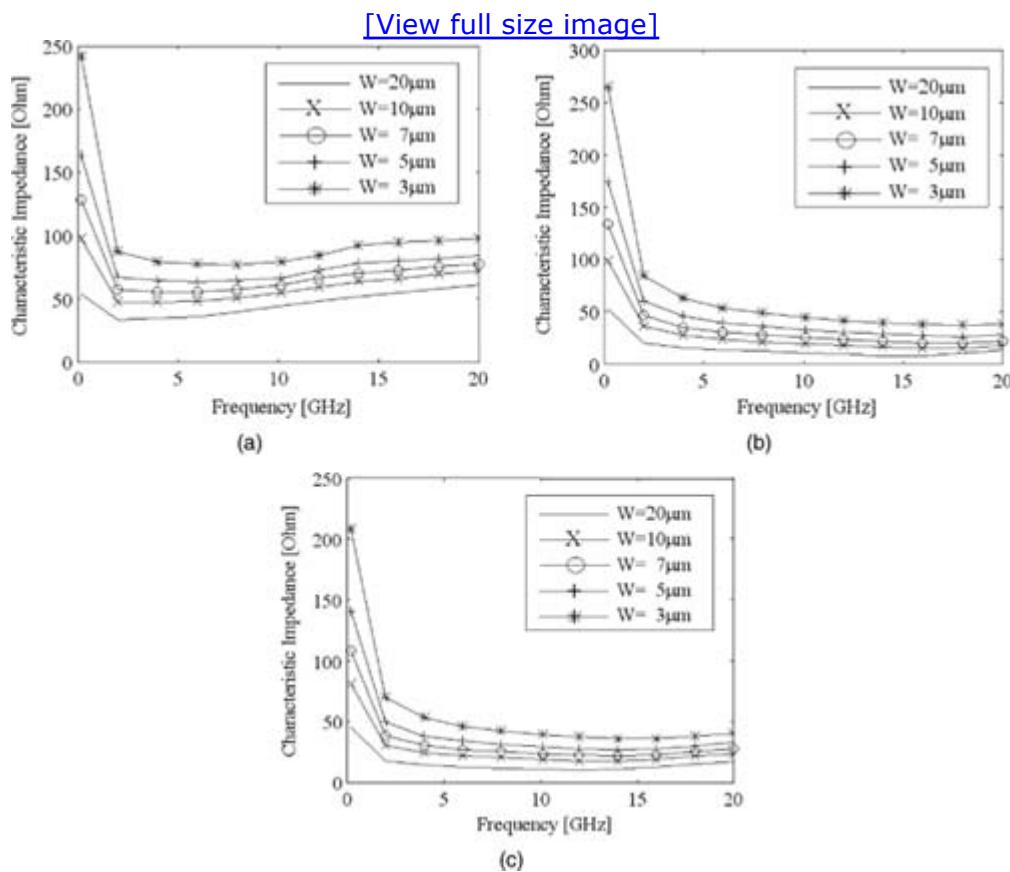


Figure 9.19 (a), (b), and (c) illustrate the characteristic impedances of the MIS, the EM, and the IEM structures up to 20GHz. The interconnect lines of the structures have widths of 3, 5, 7, 10, and 20 μm . As **Figure 9.19 (b)** and **(c)** show, the EM and the IEM structures appear more feasible for low characteristic impedance. Also, within a few μm of line width, 50-ohm impedance matching is easily achievable, using the microstrip structures. At 2-GHz frequency, the characteristic impedance of the microstrip structures makes the transition from extremely high DC impedance to the mode's constant characteristic impedance. In the quasi-TEM mode propagation, the impedance of the transmission line is inversely proportional to the square root of line capacitance. Wider lines have higher line capacitance and, therefore, lower characteristic impedance. This tendency is observed in all three structures. Also a thinner dielectric guiding layer results in low impedance. Based on the analysis of the SWF and the characteristic impedance of the interconnect line structures, it shows that the microstrip structures support the quasi-TEM mode propagation at high frequency and

are more appropriate to achieve 50-ohm impedance.

Figure 9.19. Characteristic impedance of MIS, EM, and IEM structures depending on the line widths of 3, 5, 7, 10, 20 μ m. (All data is extracted from de-embedded S-parameters.) (a) characteristic impedance of MIS structure. (b) characteristic impedance of EM structure. and (c) characteristic impedance of IEM structure.

Source: W. Ryu, S. Baik, H. Kim, J. Kim, M. Sung, and J. Kim, "Embedded Microstrip Interconnection Lines for Gigahertz Digital Circuits," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp 495–503, Aug. 2000 © [2000] IEEE.



To provide high-performance interconnect line structures for GHz ICs and SoCs, transmission line structures, such as the EM and the IEM structures, are required. These two structures exhibit constant impedance and high-phase velocities at frequencies more than 1GHz. Due to the high dielectric loss of the substrate, we found that the conventional MIS structure could not support the quasi-TEM mode propagation. On the other hand, it is proved that the transmission line structures, including EM and IEM, can carry GHz digital signals with the quasi-TEM mode.

9.1.4.3. On-Chip PDN Characterization

The performance of the on-chip PDN can be measured by on-wafer VNA

characterization. As discussed in [Chapter 4](#), “System Interconnects,” different elements of on-chip PDN exist, which include power grid, intentional decoupling capacitors, and unintentional decoupling capacitors. For determining the power grid parasitics, a special test vehicle needs to be designed, containing only the power grid, as shown in [Figure 5.30](#). There are two structures on this vehicle: open power grid and short power grid. Because no access exists to probe the die at the lower metal layers, these two structures are needed. With measuring both the open and short S-parameters of the grid, the [2×2] matrix can be constructed and the simple RLGC model can be extracted.

For the on-chip PDN of the entire interface, the S-parameters are probed on the wafer. [Figure 5.36](#) shows the on-chip PDN measurements for the I/O interface. This measurement can verify the on-chip model, constructed with grid and intentional/unintentional capacitors. Note that for the on-chip interface, the measurements can be performed on the die-bumps, using small VNA probes. If the bump size is too small compared to the probe size, the two probes in the two-port method may connect to different sets of power/ground bumps. In that case, the die-bumps for the two ports need to be electrically close. If higher parasitics exist between two power bumps, due to on-chip routing, then two-port method cannot be used to acquire the Z_{11} of the on-chip PDN; however, Z_{21} , the transfer impedance between two bumps, can be obtained.

9.1.5. Pad Capacitance Characterization

The I/O device pad capacitance (C_{pad}) consists of all the capacitance seen from the chip pad; this may include capacitance of I/O circuits and interconnects. It can be measured by VNA in the frequency domain. The device capacitance can be extracted from the measured S-parameters.

9.1.5.1. Lower- and Upper-Frequency Limit

Due to large amount of reflection, VNA measurement and extraction error increases significantly. Thus, we need to select frequency range of C_{pad} extraction properly so the errors can be minimized. We define a dynamic range indicator (DRI) for reflection loss, due to C_{pad} , based on the following equation:

Equation 9.21

$$DRI = \left| 20 \cdot \log \left(1 - \frac{Z_{C_{\text{pad}}} - 50}{Z_{C_{\text{pad}}} + 50} \right) \right|$$

where $Z_{C_{\text{pad}}}$ is the impedance of the I/O capacitance C_{pad} . As frequency

decreases, impedance of the Cpad increases and the DRI decreases, making the measurement more difficult and increasing the extraction error. Table 9.1 shows with different Cpad value, how DRI varies with frequency change. In most instances, the expected Cpad value is under 2pF. The recommended DRI for a Cpad measurement is 40dB or lower. For example, the magnitude of impedance for Cpad = 1pF at 20MHz is approximately 8kΩ. Assuming a VNA with a 50Ω reference impedance, its DRI equals to 38dB. Cpad of 1pF can be measured from 20MHz up to the first resonance frequency. Open-circuited transmission line has resonant frequency at one-quarter wavelength ($\lambda/4$). At the frequency of one-quarter wavelength of the interconnects, the dynamic range clearly decreases. The higher end of the frequency range for Cpad extraction should be conducted $<< \lambda/4$ frequency. Longer package and PCB interconnect lines have lower resonant frequency. The parasitic inductance effect (3D electromagnetic effect) and return path effect will further decrease the resonance frequency.

Table 9.1. VNA DRI of Cpad Measurement Versus Frequency

Cpad	Frequency	DRI (dB)
1pF	1MHz	64
	10MHz	44
	20MHz	38
2pF	1MHz	58
	10MHz	38
	20MHz	32
3pF	1MHz	54.5
	5MHz	40.5
	10MHz	34.6

9.1.5.2. De-Embedding Method

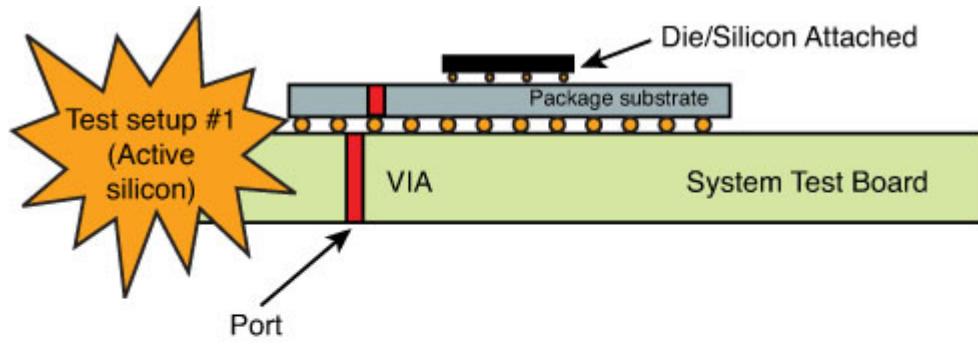
A number of various approaches have been developed for removing the effects of the test fixture from the measurement. These approaches fall into two fundamental categories: Direct measurement and de-embedding. De-embedding uses a model of the test fixture and mathematically removes the fixture characteristics from the overall measurement.

This fixture de-embedding procedure can produce extremely accurate results for the noncoaxial DUT, without complex noncoaxial calibration standards. For this case, the de-embedded measurements can be post-processed from the measurements made on the test fixture and DUT

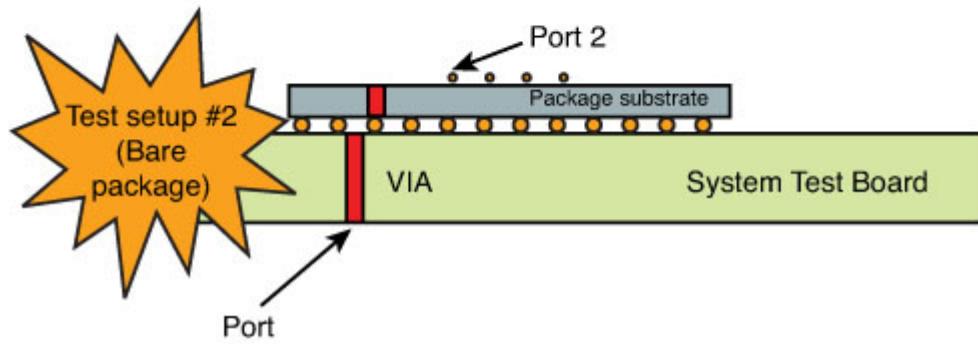
together. Using a different calibration model, we can also perform the de-embedding calculation directly on the VNA.

In the single-ended two-port based de-embedding, as Figure 9.20 shows, we use the test setup #2 to obtain the $[2 \times 2]$ S parameter of bare package and use test setup #1 to get the S_{11} of the package with die.

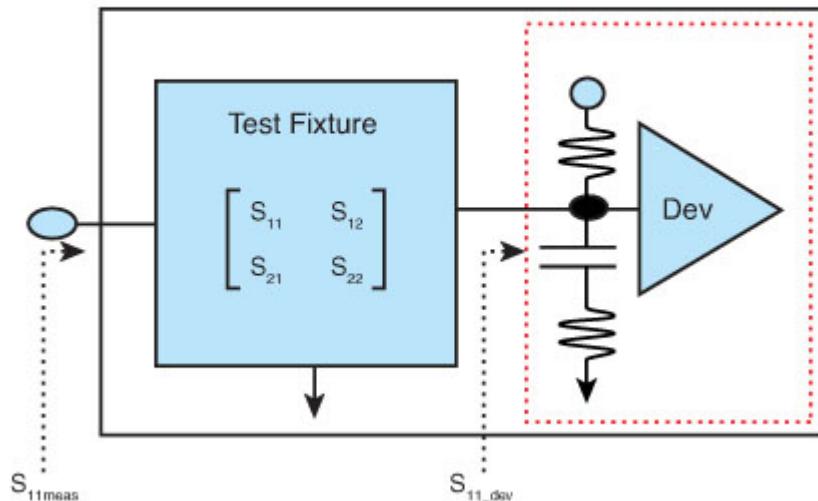
Figure 9.20. Block diagram of single-ended two-Port de-embedding method



(a) Measurement of die and package on the test board



(b) Measurement of package on the test board



(c) Block diagram of measurement scheme

The de-embedding formulae are listed here:

Equation 9.22

$$S_{11_dev} = \frac{S_{11_meas} - S_{11}}{S_{12} \cdot S_{21} - S_{11} \cdot S_{22} + S_{11} \cdot S_{11}}$$

Equation 9.23

$$Z_{11_dev} = \frac{50 \cdot (1 + S_{11_dev})}{1 - S_{11_dev}}$$

Equation 9.24

$$C_{dev} = (-1) \cdot \frac{1}{2 \cdot \pi \cdot f \cdot \text{imag}(Z_{11_dev})}$$

where S_{11_dev} and Z^{11_dev} are return loss and input impedance of I/O device and f is frequency. S_{11} , S_{12} , S_{21} , and S_{22} are two-port S-parameter of test fixtures, including bare package and PCB, as shown in [Figure 9.20](#).

9.1.6. Power Delivery-to-Signal Coupling Measurement

Jongbae Park et al. [22] experimentally demonstrated the Simultaneously Switching Output (SSO) noise coupling effect to signal. In his experimental study, the DUT has 190mm X 80mm size and the six-layer stack up same to that of DDR memory module as shown in [Figure 9.21](#). DUTs have four different signal line structures, a ground referenced microstrip line (Type-1), a ground referenced strip line (Type-2), a power referenced strip line (Type-3), and a power referenced microstrip line (Type-4), as shown in [Figure 9.22](#). Total line length is 80mm and line length between vias is 60mm. The clock driver chip was implemented as an SSO source.

Figure 9.21. Top view of test DUTs [22]

Source: J. Park, et al, “Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module,” Proceeding of EMC 2004 © [2004] IEEE.

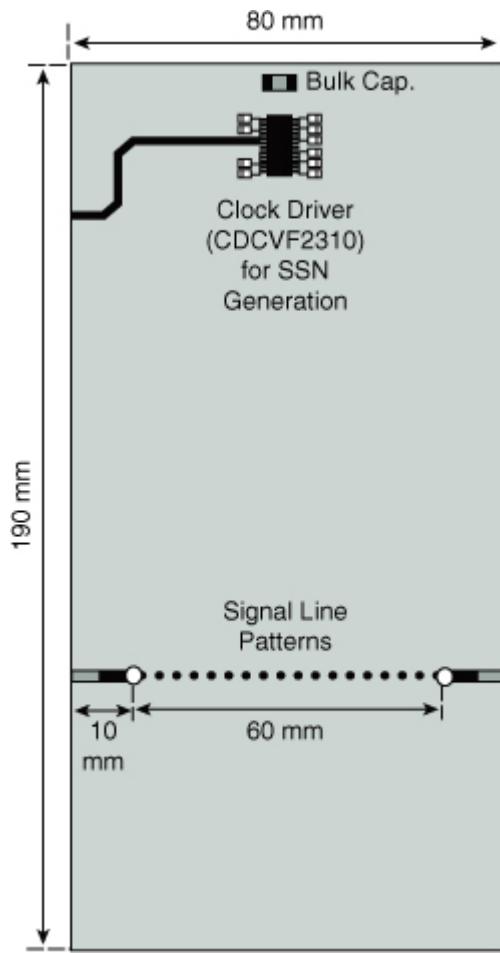


Figure 9.22. Cross-section of manufactured DUTs, which have a six-layer stackup that is the same to that of the DDR memory module. DUTs have different signal line structure: (a) ground referenced microstrip line (Type-1), (b) ground referenced strip line (Type-2), (c) power referenced strip line (Type-3), and (d) power referenced microstrip line (Type-4). [22]

Source: J. Park, et al, "Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module," Proceeding of EMC 2004 © [2004] IEEE.

[\[View full size image\]](#)

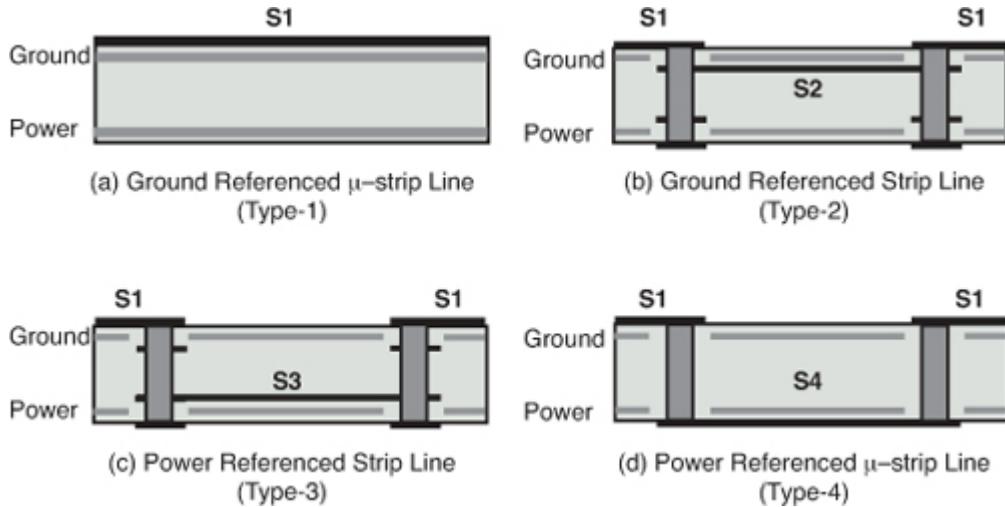
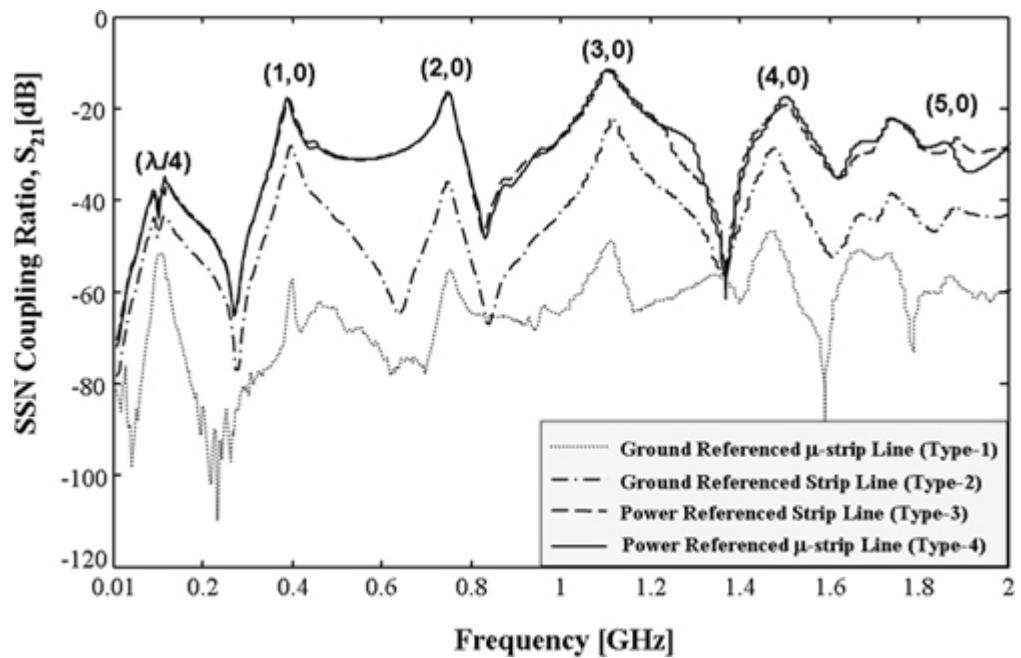


Figure 9.23 shows the measured coupling ratio, ' S_{21} ', to evaluate the SSO coupling effect to the signal. Port1 is placed between the power and ground plane at the center of the clock driver chip, and port2 is located at the one end of the signal trace, of which the other end is terminated by 50Ohm. As shown in Chapter 7, "Signal/Power Integrity Interactions," there are two SSO coupling mechanisms. The first SSO coupling mechanism is through the reference changing via, and the second coupling mechanism is SSO coupling to signal through the trace between power and ground plane. Because of the first SSO coupling mechanism, the amount of the SSO coupling to the power referenced signal line structure with the reference changing vias is larger than that to the ground referenced signal line structure without the reference changing vias. It is also shown that because of the second SSO coupling mechanism, the amount of the SSO coupling to the stripline is larger than that to the microstrip line. Through the frequency domain measurement result, we can confirm that the reference changing via is the dominant factor to couple the SSO. The peak of coupling coefficient corresponds to either the plane resonant or signal resonant mode. The plane-to-signal coupling significantly increases at resonance.

Figure 9.23. Measured coupling ratio, S_{21} , to evaluate the coupling of power/ground noise to the signal trace. Port1 is placed between power and ground plane at the center of SSO generating chip, and port2 is located at the one end of the signal trace, which the other end is terminated by 50Ohm. Ground referenced microstrip line (dotted line), ground referenced strip line (dash-dotted line), power referenced strip line (dashed line), and power referenced microstrip line (solid line) [22].

Source: J. Park, et al, "Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module," Proceeding of EMC 2004 © [2004] IEEE.

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9.2. Equivalent Circuit Model Extraction

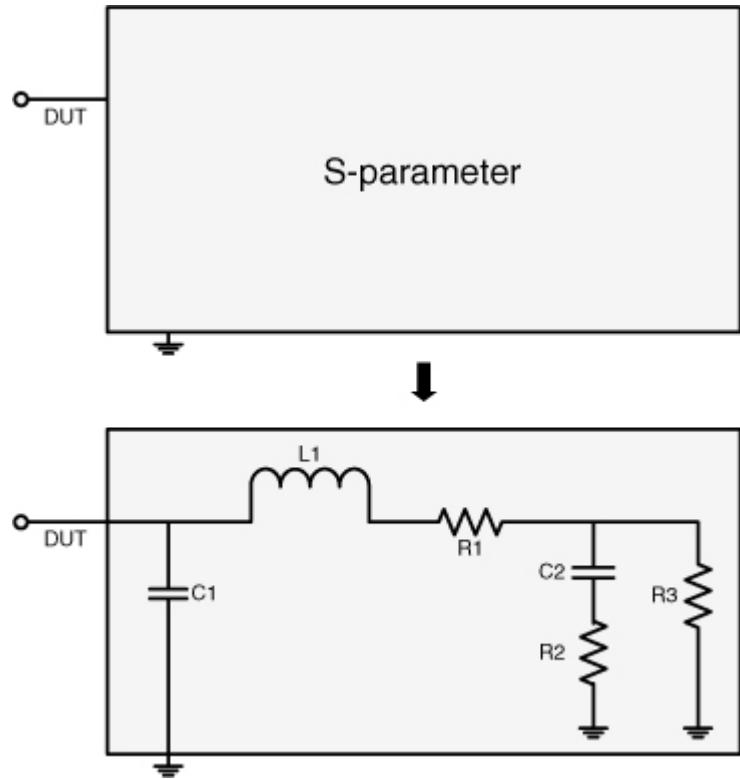
9.2.1. Need for an Equivalent Circuit Model

Measured frequency domain data provides useful behavioral information of the DUT. However, it is often required to extract circuit parameters from the measured data: (1) to validate whether the DUT meets the specification requirements and (2) to provide necessary circuit information for simulations. Especially, as some on-chip parameters are relatively sensitive compared with other off-chip parameters and their contribution to the system simulation proves substantial. Therefore, it is crucial to obtain precise measurement and accurate extraction algorithm and methodology.

9.2.1.1. Validation Purpose

In the design of an electrical system, specification of a device is assumed to be within a certain tolerance. However, because of manufacturing tolerances and faults, the specifications are often broken. To validate the DUT, frequency domain S-parameter measurement on the device is performed. Nevertheless, because the measured data is in the frequency domain, it is difficult to judge if the S-parameter data has passed the pass/fail criteria. Therefore, the extraction of parameters using predefined topology is required to validate the device. [Figure 9.24](#) shows an example of one-port S-parameter data and its approximated circuit topology. It also shows a signal line terminal at the package BGA location. From the measured and simulated S-parameters, it is required to fit them in the given equivalent circuit topology. It is required to extract the critical parameters, such as C_{pad} and R_{term} from the measured S-parameter.

Figure 9.24. Example of equivalent topology for package and transistor pad



9.2.1.2. Simulation Purpose

Simulation of measured S-parameter data can be easily conducted using the S-parameter import capability in the most SPICE-compatible simulator. However, doing so provides a probing point only at the ports of the measurement. To probe the signal on the inside of the DUT, the extraction of circuit parameters, as shown in [Figure 9.24](#), should be accurately done.

9.2.2. Extraction Methodology

The extraction of the parameters from the frequency domain measurement data requires knowledge on computational numerical analysis and system function. [Figure 9.24](#) shows a Z-parameter calculation of a DUT topology.

Equation 9.25

$$Z_{11} = (1/sC_1) \parallel (sL_1 + R_1 + (R_3 \parallel (1/sC_2 + R_2)))$$

Equation 9.26

$$Z_{11} = \frac{1}{sC_1} \parallel \left(sL_1 + R_1 + \frac{R_3 \left(\frac{1}{sC_2} + R_2 \right)}{R_3 + \frac{1}{sC_2} + R_2} \right)$$

where s is $j\omega$.

There are five unknown variables: C_1 , L_1 , R_3 , C_2 , and R_2 . Determining these five variables to minimize the difference with measured Z-parameter leads to an optimization problem or a curve fitting problem. The number of measured data frequency sampled points is higher than the number of unknown variables. As an over-determined system, it leads to solving a nonlinear least-square problem. Generalizing the problem statement: Function g of equation (9.27), which constitutes the objective function, needs to be minimized for all frequencies. Equation (9.28) states the optimization problem for the defined function.

Equation 9.27

$$g(x, f) = |Z_{11}(x, f) - Z_{11meas}(f)|$$

Equation 9.28

$$\min_x \|g(x, f)\|_2^2 \Big|_{\text{for all } f} = \min_x \left(g(x, f_1)^2 + g(x, f_2)^2 + \dots + g(x, f_n)^2 \right), lb \leq x \leq ub$$

Here, x depicts a set of unknown variables, f is the frequency, Z_{meas} is the measured Z-parameter, and g is the objective function.

To emphasize certain bandwidth for better fitting, the weight function can also be used. The modified function should look like equation (9.29), and the weight function $W(f)$ should have value in between 0 and 1 at each frequency point.

Equation 9.29

$$g(x, f) = |Z_{11}(x, f) - Z_{11meas}(f)| * W(f)$$

In summary, the final problem statement becomes a constrained, weighted nonlinear least-square problem. A number of algorithms and numerical analysis tools exist to solve the optimization problem.

9.2.2.1. Numerical Error

The extraction of the parameters, using a nonlinear least square solution, inherently introduces numerical errors because of underflow, overflow, or cancellation. For example, because of the limited floating point accuracy in computation, the vastly different circuit element units tend to cause errors. Examples of these include pF range capacitors and high-impedance resistors in the process of a circuit topology transfer function calculation. These errors, due to needless underflow, overflow, or cancellation, can be partially mitigated by using higher precision algorithms; however, it cannot be a

complete solution. Rescaling, nevertheless, can prevent these errors. It is crucial to rescale the component values to somewhat similar ranges. The unknown variable $x - \{x_0 \text{ F}, x_1 \text{ ohm}, x_2 \text{ H}\}$, for example, can be rescaled to $\{x_0 \text{ pF}, x_1 \text{ mohm}, x_2 \text{ nH}\}$ if they are expected to be in pF, mohm, and nH range, respectively.

9.2.3. Extraction Examples

The following section gives examples of extraction for the signal net and for the power net.

9.2.3.1. Receiver Model for SI

The signal net I/O interconnection, connected to receiver buffer, shows its distinctive characteristics with small inductance, losses in its transmission line, and small receiver-end capacitance. The topology should be carefully selected to reflect the I/O signal's distinctive characteristics. Also, the units for the unknown variables should be carefully rescaled to avoid any big accuracy loss due to numerical errors. [Figure 9.25](#), [Figure 9.26](#), and [Figure 9.27](#) show examples of the parameter extraction results, with the aforementioned optimization technique for a structure similar to [Figure 9.24](#).

Figure 9.25. Magnitude comparison of extracted versus measured data

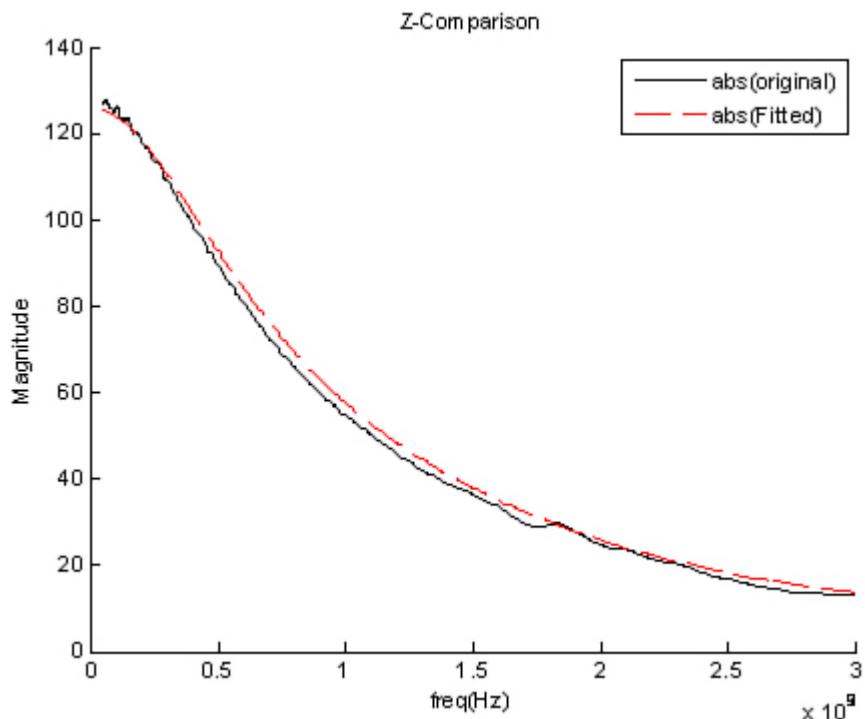


Figure 9.26. Real part comparison of extracted versus measured data

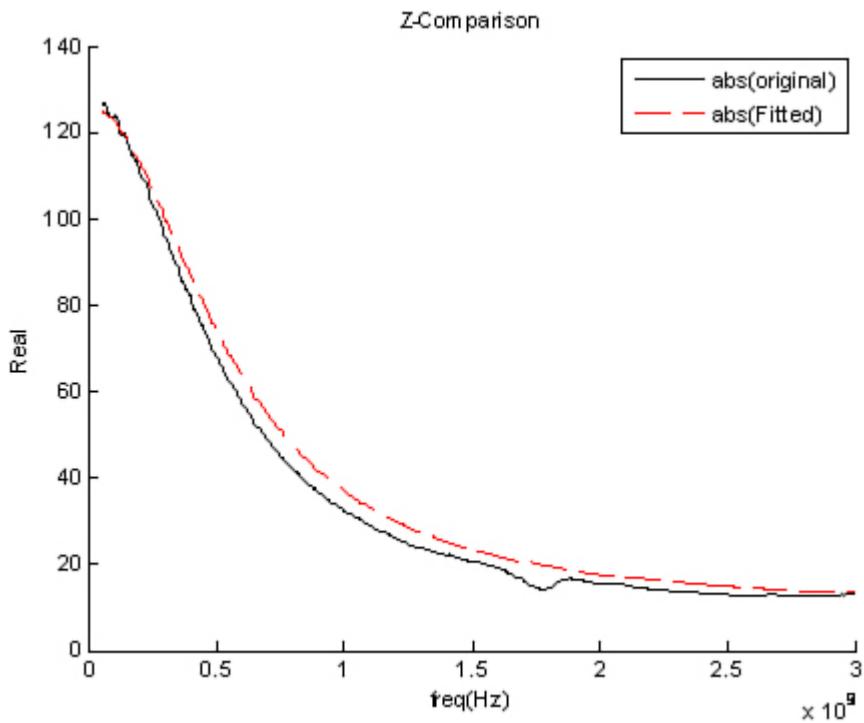
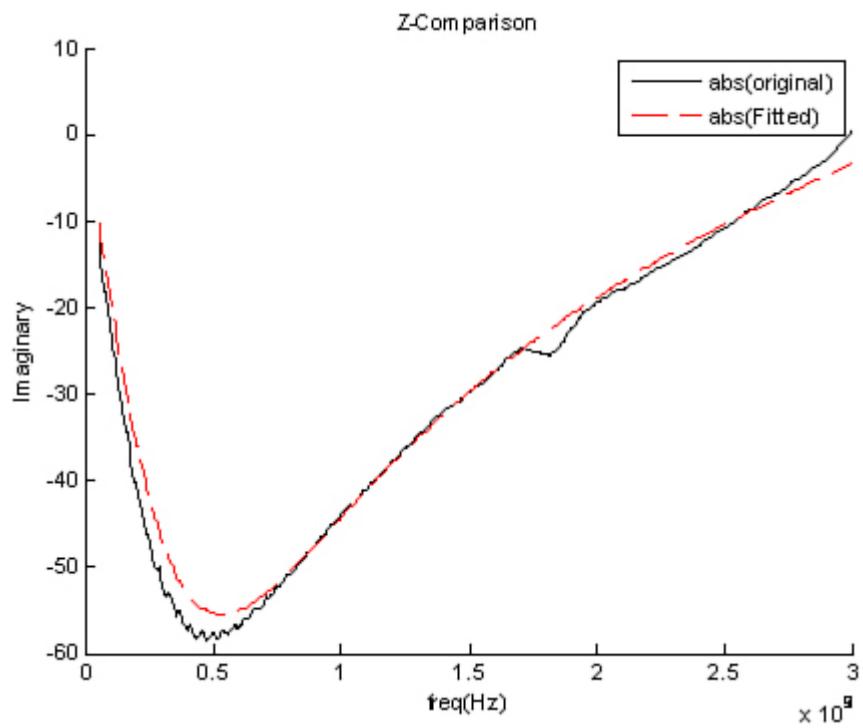


Figure 9.27. Imaginary part comparison of extracted versus measured data



9.2.3.2. PDN Model

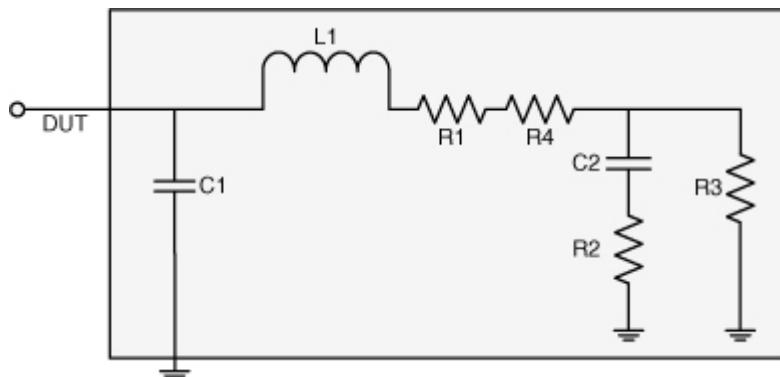
All the extraction procedures and algorithms for power net are identical as those for signal net. Equivalent circuit topology for power net may even primarily resemble a topology similar to the signal net. However, the components of the topology often have a different value range than the

signal interconnection components. Rescaling the unknown variables according to the each variable value range is important in obtaining reasonable and accurate solutions. Figure 5.29 shows an example of the parameter extraction results with the aforementioned optimization technique. In Figure 5.29, the on-chip PDN parameters are extracted when probing is done on the package BGA location. The topology of extracted circuit is shown in Figure 5.27 with on-chip PDN components. Figure 5.31 shows another example of the power net. The response of extracted circuits and that of the S-parameters correlate well as shown in Figure 5.32.

9.2.3.3. Topology Identification

To represent all the parasitic effects, topology of the inside of the DUT should be determined based on the configuration at its best. Because of the efficiency limitation of the nonlinear least square solver, the number of unknown variables should not be too high. Also to make the solution as unique as possible, the ambiguous definition of topology, such as two resistors R1 and R4 in the same branch as shown in Figure 9.28, should be avoided. Practically, the number of the unknown variable should be kept smaller than approximately a dozen for one-port measurement data.

Figure 9.28. Example of ambiguous construction of equivalent circuit topology



9.2.4. Extension to Multiport Measurement

For the multiport S-parameters measurement data, the objective function should be modified to accommodate the multiport S-parameters. So the objective function becomes:

Equation 9.30

$$g(x, f) = \sum_{k=1}^N \left(|Z_{k1}(x, f) - Z_{k1meas}(f)| + \dots + |Z_{kN}(x, f) - Z_{kNmeas}(f)| \right)$$

Increasing the number of measurement ports increases accuracy of

optimization. However, the cost and physical difficulties of probing inside of the DUT often hinder multiport measurement of the devices.

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9.3. Time Domain Characterization

The time domain measurement has historically been the standard measurement tool for characterizing and troubleshooting I/O signaling and serves as a common method in the areas of signal/power integrity. Oscilloscopes are used for time domain noise and timing measurements. TDR and TDT are time domain techniques based on the principle of wave reflections and transmissions respectively. The following section addresses the TDR application with faster rise times.

9.3.1. Time Domain Reflectometry (TDR)

As TDR serves as an extremely effective tool for interconnection characterization and analysis and has been used for the analysis of traces on dielectric substrates of packages and PCBs. The analysis is typically performed by measuring characteristic impedances or by observing signal profile to detect failure mechanisms of various transmission lines. In addition, some extended applications of TDR on interconnects (transmission channels containing connectors and via structures) show impedance variations as a function of time. This may be a particularly useful tool for the high-speed interconnect design and validation. However, when it comes to package design and validation, the resolution of conventional TDR is not sufficient to analyze vertical via effects in multilayer chip-carrier packages whose thicknesses are about 1mm. This proves especially true when the package design validation is performed as standalone, that is, without assembly of the package on an evaluation PCB.

To increase the resolution, the rise time needs to be decreased; however, this requires hardware reconfiguration in both the incident pulse generator and the sampling head of the reflected signal, which can be costly. Another option would be a software enhancement using normalization or a calibration algorithm to compensate for the loss due to cables and fixtures. However, this method is available only in certain TDR equipment and reveals limitation due to the fact that it boosts not only the signal level but also the noise level of the system. It was found that the special type of TDR equipment with a normalization scheme can make about 20–25ps rising time depending on microprobe pitch, when the ground-signal-ground (GSG)

configurations were used in the measurement setup.

A state of the art TDR with a rise time of 9ps was employed in the characterization of multilayer BGA/LGA packages, and its time waveforms were converted into frequency domain to validate its equivalent performance to 50GHz VNA [16]. Special hardware was used to reduce a standard TDR rise time of 20–40ps to 9ps. As for the sampling unit, a 70GHz bandwidth plug-in was used. It should be mentioned that the direct output waveform of 9ps module contains too much aberration and could not be directly applied to the DUT as-is. TDR equipment supports external single channel normalization that uses short and load calibration standards to remove systematic errors and provides sufficient accuracy in most cases. However, it does not support external dual-channel normalization that may be either a common or differential normalization. Here, only a single-channel time domain Short, Open, and Load (SOL) calibration algorithm [1] and single-port S-parameter computation software have been utilized. The calibrated step pulse resulting from the aforementioned algorithm provided 4-5 times higher resolution reflected signals than conventional TDR. The increased resolution clearly indicates the causes of multilayer package's signal integrity problems due to vias and planes, which cannot be observed with a conventional TDR.

9.3.1.1. Development of 9ps TDR Measurement Setup

Figure 9.29 shows 9ps TDR setup and probing solutions. As in VNA, the time domain TDR/TDT needs to be calibrated before actual DUT measurements to reduce systematical errors and uncertainties, due to fixtures and cables. The calibration of 9ps TDR has been computed in two ways: 1) direct convolution and 2) using SOL calibration. The direct convolution is done using

Equation 9.31

$$S_{11}(f) = \frac{V_{tdr} - V_{load}}{V_{load} - V_{short}}$$

where V_{tdr} , V_{short} and V_{load} are frequency domain data transformed from TDR reflected, short, and load standards' waveforms. Note that with subtracting the load waveform, a port calibration is accomplished. This is the simplified version of normalization without the digital filter and also the simplified version of a full one-port calibration when the source impedance matching term is zero. Another calibration is employed using the well-known calibration procedure for VNA, including the source impedance matching error term, and it is expected to provide better accuracy than the direct convolution method. Among the various calibration methods, we used SOL as our first attempt. Using the one port error model [16], we can

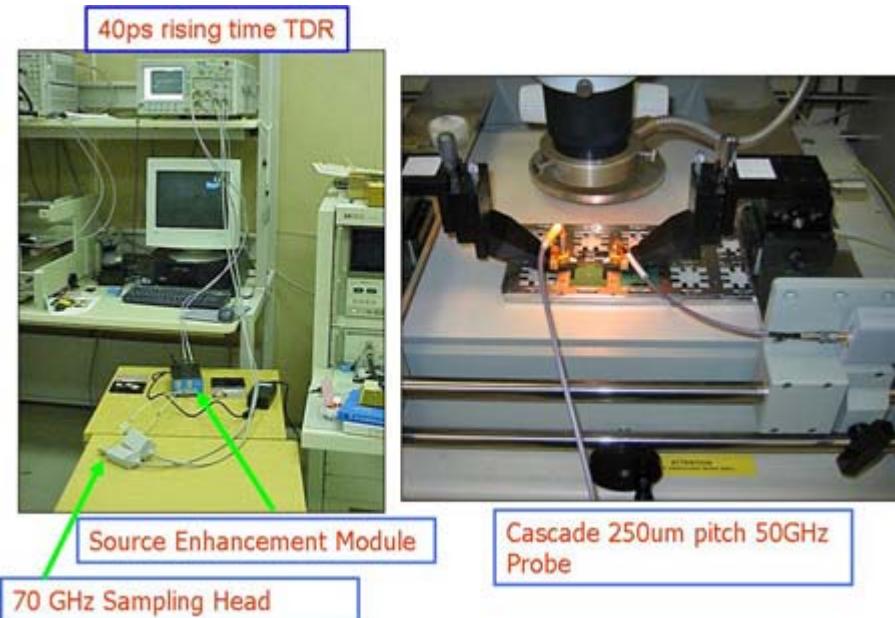
calculate S_{11} as

Equation 9.32

$$S11(f) = \frac{(V_{ldr} - E_D)}{E_S(V_{ldr} - E_D) + E_R}$$

Figure 9.29. 9ps TDR/T microprobing setup

Source: D.-H. Han, M. J. Choi, S. Gardiner, B.-S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.



Where the three error terms E_D , E_R and E_S can be solved from following equation

Equation 9.33

$$\begin{pmatrix} V_{short} \\ V_{load} \\ V_{open} \end{pmatrix} = \begin{pmatrix} 1 & S_{short}^{nor} & V_{short}S_{short}^{nor} \\ 1 & S_{load}^m & V_{load}S_{load}^{nor} \\ 1 & S_{open}^{nor} & V_{open}S_{open}^{nor} \end{pmatrix} \begin{pmatrix} E_D \\ E_R - E_D E_S \\ E_S \end{pmatrix}$$

where V_{short} , V_{load} , and V_{open} denote a short, load and open measured waveforms, S_{short} , S_{load} , and S_{open} are the S_{11} parameters for short, load and open standards.

The S-parameters of the calibration standards are assumed to be ideal,

resulting in $S_{\text{short}}^{\text{nor}} = -1$, $S_{\text{load}}^{\text{m}} = 0$ and $S_{\text{open}}^{\text{nor}} = +1$, respectively.

To calculate DFT of the sampled waveforms, the following equation is used [16]:

Equation 9.34

$$DFT(k) = \Delta t \cdot \left\{ FFT_N(k) + \frac{v_{N-1}}{1 - \exp(-j2\pi k/N)} \right\}, k=0, 1, \dots, N-1$$

Where Δt is the sampling interval, v_{N-1} is the last data value in the N -point equidistant time samples, and $FFT_N(k)$ denotes a N -point FFT calculation on this series. The frequency resolution is thus $\frac{1}{N\Delta t}$, which is in the GHz range for a typical sample length and sample rate. The DFT method given here actually specifies an estimate for the sample value outside of the time window to be equal to the last sample. Therefore, it requires that the sample time is long enough to reach a steady state.

9.3.1.2. Package Validation Using TDR

Typical design validation has been done using an evaluation PCB where a designed package is assembled. The measurements may be completed from the topside of the package to the short section of PCB trace escaped from the bottom of the package in terms of either TDR/TDT or S-parameters.

[Figure 9.30](#) shows a typical package stackup for a chip-carrier. Any signal path consists of a horizontal transmission line, typically located on a surface layer, and a vertical via transition whose physical length is less than 1mm. Signal integrity issues primarily arise due to the vertical via transitions consisting of long PTH vias, micro vias, and multilayers of conductors. To demonstrate this, 9ps TDR measurements were made for 50ohm and 70ohm microstrip lines and six vertical via transitions from the surface to bottom. [Figure 9.31](#) shows the surface layer where two microstrip lines of 58um and 26um widths and six vertical IO signal probing pads are placed. [Figure 9.32](#) is the collection of each layer snap-shot taken below the core layer. From the surface layer to the bottom core layer, all the antipad designs are identical. The signal channels 1 through 3 also identically differ from channel 4 through 6 in terms of antipad size. The different antipad designs result in different parasitic capacitance values exiting between signal paths and crossing planes.

Figure 9.30. A chip-carrier flip chip package

Source: D.-H. Han, M. J. Choi, S. Gardiner, B.-S. Xu, J. He, and C. Lee, “Realization of ultra-wideband high-resolution TDR for chip-carrier packages,” Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

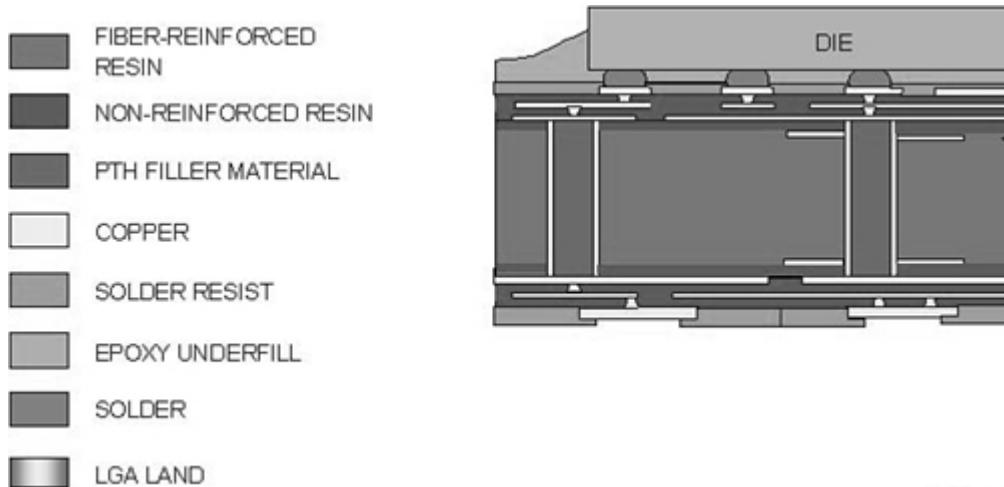


Figure 9.31. Topside view of six IO channel probing pads and two 7mm long microstrip lines (width of 58um and 26um)

Source: D.-H. Han, M. J. Choi, S. Gardiner, B.-S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

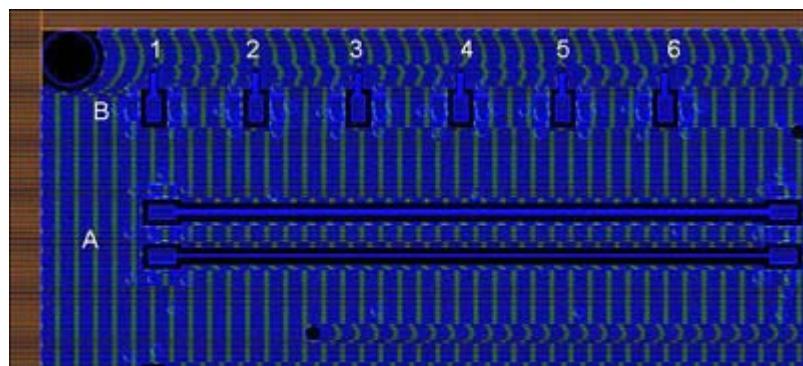


Figure 9.32. Snapshots of each layer view of six signals via transitions

Source: D.-H. Han, M. J. Choi, S. Gardiner, B.-S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

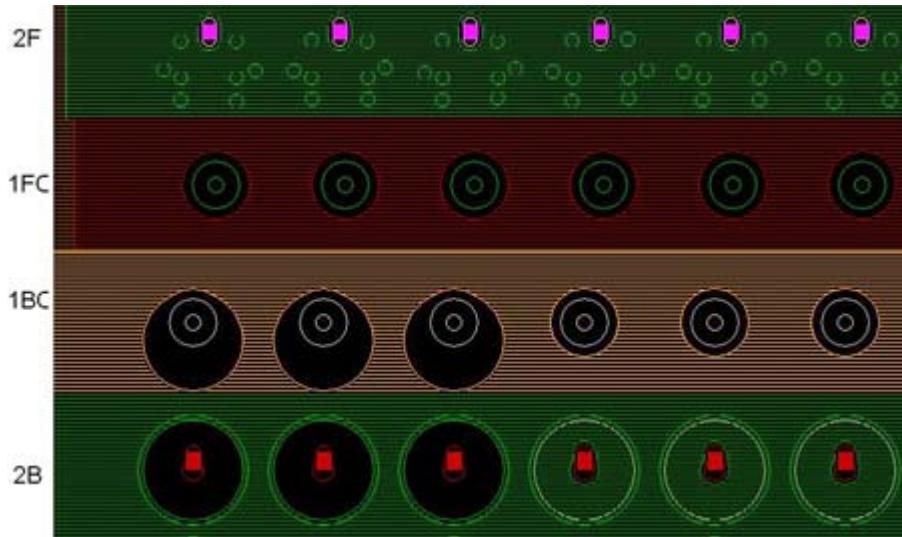


Figure 9.33 shows 9ps TDR waveforms for a 50ohm microstrip line and 68ohm microstrip line with other six vertical IO channels. If the source impedance is 50ohms and traces are routed with 58um microstrip lines, there would be no impedance mismatching on the surface layer. It is also interesting to observe that the microstrip impedance profiles are flat about 60ps duration, even though the trace length is 7mm long. Due to fast rising-time, open-end waveform does not impact much on the DUT, even if the DUT length is not long enough. On the other hand, due to open-end, for a shorter length DUT, a conventional TDR with a 30ps rising time would show increasing slope. It is not difficult to say that microstrip line impedance characterization structures do not need to be longer than 3-4mm (propagation time of $4 \times Tr$) if 9ps TDR is used to measure their characteristic impedances. As may be expected, signals denoted as channels 1–3 show almost the same impedance waveforms, but they clearly differ from channel 4–6 waveforms. Obviously, the larger antipads remove almost all the parasitic capacitances existing below core layers; resulting in better impedance matching. The signals denoted as channel 4–6 suffer impedance mismatching, due to two capacitances separating each other by a PTH inductance. The PTH impedance does not show any severe impedance mismatching; which means a thick core is not a bottleneck for high-speed IO signal path. From this study, it becomes clear that the root causes of impedance mismatching along the vertical via transition is due to parasitic capacitance that can be reduced by increasing the size of antipads or the distance between the signal and plane around the antipads. In this study, the antipad size has been increased. Note that the second dip (below the core) is larger in magnitude and wider than the first one indicating it is more capacitive. This indicates there is an additional parasitic capacitance after the PTH, and this might be caused by a geometrical mismatching from a micro-via to a large landing pad in the signal path itself.

Figure 9.33. 9ps TDR measurements of six IO signals and two microstrip lines

Source: D. H. Han, M. J. Choi, S. Gardiner, B. S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

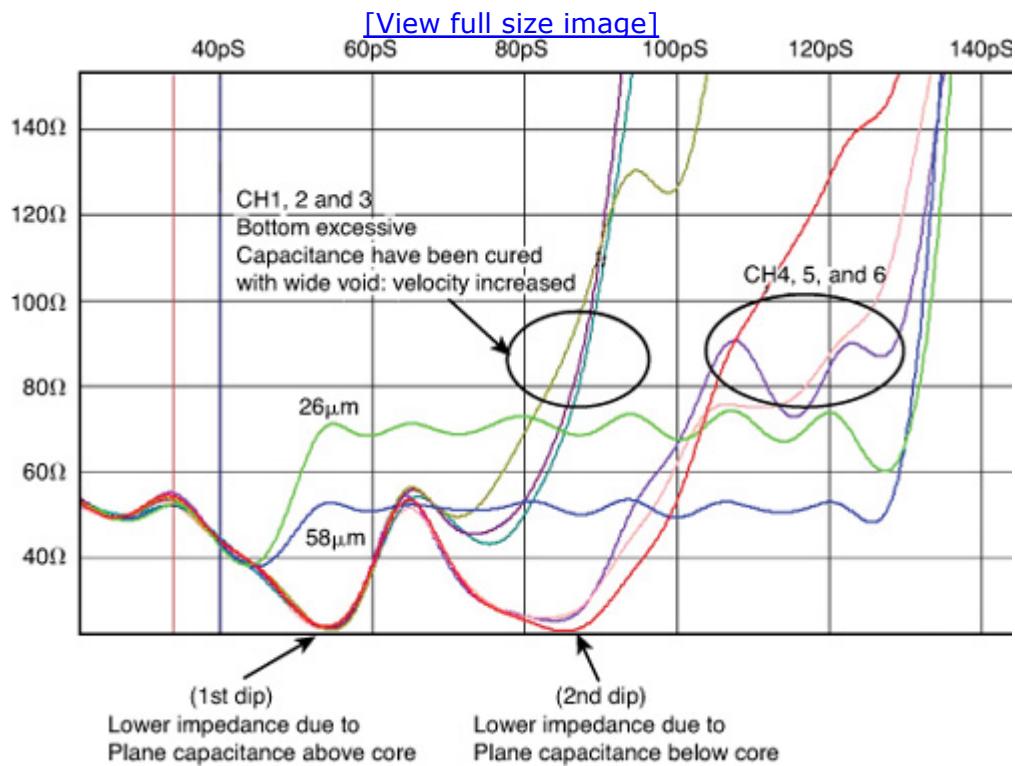
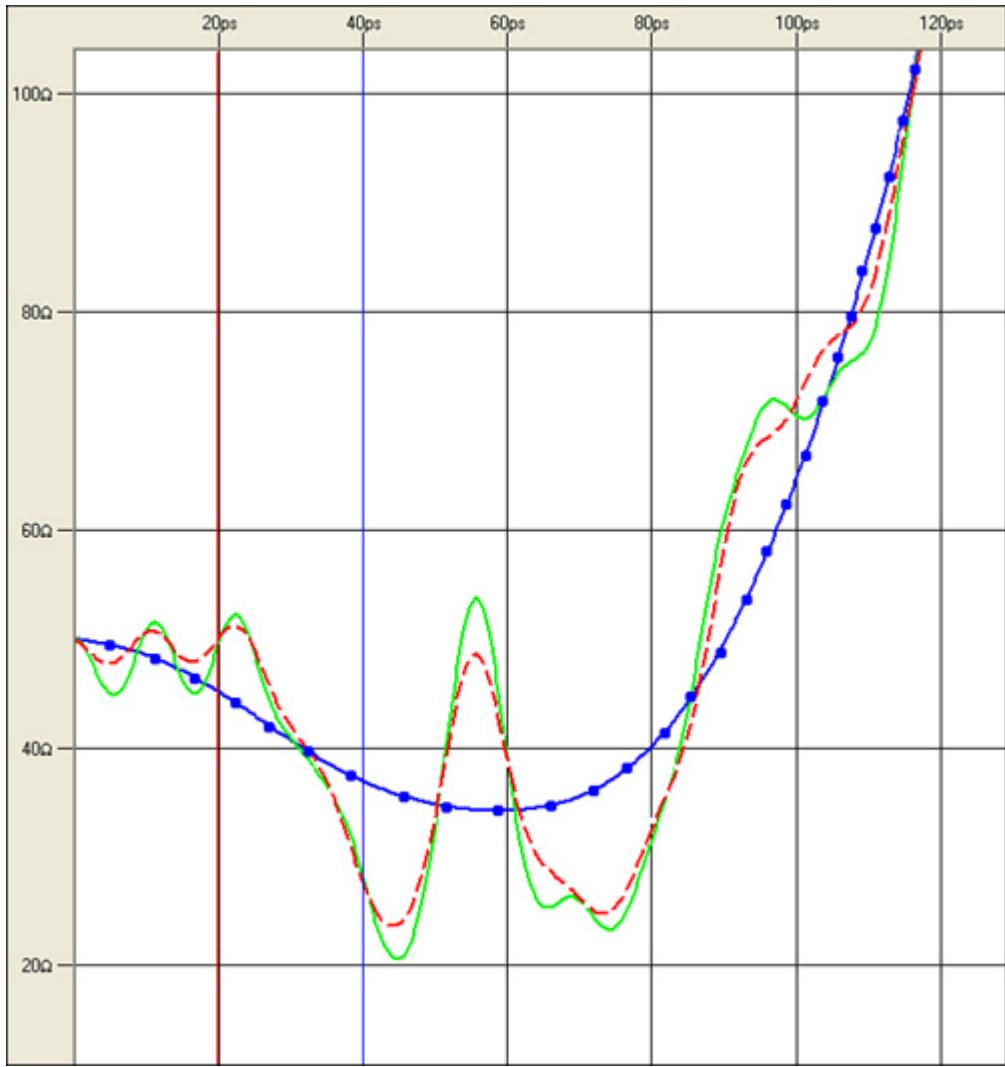


Figure 9.34 shows impedance waveforms of channel 4 with different rising times. The first curve is measured with 40ps, second with 11ps, and third with 9ps rising time. With a 40ps TDR signal, the package is seen as one capacitance; therefore, it is hard to identify PTH parasitic components. However, a 9pS TDR signal is fast enough to identify PTH parasitic components.

Figure 9.34. Impedance profiles using three different rising times: 9ps, 11ps (dotted), and 40ps (circles).

Source: D. H. Han, M. J. Choi, S. Gardiner, B. S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

[\[View full size image\]](#)



Using the developed SOL calibration algorithm, 9ps TDR waveforms were measured and transformed into the frequency domain for channel 3 reflected signal and calibration standards (open, short, and load). Figure 9.35 gives the measured TDR waveforms for channel 3 and accordingly the converted S_{11} data in comparison with VNA measurement up to 50GHz. The sampling interval was 244.14 fs and the total length was 1ns, which produces 4,096 samples. The converted S_{11} agrees extremely well with VNA measurement from DC to 50GHz. The difference between the two conversion methods is minute and occurs around 20GHz. Figure 9.36 demonstrates the TDR measurement and derived S_{11} for another signal channel (channel 4) which has more capacitive parasitic components along the path. The correlation with VNA measurement is good up to 10GHz whereas the calibration method shows closer agreement with VNA data than direct convolution.

Figure 9.35. 9ps TDR waveforms of channel 3 and S_{11} comparisons

Source: D.-H. Han, M. J. Choi, S. Gardiner, B. S. Xu, J. He, and C. Lee, “Realization of ultra-

wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

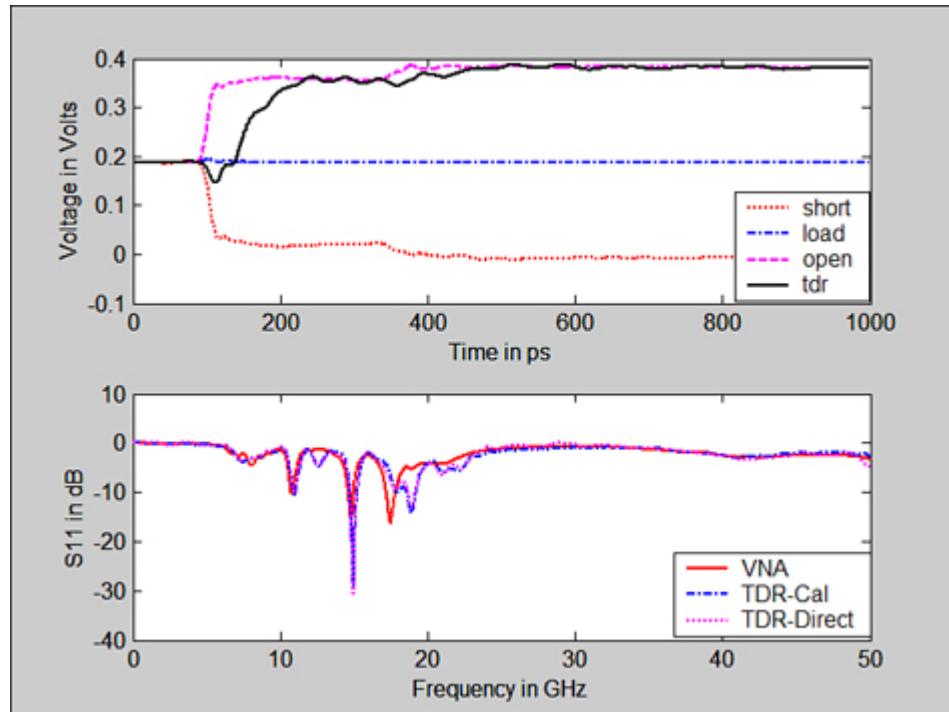
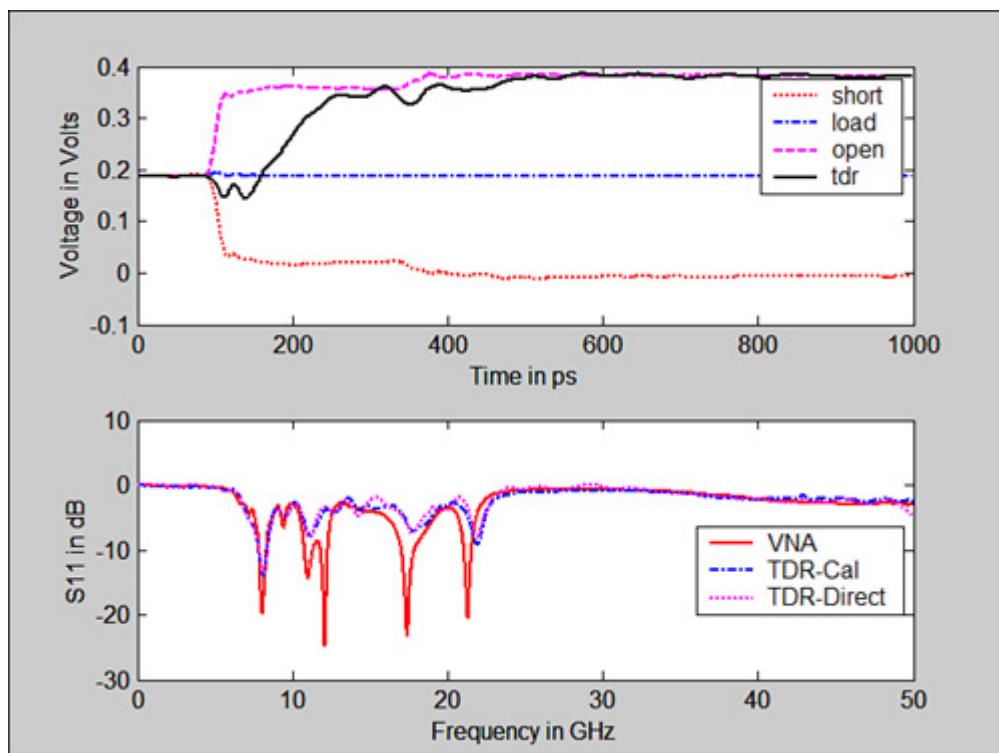


Figure 9.36. 9ps TDR waveforms of channel 4 and S11 comparisons

Source: D. H. Han, M. J. Choi, S. Gardiner, B. S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.



Because the faster TDR instrument is pushing the limit of the signal level close to the noise level of the system, several aspects deserve special care in practical TDR measurements. It is desirable to collect the TDR and TDT waveforms and the short/open/load waveforms at one measurement setup and in short-time because, in general, the sampling scope's long time stability is found to be much worse than that of the VNA. The long-time instability of the TDR instrument causes voltage drift and time base wander that may produce errors, which are difficult to compensate later. The user needs to balance the horizontal scale with the sample length to allow the beginning and ending part of the sampled waveform to be settled. It is preferred to keep the same position and vertical scale while capturing all the TDR/TDT, the short/open/load/through, waveforms. Adjusting the vertical scale to nearly a full range will obtain the best signal-to-noise ratio. Averaging can help reduce random noise in the vertical scale but excessive averaging will make the capturing procedure too long to obtain a timing error accumulated; 256-point averaging is selected as the trade-off in this work. Time domain comparison is shown in [Figure 9.37](#) and [Figure 9.38](#) for channel 3 and channel 4, respectively. The rising edge correlates quite well, whereas some part after the rising edge reveals some differences. This corresponds to the better correlation at a high frequency; compared to that at the middle frequency of the measured bandwidth, as [Figure 9.35](#) and [Figure 9.36](#) show.

Figure 9.37. 9ps TDR waveforms of channel 4 and S11 comparisons

Source: D.-H. Han, M. J. Choi, S. Gardiner, B. S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.

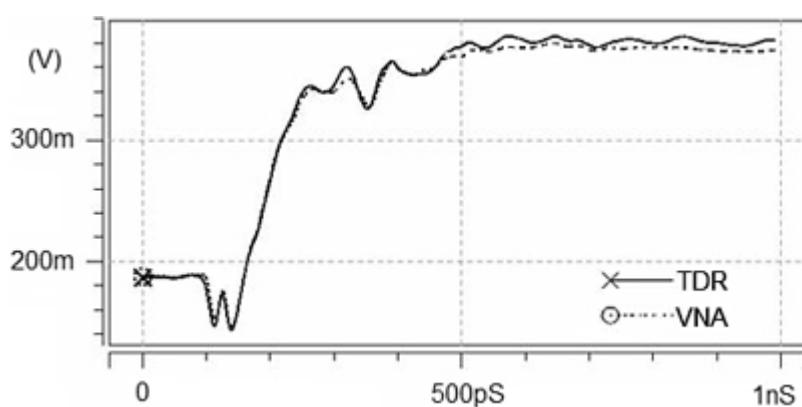
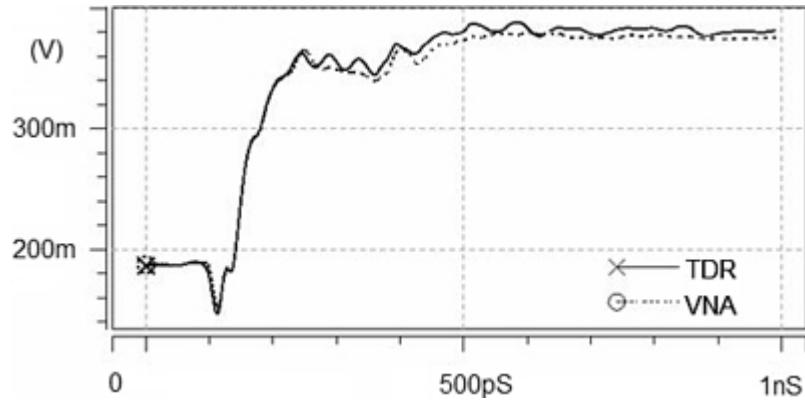


Figure 9.38. 9ps TDR waveforms of channel 4 and S11 comparisons

Source: D.-H. Han, M. J. Choi, S. Gardiner, B. S. Xu, J. He, and C. Lee, "Realization of ultra-wideband high-resolution TDR for chip-carrier packages," Ipack2005-73291, Proceedings of Ipack 2005 © [2005] ASME.



9.3.1.3. Differential TDR and TDT

Driving the two transmission lines by single-ended signals that are exactly out-of-phase is called differential driving. Differential signaling links have been widely used to achieve higher noise immunity for multi-GHz I/O interfaces. From even/odd measurements, using a differential TDR/TDT instrument, we can extract differential and common mode impedance and propagation delay to describe differential transmission line behavior.

Differential impedance consists of the impedance measured between two conductors driven differentially, whereas the odd mode impedance constitutes the impedance of a single conductor in a differential pair. The even mode impedance is the impedance of either conductor when the differential pair is driven with identical, same-polarity signals. Common mode impedance is the impedance of the two conductors in a differential pair, when both conductors are driven with a single common mode signal, relative to ground. The differential impedance is twice the value of the odd mode impedance, and the even mode is twice the common mode value. If the common mode impedance is much lower than the differential impedance, the common mode rejection will be high. In the case of no coupling between the lines in the differential pair, both even- and odd-mode impedances approach the single-ended characteristic impedance of each line [17].

9.3.2. PDN Noise Measurement

PDN noise is also known as supply noise. As Chapter 6, "Time Domain Analysis," discusses, there is a specific design target for the PDN noise at the chip or die. It is especially difficult to measure the die by itself because no physical terminal exists for the measurement. When the on-chip noise travels to the package or the PCB, it becomes significantly modified. There may be capacitors on the package that can filter out the noise at higher frequencies. Also, there may be unwanted PDN resonances on the package and PCB, so at the measuring point, the noise may be altered significantly.

PDN noise measurements are performed with an oscilloscope [10], and the

bandwidth of measurement plays an important role. [Chapter 5](#), “Frequency Domain Analysis,” shows the frequency impact for on-chip PDN, package PDN, and PCB PDN. The PDN noise measurements may be performed on the PCB with low bandwidth ($\sim 20\text{MHz}$), because the PCB PDN may affect only the low frequencies, and the noise coming from the chip may be filtered out before it reaches the PCB PDN. If the high-frequency noise is measured on the PCB, it needs to be properly calibrated, considering the PDN response at the measurement point of the PCB. For the high frequency PDN noise measurement, the bandwidth may be at least three times that of the maximum clock frequency for the interface. Proper interconnecting elements need to be connected for high-frequency measurements, because the parasitics of those elements might skew the results. Power consumption due to the PDN needs to be noted, and a DC block might be necessary to protect the oscilloscope. Many oscilloscopes have FFT functionality, which may be used to interpret the frequency contents of the noise. [Figure 6.20](#) shows an example of the FFT display of the waveform.

For the logic and internal circuits, the noise is internal to the chip and no transmission line is involved. The noise travels from chip to package and from package to the PCB. Typically, that PDN does not serve as a reference of the signals. For the final stage of I/O interface, PDN serves as the reference to the signals on the package and on the PCB. Due to resonances of the PCB PDN, the noise coming from the chip and package may be amplified. In that case, high frequency noise measurement may be required. In general, the noise measured on the PCB may differ from its source on the chip, especially at high frequencies. However, high-frequency noise measurement on the PCB proves helpful in determining unwanted resonance coupling and EMI impacts.

As [Chapter 6](#) discusses, for single-ended or differential interface, the worst-case loading condition is determined. The I/O interface is exercised with that loading condition. The generated noise at an on-chip power network needs to be quantified in the lab. Various ways with which the on-chip or on-die noise can be measured, including the following:

- **Special on-die circuits:** Special on-die circuits like on-die droop detector as described in [\[11, 12, 13\]](#) are designed to detect the on-die noise. For designing such circuits, bandwidth of the noise is considered to be an important parameter. Some types of circuits can detect the peak noise, and other types can reproduce the time domain waveform.
- **Picoprobing:** Special silicon needs to be fabricated so as to have inner metal on-die points that can be measured with the picoprobe [\[14\]](#). Picoprobes are tiny RF probes that connect to the special silicon so the on-die noise measurements can be completed. In [Chapter 6](#), picoprobing results were obtained for the SSO type of noise measurements, as shown in [Figure 6.20](#). The measurement frequency is limited by capacitance, so low-capacitance probes need to be used

for high-frequency measurements.

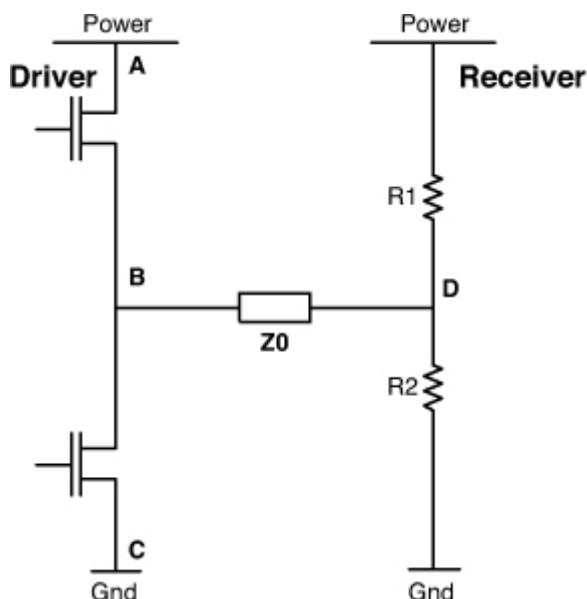
In the fabrication of special silicon, it may or may not be possible to obtain the nearby power and ground terminals. The power terminal and ground terminal may be electrically away. This may result in inaccurate measurements of the on-die noise. Also, the yield of such samples may be low, so good quality samples may not be available for measurements.

- **On-package measurement:** Another alternative is to measure the on-die noise when it travels to the package. In this scenario, special bumps are designed for the package, and these bumps do not connect to the PCB. These bumps are power and ground bumps for which the noise needs to be measured.

The measurement is completed on these bumps, and de-embedding is done from the bump to the buffer to obtain the noise at the power nets of the buffer. Another option is to measure it on the package decoupling capacitor location near the chip.

- **PCB PDN measurements:** As mentioned earlier, PDN noise on the PCB may be different than that on the chip itself. However, special techniques are used to measure PDN noise on the PCB and to project it at the chip or die. For a single-ended interface, driver side on-chip PDN noise may be measured at the PCB (receiver). [Figure 9.39](#) shows the single-ended driver and the terminations at the receiver[15]. The noise at the power/ground nodes of the driver (point A-C) may be measured at the receiver. When all the bits at the interface are switching, the on-chip SSO is coupled through the Ron and receiver terminations.

Figure 9.39. Single-ended driver with terminations



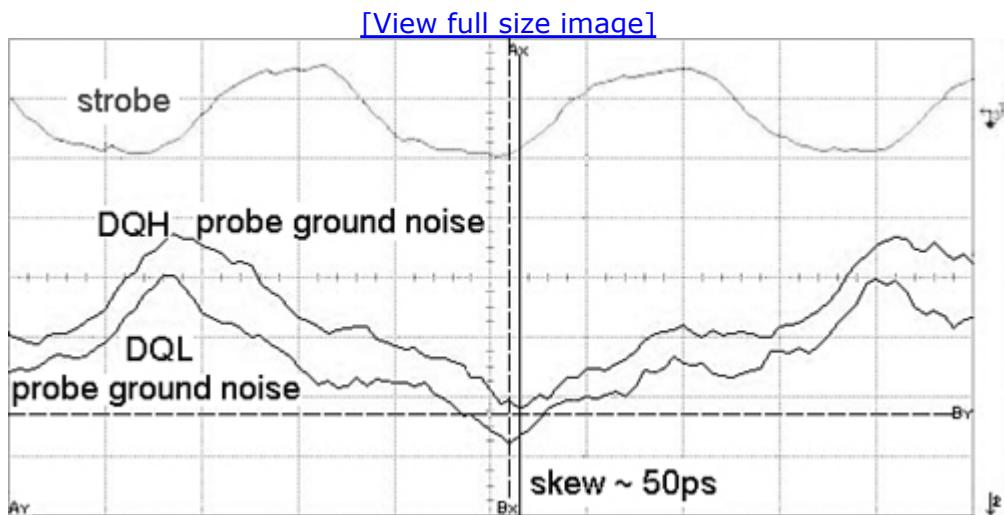
Two adjacent DQ bits are used for the measurements: DQH and DQL. The

concept in this instance is that one bit is held high and the other held low. The delta noise at the receiver node D for these two bits is measured. This noise corresponds to the power/ground noise at the driver.

When all other bits are switching simultaneously, it is ensured that the two DQ bits (DQH and DQL) have identical noise on the power and ground. To confirm that, both the bits DQH and DQL are held low. When a bit is held low, referring to [Figure 9.39](#), the noise at the ground node C of the driver appears at point D. There is some skew in between the DQH and DQL bits when both are held low, as shown in [Figure 9.40](#). With this, the waveforms may be phase-aligned before performing DQH-DQL measurements.

Figure 9.40. Calibration method

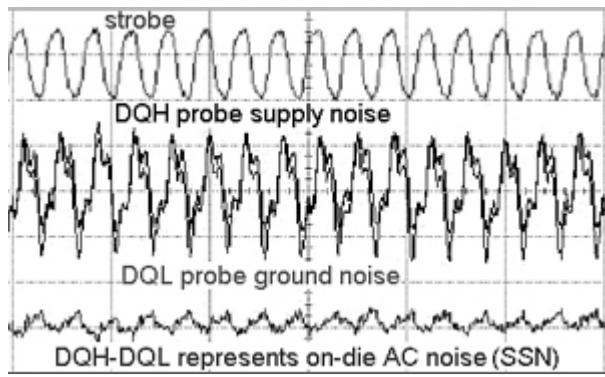
Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



Next, the DQH probe is held high. Referring to [Figure 9.39](#), the noise at the power node A appears at point D. Now, DQH line is held high and DQL held low. [Figure 9.41](#) shows the DQH noise, DQL noise, and the DQH-DQL delta noise.

Figure 9.41. DQH-DQL measured noise with 1010 data pattern

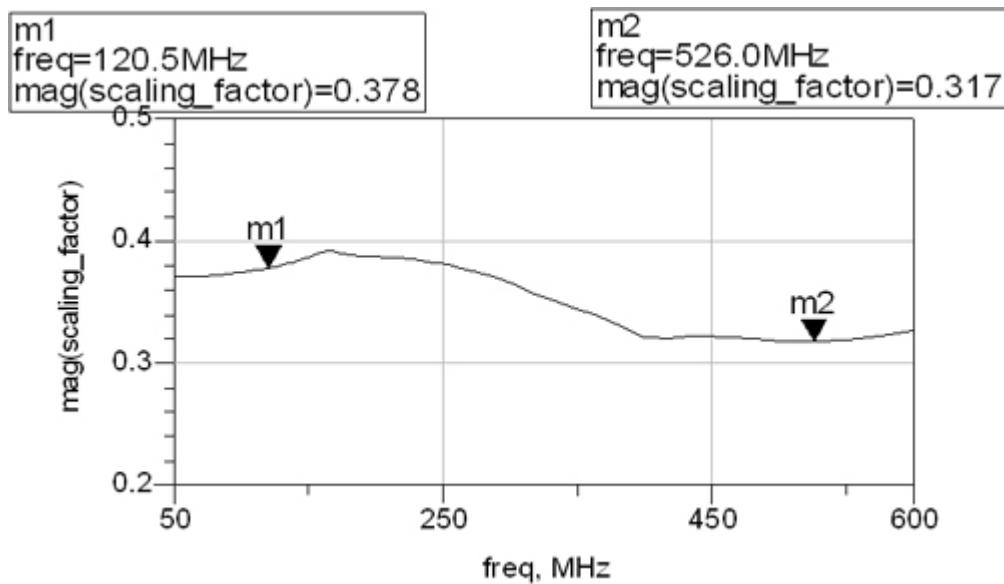
Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



The switching data lines have a 1010 pattern with maximum MTPS data rate. The delta noise has a maximum frequency component. This delta noise is measured at D, so the transfer function from point A to D needs to be determined. Various components in the system from point A to D exist, like R_{on} , transmission lines, and connectors. The losses due to these are calibrated out. [Figure 9.42](#) shows the voltage transfer function in a frequency domain from point A to point D.

Figure 9.42. Transfer function for determining on-chip noise

Source: V. Pandit, A. N. Pardiwala, Hsiao-ching Chuang, M. J. Choi, and Md. R. Quddus, “SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity,” DesignCon 2009.



This transfer function is applied to measured noise at point D, and the projected noise at the driver (V_{A-C}) is plotted. Similarly, the process is repeated for other frequency points. [Figure 6.22](#) in Chapter 6 shows resultant noise from the DQH-DQL method.

This DQH-DQL method is specifically for the driver for the single-ended interface, as shown in [Figure 9.39](#). For a differential interface, a similar method may be used, based on the topology of the driver, as shown in

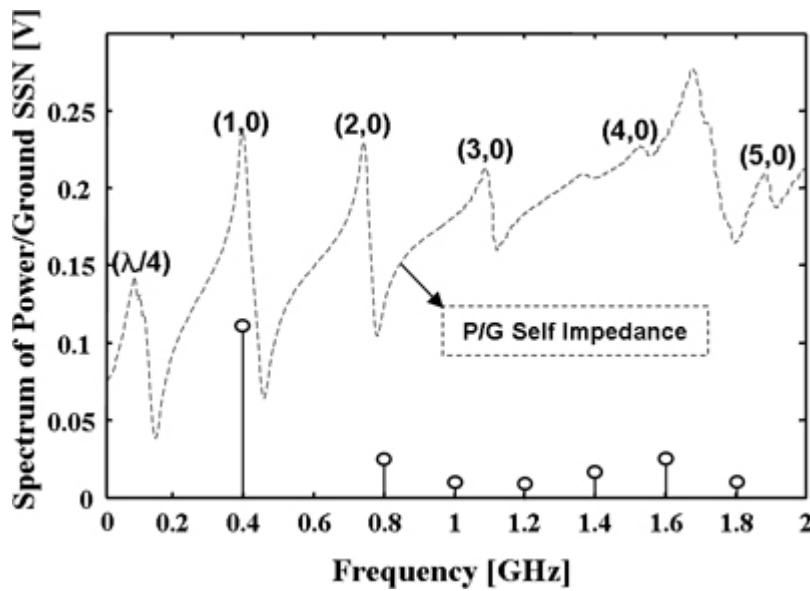
reference [18].

9.3.3. SSO Coupling Measurement in Time Domain

To characterize the time domain SSO coupling effect of the test vehicle, shown in [Figure 9.21](#) and [Figure 9.22](#), the measurement for clock signal was done with an oscilloscope and pulse pattern generator. The clock driver chip consumes about 200mA current with 200MHz frequency and generates SSO. The SSO is about 600mV and dominant at 400MHz because the second harmonic of the frequency consuming the current from the power and ground plane encounters with the power/ground cavity resonance mode $\text{TM}(1, 0)$, which is at 400MHz. [Figure 9.43](#) shows the spectrum of the measured SSO and the power/ground self impedance at the center of clock driver chip. The generated SSO is dominant at 400MHz because the second harmonic of the frequency consuming current from power/ground encounters with the power/ground cavity resonance mode $\text{TM}(1, 0)$, which is at 400MHz.

Figure 9.43. Spectrum of the measured SSO and the cavity resonance modes power/ground self-impedance at the center of the SSO generating chip

Source: J. Park, et al, “Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module,” Proceeding of EMC 2004 © [2004] IEEE.

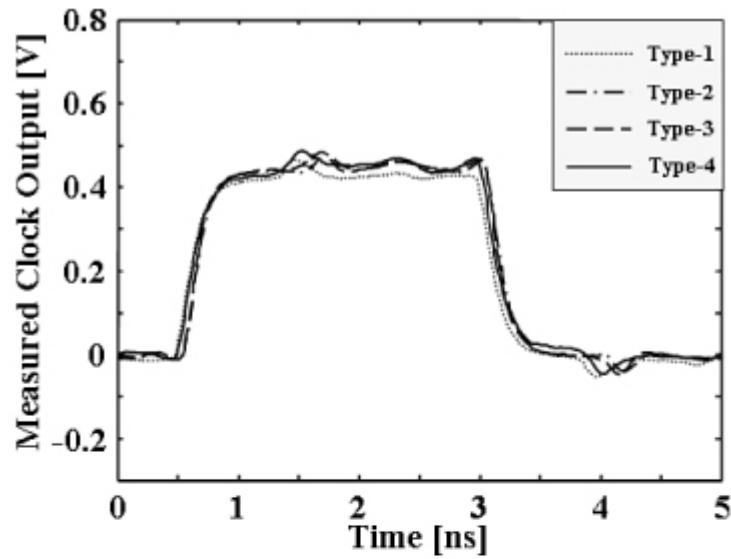


A 200-MHz clock with a 500mV peak to peak is used to compare the four different signal line structures, as shown in [Figure 9.21](#) and [Figure 9.22](#). When no SSO exists, the output clock waveforms for the four different signal line structures are as shown in [Figure 9.44 \(a\)](#). No difference for line structures exists. Their spectrums possess odd harmonics for ideal clock, with the half of duty cycle, as shown in [Figure 9.44 \(b\)](#). However, when a

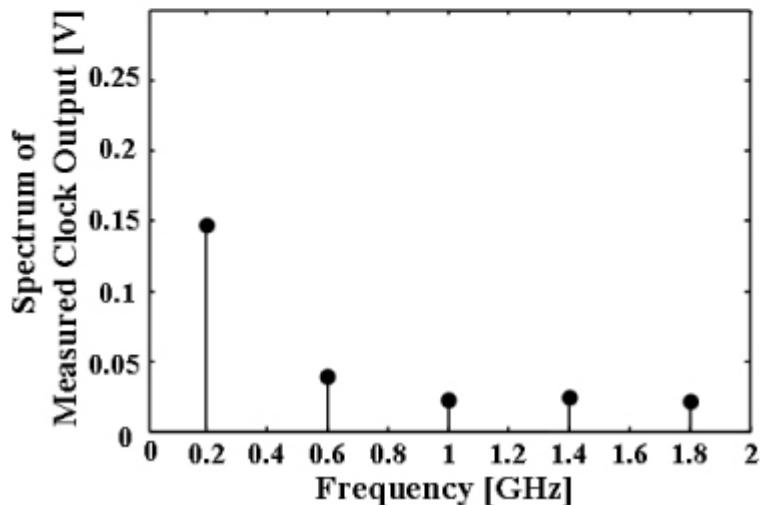
600mV SSO noise exists between power/ground planes, the output waveforms for the four different signal line patterns are differently distorted, as shown in Figure 9.45 (a). Figure 9.45 (b) shows spectrums to analyze the cause of distortion. As mentioned earlier, there are two SSO coupling mechanisms: first through the reference changing via, and the second is SSO coupling to signal through the trace between power and ground plane. It is shown that the 400MHz element, which is the dominant element of the SSO, is added on the spectrum of the ideal clock signal. Type-3, which is the power referenced strip line, has the highest 400MHz element because it is coupled by both the first and second SSO coupling mechanism. Nevertheless, the 400MHz element of Type-4 has almost the same amount as that of Type-3, due to reference transition, which is the dominant factor to couple the SSO. However, Type-1 and Type-2, without reference transition, have little SSO coupling to signal line.

Figure 9.44. Signaling with no SSO noise (a) output clock waveforms and (b) output clock spectrum of 200MHz input clock signal with 500 mV peak to peak, when there is no SSO

Source: J. Park, et al, "Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module," Proceeding of EMC 2004 © [2004] IEEE.



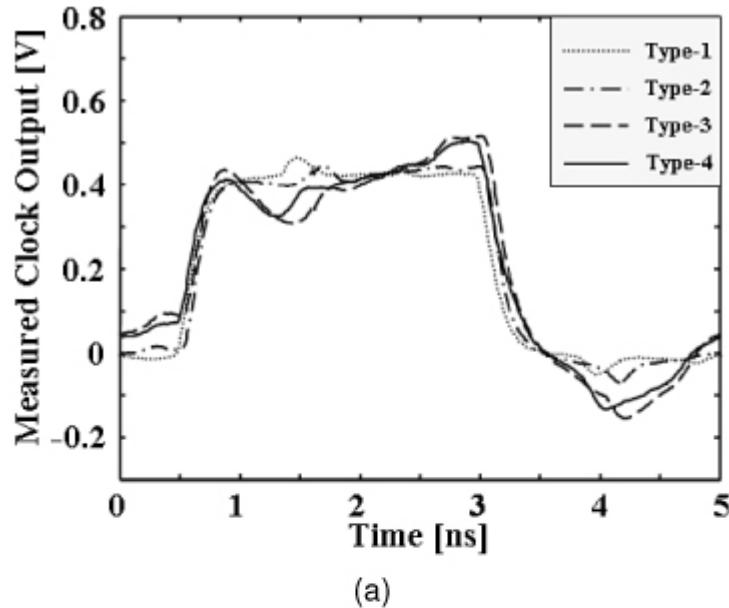
(a)



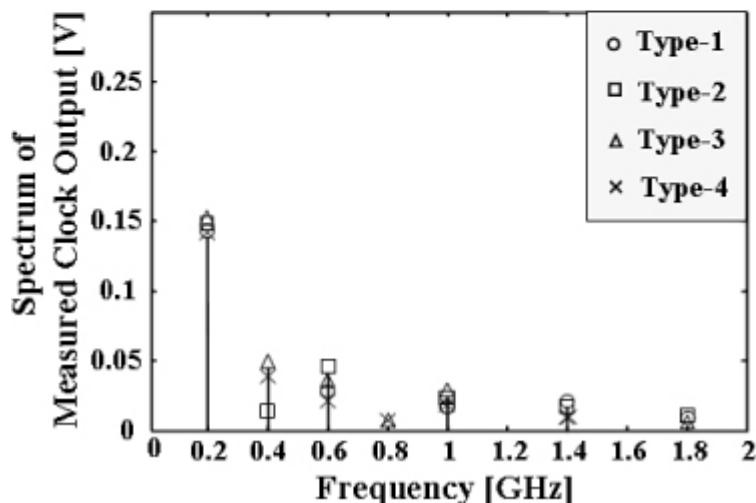
(b)

Figure 9.45. SSO noise coupling effect (a) output clock waveforms and (b) output clock spectrum of 200MHz input clock signal with 500 mV peak to peak, when a 600 mV SSO exists

Source: J. Park, et al, "Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module," Proceeding of EMC 2004 © [2004] IEEE.



(a)



(b)

As previously mentioned, the power referenced microstrip line and power referenced strip line with reference changing via are most sensitive to SSO coupling. However, to change a reference plane is inevitable to effectively route many data or command lines in memory module. To mitigate SSO noise coupling to signal trace, it is recommended to place stitching vias or capacitors at the position with low power/ground cavity impedance as described in [Chapter 7](#).

9.3.4. Jitter Measurement

Jitter, an important measure, must be modeled accurately in system budgeting. In measurement, jitter is measured with a real-time oscilloscope. For a single-ended system, [Chapter 6](#) shows examples of supply noise induced jitter. For a source synchronous single ended system, there is data DQ and strobe DQS. Measuring individual jitter of DQ or DQS, it is triggered on the system clock for that interface. Although the clock may

have jitter, the overall jitter level of the clock may be lower than that for DQ or DQS. [Figure 6.34](#) shows DQ jitter when triggered on the clock. If the window margin is required to be determined, the DQ is triggered on the DQS. [Figure 6.37](#) shows an example of the DQ jitter when triggered on the DQS.

As [Chapter 6](#) describes, different elements of the total jitter exist, such as random and deterministic. For a differential interface, if the separate clock is not sent along with the data, it is a nonsource synchronous interface. The clock, embedded in the data, has to be recovered at the receiver. Jitter requirements for such a system are more stringent compared to those for source-synchronous system. A differential interface is expected to have a certain bit error rate (BER) and can be measured with the BER tester. Eye diagrams can be obtained using an oscilloscope for the differential signals at the receiver. The relationship between the eye margin and the BER needs to be established, and different components of the jitter need to be determined. More details of the jitter for high-speed links, including the statistical approach can be found in references [19, 20, 21]. Signal integrity impact along with power integrity impact on jitter is described in [Chapter 8](#), "Signal/Power Integrity Co-Analysis." It illustrates that due to the SSO impact, there is a nonlinear modulation on the signal pad of the corresponding victim buffer, which is another source of jitter. As the system budget gets tighter it is necessary to include jitters from various noise sources such as SSO, ISI, crosstalk, and combinations thereof. Advanced computational capability facilitates modeling of these sources and interactions between them. Measurement of jitter of the active system has also been improving with the advancement in the equipment and the computational algorithm.

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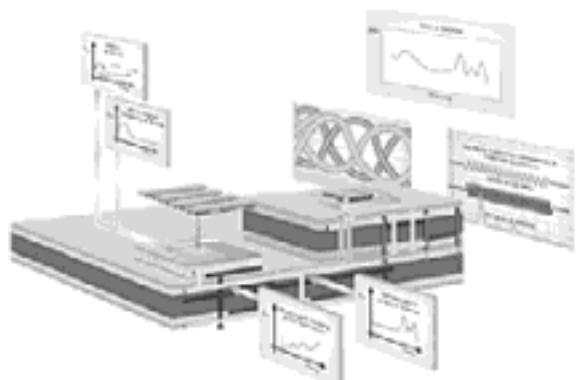
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PRENTICE
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With Signal Integrity/Power Integrity Co-Design

Foreword by Joongho Kim

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