A Fast-Lock All-Digital PLL with a TDC-based FLL

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Abstract— **This paper presents a fast-lock all-digital phase-locked loop (PLL) for double-data rate (DDR) interface and zero-delay buffer applications. The proposed PLL utilizes a new time-to-digital converter (TDC)-based frequency-locked loop (FLL) to achieve a fast lock time. Implemented in a 40-nm 1.1V CMOS process, the proposed PLL achieves an operating frequency range of 1.5–3.2 GHz. It achieves a frequency lock time of approximately 100 ns and a phase lock of 310 ns or less. The simulated RMS jitter is 0.87 ps at 2.7 GHz. It occupies a core area of only 0.0345 mm^2 and consumes a power of 6.2 mW at 2.7 GHz.**

Keywords; RCD, PLL, TDC, FLL, DLL

I. INTRODUCTION

A registering clock driver (RCD) [1] is an electronic component that distributes clock signals to various DDR4 and DDR5 memory modules and subsystems in a computer or electronic system, ensuring synchronized and minimal skew signals. The RCD market is growing rapidly due to the rising demand for high-performance computing systems and data centers, which require efficient clock distribution networks. RCDs are essential for precise and reliable clock distribution in these systems. A key technical element in RCD technology is the design of fast-lock phase-locked loops (PLLs).

PLLs are being adopted over delay-locked loops (DLLs) for clock generation in RCDs that do not require frequency multiplication [2]. This is due to PLLs' ability to filter jitter effectively through their limited loop bandwidth, a critical feature for RCD applications. Unlike DLLs, which have all-pass jitter transfer characteristics, PLLs offer essential jitter suppression for stable and reliable clock distribution, particularly in I/O interface systems where there is latency mismatch between the clock and data paths [3]. In addition, the fast-lock feature allows the PLL to quickly achieve phase and frequency lock with the reference clock, reducing the time it takes to stabilize the clock signal after power-up or frequency changes. However, [2] does not address the fast-lock function.

This paper presents a novel fast-lock all-digital PLL (ADPLL) for RCD applications. The ADPLL employs a new time-to-digital converter (TDC)-based FLL to achieve rapid lock times. Implemented in a 40-nm 1.1V CMOS process, the ADPLL operates within a frequency range of 1.5 to 3.2 GHz. It achieves frequency and phase lock within 310 ns. Post-layout simulations indicate an RMS jitter of 0.87 ps, with a power consumption of 6.2 mW at 2.7 GHz.

II. PROPOSED ADPLL ARCHITECTURE

Fig.1 shows the block diagram of the proposed ADPLL. It consists of a bang bang phase detector (BBPD), a main digital loop filter (Main_DLF), a frequency-locked loop DLF (FLL_DLF), a digitally controlled oscillator (DCO), a 1/32 divider, a 2-to-1 multiplexer (MUX), and a TDC-based FLL. The FLL consists of a MUX, a D flip-flop, cyclic Vernier TDC, two registers (A and B), a 9-bit comparator, and a FLL controller.

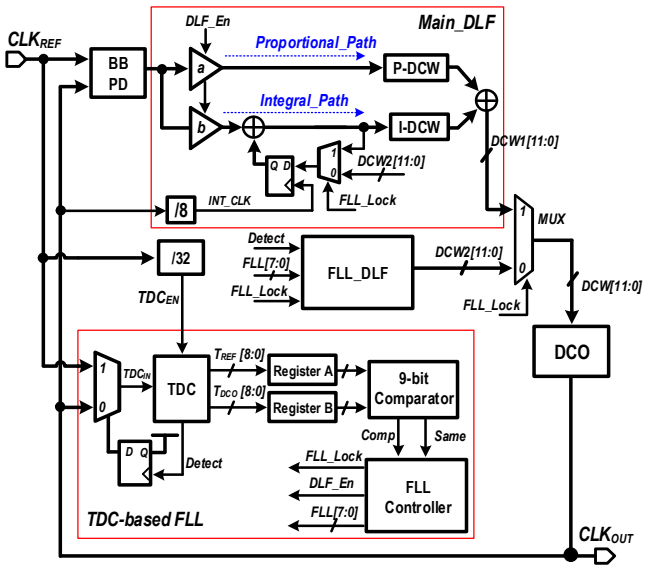

Fig. 1. Block diagram of the proposed ADPLL

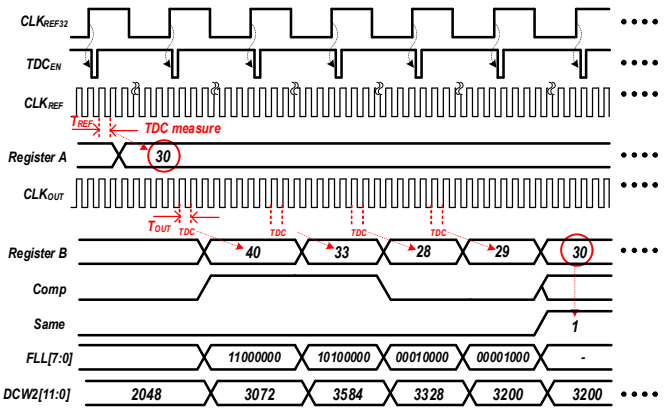

Fig. 2. Frequency locking process of the proposed TDC-based FLL

Fig.2 shows the frequency locking process of the proposed TDC-based FLL. When the TDC_{EN} signal is enabled, the period of the reference clock (= T_{REF}) is measured by the cyclic-Vernier TDC [4] and stored in the register A. Then, when the TDC_{EN} signal is activated repeatedly, the TDC measures the period of the output clock (= T_{OUT}) and stores it in the register B. The 9-bit comparator compares the values of

register A and register B, adjusting the FLL[7:0] control signal of the FLL_DLF using a successive approximation register (SAR)-controlled binary search algorithm until the values match and the "Same" signal is asserted. At the start of PLL operation, the DCW2[11:0] value initializes at the midpoint and is directly applied to DCW[11:0], the DCO control signal, enabling rapid frequency lock completion.

Once frequency locking is achieved and the FLL_Lock and DLF_EN signals are activated, the TDC-based FLL is disabled. The system then switches to phase locking mode, where the BBPD and the Main_DLF become operational.

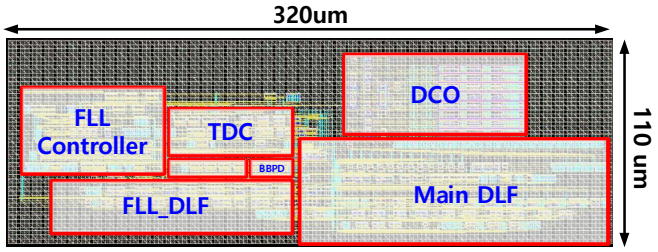

Fig. 3. Chip layout of the proposed ADPLL

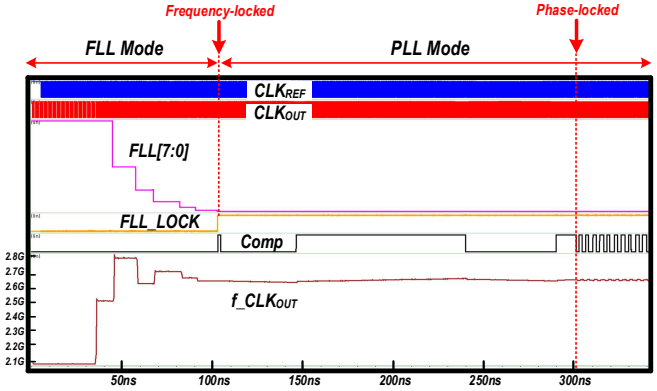

Fig. 4. Post-layout simulated locking process of the ADPLL at 2.7 GHz

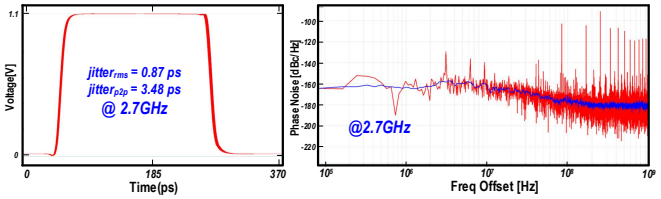

Fig. 5. Post-layout simulated jitter and phase noise simulation results at 2.7 GHz

III. Experiments Results

The proposed ADPLL is implemented in a 40nm 1.1-V CMOS process. Fig. 3 shows the layout of the proposed ADPLL with an active area of only 0.0345 mm^2. Fig. 4 displays the post-layout simulated locking process of the ADPLL at 2.7 GHz. The TDC-based FLL achieves frequency lock within approximately 100 ns. Subsequently, the system transitions to operate as a digital bang-bang PLL, achieving phase lock with a total lock time of approximately 310 ns. Fig. 5 shows the post-layout simulated jitter and phase noise performance at 2.7 GHz. The proposed PLL achieves a peak-to-peak (p-p) and an RMS jitter of 3.48 ps and 0.87 ps, respectively. Table 1 provides a performance comparison between the proposed ADPLL and other digital PLLs with high loop bandwidth.

IV. Conclusion

In this paper, a fast-lock all-digital PLL designed for DDR4/DDR5 RCD applications is introduced. The proposed all-digital PLL incorporates an innovative TDC-based FLL to achieve a rapid frequency lock time of just 100 ns, contributing to a total lock time of under 310 ns. Implemented in a 40-nm CMOS process, the PLL operates with a power consumption of only 6.2 mW at 2.7 GHz and supports a frequency range of 1.5–3.2 GHz. The simulated RMS jitter at 2.7 GHz is only 0.87 ps.

TABLE I. Performance Comparison

	[2]	[5]	[6]	This work*
Process [nm]	28	65	28	40
Supply [v]	1.1	1.3	1.0	1.1
Output freq. (GHz)	1.05–3.2	3.35–5.6	3.25–6.25	1.5–3.2
RMS jitter (ps)	0.27	1.8	1.15	0.87
Power (mW)	12.1	22.5	21.23	6.2
Lock time (µs)	-	2.19	1.5	0.31

* Post-layout simulation results

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