Time-to-Digital Converters: A Literature Review and New Perspectives

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***Abstract*—Time measurements with time resolution achieving picosecond accuracy are required in many fields such as high-energy physics, satellite positioning, or medical imaging. Time-to-digital converters (TDCs) are widely used for this purpose. In addition to accuracy, a high dynamic range and a good linearity are often requested for most applications. This paper presents a state-of-the-art of the recent CMOS structures of TDCs. Furthermore, usual key performance metrics are described in order to compare and to study TDCs.**

***Index Terms*—Time-to-digital converter, time precision, coarse-fine measurements, self-timed ring.**

I. Introduction

Time measurement between two events is a key technique used in many fields such as high-energy physics, time-of-flight measurement, instrumentation and satellite positioning [1]–[4]. Devices called time-to-digital converters (TDCs) are widely used for precise time measurement. The time interval T to be measured is generally defined with a *Start* signal, which indicates its beginning, and a *Stop* signal, which points the end. The time conversion into a digital word facilitates the data processing and its integration in digital systems. Such an approach takes advantage of reduced die area, power and functional complexity. Moreover, TDCs can easily be integrated on-chip in CMOS technology.

The first generation of TDCs was based on analog techniques. They have been designed to enhance the previous technique initially developed for time measurement based on the time-to-amplitude converters (TAC) [5], [6]. Recently, fully digital approaches are mostly used for time measurement. The simplest architecture of TDC is based on a timer counting the number of edges of a reference clock signal. The precision depends on the timer resolution (sampling step) by which the measurement is performed. This can be carried out by low-power and compact circuits.

Many TDC principles, which deal with time resolution improvement, have been proposed in the literature as second generation of TDCs. In the simplest TDC architectures, the time resolution is bounded by a CMOS gate delay. In order to overcome this technological limitation, sub-gate delay resolution solutions have also been proposed [7]–[10], which correspond to the TDC third generation. As a wide dynamic range of time measurement is required in many applications, dedicated architectures have been proposed, such as using an interpolation scheme or multi-quantization levels to achieve wide measurement ranges with fine time resolutions [11]. Nevertheless, while many of the proposed TDC architectures in the literature can achieve high measurement accuracy, they often require repetitive measurements. Therefore, on-the-fly measurements on fast non-periodic signals are challenging in TDC designs.

This paper provides a literature review of the main used architectures of TDCs including our new proposed TDC architecture [12], [13]. In addition, key performance metrics are given in order to analyze the TDC performances. The paper is organized as follows. The second section exposes the main key performances metrics to take into consideration in TDCs design. Section III and Section IV presents respectively the main TDC architectures based on analog and digital techniques. Section V describes a new TDC architecture based on self-timed ring oscillator as a new perspective. Finally, Section VI states the paper conclusions.

II. TDC: key performance metrics

Time-to-digital converter is used to quantify the time between the *Start* and *Stop* events and to express the result as a digital value. Many parameters characterize the TDC performances. They are frequently used to evaluate the quality and the performances of a TDC.

A. Main TDC metrics

1) Time resolution: The time resolution characterizes the measurement precision of a time interval T. It represents the minimum time input that a TDC can correctly quantify. It is often referenced as the least significant bit (LSB). This parameter generally depends on the circuit characteristics, *i.e.*, the technology and the noise performances. An ideal TDC is a TDC in which the first code appears at a time equal to one LSB and then the characteristic of this TDC is shifted by this value (1 LSB) along the time axis. The resolution in this case is supposed to be constant. The quantification characteristic is given by Fig. 1 for an ideal TDC in absence of any distortion. A range of time interval with a variation lower than one LSB is coded by the same word. Thus, the transfer function is a stepped curve (with a step width of 1 LSB).

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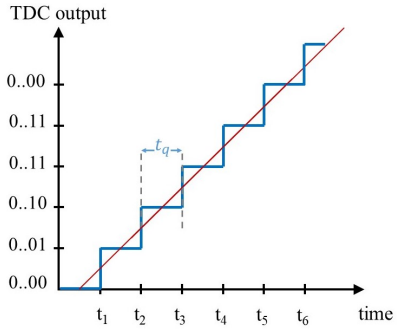


Figure 1. Example of TDC transfer function for an ideal case.

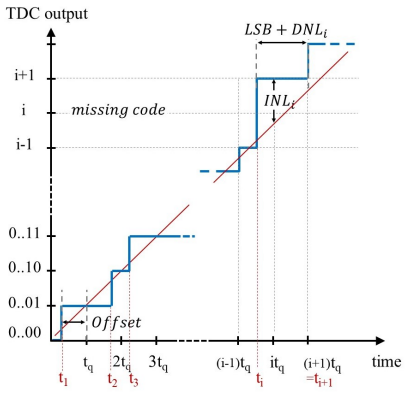


Figure 2. An example of the TDC non-linearity.

2) Dynamic range: It expresses the TDC maximal time input to correctly be quantified. For the structures using counters, this parameter is related to the number of bits of this counter.

3) Conversion time: It is the minimal time needed for a TDC to digitize a time input to a valid digital word. This time is counted from the *Start* event. This value is very important for the high-speed applications in which a minimal dead time should be respected.

4) Latency: It is the time needed after the *Stop* event for a TDC to compute a valid digital word. This time is included in the conversion time. Generally, this parameter gives the TDC rapidity to present a valid output.

B. Linear and nonlinear imperfections

The TDC imperfections can be classified into two categories. Firstly, the linear imperfections are easily detectable and not too much difficult to compensate such as the offset [1]. Contrarily, the nonlinear imperfections require advanced calibration schemes cannot always be completely removed. The Differential and Integral nonlinearities are the most important static errors to analyze. Furthermore, if the errors become large enough, missing code are a crucial issue affecting TDCs as illustrated in Fig. 2 (code i is missing).

In addition to these imperfections, noise sources like the jitter and the thermal noise can also degrade the performances of the TDC.

1) Offset error: The *Offset* represents a deviation of the TDC from the ideal first measurement which should be equal to 1 LSB. For $0 \leq t < LSB$, the code should be 0 until reaching a time time equal to one LSB. The time difference between the time, t_1, for the appearance of the first code 0..01 and the first LSB present the offset error. The normalized value of this error, E_{Offset}, is expressed:

$$E_{\text{Offset}} = \frac{t_1 - t_q}{t_q} \tag{1}$$

2) Quantization error: The conversion introduces a distortion between the digital output value and the original value. It is an inherent error related to any digital converter. Thus, the measured time interval is a function of the TDC output TDC_{out} given by:

$$T_m = \text{TDC}_{\text{out}} \times t_q + \varepsilon \tag{2}$$

where ε is the quantization error. The latter is generally modeled by a uniform random variable. The quantization error is the main error affecting the precision of a TDC.

3) Differential non-linearity (DNL): For a specific code, the differential non-linearity corresponds to the deviation of the step width from the theoretical LSB step width. As a result, the real step width is equal to $\text{LSB} + \text{DNL}$ (DNL is a real number). The expression of the differential non-linearity value per one LSB describing the fluctuation effect for the code digit i is given by (3), where t_i represents the measured delay for the first appearance of the i^{th} step.

$$\text{DNL(i)} = \frac{t_{i+1} - t_i}{\text{LSB}} - 1 \tag{3}$$

4) Integral non-linearity (INL): It is a measurement of the gap between the transfer characteristic and the straight red line in Fig. 2. It represents at the same time the cumulative deviation of each step from an ideal value providing a measurement of the non-linearity [1]. The INL is obtained by integrating the DNL curve. Thus, the cumulative i^{th} INL is expressed by:

$$\text{INL(i)} = \sum_{k=0}^{i} \text{DNL}_\text{k} \tag{4}$$

The INL (as the DNL) can be presented by its maximal value or by its root mean square (rms) value over all steps. They are usually normalized to be expressed in LSB.

III. Analog Time-to-Digital Converters

The first proposed architectures of time-to-digital converters were based on analog techniques. They are suitable for short measurement ranges since they provide high precision and good linearity. The traditional structure is based on the conversion of a time interval into a voltage. Thus, they show high performances in term of time resolution. They can reach a resolution of a few picoseconds [10], [14]. Nevertheless, these TDCs require a calibration and often repetitive measurements.

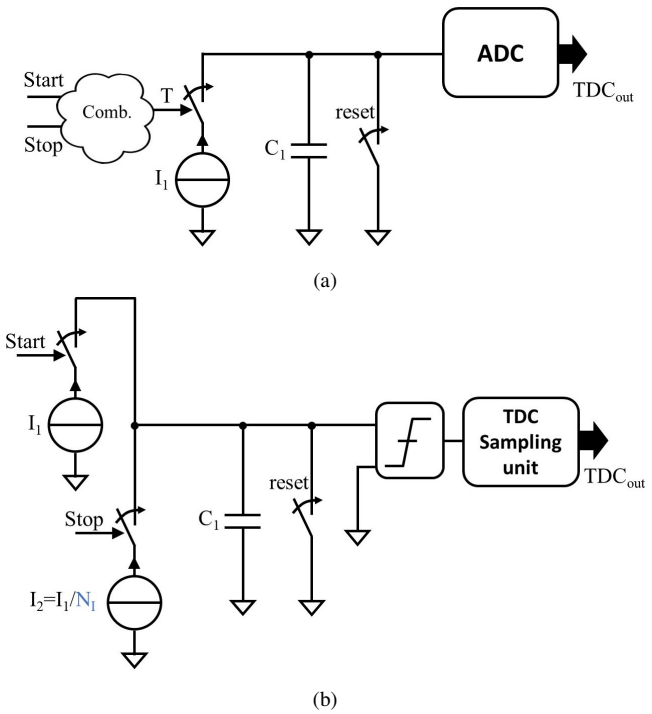


Figure 3. (a) Basic architecture of analog TDC, (b) Analog TDC with time stretching.

This first category of analog TDCs uses an analog-to-digital converter (ADC). Thereafter, these restrictions have been removed for the second analog TDC category, which is basically built on time stretching techniques as presented in the sequel.

A. Analog TDCs based on analog-to-digital converter

Based on a similar principle of ADCs, the classical analog approach converts into a voltage the time interval T [5], [6], [14], [15]. Traditionally, one possible way to generate the corresponding voltage is to use an integrator, in which a capacitor is charged with a constant current source, as presented in Fig. 3a. The integrator transforms the pulse into a voltage corresponding to the time intervals T. Then, this voltage is converted thanks to an ADC, which provides the digital output. The analog design constraints of the ADC limit the finest resolution t_q. Moreover, the trade-off between the resolution and the dynamic range (DR) should also be taken into account. A high resolution means a short time to sweep from ground to the supply voltage at the ADC input and, thus, limits the time DR. On the opposite, a large DR assumes to have a longer time to go from zero to the supply voltage (the time step increases as well).

B. Analog time-to-digital converters with time stretching

The most common structures of analog TDCs are based on the pulse-stretching techniques [16], [17]. In this case, no ADC is used and its limitation is eliminated. The principle is to charge the capacitor C_1 with a first current source I_1 and then to discharge it with a lower current source $I_2 = I_1/N_I$, as illustrated in Fig. 3b. A comparator is used to detect when the second integrator completes its discharge operation (time for zero-crossing), which corresponds to the time interval multiplied by the ratio N_I between the two current sources. A counter controlled with a stable clock reference records the number of cycles during this operation. Thanks to this architecture, as the capacitor C_1 is discharged slowly (N_I times), capturing the time with a better resolution becomes easier as the time has been stretched. To further improve the time resolution, dual and triple-slope stretching schemes have been proposed based on the same principle [3], [18], [19].

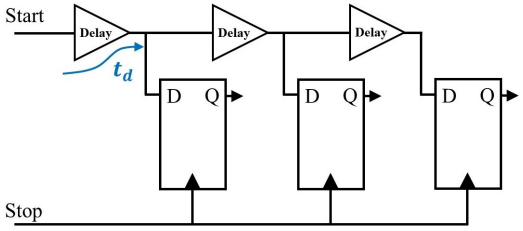


Figure 4. Basic implementation of a delay-line based TDC

IV. Fully Digital Time-to-Digital Converters

Analog TDCs have many limitations. Firstly, the current sources generate a nonlinear output and suffer from a finite output resistance (non ideal source). Thus, the linearity of the TDC is degraded especially for large dynamic ranges since the analog TDCs are known to be sensitive to the temperature [1]. Secondly, they are not suitable for fast applications due to the limitation related to the dead time [20]. Furthermore, these TDCs are requiring a large area due to capacitors. Consequently, they consume more power than their digital conterparts [20]. Thus, they are less suitable for advanced CMOS technologies. Today, fully digital techniques have been deployed to solve these issues. These TDCs can be carried out by very small, low power and simple circuits. The usual architecture of a TDC is simply based on computing the number of edges of a reference clock signal.

A. TDC with gate-delay resolution

1) Delay-Line based TDC: A TDC with gate-delay resolution, called delay-line based TDC, is depicted in Fig. 4. It is a compact architecture that has been proposed as a first fully digital solution. In this architecture, the *Start* signal provides an event propagating along the delay line. The arrival of the *Stop* signal triggers the registers to start copying the state of each gate output. Thus, the measured time interval T_m corresponds to the number of stages that have propagated the *Start* signal. The measured time is defined by the thermometer code given by the output registers. This topology is the basis for most of the other digital TDC architectures. Admittedly, this TDC is a simple structure that can be easily integrated into ASIC or FPGA but with moderate performances. It presents a low latency because the output can be quickly available after the arrival of the *Stop* event. However, its resolution is

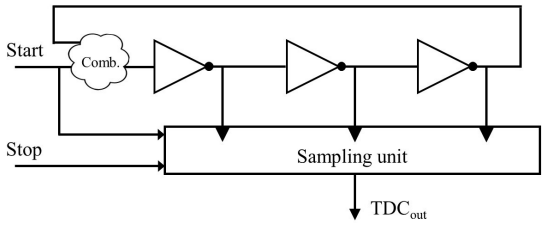


Figure 5. Inverter Ring Oscillator based TDC.

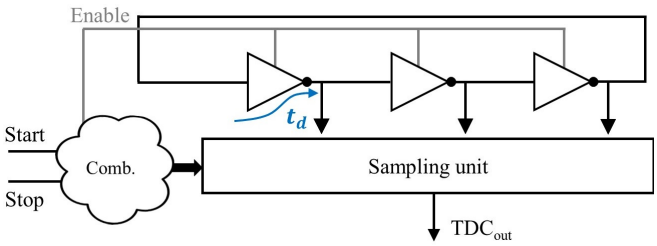


Figure 6. Gated Ring Oscillator based TDC.

bounded by the CMOS gate delays; it cannot be lower than the propagation delay of a logical gate. In addition, to cover a larger time interval, the number of stages must be duplicated as needed. Thus, the cost and power consumption will increased. This concerns as well the maximal sampling rate, which is decreased when drastically expanding the clock tree.

Otherwise, the PVT variations affect the delay of the stages [1]. The jitter contribute to the measurement errors due to the temperature and supply voltage variations. With the accumulation of these random variations, the delay-line may present an important deviation at its end. Furthermore, the linearity could be affected by the random mismatch of the delay-line gates. Therefore, the delay-locked-lines (DLLs) are often deployed to calibrate the process variations [21]. The delay unit of the DLL is voltage-controllable, which allows locking its delay to a fraction of a reference clock whatever the variations [22].

2) Ring Oscillator: A simple way to overcome the limitation of the dynamic range of the delay-line TDC is to wrap the line into a ring [7], [23]–[25]. Compared to the simple delay-line, each stage can be used several times. Therefore, the electrical event, which provides the time stamping, will propagate several times in the ring allowing to cover large dynamic ranges. Moreover, a gain of power and area is obtained. If double edge is considered, using CMOS inverters or buffers as delay gate is the same. Else, using inverters instead of buffers allows doubling the resolution [1]. However, the problem of the transition slope asymmetry related to the design of inverters, can affect the linearity of the TDC. This can be fixed via design but any process variation can produce similar problems [1]. Fig. 5 shows the structure of the inverter ring oscillator (IRO).

The oscillation frequency of the IRO is a function of the stages number. Assuming that the IRO includes L stages having as propagation delay $t_q = \mathrm{INV}_{\mathrm{gate_delay}}$, the oscillation period is expressed by (5). The period of this oscillator is twice the number of stages since the event has to propagate twice to regain the initial polarity [1].

$$T_{RO} = 2L \times t_q \tag{5}$$

Propagating many events in the same structure allows exploiting the phase difference, and thus improving the resolution. In IROs, only one event can propagate. However, in [24], a modified structure allowing to propagate two events,called "Third-Harmonic Ring TDC", has been proposed.

3) Gated Ring Oscillator: An improved topology, called gated-ring oscillator (GRO), has been proposed to limit the power consumption due to the free running mode in IROs [7], [23], [25]. This mode is a consequence of the propagation of the timing events even if the measurement has been stopped. As shown in Fig. 6, the inverters are gated with an *Enable* signal to turn OFF the oscillator outside the interval measurement. In addition, the status at each inverter output is frozen and kept until the next measurement which reduces the quantization error. Thus, it allows to benefit from first-order noise shaping and to keep the residue of the last measurement transferred to the next one [7]. The benefit from the gating technique, especially with successive measurements, is the increased effective time resolution which cannot be achieved for a simple measurement [1]. Otherwise, the time resolution of this TDC is still limited by the ring stage delay. In addition, the signal controlling the frozen state of signals should be able to stop and start the signal propagation in any state, else the measurements will not be correct.

B. TDC with sub-gate-delay resolution

1) Vernier based TDC:

a) Standard Vernier based TDC: In order to overcome the gate-delay limitation, sub-gate delay resolution solution called Vernier-TDCs have been proposed [26], [27]. Fig. 7 illustrates the Vernier-TDC architecture. In this topology, the events *Start* and *Stop* propagate in two delay lines having slightly different propagation delays t_{d1} and t_{d2} ($t_{d1} < t_{d2}$). At the beginning of the measurement, they propagate with a time difference equivalent to T. Then, they start reducing slightly the time difference until they become in phase. At that point, the *Stop* signal catches the *Start* signal and the order is inverted [1]. The Vernier stage i, called the tap i, is referred to a combination of two delay gates i: one from the first line and the other from the second line. The TDC output is expressed by the resulting effective resolution $t_q = t_{d1} - t_{d2}$, which is smaller than the stage delay [26]. Thus, no matter the technology is used, the time resolution is sub-gate. Offering a sub-gate delay resolution, the Vernier is deployed in many TDC propositions in literature as presented in the sequel.

As any open structure, such as the delay-line, the Vernier is not appropriate for large dynamic range measurements otherwise it presents amplified issues. In fact, for a maximal time interval T_{max}, a maximal number of stages $N = \frac{T_{max}}{t_q}$ is

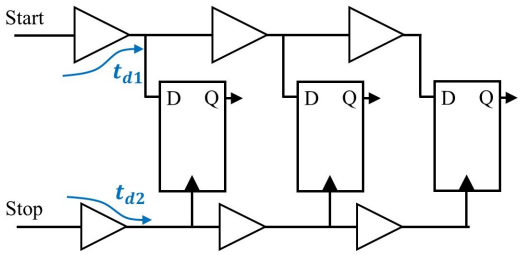


Figure 7. A Vernier delay-line TDC structure.

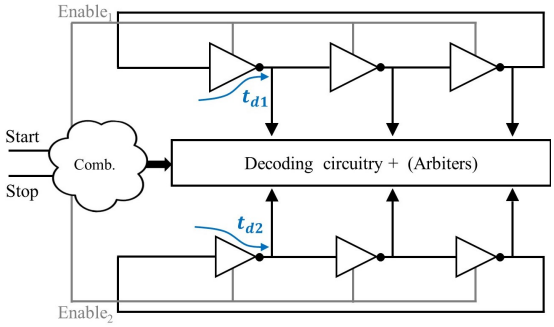


Figure 8. Vernier gated ring oscillator TDC.

required for each line. Therefore, the time resolution enhancement will be limited by the area. In addition, the latency, which represents the most critical issue of the Vernier, depends on the length of the time interval. On the other hand, since two delay-lines are used, the jitter is duplicated and the TDC becomes more sensitive to mismatch. In addition, the delay-lines have to be well matched. In fact, it is very difficult to precisely adjust the time difference without using complex calibration schemes [20]. Finally, all the delay gates are switching many time, independently of the T length, especially with successive measurements. This increases the power consumption.

b) Two-dimension Vernier TDC: An advanced topology using two orthogonal dimensions, called 2D-Vernier based TDC, has been proposed [9]. This structure increases the dynamic range and also provides extra freedom degrees for reducing the latency. It minimizes the length of the delay-lines to one third of lines used to cover the same dynamic range. Compared to the simple Vernier, the linearity of this type of TDCs is more sensitive to the delay variations. Thus, any delay variations can cause a large non-linearity.

c) Vernier ring oscillator TDC: To exploit the sub-gate resolution given by the Vernier, hybrid techniques have been proposed using RO [28] or GRO [25]. The architecture of this hybrid TDC with a GRO is presented in Fig. 8. They keep the same principle of the Vernier by just replacing the delay-lines by ring oscillators. The loop structure allows reusing the delay-line many times. As a result, they offer a large dynamic range. However, when resolution is improved to picoseconds level, these methods suffer from a degradation of the linearity and they are subject to the jitter accumulation [20], [25], [28].

d) Two-dimension ring oscillator Vernier TDC: The 2D-RO Vernier TDC has been developed to fold lines and gain more performances of the previous structure [29], [30]. The principle is to extend the time step quantification. Instead of considering a fixed value t_q for the taps, the two dimensions offers more flexibility for interpolating steps between axis values. This is an effective solution for high resolution and reduced latency time. To combine these advantages with the first noise shaping technique, it is recommended to use a GRO (Fig. 9). However, as the 2D-Vernier, it is sensitive to delay variations, and its linearity is easily degraded.

2) TDC with interpolation technique: Generally, hybrid approaches present further interesting results. For TDCs, the interpolation allows to combine the advantages of several architectures. Mainly, the interpolation is often proposed as an alternative to cover a wider dynamic range, because the sub-gate resolution requirements tend to limit this latter. Notice that most of the proposed TDCs with interpolation are based on time stretching.

a) Local-passive interpolation: The local-passive interpolation is originally based on introducing parallel resistive voltage dividers between the inputs of the delay gates and their outputs in a delay-line. The goal is to create intermediate signals. Thus, the effective delay par stage is reduced based on the averaged impedance at each output [1], [23]. A cyclic architecture is required in order to appropriately sample all the signals, which may increase the size and the circuit complexity [23]. The resistive voltage dividers can be advantageously replaced by digital gates. This technique is essentially based on the fan-out of the gates.

b) Differential delay-line interpolation: Similarly to the local-passive interpolation, differential delay-lines has been proposed [1], [31]. In fact, the need for stable delay gates, which is not generally trivial to implement, encourages research to develop techniques such as differential delay elements. This principle has been integrated in delay-lines for an interpolated TDC, which is known as parallel scaled delay technique [31]. In this example, the coarse measurement is measured using a counter and the fine measurement is assured with a DLL providing an effective time resolution of 12.2 ps using 350 nm CMOS technology.

c) Multi-path GRO: Another solution to obtain a sub-gate delay resolution is to exploit the phase difference between events propagating in different rings. Straayer *et. al.* [7] presented an architecture based on this principle using a multi-path GRO. The implementation of the inverter gate has been modified to include multiple inputs and a single output. These multiple inputs allow coupling the oscillators together, which makes the oscillation more robust. This architecture benefits from the first order noise shaping due to the use of the GRO. Two transistors, controlled by the *Enable* signal, are included in the inverter gate in order to ensure this gating operation. Theoretically, an oscillator of L stage, coupled with other $M-1$ oscillator, will reduce the effective delay per stage by a factor of M.

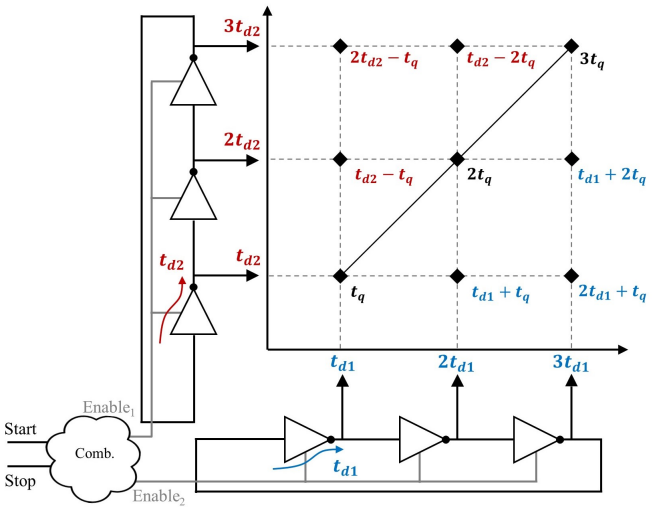


Figure 9. 3×3 2-D Vernier gated ring oscillator TDC.

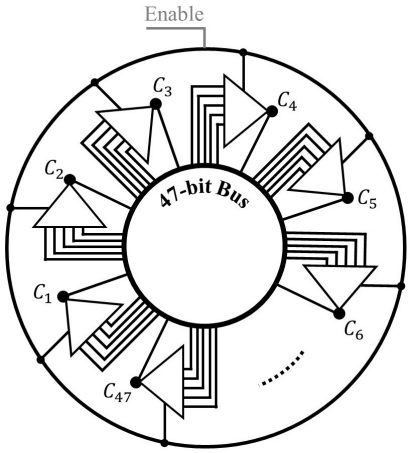


Figure 10. The proposed multipath GRO structure in [7]

Using this interpolation technique, a time base with an average resolution which is lower than the gate delay is presented. In practice, the effective time stamping is not regular: locally, the effective resolution may be either higher or lower than the gate delay. In [7], a 47-stage penta-path GRO is used as illustrated in Fig. 10. For a minimal design goal, the proposed inverter gate has been designed with five inputs. The average resolution is improved by over a factor of 5 compared to the basic GRO structure. The corresponding logic unit of this structure is more complicated and not obvious to design. Since the architecture requires full custom design instead of using standard cells, the transistors technology scaling is not simple and purely requires a complete TDC redesign. Moreover, getting a robust implementation with low power and area, the measurement of a time interval T with a sub-gate delay resolution still becomes challenging.

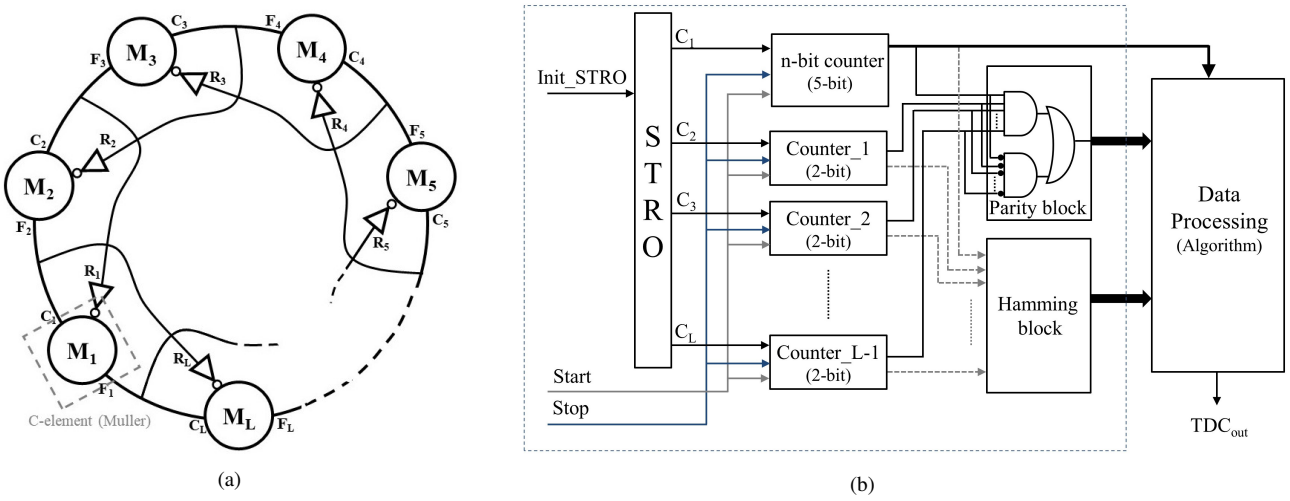
d) Interpolation with time variation: Pulse shrinking is often an unwanted effect in TDCs because it limits the time interval [1]. Notice that some TDCs are based on this effect to get sub-gate delay resolution. For a digital approach, the slope asymmetry of each delay stage is exploited to generally reduce the time width. In fact, a time width is formed with the rising edge of the *Start* signal and the falling edge of the *Stop* signal. As considered for the Vernier technique, the pulse width becomes smaller while propagating in the structure until that pulse disappears at a specific position. Likely, the power and area are function of the dynamic range. This concerns as well the latency and the conversion time, which are complicated to interface [1]. Otherwise, any PVT variations can disturb the sampling operation, especially when the pulse becomes very small before vanishing.

Contrarily, many interpolation techniques are based on time amplification. The time interval cannot be directly amplified but the small time residue from each tap after a coarse measurement. In fact, the time amplifiers can only amplify small time intervals due to their small dynamic range. In [10], the time interval is first quantified with a counter as coarse measurement driven with a high-stability reference clock. Then, the remaining time of this first quantification is amplified using arbiters, used as time amplifier (TA). Therefore, the resolution is greatly improved. The need for an implementation of TA at each tap is necessary because the time cannot be stored directly in the time domain. This will present a critical issue related to the latency. Moreover, the time amplification cannot handle continuous events, especially if arbiters are used as TA. Unlikely, the analog TAs are able to process continuous events [1]. Unfortunately, this method can yield to more complex systems. Additionally, this technique suffers from gain uncertainty due to the local PVT variations, which makes it difficult to operate linearly [1].

e) Three-level conversion: Recently, to gain an enhancement of the time resolution, the interpolation technique has been supported by an additional conversion level. Jin Wu *et. al.* propose a TDC with Three-level scheme implemented in 350 nm CMOS technology [11]. The first conversion (high-level) is based on counters driven by a stable clock, which ensure the wide range (25.0 ns). The middle-level (as fine TDC) is a dual DLL (made by primary and secondary DLL), offering a time resolution of 3.125 ns. This resolution is defined by the eight-stage voltage controlled delay line in the primary DLL. A Vernier implemented by the dual VCO is used as final step providing a sub-gate resolution of 390 ps. Notice that the TDCs implemented on FPGA boards are often designed using this technique of multi-level conversion.

V. TDC BASED ON A SELF-TIMED RING OSCILLATOR

This TDC is based on a self-timed ring oscillator (STRO). Thanks to the STRO features, this TDC is able to achieve a time resolution as fine as needed by simply increasing its number of stages, *i.e.* the number of phase outputs. This resolution is only limited by the noise floor of the STRO stage.



(a) (b)

Figure 11. (a) STRO Architecture of L-stages (b) The proposed TDC architecture using L-stage STRO.

A. Self-Timed Rings and Operating Principles

Self-timed ring oscillators (STROs) have been inspired by the control path of a linear micropipeline circuit [32], which has been looped. Each ring stage is composed by a C-element (Muller gate) and an inverter as shown in Fig. 11a. In this architecture, several events (electrical transitions) can propagate simultaneously without colliding thanks to a request/acknowledgement handshake protocol. The number of events is set at the ring initialization, and stays invariant. The frequency oscillation of the STRO does not directly depend on the number of stages, but rather on the occupancy ratio, which is the number of events N over the number of stages L. In fact, a same frequency can be obtained for different STROs with different number of stages by respecting the same occupancy ratio. Moreover, the ring exhibits a unique oscillation mode in which events propagate in the ring with a uniform time spacing (evenly-spaced oscillation mode) [33] due to the Charlie effect [34]. These features have been exploited to propose a new TDC architecture based on STRO. It primarily benefits from the uniform distribution of phases with a sub-gate time resolution. In this particular case, the number of events N is co-prime with L and the time resolution is given by:

$$\Delta\varphi = \frac{T_{\mathrm{STR}}}{2L} \tag{6}$$

B. STR-based TDC Architecture

The proposed STR-based TDC architecture is presented in Fig. 11. A proof-of-concept of this architecture using 28 nm FDSOI CMOS technology has already been presented in [12], [13]. An L-stage STRO, with a number of events co-prime with L, provides L signals evenly distributed over its half oscillation period $T_{\mathrm{STR}}/2$. As a result, the measured time interval T_m can be expressed as a function of $\Delta\varphi$ and $T_{\mathrm{STR}}/2$ (7). The principle of this structure is to firstly count the number of $T_{\mathrm{STR}}/2$ steps and then to quantify the remaining time with a resolution of $\Delta\varphi$. A simple architecture deriving from this equation is made by a double-edge counter at each STRO output. Basically, k counters show the value $M+1$ while the other $L-k$ counters exhibit the value M. Obviously, the information about the number of counters showing M or $M+1$ can be derived from the two least significant bits of all counters. Therefore, the architecture can be optimized to include a unique n-bit counter placed on a STRO output showing the value N_v (*e. g.,* 5-bit counter) and 2-bit counters for the other outputs. The obtained results from these counters are sufficient to determine M and k as detailed in [12]. Actually, the Hamming block uses the LSBs to compute the hamming weight H which is equal to k when M is even and $L-k$ when M is odd. Then, the Parity block evaluates the parity of M by using the second lower bits of the counters.

$$T_m = M \cdot \frac{T_{\mathrm{STR}}}{2} + k \cdot \Delta\varphi = (M \cdot L + k) \cdot \Delta\varphi \tag{7}$$

The TDC output is given by a data processing algorithm based on the collected data from the n-bit counter, Hamming and Parity blocks.

Thanks to the STRO unique features, the STR-based TDC can virtually achieve as fine as desired a time resolution, which is only limited by the jitter of stages. In addition, it is based on a simple and comprehensive measurement scheme: its implementation is straightforward. Simulations using 28 nm FDSOI technology has been used to demonstrate a 9-stage TDC able to perform on-the-fly measurements on fast non-periodic signals. A sub-gate delay resolution of 8.9 ps was obtained. DNL and INL results confirmed the accuracy of the measurements. This proposition opens new perspectives for applications requiring on-the-fly measurement with a fine time resolution.

VI. Conclusion

This paper provides a literature review of the main used TDC architectures, especially for the CMOS integration. In addition, key performance metrics have been described in order to compare and study the TDCs. Thus, the right TDC

architecture can be adopted for the right an application according to its specifications. For applications requiring on-the-fly measurements with a fine resolution, the STR-based TDC offers interesting perspectives compared to the other TDCs. Thanks to the STRO features, this TDC is able to achieve a time resolution as fine as needed by simply increasing its number of stages, *i.e.* the number of phase outputs. In addition, the implementation is simple and fully digital which makes it suitable for all digital circuits and for taking advantages of the down-scaling of CMOS technologies.

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