Design of a time-to-digital converter to be used as a phase detector in a PLL in 65 nm technology

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March 7, 2025

Abstract

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Dedications

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Context and motivation

1.1.1 Low jitter PLLs in modern IC design

1.1.2 Limitations of analog PLLs

1.1.3 Limitations of traditional PFDs

1.2 Problem statement

1.3 Objectives

1.3.1 General objective

1.3.2 Specific objectives

1.4 Significance

1.4.1 Academic significance

1.4.2 Industry significance

Clock generation

SerDes

Chapter 2

Theoretical framework

2.1 Phase-locked loop fundamentals

2.1.1 Basic structure

2.1.2 Key PLL parameters

Phase noise / jitter

Jitter is defined as the time deviation (Δ_t) of a signal's transition edges from their ideal positions in time. It is a metric of the outmost importance in the design of PLLs as it is a direct measure of the quality of the clock signal generated. Phase noise describes the same phenomenon in the frequency domain (the phase noise of a signal is the Fourier transform of the jitter) and is usually expressed in dBc/Hz.

Output frequency

It is defined as the range of frequencies that the PLL is capable of generating and can be determined by the VCO output range and the division ratio of the feedback frequency divider. This is a key metric in establishing the application of the PLL (e.g., clock generation or RF synthesizer) and it bears

significant importance in the design process due to the tradeoff it has with the phase noise performance of the PLL.

Loop bandwidth

The closed-loop bandwidth of a PLL is the frequency range over which the PLL can track the phase/frequency variations of the input signal (from DC to -3 dB from the open-loop gain). It affects the acquisition time and phase noise performance of the PLL.

Noise bandwidth

It is the PLL's noise due to the filter's loop bandwidth, the higher frequencies of the voltage-controlled oscillator (VCO) are the major contributor to this effect, therefore the need to set a low enough bandwidth in order to supress the most out of it. Even if reducing the loop bandwidth would be desirable to supress in-band phase noise, it's also necessary to take into consideration that there is a tradeoff between the lock-in time and in-band phase noise.

Beat-note period

Defined as the time interval between successive "beats" (oscillations) observed at the phase detector output, in other words, is the inverse of the frequency difference's magnitude between the reference and feedback signals as shown in figure 2.2. Beat-note period is closely related to the acquisition time of the PLL and can be estimated by equation (2.1). This metric is a direct measure of the frequency mismatch between the reference and the feedback signals.

$$T_{beat} = \frac{1}{|f_{ref} - f_{feed}|} \tag{2.1}$$

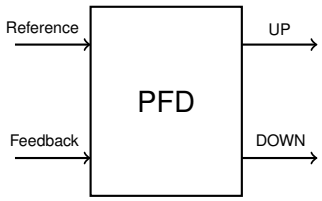

Figure 2.1: a) PFD block.

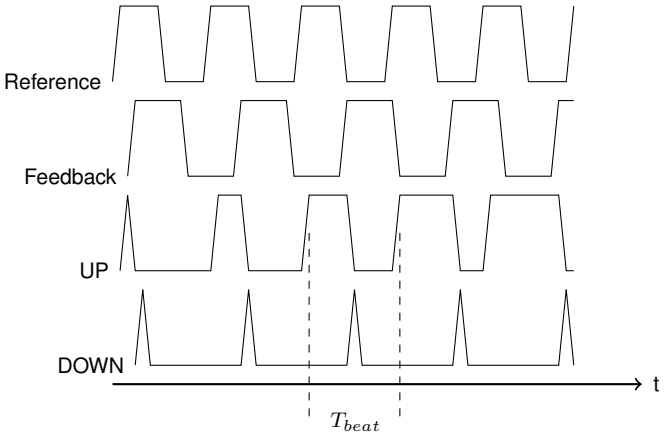

Figure 2.2: b) PFD output.

Lock-in time

Lock-in time (also called aquisition or settling time) is defined as the time for the PLL to lock on to the input reference phase and frequency within one beat-note period (T_{beat}) after a frequency change or startup of the system. This parameter measures the time required for the PLL to achieve the final phase lock once the VCO frequency is within the lock-in range. The lock-in time can be estimated with equation (2.2).

$$T_{lock-in} = \frac{ln(\epsilon)}{\zeta\omega_n} \tag{2.2}$$

where:

$\epsilon =$ acceptable phase error

$\zeta =$ damping factor

$\omega_n =$ natural frequency

Pull-in time

In contrast with the lock-in time, the pull-in time is the required amount of time for the PLL to initially aquire lock on to the reference signal from an

arbitrary starting frequency (when the VCO's initial frequency is far from the target).

Lock-in range

The frequency range within which the PLL locks to the reference frequency in one T_{beat}. Once the feedback signal is in this range, the PLL will enter lock state within the next T_{beat}.

Pull-in range

Range of frequency within which the PLL can aquire lock on to the reference signal once the VCO has the correct frequency and several beat-note periods have passed.

Pull-out range

The maximum allowed frequency or phase abrupt change applied to the reference signal beyond which the PLL unlocks.

Hold range

This parameter establishes the maximun theoretical frequency range for an input reference beyond which the PLL never locks. Hold range is bigger than both lock-in and pull-in ranges.

SNR

The signal to noise ratio is an appropiate way to measure the impact of noise on a circuit. It's often used in most figures of merit (FOM) for making fair comparisons between PLLs.

Power consumption

An important parameter in measuring the performance of integrated circuits. Often used in most FOMs.

Spurs

Spurious tones are unwanted periodic signals that appear at the output spectrum of the PLL. Spurs are completely deterministic, thus they are distinct from phase noise which is random and spreads across the spectrum of the signal.

2.1.3 Analog phase-locked loop

The principles of operation of the digital PLL stem from its analog counterpart, therefore this subsection describes the fundamental building blocks of the analog PLL as well as a simplified model of the system which allows the circuit designer to analyse its behaviour.

Linearized model

The PLL is a non-linear system, yet it can be approximated quite accurately in to the linear system of figure 2.1 if certain assumptions are taken in to consideration. The first of this assumptions is that the phase error (ϕ_e) must be small enough, meaning the PLL is near lock state. Another one is that the characteristic of the phase detector must be approximately linear and given by (2.3). Lastly, the VCO range of operation must be within its linear region like in figure 1313 and thus be described by (2.4).

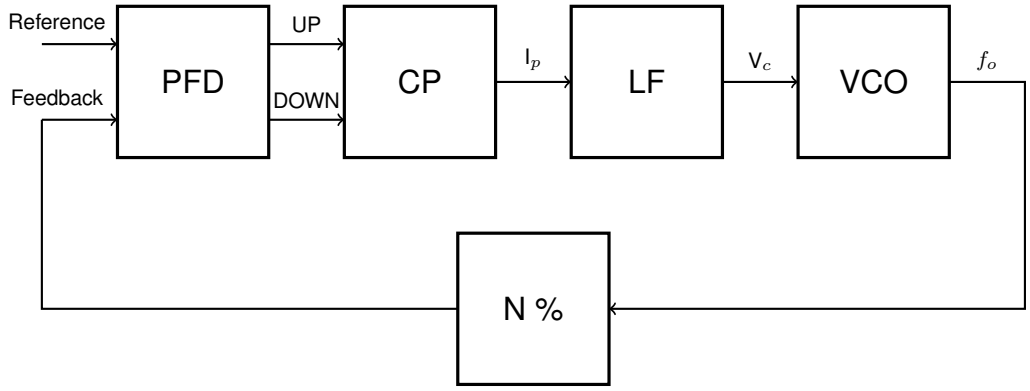

Figure 2.3: Block diagram of the linearized PLL model.

$$v_d = K_{PD}\,\phi e + \underbrace{V_{do}}_{\text{free running voltage}} \tag{2.3}$$

$$\Delta_{\omega_o} = K_{VCO}\,(V_c - V_{co}) \tag{2.4}$$

The closed-loop transfer function of the model shown in figure 2.3 can be obtained using Mason's gain equation (2.5) in the system's equivalent of figure 2.4. Note that the loop filter is of second order.

$$H(s) = \frac{\Sigma_{F.P}(1 - \Sigma_{not\,touching})}{1 - \Sigma_{loops}} \tag{2.5}$$

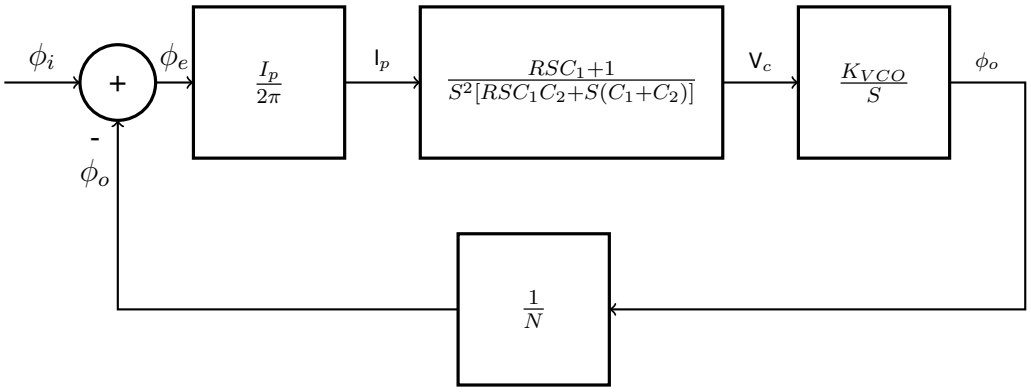

Figure 2.4: Block diagram of the linearized PLL with each block transfer function.

Thus, the closed loop transfer function of this system is that of equation (2.6). This transfer function describes the dynamics of the PLL entirely.

$$A_{CL} = \frac{SI_{CP}RC_1K_{VCO}N + I_{CP}K_{VCO}N}{S^3NRC_1C_2 + S^2N(C_1 + C_2) + SI_{CP}RC_1 + I_{CP}K_{VCO}} \qquad (2.6)$$

Phase frequency detector

A PLL that has a phase frequency detector (PFD) instead of a phase detector (PD) is superior because it can track changes in both phase and frequency at the input signal. This approach provides robustness to the system because the PLL locks regardless of the initial value of the output frequency, therefore making the pull-in range equal to the VCO tuning range.

The most common implementation of a PFD is shown in figure 2.5. The operation of this circuit is as follows: When either of the two signals arrive with a rising edge to the corresponding D flip-flop CLK terminal a HIGH state is pass along to its output (Q), this result is mantained until the other signal's rising edge arrives at the other flip-flop because at that moment in time the AND gate would activate and reset both flip-flops. This behavior can be observed in figure 2.6.

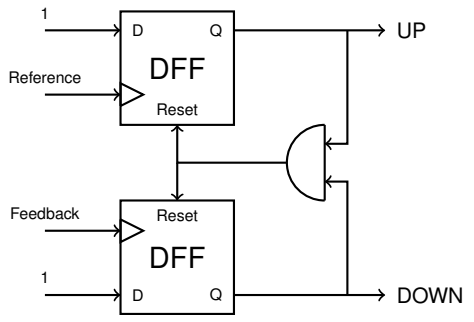

Figure 2.5: Three states PFD implementation.

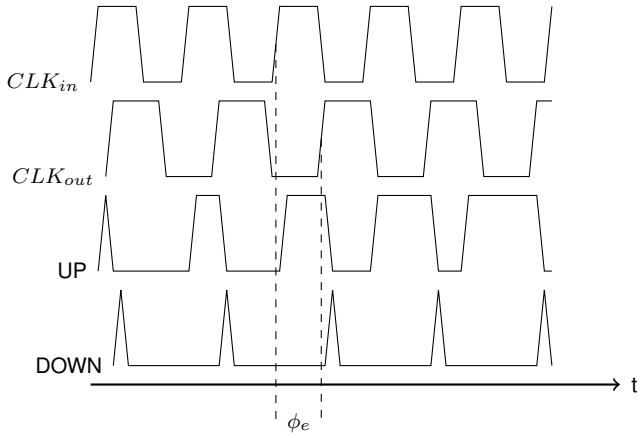

Figure 2.6: Transient response of the PFD.

Charge pump

Loop filter

Voltage-controlled oscillator

Frequency divider

2.2 Digital phase-locked loop

anan

2.3 Time-to-digital converter

2.3.1 Delay-locked loop fundamentals

2.3.2 TDC as a phase detector

2.4 65 nm CMOS technology

Chapter 3

Literature review

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Chapter 4

Methodology

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Chapter 5

Results

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Chapter 6

Discussion

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Chapter 7

Conclusion

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Appendix A

Appendix

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