Design of a time-to-digital converter to be used as a phase detector in a PLL in 65 nm technology

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July 10, 2025

Abstract

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Chapter 1

Introduction

1.1 Context and motivation

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1.1.2 Limitations of analog PLLs

1.1.3 Limitations of traditional PFDs

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Chapter 2

Theoretical framework

2.1 Phase-locked loop fundamentals

2.1.1 Basic concept

The PLL is a feedback control system that is used to synchronize the phase and frequency of an output signal to a reference signal. The reference signal is a very stable clock signal locally generated usually by a crystal oscillator. The PLL compares the phase of this reference signal with the phase of the output signal and generates an error signal that is used to adjust the frequency of the output signal.

There's two types of applications for PLLs broadly speaking: clock generation and clock data recovery. In the first case, the PLL is used to generate a clock signal that is synchronized to the reference signal. In the second case, the PLL is used to recover the clock signal from a data stream.

The PLL consists of three main components: a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). The PD compares the phase of the reference signal with the phase of the output signal and generates an error signal that is proportional to the phase difference between

the two signals. The LF smooths out the ripple riddled signal generated by the PD, reduces the high frequency noise of the loop and provides a stable control voltage to the VCO. The VCO generates an output signal whose frequency is proportional to the control voltage. Lastly, the output signal is fed back to the PD, thereby creating a closed-loop system.

If the PLL also has a frequency divider in the feedback path, the system is also capable of generating a frequency that is a multiple or fraction of the reference frequency. This is useful in applications where a higher frequency is needed, such as in RF synthesizers.

2.1.2 Key PLL parameters

Phase noise / jitter

Jitter is defined as the time deviation (Δ_t) of a signal's transition edges from their ideal positions in time. It is a metric of the outmost importance in the design of PLLs as it is a direct measure of the quality of the clock signal generated. Phase noise describes the same phenomenon in the frequency domain (the phase noise of a signal is the Fourier transform of the jitter) and is usually expressed in dBc/Hz.

Output frequency

It is defined as the range of frequencies that the PLL is capable of generating and can be determined by the VCO output range and the division ratio of the feedback frequency divider. This is a key metric in establishing the application of the PLL (e.g., clock generation or RF synthesizer) and it bears significant importance in the design process due to the tradeoff it has with the phase noise performance of the PLL.

Loop bandwidth

The closed-loop bandwidth of a PLL is the frequency range over which the PLL can track the phase/frequency variations of the input signal (from DC to either -3 dB from the open-loop gain or to the unity-gain frequency at 0 dB). It affects the acquisition time and phase noise performance of the PLL.

Noise bandwidth

It is the PLL's noise due to the filter's loop bandwidth, the higher frequencies of the voltage-controlled oscillator (VCO) are the major contributor to this effect, therefore the need to set a low enough bandwidth in order to suppress the most out of it. Even if reducing the loop bandwidth would be desirable to suppress in-band phase noise, it's also necessary to take into consideration that there is a tradeoff between the lock-in time and in-band phase noise.

Beat-note period

Defined as the time interval between successive "beats" (oscillations) observed at the phase detector output, in other words, is the inverse of the frequency difference's magnitude between the reference and feedback signals as shown in figure 2.2. Beat-note period is closely related to the acquisition time of the PLL and can be estimated by equation (2.1). This metric is a direct measure of the frequency mismatch between the reference and the feedback signals.

$$T_{beat} = \frac{1}{|f_{ref} - f_{feed}|} \tag{2.1}$$

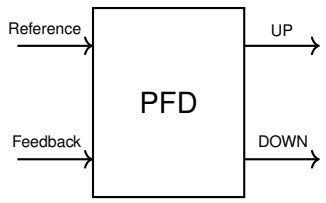

Figure 2.1: a) PFD block.

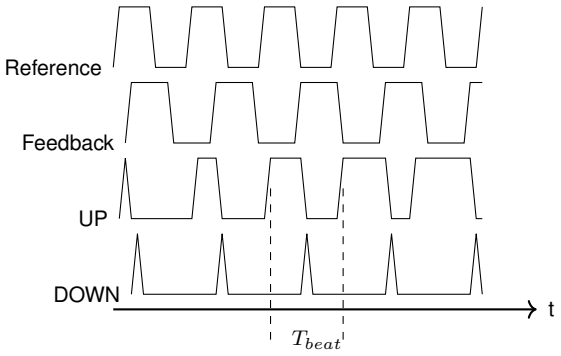

Figure 2.2: b) PFD output.

Lock-in time

Lock-in time (also called aquisition or settling time) is defined as the time for the PLL to lock on to the input reference phase and frequency within one beat-note period (T_{beat}) after a frequency change or startup of the system. This parameter measures the time required for the PLL to achieve the final phase lock once the VCO frequency is within the lock-in range. The lock-in time can be estimated with equation (2.2).

$$T_{lock-in} = \frac{ln(\epsilon)}{\zeta\omega_n} \tag{2.2}$$

where:

$\epsilon =$ acceptable phase error

$\zeta =$ damping factor

$\omega_n =$ natural frequency

Pull-in time

In contrast with the lock-in time, the pull-in time is the required amount of time for the PLL to initially aquire lock on to the reference signal from an

arbitrary starting frequency (when the VCO's initial frequency is far from the target).

Lock-in range

The frequency range within which the PLL locks to the reference frequency in one T_{beat}. Once the feedback signal is in this range, the PLL will enter lock state within the next T_{beat}.

Pull-in range

Range of frequency within which the PLL can aquire lock on to the reference signal once the VCO has the correct frequency and several beat-note periods have passed.

Pull-out range

The maximum allowed frequency or phase abrupt change applied to the reference signal beyond which the PLL unlocks.

Hold range

This parameter establishes the maximun theoretical frequency range for an input reference beyond which the PLL never locks. Hold range is bigger than both lock-in and pull-in ranges.

SNR

The signal to noise ratio is an appropiate way to measure the impact of noise on a circuit. It's often used in most figures of merit (FOM) for making fair comparisons between PLLs.

Power consumption

An important parameter in measuring the performance of integrated circuits. Often used in most FOMs.

Spurs

Spurious tones are unwanted periodic signals that appear at the output spectrum of the PLL. Spurs are completely deterministic, thus they are distinct from phase noise which is random and spreads across the spectrum of the signal.

2.1.3 Analog phase-locked loop

The principles of operation of the digital PLL stem from its analog counterpart, therefore this subsection describes the fundamental building blocks of the analog PLL as well as a simplified model of the system which allows for the circuit designer to analyze its behavior.

Linear phase model of the PLL

The PLL is a non-linear system, yet it can be approximated quite accurately into the linear system of figure 2.1 if certain assumptions are taken in to consideration. The first of this assumptions is that the phase error (ϕ_e) must be small enough, meaning the PLL is near lock state. Another one is that the characteristic of the phase detector must be approximately linear and given by (2.3). Lastly, the VCO's tuning range must be within its linear region of operation (it is generally desirable to limit the variation of K_{VCO} to no more than 20%) like the frequency range between ω_1 and ω_2 in figure 2.4, only in this conditions the VCO can be considered a linear system and thus be described by (2.4).

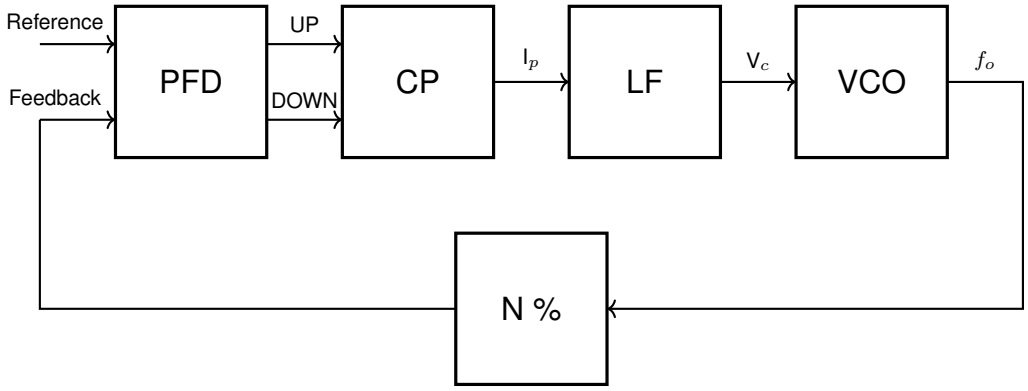

Figure 2.3: Block diagram of the linear phase PLL.

$$v_d = K_{PD}\,\phi e + \underbrace{V_{do}}_{\text{free running voltage}} \tag{2.3}$$

$$\Delta_{\omega_o} = K_{VCO}\,(V_c - V_{co}) \tag{2.4}$$

Each of the blocks in 2.3 has a transfer function associated with it, which can be expressed as follows: The PFD/CP combination is modeled as a current source with a gain of $I_p/2\pi$. The VCO is modeled as an ideal integrator with gain K_{VCO} and its transfer function is given by K_{VCO}/S. The feedback divider is modeled as a simple gain of $1/N$. Finally, the loop filter (LF) depends on the order of the filter and the type of components used.

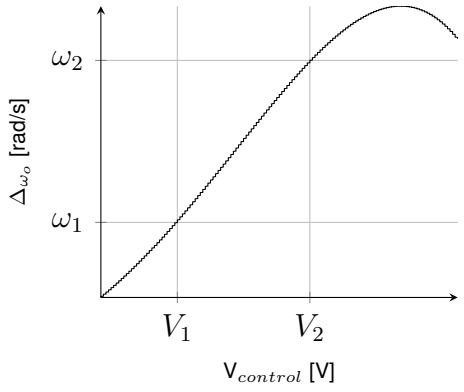

Figure 2.4: VCO characteristic example.

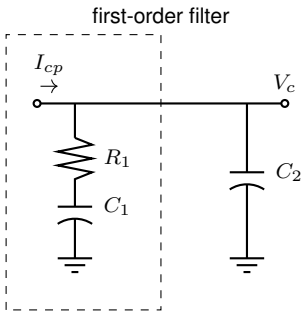

Figure 2.5: Second-order passive loop filter.

The most common implementation is a passive RC filter, which can be modeled either as a first-order or a second-order system. For the sake of sim-

plicity in this analysis, the LF is modeled as a first-order circuit like the one enclosed by dashed lines in figure 2.5. The transfer function of the LF is then given by $(R_1SC_1 + 1)/(SC_1)$.

Knowing the transfer functions of each block, one can represent the PLL system as in figure 2.6. Then with the help of Mason's rule (2.5), the overall closed-loop transfer function (2.6) of the PLL can be obtained.

$$H(s) = \frac{\Sigma_{F.P}(1 - \Sigma_{loops\,not\,touching})}{1 - \Sigma_{loops}} \tag{2.5}$$

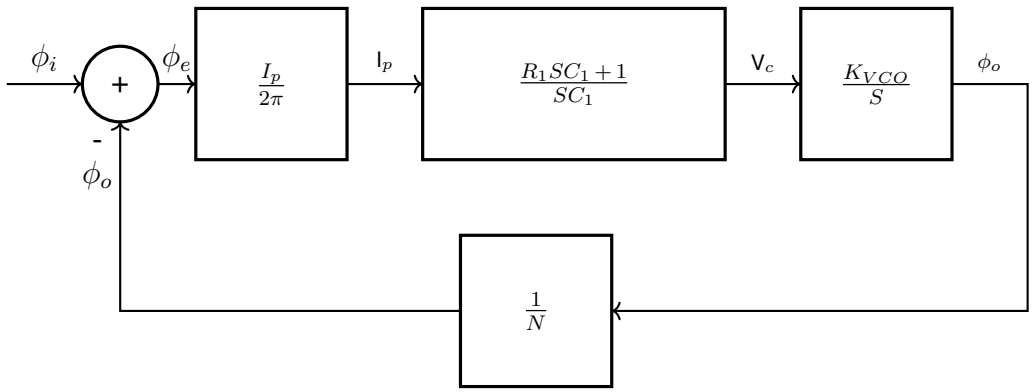

Figure 2.6: Block diagram of the linear phase PLL with each block transfer function.

$$A_{CL} = \frac{\frac{I_pK_{VCO}}{2\pi C_1}(R_1SC_1 + 1)}{S^2 + S\frac{I_p}{2\pi}K_{VCO}R_1 + \frac{I_pK_{VCO}}{2\pi C_1}} \tag{2.6}$$

From the closed-loop transfer function (2.6) one can see that the PLL behaves as a second-order system with two poles at the origin (two ideal integrators), opening up the possibility of instability. In order to ensure stability, the PLL must be designed to have a sufficiently high phase margin (ϕ_m), and consequently an adequate damping factor (ζ) and natural frequency (ω_n). Both ω_n (2.7) and ζ (2.8) are crucial parameters in the design of the PLL, as they determine the bandwidth and transient response of the system.

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}} \tag{2.7}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi}} \tag{2.8}$$

It can be proven that the loop bandwidth (ω_u) is related with ω_n and ζ by equation (2.9).

$$\omega_u^2 = (2\zeta^2 + \sqrt{4\zeta^4 + 1})\omega_n^2 \tag{2.9}$$

Phase frequency detector

A PLL that has a phase frequency detector (PFD) instead of just a phase detector (PD) is superior because it can track changes in both phase and frequency at the input signal. This approach provides robustness to the system because the PLL locks regardless of the initial value of the output frequency, therefore making the pull-in range equal to the VCO tuning range.

The most common implementation of a PFD is shown in figure 2.7. The operation of this circuit is as follows: When either of the two signals arrive with a rising edge to the corresponding D flip-flop CLK terminal a HIGH state is pass along to its output (Q), this result is maintained until the other signal's rising edge arrives at the second flip-flop because at that moment in time the AND gate would activate and reset both flip-flops. This behavior can be observed in figure 2.8.

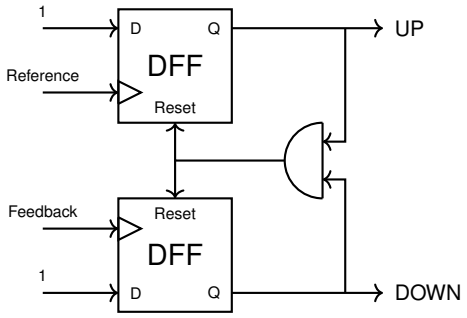

Figure 2.7: Three states PFD implementation.

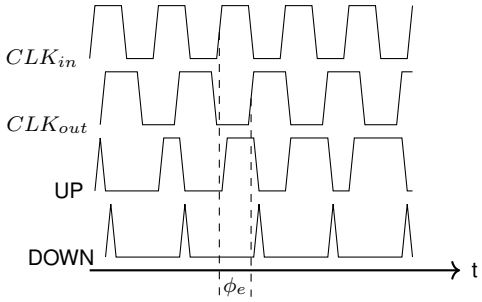

Figure 2.8: Transient response of the PFD.

Loop filter

The function of the loop filter is to filter out the high frequency noise from the VCO and to provide a stable control voltage to the VCO. The loop filter is usually a passive RC filter as the one in figure 2.5, but it can also be an active filter. The loop filter is a critical component of the PLL because it determines the bandwidth, the noise performance and the transient response of the PLL. The loop filter is usually designed to be a second-order low-pass filter, but it can also be a higher-order filter if needed. The values of the components of the filter should be designed first and foremost to achieve stability at a given bandwidth, equations (2.8) and (2.9) are useful for this purpose.

The -3dB closed-loop bandwidth and the open-loop unity-gain bandwidth are fairly close to each other for $\zeta \geq 1$. It is for this reason that both quantities are often used interchangeably. In order to achieve a good transient response and noise performance, the loop bandwidth should be set to a value of $\omega_{ref}/10\,[rad/s]$ or less, where ω_{ref} is the reference frequency.

Charge pump

Charge pumps (CP) are circuits designed to either source or sink charge to/from a capacitor for a controlled amount of time. There are many different implementations of charge pumps, but all of them consist of a current source, a switch and a capacitor (which is usually part of the loop filter).

Most of the PLLs designed today are CPPLLs (or type-II PLLs) because the combination of PFD/CP/LF exhibit an infinite gain for a finite phase error, which means that for the control voltage to be finite, the phase error must be zero. This is a desirable property because it allows the PLL to have a very low phase error. Figure 2.9 shows the diagram of a charge pump, while figure 2.10 shows the schematic of a CMOS drain switched charge pump.

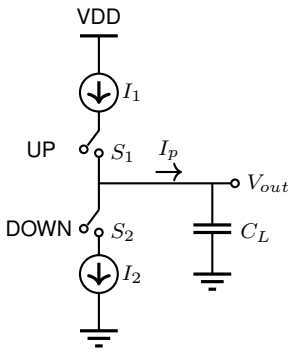

Figure 2.9: Charge pump schematic.

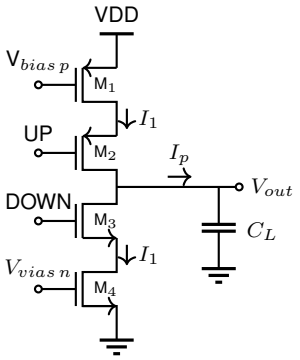

Figure 2.10: CMOS drain switched charge pump.

The greatest challenge in designing a charge pump resides in eliminating any current mismatch between I_1 and I_2 while maintaining a large output voltage compliance. This task is particularly difficult to achieve because the channel length modulation in the MOSFETs causes the output current to be dependent on the output voltage (V_{DS} modulates the current). This means that both the output voltage compliance and the lessening of the current mismatch trade off with each other.

There are multiple solutions to this problem (some involving more complex topologies dealing also with the issue of clock feedthrough), yet the simplest one is to use wide enough (also large enough in the case of the current sources) transistors to minimize the channel length modulation effect. This solution is far from ideal, but is good enough for some applications.

Voltage-controlled oscillator

The VCO is the block that generates the output signal of the PLL. The frequency of the output signal is determined by the control voltage that the loop filter provides. It is a non-linear circuit that converts a voltage into a frequency (though it can be assumed to be linear for the conditions mentioned in the previous section). The VCO response looks like that of figure 2.12, where the gain of the VCO (K_{VCO}) is an important design parameter. In general, it is desirable to have a relatively small (without compromising the stability of the PLL) K_{VCO} value so that any noise coupled to the previous stage does not translate into a large phase/frequency fluctuation at the output. A good rule of thumb is to keep K_{VCO} below $0.1 f_m Hz/V$ where f_m is the center frequency of the VCO tuning range.

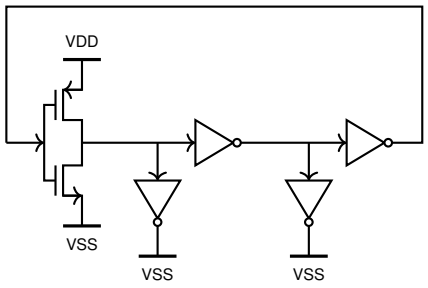

Figure 2.11: CMOS ring oscillator.

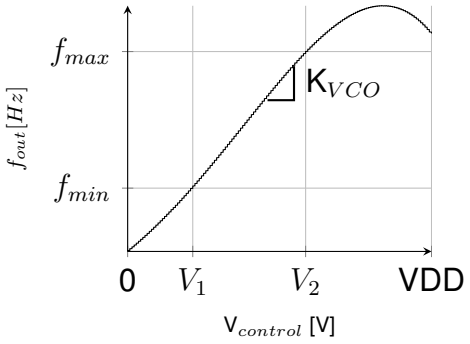

Figure 2.12: VCO characteristic curve.

There is a wide variety of VCOs, but the most common ones are the ring oscillator and the LC oscillator. The ring oscillator can be realized with CMOS inverters (Fig. 2.11) or with differential pairs, usually the former is preferred because is easier to implement, more compact and suffers less from mismatch. According to (2.10), the frequency of the ring oscillator is determined by the number of stages and the delay of each stage.

$$f_o = \frac{1}{2N\,t_p} \tag{2.10}$$

The analog frequency tuning is done by either changing the capacitance of

the load (varactor implementation) or by reducing the strength of the inverters (via changing the pull-up or pull-down resistance), figures 2.13 and 2.14 show both tuning methods respectively.

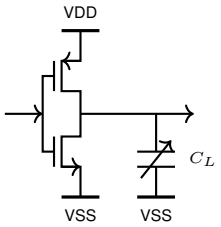

Figure 2.13: CMOS ring oscillator stage with varactor load tuning.

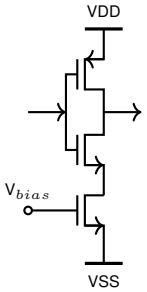

Figure 2.14: CMOS ring oscillator stage with resistive load tuning.

The LC oscillator is preferred for applications that require low phase noise and high frequency operation. This VCO is based on the resonator circuit (LC tank) shown in figure 2.15. The frequency of oscillation of an ideal LC tank is given by (2.11), in practice however, there's a need for an active device to compensate for the losses in the circuit and sustain oscillation. This losses, responsible for dampening the oscillation are primarily caused by the the parasitic series resistance of the inductor.

$$f_n = \frac{1}{2\pi\sqrt{LC}} \tag{2.11}$$

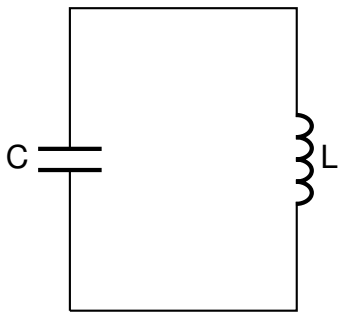

Figure 2.15: Ideal LC tank circuit.

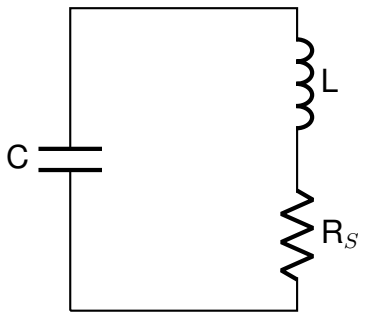

Figure 2.16: Real LC tank circuit.

The LC tank of figure 2.16 can be modeled as a parallel RLC circuit, where

the inductor is modeled as an ideal inductor in parallel with a resistor (R_p) and an ideal capacitor; the equivalent circuit is shown in figure 2.17. Equating the transfer functions of both 2.16 and 2.17 yields equation (2.12), which can be used to compute R_p.

$$-L^2\omega^2 + R_S R_P + j\omega L R_S = 0 \tag{2.12}$$

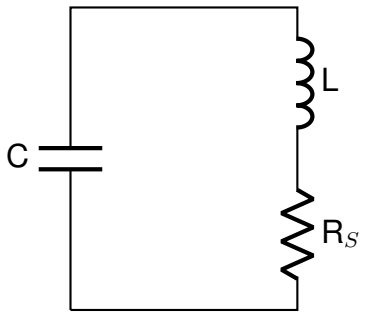

Figure 2.17: Equivalent LC tank circuit.

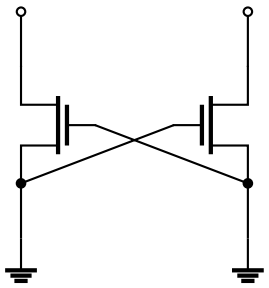

Figure 2.18: Cross-coupled pair.

The active circuit of figure 2.18 is known as a cross-coupled pair, it compensates for R_p with a negative resistance. In fact, by analyzing the small signal model of the cross-coupled pair the designer can arrive at equation (2.13), which allows to solve for the pair's transconductance (g_m). R_{pair} should be chosen $\gg R_p$ so that the former dominates in parallel with the latter (compensating for the losses).

$$R_{pair} = -\frac{2}{g_m} \tag{2.13}$$

The previous discussion focused on sustaining the oscillations of the LC tank, the control of the frequency is done by changing the capacitance of the tank. The most common way to do this is by using a varactor, such a device can be implemented with a MOSFET in the triode region and wiring it as shown in figure 2.19. The capacitance of the MOS varactor doesn't change linearly across all of the applied voltage. 2.20 shows the typical response of a MOS varactor in 65 nm, where it can be distinguished between three

regions: Accumulation region, depletion and inversion. The region of interest is the inversion region, where the capacitance changes approximately linearly.

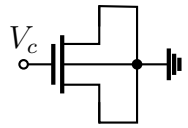

Figure 2.19: MOS varactor.

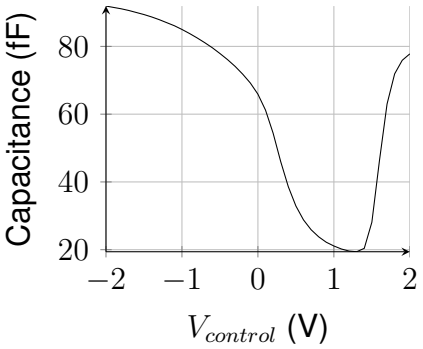

Figure 2.20: MOS varactor characteristic.

The tuning range can be extended by putting two varactors back to back on their gates. The final circuit of the cross-coupled pair VCO is shown in figure 2.21.

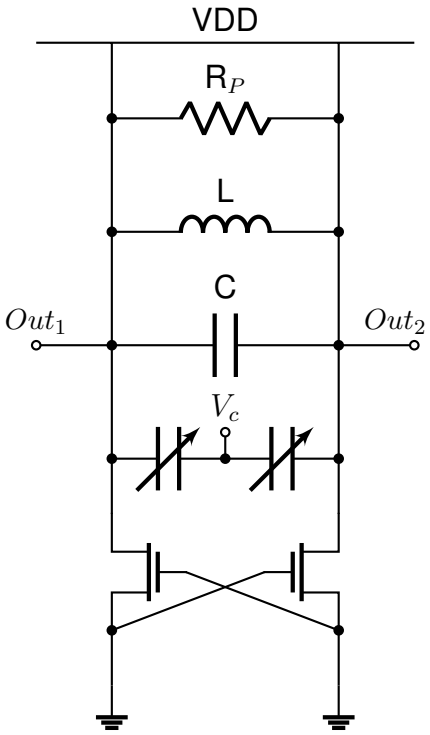

Figure 2.21: Cross-coupled pair VCO schematic.

Frequency divider

The frequency divider is a circuit that takes an input signal and produces an output signal with a frequency that is a fraction of the input frequency. The most common frequency divider is the flip-flop (fig. 2.22), which divides the input frequency by two, although there are other types of dividers that can divide by any integer number. The frequency divider is used in PLLs to reduce the frequency of the input signal to a level that can be processed by the other blocks of the PLL (to match the frequency of the reference signal).

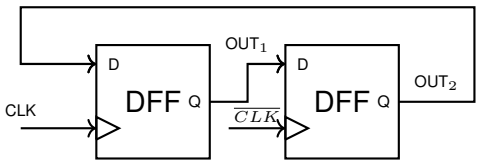

Figure 2.22: %2 frequency divider using D flip-flops.

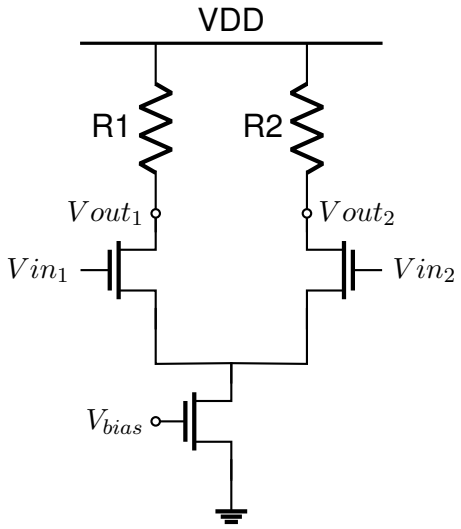

Figure 2.23: CML frequency divider.

Although the flip-flop is the most common frequency divider, there are other types of dividers that can be used in PLLs. One of the most relevant is the CML frequency divider (fig. 2.23), which is a type of frequency divider that uses current-mode logic (CML) to achieve high speed operation. CML dividers are typically used in high-speed applications, such as high-speed data communication systems, where the output of the VCO is too high to be processed by any regualr flip-flop. The CML frequency divider is based on the principle of current steering, where the input signal is used to control the current flowing through a branch of the differential pair.

A CML signal resembles a sinusoidal wave and has a lower harmonic

content than a regular square wave, yet its power consumption is higher because of the constant current through the circuit due to the current source of the differential pair.

2.2 Digital phase-locked loop

anan

2.2.1 Time-to-digital converter

1. Fundamental Role of Phase Detection in PLLs

The core function of a Phase-Locked Loop (PLL) is to align the phase and frequency of an output signal with a reference input, a process heavily dependent on the accuracy of phase detection. Traditional PLLs employ a Phase-Frequency Detector (PFD) combined with a charge pump (CP) to generate an analog error signal proportional to the phase difference. While effective, this approach faces limitations in advanced CMOS nodes (e.g., 65nm and below), where analog components suffer from increased leakage current, supply noise sensitivity, and device mismatch. These challenges have driven the adoption of Time-to-Digital Converters (TDCs), which digitize phase error measurements, enabling fully digital or hybrid PLL architectures with improved resolution and scalability. 2. Operating Principle of TDC-Based Phase Detection

A TDC measures the time interval between two events—typically the rising edges of the reference clock (REF) and the feedback clock (DIV) from the voltage-controlled oscillator (VCO). Unlike a PFD, which produces a continuous analog output, a TDC quantizes the time difference into a digital word, making it inherently compatible with digital loop filters and control systems. The most common TDC implementation in PLLs is the delay-line TDC, where a chain of buffer stages propagates the time difference, and flip-flops

sample the state of the delay line to generate a binary-coded output.

The resolution of a delay-line TDC is determined by the propagation delay of a single stage (Δ_t). In deep-submicron processes like 65nm CMOS, gate delays can be extremely small (on the order of picoseconds), allowing for high-precision phase detection. However, nonlinearities in the delay line due to process variations and temperature fluctuations introduce differential nonlinearity (DNL) and integral nonlinearity (INL), which degrade PLL performance. To mitigate these effects, advanced calibration techniques, such as least-mean-square (LMS) algorithms or dynamic element matching (DEM), are employed to correct quantization errors dynamically. 3. Advantages of TDC-Based PLLs Over Conventional Architectures

The shift from analog PFDs to TDCs in PLL design is motivated by several key advantages:

Superior Phase Resolution: TDCs can achieve sub-picosecond resolution, enabling ultra-low-jitter clock generation, which is critical in high-speed communication systems like SerDes and RF synthesizers.

Digital Process Compatibility: As CMOS technology scales, analog components become increasingly difficult to design due to reduced voltage headroom and increased variability. TDCs, being primarily digital, are more robust in advanced nodes.

Reduced Sensitivity to Supply Noise: Unlike charge pumps, which are highly susceptible to power supply fluctuations, TDCs operate in the time domain, making them less affected by voltage noise.

Easier Integration with Digital Calibration: Since the TDC output is digital, it can be processed using adaptive algorithms to compensate for process, voltage, and temperature (PVT) variations.

However, TDCs are not without trade-offs. Their quantization noise

introduces phase error that must be filtered by the PLL loop, and their limited dynamic range makes them unsuitable for initial frequency acquisition in wide-band PLLs. This limitation has led to the development of hybrid PFD-TDC architectures, where a coarse PFD handles frequency locking, and the TDC refines phase alignment once the PLL is near lock. 4. Challenges in TDC Design and Emerging Solutions

Despite their benefits, TDC-based PLLs face several design challenges that must be addressed to achieve optimal performance:

Nonlinearity and Metastability Variations in delay stages cause nonlinearities, while sampling uncertainties can lead to metastability in the flip-flops capturing the TDC output. Recent solutions include Vernier delay-line TDCs, which use two delay lines with slightly different delays to improve resolution, and time amplifiers, which stretch small time intervals before digitization to reduce quantization error.

Power Consumption vs. Resolution Trade-off Higher resolution requires longer delay lines or more complex architectures, increasing power consumption. Two-step TDCs and successive-approximation register (SAR) TDCs have been proposed to reduce power while maintaining precision.

Dynamic Range Limitations Pure TDC-based PLLs struggle with large frequency offsets, necessitating hybrid approaches. An alternative is the bang-bang PLL (BBPLL), which uses a binary TDC for simplicity but requires careful loop stabilization.

5. Evolution of TDC Architectures and Future Directions

Recent advancements in TDC design focus on improving linearity, resolution, and power efficiency. Noise-shaping TDCs, inspired by delta-sigma modulation, push quantization noise to higher frequencies, where it can be filtered by the PLL loop. Gated ring oscillator (GRO) TDCs offer inherent noise filtering by only activating during measurement intervals, while

SAR-TDCs reduce conversion time and energy consumption through binary search techniques.

The integration of machine learning for adaptive TDC calibration is an emerging trend, where real-time algorithms adjust delay-line characteristics to compensate for PVT variations. Furthermore, the rise of all-digital PLLs (ADPLLs) has solidified the TDC's role as a critical component in next-generation clocking systems, particularly in applications requiring ultra-low jitter and fast locking, such as 5G transceivers and high-performance computing.

TDC as a phase detector

Delay-locked loop fundamentals

2.2.2 Digital loop filter

2.2.3 Digitally controlled oscillator

Chapter 3

Literature review

Recent advancements in Phase-Locked Loop (PLL) design have increasingly incorporated Time-to-Digital Converters (TDCs) as replacements for traditional analog phase detectors. This shift enables higher resolution, better scalability in advanced CMOS nodes, and improved noise performance. This literature review examines key contributions from recent research (2022-2025), focusing on architectural innovations, calibration techniques, and performance metrics in TDC-based PLL designs. Hybrid and Digital-Intensive PLL Architectures Calibrated Dual-Referenced Interpolating TDC

A significant contribution in 28nm CMOS technology demonstrated a fractional-N Digital PLL (DPLL) employing a dual-interpolated TDC (DI-TDC) to address process-voltage-temperature (PVT) induced non-uniform resolution [$\mathbf{di\_tdc\_2023}$]. This design implemented foreground and background calibration to match TDC resolution to the Digitally Controlled Oscillator (DCO) period, achieving -17.5 dBc integrated phase noise at 570 MHz while occupying only 0.019 mm² active area. The architecture eliminates the need for delta-sigma modulators, thereby reducing quantization noise, though it requires complex calibration logic for wide frequency operation (475 MHz to 1.1 GHz). Fast-Locking Hybrid Architectures

A hybrid approach combining TDC with adaptive charge pump in 180nm CMOS demonstrated significant improvements in lock time [$\mathbf{hybrid\_pll\_2022}$]. This design used the TDC to quantize phase errors and dynamically enable a secondary charge pump, achieving 1.11 μs lock time while maintaining -98.07 dBc/Hz phase noise at 1 MHz offset. The architecture presents an effective compromise between analog and digital implementations, though it highlights the persistent trade-off between TDC resolution and power consumption in scaled technologies. Low-Power and IoT-Optimized Designs Calibration-Free RO-Based TDC

A notable innovation for IoT applications appeared in a 40nm ADPLL that reused a ring oscillator (RO) as both the DCO and TDC delay line [$\mathbf{ro\_tdc\_2023}$]. This self-referencing approach automatically tracks the DCO period with the TDC step, achieving 1.4 mW power consumption and -114 dBc/Hz phase noise at 1 MHz offset. The design's calibration-free operation significantly simplifies implementation for Bluetooth Low Energy (BLE) applications, though it requires careful RO tuning to mitigate injection-locking induced differential nonlinearity (DNL) errors. Ultra-Low Power Implementations

Recent divider-less ADPLL architectures have pushed power efficiency boundaries by employing embedded TDCs. A 65nm accumulator-based design achieved 0.53 mW power consumption and 0.87 ps RMS jitter through combination of a class-F^{-1} DCO with narrow-range TDC [$\mathbf{low\_power\_2024}$]. This approach demonstrates the potential for eliminating dividers to reduce quantization noise, though it demands exceptionally high TDC linearity. Advanced Calibration Techniques Noise-Shaping TDCs

Delta-sigma based TDCs have emerged as a powerful technique for quantization noise suppression [$\mathbf{noise\_shaping\_2023}$]. By shaping noise to higher frequencies, these implementations have demonstrated 10-15 dB improvement in in-band phase noise, becoming particularly valuable for

high-performance RF synthesizers in 5G and Wi-Fi applications. PVT-Robust Designs

A 12nm ADPLL implementation addressed PVT variations through digitally controlled delay inverters (DCDIs) that calibrate TDC buffers in real-time [pvt_robust_2024]. This approach maintains sub-picosecond resolution across process corners, though it introduces calibration overhead that increases design complexity. Emerging Topologies and Future Directions Successive-Approximation TDCs

SAR-TDCs have shown promise in reducing conversion latency and power consumption. A 28nm implementation achieved 543 fs RMS jitter at just 0.82 mW power [sar_tdc_2023], demonstrating the efficiency of binary search approaches in time-domain conversion. Time-Amplification Techniques

Time-amplifier-assisted TDCs represent a cutting-edge development, enabling sub-100 fs resolution by amplifying picosecond-scale time differences prior to digitization [time_amp_2024]. These techniques are particularly relevant for next-generation high-precision applications. Performance Comparison

Table 3.1 summarizes key metrics from state-of-the-art implementations:

Table 3.1: Performance Summary of State-of-the-Art TDC-PLLs

Metric	Value	Technology	Technique
Phase Noise	-114 dBc/Hz @1MHz	40nm CMOS	RO-based TDC
Power	0.38 mW	40nm CMOS	Accumulator-based
Jitter	320 fs RMS	65nm CMOS	Noise-shaping
Lock Time	1.11 µs	180nm CMOS	TDC-assisted CP
Area	0.019 mm^2	28nm CMOS	DI-TDC

Challenges and Future Directions

Current research faces several key challenges:

- The linearity versus power trade-off remains problematic for high-resolution TDCs
- Sub-10nm integration requires digitally intensive TDCs with self-healing capabilities
- Wideband applications demand multi-core architectures for GHz-range operation

Future work will likely focus on machine learning for adaptive calibration and 3D-integrated TDCs for next-generation systems.

TDC-Based PLLs with Full-Range Phase Acquisition ($\pm 2\pi$) 1. Hybrid PFD-TDC Architectures for Extended Range

A key innovation in CN101753142B addresses the limited pull-in range of conventional TDCs by integrating:

- A coarse phase-frequency detector (PFD) for initial frequency acquisition
- A fine-resolution TDC for phase tracking
- A frequency detector that converts frequency errors to digital codes 4

This hybrid approach enables operation across the full $\pm 2\pi$ range by:

- Using the PFD to handle large frequency offsets (beyond the TDC's native range)
- Switching to the TDC for high-resolution phase alignment once the PLL is near lock
- Employing a delay-line TDC with intermediate node taps to detect both phase and frequency errors 4

2. Dual-Loop Gain Techniques

The bang-bang PLL in 18 demonstrates an alternative method using:

- Two discrete loop gains (inner and outer loops)
- A quaternary phase detector that toggles between gains based on phase error magnitude
- Outer loop optimized for pull-in range ($\pm 2\pi$ capability)
- Inner loop optimized for jitter performance during lock 18

Key equations derived show the pull-in range depends primarily on the outer loop gain, freeing the inner loop for noise optimization 18. 3. State-of-the-Art Performance Tradeoffs

Recent designs face critical challenges:

- Power vs. Resolution: High-resolution TDCs (<1ps) in 4 consume more power during full-range operation
- Linearity: Delay-line mismatches in TDCs introduce nonlinearities that complicate wide-range operation 4
- Lock Time: Hybrid architectures in 418 show 20-30% faster locking than pure TDC-PLLs

4. Emerging Solutions

Innovations to enhance $\pm 2\pi$ capability include:

- Time Amplifiers: Stretch small time differences before TDC digitization 4
- Noise-Shaping TDCs: Improve in-band resolution while maintaining wide range 4
- Adaptive Calibration: Background calibration of TDC nonlinearities

during operation 4

5. Comparative Analysis [1]

Table 3.2: Comparison of Full-Range ($\pm 2\pi$) TDC-Based PLL Architectures

Design	**Technology**	**Range**	**Resolution**	**Lock Time**
Hybrid PFD-TDC [**hybrid_patent**]	65nm CMOS	$\pm 2\pi$	$<$5ps	$<2\mu$s
Dual-Loop BB-PLL [**dual_loop**]	180nm CMOS	$\pm 2\pi$	Coarse/Fine	1.5μs
RO-TDC ADPLL [**ro_tdc**]	40nm CMOS	$\pm \pi/2$	1.2ps	5μs
SAR-TDC PLL [**sar_tdc**]	28nm CMOS	$\pm 2\pi$	543fs	3μs

Chapter 4

Methodology

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Chapter 5

Results

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Chapter 6

Discussion

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Chapter 7

Conclusion

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Appendix A

Appendix

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[1] Mark Van Paemel. “Analysis of a charge-pump PLL: A new model”. In: *IEEE Transactions on communications* 42.7 (1994), pp. 2490–2498.