Design of a time-to-digital converter to be used as a phase detector in a PLL in 65 nm technology

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July 9, 2025

Abstract

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Contents

List of figures **9**

List of tables **10**

1 Introduction **11**

1.1 Context and motivation 12

1.1.1 Low jitter PLLs in modern IC design 12

1.1.2 Limitations of analog PLLs 12

1.1.3 Limitations of traditional PFDs 12

1.2 Problem statement 12

1.3 Objectives 12

1.3.1 General objective 12

1.3.2 Specific objectives 12

1.4 Significance 12

1.4.1 Academic significance 12

1.4.2 Industry significance 12

1.5 Scope and limitations 12

1.6 Thesis roadmap 12

2 Theoretical framework **13**

2.1 Phase-locked loop fundamentals 13

2.1.1 Basic concept 13

2.1.2 Key PLL parameters 14

2.1.3 Analog phase-locked loop 18
2.2 Digital phase-locked loop 29
2.2.1 Time-to-digital converter 29
2.2.2 Digital loop filter 29
2.2.3 Digitally controlled oscillator 29

3 Literature review **30**

4 Methodology **32**

5 Results **34**

6 Discussion **36**

7 Conclusion **38**

A Appendix **40**

List of Figures

2.1 a) PFD block. 16
2.2 b) PFD output. 16
2.3 Block diagram of the linear phase PLL. 19
2.4 VCO characteristic example. 19
2.5 Second-order passive loop filter. 19
2.6 Block diagram of the linear phase PLL with each block transfer function. 20
2.7 Three states PFD implementation. 22
2.8 Transient response of the PFD. 22
2.9 Charge pump schematic. 23
2.10 CMOS drain switched charge pump. 23
2.11 CMOS ring oscillator. 24
2.12 VCO characteristic curve. 24
2.13 CMOS ring oscillator stage with varactor load tuning. 25
2.14 CMOS ring oscillator stage with resistive load tuning. 25
2.15 Ideal LC tank circuit. 25
2.16 Real LC tank circuit. 25
2.17 Equivalent LC tank circuit. 26
2.18 Cross-coupled pair. 26
2.19 MOS varactor. 27
2.20 MOS varactor characteristic. 27
2.21 Cross-coupled pair VCO schematic. 27
2.22 MOS varactor. 28

2.23 MOS varactor characteristic. 28

List of Tables

Chapter 1

Introduction

1.1 Context and motivation

1.1.1 Low jitter PLLs in modern IC design

1.1.2 Limitations of analog PLLs

1.1.3 Limitations of traditional PFDs

1.2 Problem statement

1.3 Objectives

1.3.1 General objective

1.3.2 Specific objectives

1.4 Significance

1.4.1 Academic significance

1.4.2 Industry significance

Clock generation

SerDes

Chapter 2

Theoretical framework

2.1 Phase-locked loop fundamentals

2.1.1 Basic concept

The PLL is a feedback control system that is used to synchronize the phase and frequency of an output signal to a reference signal. The reference signal is a very stable clock signal locally generated usually by a crystal oscillator. The PLL compares the phase of this reference signal with the phase of the output signal and generates an error signal that is used to adjust the frequency of the output signal.

There's two types of applications for PLLs broadly speaking: clock generation and clock data recovery. In the first case, the PLL is used to generate a clock signal that is synchronized to the reference signal. In the second case, the PLL is used to recover the clock signal from a data stream.

The PLL consists of three main components: a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). The PD compares the phase of the reference signal with the phase of the output signal and generates an error signal that is proportional to the phase difference between

the two signals. The LF smooths out the ripple riddled signal generated by the PD, reduces the high frequency noise of the loop and provides a stable control voltage to the VCO. The VCO generates an output signal whose frequency is proportional to the control voltage. Lastly, the output signal is fed back to the PD, thereby creating a closed-loop system.

If the PLL also has a frequency divider in the feedback path, the system is also capable of generating a frequency that is a multiple or fraction of the reference frequency. This is useful in applications where a higher frequency is needed, such as in RF synthesizers.

2.1.2 Key PLL parameters

Phase noise / jitter

Jitter is defined as the time deviation (Δ_t) of a signal's transition edges from their ideal positions in time. It is a metric of the outmost importance in the design of PLLs as it is a direct measure of the quality of the clock signal generated. Phase noise describes the same phenomenon in the frequency domain (the phase noise of a signal is the Fourier transform of the jitter) and is usually expressed in dBc/Hz.

Output frequency

It is defined as the range of frequencies that the PLL is capable of generating and can be determined by the VCO output range and the division ratio of the feedback frequency divider. This is a key metric in establishing the application of the PLL (e.g., clock generation or RF synthesizer) and it bears significant importance in the design process due to the tradeoff it has with the phase noise performance of the PLL.

Loop bandwidth

The closed-loop bandwidth of a PLL is the frequency range over which the PLL can track the phase/frequency variations of the input signal (from DC to either -3 dB from the open-loop gain or to the unity-gain frequency at 0 dB). It affects the acquisition time and phase noise performance of the PLL.

Noise bandwidth

It is the PLL's noise due to the filter's loop bandwidth, the higher frequencies of the voltage-controlled oscillator (VCO) are the major contributor to this effect, therefore the need to set a low enough bandwidth in order to suppress the most out of it. Even if reducing the loop bandwidth would be desirable to suppress in-band phase noise, it's also necessary to take into consideration that there is a tradeoff between the lock-in time and in-band phase noise.

Beat-note period

Defined as the time interval between successive "beats" (oscillations) observed at the phase detector output, in other words, is the inverse of the frequency difference's magnitude between the reference and feedback signals as shown in figure 2.2. Beat-note period is closely related to the acquisition time of the PLL and can be estimated by equation (2.1). This metric is a direct measure of the frequency mismatch between the reference and the feedback signals.

$$T_{beat} = \frac{1}{|f_{ref} - f_{feed}|} \tag{2.1}$$

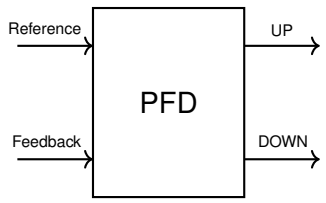

Figure 2.1: a) PFD block.

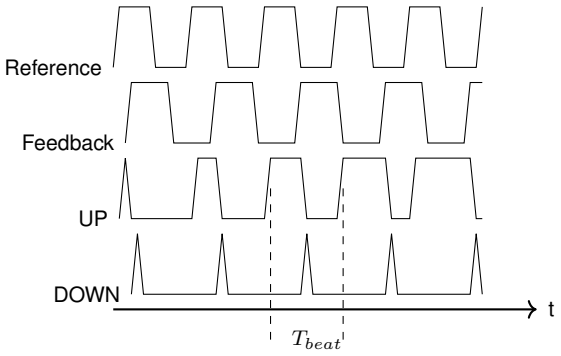

Figure 2.2: b) PFD output.

Lock-in time

Lock-in time (also called aquisition or settling time) is defined as the time for the PLL to lock on to the input reference phase and frequency within one beat-note period (T_{beat}) after a frequency change or startup of the system. This parameter measures the time required for the PLL to achieve the final phase lock once the VCO frequency is within the lock-in range. The lock-in time can be estimated with equation (2.2).

$$T_{lock-in} = \frac{ln(\epsilon)}{\zeta\omega_n} \tag{2.2}$$

where:

$\epsilon =$ acceptable phase error

$\zeta =$ damping factor

$\omega_n =$ natural frequency

Pull-in time

In contrast with the lock-in time, the pull-in time is the required amount of time for the PLL to initially aquire lock on to the reference signal from an

arbitrary starting frequency (when the VCO's initial frequency is far from the target).

Lock-in range

The frequency range within which the PLL locks to the reference frequency in one T_{beat}. Once the feedback signal is in this range, the PLL will enter lock state within the next T_{beat}.

Pull-in range

Range of frequency within which the PLL can aquire lock on to the reference signal once the VCO has the correct frequency and several beat-note periods have passed.

Pull-out range

The maximum allowed frequency or phase abrupt change applied to the reference signal beyond which the PLL unlocks.

Hold range

This parameter establishes the maximun theoretical frequency range for an input reference beyond which the PLL never locks. Hold range is bigger than both lock-in and pull-in ranges.

SNR

The signal to noise ratio is an appropiate way to measure the impact of noise on a circuit. It's often used in most figures of merit (FOM) for making fair comparisons between PLLs.

Power consumption

An important parameter in measuring the performance of integrated circuits. Often used in most FOMs.

Spurs

Spurious tones are unwanted periodic signals that appear at the output spectrum of the PLL. Spurs are completely deterministic, thus they are distinct from phase noise which is random and spreads across the spectrum of the signal.

2.1.3 Analog phase-locked loop

The principles of operation of the digital PLL stem from its analog counterpart, therefore this subsection describes the fundamental building blocks of the analog PLL as well as a simplified model of the system which allows for the circuit designer to analyze its behavior.

Linear phase model of the PLL

The PLL is a non-linear system, yet it can be approximated quite accurately into the linear system of figure 2.1 if certain assumptions are taken in to consideration. The first of this assumptions is that the phase error (ϕ_e) must be small enough, meaning the PLL is near lock state. Another one is that the characteristic of the phase detector must be approximately linear and given by (2.3). Lastly, the VCO's tuning range must be within its linear region of operation (it is generally desirable to limit the variation of K_{VCO} to no more than 20%) like the frequency range between ω_1 and ω_2 in figure 2.4, only in this conditions the VCO can be considered a linear system and thus be described by (2.4).

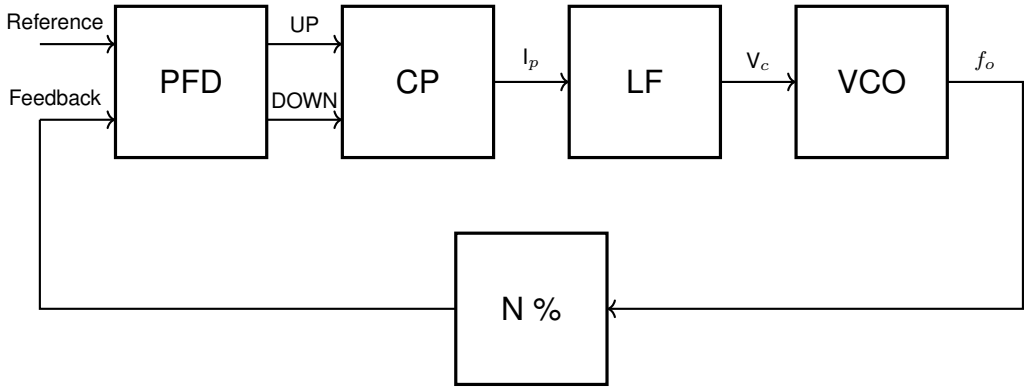

Figure 2.3: Block diagram of the linear phase PLL.

$$v_d = K_{PD}\,\phi e + \underbrace{V_{do}}_{\text{free running voltage}} \tag{2.3}$$

$$\Delta_{\omega_o} = K_{VCO}\,(V_c - V_{co}) \tag{2.4}$$

Each of the blocks in 2.3 has a transfer function associated with it, which can be expressed as follows: The PFD/CP combination is modeled as a current source with a gain of $I_p/2\pi$. The VCO is modeled as an ideal integrator with gain K_{VCO} and its transfer function is given by K_{VCO}/S. The feedback divider is modeled as a simple gain of $1/N$. Finally, the loop filter (LF) depends on the order of the filter and the type of components used.

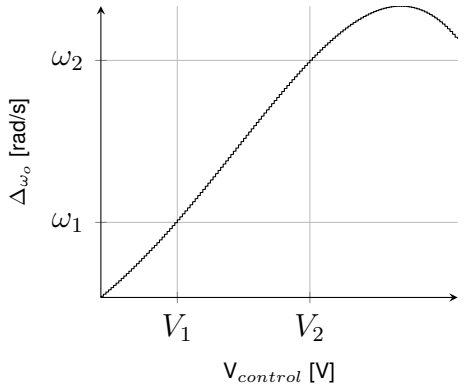

Figure 2.4: VCO characteristic example.

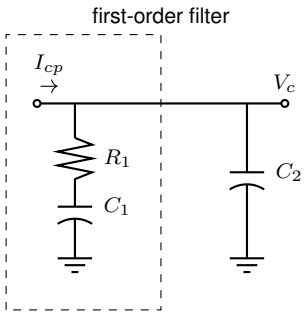

Figure 2.5: Second-order passive loop filter.

The most common implementation is a passive RC filter, which can be modeled either as a first-order or a second-order system. For the sake of sim-

plicity in this analysis, the LF is modeled as a first-order circuit like the one enclosed by dashed lines in figure 2.5. The transfer function of the LF is then given by $(R_1SC_1 + 1)/(SC_1)$.

Knowing the transfer functions of each block, one can represent the PLL system as in figure 2.6. Then with the help of Mason's rule (2.5), the overall closed-loop transfer function (2.6) of the PLL can be obtained.

$$H(s) = \frac{\Sigma_{F.P}(1 - \Sigma_{loops\,not\,touching})}{1 - \Sigma_{loops}} \tag{2.5}$$

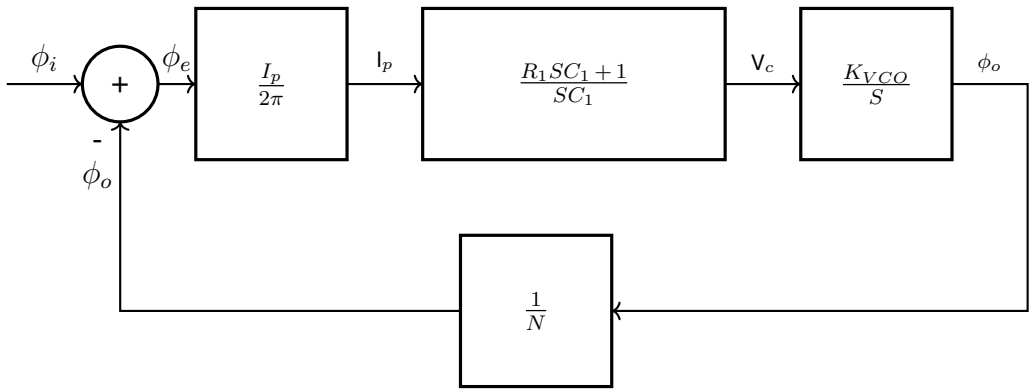

Figure 2.6: Block diagram of the linear phase PLL with each block transfer function.

$$A_{CL} = \frac{\frac{I_pK_{VCO}}{2\pi C_1}(R_1SC_1 + 1)}{S^2 + S\frac{I_p}{2\pi}K_{VCO}R_1 + \frac{I_pK_{VCO}}{2\pi C_1}} \tag{2.6}$$

From the closed-loop transfer function (2.6) one can see that the PLL behaves as a second-order system with two poles at the origin (two ideal integrators), opening up the possibility of instability. In order to ensure stability, the PLL must be designed to have a sufficiently high phase margin (ϕ_m), and consequently an adequate damping factor (ζ) and natural frequency (ω_n). Both ω_n (2.7) and ζ (2.8) are crucial parameters in the design of the PLL, as they determine the bandwidth and transient response of the system.

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}} \tag{2.7}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi}} \tag{2.8}$$

It can be proven that the loop bandwidth (ω_u) is related with ω_n and ζ by equation (2.9).

$$\omega_u^2 = (2\zeta^2 + \sqrt{4\zeta^4 + 1})\omega_n^2 \tag{2.9}$$

Phase frequency detector

A PLL that has a phase frequency detector (PFD) instead of just a phase detector (PD) is superior because it can track changes in both phase and frequency at the input signal. This approach provides robustness to the system because the PLL locks regardless of the initial value of the output frequency, therefore making the pull-in range equal to the VCO tuning range.

The most common implementation of a PFD is shown in figure 2.7. The operation of this circuit is as follows: When either of the two signals arrive with a rising edge to the corresponding D flip-flop CLK terminal a HIGH state is pass along to its output (Q), this result is maintained until the other signal's rising edge arrives at the second flip-flop because at that moment in time the AND gate would activate and reset both flip-flops. This behavior can be observed in figure 2.8.

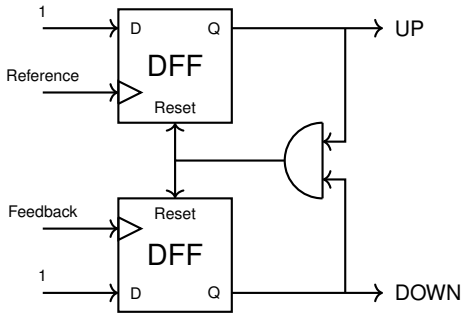

Figure 2.7: Three states PFD implementation.

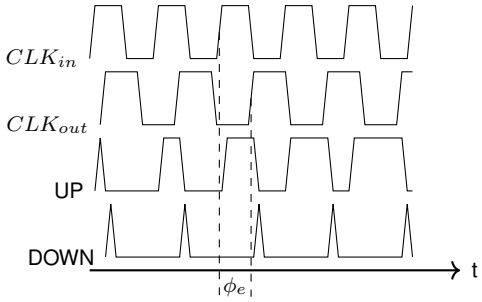

Figure 2.8: Transient response of the PFD.

Loop filter

The function of the loop filter is to filter out the high frequency noise from the VCO and to provide a stable control voltage to the VCO. The loop filter is usually a passive RC filter as the one in figure 2.5, but it can also be an active filter. The loop filter is a critical component of the PLL because it determines the bandwidth, the noise performance and the transient response of the PLL. The loop filter is usually designed to be a second-order low-pass filter, but it can also be a higher-order filter if needed. The values of the components of the filter should be designed first and foremost to achieve stability at a given bandwidth, equations (2.8) and (2.9) are useful for this purpose.

The -3dB closed-loop bandwidth and the open-loop unity-gain bandwidth are fairly close to each other for $\zeta \geq 1$. It is for this reason that both quantities are often used interchangeably. In order to achieve a good transient response and noise performance, the loop bandwidth should be set to a value of $\omega_{ref}/10\,[rad/s]$ or less, where ω_{ref} is the reference frequency.

Charge pump

Charge pumps (CP) are circuits designed to either source or sink charge to/from a capacitor for a controlled amount of time. There are many different implementations of charge pumps, but all of them consist of a current source, a switch and a capacitor (which is usually part of the loop filter).

Most of the PLLs designed today are CPPLLs (or type-II PLLs) because the combination of PFD/CP/LF exhibit an infinite gain for a finite phase error, which means that for the control voltage to be finite, the phase error must be zero. This is a desirable property because it allows the PLL to have a very low phase error. Figure 2.9 shows the diagram of a charge pump, while figure 2.10 shows the schematic of a CMOS drain switched charge pump.

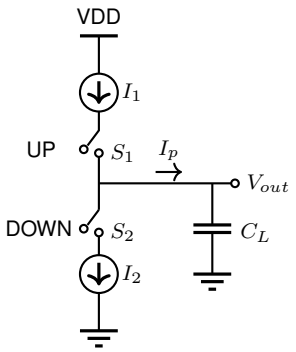

Figure 2.9: Charge pump schematic.

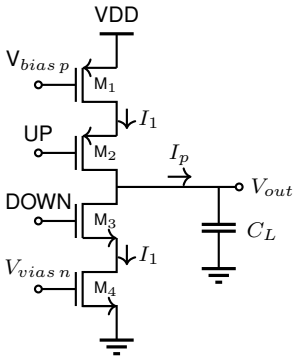

Figure 2.10: CMOS drain switched charge pump.

The greatest challenge in designing a charge pump resides in eliminating any current mismatch between I_1 and I_2 while maintaining a large output voltage compliance. This task is particularly difficult to achieve because the channel length modulation in the MOSFETs causes the output current to be dependent on the output voltage (V_{DS} modulates the current). This means that both the output voltage compliance and the lessening of the current mismatch trade off with each other.

There are multiple solutions to this problem (some involving more complex topologies dealing also with the issue of clock feedthrough), yet the simplest one is to use wide enough (also large enough in the case of the current sources) transistors to minimize the channel length modulation effect. This solution is far from ideal, but is good enough for some applications.

Voltage-controlled oscillator

The VCO is the block that generates the output signal of the PLL. The frequency of the output signal is determined by the control voltage that the loop filter provides. It is a non-linear circuit that converts a voltage into a frequency (though it can be assumed to be linear for the conditions mentioned in the previous section). The VCO response looks like that of figure 2.12, where the gain of the VCO (K_{VCO}) is an important design parameter. In general, it is desirable to have a relatively small (without compromising the stability of the PLL) K_{VCO} value so that any noise coupled to the previous stage does not translate into a large phase/frequency fluctuation at the output. A good rule of thumb is to keep K_{VCO} below $0.1 f_m Hz/V$ where f_m is the center frequency of the VCO tuning range.

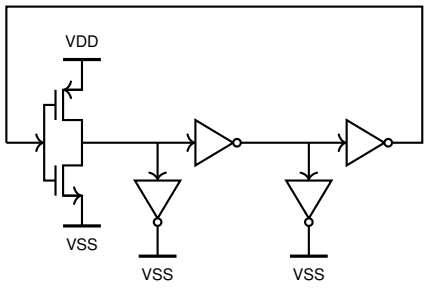

Figure 2.11: CMOS ring oscillator.

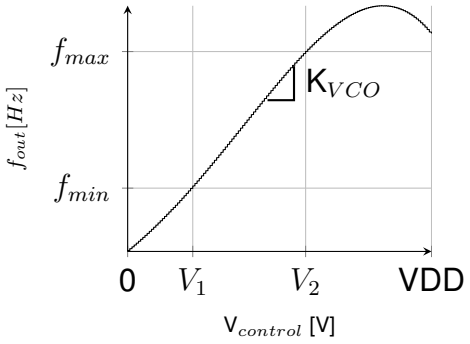

Figure 2.12: VCO characteristic curve.

There is a wide variety of VCOs, but the most common ones are the ring oscillator and the LC oscillator. The ring oscillator can be realized with CMOS inverters (Fig. 2.11) or with differential pairs, usually the former is preferred because is easier to implement, more compact and suffers less from mismatch. According to (2.10), the frequency of the ring oscillator is determined by the number of stages and the delay of each stage.

$$f_o = \frac{1}{2N\,t_p} \tag{2.10}$$

The analog frequency tuning is done by either changing the capacitance of

the load (varactor implementation) or by reducing the strength of the inverters (via changing the pull-up or pull-down resistance), figures 2.13 and 2.14 show both tuning methods respectively.

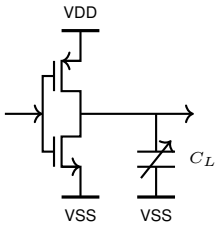

Figure 2.13: CMOS ring oscillator stage with varactor load tuning.

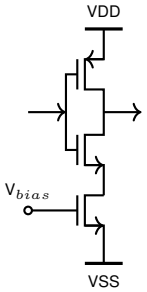

Figure 2.14: CMOS ring oscillator stage with resistive load tuning.

The LC oscillator is preferred for applications that require low phase noise and high frequency operation. This VCO is based on the resonator circuit (LC tank) shown in figure 2.15. The frequency of oscillation of an ideal LC tank is given by (2.11), in practice however, there's a need for an active device to compensate for the losses in the circuit and sustain oscillation. This losses, responsible for dampening the oscillation are primarily caused by the the parasitic series resistance of the inductor.

$$f_n = \frac{1}{2\pi\sqrt{LC}} \tag{2.11}$$

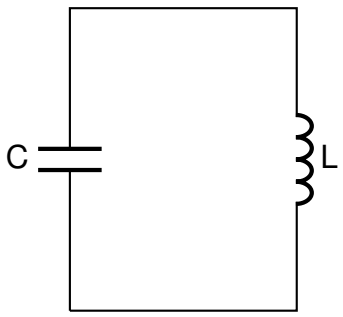

Figure 2.15: Ideal LC tank circuit.

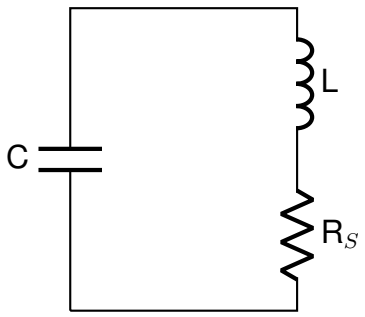

Figure 2.16: Real LC tank circuit.

The LC tank of figure 2.16 can be modeled as a parallel RLC circuit, where

the inductor is modeled as an ideal inductor in parallel with a resistor (R_p) and an ideal capacitor; the equivalent circuit is shown in figure 2.17. Equating the transfer functions of both 2.16 and 2.17 yields equation (2.12), which can be used to compute R_p.

$$-L^2\omega^2 + R_S R_P + j\omega L R_S = 0 \tag{2.12}$$

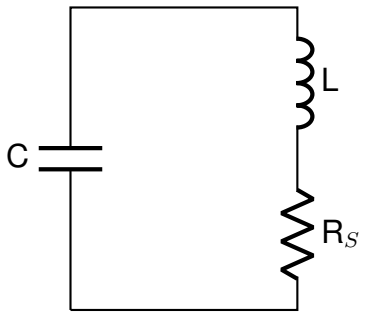

Figure 2.17: Equivalent LC tank circuit.

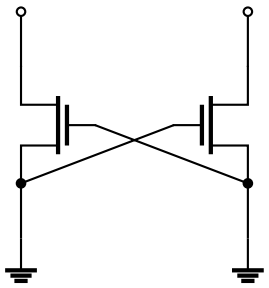

Figure 2.18: Cross-coupled pair.

The active circuit of figure 2.18 is known as a cross-coupled pair, it compensates for R_p with a negative resistance. In fact, by analyzing the small signal model of the cross-coupled pair the designer can arrive at equation (2.13), which allows to solve for the pair's transconductance (g_m). R_{pair} should be chosen $\gg R_p$ so that the former dominates in parallel with the latter (compensating for the losses).

$$R_{pair} = -\frac{2}{g_m} \tag{2.13}$$

The previous discussion focused on sustaining the oscillations of the LC tank, the control of the frequency is done by changing the capacitance of the tank. The most common way to do this is by using a varactor, such a device can be implemented with a MOSFET in the triode region and wiring it as shown in figure 2.22. The capacitance of the MOS varactor doesn't change linearly across all of the applied voltage. 2.23 shows the typical response of a MOS varactor in 65 nm, where it can be distinguished between three

regions: Accumulation region, depletion and inversion. The region of interest is the inversion region, where the capacitance changes approximately linearly.

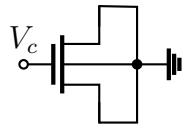

Figure 2.19: MOS varactor.

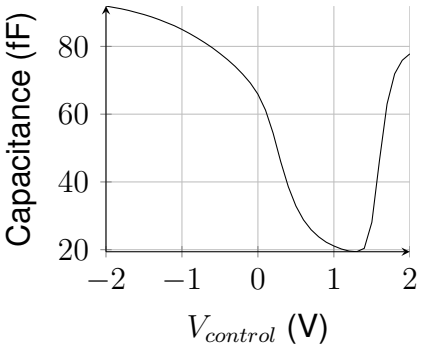

Figure 2.20: MOS varactor characteristic.

The tuning range can be extended by putting two varactors back to back on their gates. The final circuit of the cross-coupled pair VCO is shown in figure 2.21.

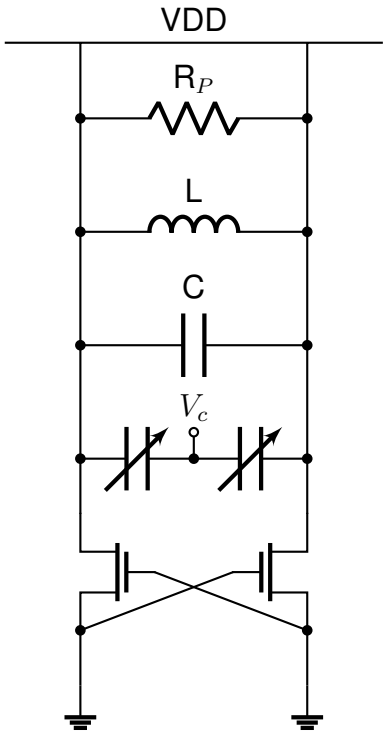

Figure 2.21: Cross-coupled pair VCO schematic.

Frequency divider

The frequency divider is a circuit that takes an input signal and produces an output signal with a frequency that is a fraction of the input frequency. The most common frequency divider is the flip-flop (fig. ??), which divides the input frequency by two, although there are other types of dividers that can divide by any integer number. The frequency divider is used in PLLs to reduce the frequency of the input signal to a level that can be processed by the other blocks of the PLL (to match the frequency of the reference signal). The frequency divider of figure ?? can also be used to increase the frequency of the output signal, in this case it is called a frequency multiplier.

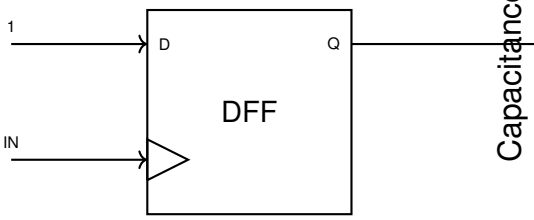

Figure 2.22: MOS varactor.

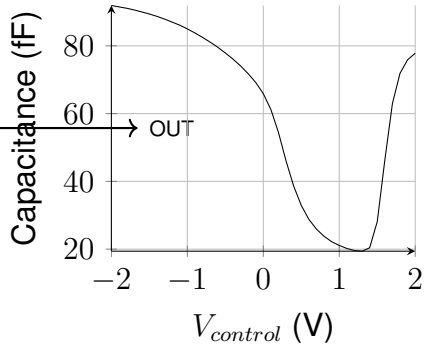

Figure 2.23: MOS varactor characteristic.

Although the flip-flop is the most common frequency divider, there are other types of dividers that can be used in PLLs. One of the most relevant is the CML frequency divider, which is a type of frequency divider that uses current-mode logic (CML) to achieve high speed operation. CML dividers are typically used in high-speed applications, such as high-speed data communication systems, where the output of the VCO is too high to be processed by any regualr flip-flop. The CML frequency divider is based on the principle of current steering, where the input signal is used to control the current flowing through a branch of the differential pair.

A CML signal resembles a sinusoidal wave and has a lower harmonic content than a regular square wave, yet its power consumption is higher

because of the constant current through the circuit due to the current source of the differential pair.

2.2 Digital phase-locked loop

anan

2.2.1 Time-to-digital converter

TDC as a phase detector

Delay-locked loop fundamentals

2.2.2 Digital loop filter

2.2.3 Digitally controlled oscillator

Chapter 3

Literature review

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Chapter 4

Methodology

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Chapter 5

Results

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Chapter 6

Discussion

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Chapter 7

Conclusion

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Appendix A

Appendix

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[1] Mark Van Paemel. "Analysis of a charge-pump PLL: A new model". In: *IEEE Transactions on communications* 42.7 (1994), pp. 2490–2498.