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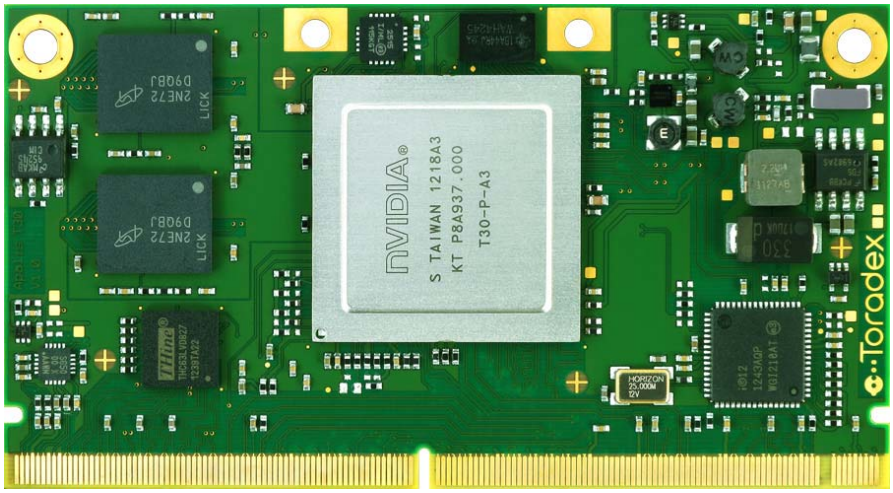
Apalis Computer Module

Carrier Board Design Guide



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8th April 2013	V1.0	Initial Release: Preliminary Version
27th August 2013	V1.1	Correction in section 5.3 on page 79
26th November 2013	V1.2	Correction in the figure 65 on page 49 Correction in the tables 16, 17, 18, 21: signals USBH_OC# and USBH_EN pin numbers Correction in the table 25: description of the pins 282-302

1 Introduction

1.1 Overview

This document is designed to guide users through the development of a customized carrier board for the Apalis Computer module. The Apalis Computer module features new high speed interfaces such as PCI Express, SATA, HDMI and LVDS which require special layout considerations regarding trace impedance and length matching. Please read this document very carefully when designing a carrier board.

This document also contains reference schematics for the different interfaces. It describes only the standardized primary functions on the Apalis modules. Type specific interfaces and secondary functions are not guaranteed to be compatible between different Apalis modules. These interfaces are described in the datasheet of each Apalis module. Some Apalis modules do not feature the full set of standard interfaces. Therefore, it is strongly recommended to read the datasheets of the Apalis modules that are required to be support by the carrier board.

1.2 Additional Documents

1.2.1 Apalis Module Datasheets

Datasheets which are specific to each Apalis module contain detailed information describing type specific interfaces and alternate pin functions. Before starting the development of a custom carrier board design, please check thee datasheets to ensure that the interfaces you wish to support are available for specific modules.

http://www.toradex.com

1.2.2 Apalis Module Definition

This document describes the Apalis Module standard. It provides additional information about the interfaces.

http://www.toradex.com

1.2.3 Toradex Developer Centre

You can find a lot of additional information in the Toradex Developer Centre, which is updated with the latest product support information on a regular basis.

Please note that the Developer Centre is common for all Toradex products. You should always check to ensure if information is valid or relevant for products in the Apalis family.

http://www.developer.toradex.com

1.2.4 Apalis Evaluation Board Schematics

We provide complete schematics including the Altium project file for the Apalis Evaluation Board at no charge and freely downloadable from the developer website. It is highly recommended that you make use of these design files as a starting point for any custom carrier board design.

http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.3 Abbreviations

Abbreviation	Explanation
ADC	Analogue to Digital Converter
AGND	Analogue Ground, separate ground for analogue signals
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX f is able to detect whether RX and TX need to be crossed (MDI or MDIX)
CAD	Computer-Aided Design, in this document is referred to PCB Layout tools
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CDMA	Code Division Multiplex Access, abbreviation often used for a mobile phone standard for data communication
CEC	Consumer Electronic Control, HDMI feature that allows to control CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analogue Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor, in this document DDC2B (based on I^2C) is always meant
DRC	Design Rule Check, a tool for checking whether all design rules are satisfied in a CAD tool
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrical compatible with HDMI
DVI-A	Digital Visual Interface Analogue only, signals are compatible with VGA
DVI-D	Digital Visual Interface Digital only, signals are electrical compatible with HDMI
DVI-I	Digital Visual Interface Integrated, combines digital and analogue video signals in one connector
EDA	Electronic Design Automation, software for schematic capture and PCB layout (CAD or ECAD)
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document also called LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
GSM	Global System for Mobile Communications
HDA	High Definition Audio (HD Audio), digital audio interface between CPU and audio codec
HDCP	High-Bandwidth Digital content Protection, copy protection system that is used by HDMI beside others
HDMI	High-Definition Multimedia Interface, combines audio and video signal for connecting monitors, TV sets or Projectors, electrical compatible with DVI-D
I^2C	Inter-Integrated Circuit, two wire interface for connecting low speed peripherals
I^2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
IrDA	Infrared Data Association, infrared interface for connecting peripherals
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signalling, electrical interface standard that can transport very high speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MDI	Medium Dependent Interface, physical interface between Ethernet PHY and cable connector
MDIX	Medium Dependent Interface Crossed, an MDI interface with crossed RX and TX interfaces
mini PCIe	PCI Express Mini Card, card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
mSATA	Mini-SATA, a standardized form factor for small solid state drive, similar dimensions as mini PCIe

Abbreviation	Explanation
MXM3	Mobile PCI Express Module (second generation), graphic card standard for mobile device, the Apalis form factor uses the physical connector but not the pin-out and the PCB dimensions of the MXM3 standard.
N/A	Not Available
N/C	Not Connected
OD	Open Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
OWR	One Wire (1-Wire), low speed interface which needs just one data wire plus ground
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analogue signals, standard interface for digital audio
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	Single ended serial port interface
RS422	Differential signalling serial port interface, full duplex
RS485	Differential signalling serial port interface, half duplex, multi drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
S/PDIF	Sony/Philips Digital Interconnect Format, optical or coaxial interface for audio signals
SATA	Serial ATA, high speed differential signaling interface for hard drives and SSD
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, identification card for GSM phones
SMBus	System Management Bus (SMB), two wire bus based on the I^2C specifications, used specially in x86 design for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
TIM	Thermal Interface Material, thermal conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signalling, serial high speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, diode that is used to protect interfaces against voltage spikes
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver a RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals
VCC	Positive supply voltage
VGA	Video Graphics Array, analogue video interface for monitors

Table 1: Abbreviations

2 Layout

The Apalis module features a range of high speed interfaces which need special treatment with regard to PCB layout. This section describes a collection of basic rules to follow. It should be noted that it is often not possible to follow all rules. It is the job of the design engineer, with the aid of this design guide, to decide which rule can be violated, in what area and for which signals when it is necessary to do so.

The interfaces have an importance priority over one another when it comes to ensuring optimal routing of designs. The below list describes the importance priority of the signals. PCIe is the first one in the list and has the highest priority, and should be routed with special care. Signals continue to be ordered with descending priority and as such become less problematic with respect to layout and routing. Often, a good approach to take is to layout and route interfaces in order of their importance priority, from high to low.

1. PCI Express
2. USB 3.0 (Super Speed signals)
3. SATA
4. Ethernet
5. HDMI
6. LVDS Display
7. USB 2.0
8. SD/MMC/SDIO
9. Parallel RGB LCD Interface
10. Parallel Camera Input
11. HD Audio
12. Analogue VGA
13. Analogue Audio, ADC Inputs, Touch Panel
14. Low Speed Interfaces (I2C, UART, SPI, CAN, PWM, OWR, S/PDIF, Keypad, GPIO)

2.1 PCB Stack-Up

In order to reduce reflections on high speed signals, it is necessary to match the impedance between source, sink and transmission line. The impedance of a signal trace depends on its geometry and it's position with respect to any reference planes. The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realised. The presented stack-ups in the following subsections are intended as examples which can be used as a starting point for helping in stackup evaluation and selection.. If a different stack-up is required other than those shown in the examples, please recalculate the dimensions of the traces. Work closely with your PCB manufacturer when selecting suitable stack-up solution.

2.1.1 Four Layer Stack–Up

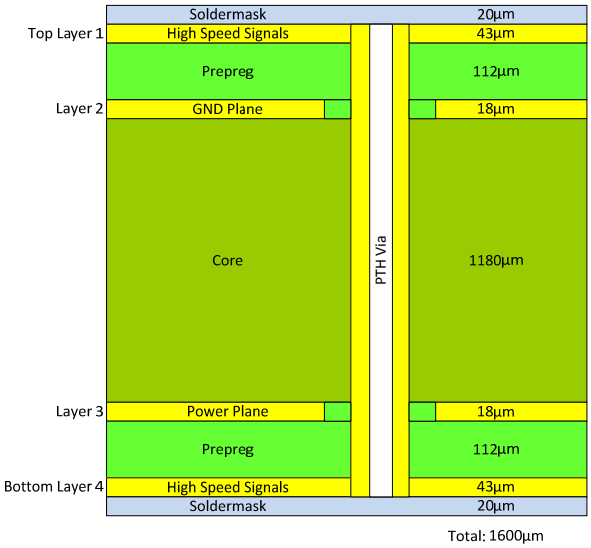


Figure 1: Four Layer PCB Stack-Up Example

The high speed signals on the top layer are referenced to the ground plane on layer 2. Since the references for the high speed signals on the bottom layer are the power planes on layer 3, it is necessary to place stitching capacitors between the aforementioned power planes and ground. More information about stitching capacitors can be found in section 2.3.8. In this stack up, it is preferential to route high speed signals on the top layer as opposed to the bottom layerso that the signals have a direct reference to the ground layer. For some designs it may be desirable to have the bottom layer as primary high speed routing layer. In this case, the power and ground usage on Layer 2 and 3 could be swapped.

2.1.2 Six Layer Stack–Up

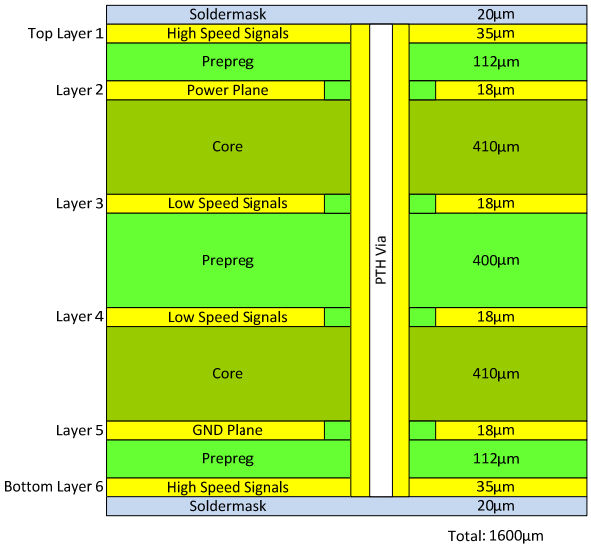


Figure 2: Six Layer PCB Stack-Up Example

In this example, the reference planes for the high speed signals on the top layer are the power planes on layer 2. Stitching capacitors from the associated reference power plane to ground are therefore required. More information about stitching capacitors can be found in section 2.3.8. The signal reference for the bottom layer is the ground plane on layer 5. In this stack-up, it is preferable to route high speed signals on the bottom layer. As in the previous example, power and ground layers could be swapped if it is desirable to have the primary high speed routing layer on the top layer.

The reference planes for signals on layer 3 are located on layer 2 and 5. The same reference planes are used by signals routed on layer 4. As the reference planes are on layers which have a relatively large distance from signal layers 3 and 4, the traces would need to be very wide in order to achieve a common impedance of 50Ω. Therefore, these layers are not suitable for routing high speed signals. In this stack-up approach, layers 3 and 4 can only be used for routing low speed signals where impedance matching is not required.

2.1.3 Eight Layer Stack–Up

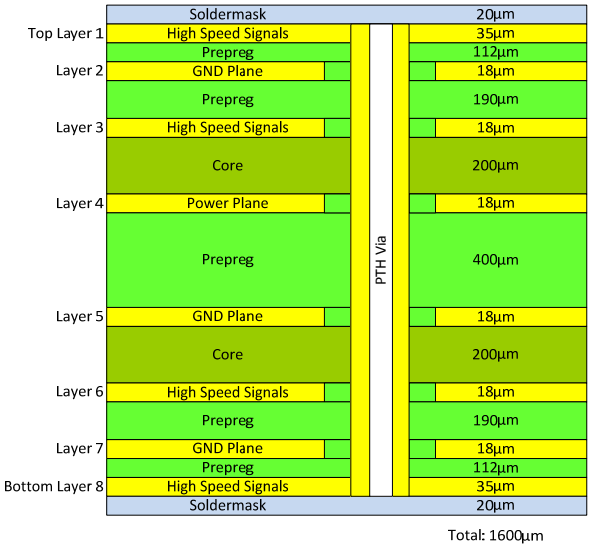


Figure 3: Eight Layer PCB Stack-Up Example

The signals on the top layer are referenced to the plane in layer 2, while the signals on the bottom layer are referenced to layer 7. The reference planes for signal layer 3 are the ground plane on layer 2 and the power planes on layer 4. When routing high speed signals on layer 3, stitching capacitors need to be placed between the power and the ground planes. The power planes on layer 5 and 7 are used as references for the high speed signals routed on layer 6.

The inner layer 6 with the two adjacent ground planes is the best choice for routing high speed signals which have the most critical impedance control requirements. The inner layers cause less EMC problems as they are capsulated by the adjacent ground planes. As layer 3 is referenced to a power plane, outer layer 1 and 8 are preferable for high speed routing if layer 6 is already occupied.

2.2 Trace Impedance

Care should be taken to distinguish between single ended and differential trace impedance. High speed single ended signals such as the parallel RGB LCD or camera interface need to be routed with the specified single ended impedance. This is the impedance between the trace and the reference ground.

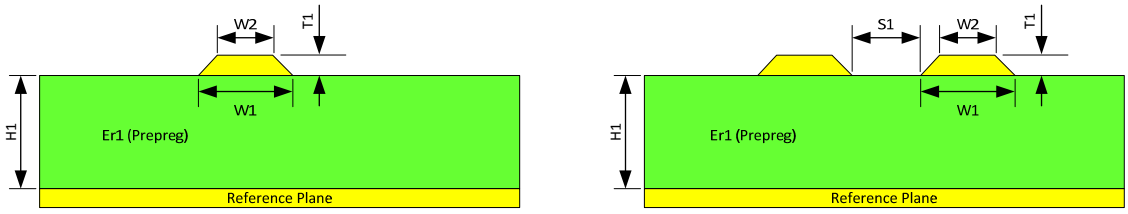
High speed differential pair signals such as PCIe, SATA, USB, HDMI etc. need to be routed with differential impedance. This is the impedance between the two signal traces of a pair. As the signals are also referenced to ground, each differential pair signal also has a single ended impedance. When selecting trace geometry, priority should be given to matching the differential impedance over the single ended impedance. The differential impedance is always smaller than twice the single ended impedance

$$Z_{Differntial} < 2 \cdot Z_{Single\ Ended}$$

The signals allow a certain impedance tolerance (e.g. 50Ω ±15%). When defining trace geometry, try to keep the calculated impedance value as close as possible to the exact impedance value. This allows greater flexibility during PCB manufacture. Variation in impedances will occur between different production lots. If the calculated impedance is in the middle of the tolerance band, this will help ensure maximum production yield.

Different tools can be used for calculating the trace impedance. Polar Instruments offers a widely used tool. Many PCB manufacturers use this tool. PCB manufacturers can often help customers with impedance calculations, and it is suggested you work with your chosen PCB manufacturer during your design. Many PCB layout tools offer a very basic impedance calculator. Unfortunately, these calculators are not reliable in all situations.

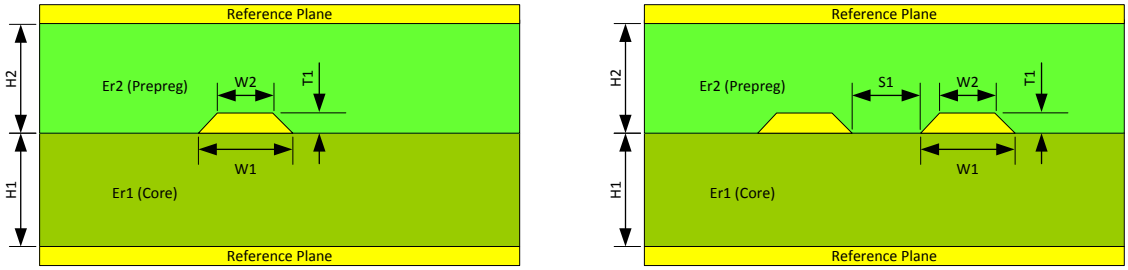
Traces on the top or bottom layer have only one reference plane. These traces are called microstrip. The following figure shows the geometry of such microstrips. H1 is the distance from the trace to the according reference plane. Er1 is the relative permittivity of the isolation material. The traces have a trapezoid form due to the etching process. In the layout tool, the traces have to be designed with a width of W1. W2 depends on the trace height (T1) and the duration of the etching. Contact your PCB manufacturer in order to get the information about the resulting width W2. S1 is the spacing within a differential pair.



Single Ended Impedance of Microstrip | Differential Impedance of Microstrip

Figure 4: Trace Geometry of Microstrips

Traces in the inner layer of a PCB have two reference planes, reducing electromagnetic emissions and increasing immunity to external noise sources. These traces are called stripline. The following figure shows the geometry of such striplines. When making impedance calculation of striplines, special care needs to be taken when it comes to the isolation thickness H1 and H2. H1 is the thickness of the core material. The traces are embedded in the prepreg material. As the traces have a finite height, the prepreg height H2 depends on the copper density. The relative permittivity of the core and prepreg material can be slightly different. Many impedance calculation tools can take this in account.



Single Ended Impedance of Stripline | Differential Impedance of Stripline

Figure 5: Trace Geometry of Striplines

The following table shows typical trace geometries for traces using in the four layer stack-up, presented in section 2.1.

Signal Type	Required $Z_{Single\ Ended}$	Required $Z_{Differential}$	Layer	Trace Type	W1	S1
Common Single Ended	50Ω	N/A	1, 4	Microstrip	180µm	N/A
PCIe, USB, HDMI,	50Ω	90Ω	1, 4	Microstrip	180µm	190µm
SATA	55Ω	90Ω	1, 4	Microstrip	150µm	150µm

Signal Type	Required $Z_{Single\ Ended}$	Required $Z_{Differential}$	Layer	Trace Type	W1	S1
Ethernet	55Ω	95Ω	1, 4	Microstrip	150µm	165µm
LVDS	55Ω	100Ω	1, 4	Microstrip	150µm	200µm

Table 2: Four Layer Stack-Up Example

The following table shows typical trace geometries for traces using in the six layer stack-up, presented in section 2.1.

Signal Type	Required $Z_{Single\ Ended}$	Required $Z_{Differential}$	Layer	Trace Type	W1	S1
Common Single Ended	50Ω	N/A	1, 6	Microstrip	180µm	N/A
PCIe, USB, HDMI,	50Ω	90Ω	1, 6	Microstrip	180µm	200µm
SATA	55Ω	90Ω	1, 6	Microstrip	150µm	130µm
Ethernet	55Ω	95Ω	1, 6	Microstrip	150µm	165µm
LVDS	55Ω	100Ω	1, 6	Microstrip	150µm	200µm

Table 3: Six Layer Stack-Up Example

The following table shows typical trace geometries for traces used in the eight layer stack-up, presented in section 2.1.

Signal Type	Required $Z_{Single\ Ended}$	Required $Z_{Differential}$	Layer	Trace Type	W1	S1
Common Single Ended	50Ω	N/A	1, 8	Microstrip	180µm	N/A
			3, 6	Stripline	170µm	N/A
PCIe, USB, HDMI,	50Ω	90Ω	1, 8	Microstrip	180µm	200µm
			3, 6	Stripline	170µm	185µm
SATA	55Ω	90Ω	1, 8	Microstrip	150µm	130µm
			3, 6	Stripline	140µm	120µm
Ethernet	55Ω	95Ω	1, 8	Microstrip	150µm	165µm
			3, 6	Stripline	140µm	155µm
LVDS	55Ω	100Ω	1, 8	Microstrip	150µm	200µm
			3, 6	Stripline	140µm	200µm

Table 4: Eight Layer Stack-Up Example

2.3 High Speed Layout Considerations

2.3.1 Power Supply Bypass Capacitors

Digital circuits often draw a non-continuous current from their supply power. Peak current consumption can be relatively large with high frequency components. If the supply traces are long, such current peaks can cause high frequency noise emission, which can be introduced into other signals. As traces have parasitic resistance and inductance, this high frequency noise can be coupled into supplies for other circuits (see left figure below). Another problem is that the parasitic inductance of the supply trace reduces the ability for the trace to carry the current peaks, which can cause voltage drops at the consuming circuit. It is therefore necessary to add bypass capacitors to the power input pins of digital circuits, which act to provide a reservoir of energy that can be drawn on to help supply the short term peak currents that may be required.

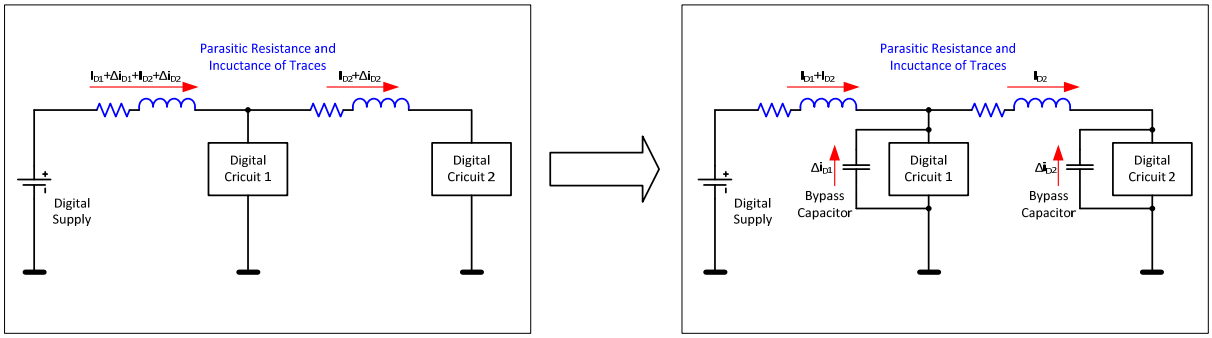


Figure 6: Add bypass capacitors

When possible, individual bypass capacitors should be place on every power supply pin of an integrated circuit. If supply pins are close together, a bypass capacitor may be shared between both pins. Capacitors should be placed as close as possible to supply pins. Try to enlarge the supply trace widths and keep them short. Current flow direction should also be considered. It is preferable that the current first passes the bypass capacitor and then enters the supply pin. Add an adequate amount of vias to the power supply traces. As a rule of thumb, place one via for one ampere of current consumption. If the decoupling capacitors are placed on the other side of the PCB and the current needs to go through vias, also consider the peak current. Also, do not forget about the ground return current. The ground should have the same amount of vias as the supply as a minimum.

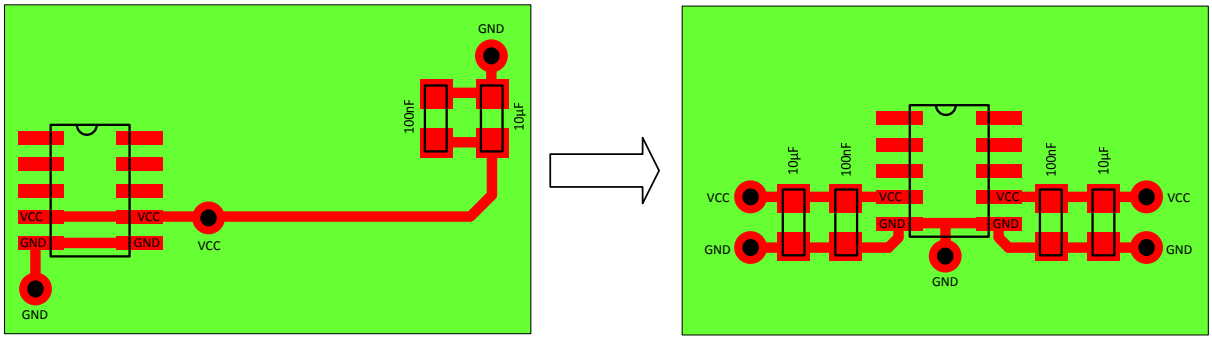


Figure 7: Place Bypass Capacitors close to IC pins

Large capacitors have a limitation in the speed they can provide energy to counter the current peaks, while small capacitors may not have enough capacity to satisfy the energy demand. Therefore, often a combination of small and big (e.g. 100nF + 10 µF) capacitors is a good choice for such supply circuits. Ensure the smaller capacitor is placed closer to the supply pin than the bigger one.

2.3.2 Trace Bend Geometry

When routing high speed signals, bends should be minimized. If bends are needed, use 135° bends instead of 90°.

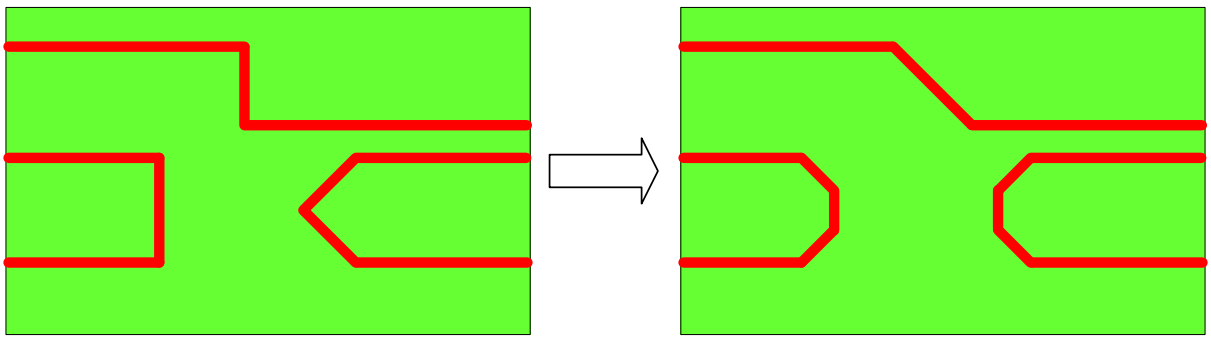


Figure 8: Use 135° Bends instead of 90°

Serpentine traces (also called meander) are often needed when a certain trace length needs to be achieved. Keep a minimum distance between adjacent copper in a single trace of four times the trace width. The individual segments of the bends should be at least 1.5 times the trace width. A lot of DRCs in CAD tools do not check these minimum distances as the traces are part of the same net.

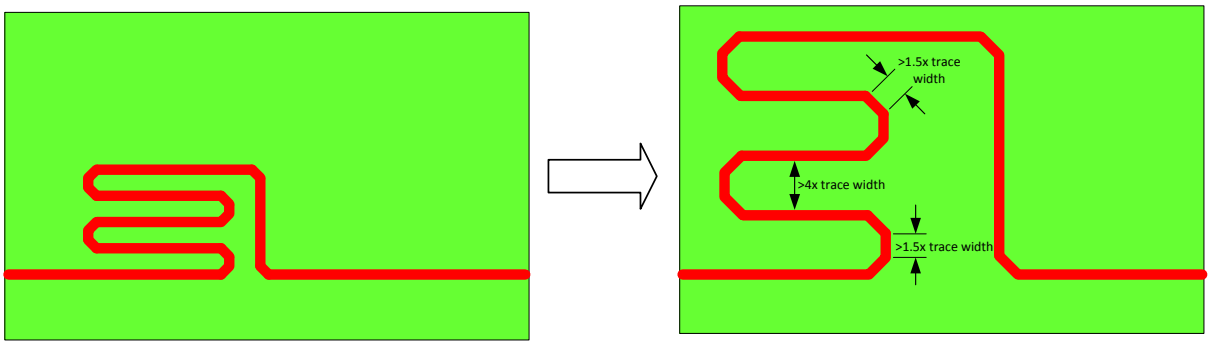


Figure 9: Keep minimum Distance and Segment Length at Bends

2.3.3 Signal Proximity

Information about the required minimum distance between high speed signals can be found in section 3. A minimum distance is required in order to minimise cross talk between traces. The level of cross talk depends on the distance between two traces and the length in which they are routed closely. Sometimes, bottlenecks can force the routing of traces closer than is normally permitted. Try to minimise such areas and enlarge the distance between the signals outside of the bottleneck. If there is space available, try to enlarge the distance between the high speed signals (and between high speed and low speed signals) even if the minimum trace separation requirement has been met.

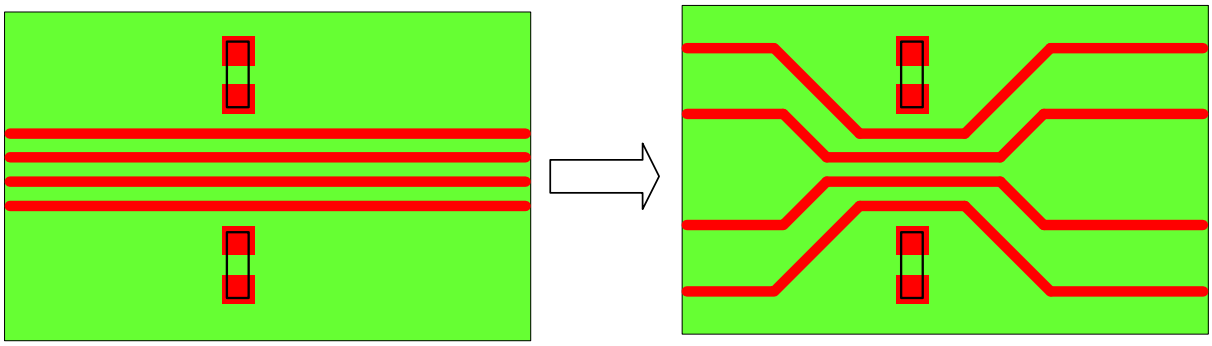


Figure 10: Try to increase spacing between traces whenever it is possible

2.3.4 Trace Stubs

Long stub traces can act as antennas and therefore increase problems complying with EMC standards. Stub traces can also produce reflections which negatively impacts signal integrity. Common sources for stubs are pull-up or down resistors on high speed signals. If such resistors are required, route the signals as a daisy chain.

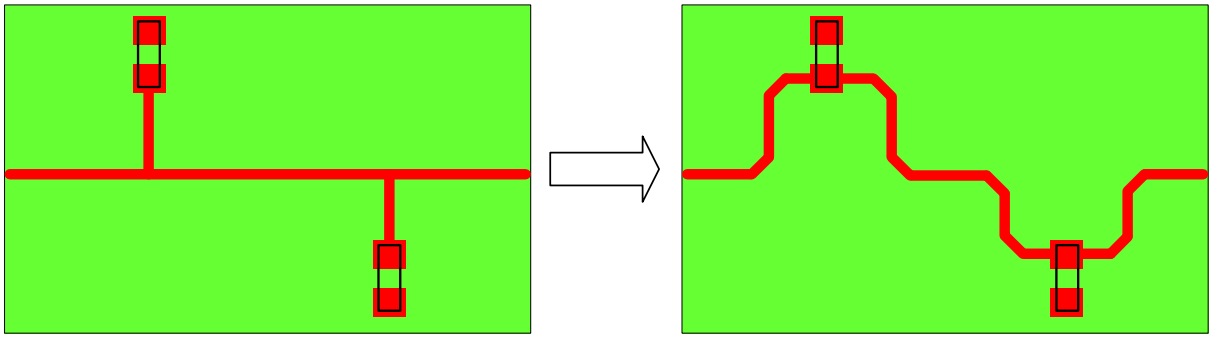


Figure 11: Avoid Stub Traces by Daisy Chain Routing

As a rule of thumb, stubs longer than a tenth of the wavelength should be considered as problematic. The following example shows the calculations on a Gen3 PCIe signal:

$$l_{MAX} \ll \frac{1}{10}\lambda_{MIN} = \frac{v}{10 \cdot f_{MAX}} = \frac{\frac{c}{\sqrt{\varepsilon_r}}}{10 \cdot f_{MAX}} = \frac{\frac{300 \cdot 10^6\, m/s}{\sqrt{4.5}}}{10 \cdot 4GHz} = 3.5mm$$

Vias can also act as stubs. For example, in a six layer board, when a signal changes from layer 1 to 3 by using a via, the via creates a stub which reaches layer 6. Back-drilling the vias in order to avoid such stubs is a quite expensive technology and one which is not supported by most PCB manufacturers. The only practical solution is to reduce the number of vias in high speed traces.

2.3.5 Ground Planes under Pads

The impedance of a trace depends on its width and the distance between trace and reference plane. A wide trace has lower impedance than a thin one with the same distance. The same effect also exists for connector and component pads. A large pad has significantly lower impedance than the trace which is connected to the pad. This impedance discontinuity can cause reflections reduces signal integrity. Therefore, under large connector and component pads, a plane obstruct should be placed. In this case, an active reference plane on another layer should be placed. This reference plane needs to be stitched with vias to the normal reference plane.

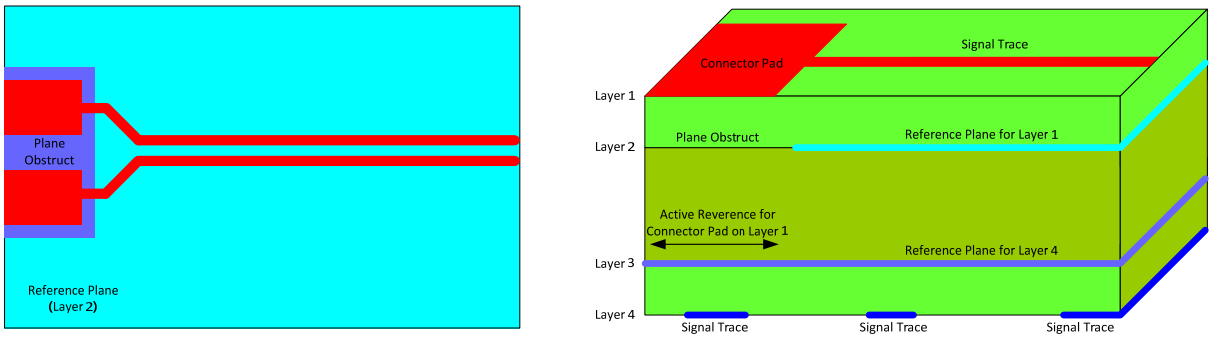


Figure 12: Remove Ground Plane under large Pads

Vias are another source of impedance discontinuity. In order to minimise the effect, the not used pads of vias in inner layers should be removed. This can be done at design time in the CAD tool or by the PCB manufacturer.

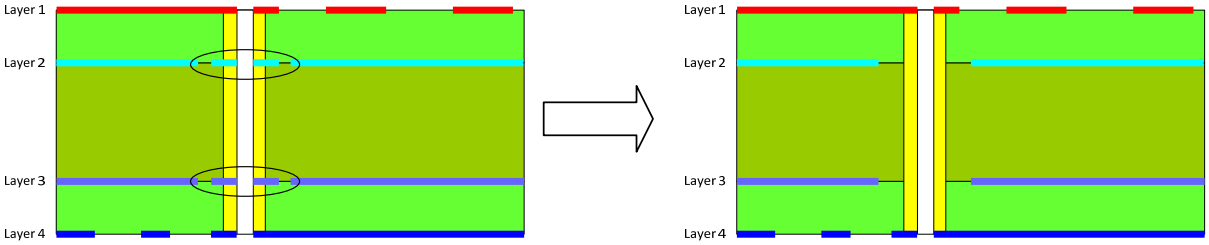


Figure 13: Remove unused Via Pads

2.3.6 Differential Pair Signals

High speed differential pair signals need to be routed in parallel with a specific, constant distance between the two traces. This distance is required in order to obtain the specified differential impedance (see section 2.2). Differential pair signals need to be routed symmetrically. Try to minimize the area in which the specified spacing is enlarged due to pad entries.

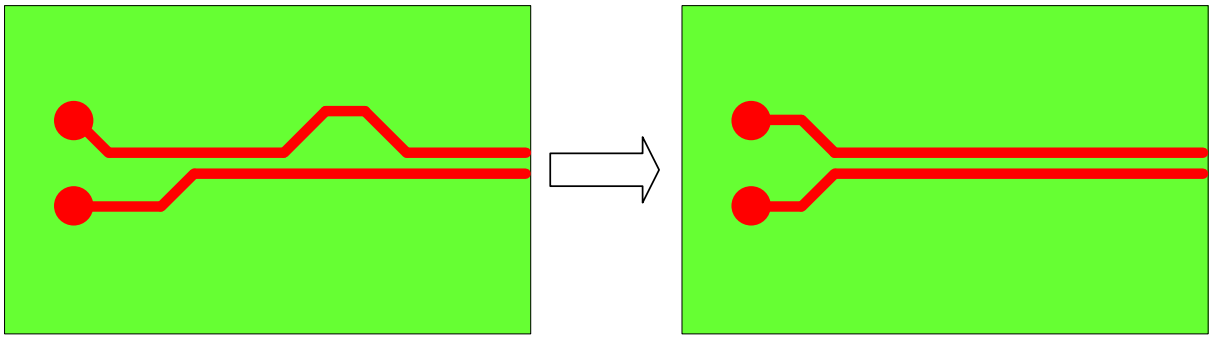


Figure 14: Route Differential Pairs symmetrically and keep Signals always parallel

It is not permitted to place any components or vias between the differential pairs, even if the signals are routed symmetrically. Components and vias between the pairs could lead to EMC compliance problems and create an impedance discontinuity.

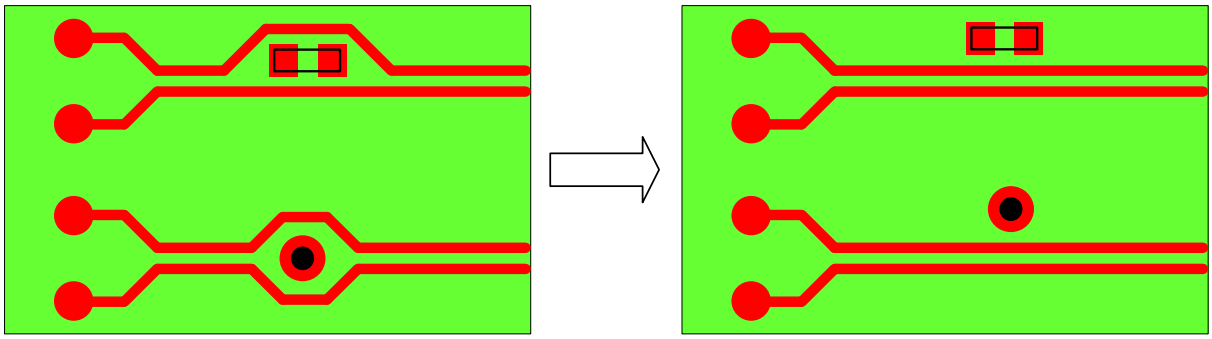


Figure 15: Do not put any Components or Vias between Differential Pairs

Some differential pair high speed signals require serial coupling capacitors. Place such capacitors symmetrically. The capacitors and the pads create impedance discontinuities. 0402 sized capacitors are preferable, 0603 are acceptable. Do not place larger packages such as 0805 or C-packs.

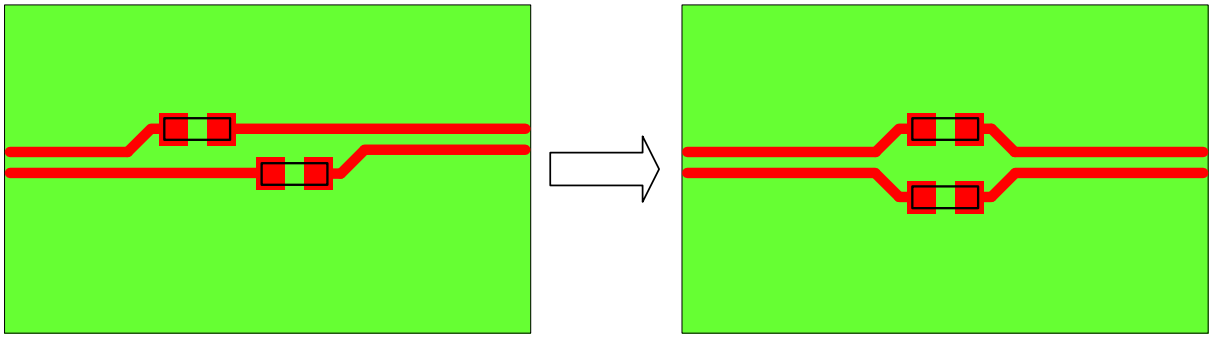


Figure 16: Place Coupling Capacitors symmetrical

Vias introduce a huge discontinuity in impedance. Try to reduce the amount of placed vias to a minimum and place the vias symmetrically.

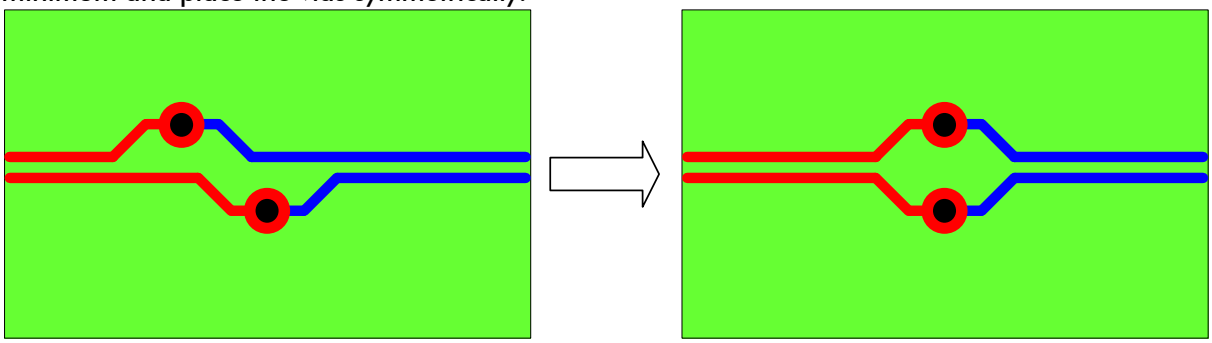


Figure 17: Place Vias symmetrical

In order to meet the impedance requirements of a differential pair, both signal traces need to be routed on the same layer. Add the same amount of vias to the traces.

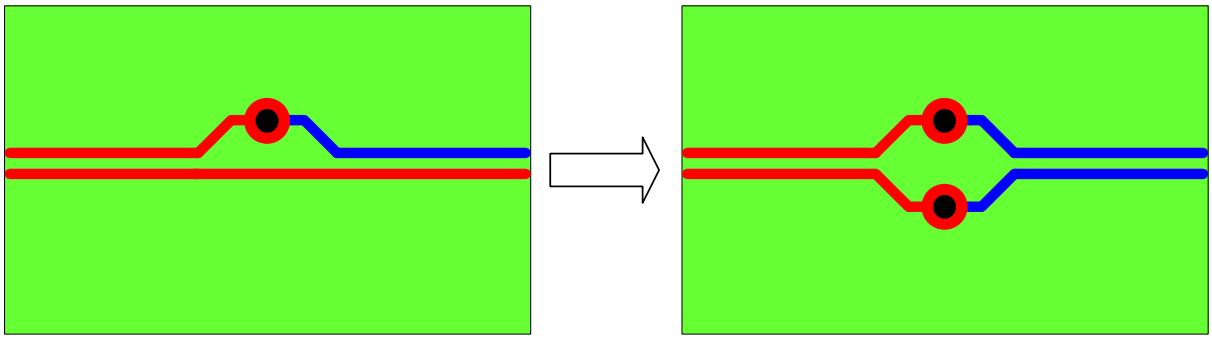


Figure 18: Route Pairs on the same Layer, place same amount of Vias

2.3.7 Length Matching

High speed interfaces have additional requirements regarding the time of arrival skew between different traces and pairs of signals. For example, in a high speed parallel bus, all data signals need to be arrive within a time period in order to meet the setup and hold time requirements of the receiver. The carrier board designer needs to make sure that such permitted skew is not exceeded. In order to meet this requirement, length matching is required. In section 3, more information about the length matching requirements for each interface type can be found. Often, the requirements are given as a maximum time skew. In order to calculate the maximum trace length difference, the propagation speed on the PCB needs to be estimated. The following formula can be used for calculating the speed:

$$v = \frac{c}{\sqrt{\varepsilon_r}}$$

The symbol c stands for the speed of light while ε_r is the relative permittivity of material between the trace and the reference plane. The relative permittivity of an FR-4 PCB is around 4.5 while air has 1. Some of the coupling between Microstrip signals on the outer layer of a PCB and the reference plane is over the air and the solder mask. Since the relative permittivity of both materials is lower than the one of the FR-4, the signals are propagated slightly faster than in the inner layers (Striplines). As a rule of thumb, the signals on a PCB are propagated with half speed of light. This equals to a speed of around 150 μm/ps.

$$v \approx 150 \frac{\mu m}{ps}$$

Differential pair signals often require a very tight delay skew between the positive and negative signal traces. Therefore, length differences need to be compensated for using serpentines (also called meanders). The geometry of serpentine traces need to be carefully chosen in order to reduce impedance discontinuity. The following figure shows the requirements for ideal serpentine traces:

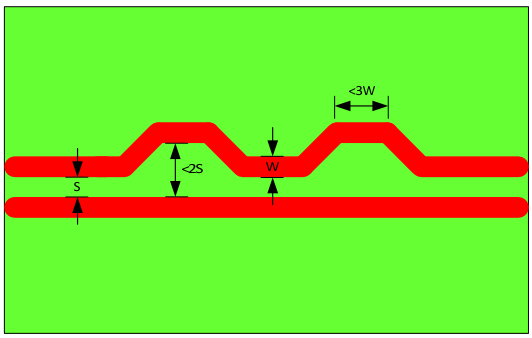


Figure 19: Preferred serpentine trace geometry

The serpentine traces should be placed at the origin of the length mismatching. This makes sure that the positive and negative signal component are propagated synchronously over the major part of the connection.

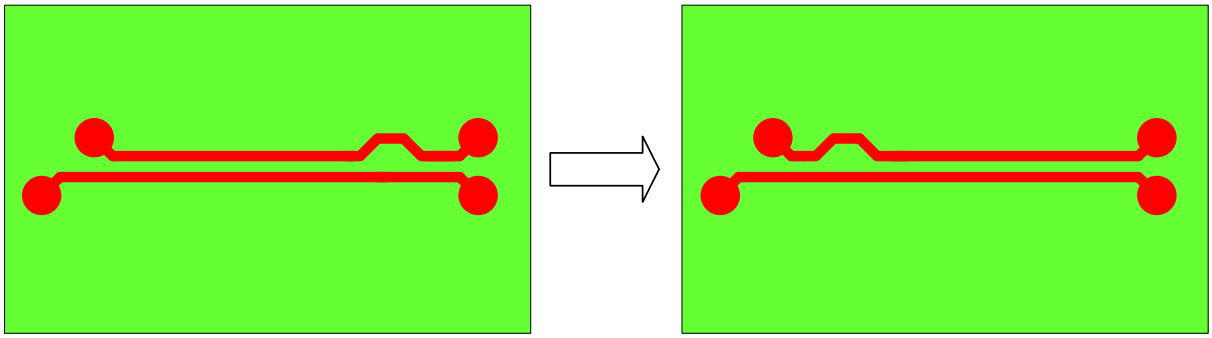


Figure 20: Add length correction to the mismatching point

Bends are a common source of length mismatching. The compensation should be placed close to the bend with a maximum distance of 15mm.

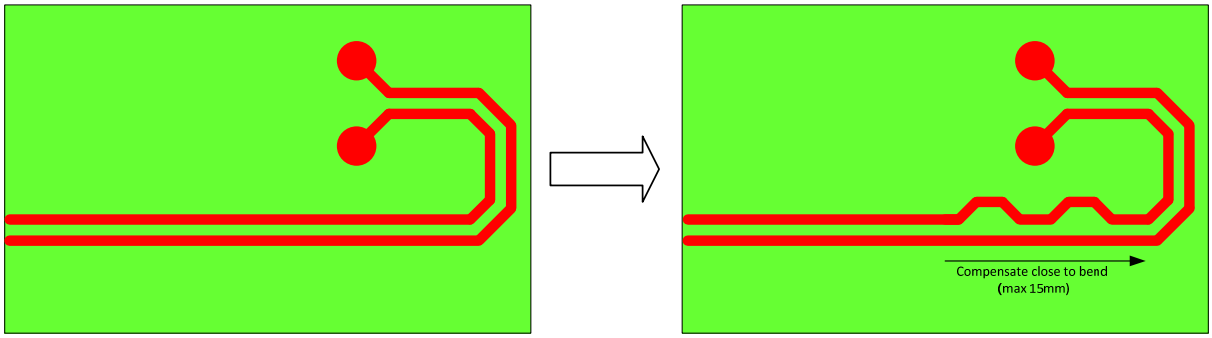


Figure 21: Place Length Compensation close to Bend

Often two bends compensate each other. If the bends are closer than 15mm, no additional compensation with serpentines is necessary. The signals should not propagate asynchronously over a distance greater than 15mm.

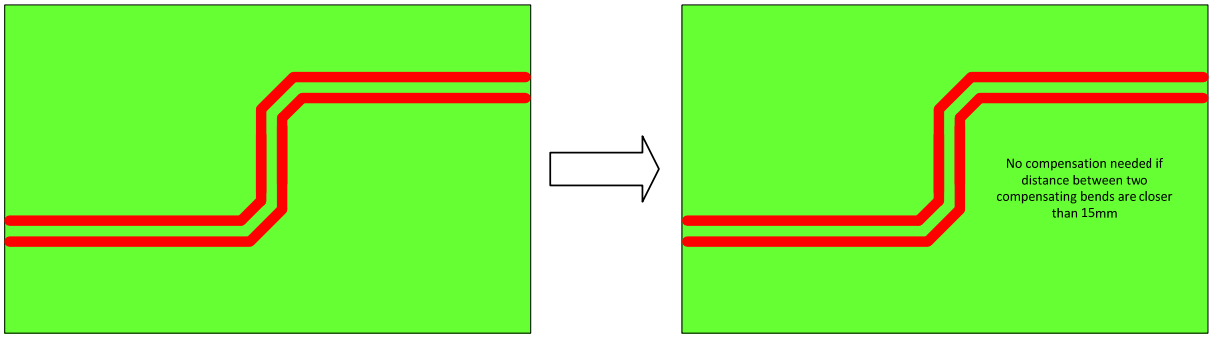


Figure 22: Bends can compensate each other

Each segment of a differential pair connection needs to be matched individually. A connection can be segmented by a connector, serial coupling capacitors or vias. The two bends in the following figure would compensate each other. Since the vias divide the differential pair into two segments, the bends need to be compensated individually. This makes sure that the positive and negative signal are propagated synchronous through the vias. The violation of this rule might need to be checked manually as the DRC may only check the length difference over the whole connection.

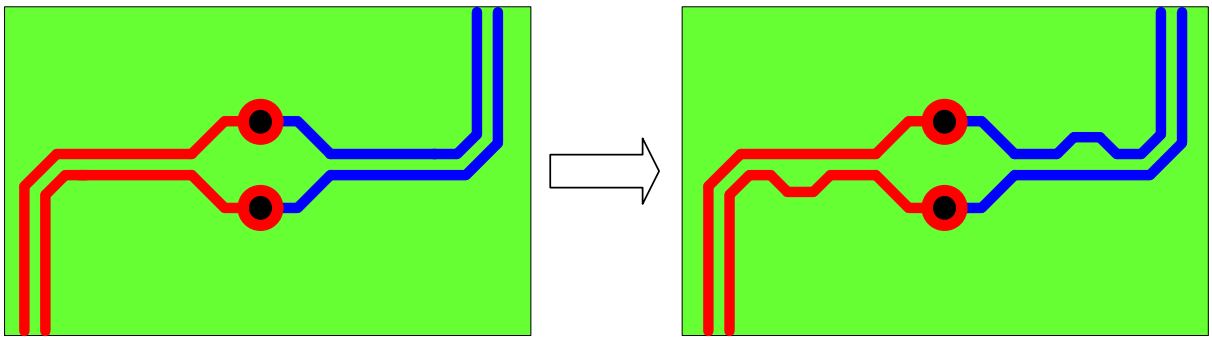


Figure 23: Length differences need to be compensated in each segment

The signal speed is not equal on different layers. Since the difference is hard to estimate, it is preferable to route signals on the same layer if they need to be matched. For example, the LVDS display interface requires tight matching between the signal pairs and the clock pair. It is preferable to route all data and clock signals of an LVDS channel on the same layer.

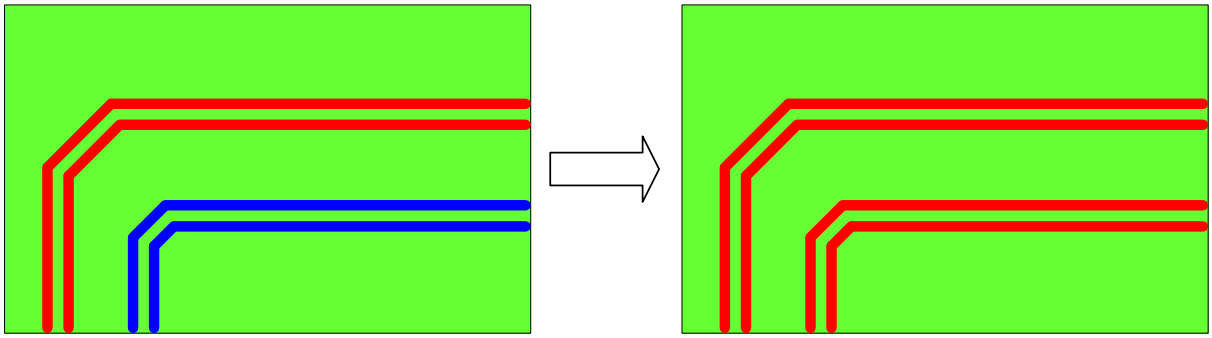


Figure 24: Pairs within same interface should be routed on same layer when possible

Please be aware that some CAD tools also count the trace length inside of a pad to the total length. The following figure shows two layouts which are similar from the electrical point of view. On the left side, the traces inside of the capacitor pads do not have equal length. Even though the signals are not using the internal traces, some CAD tools use this as part of the length calculation and show a length difference between the positive and negative signal. In order to minimise the impact incorrect trace length calculations, ensure that the pad entry is equal for both signals. Similarly, some CAD tools do not take in account the length of vias when calculating the total length. As differential pairs should have the same amount of vias in both traces, the error does not affect the length matching. It can, however, affect calculations for matching two differential pairs or the matching of parallel buses.

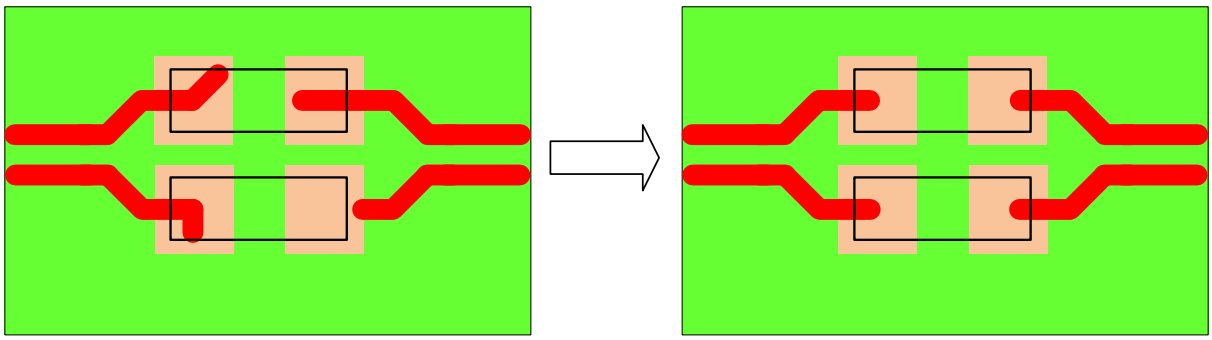


Figure 25: Length calculation problem with some CAD Tools

Whenever it is possible, a symmetric breakout of differential pair signal is preferred in order to avoid the need of serpentine traces.

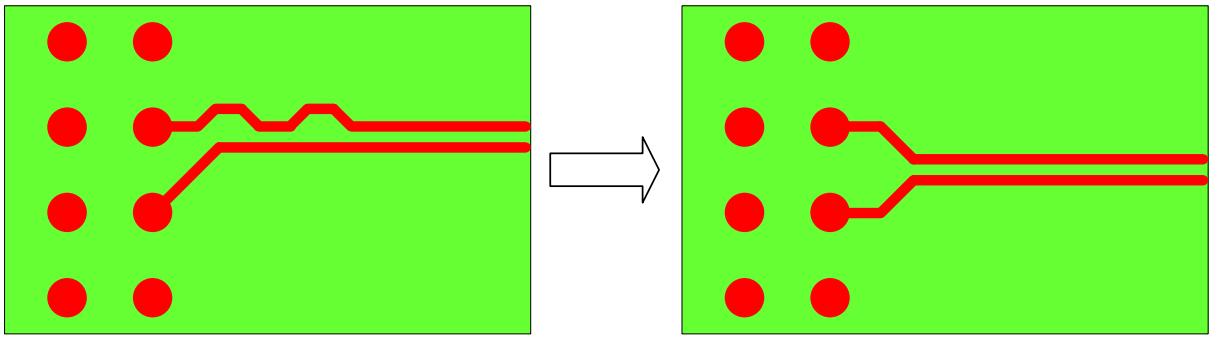


Figure 26: Preferred symmetrical breakout

If the space between the pads permits, try to add a small loop to the shorter trace. This is the preferred solution for matching the length difference as opposed to creating a serpentine trace.

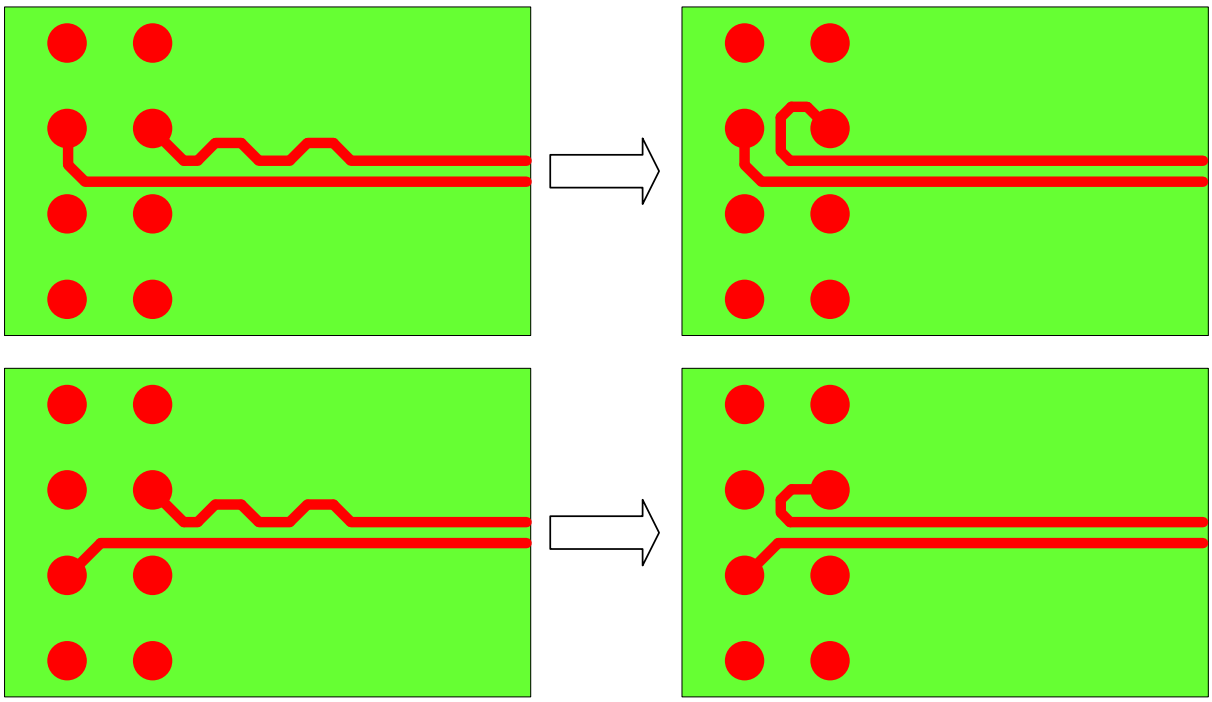


Figure 27: Preferred Breakout of Differential Pairs

2.3.8 Signal Return Path

An incorrect signal return path is one of the most common sources for noise coupling and EMI problems. When routing a signal, the return path of the signal current should always be considered. Power rails and low speed signals take the shortest (lowest resistance) path for the return current. In contrast, the return current of high speed signals tries to follow the signal path. Differential pair signals feature a positive and negative signal trace. Even these signals require a return path which needs to be considered when routing such signals.

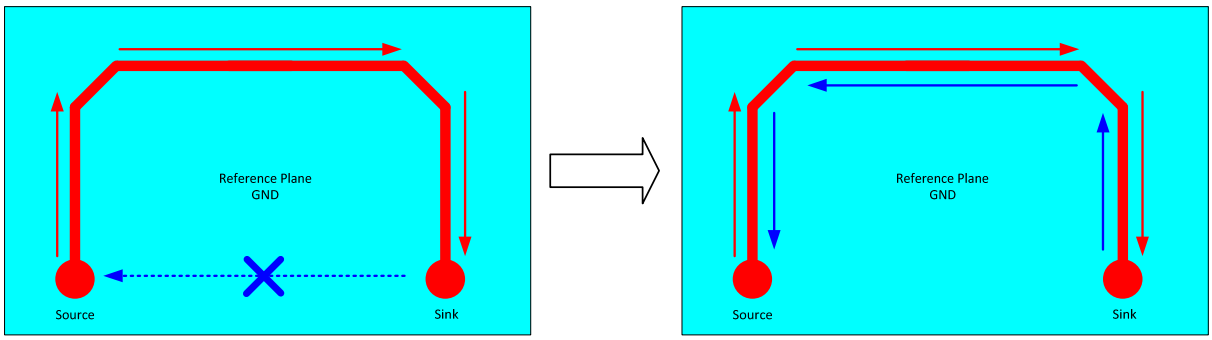


Figure 28: Return Current tries to follow the Signal Path

A signal should not be routed over a spit plane as the return path is not able to follow the signal trace. If a plane is split between a sink and source, route the signal trace around it. If the forward and return paths of a signal are separated, the area between them acts as a loop antenna.

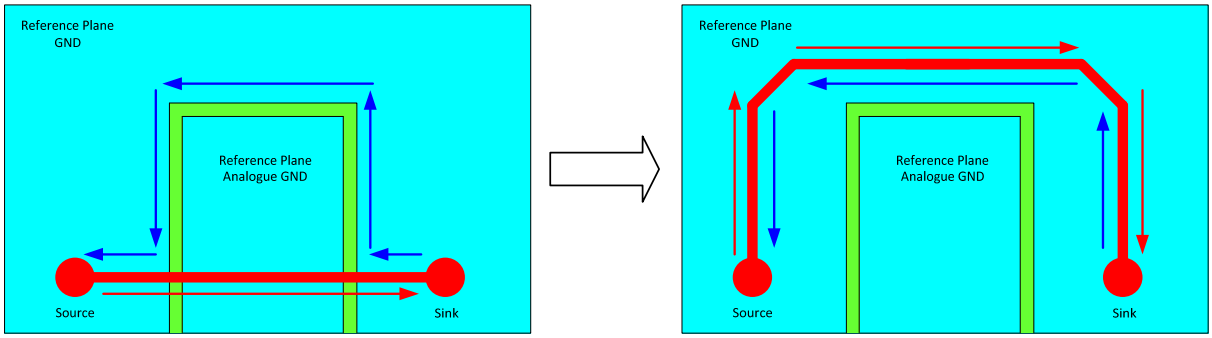


Figure 29: Avoid Routing over Split Planes

If a signal needs to be routed over two different reference planes, a stitching capacitor between the two reference planes is needed. The capacitor allows the return current to travel from one reference plane to the other. The capacitor should be placed close to the signal path in order to keep the distance between forward and return path small. A good value for the stitching capacitor is between 10nF and 100nF.

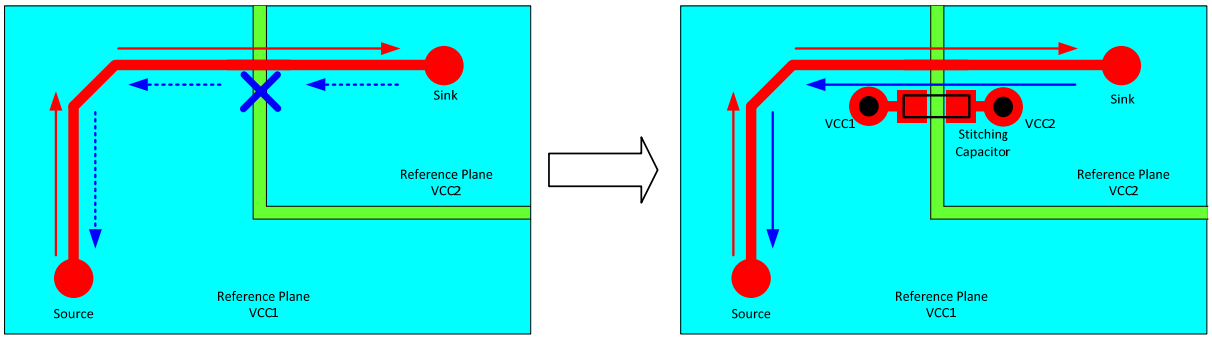


Figure 30: Stitching Capacitor needed when routed over Split Planes

Plane obstructions and plane slots should be avoided in general. Try to avoid routing signals over such obstructions. If it is not avoidable, stitching capacitors should be used to minimise the problems created by a separated return path.

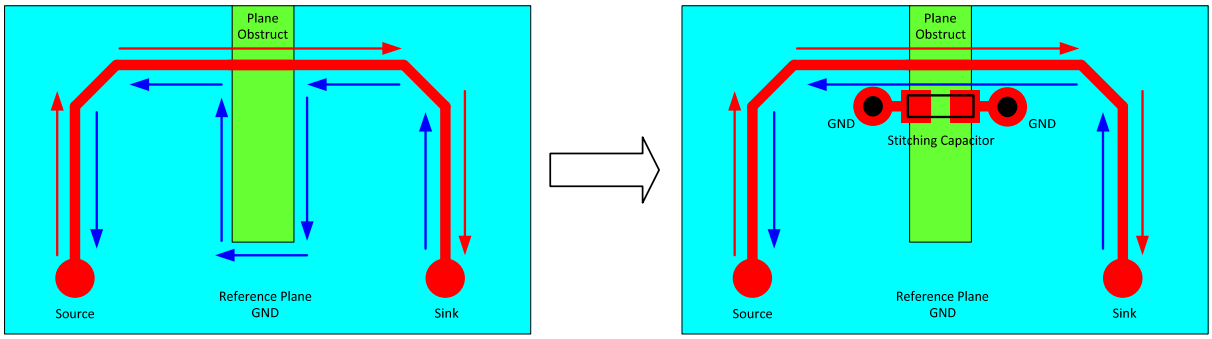


Figure 31: Stitching Capacitor needed when routing over Plane Obstructs

When placing vias close together, voids in reference planes can result. Be aware of such voids when routing high speed signals. Try to avoid large void areas by ensuring adequate separation between vias. Sometimes it is better to place fewer ground and power vias in order to reduce via voids.

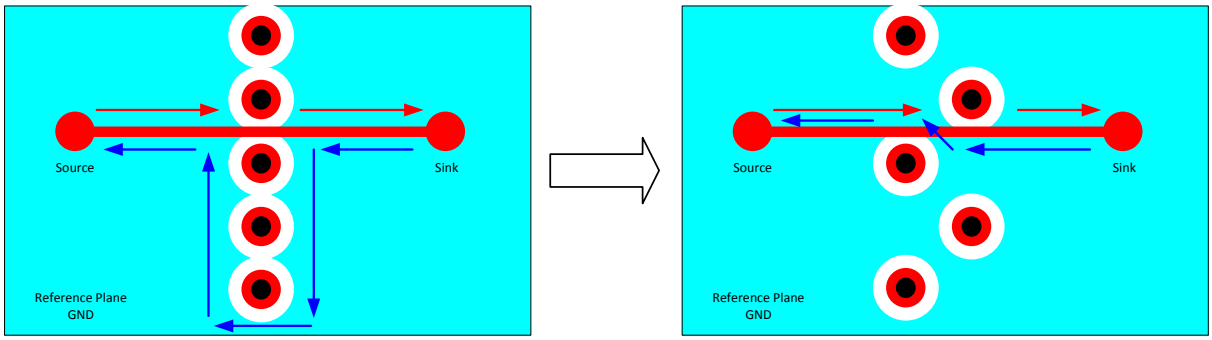


Figure 32: Avoid via plane voids

The return path needs to be considered at the source and sink of a signal. The left figure below shows a bad example. As there is only a single ground via on the source side, the return current cannot travel back on the reference ground plane as intended. The return path for the current is instead the ground connection on the top layer. The problem is that the impedance of the signal trace is calculated as referenced to the ground plane and not to the ground trace on the top layer. Therefore, it is necessary to place ground vias at the source and sink side of the signal. This permits the return current to travel back on the ground plane.

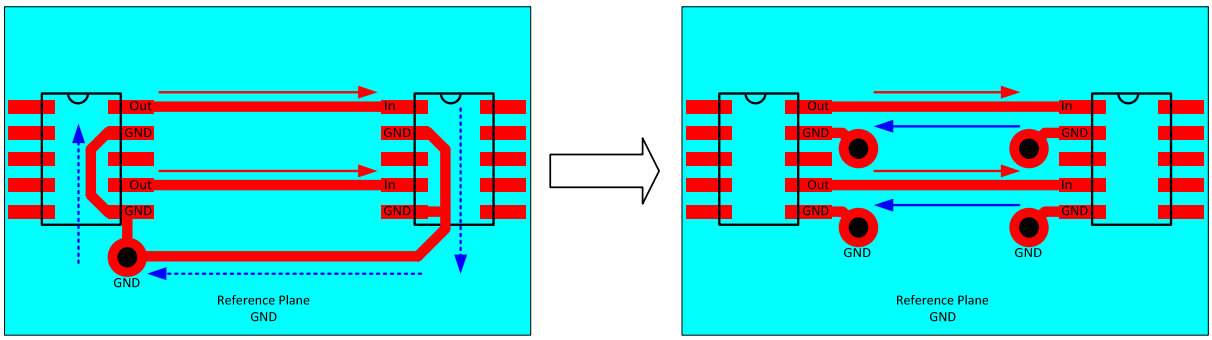


Figure 33: Consider return path when placing ground vias

When a signal trace uses a power plane as reference, the signal needs to be able to travel back over the power plane. In the source and sink, the signals are referenced to ground. In order to change the reference to the power plane, stitching capacitors at the sink and source are needed. If the sink and source are using the same power rail for their supply, the bypass capacitors can act as stitching capacitors if they are placed close to the signal entry/exit point. A good value for the stitching capacitor is between 10nF and 100nF.

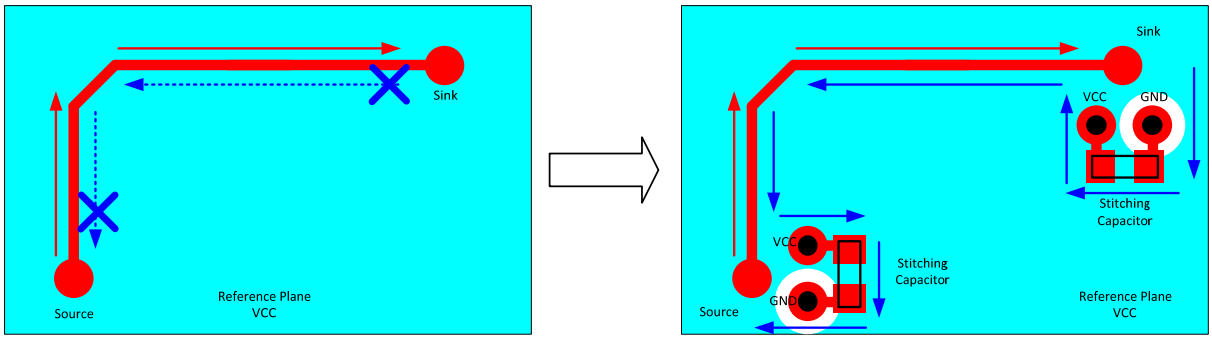


Figure 34: Add stitching capacitors when using a power plane as reference

If a signal trace changes layer and therefore also the reference ground plane, stitching vias should to be added close to the layer change vias. This allows the return current to change ground plane. For differential signals, switching ground vias should be placed symmetrically.

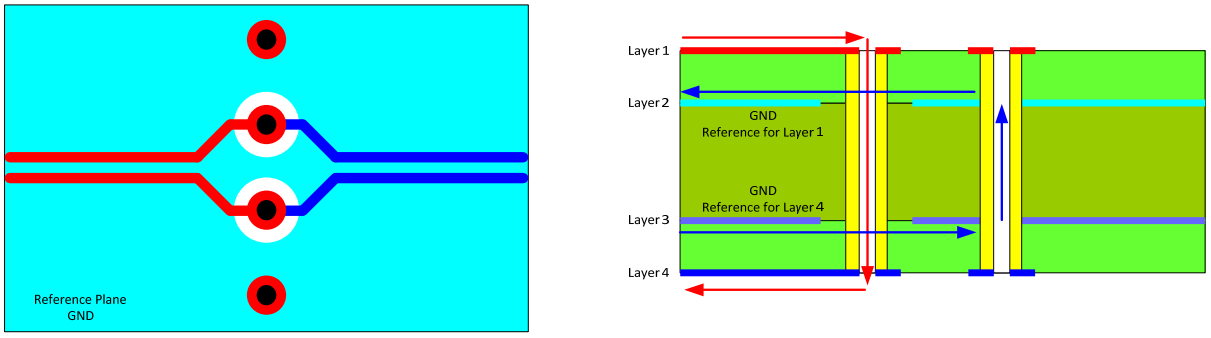


Figure 35: Place stitching vias when signal changes ground reference

If a signal trace changes to a layer which has a different net as reference (e.g. from ground reference to power plane reference), stitching capacitors are required. This allows the return current to flow from the ground plane through the stitching capacitor to the power plane. Stitching capacitor placement and routing should be symmetrical for differential pair signals.

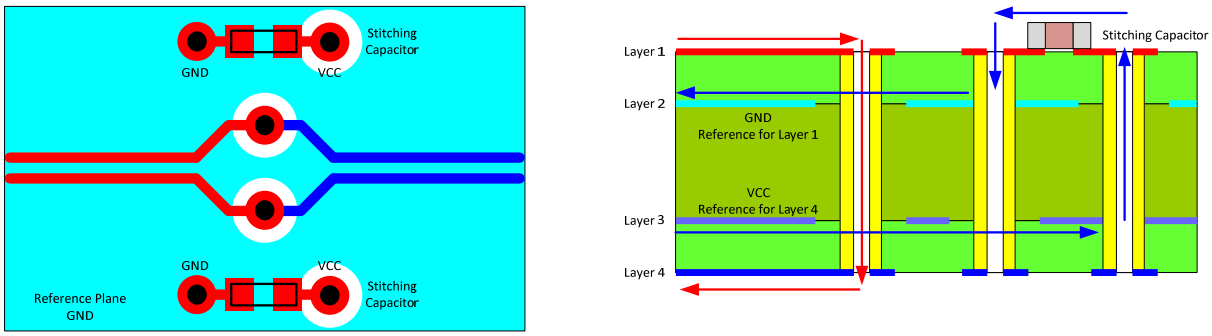


Figure 36: Place stitching capacitors when changing signal reference plane

Avoid routing high speed signals on the edge of reference planes or close to PCB borders. Otherwise, this can adversely affect the trace impedance.

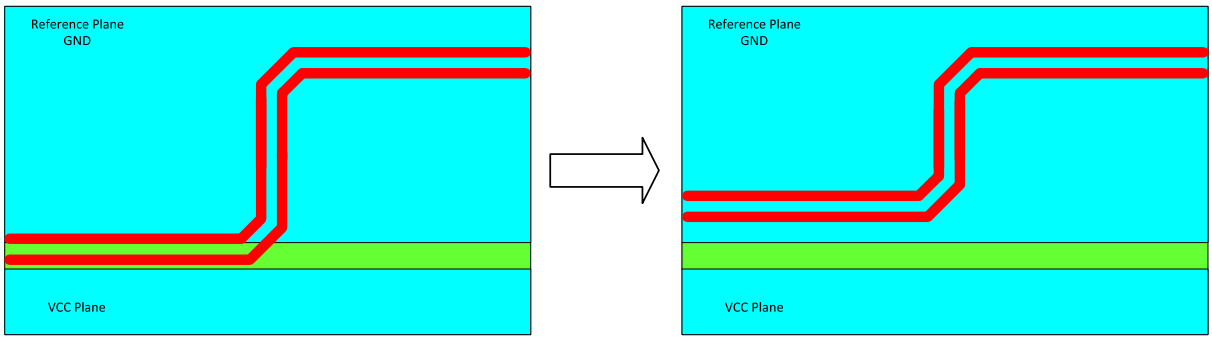


Figure 37: Do not route high speed signals at plane edge or PCB borders

2.3.9 Analogue and Digital Ground

Analogue signals and circuits can be very sensitive to digital noise. There are two main coupling problems which can introduce digital noise into the analogue part. The first one is the capacitive and inductive coupling of the signals. This coupling can be avoided by separating the signals from each other. Special care should be taken if analogue and digital signals are routed in parallel over long distances. Increase the space between such signals as much as possible. Try to keep the analogue part away from clock signals and high current switching components (e.g. power supplies).

The second type of coupling is conductive coupling. The left figure below explains this problem. If the digital and analogue share a common return path for the power supply, the current spikes of the digital circuit can be coupled over the parasitic resistance and inductance to the analogue

supply. The same coupling exists also if the return path of signals is common. It is necessary to separate the return path of the digital circuits from the return path of analogue circuits.

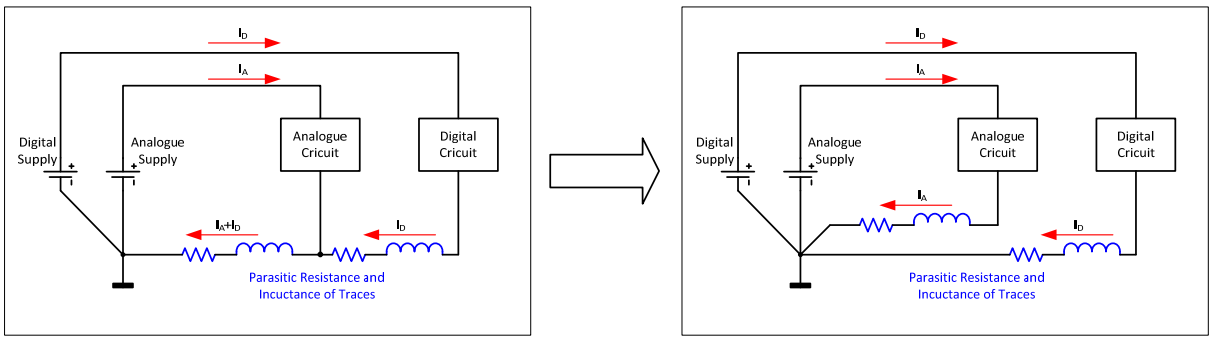


Figure 38: Separate return path of analogue and digital supply and signals

There are two different approaches for the separation of the digital and analogue return path (ground plane separations). The first physically divides the analogue ground planes from the digital one, and is referred to as the "Split Plane Approach". The second divides the grounds virtually, and is similarly referred to as the "Virtual Split Plane Approach". Both approaches have some advantages which make it difficult to judge which one is better.

2.3.9.1 Split Plane Approach

A lot of reference schematics for mixed signal integrated circuits (e.g. ADC) propose a split ground approach. It makes it easy in the schematic to show which components and pins should be connected to a digital ground and which to an analogue ground. Such schematics can be routed by placing two different ground planes as reference. The two planes need to be placed carefully. The analogue ground should only be placed under analogue pins and components. This requires careful placement of the components.

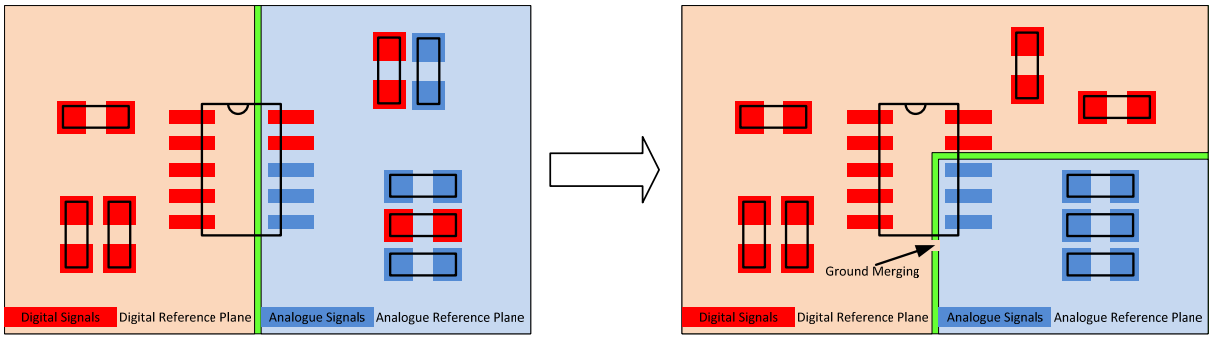


Figure 39: Power plane splitting needs careful placement considerations

Mixed signal circuits need to have the analogue and digital ground connected together at a single location. In reference schematics it is often recommend to place ferrite beads or zero ohm resistors between the two nets. The merging of the digital and analogue ground should be placed close to the integrated circuit which features both analogue and digital signals.

In a mixed signal design with split planes it is important that no digital signal is routed over an analogue ground plane while no analogue signal is routed over the digital ground plane. The two domains need to be completely separated.

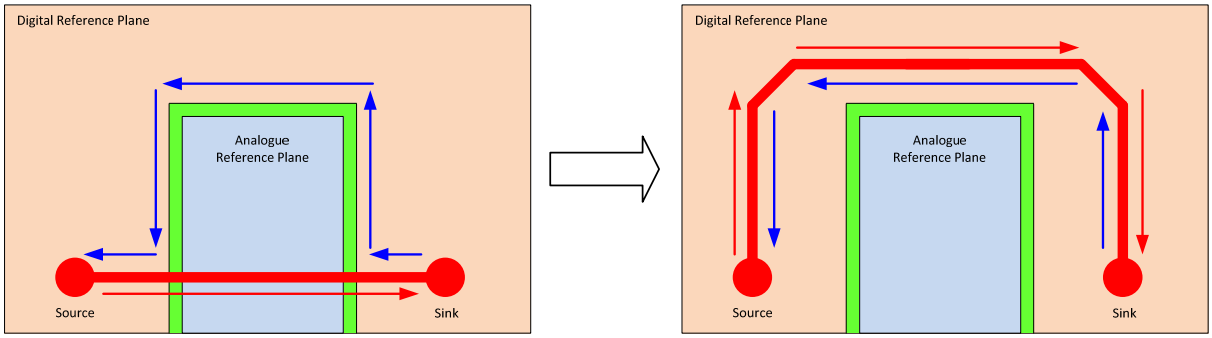


Figure 40: No digital signals are permitted to cross the analogue ground plane

One of the advantages of the split plane approach is that it is clear in the schematic which ground connections are digital and which ones are analogue. In the layout, the separation between the two domains is also clearly visible. Schematic and layout can be less confusing if more than one engineer is working on the project.

2.3.9.2 Virtual Split Approach

The virtual split approach does not split the analogue and digital ground in the schematic diagram. In the layout, the two ground domains are not electrically split. The trick is to implement the layout as if there is an imaginary separation between the analogue and digital ground. Some CAD tools allow drawing a help line on an unused mechanical layer. The components need to be placed carefully on the correct side of the virtual split planes.

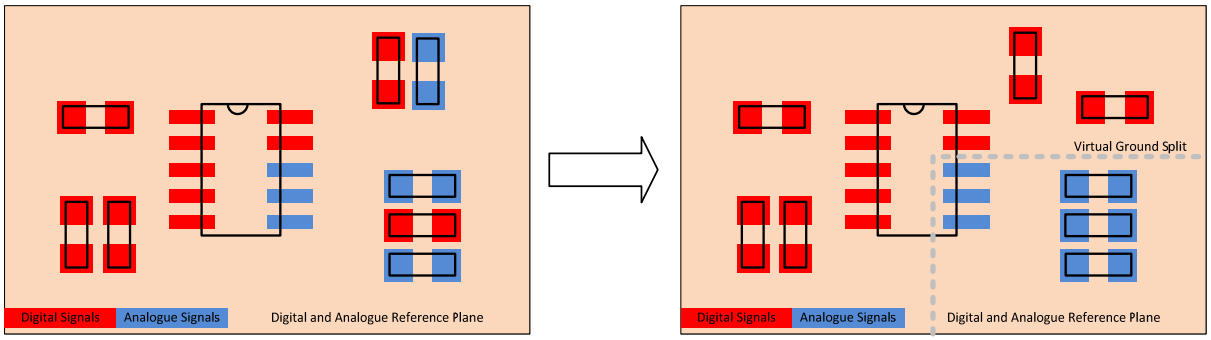


Figure 41: Careful component placement is needed even with virtual plane splitting

The virtual line between the two ground domains needs to be respected during the routing. No digital or analogue signal trace is permitted to cross the virtual split line. The virtual split line should not be placed with a too complicated shape as there are no plane obstructs to keep the analogue and digital return current separated.

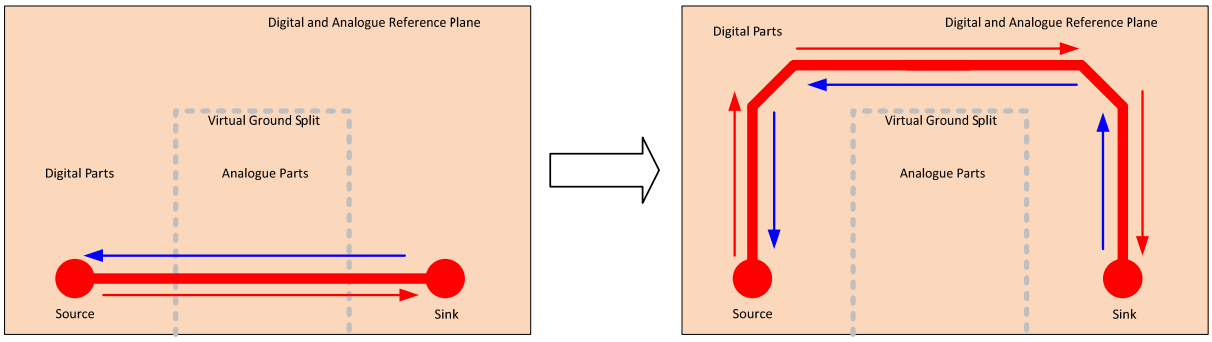


Figure 42: No digital signals are allowed to cross the virtual analogue ground

Routing can be more challenging with the virtual split plane approach, as it is easy to make an improper separation of the two domains which will not be picked up by the DRC. Special care has to be taken that the analogue and digital ground parts are correctly split. If the layout is correctly implemented with this approach, a better solution can be achieved than with the physical split plane approach.

3 Interfaces

3.1 Architecture

The block diagram in Figure 43 shows the basic architecture of the Apalis module, depicting the standard interfaces and some examples of type specific interfaces.

Standard interfaces are interfaces that are compatible between different Apalis modules. The pins are reserved for this specific function and are not used for other purpose. This guarantees electrical compatibility between carrier board designs which only make use of the standard interfaces. This helps to ensure longevity carrier board designs and support for future modules. Some modules may not feature all the standard interfaces. In this case, for the GPIO compatible interfaces, GPIO functionality is provided. Other interfaces might be unconnected at the module side.

Type specific interfaces are interfaces which are not guaranteed to be functionally or electrically compatible between modules. If a carrier board design uses such features, then it is possible that other modules in the Apalis module family do not provide these features and instead provide other features on the associated pins. These interfaces might be electrical incompatible. In this case, the carrier board will be restricted for use only with certain Apalis modules.

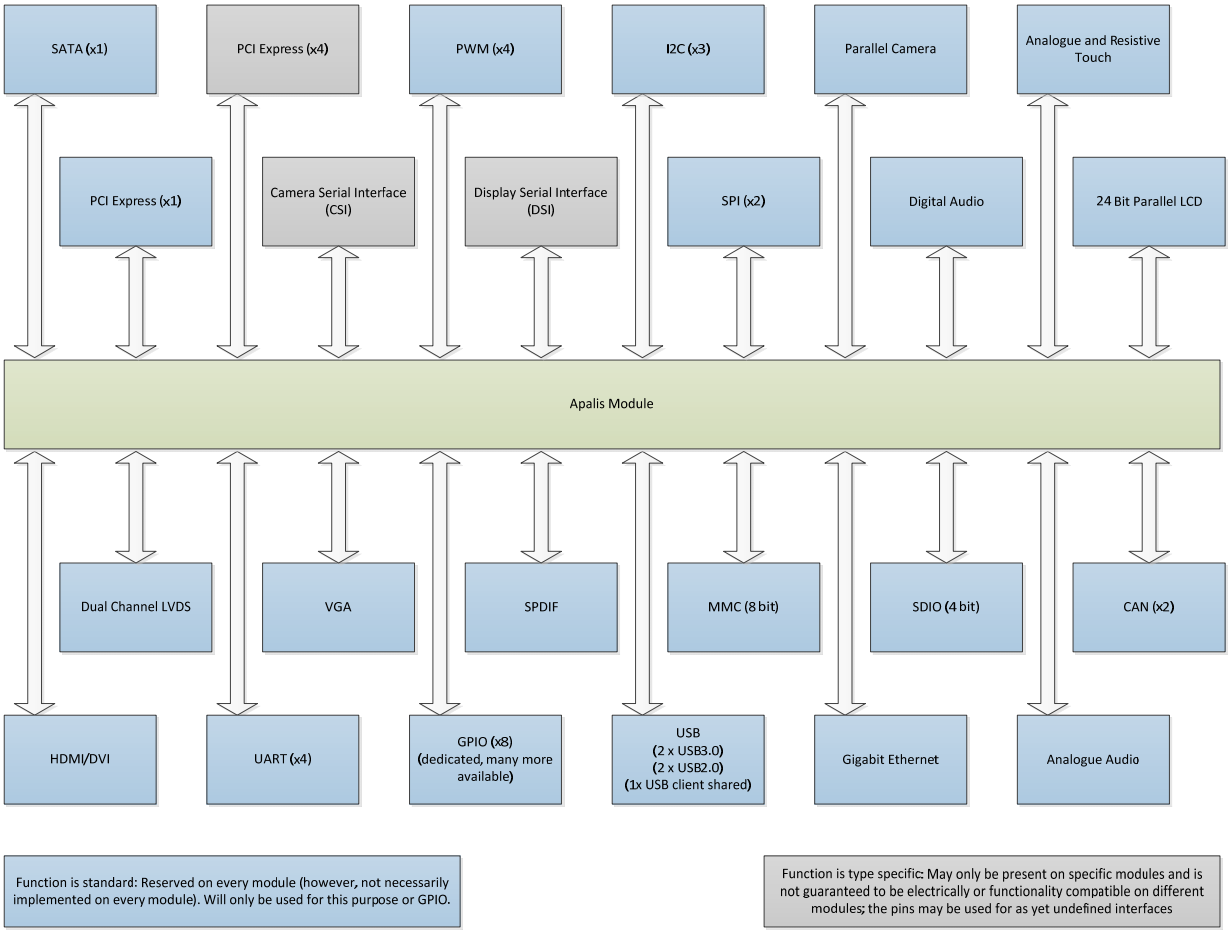


Figure 43: Apalis Module Architecture

3.1.1 Standard Interfaces

The standard interfaces on the Apalis module family guarantees electrical and functional compatibility between module family members. The table below shows an overview of the standard interfaces that are provided by an Apalis module. The "GPIO Capable" column indicates whether the assigned pins can be used as GPIOs. Yes and No are self-Explanatory, Optional indicates that it may be possible for some modules, but not all.

The "Standard" column indicates the number of interfaces that the specification allows for in the standard pin out. Customers should consult the datasheet for specific Apalis module variants to check which interfaces are available for that module. If a module does not feature the complete number of interfaces that is specified by the Apalis standard, the provided interfaces are filled in the order low to high. For example, the Apalis standard features 4 USB ports (port 1 to port 4). If a module only provides 3 USB interfaces, they are provided at port 1, 2 and 3 of the module edge connector. Port 4 will be left unconnected in this case. If a custom carrier board only uses 2 USB interfaces, port 1 and 2 should be used. This guarantees better compatibility with Apalis modules that do not feature all USB ports.

Description	Standard	Note	GPIO Capable
4/5 Wire Resistive Touch	1	Touch wiper shared with analogue input 4	No
Analogue Inputs	4	Minimum 8 bit resolution, 0-3.3V nominal range	No
Analogue Audio	1	Line in L&R, Microphone in, Headphone out L&R	No
CAN	2		Optional
Digital Audio	1	HDA	Yes
Dual Channel LVDS Display	1	1x or 2x single channel or 1x dual channel mode	No
Gigabit Ethernet	1		No
GPIO	8		Yes
HDMI (TDMS)	1		No
I2C	3	Including DDC	Yes
Parallel Camera	1	8 bit YUV	Optional
Parallel LCD	1	24 bit resolution	Optional
PCI-Express (lane count)	1	Single lane and clock	No
PWM	4		Yes
SATA	1		No
SDIO	1	4 bit	Yes
SDMMC	1	8 bit	Yes
S/PDIF	1	1 input, 1 output	Optional
SPI	2		Yes
UART	4	1 Full Function, 1 CTS/RTS, 2 RXD/TXD only	Yes
USB	4	2 x USB 3.0, 2 x USB 2.0, 1 x shared host/client USB 2.0	No
VGA	1		No

Table 5: Standard Interfaces

3.1.2 Type specific Interfaces

Type specific interfaces allow for the possibility of including interfaces which may not yet exist or be widely adopted, or interfaces which may be specific to a particular device or groups of devices. They also offer a mechanism for extending features which are present on the standard interfaces, such as providing additional PCI-Express lanes. This provides the Apalis module with the flexibility of being able to reconfigure a subset of pins for different uses between different modules.

It should be noted that type specific interfaces will be kept common across modules that share such interfaces where possible. For example, if both module A and module B have three additional PCI-Express lanes which are available in the same configurations as a type specific interface, then they shall be assigned to the same pins in the type specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type specific interface.

The signal routing and need for external components for the type specific interfaces are not reflected in this document. Please consult the applicable Apalis module datasheet for more information on these interfaces.

3.1.3 Pin Numbering

The diagrams in the figures below show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema.
Pins on the top side of the module have an even number and pins on the bottom side have an odd number.

The pin number increases linearly as a multiple of the pitch – that is, pins which are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins which do not exist due to the connector notch are also accounted for (pins 166 through 172).

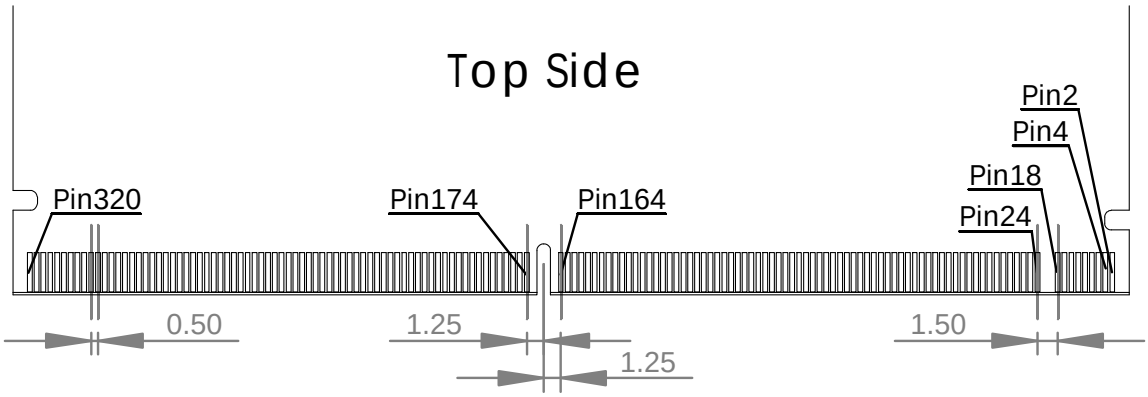


Figure 44: Pin numbering schema on the top side of the module

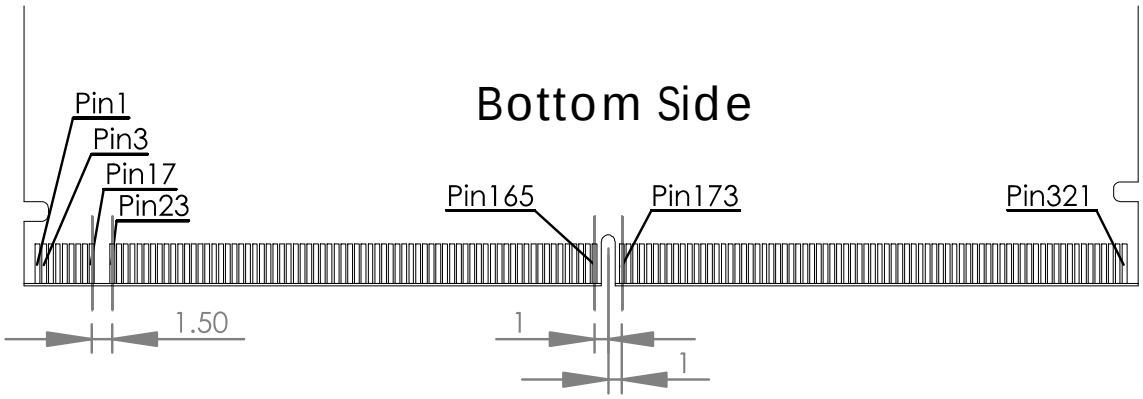


Figure 45: Pin numbering schema on the bottom side of the module

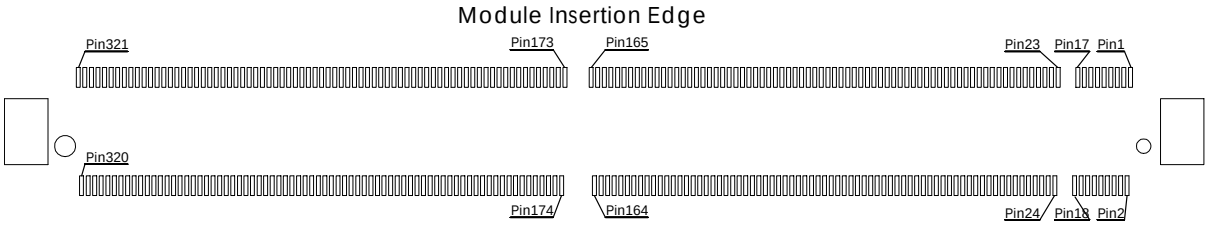


Figure 46: Pin numbering schema on the module connector land pattern

3.2 PCI Express

The Apalis module form factor only features one PCIe lane as standard interface. Depending on the module, there are maybe additional lanes available in the type specific area.

3.2.1 PCIe Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
55	PCIE1_CLK+	O	PCIe		PCIe 100MHz reference clock output positive
53	PCIE1_CLK-	O	PCIe		PCIe 100MHz reference clock output negative
49	PCIE1_TX+	O	PCIe		PCIe transmit data positive
47	PCIE1_TX-	O	PCIe		PCIe transmit data negative
43	PCIE1_RX+	I	PCIe		PCIe receive data positive
41	PCIE1_RX-	I	PCIe		PCIe receive data negative
37	WAKE1_MICO	I	CMOS	3.3V	General purpose wake signal
26	RESET_MOCI#	O	CMOS	3.3V	General reset output of the module
209	I2C1_SDA	I/O	OD	3.3V	I2C interface data, some PICe device need SMB interface for special configuration
211	I2C1_SCL	O	OD	3.3V	I2C interface clock, some PICe device need SMB interface for special configuration

Table 6: PCIe signals

The PCIe interface supports polarity inversion. This means the positive and negative signal pins can be inverted in order to simplify the layout by avoiding crossing of the signals. Some PCIe devices support additional lane reversal for multi-lane interfaces. As the standard interfaces on Apalis provide only a single lane PCIe interface, the lane reversal feature is not relevant to the Apalis specification. Some Apalis modules provide additional multi-lane PCIe interfaces as type specific interfaces. Please consult the datasheets for such modules to determine if lane reversal is applicable and supported.

3.2.2 Layout Requirements

Parameter	Requirement
Max Frequency	Gen1: 1.25GHz (2.5GT/s) Gen2: 2.5GHz (5GT/s) Gen3: 4GHz (8GT/s)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max intra-pair skew	<1ps ≈150µm
Max trace length skew between clock and data pairs	<1.6ns ≈240mm

Parameter	Requirement
Max trace length on carrier board (device-down)	<300mm
Max trace length on carrier board (PCIe slot connector, PCIe Mini card)	<200mm
Minimum pair to pair spacing	>500µm
AC coupling capacitors	100nF ±20%, discrete 0402 package preferable
Maximum allowed via	2 vias for TX traces 4 vias for RX traces (device-down) 2 vias for RX traces (PCIe slot connector, PCIe Mini card)

Table 7: PCIe Layout Requirements

3.2.3 Reference Schematics

The PCIe schematic is different depending on whether the PCIe device is soldered directly to the carrier board (device-down) or is located on a PCIe card. Special care needs to be taken as to whether or not AC coupling capacitors are required. The maximum trace length of the lanes depends on whether the design is for an external card or a device-down.

Every PCIe lane consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Normally, the signals are named from the perspective of the host until reaching the pins of the PCIe device. Therefore, the transmitting pins of the Apalis modules should be called TX at the carrier board while the receiving pins of the module should be called RX. Please carefully read the datasheet of the PCIe device in order to make sure that RX and TX are not inadvertently swapped.

Every PCIe device needs a 100MHz reference clock. It is not permitted to connect a reference clock to two device loads. The Apalis module provides one reference clock output as a standard interface. There may be additional PCIe reference clocks outputs in the type specific area. If there are not enough PCIe reference clocks available (e.g. a PCIe switch is used or the PCIe interfaces in the type specific area do not provide additional clock outputs), a zero delay PCIe clock buffer is required on the baseboard. Some PCIe switches features an internal PCIe clock buffer, which can avoid the necessity of a dedicated clock buffer.

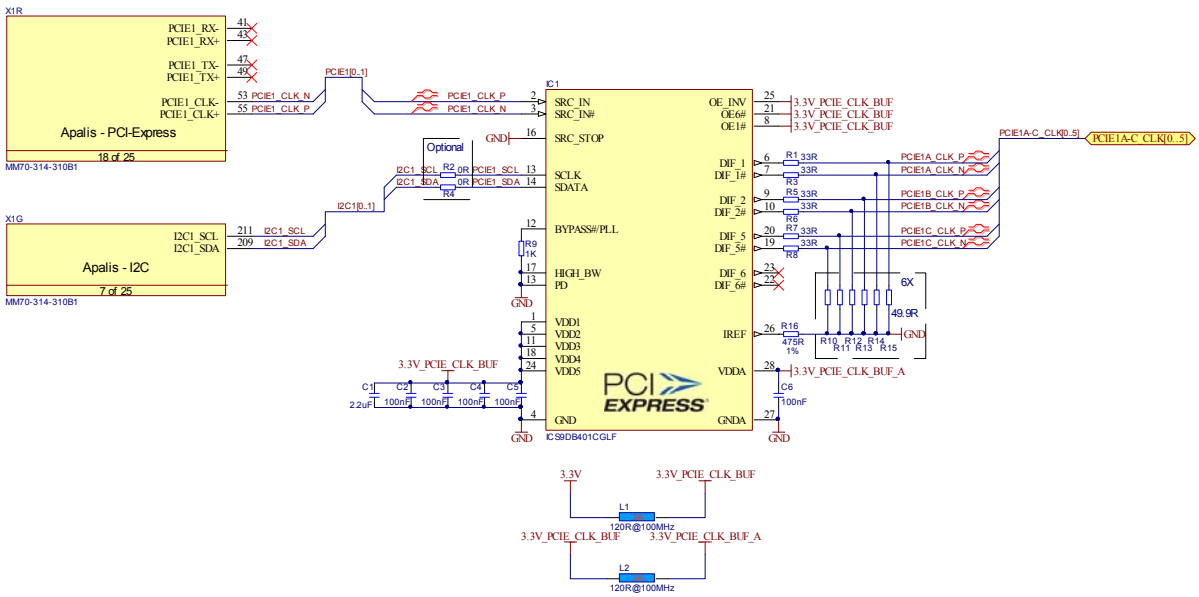


Figure 47: PCIe reference clock buffer example

3.2.3.1 PCIe x1 Slot Schematic Example

The PCIe card slot design defines that the decoupling capacitors for the TX lanes should be placed on the module and the RX lanes on the card. Therefore, no additional decoupling capacitors are permitted to be placed on the carrier board in the RX, TX and reference clock lines.

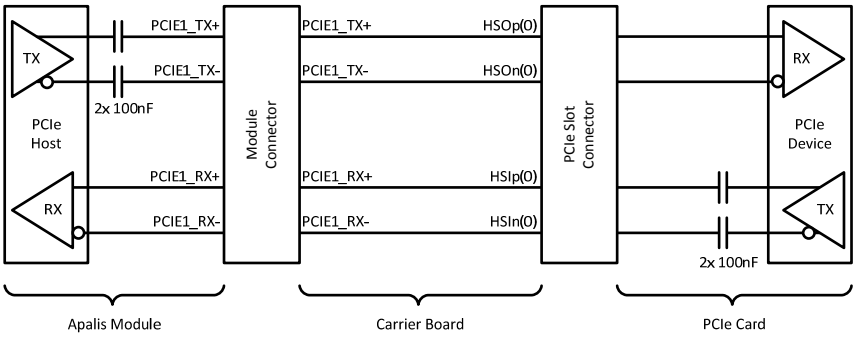


Figure 48: PCIe x1 Slot Block Diagram

The Apalis module standard does not feature a dedicated PCIe reset output as it does not provide the PCIe hot plug functionality. Therefore, the PCIe reset input (PERST#, pin A11) of the slot should be served by the general module reset output (RESET_MOCI#). Some Apalis modules may provide the additional hot plug signals such as reset and hot plug detect as secondary functions or as type specific interfaces. Nevertheless, as the compatibility between different Apalis modules cannot be guaranteed using these hot plug signals, it is recommended that the RESET_MOCI# signal is used as reset.

The PCIe x1 slot uses two card present signals (PRSNT1#, pin A1 and PRSNT2#, pin B18) which are shorted to ground by the card if it is inserted. Again, as the Apalis module standard does not feature the PCIe hot plug feature, these pins can be left unconnected.

The wake output of the PCIe slot (WAKE#, pin B11) can be connected to the general wake input of the Apalis module (WAKE1_MICO#). Wake up capable PCIe cards such as Ethernet cards can use this signal to wake up the module from suspend.

The JTAG interface on the PCIe slot can be left unconnected. This interface is only used for debugging purposes. No termination on the carrier board is needed.

The PCIe slot pin out features an SMB interface for additional power management control. As the SMB and I2C buses are compatible, it is recommended that the I2C1 interface on the Apalis module is used if the SMB interface is needed. Most PCIe cards do not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications.

In addition to the 3.3V input, the PCIe slot features an additional +3.3V aux (pin B10) and +12V (pin A2, A3, B1 and B2). The +3.3V aux is a standby rail for cards that feature wake up functionality. If the card does not need to be powered in standby, it is recommended that this pin is connected to the normal +3.3V supply. Do not leave this pin unconnected.

Not all PCIe cards need the +12V supply. For a battery powered system or a carrier board with a wide voltage input range, it might be difficult to generate a regulate 12V rail. In this case, we recommend checking with the PCIe card(s) manufacturer to determine if the +12V supply is required.

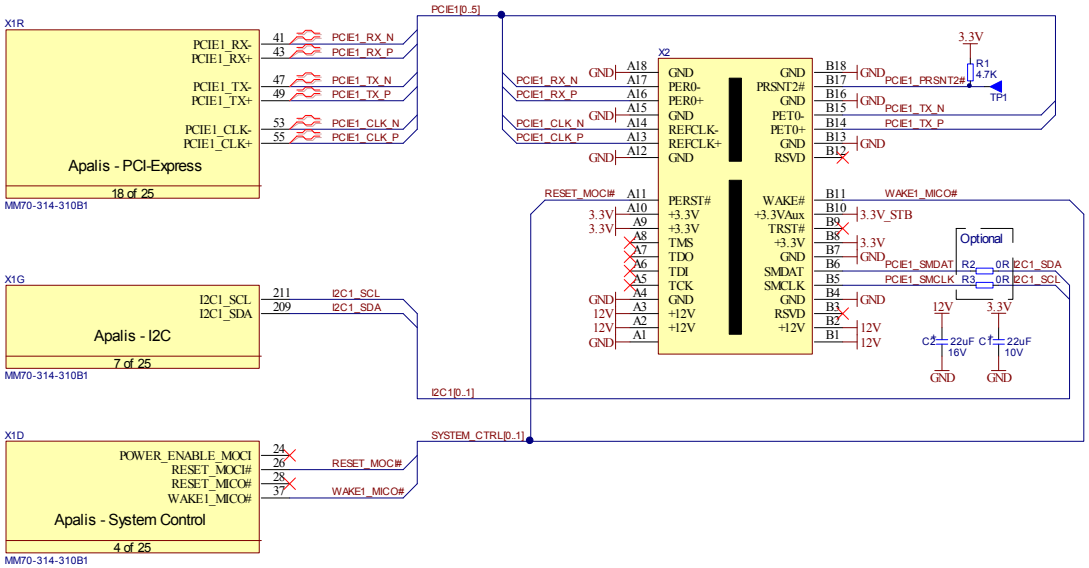


Figure 49: PCIe x1 slot reference schematic

3.2.3.2 Mini PCIe Card Schematic Example

The Mini PCIe Card (also called PCI Express Mini Card, Mini PCI Express or Mini PCIe) also features a USB 2.0 High Speed interface. In order to be compliant, the carrier board needs to provide both interfaces, the PCIe and USB. As most of the Mini PCIe Cards use only one of the interfaces, for an embedded carrier board which is developed for a restricted set of compatible cards, it might be sufficient to implement only the required interface. Check with the Mini PCIe Card vendor whether the USB, PCIe or both interfaces are used by the card.

The Mini PCIe Card features the decoupling capacitors for the RX lines on the card. Therefore, no additional decoupling capacitors should to be placed on the carrier board in either the RX, TX or reference clock lines.

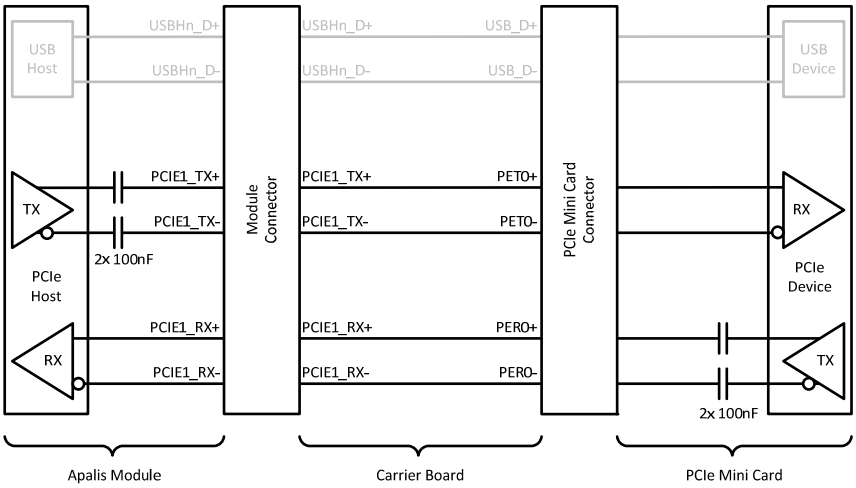


Figure 50: Mini PCIe Card Block Diagram

The Apalis module standard does not feature a dedicated PCIe reset output as it does not provide the PCIe hot plug functionality. Therefore, the PCIe reset input (PERST#, pin 22) of the card should be served by the general module reset output (RESET_MOCI#). Some Apalis modules might provide the additional hot plug signals such as reset and hot plug detect as secondary functions or as type specific interfaces. Nevertheless, as compatibility between different Apalis modules could

not be guaranteed by using these hot plug signals, it is recommended that the RESET_MOCI# signal is used as reset.

The clock request output of the card (CLKREQ#, Pin 7) can be left unconnected. It might also be connected to a free GPIO on the Apalis module. In this case, the clock request functionality needs to be implemented in software.

The wake output of the Mini PCIe Card (WAKE#, pin 1) can be connected to the general wake input of the Apalis module (WAKE1_MICO#). Wake up capable Mini PCIe Cards such as Wi-Fi cards can use this signal to wake up the module from suspend.

The R-UIM interface of the Mini PCIe Card (UIM, pin 8, 10, 12, 14 and 16) are only needed for mobile broadband modem cards such as 3G cards. If the card interface needs to support such modems, an additional SIM card holder needs to be attached to this interface.

The Mini PCIe Card pin out features an SMB interface for additional power management control. As the SMB and I2C buses are compatible, it is recommended that the I2C1 interface on the Apalis module is used if the SMB interface is needed. Most PCIe cards do not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications.

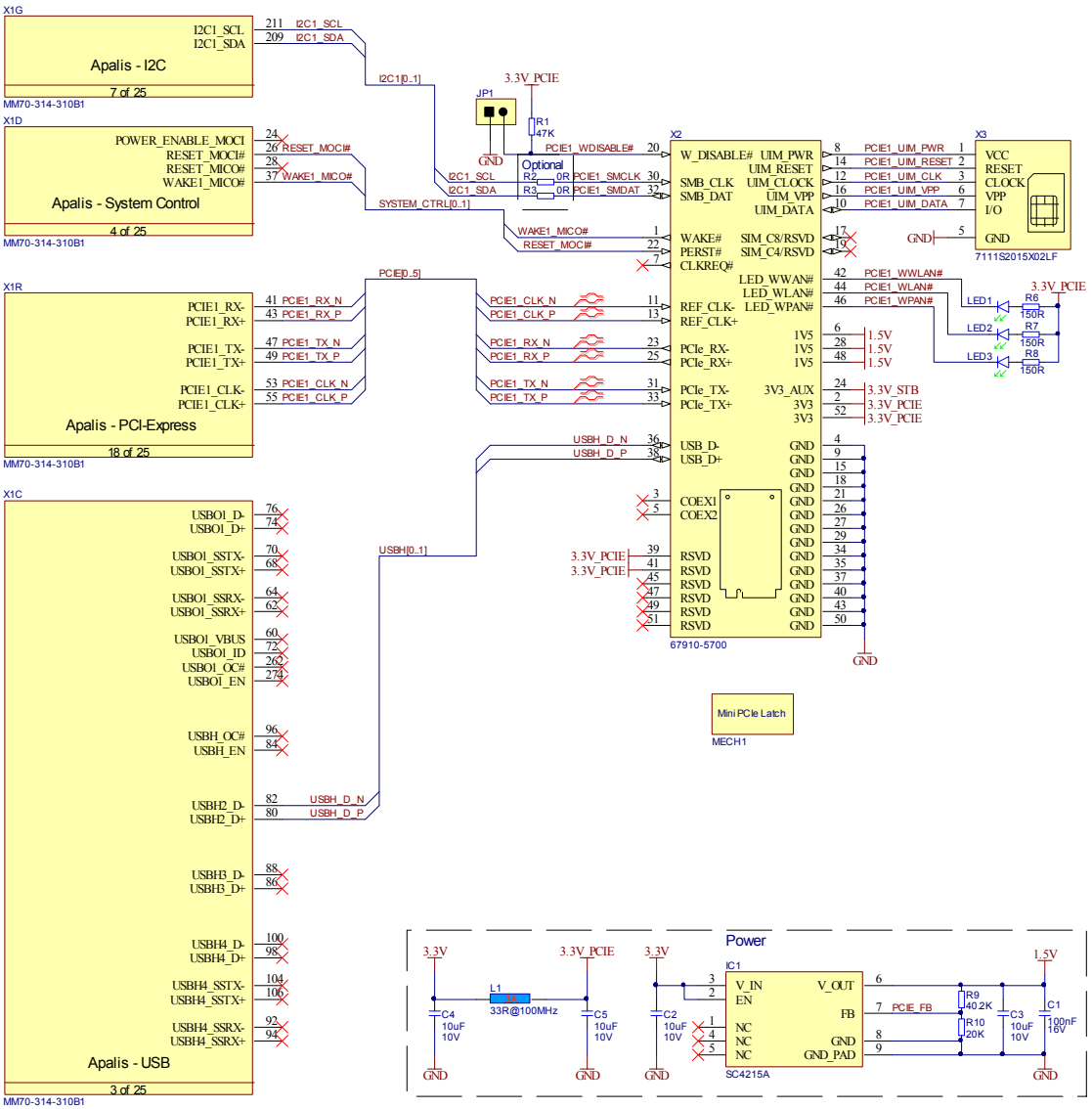


Figure 51: Mini PCIe card reference schematic

3.2.3.3 PCIe x1 Device-Down Schematic Example

Device-Down means that the PCIe device is soldered directly to the carrier board. The decoupling capacitors for the RX lanes (TX from the device) need to be placed on the carrier board. As the capacitors for the TX lanes are located on the Apalis module, no additional capacitors should be place on the TX lines. The reference clock lines do not need decoupling capacitors.

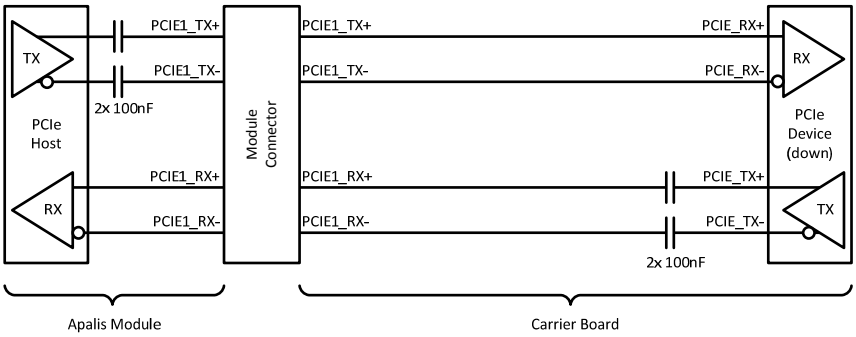


Figure 52: PCIe Device-Down block diagram

The schematic diagram below is an example of a device-down design of a gigabit Ethernet controller. Please be aware that the TX lane from the module needs to be connected to the RX input of the controller. The RX lane from the module needs to be connected to the TX output of the controller. Check your device carefully to determine whether it needs this crossing or not.

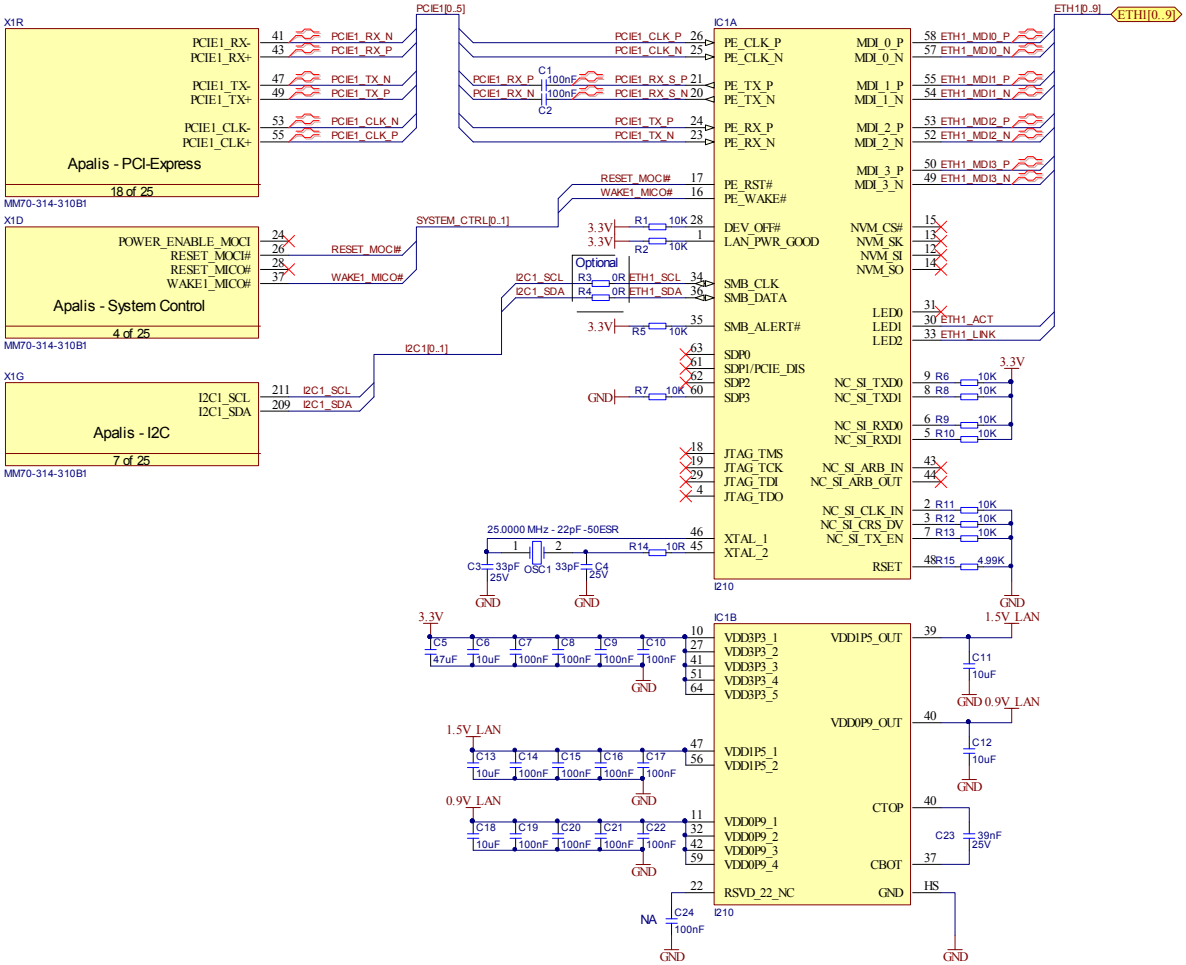


Figure 53: PCIe Device-Down example schematic

3.2.4 Unused PCIe Signals Termination

Apalis Pin	Apalis Signal Name	Recommended Termination
55	PCIE1_CLK+	Leave NC if not used
53	PCIE1_CLK-	Leave NC if not used
49	PCIE1_TX+	Leave NC if not used
47	PCIE1_TX-	Leave NC if not used
43	PCIE1_RX+	Preferable connect to GND if not used or leave NC
41	PCIE1_RX-	Preferable connect to GND if not used or leave NC
37	WAKE1_MICO	Add pull up resistor or disable the wake function in software
26	RESET_MOCI#	Leave NC if not used
209	I2C1_SDA	Add pull up resistor or disable the I^2C function in software
211	I2C1_SCL	Add pull up resistor or disable the I^2C function in software

Table 8: Unused PCIe Signals Termination

3.3 SATA

The Apalis module form factor features one SATA interface as standard interface. Depending on the module, there are maybe additional interfaces type specific SATA interfaces available.

3.3.1 SATA Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
33	SATA1_TX+	O	SATA		SATA transmit data positive
31	SATA1_TX-	O	SATA		SATA transmit data negative
25	SATA1_RX+	I	SATA		SATA receive data positive
27	SATA1_RX-	I	SATA		SATA receive data negative
35	SATA1_ACT#	O	OD	3.3V	Activity indication LED output, active low

Table 9: SATA Signals

The SATA interface does not support polarity inversion. This means the positive and negative signal pins cannot be swapped for layout simplification.

3.3.2 Layout Requirements

Parameter	Requirement
Max Frequency	SATA I: 750MHz (1.5GT/s) SATA II: 1.5GHz (3GT/s) SATA III: 3GHz (6GT/s)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 55Ω ±15% single ended
Max intra-pair skew	<1ps ≈150µm
Max trace length skew between data pairs	<0.8ns ≈120mm
Max trace length on carrier board	<150mm
Minimum pair to pair spacing	>500µm

Parameter	Requirement
AC coupling capacitors	No coupling capacitors needed on the carrier board
Maximum allowed via	2 vias for RX and TX traces

Table 10: SATA layout requirements

3.3.3 Reference Schematics

Every SATA interface consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as at the end, the transmitter of the host needs to be connected to the receiver of the device and vice versa. Normally, the signals are named after the host until they reach the pins of the SATA device. Therefore, the transmitting pins of the Apalis modules should be called TX on the carrier board while the receiving input pins of the Apalis module should be called RX.

3.3.3.1 SATA Connector Schematic Example

The AC coupling capacitors for the RX and TX lines are placed on the Apalis module. Therefore, no additional serial capacitors are needed nor permitted on the carrier board.

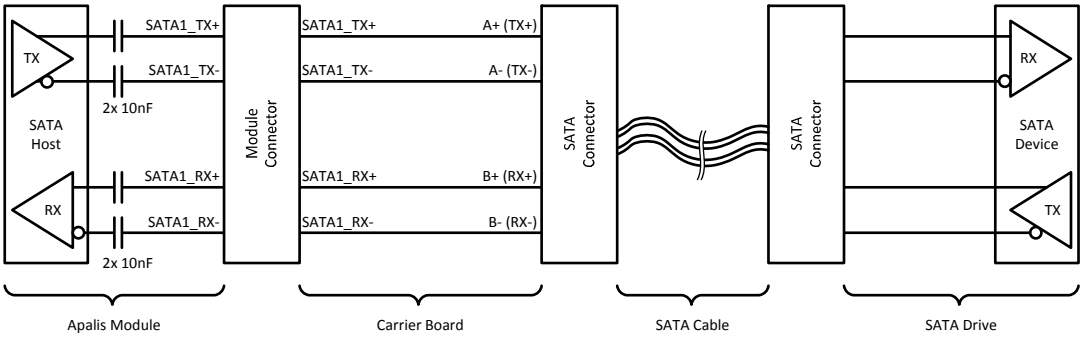


Figure 54: SATA connector block diagram

Additional to the RX and TX pairs, the SATA interface on the Apalis module features a LED output signal for signalling activity at the SATA interface (SATA1_ACT#). This information is provided by the host driver. The signal type is open drain. Therefore a pull up resistor is required on the carrier board. As the signal is used as signal reference for the SATA1_TX+ signal in the MXM3 connector, a strapping capacitor of 1nF should be placed from SATA1_ACT# to GND close to the MXM3 connector.

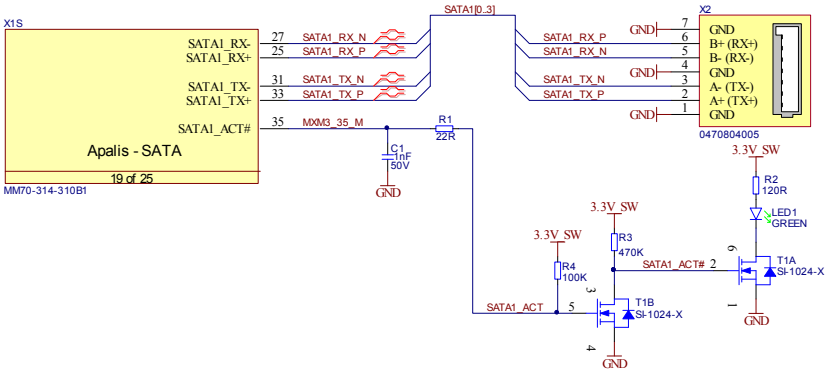


Figure 55: SATA connector reference schematic

3.3.3.2 mSATA Card Schematic Example

Mini-SATA is a standard for solid state drive cards that uses the Mini PCIe Card connector and clip. The pin-out is electrically compatible, but the PCIe data signals are connected to the SATA

interface instead. Please do not confuse mSATA with Mini PCIe Cards solid state drives. These cards feature an on module flash controller with PCIe interface.

As the AC coupling capacitors for both RX and TX lines are placed on the Apalis module, no extra serial capacitors are required on the carrier board.

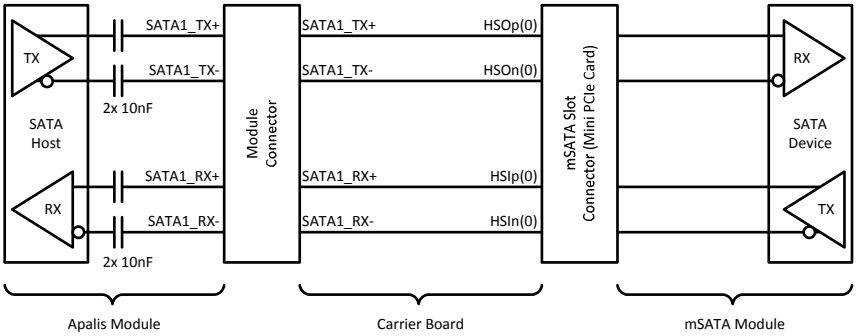


Figure 56: mSATA block diagram

The mSATA pin-out features an activity indication output (pin49). This is output indicates the activity of the SATA device controller similar to the SATA1_ACT# output of the Apalis module. Both signals are designed to drive an indication LED. As the output of the mSATA card is not mandatory, it is recommended that the SATA1_ACT# output of the Apalis module is used instead.

Pin 51 of the mSATA connector can be used to detect whether an mSATA card is present or not. This signal could be used for switching the SATA/PCIe signal in an mSATA/Mini PCIe Card dual design.

The mSATA does not make use of the SMB interface. Therefore, the I2C1 interface does not need to be connected to the mSATA connector.

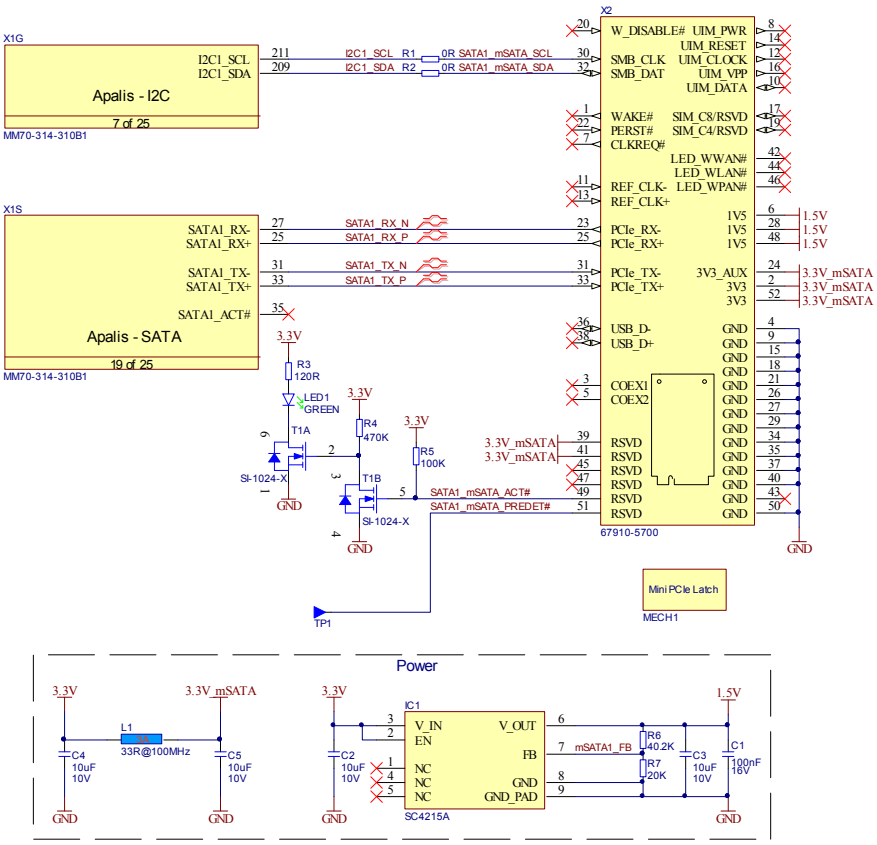


Figure 57: mSATA reference schematic

3.3.4 Unused SATA Signals Termination

Apalis Pin	Apalis Signal Name	Recommended Termination
33	SATA1_TX+	Leave NC if not used
31	SATA1_TX-	Leave NC if not used
25	SATA1_RX+	Preferable connect to GND if not used or leave NC
27	SATA1_RX-	Preferable connect to GND if not used or leave NC
35	SATA1_ACT#	Leave NC if not used

Table 11: Unused SATA signal termination

3.4 Ethernet

The Apalis module standard features a single Gigabit Ethernet (1000Base-T) interface port. The interface is backward compatible with the 10/100Mbit Ethernet (10/100Base-TX) standard.

3.4.1 Ethernet Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
50	ETH1_MDI0+	I/O	Analogue		1000Base-T: DA+ 10/100Base-TX: Transmit +
48	ETH1_MDI0-	I/O	Analogue		1000Base-T: DA- 10/100Base -TX: Transmit -
56	ETH1_MDI1+	I/O	Analogue		1000Base-T: DB+ 10/100Base -TX: Receive +
54	ETH1_MDI1-	I/O	Analogue		1000Base-T: DB- 10/100Base -TX: Receive -
32	ETH1_MDI2+	I/O	Analogue		1000Base-T: DC+ 10/100Base -TX: Unused
34	ETH1_MDI2-	I/O	Analogue		1000Base-T: DC- 10/100Base -TX: Unused
38	ETH1_MDI3+	I/O	Analogue		1000Base-T: DD+ 10/100Base -TX: Unused
40	ETH1_MDI3-	I/O	Analogue		1000Base-T: DD- 10/100Base -TX: Unused
46	ETH+_CTREF	O	Analogue		Centre tap supply
42	ETH1_ACT	O	CMOS	3.3V	LED indication output for activity on the Ethernet port
44	ETH1_LINK	O	CMOS	3.3V	LED indication output for established Ethernet link

Table 12: Ethernet signals

3.4.2 Layout Requirements

Parameter	Requirement
Max Frequency	10Base-T: 10MHz (10Mbit/s) 100Base-TX: 31.25MHz (100Mbit/s) 1000Base-T: 62.5MHz (1Gbit/s)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	95Ω ±15% differential; 55Ω ±15% single ended
Max intra-pair skew	<1.6ps ≈250µm
Max trace length skew between data pairs	<330ps ≈50mm
Max trace length on carrier board between module connector and magnetics	<~100mm, keep it as short as possible

Parameter	Requirement
Max trace length on carrier board between magnetics and Ethernet Jack (discrete magnetics)	Place magnetics as close as possible to the Ethernet connector in order to reduce EMC and ESD problems. Separate the reference ground under the traces between magnetics and Ethernet connector. Keep a minimum distance of 2mm between this ground and the common ground.
Minimum pair to pair spacing	>450µm
Minimum spacing between MDI signals and other high speed signals	>7.5mm
Minimum spacing between MDI signals and low speed signals	>2.5mm
Maximum allowed via	2 vias for all MDI traces

Table 13: Ethernet layout requirements

3.4.3 Reference Schematics

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care has to be taken to route the signals between the magnetics and Ethernet connector. If only Fast Ethernet (100Mbit/s) is required, some design cost may be saved by using only 10/100Base-TX magnetics.

The Ethernet MDI signals are analogue differential pair signals which need to be routed carefully. Try to keep the MDI signals as short as possible and keep them away from digital signals. Try to avoid any stubs on these signals.

The LED output signals ETH1_ACT and ETH1_LINK can be connected directly to the LED of the Ethernet jack with suitable serial resistors. There is no need for additional buffering if the current draw does not exceed 10mA. The ETH1_ACT signal is used as reference for the ETH1_MDI3- signal in the MXM3 connector, a strapping capacitor of 1nF should be placed to GND close to the MXM3 connector.

3.4.3.1 Gigabit Ethernet Schematic Example (Integrated Magnetics)

The need for centre tap voltage depends on the Ethernet PHY used on the Apalis module. In order to keep the carrier board compatible with all Apalis modules, the centre tap pins of the magnetics should all be connected to the centre tap voltage source pin of the module connector (ETH1_CTREF). Please add a ferrite bead and capacitors according to the reference schematic.

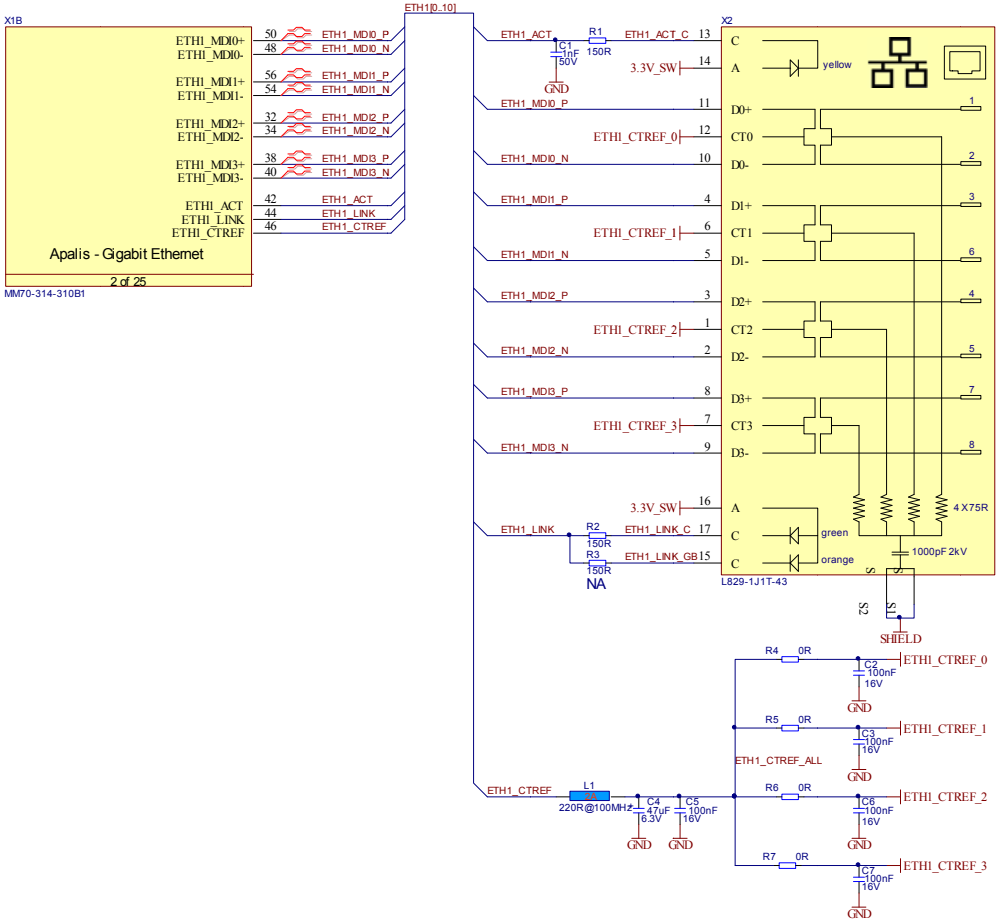


Figure 58: Gigabit Ethernet with integrated magnetics reference schematic

3.4.3.2 Gigabit Ethernet Schematic Example (Discrete Magnetics)

If discrete magnetics are used instead of a RJ-45 Ethernet jack with integrated magnetics, special care has to be taken to route the signals between the magnetics and the jack. These signals are required to be high voltage isolated from the other signals. It is therefore necessary to place a dedicated ground plane under these signals which has a minimum separation of 2mm from every other signal and plane. Additionally, a separate shield ground for the LAN device is needed. Try to place the magnetics as close as possible to the Ethernet jack. This reduces the length of the signal traces between the magnetics and jack.

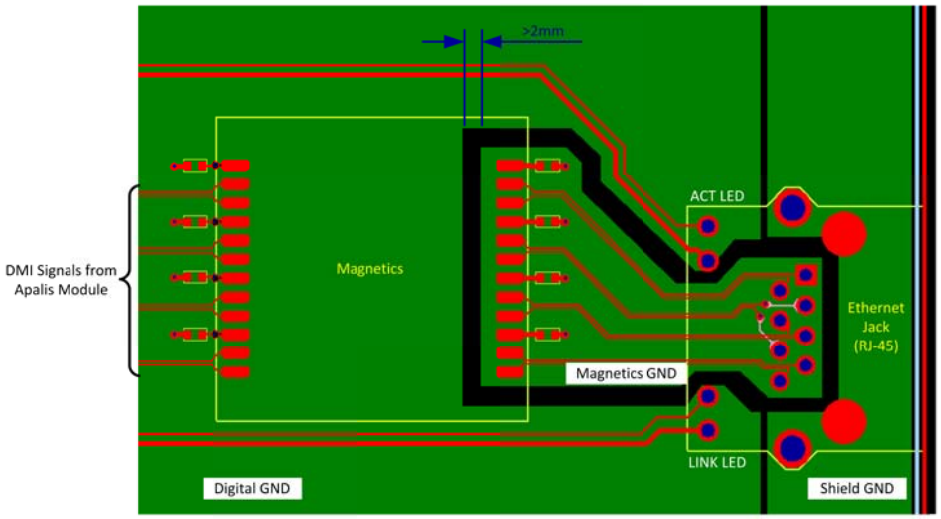


Figure 59: Separation of magnetics ground

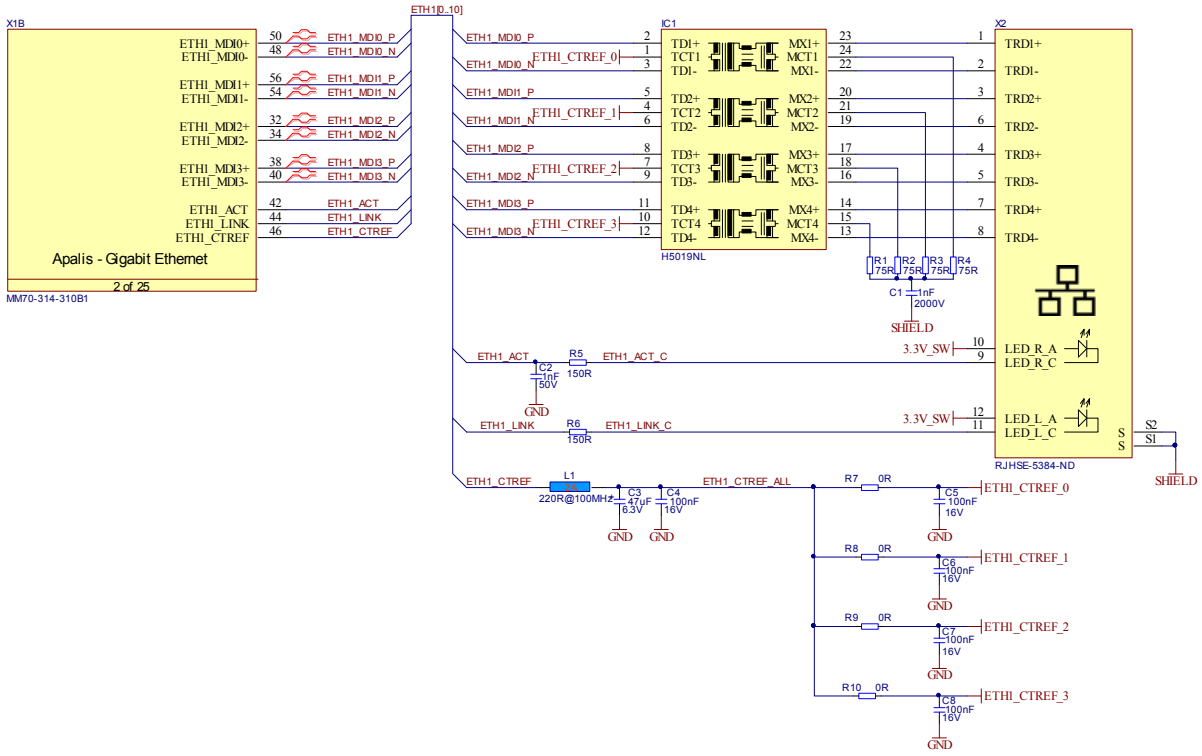


Figure 60: Gigabit Ethernet with discrete magnetics reference schematic

3.4.3.3 10/100Mbit Ethernet Schematic Example (Integrated Magnetics)

The Fast Ethernet interface uses the MDI0 as transmitting lanes and the MDI1 as receiving lane. As most Ethernet PHYs feature Auto-MDIX, the signal direction RX and TX could be swapped. It is strongly recommend that RX and TX lanes are not swapped in order to ensure compatibility between all Apalis modules.

The MDI2 and MDI3 lanes are not used for the 10/100Base-TX interface. These signals can be left unconnected. Most of the Fast Ethernet PHYs do not need a centre tap voltage. Even so, it is recommend the centre tap pins of the magnetics are connected to the centre tap source pin of the Apalis module connector.

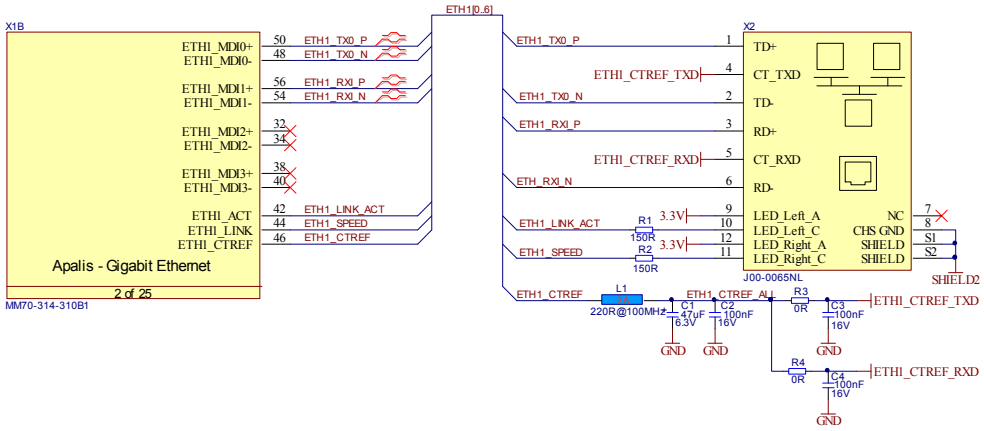


Figure 61: Fast Ethernet with integrated magnetics reference schematic

3.4.4 Unused Ethernet Signals Termination

All unused Ethernet signals can be left unconnected.

3.5 USB

3.5.1 USB Signals

The Apalis standard features four USB interfaces. Two of them support the additional signals required for USB 3.0 Super Speed. One of the USB interfaces features the additional signals that are needed for OTG. The following table shows the possible features for each USB interface in the Apalis module standard. Please note, not all Apalis modules will provide all four USB interfaces or all USB features. Please check the datasheet for the respective Apalis module in order to determine which features are supported.

Apalis Port	1.5Mbit/s Low Speed (1.1)	12 Mbit/s Full Speed (1.1)	480Mbit/s High Speed (2.0)	5Gbit/s Super Speed (3.0)	OTG
USBO1	✓	✓	✓	✓	✓
USBH2	✓	✓	✓		
USBH3	✓	✓	✓		
USBH4	✓	✓	✓	✓	

Table 14: Maximum possible supported features for the USB ports

The USBO1 is a Super Speed OTG capable interface. As most Apalis modules will use this USB port for debugging and flash memory recovery, it is recommended that this interface is accessible even for carrier board designs which do not need any USB interface. This USB port does not share any signals with the other ports and has its own power enable and over current signals.

The additional data links for USB 3.0 Super Speed run at 5 Gbit/s and are fully compliant with the PCI Express Base Specification, Revision 2.0. Super Speed signals support polarity inversion. This means the positive and negative signal pins can be inverted in order to simplify the layout by avoiding crossover of the signals. It is not permitted to swap the receiving signals with the transmitting ones. The USB 2.0 data signals do not support polarity inversion; D+ and D- cannot be swapped.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
74	USBO1_D+	I/O	USB	3.3V	Positive differential USB signal, OTG capable
76	USBO1_D-	I/O	USB	3.3V	Negative differential USB signal, OTG capable
62	USBO1_SSRX+	I	USB		Positive differential receiving signal for USB3.0, OTG capable
64	USBO1_SSRX-	I	USB		Negative differential receiving signal for USB3.0, OTG capable
68	USBO1_SSTX+	O	USB		Positive differential transmission signal for USB3.0, OTG capable
70	USBO1_SSTX-	O	USB		Negative differential transmission signal for USB3.0, OTG capable
72	USBO1_ID	I	CMOS	3.3V	Cable identification pin for the OTG
60	USBO1_VBUS	I	CMOS	3.3V/ 5V tolerant	Bus voltage detection in the OTG client mode
274	USBO1_EN	O	CMOS	3.3V	Enable signal for the bus voltage output in host mode for the USBO1 interface
262	USBO1_OC#	I	OD	3.3V	Over current input signal for the USBO1 interface

Table 15: USBO1 signals

USBH2 and USBH3 ports do not provide the additional data signals for Super Speed USB3.0. The power enable and over current signals are shared also with the USBH4 port.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
80	USBH2_D+	I/O	USB	3.3V	Positive differential USB host signal
82	USBH2_D-	I/O	USB	3.3V	Negative differential USB host signal
84	USBH_EN	O	CMOS	3.3V	Enable signal for the bus voltage output, shared with all USB host ports
96	USBH_OC#	I	OD	3.3V	Over current input signal, shared with all USB host ports

Table 16: USBH2 signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
86	USBH3_D+	I/O	USB	3.3V	Positive differential USB host signal
88	USBH3_D-	I/O	USB	3.3V	Negative differential USB host signal
84	USBH_EN	O	CMOS	3.3V	Enable signal for the bus voltage output, shared with all USB host ports
96	USBH_OC#	I	OD	3.3V	Over current input signal, shared with all USB host ports

Table 17: USBH3 signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
98	USBH4_D+	I/O	USB	3.3V	Positive differential USB host signal
100	USBH4_D-	I/O	USB	3.3V	Negative differential USB host signal
94	USB H4_SSRX+	I	USB		Positive differential receiving host signal for USB3.0
92	USB H4_SSRX-	I	USB		Negative differential receiving host signal for USB3.0
106	USBH4_SSTX+	O	USB		Positive differential transmission host signal for USB3.0
104	USB H4_SSTX-	O	USB		Negative differential transmission host signal for USB3.0
84	USBH_EN	O	CMOS	3.3V	Enable signal for the bus voltage output, shared with all USB host ports
96	USBH_OC#	I	OD	3.3V	Over current input signal, shared with all USB host ports

Table 18: USBH4 signals

3.5.2 Layout Requirements

3.5.2.1 USB 2.0 Signals

Parameter	Requirement
Max Frequency	Low Speed: 750kHz (1.5Mbit/s) Full Speed: 6MHz (12Mbit/s) High Speed 240MHz (480Mbit/s)
Configuration /Device Organisation	1 load (10pF High Speed, 150pF Full Speed, 600pF Low Speed)
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max intra-pair skew	<7.5ps ≈1.1m
Max trace length on carrier board (USB3.0 connector)	<200mm
Minimum pair to pair spacing	>500µm
AC coupling capacitors	No coupling capacitors allowed
Maximum allowed via	A minimum amount of vias should be used.

Table 19: USB2.0 layout requirements

3.5.2.2 USB 3.0 Signals

Parameter	Requirement
Max Frequency	Super Speed: 2.5GHz (5GT/s)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max intra-pair skew	<1ps ≈150µm
Max trace length skew between RX and TX data pairs	<1.6ns ≈240mm
Max trace length on carrier board (USB3.0 connector)	<200mm
Minimum pair to pair spacing	>500µm
AC coupling capacitors	100nF ±20%, discrete 0402 package preferable
Maximum allowed via	2 vias for TX traces 4 vias for RX traces (device-down) 2 vias for RX traces (USB3.0 connector)

Table 20: USB3.0 layout requirements

3.5.3 Reference Schematics

As the additional Super Speed USB 3.0 data signals are PCIe Gen2 signals at the physical layer, the schematic requirements are similar to those for PCIe. This means AC coupling capacitors are required. The placement of the capacitors depends whether the USB 3.0 device is populated on the carrier board (device-down) or is connected over a cable. The USB 2.0 data signals do not need any coupling capacitors.

The Super Speed interface consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Normally, the signals are named after the host until they reach the pins of the USB device. Therefore, the transmitting pins on the Apalis module should be called TX on the carrier board while the receiving pins should be called RX. Please carefully read the datasheet of the USB device (device-down) in order to ensure RX and TX are not confused.

3.5.3.1 USB 3.0 OTG Schematic Example

The AC coupling capacitors for the Super Speed TX signals are located on the Apalis module while the capacitors for the RX signals are located on the USB device. No additional series capacitors are required nor permitted on the Carrier board. The USB 2.0 data signals do not need any series capacitors at all.

If the USB signals are externally available, ESD protection diodes need to be placed at all the USB signals. Make sure that the protection diodes are USB 3.0 compliant. The USB 2.0 signals additionally require a common mode choke for passing EMI testing. Use common mode chokes that are specified for High Speed USB 2.0.

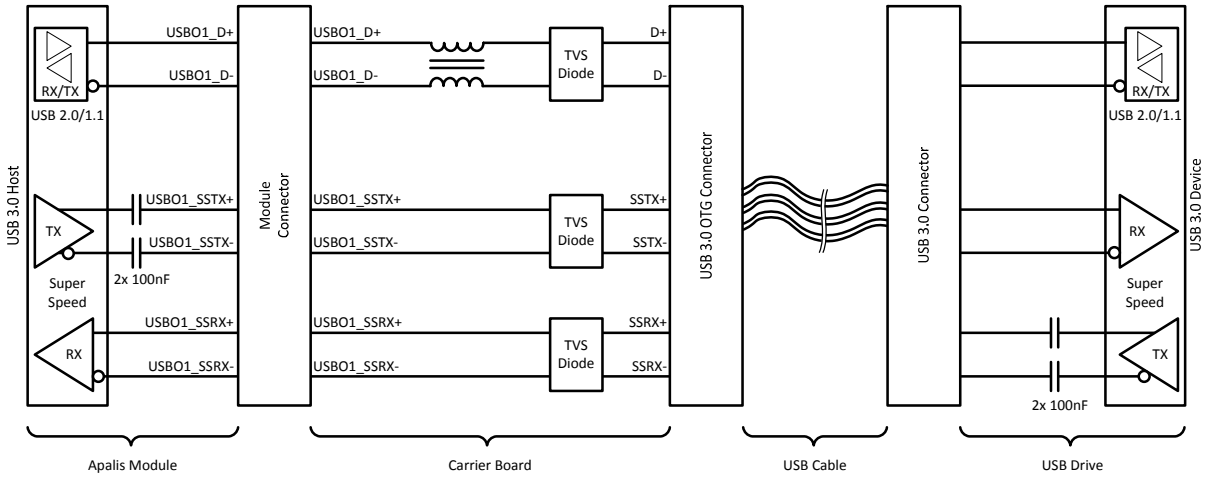


Figure 62: USB 3.0 OTG Block Diagram

The USBO1_ID signal is used to detect which type of USB connector is plugged into the OTG jack (Micro-AB jack). When a Micro-A connector is inserted, the ID pin is connected to signal ground, causing the OTG port to be configured as a host. If a Micro-B USB connector is inserted, the ID pin is left unbiased and the OTG port will be configured as a slave device. For the USBO1_ID signal a pull up resistor to 3.3V is needed.

The USBO1_VBUS input signal is only used if the OTG port is in client mode (Micro-B USB connector plugged in or by software configured as slave only). The signal is used to detect whether a host is connected on the other end of the USB cable. This signal is 5V tolerant and can be connected directly to the power supply pin of the USB jack. ESD protection diodes should be used for this signal.

The USBO1_EN and USBO1_OC# signals are only used when the OTG port is operating in host mode (Micro-A USB connector is plugged in or the port is configured by software as host only). The USBO1_EN signal is used to enable the USB bus power supply if it needs to be switchable. A USB compliant design needs to detect over current on the USB bus power supply and switch the power off should an over-current condition occur. The USBO1_OC# signal is used to signal to the host controller that an over-current condition has occurred. This signal is active low and requires a pull up resistor on the baseboard.

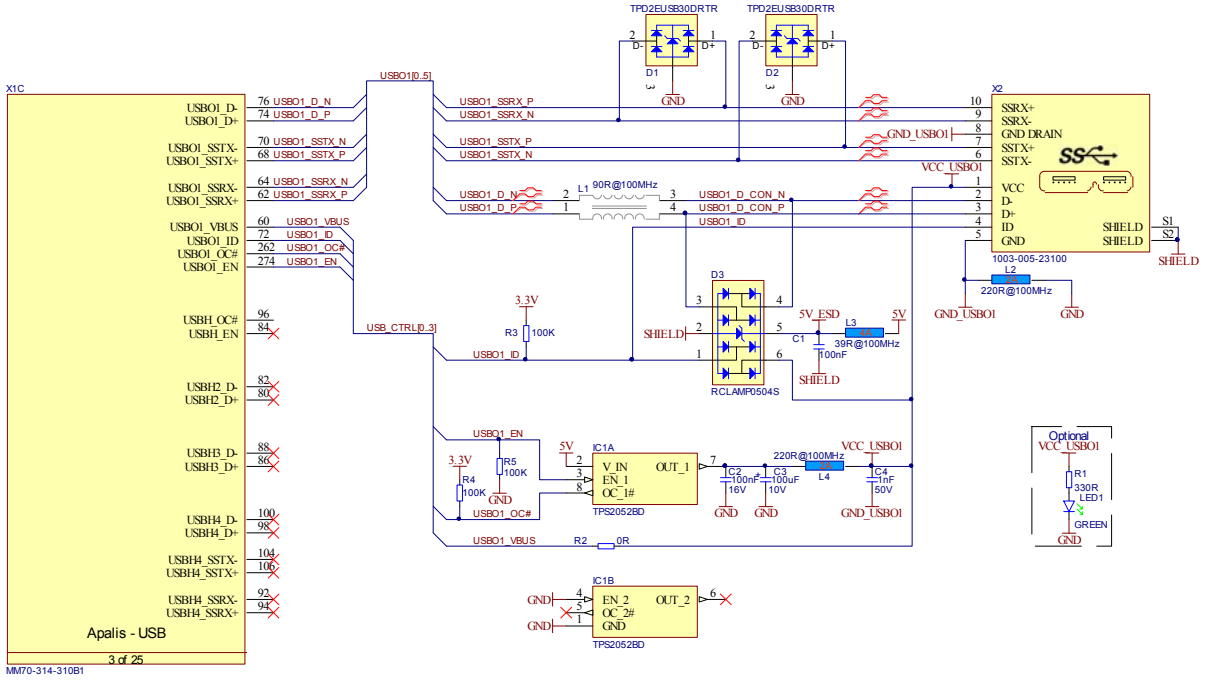


Figure 63: USB 3.0 OTG reference schematic

3.5.3.2 USB 2.0 Client Schematic Example

If the USBO1 port is used only as high speed client interface (e.g. if only used as debugging interface), a simplified schematic diagram is necessary.

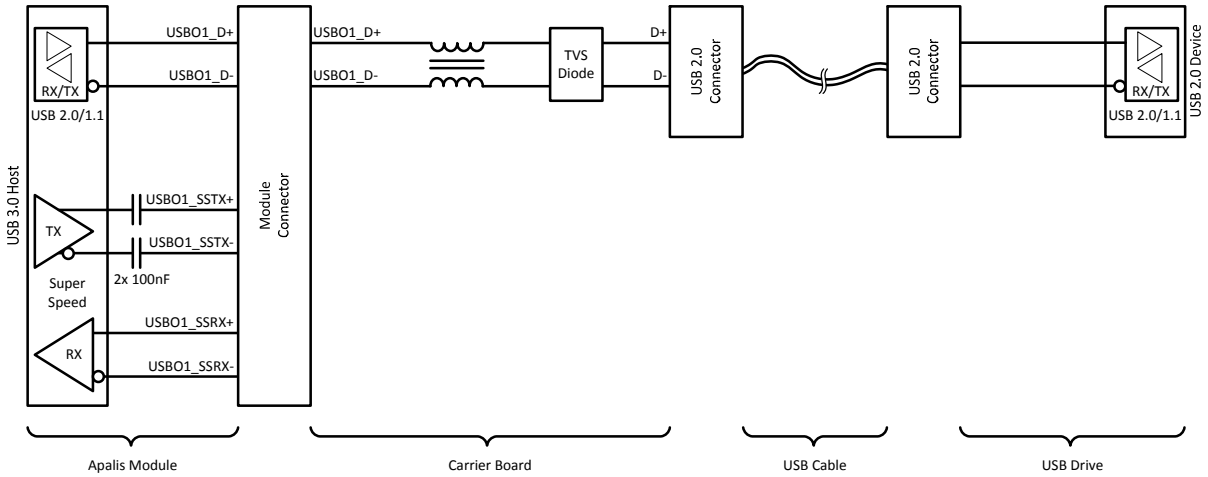


Figure 64: USB 2.0 client block diagram

USBO1_EN, USBO1_OC# and USBO1_ID pins are not used in this configuration. The USBO1_EN pin can be left unconnected. The USBO1_OC# should be pulled up to 3.3V or disabled in software. The USBO1_ID pin needs to be pulled up to 3.3V or the OTG port needs to be configured by software to be client only.

The USBO1_VBUS pin can be connected directly to the USB bus power supply of the USB Type B connector. This signal is needed to indicate to the system that a host is connecter at the other end of the USB cable.

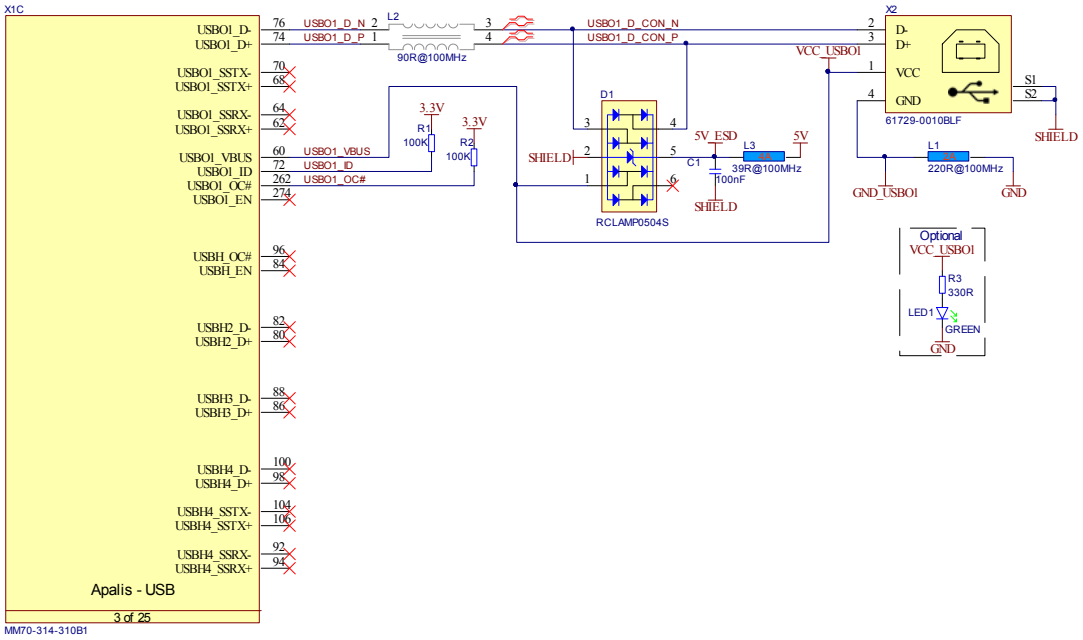


Figure 65: USB 2.0 client reference schematic

3.5.3.3 USB 3.0 Host Connector Schematic Example

The following schematic example shows how to use the USBH4 port as a USB 3.0 host interface. As USB 3.0 is backward compatible, this port could also be used as a USB 2.0 host interface.

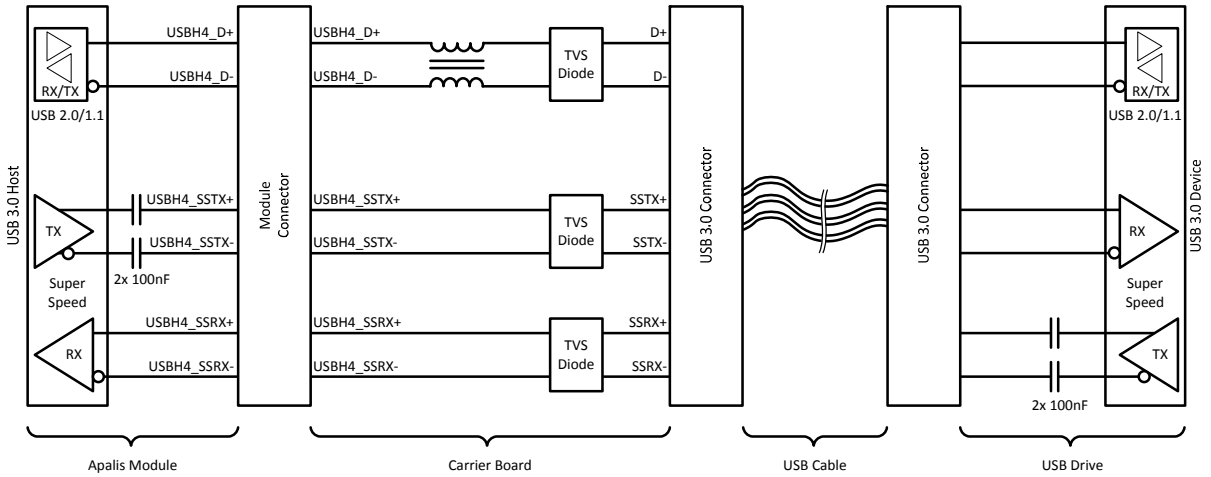


Figure 66: USB 3.0 host block diagram

The power enable signal USBH_EN is shared with the other two host interfaces USBH2 and USBH3. If the USB bus power supply needs to be switched individually for each port, any free pin with GPIO functionality could be used. In this case the USB driver needs to be modified to support such an implementation.

The USBH_OC# signal is shared between all the USB host ports of the Apalis. Since the signal is open drain type, it can be connected directly to the all over current output ports. The signal requires a pull up resistor on the carrier board.

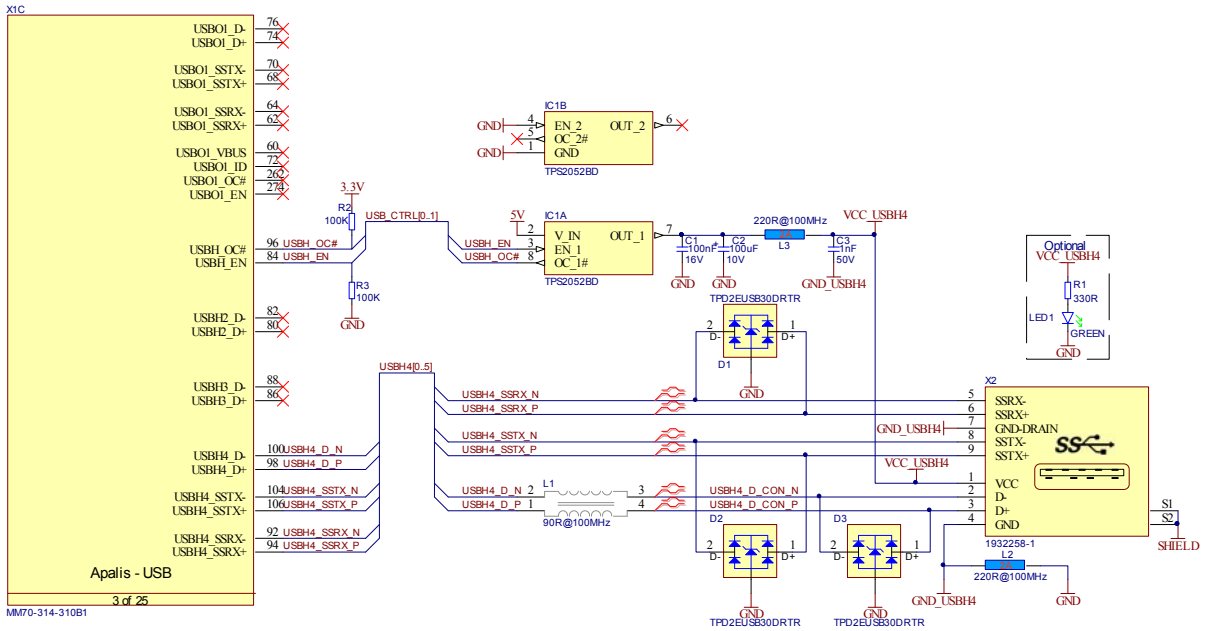


Figure 67: USB 3.0 host reference schematic

3.5.3.4 USB 3.0 Device Down Schematic Example

Device-Down means that the USB device is soldered to the carrier board. The AC coupling capacitors for the Super Speed RX lane (TX from the device) need to be placed on the carrier board. As the capacitors for the TX lane are located on the Apalis module, no additional capacitors are required nor permitted on the TX lines.

No series capacitors should be placed in the USB 2.0 data signal lines. It is recommended that series resistors are added for reducing the slew rate, which will help minimise EMC problems. The value of the series resistor is a trade-off between reducing electromagnetic radiation and signal quality. A good starting value is 22Ω.

ESD protection diodes and common mode chokes are not needed for device-down implementations.

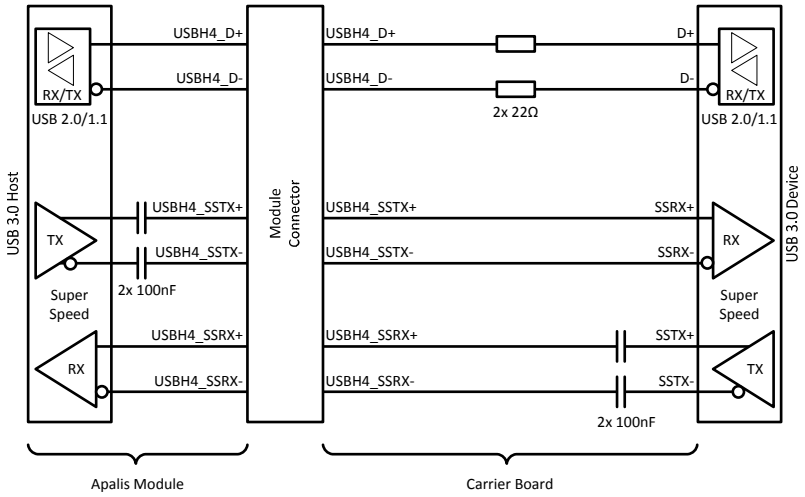


Figure 68: USB 3.0 device down block diagram

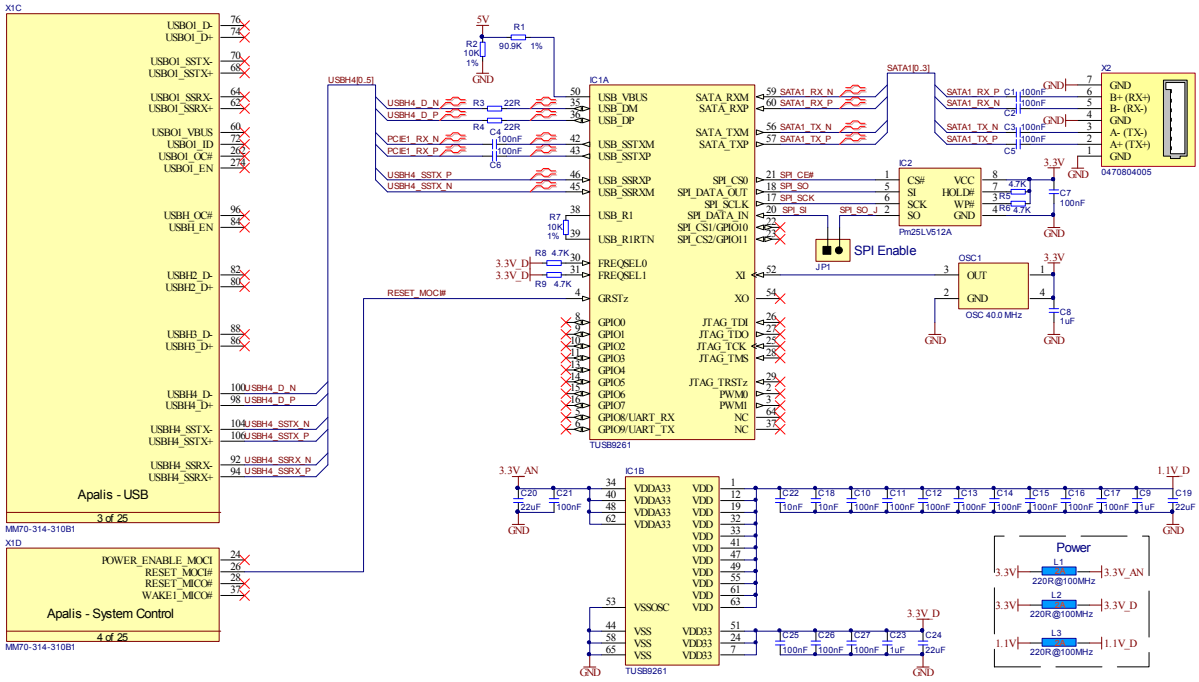


Figure 69: USB 3.0 device down reference schematic

3.5.3.5 USB 2.0 Host Connector Schematic Example

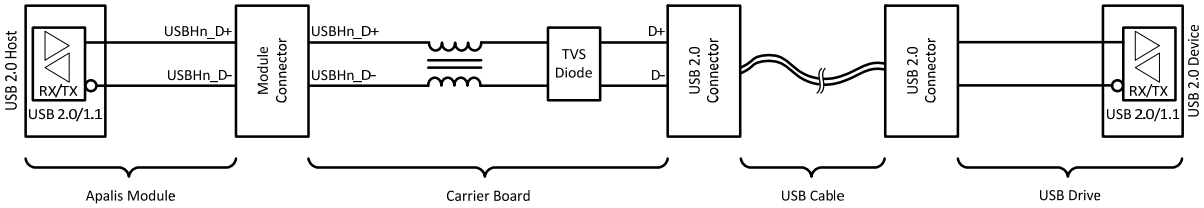


Figure 70: USB 2.0 host block diagram

The power enable signal USBH_EN is shared with the other all three host interfaces USBH2, USBH3 and USBH4. If USB bus power supply needs to be switched individually for each port, any free pin with GPIO functionality could be used to control the USB power rails individually. In this case the USB driver needs to support such an implementation.

The USBH_OC# signal is shared between all the USB host ports of the Apalis. Since the signal is open drain type, it can be connected directly to the all over current output ports. The signal requires a pull up resistor on the carrier board.

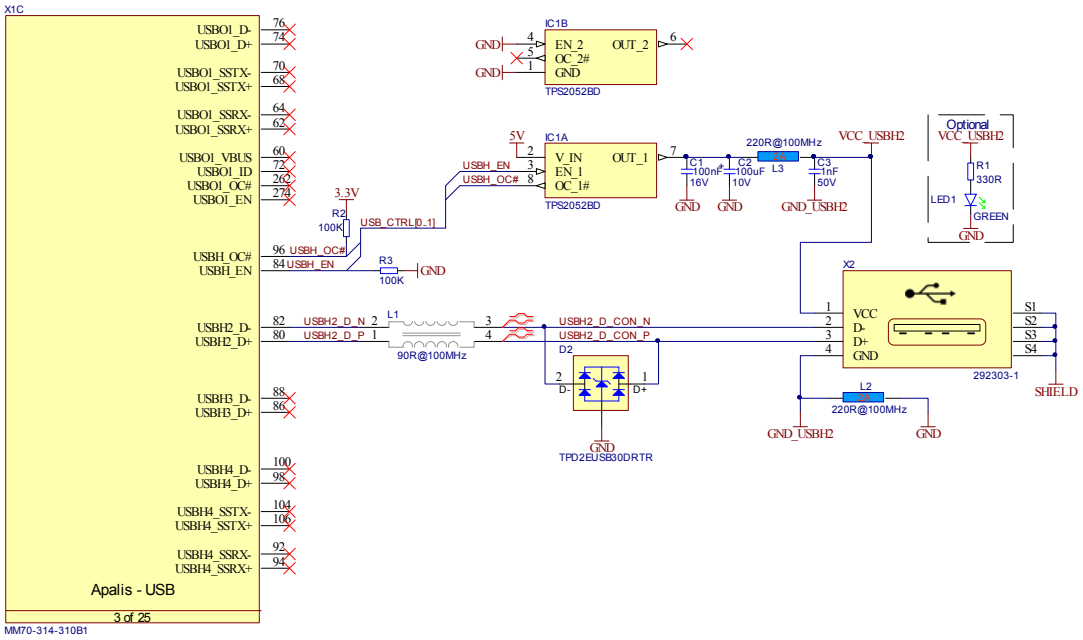


Figure 71: USB 2.0 host reference schematic

3.5.4 Unused USB Signal Termination

Apalis Pin	Apalis Signal Name	Recommended Termination
74	USBO1_D+	Leave NC if not used
76	USBO1_D-	Leave NC if not used
62	USBO1_SSRX+	Leave NC if not used
64	USBO1_SSRX-	Leave NC if not used
68	USBO1_SSTX+	Leave NC if not used
70	USBO1_SSTX-	Leave NC if not used
80	USBH2_D+	Leave NC if not used
82	USBH2_D-	Leave NC if not used
86	USBH3_D+	Leave NC if not used
88	USBH3_D-	Leave NC if not used
98	USBH4_D+	Leave NC if not used
100	USBH4_D-	Leave NC if not used
94	USB H4_SSRX+	Leave NC if not used
92	USB H4_SSRX-	Leave NC if not used
106	USBH4_SSTX+	Leave NC if not used
104	USB H4_SSTX-	Leave NC if not used
72	USBO1_ID	Leave NC and set the USB port direction in software to host or client or ground the pin if port is used permanently as host or add pull up resistor if port is used as slave.
60	USBO1_VBUS	Leave NC if not used
274	USBO1_EN	Leave NC if not used
262	USBO1_OC#	Add pull up resistor or disable the overcurrent function in software
84	USBH_EN	Leave NC if not used
96	USBH_OC#	Add pull up resistor or disable the overcurrent function in software

Table 21: Unused USB signal termination

3.6 Parallel RGB LCD Interface

3.6.1 Parallel RGB LCD Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
251	LCD1_R0	O	CMOS	3.3V	Red LCD data signals (LSB: 0, MSB: 7)
253	LCD1_R1	O	CMOS	3.3V	
255	LCD1_R2	O	CMOS	3.3V	
257	LCD1_R3	O	CMOS	3.3V	
259	LCD1_R4	O	CMOS	3.3V	
261	LCD1_R5	O	CMOS	3.3V	
263	LCD1_R6	O	CMOS	3.3V	
265	LCD1_R7	O	CMOS	3.3V	
269	LCD1_G0	O	CMOS	3.3V	Green LCD data signals (LSB: 0, MSB: 7)
271	LCD1_G1	O	CMOS	3.3V	
273	LCD1_G2	O	CMOS	3.3V	
275	LCD1_G3	O	CMOS	3.3V	
277	LCD1_G4	O	CMOS	3.3V	
279	LCD1_G5	O	CMOS	3.3V	
281	LCD1_G6	O	CMOS	3.3V	
283	LCD1_G7	O	CMOS	3.3V	
287	LCD1_B0	O	CMOS	3.3V	Blue LCD data signals (LSB: 0, MSB: 7)
289	LCD1_B1	O	CMOS	3.3V	
291	LCD1_B2	O	CMOS	3.3V	
293	LCD1_B3	O	CMOS	3.3V	
295	LCD1_B4	O	CMOS	3.3V	
297	LCD1_B5	O	CMOS	3.3V	
299	LCD1_B6	O	CMOS	3.3V	
301	LCD1_B7	O	CMOS	3.3V	
249	LCD1_DE	O	CMOS	3.3V	Data Enable (other names: Output Enable)
243	LCD1_PCLK	O	CMOS	3.3V	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
247	LCD1_HSYNC	O	CMOS	3.3V	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
245	LCD1_VSYNC	O	CMOS	3.3V	Vertical Sync (other names: Frame Clock, L_FCLK)
239	BKL1_PWM	O	CMOS	3.3V	Backlight PWM, can be used to control the brightness of the LCD backlight
286	BKL1_ON	O	CMOS	3.3V	Backlight enable signal
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface that might be used for the extended display identification data (EDID) or as DDC if a converter to VGA or DVI is added. This interface is shared with the other display interfaces.
207	I2C2_SCL	O	OD	3.3V	

Table 22: Parallel RGB LCD signals

3.6.2 Colour Mapping

The 24bit colour mapping is guaranteed to be compatible with other Apalis modules. R7, G7 and B7 are the most significant bits (MSBs) and R0, G0 and B0 are the least significant bits (LSBs) for the respective colours. To use displays which require fewer bits (e.g. 18 or 16 bit displays), simply do not connect the bottom n LSBs for each colour, where n is the number of signals that are not required for a specific colour. For instance, to connect an 18 bit display, R0, R1, G0, G1 B0 and B1 will remain unused, and R2, G2 and B2 become the LSBs for this configuration.

In order to ensure compatibility between different Apalis modules, it is recommended that 18 or 16 bit displays are attached to the 24bit mapped interface according to the following table:

Apalis Pin	Apalis Signal Name	24 bit RGB	18 bit RGB	16 bit RGB
251	LCD1_R0	R0		
253	LCD1_R1	R1		
255	LCD1_R2	R2	R0	
257	LCD1_R3	R3	R1	R0
259	LCD1_R4	R4	R2	R1
261	LCD1_R5	R5	R3	R2
263	LCD1_R6	R6	R4	R3
265	LCD1_R7	R7	R5	R4
269	LCD1_G0	G0		
271	LCD1_G1	G1		
273	LCD1_G2	G2	G0	G0
275	LCD1_G3	G3	G1	G1
277	LCD1_G4	G4	G2	G2
279	LCD1_G5	G5	G3	G3
281	LCD1_G6	G6	G4	G4
283	LCD1_G7	G7	G5	G5
287	LCD1_B0	B0		
289	LCD1_B1	B1		
291	LCD1_B2	B2	B0	
293	LCD1_B3	B3	B1	B0
295	LCD1_B4	B4	B2	B1
297	LCD1_B5	B5	B3	B2
299	LCD1_B6	B6	B4	B3
301	LCD1_B7	B7	B5	B4

Table 23: Parallel RGB LCD signals

3.6.3 Layout Requirements

The layout requirements depend on the pixel clock and therefore on the required display resolution. The requirements below can be greatly relaxed if lower resolutions such as VGA 640x480 are used. The maximum length restrictions are defined due to electromagnetic radiation problems associated with the parallel interface. From the timing perspective, the trace length of the interface is not limited.

Parameter	Requirement
Max Frequency	Depending on maximum resolution of the module (e.g. 162MHz for VESA 1600x1200@60Hz). Check the datasheet of the Apalis module.
Configuration /Device Organisation	1 load (multiple load possible for lower resolutions)
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	50Ω ±15% single ended
Max skew between data signal and clock	<100ps ≈15mm, depends on pixel clock, requirement can be relaxed for lower resolution displays
Max trace length (RGB displays, including flex cable length)	<100mm (only recommended for low resolution displays)
Max trace length (converter on carrier board)	<50mm

Table 24: Parallel RGB LCD Interface Layout Requirements

3.6.4 Reference Schematics

3.6.4.1 24bit Display Schematic Example

The parallel RGB interface is can cause problems with EMC compliance when used with a high pixel clock frequency. This can be made worse if a display is connected over flat flex cables. Therefore, the flat flex cables should be kept as short as possible. Series resistors in the data lines reduce the slew rate of the signals which reduces the radiation problem but can introduce signal quality and timing problems. The serial resistor value is a trade-off between reduction of electromagnetic radiation and signal quality. A good starting value is 22Ω.

Some displays feature an I²C interface for reading out the EDID PROM or additional controls such as contrast and hue. If the carrier board provides no other display interface with DDC, it is recommended that the I2C2 on the Apalis module be used for the DDC. If the DDC is used, make sure that I²C device(s) on the RGB display do not interfere with the DDC address 50h. Otherwise, use a different I²C interface on the Apalis module. The I²C interfaces on the Apalis module are 3.3V logic level. If the display requires a 5V interface, add an I²C logic level shifter.

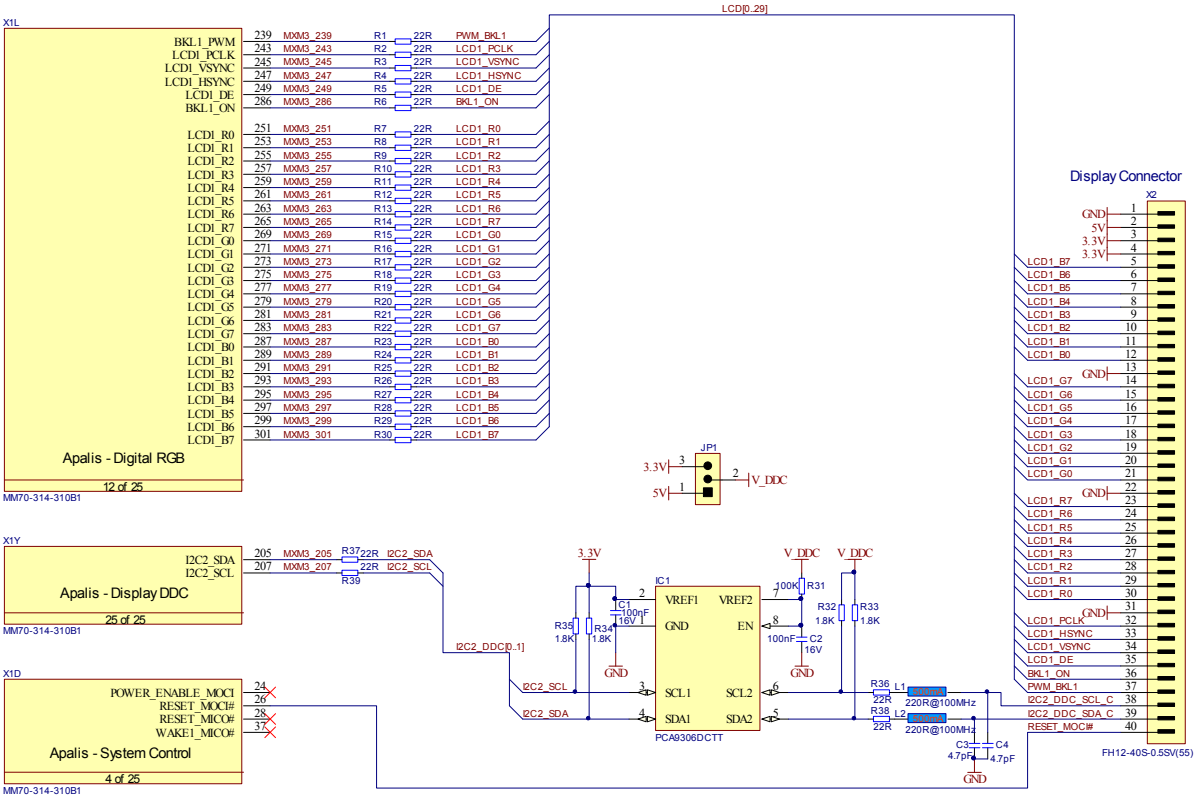


Figure 72: 24bit parallel RGB display reference schematic

3.6.4.2 VGA DAC Schematic Example

The Apalis standard features a dedicated VGA interface. Nevertheless, it is possible to add a parallel RGB to VGA converter if an additional VGA interface is needed or a specific Apalis module does not feature VGA output at the VGA pins. For additional information about availability of the dedicated VGA interface and whether it is independent from the parallel RGB interface, please consult the applicable Apalis module datasheet.

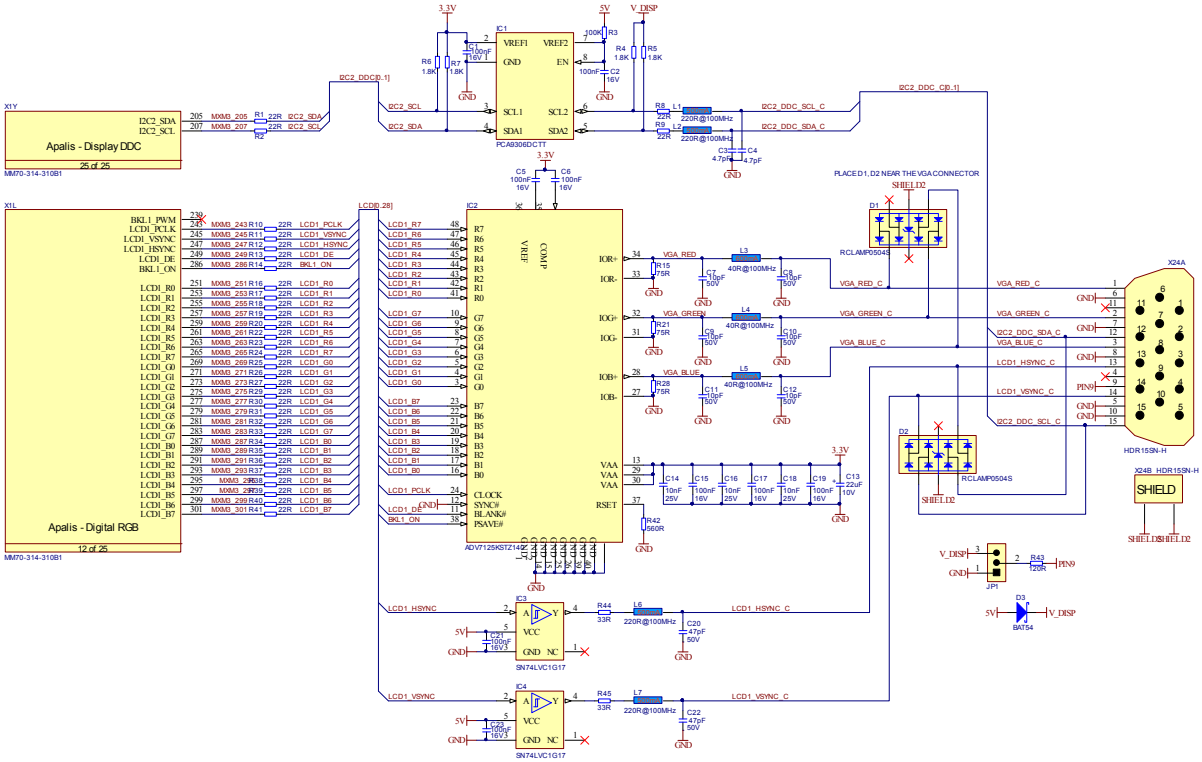


Figure 73: VGA DAC reference schematic

3.6.4.3 LVDS Transmitter Schematic Example

As EMC compliance when using the parallel RGB interface can be problematic, it is recommended to attach liquid crystal displays with high resolutions using an LVDS interface. LVDS also reduces problems with long cables. The Apalis standard features a dedicated LVDS LCD interface. If the provided LVDS interface is incompatible with the display or an additional interface is needed, a parallel RGB to LVDS transmitter can be placed on the carrier board. Please consult the Apalis module to determine whether the dedicated LVDS interface is independent from the parallel RGB interface.

As there are different LVDS colour mappings available, check with your display vendor how the RGB signals need to be connected to the transmitter.

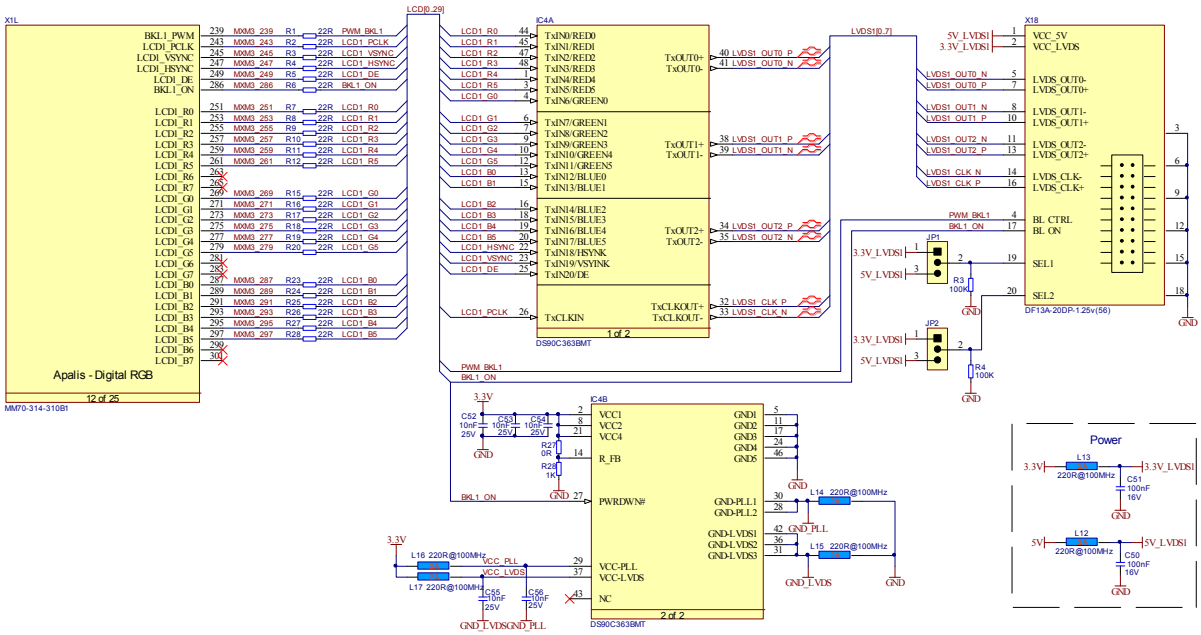


Figure 74: LVDS transmitter reference schematic

3.6.5 Unused Parallel RGB Interface Signal Termination

All unused parallel RGB interface signals can be left unconnected. Some Apalis modules might use the parallel RGB interface internally for providing an LVDS or VGA interface via a transmitter or DAC. If such a video interface is used, the unused parallel RGB interface cannot be configured for alternative functions (e.g. GPIO). Please check the Apalis module datasheet for more information about GPIO capability and any usage restrictions for the parallel RGB interface.

3.7 LVDS LCD Interface

The Apalis module standard provides an LVDS interface with up to two channel and 24bit for displays. The interface is officially called FPD-Link or FlatLink. Please carefully study datasheets for individual Apalis modules for information regarding dual or single channel, 18 or 24bit colour depth and colour mapping support.

3.7.1 LVDS Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
246	LVDS1_A_CLK-	O	LVDS		LVDS Clock out for channel A (odd pixels/single channel)
248	LVDS1_A_CLK+	O	LVDS		
252	LVDS1_A_TX0-	O	LVDS		LVDS data lane 0 for channel A (odd pixels/single channel)
254	LVDS1_A_TX0+	O	LVDS		
258	LVDS1_A_TX1-	O	LVDS		LVDS data lane 1 for channel A (odd pixels/single channel)
260	LVDS1_A_TX1+	O	LVDS		
264	LVDS1_A_TX2-	O	LVDS		LVDS data lane 2 for channel A (odd pixels/single channel)
266	LVDS1_A_TX2+	O	LVDS		
270	LVDS1_A_TX3-	O	LVDS		LVDS data lane 3 for channel A (odd pixels/single channel; unused for 18bit)
272	LVDS1_A_TX3+	O	LVDS		
276	LVDS1_B_CLK-	O	LVDS		LVDS Clock out for channel B (even pixels/unused for single channel)
278	LVDS1_B_CLK+	O	LVDS		
282	LVDS1_B_TX0-	O	LVDS		LVDS data lane 0 for channel B (odd pixels/unused for single channel)
284	LVDS1_B_TX0+	O	LVDS		

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
288	LVDS1_B_TX1-	O	LVDS		LVDS data lane 1 for channel B (odd pixels/unused for single channel)
290	LVDS1_B_TX1+	O	LVDS		
294	LVDS1_B_TX2-	O	LVDS		LVDS data lane 2 for channel B (odd pixels/unused for single channel)
296	LVDS1_B_TX2+	O	LVDS		
300	LVDS1_B_TX3-	O	LVDS		LVDS data lane 3 for channel B (odd pixels/unused for single channel; unused for 18bit)
302	LVDS1_B_TX3+	O	LVDS		
239	BKL1_PWM	O	CMOS	3.3V	Backlight PWM, can be used to control the brightness of the LCD backlight
286	BKL1_ON	O	CMOS	3.3V	Backlight enable signal
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface that might be used for the extended display identification data (EDID) or as DDC if a converter to VGA or DVI is added. This interface is shared with the other display interfaces.
207	I2C2_SCL	O	OD	3.3V	

Table 25: LVDS LCD signals

3.7.2 Compatibility between LVDS Configurations

A single channel LVDS interface can provide resolutions up to 1280x1024 pixels (depending on available displays). Displays with higher resolutions require a second LVDS channel. In this case, the odd bits are transmitted in the first channel and the even bits are transmitted in the second channel. Depending on the Apalis module, the LVDS transmitter will provide either single or dual channel signals. Some modules may be more flexible in their ability to configure the output mode of the transmitter. Please consult the applicable Apalis module datasheet for information about supported channel modes. As the following figure shows, it is not possible to connect a single channel display to a dual channel output and vice versa.

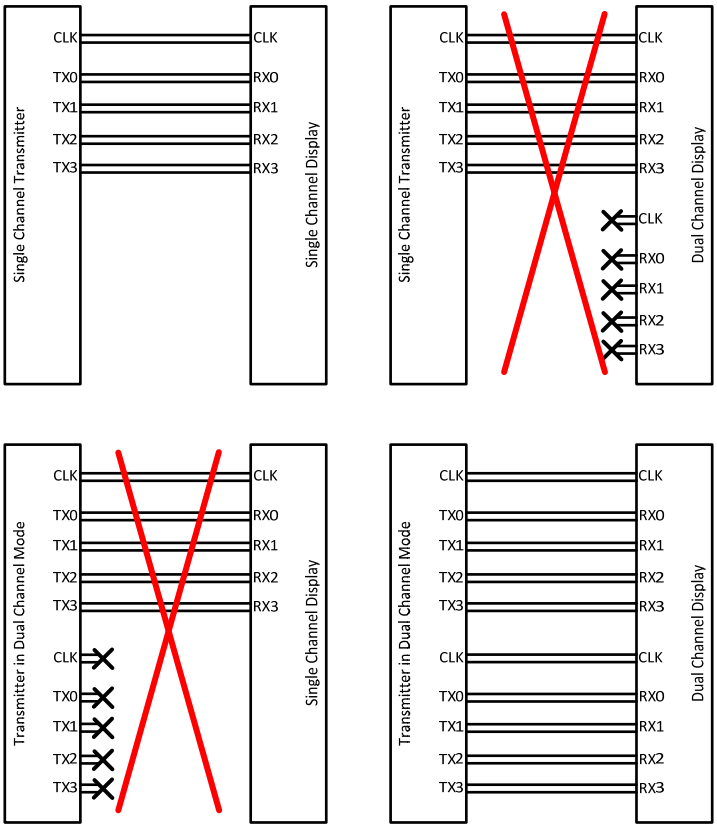


Figure 75: Compatibility between Single and Dual Channel LVDS

For the 24bit LVDS interface, there are two different colour mappings available; VESA and JEIDA. The following figure shows the compatibility between the 18bit LVDS interface and these colour mappings. When selecting a display, ensure that the Apalis module LVDS interface can be

configured to a compatible colour mapping as some modules may not support all colour mappings.

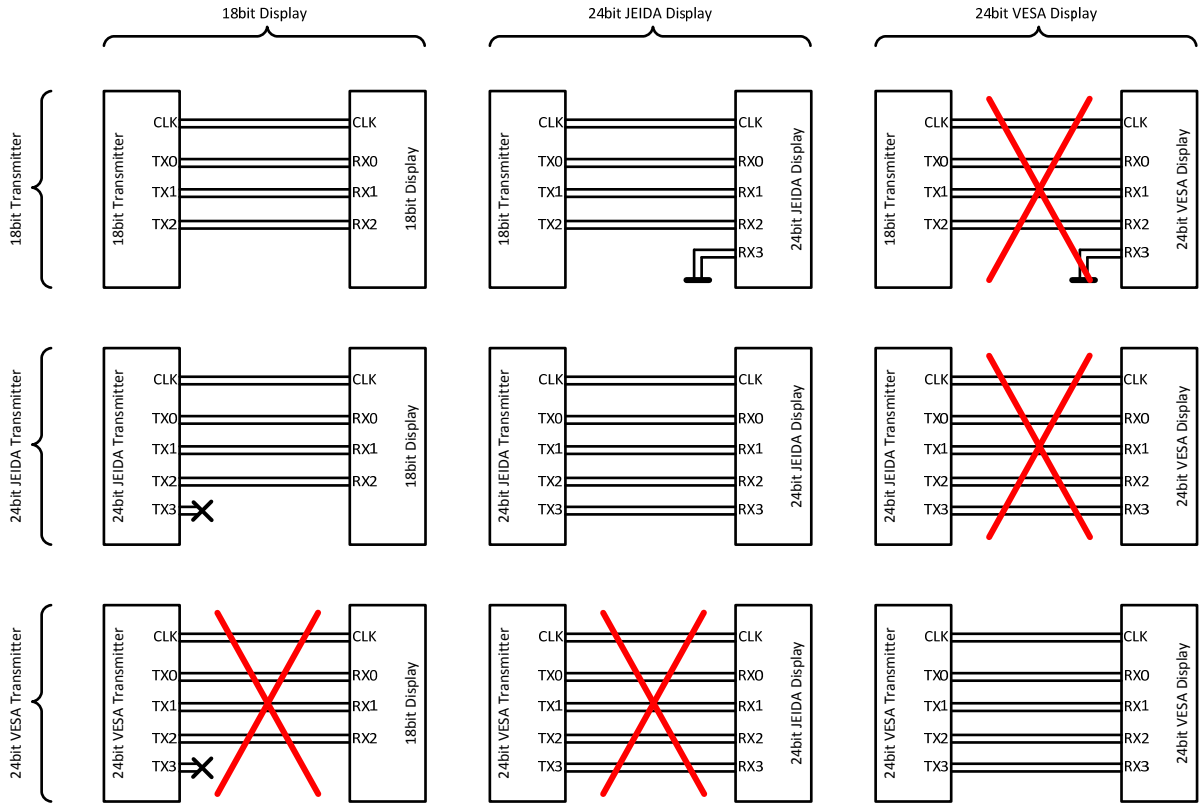


Figure 76: Compatibility between LVDS colour mapping

3.7.2.1 18bit Colour Mapping

The colour mapping for the 18bit LVDS interface is standardized and is shown in the following picture:

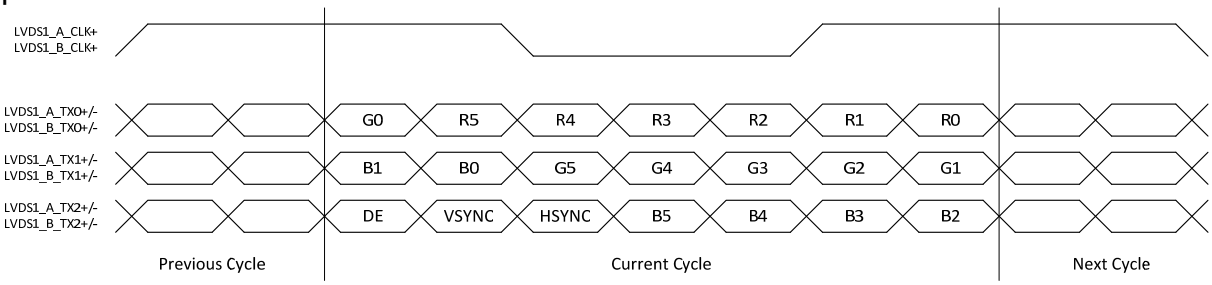


Figure 77: 18bit LVDS Colour Mapping

3.7.2.2 24bit JEIDA Colour Mapping

The JEIDA colour mapping is compatible with the 18bit LVDS interface. Therefore, the mapping is sometimes also called “24bit / 18bit Compatible Colour Mapping”. The signal names of the colour bits are renamed (e.g. the 18bit R5 is renamed to 24bit R7) but the position of the MSB is kept the same. The additional least significant bits R0, R1, G0, G1, B0 and B1 are transmitted in the additional fourth LVDS data pair.

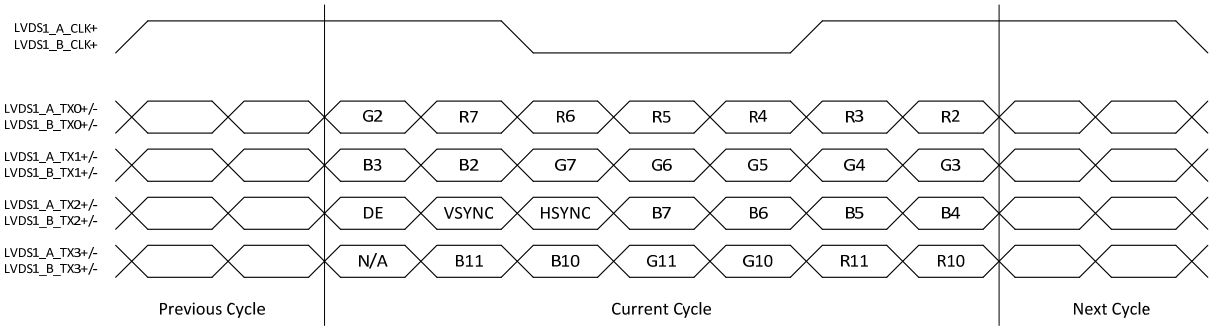


Figure 78: 24bit JEIDA LVDS colour mapping

3.7.2.3 24bit VESA Colour Mapping

Most of the 24bit LVDS displays follow the VESA Colour mapping. The VESA colour mapping does not rename the signal bits. This means that the position of the MSB is different as they are available in the additional data pair. Hence, the VESA colour mapping is not compatible with the 18bit interface.

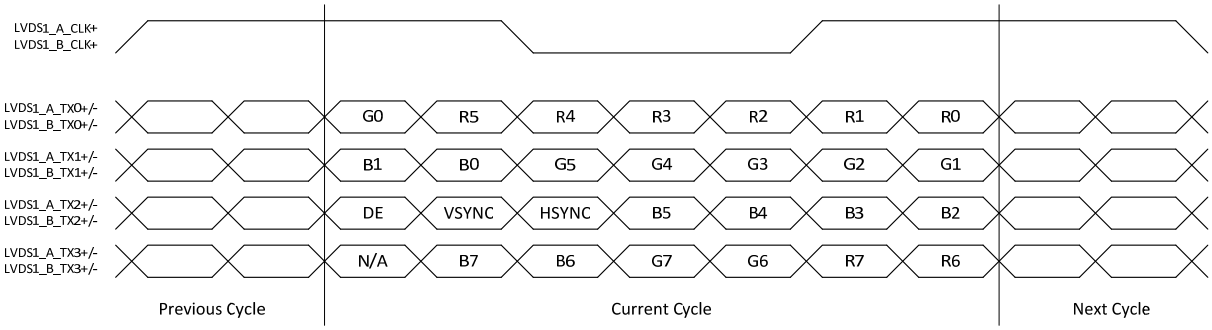


Figure 79: 24bit VESA LVDS colour mapping

3.7.3 Layout Requirements

Parameter	Requirement
Max Frequency	Depending on maximum resolution of the module. The maximum frequency is 7 times higher than the pixel clock in single channel mode.
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	100Ω ±15% differential; 55Ω ±15% single ended
Max intra-pair skew	<1ps ≈150µm
Max trace length skew between clock and data pairs	<3.5ps ≈500µm, depends on LVDS frequency since clock is not embedded, can be relaxed for lower resolutions
Max trace length on carrier board and display cable	<500mm
Minimum pair to pair spacing	>2x intra-pair spacing
Maximum allowed via	Minimize the number of via in LVDS traces

Table 26: LVDS layout requirements

3.7.4 Reference Schematics

Some displays feature an I^2C interface for reading out the EDID PROM or additional controls such as contrast and hue. If the carrier board provides no other display interface with DDC, the I2C2

interface should be used. If the DDC is used, make sure that I²C device(s) on the LVDS display does not interfere with the DDC address 50h. Otherwise, a different I²C interface should be used. The I²C interfaces on the Apalis module are 3.3V logic level. If the display requires a 5V interface, add an I²C logic level shifter.

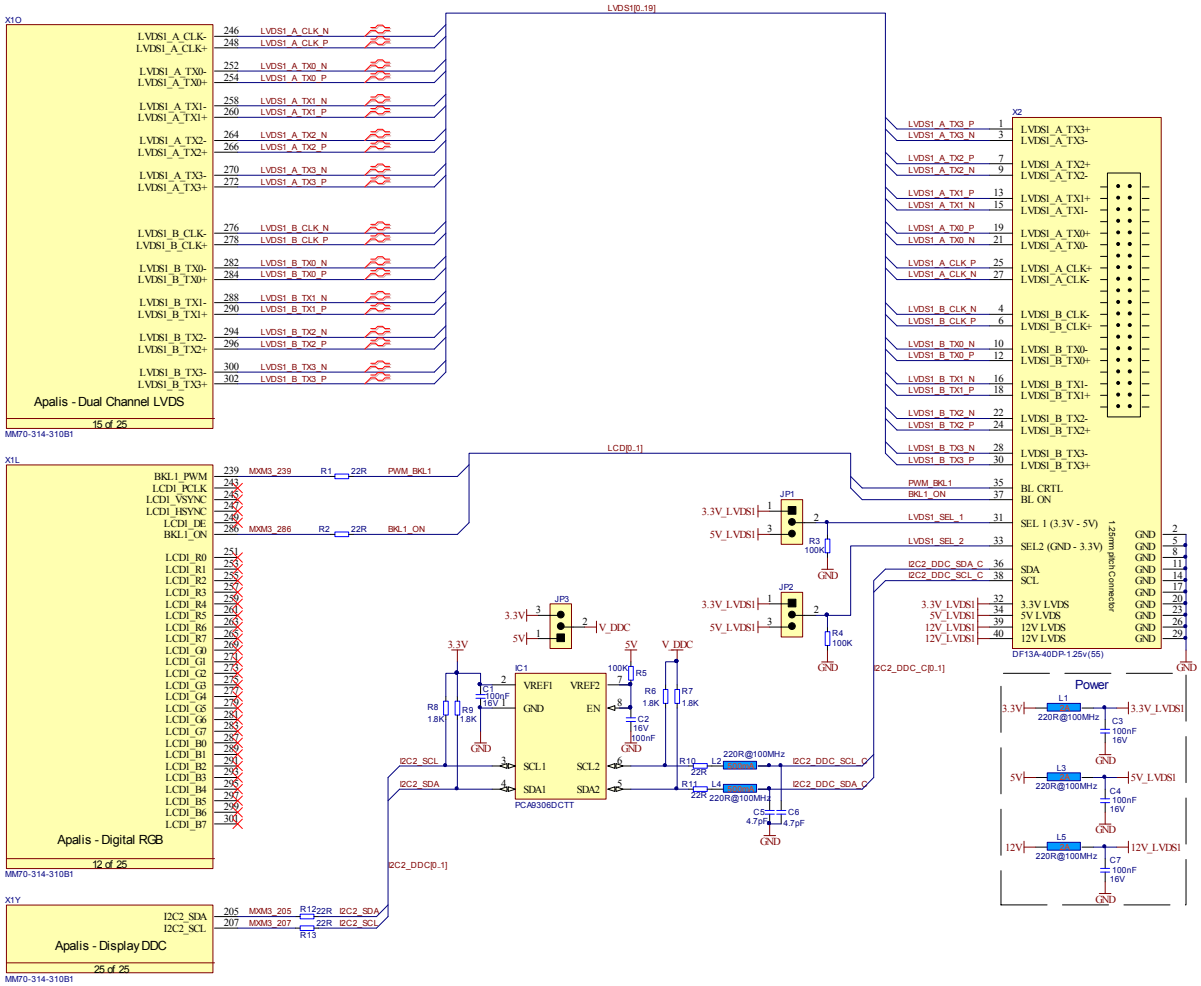


Figure 80: 24bit Dual channel LVDS display reference schematic

3.7.5 Unused LVDS Interface Signal Termination

All unused LVDS interface signals can be left unconnected.

3.8 HDMI/DVI

The HDMI and DVI interface uses a TMDS compatible physical link to transfer video and optional audio data. Electrically, HDMI and DVI are equal, but there can be some differences in the protocol. DVI is the predecessor to HDMI. HDMI specifies the additional transport for audio data and content protection (HDCP). HDMI devices (monitor, television set etc.) can be driven with the DVI interface as HDMI is backward compatible. Compatibility is not guaranteed when attempting to drive a DVI device with an HDMI interface. Some DVI displays accept the HDMI protocol and are HDCP compatible. Please read the datasheet of the Apalis module for more information about the supported HDMI and DVI protocols.

The HDMI and DVI define different connectors. There are passive adapters available in both directions. Please be aware that HDMI and HDCP have licencing restrictions in place.

3.8.1 HDMI/DVI Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
240	HDMI1_TXC+	O	TDMS		HDMI/DVI differential clock positive
242	HDMI1_TXC-	O	TDMS		HDMI/DVI differential clock negative
234	HDMI1_TXD0+	O	TDMS		HDMI/DVI differential data lane 0 positive
236	HDMI1_TXD0-	O	TDMS		HDMI/DVI differential data lane 0 negative
228	HDMI1_TXD1+	O	TDMS		HDMI/DVI differential data lane 1 positive
230	HDMI1_TXD1-	O	TDMS		HDMI/DVI differential data lane 1 negative
222	HDMI1_TXD2+	O	TDMS		HDMI/DVI differential data lane 2 positive
224	HDMI1_TXD2-	O	TDMS		HDMI/DVI differential data lane 2 negative
220	HDMI1_CEC	I/O	OD	3.3V	HDMI consumer electronic control
232	HDMI1_HPD	I	CMOS	3.3V	Hot plug detect
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface for reading the extended display identification data (EDID) over DDC. This interface is shared with other display interfaces
207	I2C2_SCL	O	OD	3.3V	

Table 27: HDMI/DVI signals

3.8.2 Layout Requirements

Parameter	Requirement
Max Frequency	Version 1.0-1.2a: 825MHz (165 MHz pixel clock) Version 1.3-1.4: 1.65GHz (340 MHz pixel clock)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max intra-pair skew	<5ps ≈750µm
Max trace length skew between clock and data pairs	<150ps ≈22mm
Max trace length on carrier board	<250mm
Minimum pair to pair spacing	>500µm
Maximum allowed via	Minimize the number of via in TDMS traces

Table 28: TDMS signal layout requirements

3.8.3 Reference Schematics

3.8.3.1 DVI Schematic Example

There are different DVI connector configurations available. The DVI-D (digital) supports only the native DVI signals. The DVI-A (analogue) provides only analogue VGA signals. The DVI-I (integrated) combines the digital DVI signals and the analogue VGA signals. For the DVI-A and DVI-I, there are passive adapters to the D-SUB VGA connector available. There is only one DDC channel available on the DVI-I interface. Therefore, the connector is not designed to use both links (DVI and VGA) simultaneously. Nevertheless, there are Y-cables available which provide a DVI and VGA output. Such cables are not standardized normally provide the DDC on either DVI or VGA output. Please be aware of this when using such a Y-cable.

The following schematic example shows a DVI-I implementation. It can be used as an example for a DVI-D design; simply remove the analogue VGA signals. The sync signals for the VGA signals need to be level shifted from 3.3V to 5V. The same is necessary for the DDC signals. The TDMS

signals need to be ESD protected using diodes. The schematic example shows a discrete solution for the level shifting and protection. There are also integrated solutions available.

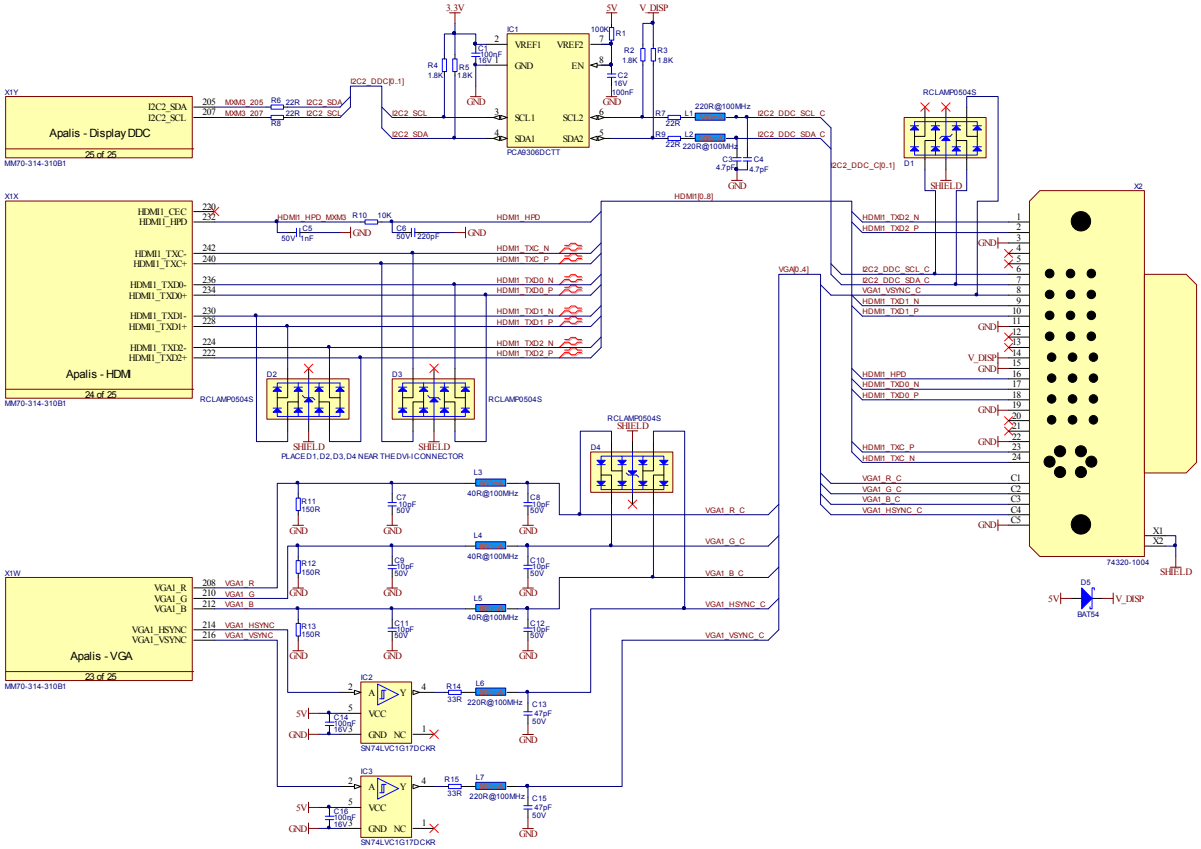


Figure 81: DVI-I reference schematic

3.8.3.2 HDMI Schematic Example

The HDMI connector does not feature an Analogue VGA interface, but there is an optional Consumer Electronics Control (CEC) interface available. This one wire interface is used to control consumer audio and video devices such as television set or AV receivers. There are many different trade names for CEC known. (VIERA Link, Anynet+, EasyLink, Aquos Link, BRAVIA Link etc.). The CEC is a 3.3V interface. Nevertheless, it is recommended that a level shifter is added. This eliminates problems with displays that may pull up the signals to other voltage levels.

The I^2C signals for the DDC and the hot plug detection (HPD) need to be shifted to/from the 5V logic level of the HDMI interface to the Apalis module signal level of 3.3V. The DDC requires external pull up resistors on the module. The HPD has a 100kΩ pull down resistor already on the baseboard. Since the HPD and CEC signals are used as references for the TDMS signals on the module connector, it is recommended that 1nF stitching capacitors are added to the HPD and 100pF stitching capacitors to the CEC signal, close to the module connector.

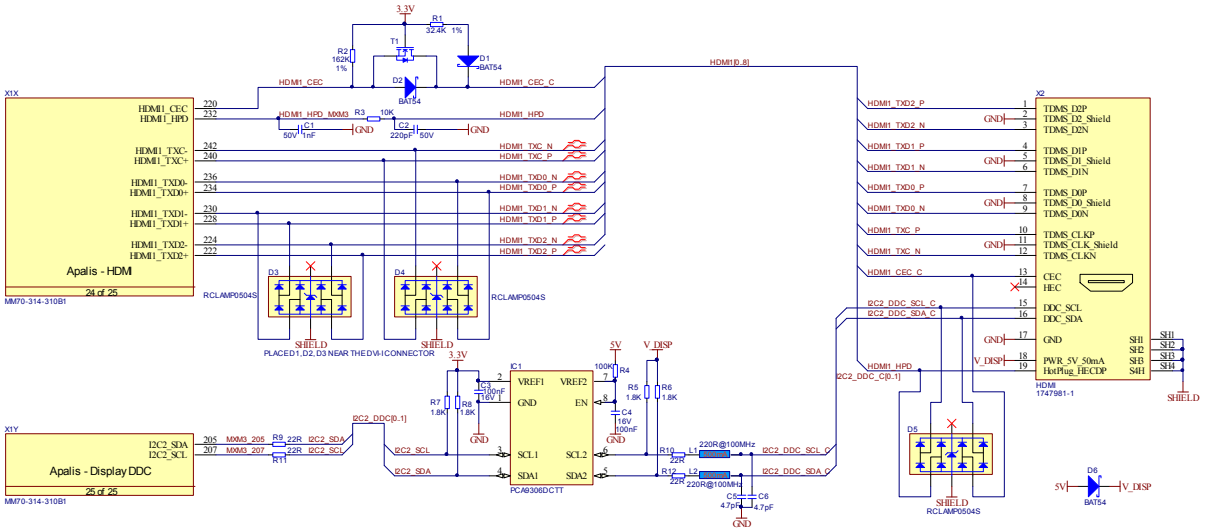


Figure 82: HDMI reference schematic

3.8.4 Unused HDMI/DVI Signal Termination

All unused HDMI/DVI signals can be left unconnected. The HPD has a 100kΩ pull down resistor on the module.

Apalis Pin	Apalis Signal Name	Recommended Termination
240	HDMI1_TXC+	Leave NC if not used
242	HDMI1_TXC-	Leave NC if not used
234	HDMI1_TXD0+	Leave NC if not used
236	HDMI1_TXD0-	Leave NC if not used
228	HDMI1_TXD1+	Leave NC if not used
230	HDMI1_TXD1-	Leave NC if not used
222	HDMI1_TXD2+	Leave NC if not used
224	HDMI1_TXD2-	Leave NC if not used
220	HDMI1_CEC	Add pull up resistor or disable the CEC function in software
232	HDMI1_HPD	Leave NC if not used, 100kΩ resistor on Apalis module
205	I2C2_SDA	Add pull up resistor or disable the I^2C function in software
207	I2C2_SCL	Add pull up resistor or disable the I^2C function in software

Table 29: Unused HDMI/DVI signal termination

3.9 Analogue VGA

3.9.1 VGA Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
208	VGA1_R	O	Analogue		Analogue red video (0 to 0.7V)
210	VGA1_G	O	Analogue		Analogue green video (0 to 0.7V)
212	VGA1_B	O	Analogue		Analogue blue video (0 to 0.7V)
214	VGA1_HSYNC	O	CMOS	3.3V	Horizontal sync
216	VGA1_VSYNC	O	CMOS	3.3V	Vertical sync
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface for reading the extended display identification data (EDID) over DDC. This interface is shared with other display interfaces
207	I2C2_SCL	O	OD	3.3V	

Table 30: VGA signals

3.9.2 Layout Requirements

Parameter	Requirement
Max Frequency	Depending on resolution, up to 388MHz for 2048x1536@85Hz
Configuration /Device Organisation	1 load
Reference Plane	AGND or GND (if GND is used, do not cross with digital signals the reference plane)
Trace Impedance	50Ω ±15% in section B 75Ω ±15% in section C (if 75Ω is not achievable, use 50Ω and keep traces short)
Max skew between analogue RGB colour signal	Try to match the trace length as close as possible
Max trace length on carrier board section B	<200mm (longer distances achievable when layout is carefully done)
Max trace length on carrier board section C	<15mm (try to keep section C as short as possible)
Minimum spacing between colour signals	>350µm
Minimum spacing between colour signals and other signals	>500µm from low speed signals >1.25mm from clock signals and high current power traces >6mm from areas with high switching currents (e.g. voltage regulators)
Maximum allowed via	Minimize the number of via in the analogue RGB traces

Table 31: Analogue VGA signal layout requirements

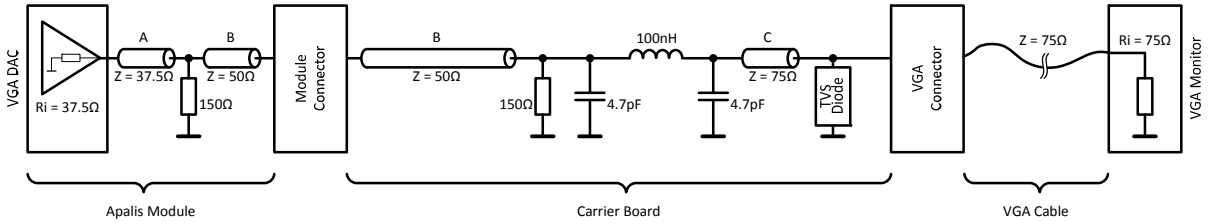


Figure 83: VGA signal trace impedance sections

3.9.3 Reference Schematics

The horizontal and vertical sync signals need to be level shifted on the baseboard. The same is true for the DDC I^2C signals. In the VGA connector standard, the carrier board needs to provide 5V power supply for the EDID memory on the DDC. This allows the system to read out the EDID information of an attached display even if it is not powered. Unfortunately, some displays source the 5V internally and also provide internal pull up resistors to the I^2C lines. This can cause back feeding problems. Therefore we recommend connecting the display and pull up resistor 5V supply over a diode to the module supply.

It is mandatory to place a 150Ω resistor to ground on every analogue RGB signal. Place this resistor as close to the VGA connector as possible. Before this resistor, the signal trace can be routed with 50Ω impedance. After the resistor, the signal should be routed with 75Ω impedance. Depending on the layer stack up, 75Ω traces cannot be reached due to the width getting too small. In this case, lower traces impedance (e.g. 50Ω) can be used but the trace length should be kept short.

All signals on the VGA D-SUB connector need to be ESD protected. TSR diodes can be used. It is recommended that a PI-filter is added to the analogue RGB signals. The values for the capacitors and inductors depend on the maximum required display resolution. The PI-filter reduces EMI problems, but also limits the maximum bandwidth of the VGA signal.

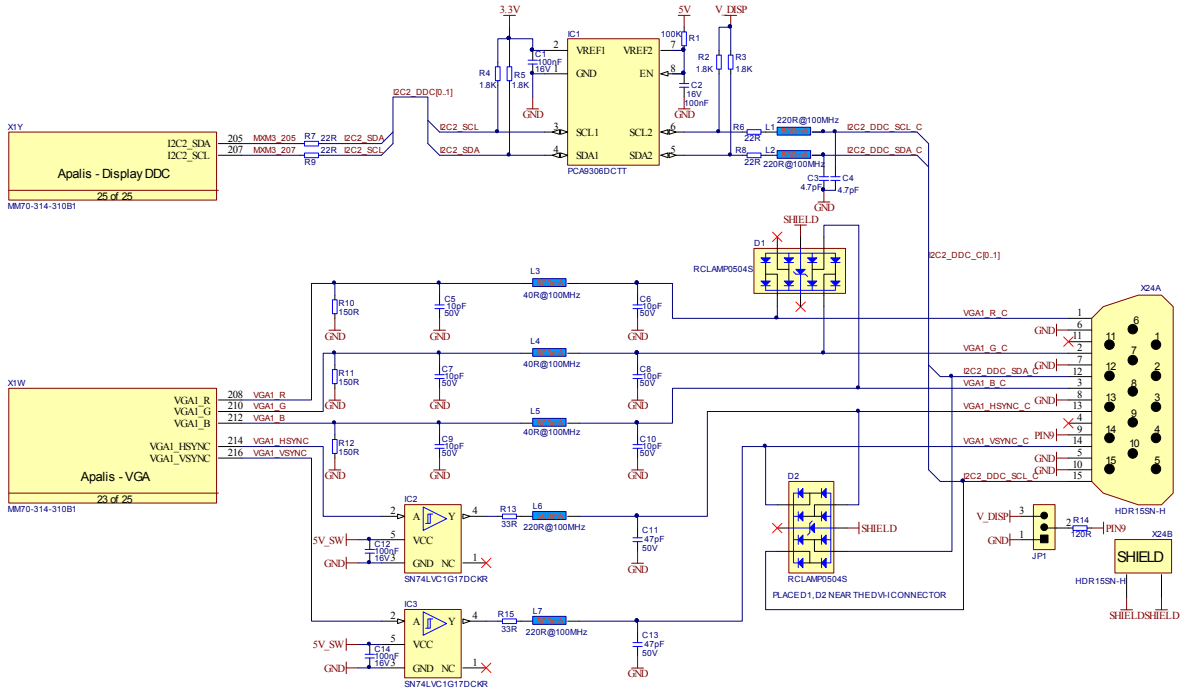


Figure 84: VGA reference schematic

3.9.4 Unused VGA Interface Signal Termination

All unused VGA interface signals can be left unconnected.

3.10 Parallel Camera Interface

The Apalis module standard features an 8 bit YUV parallel camera interface as a standard interface. Depending on the module, there are maybe additional bits available in the type specific area. Only the 8 bit YUV interface is guaranteed to be compatible between Apalis modules. Consult the Apalis datasheets for more information regarding the additional available input modes (e. g. Bayer, RGB etc.).

3.10.1 Parallel Camera Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
187	CAM1_D0	I	CMOS	3.3V	Video input pixel data
185	CAM1_D1	I	CMOS	3.3V	
183	CAM1_D2	I	CMOS	3.3V	
181	CAM1_D3	I	CMOS	3.3V	
179	CAM1_D4	I	CMOS	3.3V	
177	CAM1_D5	I	CMOS	3.3V	
175	CAM1_D6	I	CMOS	3.3V	
173	CAM1_D7	I	CMOS	3.3V	
191	CAM1_PCLK	I	CMOS	3.3V	Video input pixel clock
195	CAM1_VSYNC	I	CMOS	3.3V	Video input vertical sync
197	CAM1_HSYNC	I	CMOS	3.3V	Video input horizontal sync
193	CAM1_MCLK	O	CMOS	3.3V	Master clock output for the camera. Some Camera might do not need this clock since they use other clock sources
201	I2C3_SDA	I/O	OD	3.3V	Camera I^2C interface, might be needed for autofocus unit
203	I2C3_SCL	O	OD	3.3V	

Table 32: Parallel Camera Signals

3.10.2 Layout Requirements

The requirements for the layout depends on the pixel clock and therefore on the required camera resolution and frame rate. The requirements below can be relaxed if lower resolutions such as VGA 640x480@30Hz are used. The maximum length restriction is given due to EMC compliance problems which otherwise may occur. From the timing perspective, the trace length of the interface is not limited.

Parameter	Requirement
Max Frequency	Depending on maximum resolution of the camera and the frame rate.
Configuration /Device Organisation	1 source
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	50Ω ±15% single ended
Max skew between data signal and clock	<100ps ≈15mm, depends on pixel clock, requirement can be relaxed for lower resolution displays
Max trace length	<50mm

Table 33: Parallel Camera Interface Layout Requirements

3.10.3 Unused Parallel Camera Interface Signal Termination

All unused parallel camera input signals can be left unconnected if the interface is disabled in software. These signals may be able to be used as GPIOs when they are not used as camera interface. Please consult the applicable Apalis module datasheet.

3.11 SD/MMC/SDIO

The Apalis module form factor features two SDIO interfaces as standard interface. One of these interfaces can provide up to 8 data bit which can be used for interfacing MMCplus and eMMC memory. The 8bit interface is backward compatible with the 4bit data bus and can be used for SD, SDIO and MMC devices. The SD and SDIO interface can only make use of the 4bit wide data bus, as there is no 8bit SD interface defined.

3.11.1 SD/MMC/SDIO Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
160	MMC1_D0	I/O	CMOS	3.3V	Data signals [3:0], used for SD, MMC and SDIO interfaces, add external pull up resistors
162	MMC1_D1	I/O	CMOS	3.3V	
144	MMC1_D2	I/O	CMOS	3.3V	
146	MMC1_D3	I/O	CMOS	3.3V	
148	MMC1_D4	I/O	CMOS	3.3V	Data signals [7:0], only needed for 8bit MMC interface, add external pull up resistors, for 4bit MMC, SD and SDIO, leave this pins unconnected
152	MMC1_D5	I/O	CMOS	3.3V	
156	MMC1_D6	I/O	CMOS	3.3V	
158	MMC1_D7	I/O	CMOS	3.3V	
150	MMC1_CMD	I/O	CMOS	3.3V	Command signal, add external pull up resistor
154	MMC1_CLK	O	CMOS	3.3V	Clock output
164	MMC1_CD#	I	CMOS	3.3V	Card detect, add pull up resistor if card detect is used

Table 34: 8bit SD/MMC/SDIO signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
186	SD1_D0	I/O	CMOS	3.3V	Data signals [3:0], used for SD, MMC and SDIO interfaces, add external pull up resistors
188	SD1_D1	I/O	CMOS	3.3V	
176	SD1_D2	I/O	CMOS	3.3V	
178	SD1_D3	I/O	CMOS	3.3V	
180	SD1_CMD	I/O	CMOS	3.3V	Command signal, add external pull up resistor
184	SD1_CLK	O	CMOS	3.3V	Clock output
190	SD1_CD#	I	CMOS	3.3V	Card detect, add pull up resistor if card detect is used

Table 35: 4bit SD/MMC/SDIO signals

3.11.2 Layout Requirements

Parameter	Requirement
Max Frequency	208MHz (Ultra-High Speed SD, SDR104) 52MHz (MMCplus, eMMC)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	50Ω ±15% single ended
Max skew between data signal and clock 52MHz MMC	<100ps ≈15mm
Max skew between data signal and clock SDR104	<20ps ≈3mm
Max trace length	<100mm

Table 36: SD/MMC/SDIO Layout Requirements

3.11.3 Unused SD/MMC/SDIO Interface Signal Termination

All unused SD interface signals can be left unconnected. If one of the SD/MMC/SDIO ports is unused, the signals can be used as GPIO. Unused signals of a used port (for example the upper four data bits of the 8bit interface when using only in 4bit mode), may be able to be used as GPIO. Check the relevant Apalis module datasheet for more information.

3.12 I²C

The Apalis module standard features three I²C interfaces. The interface I2C1 is a general purpose I²C while I2C2 is intended to be used with the DDC interface and I2C3 is intended to be used with the camera interfaces. All I²C interfaces can also be used for general purpose.

3.12.1 I²C Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
246	LVDS1_A_CLK-	O	LVDS		LVDS Clock out for channel A (odd pixels/single channel)
248	LVDS1_A_CLK+	O	LVDS		
252	LVDS1_A_TX0-	O	LVDS		LVDS data lane 0 for channel A (odd pixels/single channel)
254	LVDS1_A_TX0+	O	LVDS		
258	LVDS1_A_TX1-	O	LVDS		LVDS data lane 1 for channel A (odd pixels/single channel)
260	LVDS1_A_TX1+	O	LVDS		
209	I2C1_SDA	I/O	OD	3.3V	General purpose I²C data signal, pull up resistor required on carrier board

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
211	I2C1_SCL	O	OD	3.3V	General purpose I²C clock signal, pull up resistor required on carrier board
205	I2C2_SDA	I/O	OD	3.3V	Display Data Channel I²C data signal, pull up resistor required on carrier board
207	I2C2_SCL	O	OD	3.3V	Display Data Channel I²C clock signal, pull up resistor required on carrier board
201	I2C3_SDA	I/O	OD	3.3V	Camera interface I²C data signal, pull up resistor required on carrier board
203	I2C3_SCL	O	OD	3.3V	Camera interface I²C clock signal, pull up resistor required on carrier board

Table 37: I²C signals

3.12.2 Layout Requirements

Parameter	Requirement
Max Frequency	100kHz (Standard Mode) 400kHz (Fast Mode)
Configuration /Device Organisation	Multiple load, 400pF (Standard Mode), 100pF (Fast Mode)
Reference Plane	GND or PWR (No stitching capacitors required when PWR is used as reference)
Trace Impedance	50Ω ±15% single ended
Max trace length (Standard Mode)	<450mm
Max trace length (Fast Mode)	<200mm

Table 38: I²C layout requirements

The I2C does not need to be routed as differential pair, but it is recommended not to separate the data and clock lines too much. It is not required to route the bus as daisy chain as the stub length is not a problem. The maximum trace length is limited due to the capacitive load of the traces. Therefore, traces should be kept short as possible by using a star topology.

3.12.3 Unused I²C Signal Termination

All unused I²C can be left unconnected if they are unused. Unused I²C signals can be configured to be GPIO.

4 Power Management

4.1 Power Signals

4.1.1 Digital Supply Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	PWR	3.3V	Main power supply input for the module
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	PWR		Common signal and power ground
174	VCC_BACKUP	I	PWR	3.3V	RTC supply, can be left unconnected if internal RTC is not used

Table 39: Digital supply signals

4.1.2 Analogue Supply Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
314, 320	AVCC	I	PWR	3.3V	Power supply for the analogue part of the module
303, 313, 304, 308	AGND	I	PWR		Ground for the analogue part of the module

Table 40: Analogue supply signals

The analogue power supply is used on the module for the analogue circuits. 3.3V needs to be provided to this input even if the analogue interfaces are not used in a design. In this case, the pins can be connected to the 3.3V digital supply for the module. For a better audio quality and improved resistive touch performance, it is recommended that separate filters are added to the analogue power supply rail. For the best quality, a separate power supply with linear voltage regulator is recommended.

4.1.3 Power Management Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
28	RESET_MICO#	I	CMOS	3.3V	Active low reset input
26	RESET_MOCI#	O	CMOS	3.3V	Active low reset output
24	POWER_ENABLE_MOCI	O	CMOS	3.3V	Signal for the carrier board to enable the peripheral voltage rails
37	WAKE1_MICO#	I	CMOS	3.3V	Active low main module wake input signal, needs a pull up resistor on the baseboard if wake function is used

Table 41: Power management signals

To make the direction of the power management signals clear, the ending MICO or MOCI are appended to the signal names. MICO is the abbreviation for “Module Input, Carrier board Output” while MOCI stands for “Module Output, Carrier board Input”

4.2 Power Block Diagram

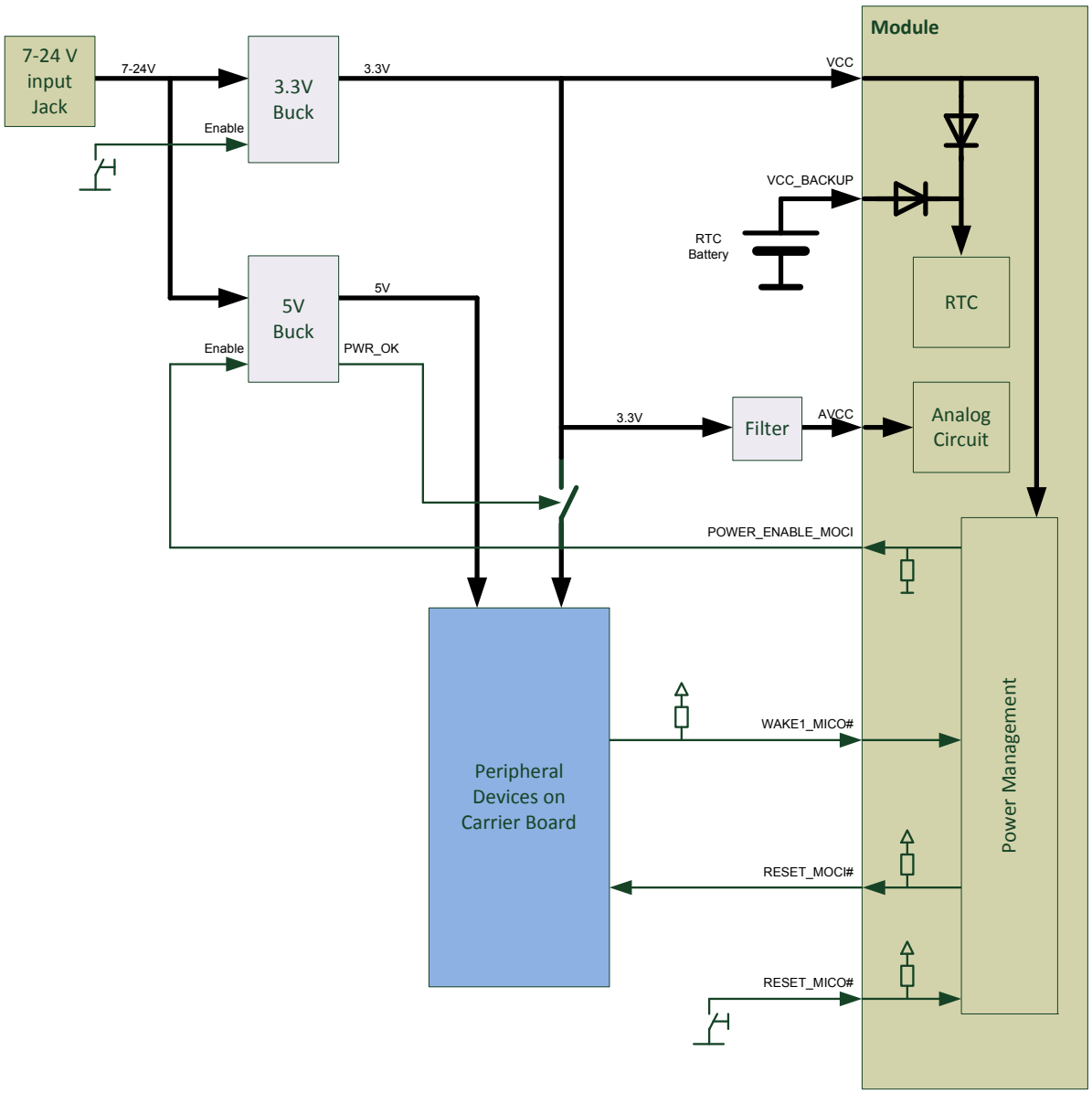


Figure 85: Power Block Diagram

4.3 Power States

The Apalis module and carrier board support different power states. The table below describes the behaviour in the different states and which power rails and peripherals are active. Additional power states can be implemented if required using available GPIOs to control additional power domains and peripherals.

Abbr.	Name	Description	Module	Carrier Board
UPG	Unplugged	No power is applied to the system, except the RTC battery might be available	No main VCC and AVCC applied, VCC_BACKUP available if backup battery is implemented	No power supply input, RTC battery maybe inserted
OFF	Off	System is off, but the carrier board input supply is available	The main VCC is available, but the CPU and peripherals are not running. Only the PMIC is running	Carrier board provides power for module, the peripheral supplies are not available

Abbr.	Name	Description	Module	Carrier Board
SUS	Suspend	System is suspended and waits for wakeup sources to trigger	CPU is suspended, wakeup capable peripherals are running while others might be switched off	Power rails are available on carrier board, peripherals might be stopped by software
RUN	Running	System is running	All power rails are available, CPU and peripherals are running	All power rails are available, peripherals are running
RST	Reset	System is put in reset state by holding RESET_MICO# is low	All power rails are available, CPU and peripherals are in reset state	All power rails are available, peripherals are in reset state

Table 42: Available Apalis power states

The figure below shows a sequence diagram for the different power states. The module automatically enters into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to suspend by software. There might be different wake up sources available. Consult the datasheet for a specific Apalis module for more information about the available wakeup events. All Apalis modules support module wake up using the signal WAKE1_MICO#. If compatibility between different Apalis modules is needed, use this pin as general wake signal.

In the running state, a shutdown request can be triggered by software. This turns off all power rails on the module and requests the carrier board to switch of the power rails for the peripherals. The module can be brought back to the running mode in two ways. The module main voltage rail (VCC) can be removed and applied again. If needed, this could also be done with a button and a small circuit. Some Apalis modules support being power cycled by asserting the RESET_MICO# signal (e.g. by pressing the reset button), please consult the associated module datasheet for more information about the support power cycle methods.

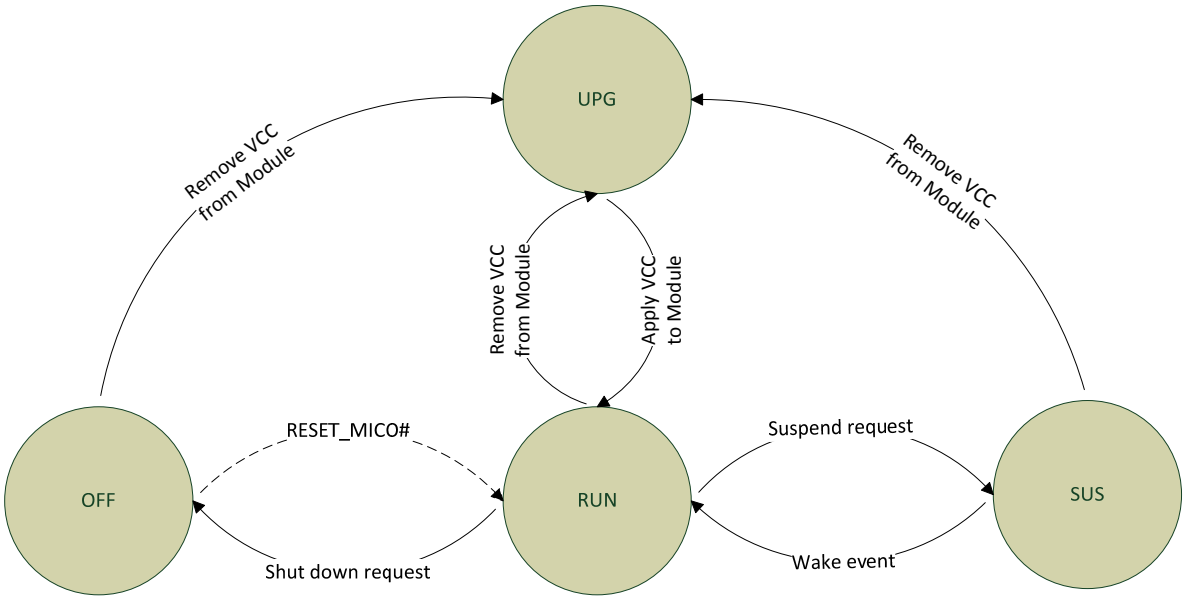


Figure 86: Power states and transitions

4.4 Power Sequences

The Apalis module starts booting as soon as the main voltage supply is applied to the module. If the system should directly boot when the main power is applied, the carrier board needs to implement the logic required to control the ramp up of the 3.3V module supply. The Apalis module will ramp up the internal power rails. When these rails are stable, the POWER_ENABLE_MOCI goes high in order to signal the carrier board that the peripheral supplies need to ramp up. The peripheral power rails on the carrier board need to ramp up in a correct sequence. The sequence starts normally with the highest voltage (e.g. 5V) followed by the lower voltages (e.g. 3.3V then

1.5V and so on). Peripherals normally require that a lower voltage rails is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for a proper sequencing.

PCIe devices require stable power supplies for at least 100ms before releasing the reset. The Apalis modules guarantees to apply the reset output RESET_MOCI# not earlier than 120ms after the POWER_ENABLE_MOCI goes high. This gives the carrier board a maximum time of 20ms for ramping up all power rails. Some Apalis modules might have longer delay, but in order to be compatible with all Apalis modules, these timings should be used.

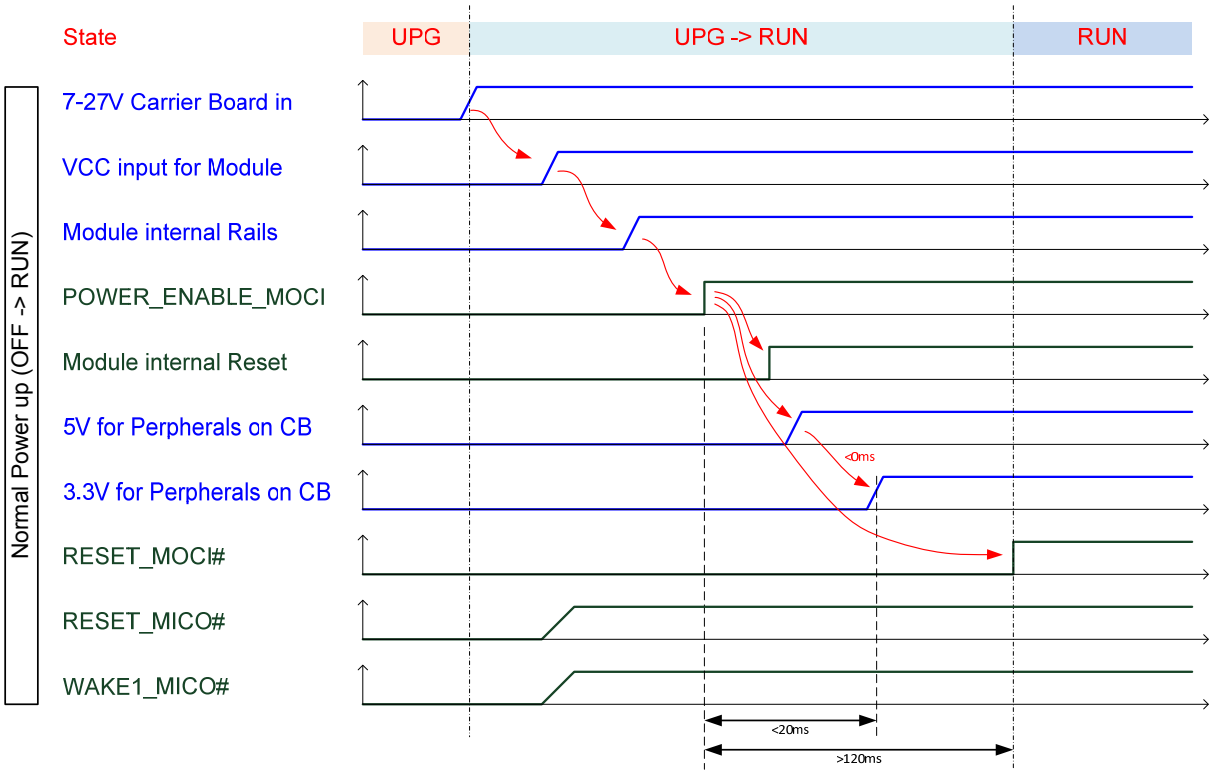


Figure 87: Power-up sequence

If the operating system supports it, a shutdown sequence can be initiated. Some systems may benefit from shutting down instead of just removing the main power supply as this allows the operating system to take care of any housekeeping (e.g. bringing mass storage devices to a controlled halt). Some operating system may not provide the shutdown function.

As it is not permitted that a lower voltage rail is present when a higher voltage rail has been switched off, the sequence of shutting down the peripheral voltages needs to be considered. The lower voltages (e.g. peripheral 3.3V) need to ramp down before the higher ones do (e.g. peripheral 5V).

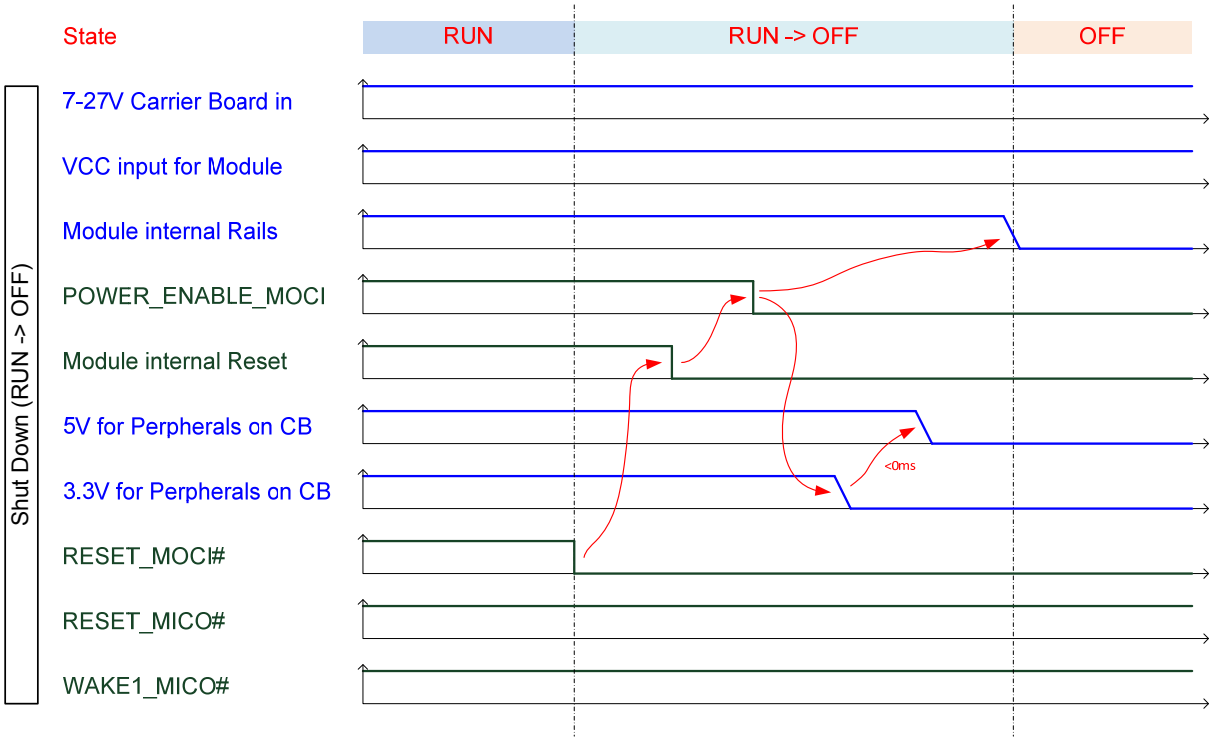


Figure 88: Shut-down sequence

When the RESET_MICO# is asserted, a reset cycle is initiated. The module internal reset and the external reset output RESET_MOCI# are asserted as long as RESET_MICO# is asserted. If the reset input RESET_MICO# is de-asserted, the internal reset and the RESET_MOCI# will remain low for at least 1ms until they are also de-asserted and the module starts booting again. This guarantees a minimum reset time of 1ms even if the reset input RESET_MICO# is triggered for a short time. Some Apalis modules may implement a power cycle during reset.

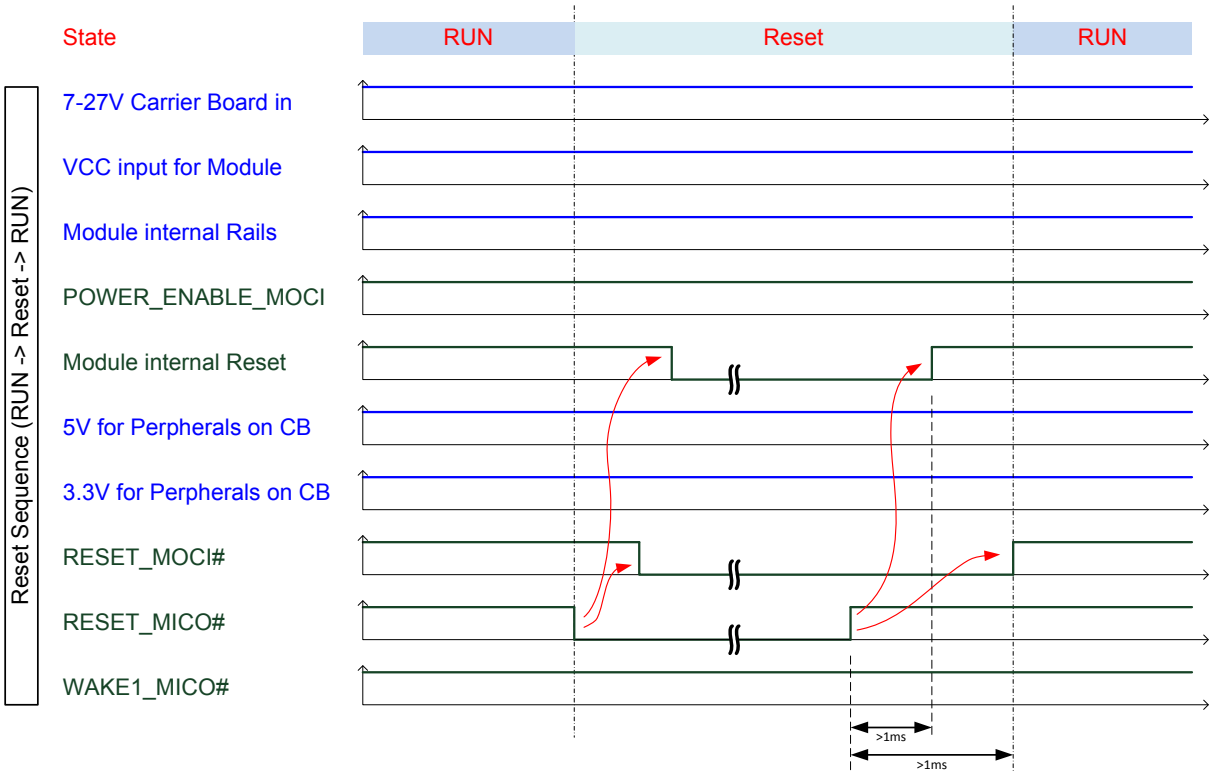


Figure 89: Reset sequence

The available suspend capabilities depends on the Apalis module. The standard approach for the carrier board is keep all peripheral supplies up, even in suspend mode. If some of the peripheral rails need to be switched off in suspend, a free GPIO can be used for this purpose. Ensure sure that the voltage power-up and power-down sequencing requirements are not violated.

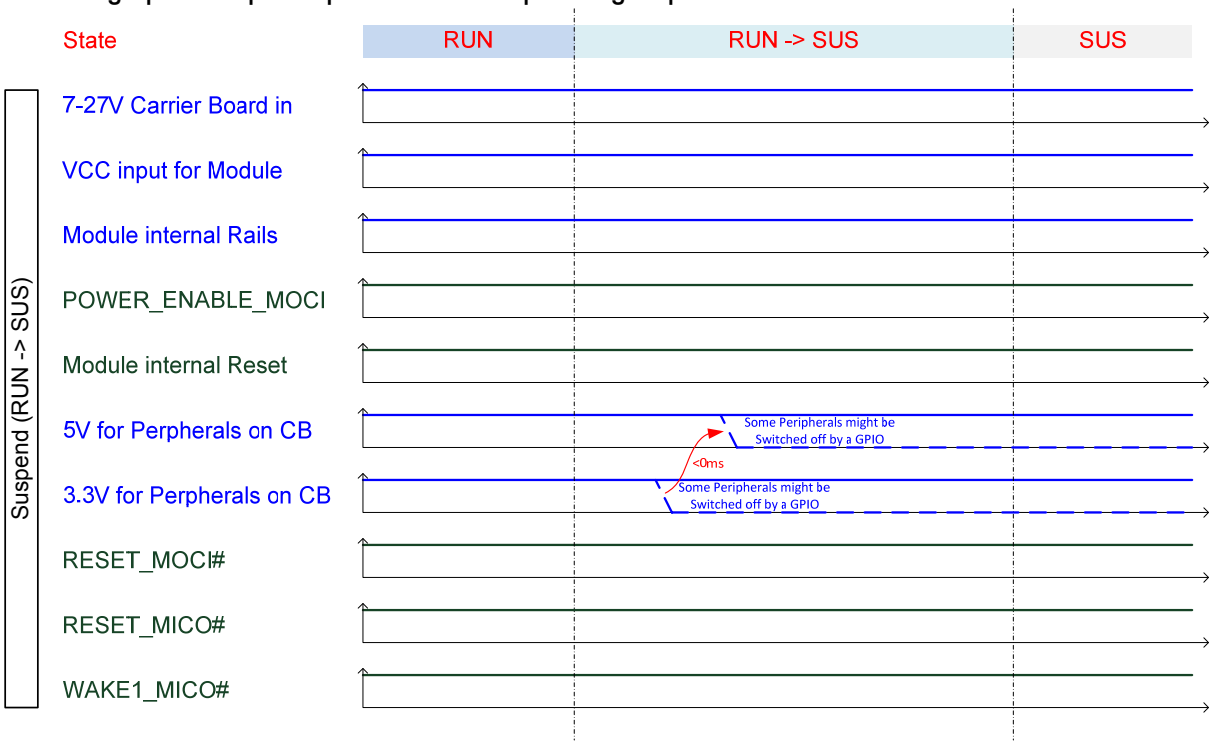


Figure 90: Suspend sequence

Different wake sources are available for different modules. The standard wake source is WAKE1_MICO#, which is guaranteed to be supported by all Apalis modules. If peripheral power supplies are controlled off by GPIO signals make sure that power sequencing requirements are not violated.

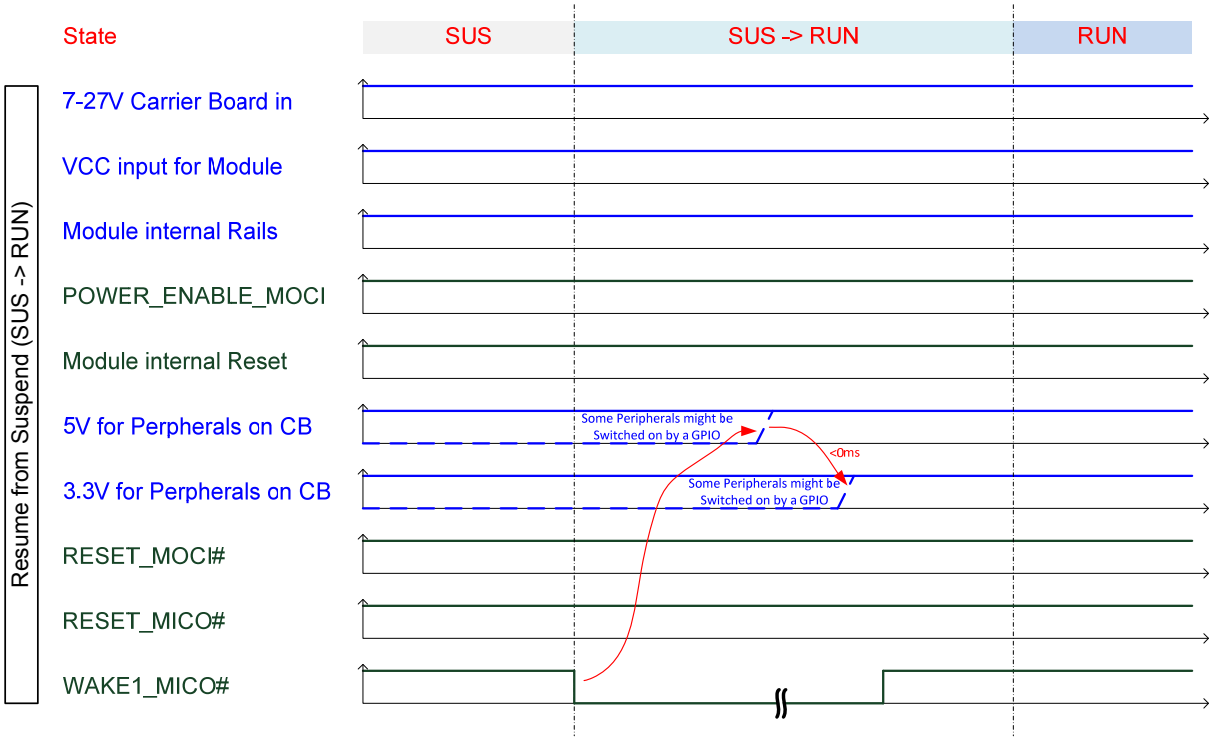


Figure 91: Resume from suspend sequence

4.5 Layout Requirements

A proper power supply layout is essential for ensuring EMC compliance. If buck or boost converters are used on the carrier board, ensure any layout requirements as defined by the manufacturer of the devices are followed. Generally, application notes and reference designs carefully document and explain any such requirements.

Place enough power supply bypass capacitors on the voltage inputs of the peripheral devices (see section 2.3.1). Place a bypass capacitor to each power input pin of the Apalis module. Be aware of the total capacity on a voltage rail when switching the voltage. If the rails are switched on too fast, the current peaks for charging all the bypass capacitors can be very high. This can produce unacceptable disturbances or can trigger an over current protection circuit. In such cases, the slew rate of switching circuits speed may need to be limited. The following figure shows a simple voltage rail switch circuit. C1 and R1 limit the switching speed. The values need to be optimized according to the requirements. It is recommended that a bypass capacitor (C2) is placed close to the switching transistor.

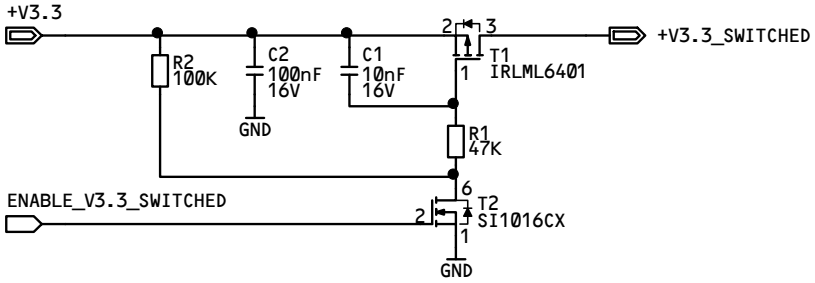


Figure 92: Simple voltage switch circuit

When routing power traces, always be aware of the electrical resistance and inductance. Try to make the traces as wide as possible. Power planes should be used instead of traces when possible. Be aware of the copper thickness of the traces. A common specification for copper foils is half ounce of copper per square foot. This is equal to a thickness of 17µm. As a rule of thumb, the resistance of a square shaped trace has a resistance of 1mΩ. This means, a trace with width of 100µm has a resistance of 1mΩ per 100µm length or a trace with the same width and a length of 100mm has a resistance of 1Ω.

Copper foils on the outer layers of a PCB (top and bottom layer) often are thicker due to the via plating process. A common value is one ounce of copper per square foot. This equals to a Thickness of 35µm. The traces of on such layers have half the electrical resistance, which is 0.5mΩ for a square shaped trace. Also consider the electrical resistance of vias. For every ampere of current, place at least one via.

4.6 Reference Schematics

It is possible to reach a suitable power up sequence by cascading the power good (e.g. PGOOD) output signals of the buck regulators with enable signal of the next regulator. The POWER_ENABLE_MOCI output features a pull down resistor on the Apalis module. An additional pull down resistor can be optionally placed on the carrier board. This pull up resistor is only needed to prevent unwanted enabling of the peripheral voltages if the module is not inserted. For designs in which the module is never removed, this pull up is not required.

The RESET_MICO# and RESET_MOCI# do not need any pull up resistors on the carrier board as these resistors are implemented on the module. The WAKE1_MICO# requires a pull up resistor on the carrier board if the wake function is implemented.

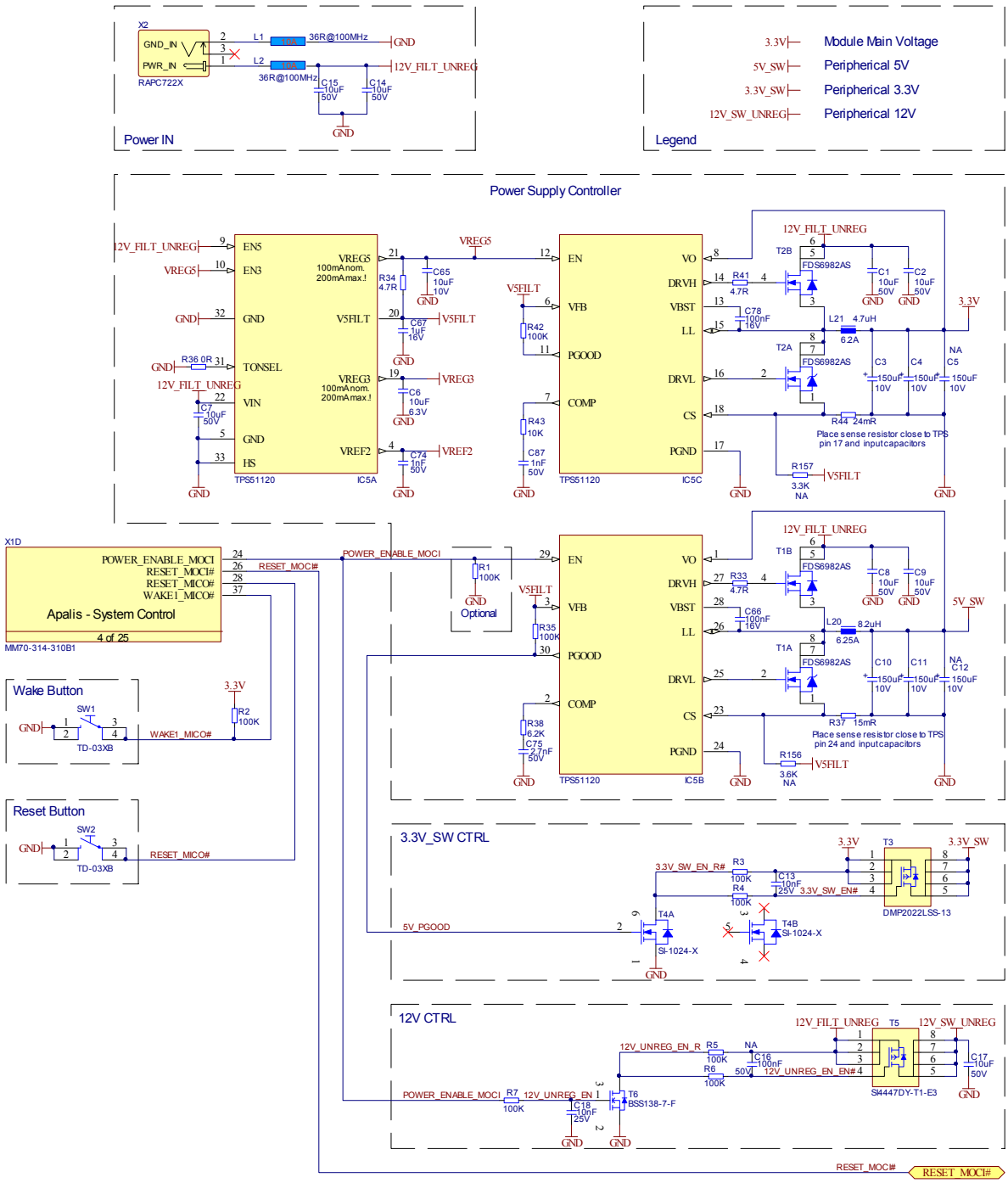


Figure 93: Simple power supply reference schematic

5 Mechanical and Thermal Consideration

5.1 Module Connector

The Apalis module is based around the MXM3 (Mobile PCI-Express Module) edge connector. This connector has been adopted by various manufacturers for use in the embedded marked. There are many suitable connectors from different manufacturers available in different stacking height. If the module is fixed to the carrier board with the MXM3 SnapLock system, a board stacking height between carrier board surface and Module bottom side of 3mm is required. In this case, the MM70-314-310B1 from JAE is recommended. Beside JAE, MXM3 connectors are also available from Aces, SpeedTech and Foxconn.

Figure 94: MXM3 Connector

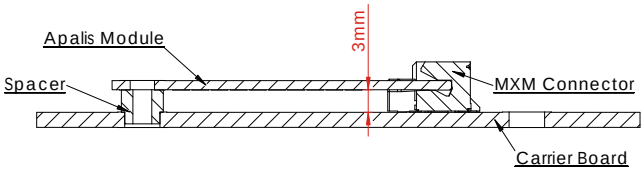


Figure 95: Board Stacking Height

5.2 Fixation of the Module

The MXM3 connector itself does not feature a locking mechanism. The mobile graphic cards using the MXM3 connector are all screwed down to the carrier board for fixation. The Apalis module features two holes which allow the module to be screwed to the carrier board. This is a preferred solution for systems that are exposed to high vibrations. Spacers need to be placed between the carrier board and the module in order to guarantee the required stacking height of the MXM3 connector. Please note that the screw holes of the Apalis modules are in a different location to those in the mobile graphic cards.

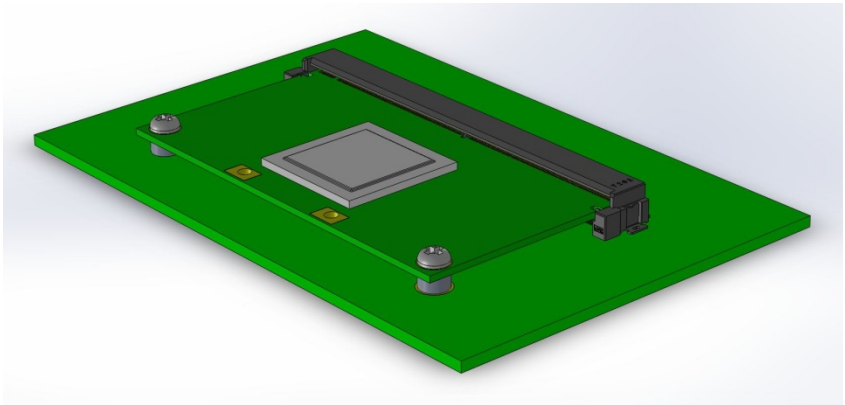


Figure 96: Screw fixation

During the development process, it may be necessary to exchange the module several times. Screwing the module to the carrier board during development can be very inconvenient. The Apalis module standard defines a mechanism of fixing the module to the carrier board with a clip mechanism, called MXM SnapLock. The clip is also used as holder of Mini PCI Express Cards. The clips are available with different stacking height and need to be consistent with the stacking height of the MXM3 connector. For the proposed stacking height of 3mm, a suitable MXM SnapLock clip is the Molex 48099-5701. If MXM SnapLock is used, the spacers at the edge of the module and under the CPU are optional if no cooling solution is required. As the MXM SnapLock connector can be assembled as normal SMD component while the spacers often need an additional production process, the unique MXM SnapLock fixing method can be cost optimized solution also for volume production.

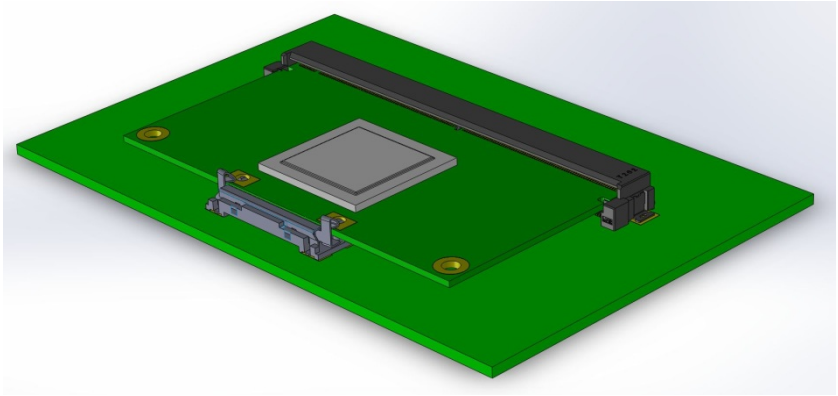


Figure 97: SnapLock fixation

5.3 Thermal Solution

Some Apalis modules may require a cooling solution when used in certain temperature range. The cooling solution needs to transport the heat (which is mainly produced by the SoC) to the external environment. The location and height of the SoC is not guaranteed to be the same between different Apalis modules. Therefore, different heat sinks may be required for different Apalis modules. This is suitable for high volume products, but for lower volume products which use different Apalis modules a solution with a heat spreader is preferable.

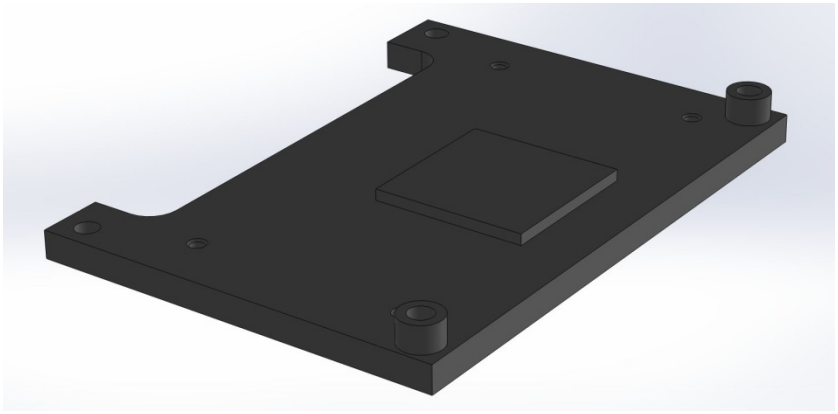


Figure 98: Bottom side of heat spreader

For every type of Apalis module, an optimized heats spreader is available. This heat spreader is not a complete cooling solution. The intention is to transport the heat to another mechanical interface. The contact area and height from the carrier board is always the same. Therefore, the system integrator can mount a customized heat sink to the heat spreader which will be compatible with all Apalis modules.

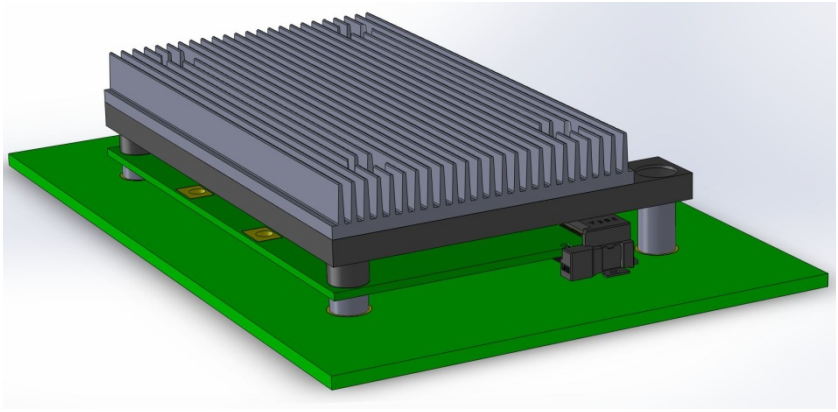


Figure 99: Heat Sink mounted on Heat Spreader

In order to guarantee good thermal conductivity between SoC and the heat spreader required for effective heat dissipation, pressure needs to be applied to the thermal interface material between SoC and spreader. As the Apalis module PCB is only 1.2mm thick, adding a force in the middle of the board would cause undesired bending and flex, which could damage to module. To prevent such bending moments, every Apalis module features a pad on the bottom side of the module. This pad allows the addition of a support standoff between module and carrier board.

If a cooling system is used that applies force to the centre area of the module PCB, it is strongly recommended that the additional spacer is added under the module.

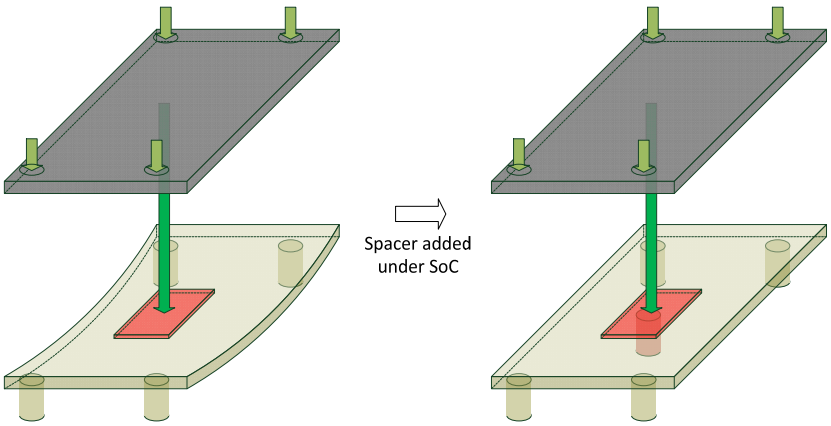


Figure 100: PCB bending problem

The figure below shows a section trough a heat spreader, mounted on an Apalis module. The overall height from carrier board surface to the top of the heat spreader is specified as 12mm. The additional spacer under the centre of the module needs have a height of 3mm.

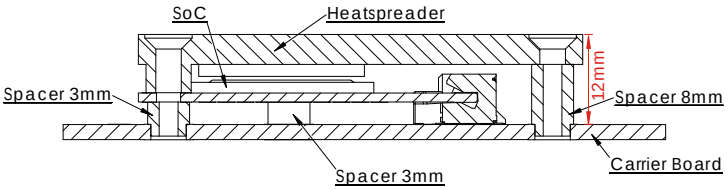


Figure 101: Stacking height of heat spreader

5.4 Module Size

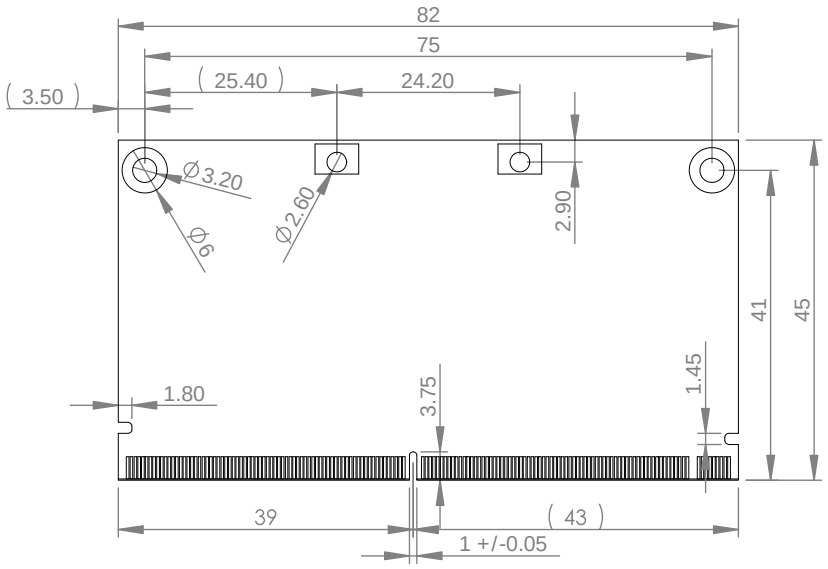


Figure 102: Module dimensions top side (dimensions in mm)

On the bottom side all modules feature a pad with a diameter of 6mm in the middle of the PCB. A standoff placed on the carrier board that contacts with this location supports the module if the cooling solution applies force. On both edges of the module, ten test pads are available. These pads are used by the module manufacturer for test purposes.

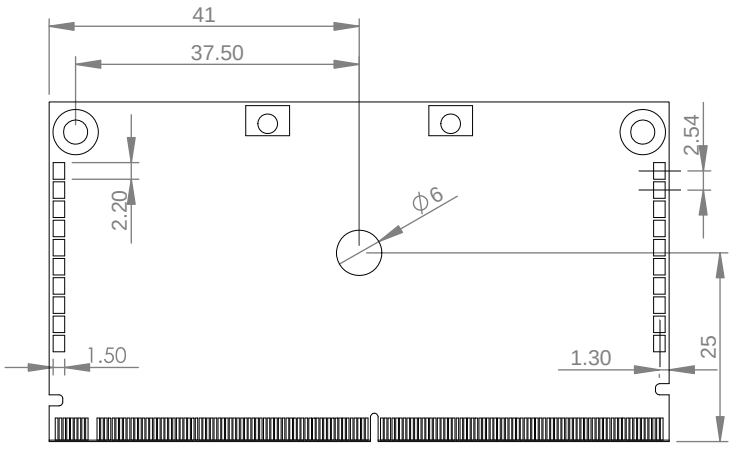


Figure 103: Module dimensions bottom side (dimensions in mm)

5.5 Connector and MXM SnapLock Land Pattern Requirements

The following figure shows the dimensions of the required land pattern for the standoffs and the MXM SnapLock connector. A carrier board does not need to feature both methods for fixing the module (SnapLock and spacers with screws), but must implement one of them. The pad and hole sizes for the standoffs depends on the assembled parts. Contact the supplier of the standoff in order to get the land pattern requirements.

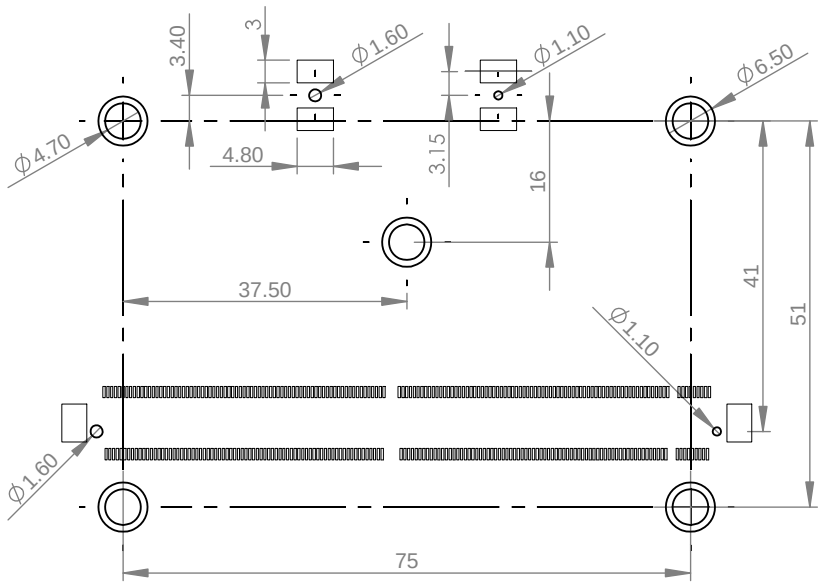


Figure 104: SnapLock and standoff land pattern (dimensions in mm)

The proposed land pattern of the MXM3 module connector is slightly different form the one that can be found in the datasheet of the connector. The reason is that the Apalis module standard does not combine power supply pins to large pads. In addition, the pin numbering is different.

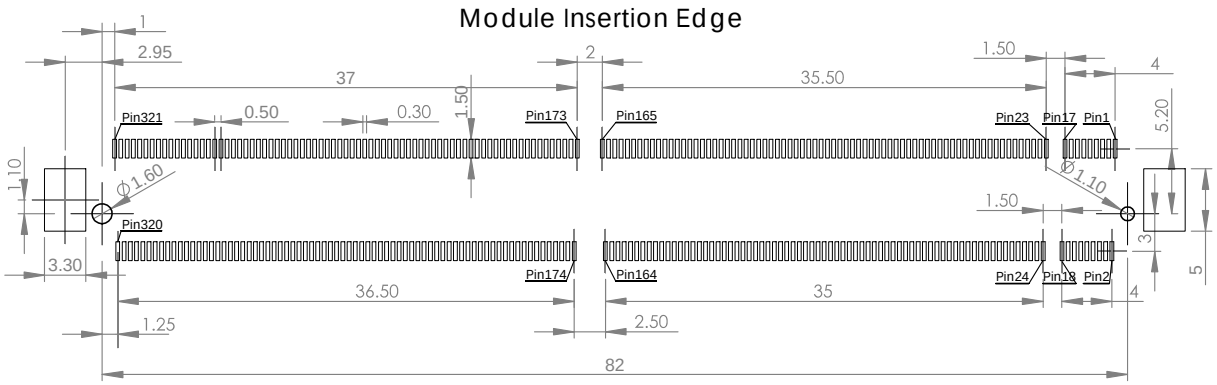


Figure 105: Module connector land pattern (dimensions in mm)

5.6 Carrier Board Space Requirements

The required PCB area for the module depends on the module fixing method and the cooling solution. The following picture shows the maximum required area if the SnapLock is used in combination with the heat spreader. Custom heat sink solutions might need additional space on the carrier board.

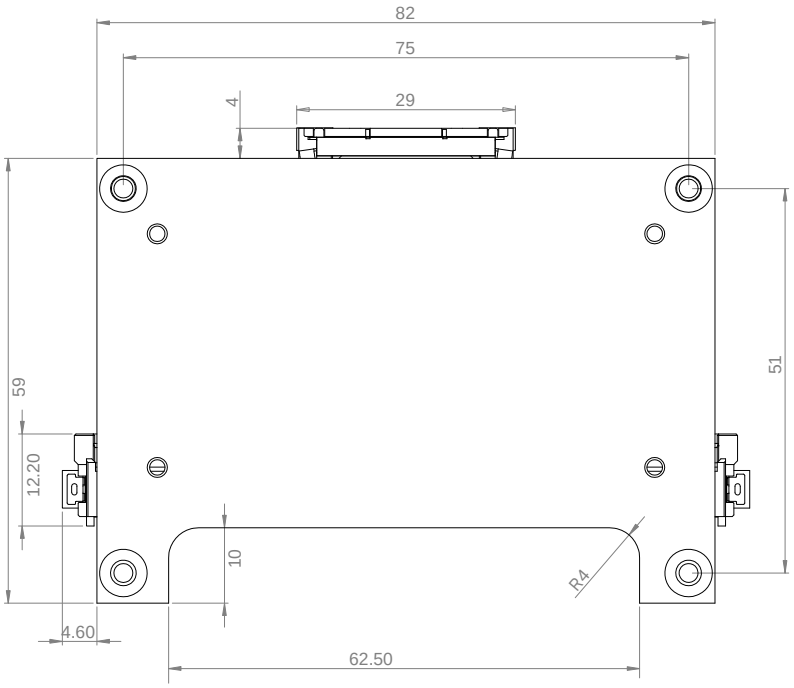


Figure 106: Maximum carrier board space requirement (dimensions in mm)

If a system does not need a cooling solution and the module is fixed by screwing it down, the required carrier board area is smaller:

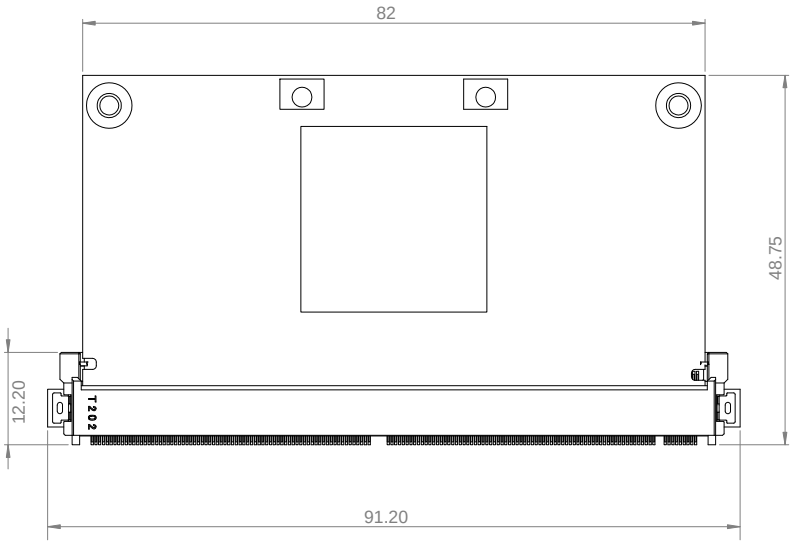


Figure 107: Minimum carrier board space requirement (dimensions in mm)

If components need to be placed under the module, the maximum required component space of the Apalis module needs to be considered. The following figure shows the maximum occupied volume on the bottom side of the Apalis module.

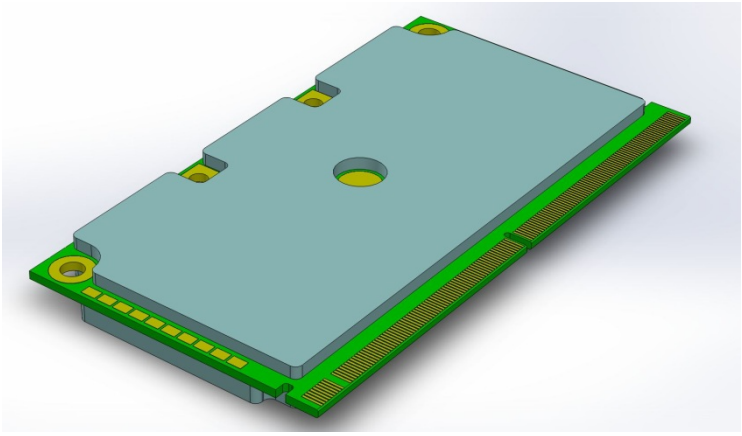


Figure 108: Maximum space requirement of components on module (bottom view)

On the bottom side of the module, components with a maximum height of 1.8mm are permitted. Components soldered on the top side of the module can be up to a maximum of 3mm in height.

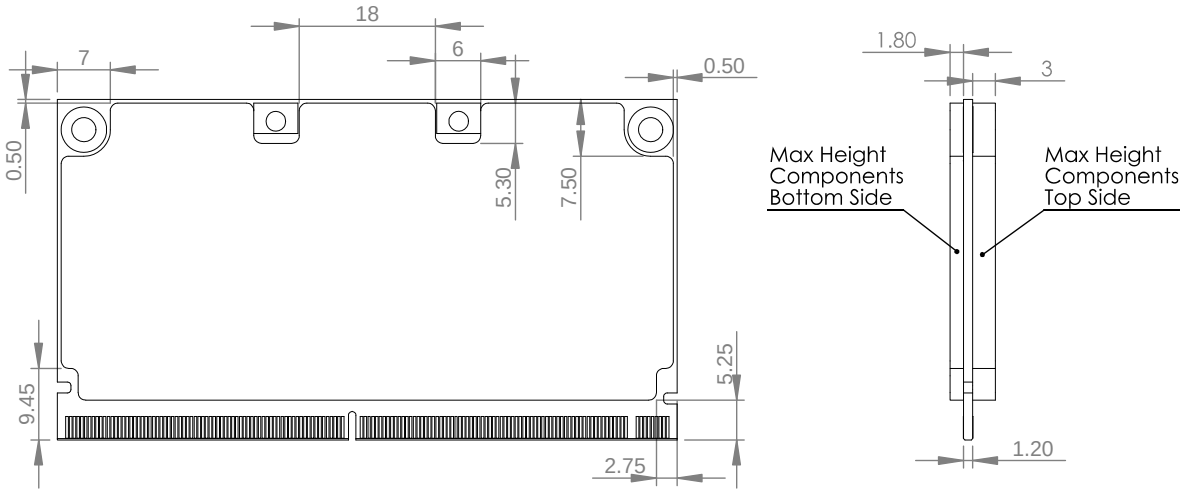


Figure 109: Maximum height of components on module (dimensions in mm)

These height restrictions of components on the module leave a space of at least 1.2mm between carrier board surface and module components when using a module connector with 3mm stacking height. To minimise the risk of any mechanical conflict, it is recommended not to place components on the carrier board directly under the module that are taller than 1mm.

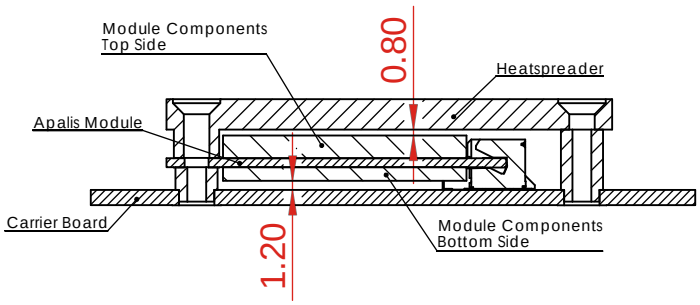


Figure 110: Maximum height of carrier board components under module

6 Appendix A – Physical Pin Definition and Location

Signal Group	Module Bottom Side	MXM3 Pins		Module Top Side	Signal Group
GPIO	GPIO1	1	2	PWM1	PWM
	GPIO2	3	4	PWM2	
	GPIO3	5	6	PWM3	
	GPIO4	7	8	PWM4	
	GND	9	10	VCC	CAN
	GPIO5	11	12	CAN1_RX	
	GPIO6	13	14	CAN1_TX	
	GPIO7	15	16	CAN2_RX	
	GPIO8	17	18	CAN2_TX	
SATA	GND	23	24	POWER_ENABLE_MOCI	System Control
	SATA1_RX+	25	26	RESET_MOCI#	
	SATA1_RX-	27	28	RESET_MICO#	
	GND	29	30	VCC	Gigabit Ethernet
	SATA1_TX-	31	32	ETH1_MDI2+	
	SATA1_TX+	33	34	ETH1_MDI2-	
	SATA1_ACT#	35	36	VCC	
	WAKE1_MICO#	37	38	ETH1_MDI3+	
PCI-Express	GND	39	40	ETH1_MDI3-	
	PCIE1_RX-	41	42	ETH1_ACT	
	PCIE1_RX+	43	44	ETH1_LINK	
	GND	45	46	ETH1_CTREF	
	PCIE1_TX-	47	48	ETH1_MDI0-	
	PCIE1_TX+	49	50	ETH1_MDI0+	
	GND	51	52	VCC	
	PCIE1_CLK-	53	54	ETH1_MDI1-	
	PCIE1_CLK+	55	56	ETH1_MDI1+	
Reserved for type specific features	GND	57	58	VCC	USB
	TS_DIFF1-	59	60	USBO1_VBUS	
	TS_DIFF1+	61	62	USBO1_SSRX+	
	TS_1	63	64	USBO1_SSRX-	
	TS_DIFF2-	65	66	VCC	
	TS_DIFF2+	67	68	USBO1_SSTX+	
	GND	69	70	USBO1_SSTX-	
	TS_DIFF3-	71	72	USBO1_ID	
	TS_DIFF3+	73	74	USBO1_D+	
	GND	75	76	USBO1_D-	
	TS_DIFF4-	77	78	VCC	
	TS_DIFF4+	79	80	USBH2_D+	
	GND	81	82	USBH2_D-	
	TS_DIFF5-	83	84	USBH_EN	
	TS_DIFF5+	85	86	USBH3_D+	
	TS_2	87	88	USBH3_D-	
	TS_DIFF6-	89	90	VCC	
	TS_DIFF6+	91	92	USBH4_SSRX-	
	GND	93	94	USBH4_SSRX+	
	TS_DIFF7-	95	96	USBH_OC#	
	TS_DIFF7+	97	98	USBH4_D+	
	TS_3	99	100	USBH4_D-	
	TS_DIFF8-	101	102	VCC	
	TS_DIFF8+	103	104	USBH4_SSTX-	
	GND	105	106	USBH4_SSTX+	
	TS_DIFF9-	107	108	VCC	UART

	TS_DIFF9+	109	110	UART1_DTR	
	GND	111	112	UART1_TXD	
	TS_DIFF10-	113	114	UART1_RTS	
	TS_DIFF10+	115	116	UART1_CTS	
	GND	117	118	UART1_RXD	
	TS_DIFF11-	119	120	UART1_DSR	
	TS_DIFF11+	121	122	UART1_RI	
	TS_4	123	124	UART1_DCD	
	TS_DIFF12-	125	126	UART2_TXD	
	TS_DIFF12+	127	128	UART2_RTS	
	GND	129	130	UART2_CTS	
	TS_DIFF13-	131	132	UART2_RXD	
	TS_DIFF13+	133	134	UART3_TXD	
	TS_5	135	136	UART3_RXD	
	TS_DIFF14-	137	138	UART4_TXD	
	TS_DIFF14+	139	140	UART4_RXD	
	GND	141	142	GND	
	TS_DIFF15-	143	144	MMC1_D2	
	TS_DIFF15+	145	146	MMC1_D3	
	GND	147	148	MMC1_D4	
	TS_DIFF16-	149	150	MMC1_CMD	
	TS_DIFF16+	151	152	MMC1_D5	MMC
	GND	153	154	MMC1_CLK	
	TS_DIFF17-	155	156	MMC1_D6	
	TS_DIFF17+	157	158	MMC1_D7	
	TS_6	159	160	MMC1_D0	
	TS_DIFF18-	161	162	MMC1_D1	
	TS_DIFF18+	163	164	MMC1_CD#	
	GND	165			
Parallel Camera	CAM1_D7	173	174	VCC_BACKUP	
	CAM1_D6	175	176	SD1_D2	
	CAM1_D5	177	178	SD1_D3	
	CAM1_D4	179	180	SD1_CMD	
	CAM1_D3	181	182	GND	SDIO
	CAM1_D2	183	184	SD1_CLK	
	CAM1_D1	185	186	SD1_D0	
	CAM1_D0	187	188	SD1_D1	
	GND	189	190	SD1_CD#	
	CAM1_PCLK	191	192	GND	
	CAM1_MCLK	193	194	DAP1_MCLK	
	CAM1_VSYNC	195	196	DAP1_D_OUT	
	CAM1_HSYNC	197	198	DAP1_RESET#	Digital Audio
I2C	GND	199	200	DAP1_BIT_CLK	
	I2C3_SDA	201	202	DAP1_D_IN	
	I2C3_SCL	203	204	DAP1_SYNC	
	I2C2_SDA	205	206	GND	
	I2C2_SCL	207	208	VGA1_R	
	I2C1_SDA	209	210	VGA1_G	VGA
	I2C1_SCL	211	212	VGA1_B	
SPDIF	GND	213	214	VGA1_HSYNC	
	SPDIF1_OUT	215	216	VGA1_VSYNC	
	SPDIF1_IN	217	218	GND	
SPI	GND	219	220	HDMI1_CEC	
	SPI1_CLK	221	222	HDMI1_TXD2+	HDMI
	SPI1_MISO	223	224	HDMI1_TXD2-	
	SPI1_MOSI	225	226	GND	

	SPI1_CS	227	228	HDMI1_TXD1+	
	SPI2_MISO	229	230	HDMI1_TXD1-	
	SPI2_MOSI	231	232	HDMI1_HPD	
	SPI2_CS	233	234	HDMI1_TXD0+	
	SPI2_CLK	235	236	HDMI1_TXD0-	
Digital RGB	GND	237	238	GND	Dual Channel LVDS
	BKL1_PWM	239	240	HDMI1_TXC+	
	GND	241	242	HDMI1_TXC-	
	LCD1_PCLK	243	244	GND	
	LCD1_VSYNC	245	246	LVDS1_A_CLK-	
	LCD1_HSYNC	247	248	LVDS1_A_CLK+	
	LCD1_DE	249	250	GND	
	LCD1_R0	251	252	LVDS1_A_TX0-	
	LCD1_R1	253	254	LVDS1_A_TX0+	
	LCD1_R2	255	256	GND	
	LCD1_R3	257	258	LVDS1_A_TX1-	
	LCD1_R4	259	260	LVDS1_A_TX1+	
	LCD1_R5	261	262	USBO1_OC#	
	LCD1_R6	263	264	LVDS1_A_TX2-	
	LCD1_R7	265	266	LVDS1_A_TX2+	
	GND	267	268	GND	
	LCD1_G0	269	270	LVDS1_A_TX3-	
	LCD1_G1	271	272	LVDS1_A_TX3+	
	LCD1_G2	273	274	USBO1_EN	
	LCD1_G3	275	276	LVDS1_B_CLK-	
	LCD1_G4	277	278	LVDS1_B_CLK+	
	LCD1_G5	279	280	GND	
	LCD1_G6	281	282	LVDS1_B_TX0-	
	LCD1_G7	283	284	LVDS1_B_TX0+	
	GND	285	286	BKL1_ON	
	LCD1_B0	287	288	LVDS1_B_TX1-	
	LCD1_B1	289	290	LVDS1_B_TX1+	
	LCD1_B2	291	292	GND	
	LCD1_B3	293	294	LVDS1_B_TX2-	
	LCD1_B4	295	296	LVDS1_B_TX2+	
	LCD1_B5	297	298	GND	
	LCD1_B6	299	300	LVDS1_B_TX3-	
	LCD1_B7	301	302	LVDS1_B_TX3+	
Analogue and Touch	AGND	303	304	AGND	Analogue Audio
	AN1_ADC0	305	306	AAP1_MICIN	
	AN1_ADC1	307	308	AGND	
	AN1_ADC2	309	310	AAP1_LIN_L	
	AN1_TSWIP_ADC3	311	312	AAP1_LIN_R	
	AGND	313	314	AVCC	
	AN1_TSPX	315	316	AAP1_HP_L	
	AN1_TSMX	317	318	AAP1_HP_R	
	AN1_TSPY	319	320	AVCC	
	AN1_TSMY	321			

Table 43: Physical pin definition and location