High Speed Channel Design Using the SFF-8431 Protocol

2013.07.10

AN-689

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This document enables engineers to design high speed channels conforming to the SFF-8431 standard. It includes a case study of a board that was designed to highlight best practices for SFF-8431 compliant channel design. The standard requires the total loss for the channel to be less than -6.5 dB at 5.5 GHz. To conform to the standard, the designer should use the following techniques to minimize the losses in high speed channels.

Factors for Signal Integrity and Loss

To ensure good signal integrity, consider these factors:

- The material that will be used to construct the board
- The routing layers to be used for the topology
- Via design for good signal integrity
- Cutouts under components to balance impedance

The following guidelines enable you to create layouts that yield well-behaved high speed data channels.

Material Selection

PCB material is a major concern for transceivers. A balance must be created between cost and performance. Performance is determined by the loss characteristics of the material.

Table 1: dB Loss for Common PCB Materials

This chart shows loss in a 5-inch run of various materials. Only one frequency is shown; however, the loss scales nearly linearly with frequency.

Material	5-inch Trace dB Loss at 12.5 Gbps
Megtron 6	-1.90
Rogers 4350B	-1.97
Nelco 4K13EPSI	-2.55
Nelco 4K13EP	-2.89
Isola FR408HR	-3.00
Isola FR370HR	-6.19

The dissipation factor for the material dictates this loss. Inexpensive material may be useful if the traces are very short.

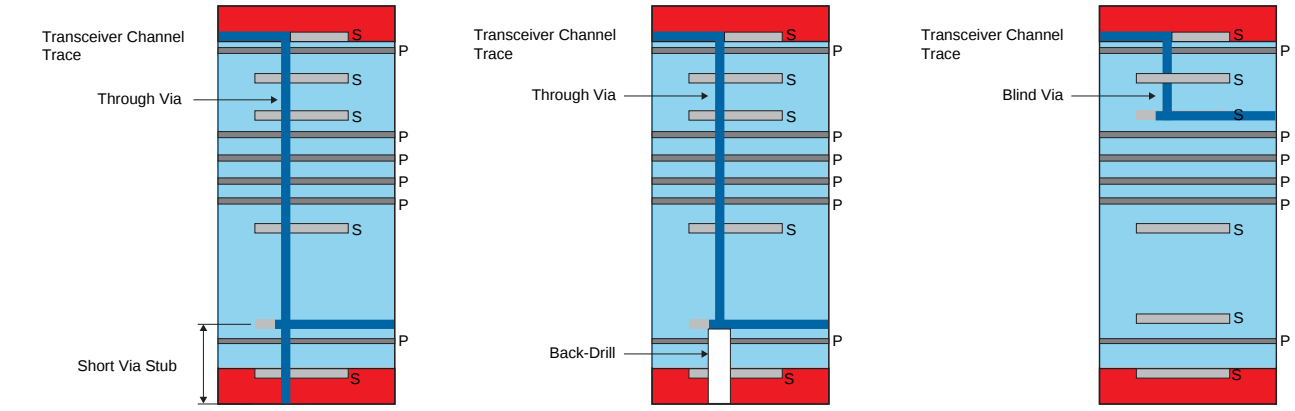
Related Information

For more details on material selection, refer to *AN-613: PCB Stackup Design Considerations for Altera FPGAs*.

Routing Layer Selection

Selection of the routing layers for the topology is determined by many variables. Routing only on the top and bottom (microstrip) layers of the PCB creates no stub lengths for the vias, but the loss when running on a microstrip layer is larger than the loss when running on an embedded (stripline) layer. The effects that arise from via stubs created when using stripline layers cause a problem. These effects can be relieved in part by back-drilling the vias to reduce the stub length. Blind vias are also a good solution for stripline routing, but raise the cost of the board.

Figure 1: Examples of Various Stripline Routing Solutions



Related Information

- *AN-651: PCB Breakout Routing for High-Density Serial Channel Designs Beyond 10 Gbps*
- *AN-613: PCB Stackup Design Considerations for Altera FPGAs*

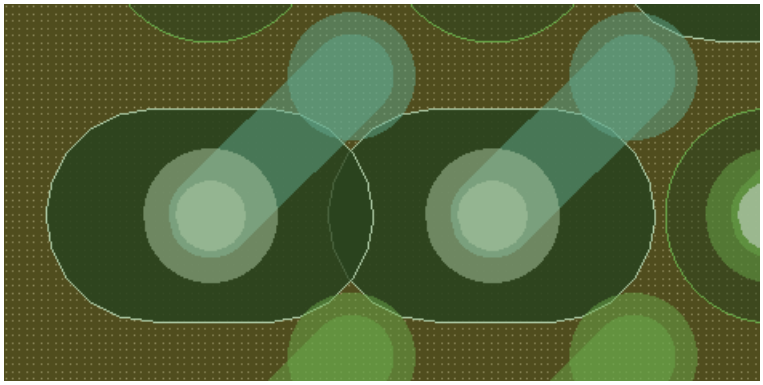
Via Design

Good via design is essential for high speed signals. It greatly reduces loss when implemented correctly.

BGA Vias

For BGA vias, all signal vias are 8 mils in diameter. For signals less than 13 Gbps, it is best to create antipads that are ellipses measuring 30 mils x 50 mils if the vias are 1 mm apart.

Figure 2: BGA Via Treatment Example

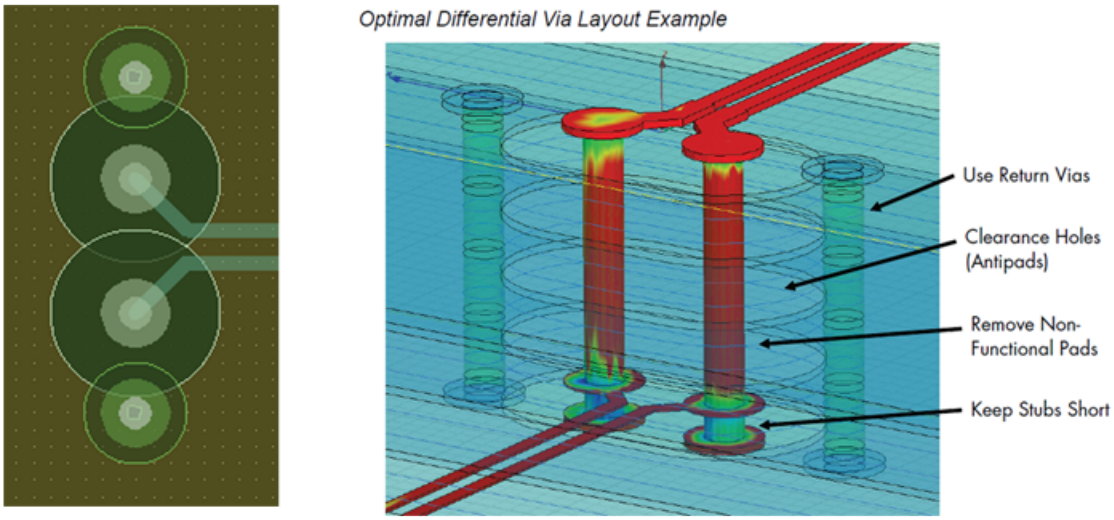


This is the best technique, given the space limitations. There is still a dip in the impedance of the system from using these anti-pads. For lines greater than 13 Gbps, route these traces on the surface layer to midline vias, if possible, to reduce reflections.

Midline Vias

Midline vias are vias that are outside of the BGA field. For an 8-mil via, use antipads of 50 mils on 40-mil centers and add grounded vias that are 30 mils away from the midline vias.

Figure 3: Midline Vias Examples



Related Information

AN-529: Via Optimization Techniques for High-Speed Channel Designs

Cutouts for Components

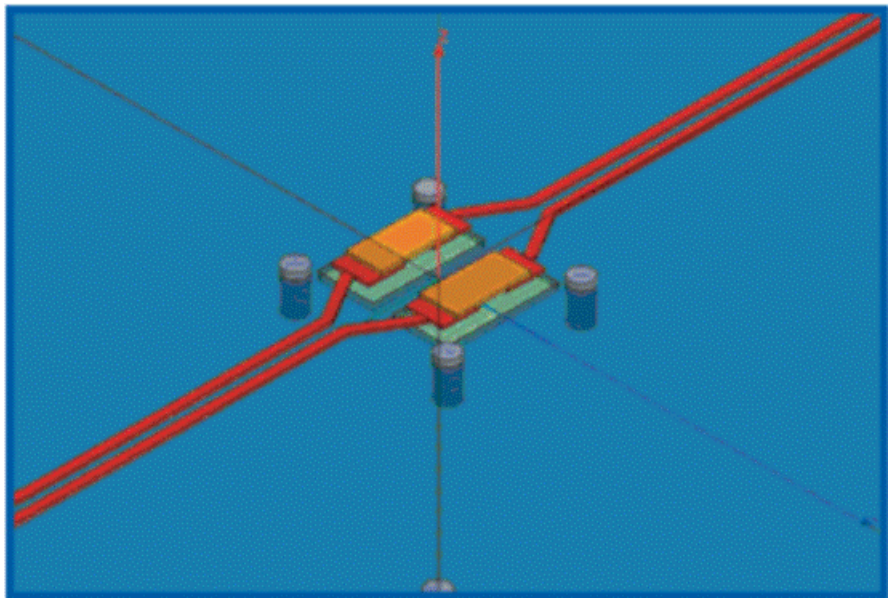
Defining cutouts for components is a very critical part of the process. On high-speed printed circuit boards, portions of the signal path like DC-blocking capacitors, series resistors, and connectors all cause impedance discontinuities.

In the case of surface mount components, the width of the mounting pad is nearly always larger than the nominal trace with a characteristic impedance of 50Ω. This larger size necessitates the removal of some material from possible reference layers below the component. This reduces the capacitive coupling of the reference planes, and creates a path without impedance discontinuities.

Surface Mount Components

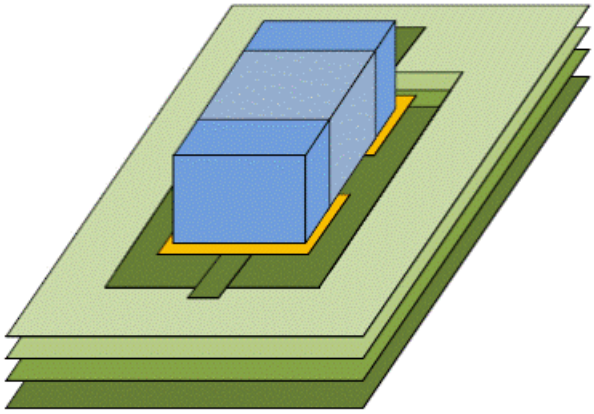
Transceiver channels often incorporate components such as DC-blocking capacitors to control the common mode voltage at the receiver. However, the presence of the blocking capacitors in the channel creates an abrupt discontinuity where the trace meets the component. The size of the component mounting pad results in additional capacitance which lowers the channel's characteristic impedance at the component. One way of reducing this capacitance is to increase the distance to the reference plane by making cut-outs underneath the body of the component mounting pad footprint.

Figure 4: DC Blocking Capacitor Plane Cut-out



By cutting out the first reference plane directly below the capacitor, the impedance increases as it references the second plane further away. However, if this second reference plane is close to the first reference plane, the impedance increase may still not be enough. In this case it also becomes necessary to cut out the second, third, or even more successive planes underneath to further increase the impedance.

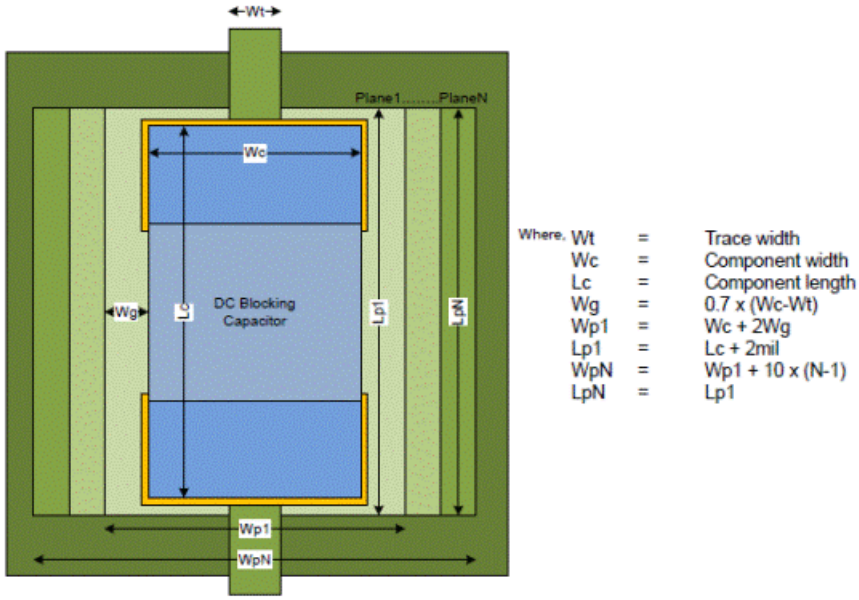
Figure 5: Successive DC Blocking Capacitor Plane Cutouts



Normally, determining the proper size of the cutouts and number of planes below the capacitor to cut is determined by extensive 3-D simulations. However, a formulaic approach based on simulations for determining this cutout is also possible.

Figure 6: Detailed Plan for Multi-Plane Cutouts Under Components

Schematic view of the relationships determined by this process. Plane 1 is the closest to the component.



Detailed Description of the Cutout Formulas

1. Cut out any plane underneath the capacitor where the proximity is within 0.75 Wc.
2. Set the side gap of the cut-out for plane 1 (Wg) = 0.7 (Wc - Wt).
3. Set the cut-out width of plane 1 (Wp1) = Wc+2 Wg.
4. Set the cut-out length of plane 1 (Lp1) = Lc+2 mils.

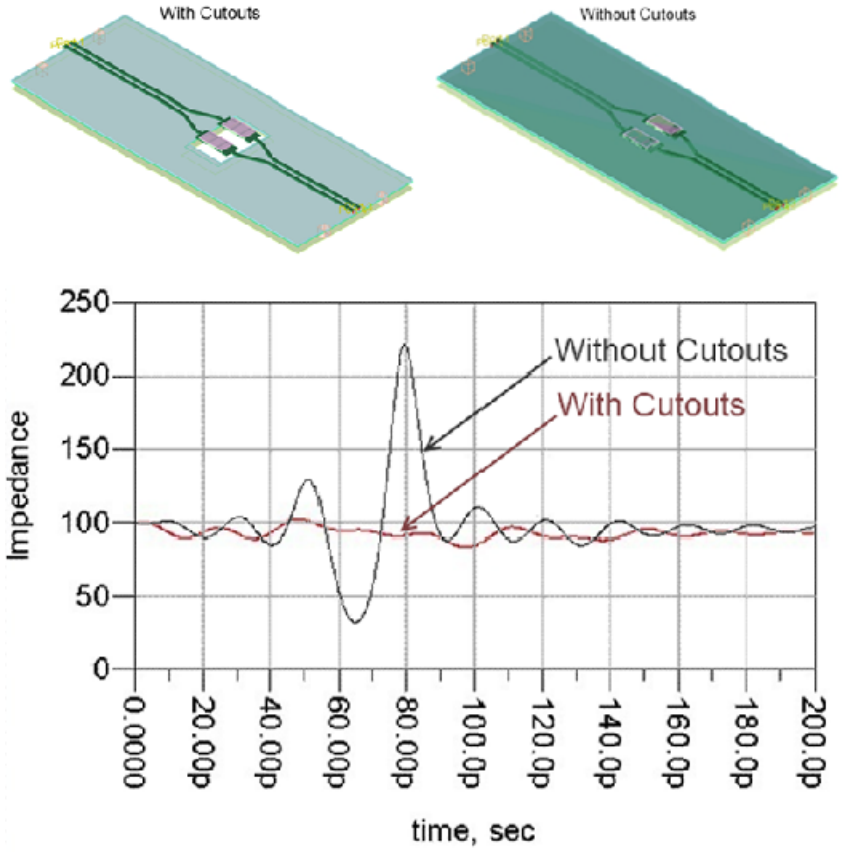
5. Set the cut-out width of successive plane N (WpN) = Wp1 + 10 (N-1).
6. Set the cut-out length of successive plane N (LpN) = Lp1.

Simulations Showing Cutout Results

With the plane cutouts properly applied using the above guidelines, the large discontinuity at the trace to DC blocking capacitor junction is eliminated.

Figure 7: Setup and TDR Results of Simulated Systems

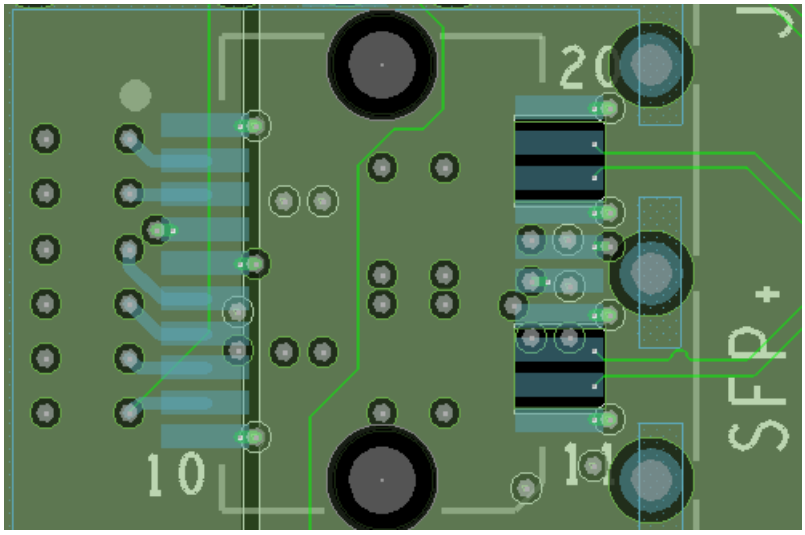
Compares the time-domain reflectometer (TDR) results of the DC blocking capacitor layout with and without the plane cutout improvements.



Surface Mount Cutouts for Connectors

The formula above produces good results for connectors also.

Figure 8: Surface Mount Cutouts for Connectors



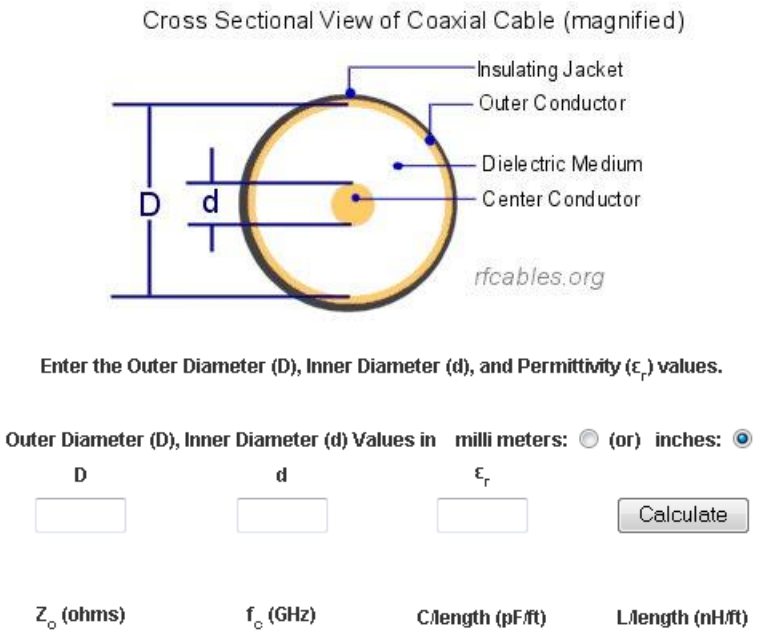
Through Hole Connectors

Many connector manufacturers provide information concerning the cutouts under their connectors to optimize the signal propagation.

In the case where this data is not provided, there are remedies. For through hole pads, it is best to consider the hole for the conductor to be the center conductor of a coax. You can find several calculators on the Internet that allow you to calculate the size of the antipads necessary to make the via conductor look like a transmission line.

To calculate the antipad diameter, first enter the diameter of the mounting hole as "d." The dielectric constant is entered as "Er." Entering some value for the antipad size as "D" and running the calculator results in a characteristic impedance for the through-hole system. Adjust the value for "D" and repeat to converge on a good antipad diameter. This antipad should be applied to all layers that are not backdrilled.

Figure 9: Example of a Coax Calculator



Related Information

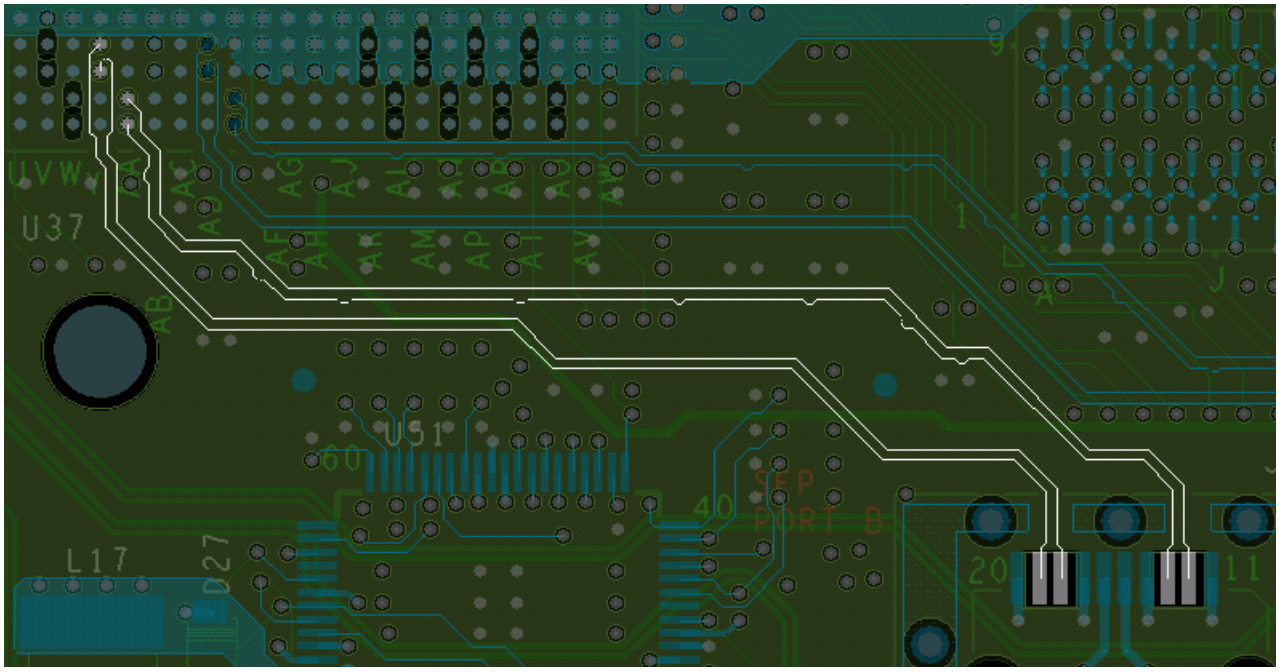
- **Online Coax Cable Impedence Calculator**
- ***AN-596: Modeling and Design Considerations for 10 Gbps Connectors***
- ***AN-651: PCB Breakout Routing for High-Density Serial Channel Designs Beyond 10 Gbps***
- ***AN-684: Design Guidelines for 100 Gbps - CFP2 Interface***

Implementation on a Board Design

The techniques above were applied to an SFF-8431 interface evaluation board using the following implementation:

- The design was constrained for crosstalk to reduce jitter.
- The length matching for transceiver pairs was constrained tightly to reduce deterministic jitter. Length matching bumps were used for this purpose

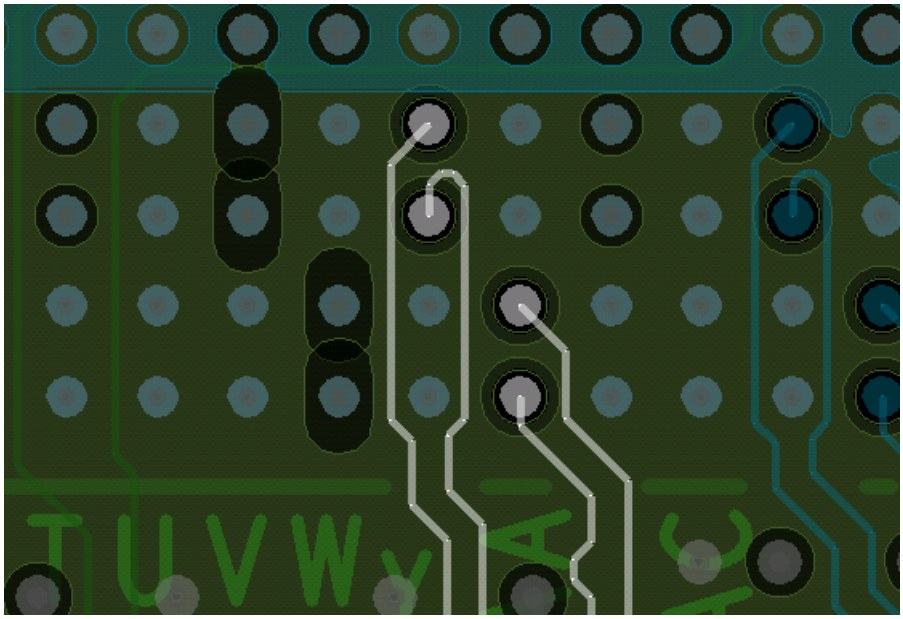
Figure 10: Length Matching Bumps



- The signals were routed on the surface layer to avoid having to use vias. Vias for through-board transceivers are visible near them.

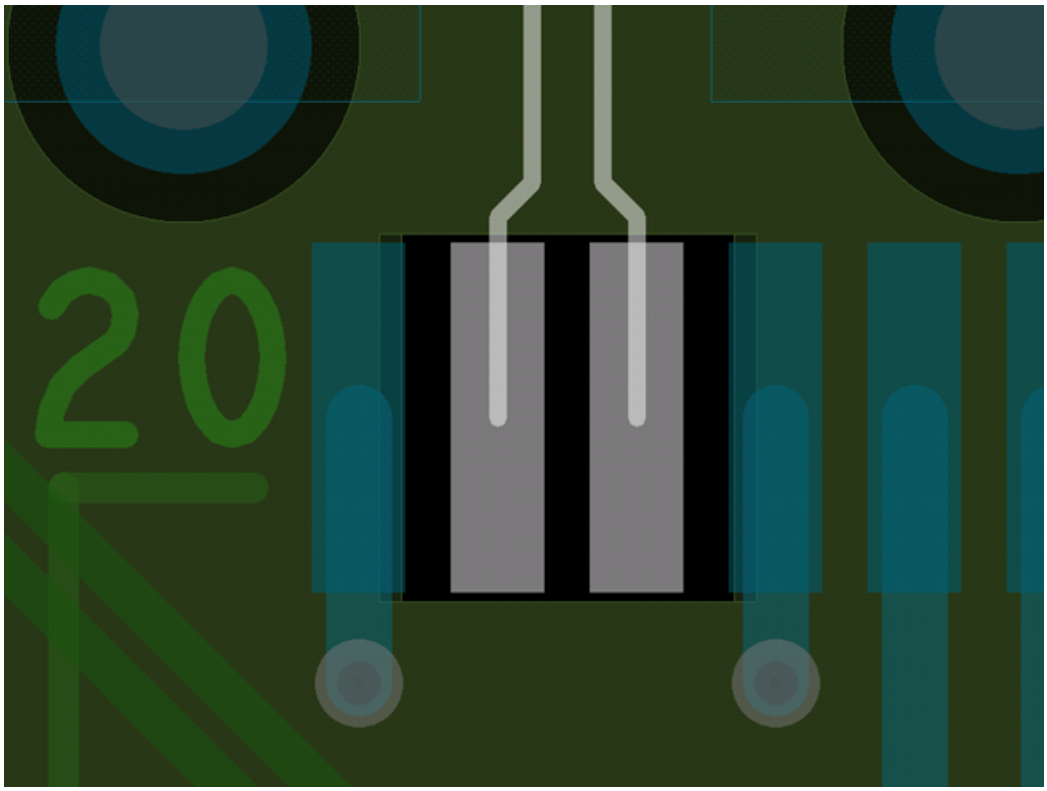
Figure 11: Through Board Transceiver Vias

Includes a close-up view of a length matching bump.



- The transceiver lines at the FPGA Mezzanine Card (FMC) connector were given cutouts on the two plane layers beneath them. These were calculated using the formulas described above.

Figure 12: Cutouts Under the Pins of the Enhanced Small Form-Factor Pluggable (SFP+) Connector



Appendix: Channel Design Guidelines for SFF-8431

This appendix provides channel design guidance for 10.3 Gbps SFF-8431 compliance, specifically improving the inter-symbol interference (ISI) due to reduced reflections and improved insertion loss at the SFP+ interface.

ISI is mainly dependent on three factors:

- Pattern type and length
- Channel insertion loss
- Channel reflections

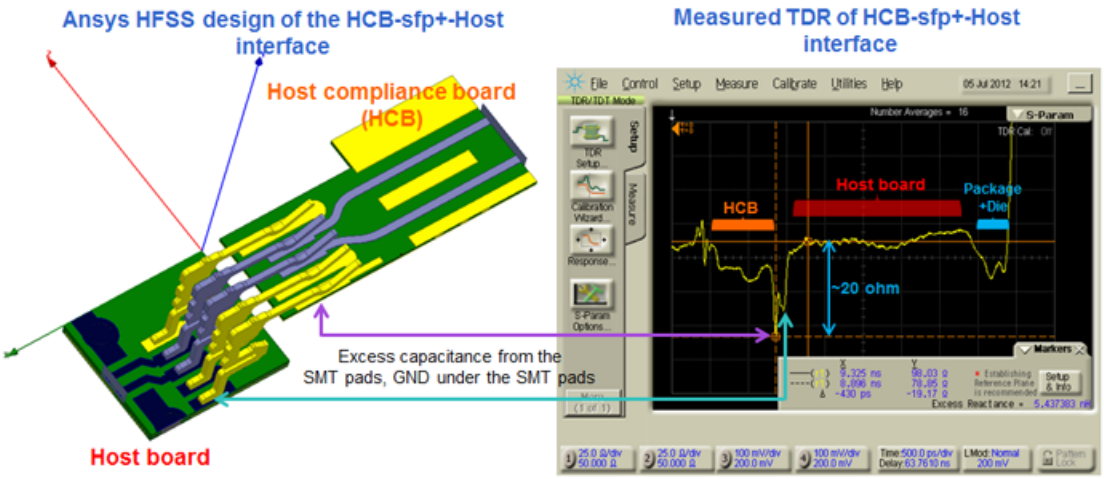
These guidelines show channel optimization to improve channel insertion loss and reduce channel reflections on the SFP+ interface, thereby improving the ISI portion of the total jitter. The results of the case study are summarized with and without optimization of the SFP+ interface, and provide details on:

- Impedance (TDR) and the channel insertion loss (SDD21) for an **un-optimized** SFP+ interface
- Impedance (TDR) and the channel insertion loss (SDD21) for an **optimized** SFP+ interface
- Optimization details to improve the SFP+ interface
- Recommendations for the SFP+ connector interface

SFP+ Interface Before Optimization

Figure 13: SFP+ Interface Before Optimization

3D design detail of the host compliance board (HCB) plugged into the host board with a SFP+ connector and its measured TDR impedance.



Source of Impedance Discontinuity

- Excess capacitance:
  - SMT pads of the host board and the HCB
  - GND under the surface-mount technology (SMT) pads of the host board and the HCB
- Inherent connector resonance:
  - 3D electromagnetic (EM) simulations of the SFP+ connector show inherent connector-only resonances at ~8 GHz

SFP+ Interface After Optimization

Figure 14: SFP+ Interface After Optimization

3D design detail of the HCB plugged into a module compliance board with an SFP+ connector and its measured TDR impedance.

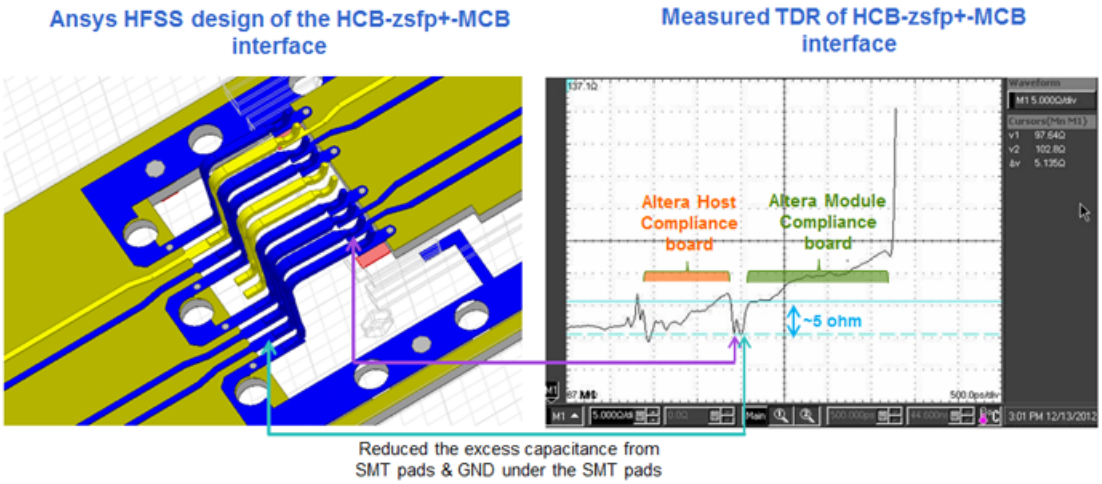


Figure 15: Channel SDD21 Before and After Optimization

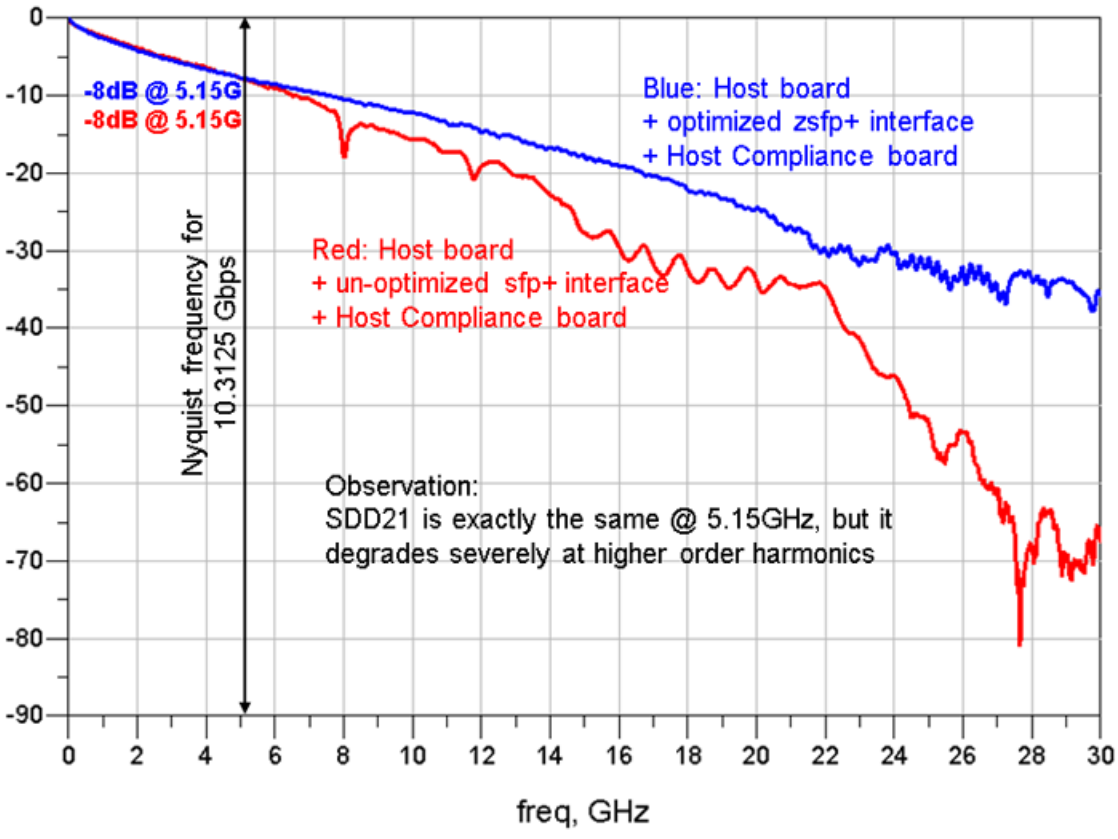


Table 2: Stratix IV GT Board Total Jitter Using Optimized and Un-optimized Channels

The improvement in total jitter in the blue curve result

Topology, Stratix IV GT Board	Total Jitter	ISI Contribution to Jitter
Un-optimized Channel, Red Curve	23.81 ps	12.6 ps
Optimized Channel, Blue Curve	20.00 ps	9.5 ps

The improvement in total jitter in the blue curve comes from lower reflections. Linear-loss channels benefit the most from pre-emphasis.

Figure 16: Impact of Insertion Loss on ISI

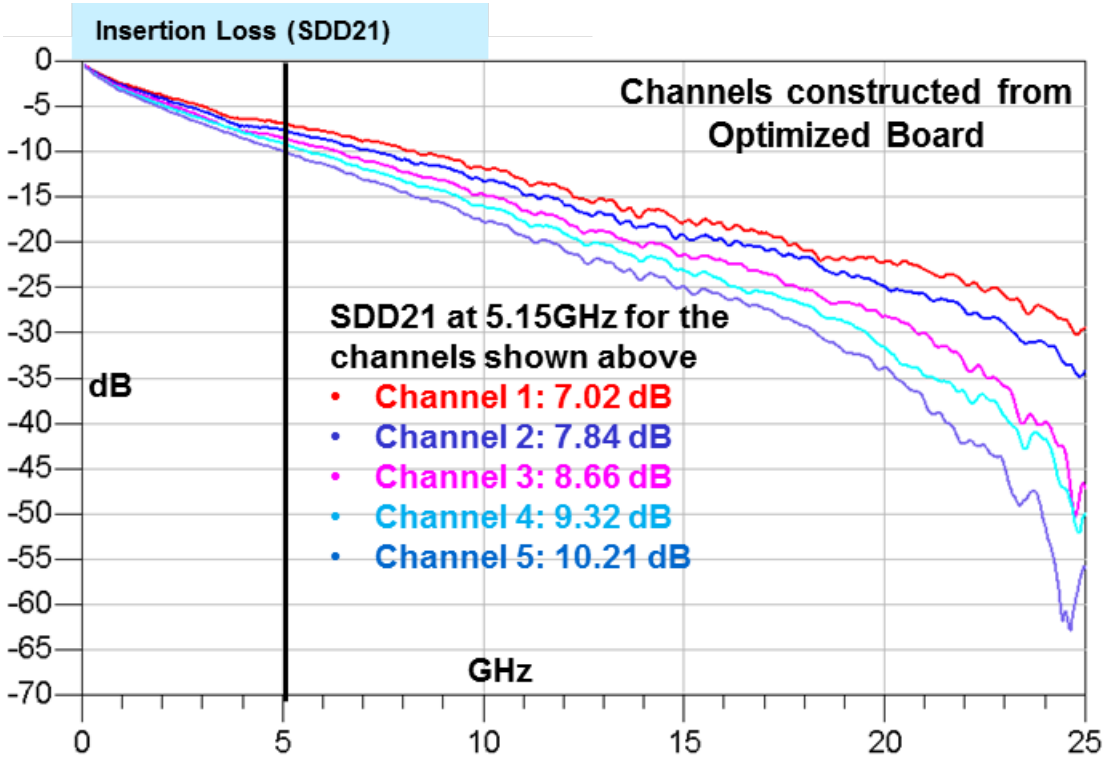


Table 3: Jitter on Stratix IV GT Optimized Channels

Pre-emphasis (Optimized)	Total Jitter	ISI Contribution to Jitter
Chanel 2: 7.84 dB	19.3 ps	9.0 ps
Channel 3: 8.66 dB	20.0 ps	9.4 ps
Channel 4: 9.32 dB	21.3 ps	10.4 ps
Channel 5: 10.21 dB	22.4 ps	11.2 ps

Observations Before and After Optimization

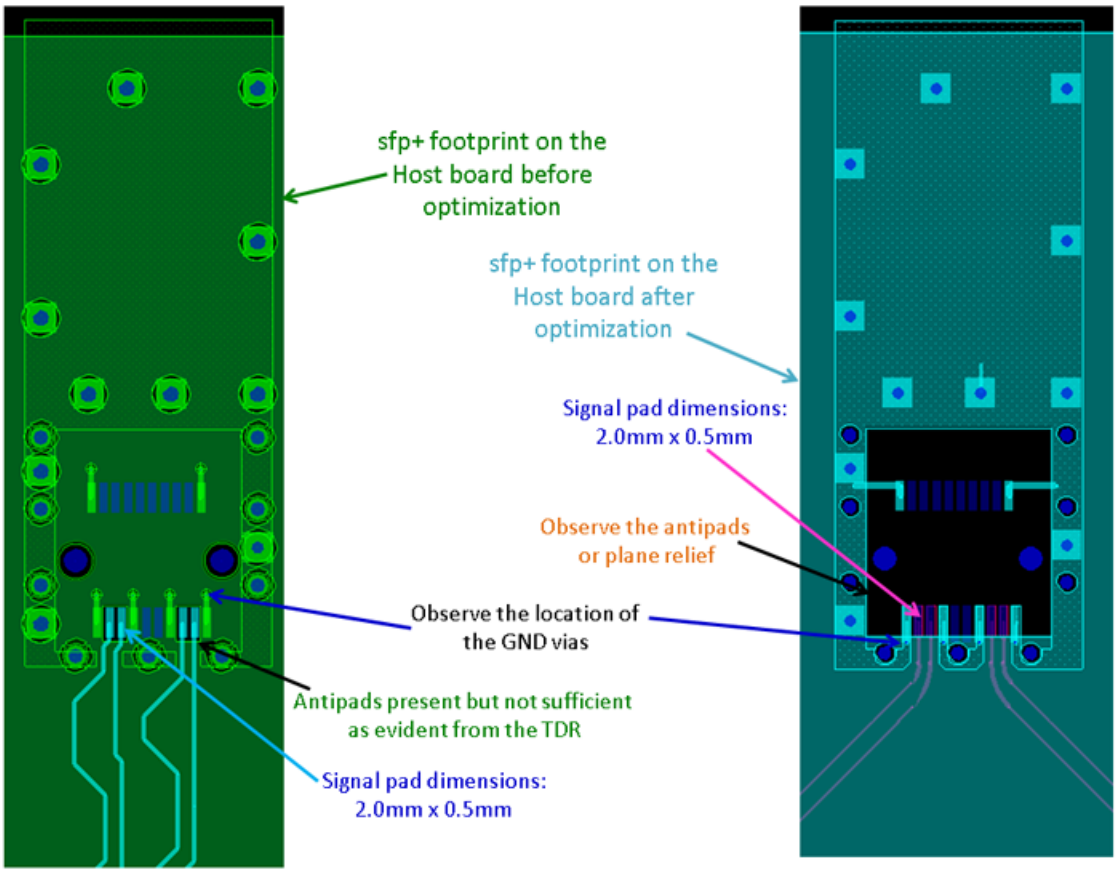
- The impedance discontinuity in TDR reduced from ~20Ω to ~5Ω after the interface is optimized.
- The differential-mode insertion loss (SDD21) has a linear trend up to 25 GHz after optimization. Without optimization, the SDD21 degrades severely at higher order harmonics. Higher order harmonics help open the eye of the signal. Without them, the signal would be sinusoidal at best.

Optimization at the SFP+ Connector Interface

1. Eliminate excess capacitance at the host board:
   a. Smaller SMT pads of the host board
   b. Anti-pads or PCB plane relief under the SMT pads of the host board
   c. Both the above optimizations are done using a 3D EM solver
   d. Note the entire black area at the right is cut out of the reference plane

Figure 17: SFP+ Footprint at the Host Board Before and After Optimization

Pad dimensions are within the dimensions mentioned in SFF-8431 specification section 3.5.

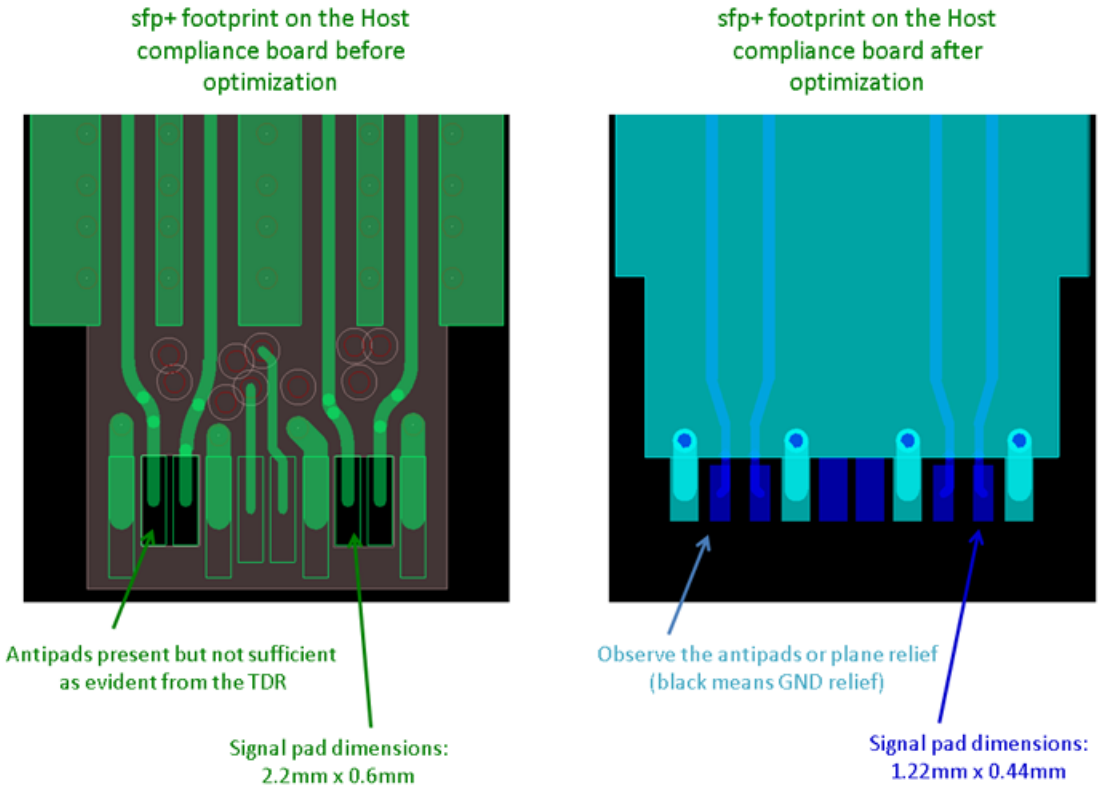


Note: The SFF-8431 specification section 3.5 states: "The solder pads for the high speed traces in the SFF-8431 Module Compliance Board are 1.1 x 0.4 mm to improve high frequency performance

instead of 2.0 x 0.5 mm as defined in the SFF-8083 for improved manufacturability. Trade-offs between host performance and manufacturability are left to the host designer."

2. Eliminate excess capacitance at the HCB:
   a. Smaller SMT pads of the Host Compliance board
   b. Anti-pads or PCB plane relief under the SMT pads of the host board
   c. Both optimizations above are done using a 3D EM solver

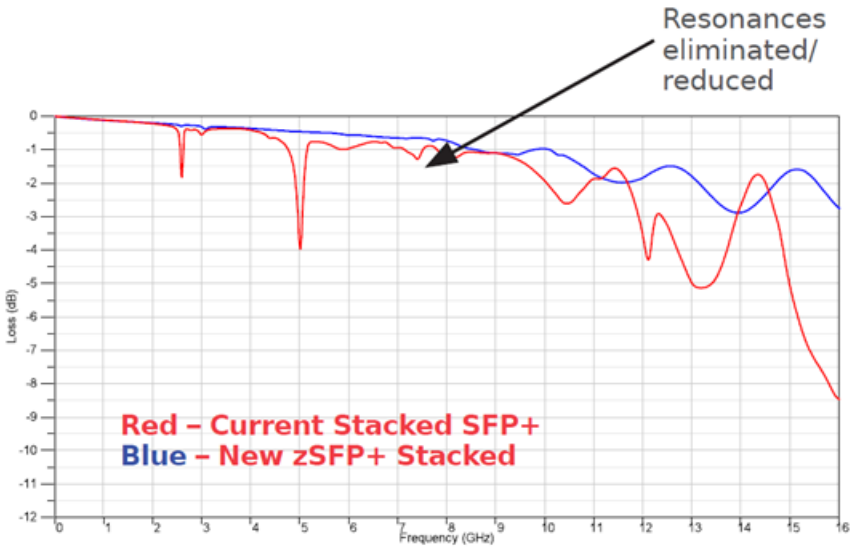
Figure 18: SFP+ Footprint at the HCB Before and After Optimization



3. Use of the Molex zSFP+ connector, which has improved SDD21 insertion loss curve compared to the Molex SFP+ connector.

Figure 19: Insertion Loss Comparison of Molex SFP+ and Molex zSFP+ Connector

Picture courtesy of Molex.



Related Information

- **Molex SFP+ connector PN: 0744410001**
- **Molex zSFP+ connector PN: 1703820002**

Recommendations for the SFP+ Connector Interface

- To lower excess capacitance:
  - Use smaller SMT pads for the high speed differential signals on the host PCB side and host compliance PCB side
  - Place anti-pads or PCB plane relief under the SMT pads
  - Use trace width optimization for the signals before the pads of the interface
  - Consider the location of the shorting GND vias
- Use an improved connector such as the Molex zSFP+ connector (Molex PN: 1703820002), which has an improved insertion loss curve as compared to the Molex SFP+ connector (Molex PN: 0744410001).
- Run 3D EM simulations on your design because the footprint is highly dependent on host board stackup, trace widths, the connector used, and the HCB used.

Related Information

- **Molex zSFP+ connector**
- **Molex zSFP+ connector Datasheet**

Document Revision History

The revision history for this document

Table 4: Document Revision History

Date	Version	Changes
July 2013	2013.07.10	Updated the *Recommendations for the SFP+ Connector Interface* section.
June 2013	2013.06.28	Initial release.