

# ESD7016, SZESD7016

## ESD Protection Diode

### Low Capacitance, USB 3.0

The ESD7016 surge protection is specifically designed to protect USB3.0 interfaces by integrating two Superspeed pairs, D+, D-, and Vbus lines into a single protection product. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines.

#### Features

- Low Capacitance (0.15 pF Typical, I/O to GND)
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

#### Typical Applications

- USB 3.0

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	$T_J$	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature - Maximum (10 Seconds)	$T_L$	260	$^\circ\text{C}$
IEC 61000-4-2 Contact (ESD)	ESD	$\pm 15$	kV
IEC 61000-4-2 Air (ESD)	ESD	$\pm 15$	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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#### MARKING DIAGRAM



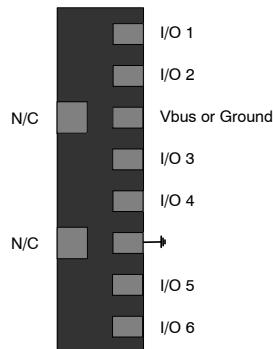
6M = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN CONFIGURATION AND SCHEMATIC



#### ORDERING INFORMATION

Device	Package	Shipping
ESD7016MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel
SZESD7016MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel

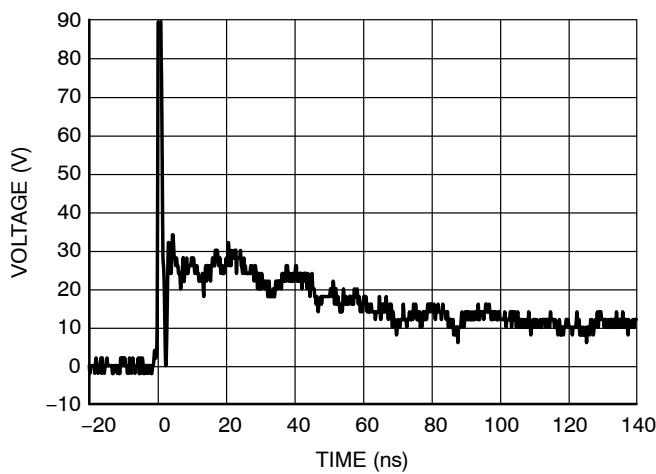
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# ESD7016, SZESD7016

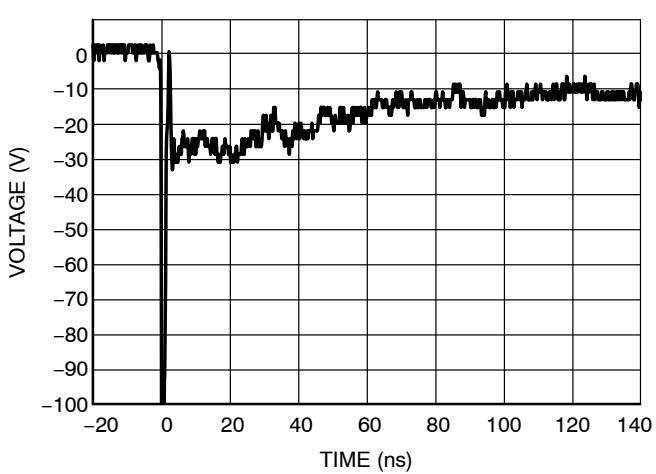
## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	I/O Pin to GND			5.0	V
Breakdown Voltage	$V_{BR}$	$I_T = 1 \text{ mA}$ , I/O Pin to GND	5.5			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5 \text{ V}$ , I/O Pin to GND			1.0	$\mu\text{A}$
Clamping Voltage (Note 1)	$V_C$	$I_{PP} = 1 \text{ A}$ , I/O Pin to GND (8 x 20 $\mu\text{s}$ pulse)			10	V
Clamping Voltage (Note 2)	$V_C$	IEC61000-4-2, $\pm 8 \text{ kV}$ Contact	See Figures 1 and 2			V
Clamping Voltage TLP (Note 3) See Figures 6 through 9	$V_C$	$I_{PP} = \pm 8 \text{ A}$ $I_{PP} = \pm 16 \text{ A}$		14.6 20.5		
Junction Capacitance	$C_J$	$V_R = 0 \text{ V}$ , $f = 1 \text{ MHz}$ between I/O Pins and GND		0.15	0.20	pF
Junction Capacitance Difference	$\Delta C_J$	$V_R = 0 \text{ V}$ , $f = 1 \text{ MHz}$ between I/O Pins and GND		0.03		pF

1. Surge current waveform per Figure 5.
2. For test procedure see Figures 3 and 4 and application note AND8307/D.
3. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 4 \text{ ns}$ , averaging window;  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .



**Figure 1. IEC61000-4-2 +8 KV Contact Clamping Voltage**



**Figure 2. IEC61000-4-2 -8 KV Contact Clamping Voltage**

# ESD7016, SZESD7016

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

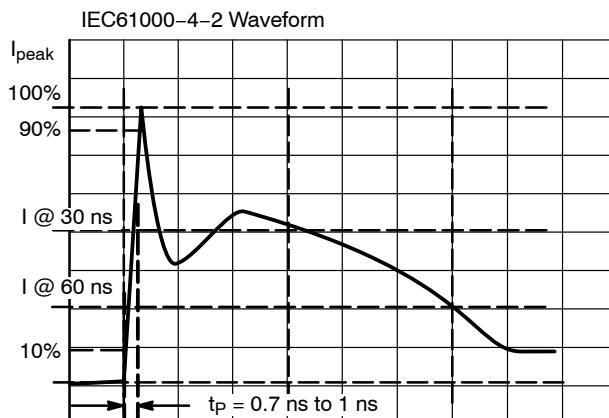


Figure 3. IEC61000-4-2 Spec

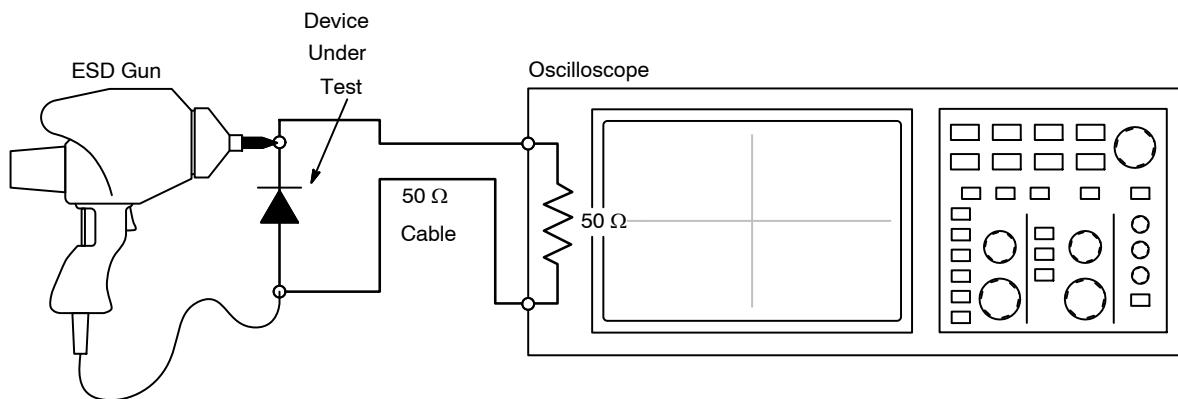


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D and AND8308/D.

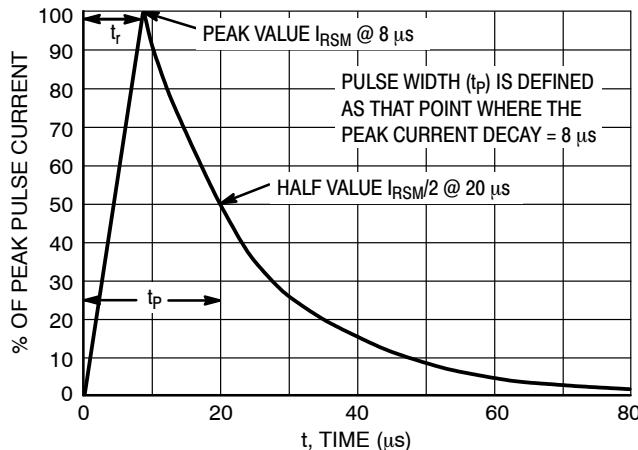
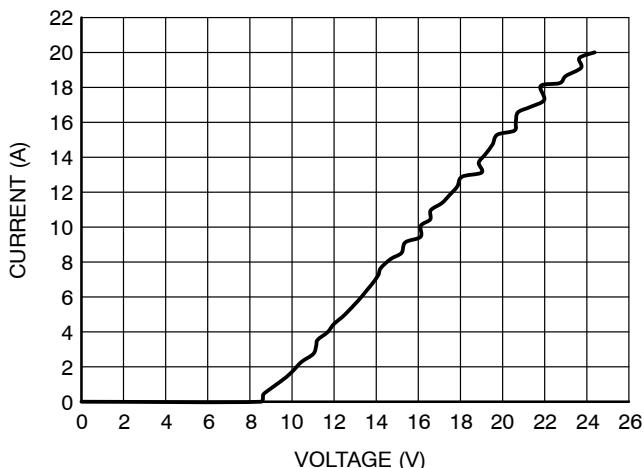
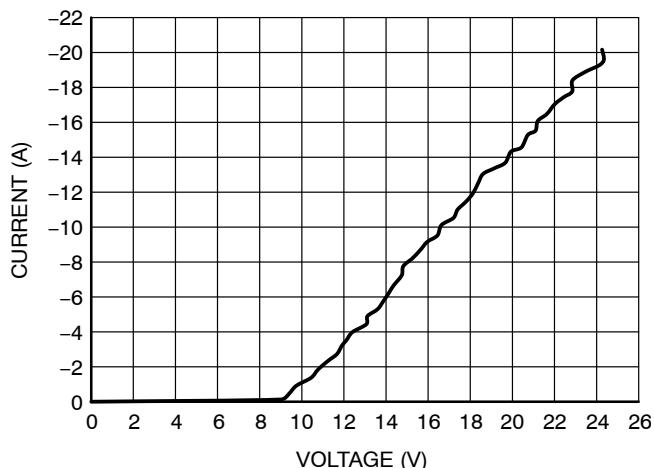


Figure 5. 8 x 20 μs Pulse Waveform

# ESD7016, SZESD7016



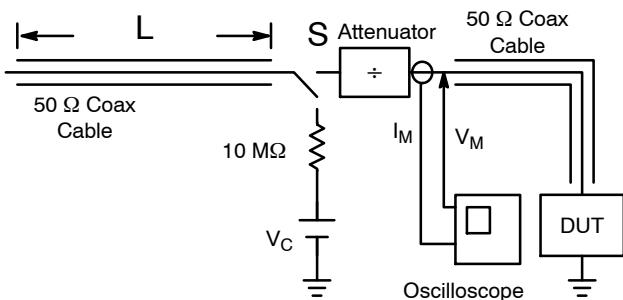
**Figure 6. Positive TLP I-V Curve**



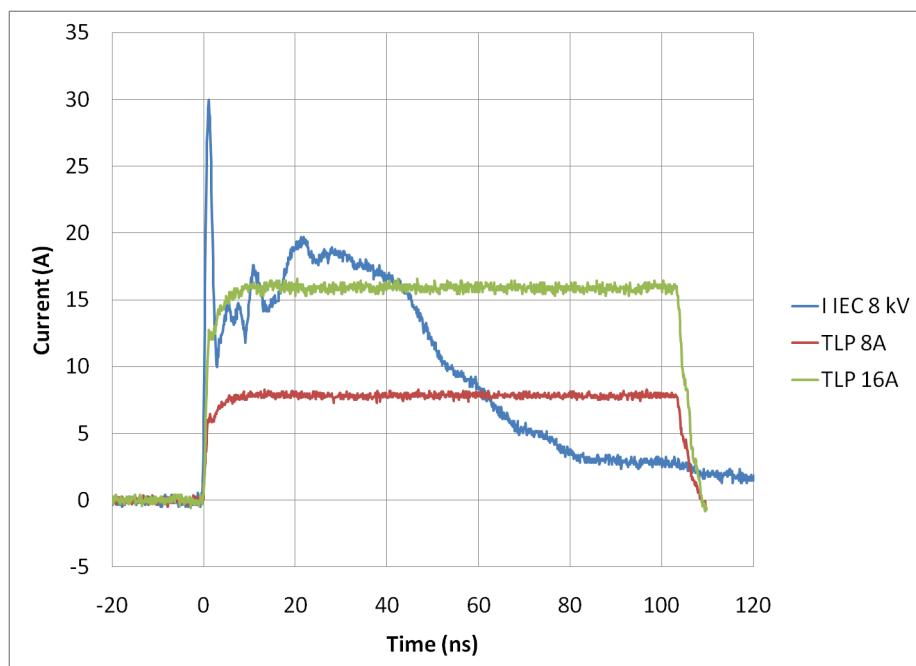
**Figure 7. Negative TLP I-V Curve**

## Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.



**Figure 8. Simplified Schematic of a Typical TLP System**



**Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms**

# ESD7016, SZESD7016

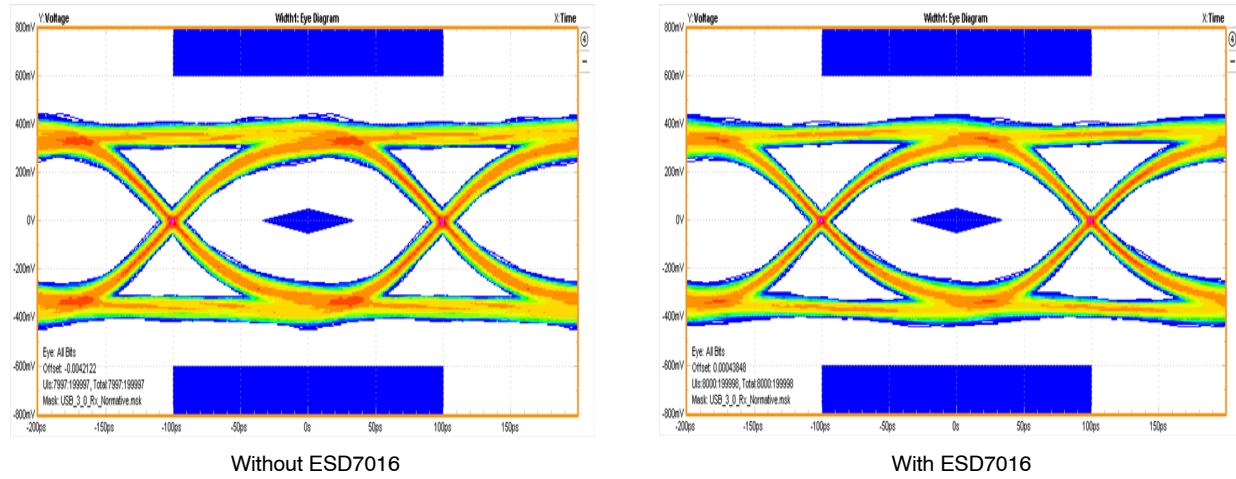


Figure 10. USB3.0 Eye Diagram with and without ESD7016, 5 Gb/s

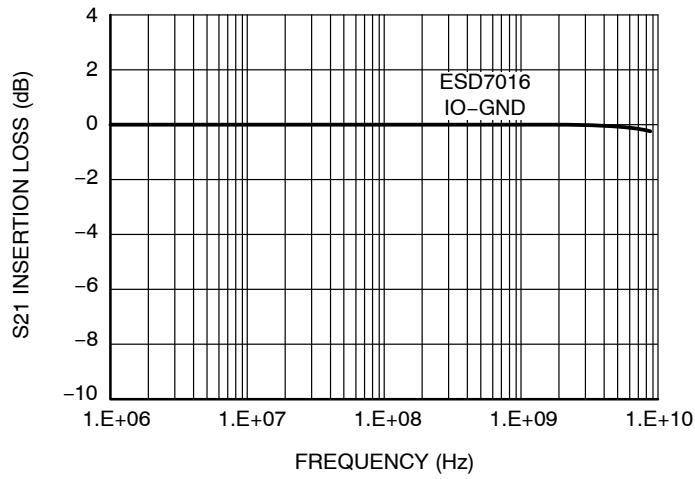
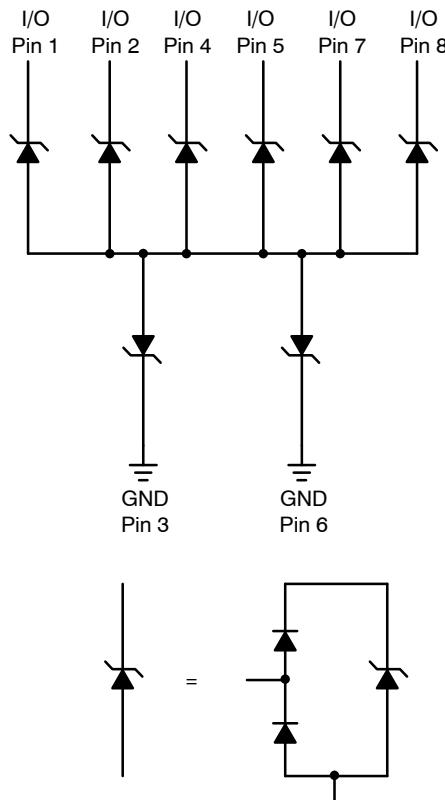
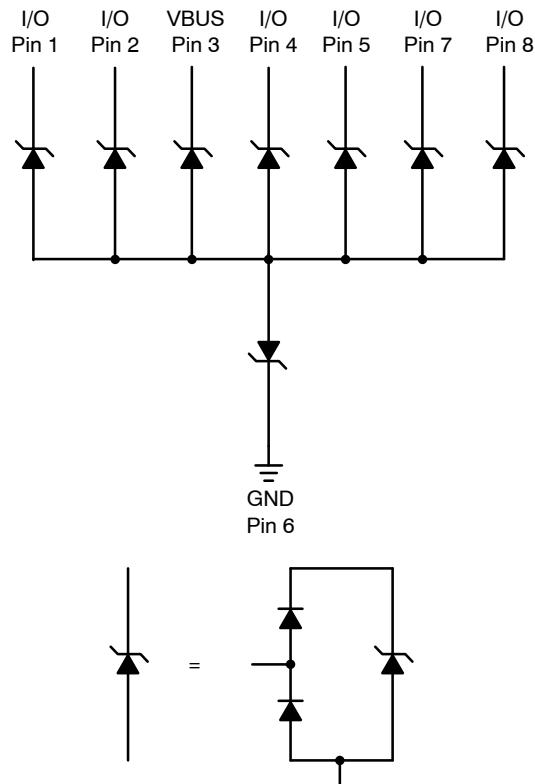
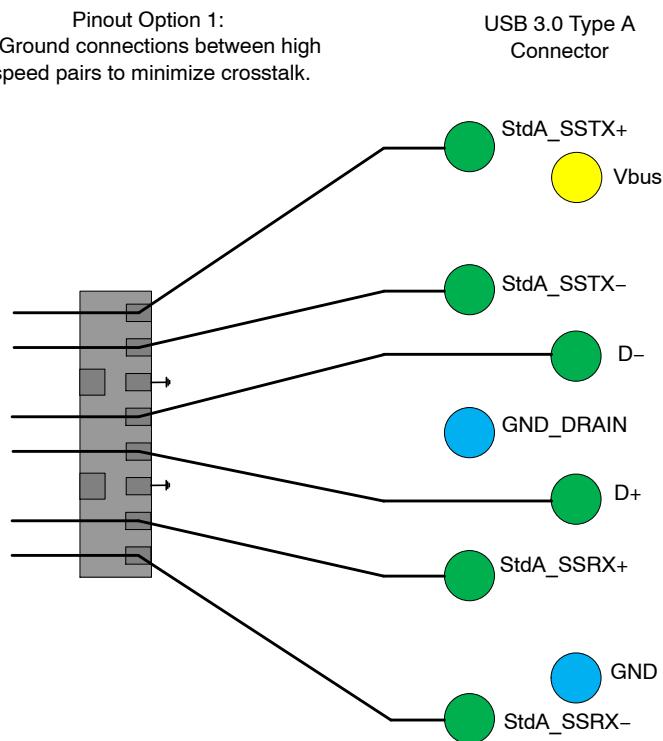


Figure 11. ESD7016 Insertion Loss

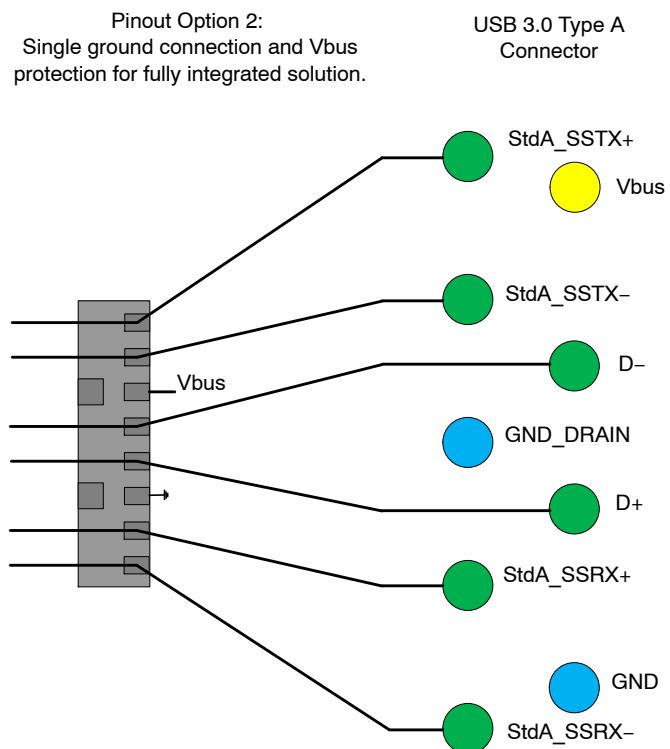
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Pinout Option 1:  
2 Ground connections between high speed pairs to minimize crosstalk.



Pinout Option 2:  
Single ground connection and Vbus protection for fully integrated solution.



**Figure 12. USB3.0 Type A Connector Layout Diagrams**

# ESD7016, SZESD7016

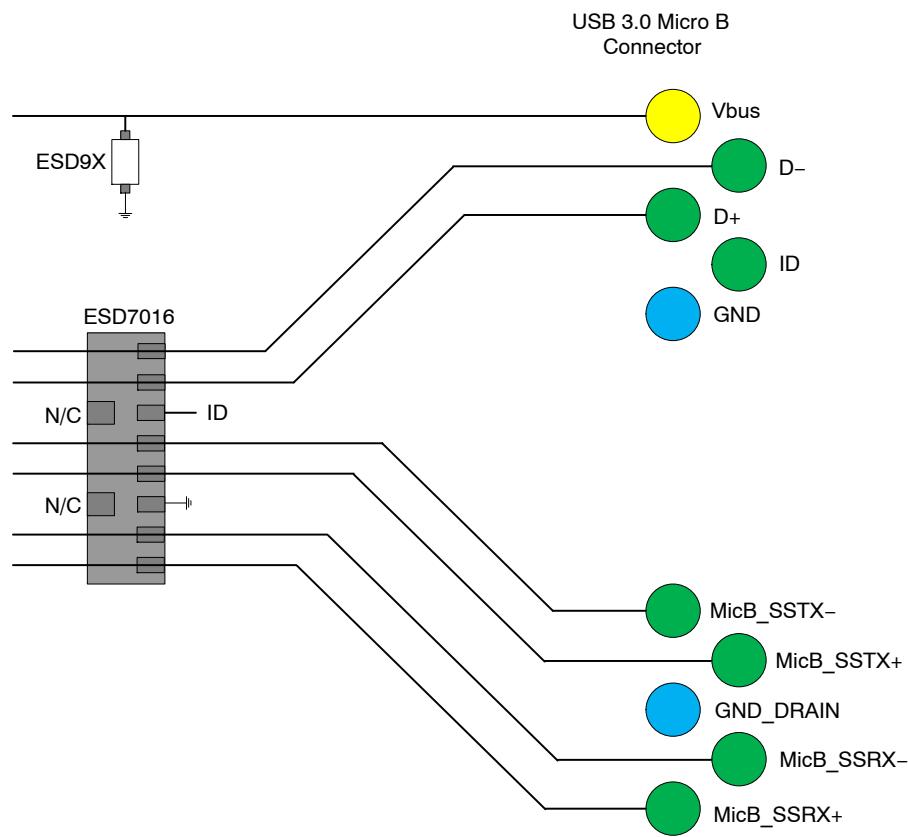


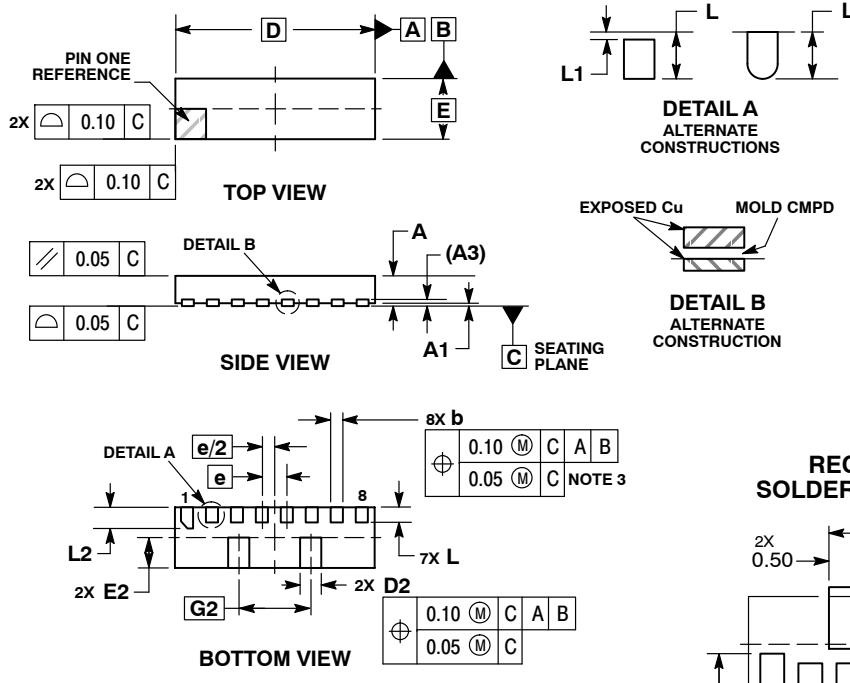
Figure 13. USB3.0 Micro B Connector Layout Diagram

## PACKAGE DIMENSIONS

UDFN8, 3.3 x 1.0, 0.4P

CASE 517CB

ISSUE O

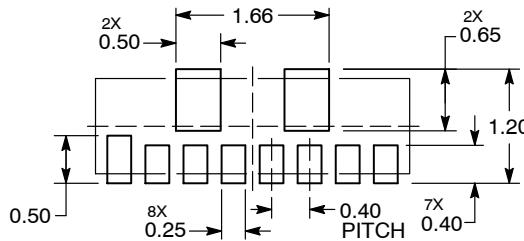


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.30 BSC	
D2	0.25	0.45
E	1.00 BSC	
E2	0.45	0.55
e	0.40 BSC	
G2	1.19 BSC	
L	0.20	0.30
L1	---	0.15
L2	0.30	0.40

## RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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