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N706-CB

Hardware User Guide

LTE Cat.1
Issue 1.1
Date 2023-01-16

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Notice

This document provides guide for users to use N706-CB.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to N706-CB.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2022-09	Initial draft	Shi Qin
1.1	2022-12	• Modified the N706-CB pad layout figure • Added the power consumption parameters • Added the ESD parameters • Added USIM1_DET Compatibility description	Shi Qin

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Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

Related Documents

Neoway_N706-CB_Product_Specifications

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1 Safety Recommendations

Ensure that this product is used in compliance with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or workplace:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, and so on.

  If the product is used in a place with flammable gas or dust such as propane gas, gasoline, or flammable spray, the product will cause an explosion or fire.

- Do not use this product in environments such as hospital or airplane where it might interfere with other electronic equipment.

  If the product is used in medical institutions or on airplanes, electromagnetic waves emitted by this product may interfere with surrounding equipment.

Follow the requirements below in design and use of the application for this module:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not insert/remove a SIM card or memory card into/from the module while it is not powered off.

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1 About N706-CB

N706-CB is an LTE industrial-grade cellular module developed based on Unisoc UIS8850, providing connectivity on FDD-LTE and TDD-LTE networks. With dimensions of (17.7±0.10) mm × (15.8±0.10) mm × (2.3±0.15) mm, the module supports rich hardware interfaces including audio, video, Wi-Fi scanning and optional GNSS function. It is suitable for developing IoT communication devices such as wireless meter reading terminals, handheld POS, industrial routers and so on.

N706-CB has the following features:

- ARM Cortex-A5 processor, 500 MHz CPU clock speed, 32 KB I-cache and 32 KB D-cache.
- Supported network mode: LTE Cat.1
- Supported functional interfaces: PCM, USIM, UART, I2C, USB2.0, SPI, and ADC.

1.1 Product Overview

The following lists the frequency bands that N706-CB supports.

Table 1-1 DTR model and frequency band

Model	Region	Frequency band	GNSS[1]	Memory
N706-CB-01	Chinese mainland	FDD-LTE: B1, B3, B5, B8 TDD-LTE: B34, B39, B40, B41	Supported	RAM: 128 Mb ROM: 64 Mb
N706-CB-02	Chinese mainland	FDD-LTE: B1, B3, B5, B8 TDD-LTE: B34, B39, B40, B41	Not supported	RAM: 64 Mb ROM: 32 Mb

1.2 Block Diagram

N706-CB series modules include the following functional units:

- Platform chip unit

GNSS[1] optional configuration.

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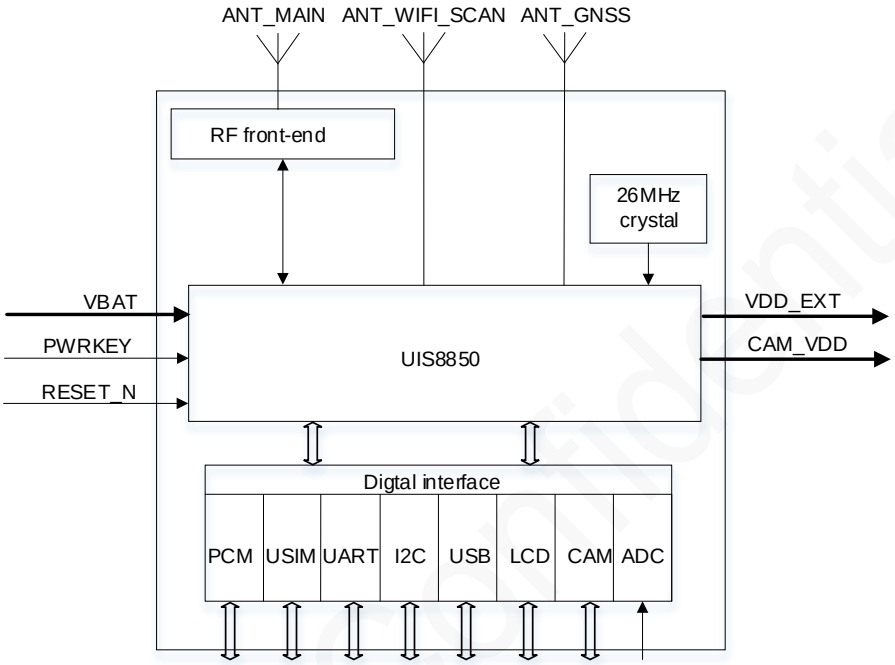
- Digital interface (PCM, USIM, UART, I2C, USB 2.0, SPI)
- Analog interface (ADC)

Figure 1-1 Block diagram



1.3 Basic Features

Features	Description
Physical features	Dimensions: (17.7 ± 0.10) mm × (15.8 ± 0.10) mm × (2.3 ± 0.15) mm Package: LCC+LGA (109 pins) Weight: TBD
Temperature ranges	Operating: -30°C to +75°C Extended*: -40°C* to +85°C* Storage: -40°C to +90°C
Operating voltage	VBAT: 3.4 V to 4.2 V, typical value: 3.8 V
Operating	PSM mode[22]: <40 uA

[2]: means the current drawn by the module in sleep mode, a low power consumption state, in which its RF function is functioning properly but its peripheral interfaces are disabled. If there is an incoming call or SMS, the module will exit from the sleep mode, and after the incoming call or voice instant messaging has ended, the module will re-enter the sleep mode.

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current	Idle mode[3]: <15 mA Operating mode[4]: <650 mA
Application processor	ARM Cortex- A5 processor, main frequency 500 MHz.
Frequency band	FDD-LTE: B1, B3, B5, B8 TDD-LTE: B34, B39, B40, B41
Wireless rate	FDD-LTE: Cat 1, Max 10 Mbps (DL)/Max 5 Mbps (UL) TDD-LTE: Cat 1, Max 8 Mbps (DL)/Max 2 Mbps (UL)
Application Interfaces	4G antenna, GNSS antenna, WLAN antenna. The characteristic impedance of each antenna is 50 Ω.
	Three UART interfaces with baud rates up to 115200 bps. Auto-bauding is enabled by default. MAIN_UART for AT communications. AUX_UART for CP-side log capturing. DBG_UART for AP-side log capturing.
	Two USIM interfaces, supporting 1.8 V/3 V USIM cards.
	One USB 2.0 interface, for slave mode only.
	Three SPI interfaces. One flash SPI; one LCD-dedicated SPI interface; one camera-dedicated SPI interface.
	Two 12-bit ADC interfaces, voltage detection range: 0.1 V - VBAT.
	Two I2C interfaces, for master mode only.
	One PCM interface
AT command	3GPP Release 13 Neoway extended AT commands
SMS	PDU, TXT
Data	PPP, RNDIS, ECM
Protocol	TCP, UDP, MQTT, FTP, HTTP/HTTPS, SSL, TLS
Certification approval	CCC*, SRRC*, RoHS*, CTA*

* means under development

[3]: means the current drawn by the module in a normal operating mode, but no data service is being processed.

[4]: means the current drawn by the module when there is data communications.

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2 Reference Standard

N706-CB is designed by referring to the following standards:

- 3GPP TS 36.521-1 V16.2.1 User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance Testing
- 3GPP TS 36.124 V16.1.0 ElectroMagnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V16.0.0 USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0 Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V17.0.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V17.0.0 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V17.0.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V16.0.0 Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

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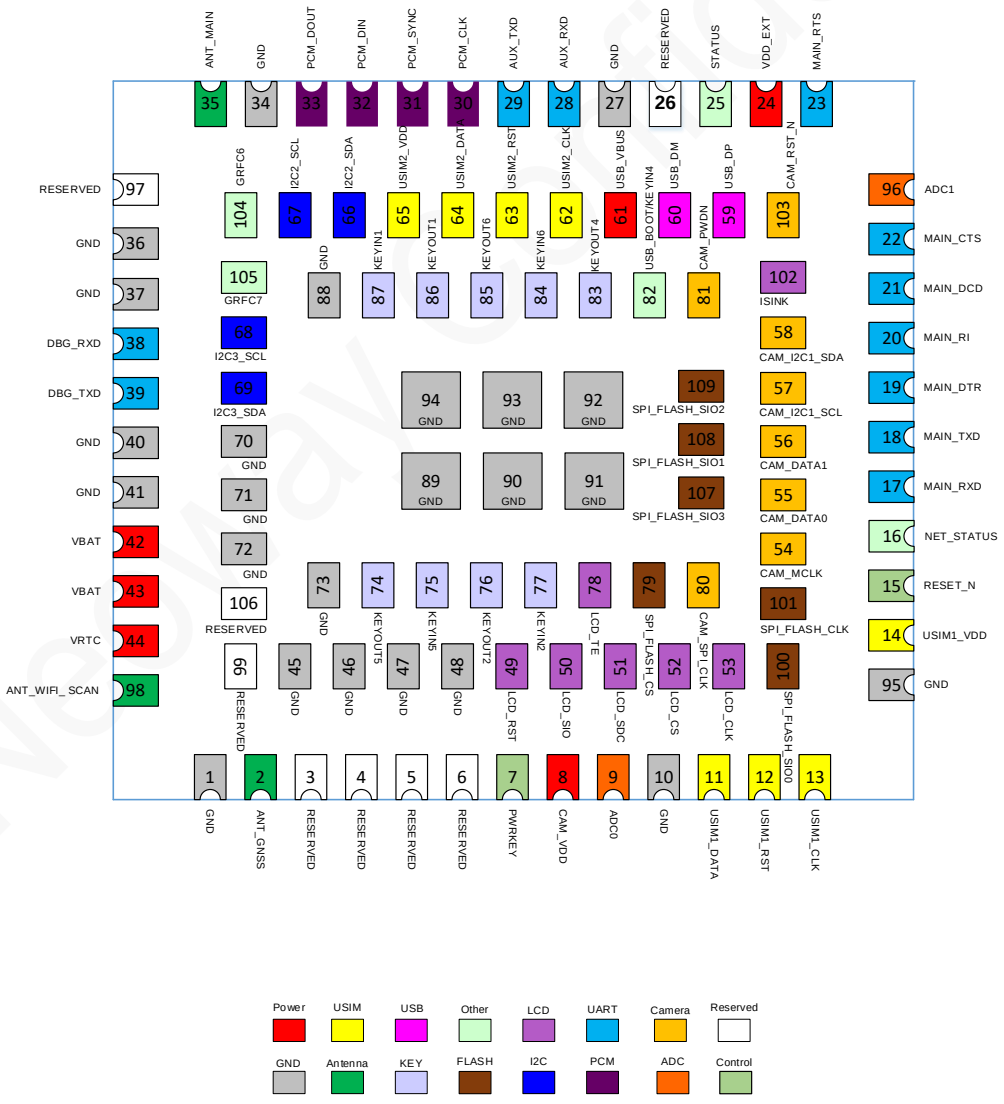
3 Pin Definitions

N706-CB modules are equipped with 109 pads, which are introduced in LCC+ LGA package.

3.1 Pin Definitions

The following figure shows the pad layout of N706-CB.

Figure 3-1 N706-CB pad layout (top view)



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3.2 Pin Description

The following table lists the IO types and DC characteristics.

Table 3-1 IO types and DC characteristics

IO type			
B	Digital input and output, CMOS logic level		
DO	Digital output, CMOS logic level		
DI	Digital input, CMOS logic level		
PO	Power output		
PI	Power input		
AO	Analog output		
AI	Analog input		
AIO	Analog input and output		
DC characteristics			
Interface type	Power domain	Logic level characteristics	
USIM	P1: Both 1.8 V and 3.0 V SIM types are supported. Activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented	1.8 V DC characteristics V_{IH}=0.7 x V_{DD_P1}~ V_{DD_P1} V_{IL}=0V~0.3 x V_{DD_P1} V_{OH}=0.9 x V_{DD_P1}~ V_{DD_P1} V_{OL}=0V~0.1 x V_{DD_P1}	3 V DC characteristics V_{IH}=0.7 x V_{DD_P1}~ V_{DD_P1} V_{IL}=0V~0.3 x V_{DD_P1} V_{OH}=0.9 x V_{DD_P1}~ V_{DD_P1} V_{OL}=0V~0.1 x V_{DD_P1}
GPIO	P2:1.8V	V_{IH}=0.7 x V_{DD_P2}~ V_{DD_P2} V_{IL}=0V~0.3 x V_{DD_P2} V_{OH}=0.9 x V_{DD_P2}~ V_{DD_P2} V_{OL}=0V~0.1 x V_{DD_P2}	

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Table 3-2 Pin description

Signal	Pin SN	I/O type	Function description	DC characteristics	Remarks
Power interface					
VBAT	42, 43	PI	Main power supply input	V_{min}=3.4 V V_{norm}=3.8 V V_{max}=4.2 V	The external power supply must ensure at least 2 A current.
VDD_EXT	24	PO	1.8 V power output	V_{norm}=1.8 V I_{max}=50 mA	IO interface, only used for voltage-level translation. Leave this pin open if unused.
VRTC	44	PI	RTC power supply	2.8 V - 3.2 V (typical value 3.0 V)	Internally connected to the real-time clock of the module. This interface can be connected to a button battery or farrar capacitor.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45, 46, 47, 48, 70, 71, 72, 73, 88, 89, 90, 91, 92, 93, 94, 95				Make sure all GND pins are grounded.
Control Interfaces					
PWRKEY	7	DI	Module on/off control	-	A low pulse for a valid time period can trigger on/off of the module (see section 4.2.1). This pin is pulled up to VBAT via a 20 kΩ resistor inside the main chip of the module.
RESET_N	15	DI	Module reset input	-	Active low This pin is pulled up to VBAT via a 20 kΩ resistor inside the main chip of the module.
UART interface					
MAIN_RXD	17	DI	Data input	P2	Software version (Standard): For

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MAIN_TXD	18	DO	Data output	P2	communication based on AT commands. Software version (Open): For data transmission.
MAIN_DTR	19	B	Data terminal ready	P2	
MAIN_RI	20	DI	Ring indicator	P2	
MAIN_DCD	21	DI	Carrier detect output	P2	
MAIN_CTS	22	DI	UART clear to send	P2	
MAIN_RTS	23	DO	UART ready to send	P2	
AUX_RXD	28	DI	UART data input	P2	AUX_UART for CP-side log capturing.
AUX_TXD	29	DO	UART data output	P2	
DBG_RXD	38	DI	UART data input	P2	DBG_UART is only used for Debug. Can be used to capture AP log.
DBG_TXD	39	DO	UART data output	P2	
USIM interface					
USIM1_DATA	11	B	USIM1 data	P1	This pin is pulled up to USIM1_VCC via a 4.7 kΩ resistor.
USIM1_RST	12	DO	USIM1 reset	P1	-
USIM1_CLK	13	DO	USIM1 clock	P1	-
USIM1_VDD	14	PO	USIM1 power	P1	-
USIM2_VDD	65	PO	USIM2 power	P1	-
USIM2_RST	63	DO	USIM2 reset	P1	-
USIM2_CLK	62	DO	USIM2 clock	P1	-
USIM2_DATA	64	B	USIM2 data	P1	This pin is pulled up to USIM2_VCC via a 4.7 kΩ resistor.

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USB interface					
USB_VBUS	61	PI	USB power supply	4.75 V - 5.25 V, typical value: 5 V	-
USB_DP	59	AIO	USB data +	-	Route the DM and DP traces as differential pairs with 90 Ω impedance.
USB_DM	60	AIO	USB data -	-	
ADC interface					
ADC0	9	AI	General A/D interface	-	12-bit, detectable voltage range: 0.1 V - VBAT. Leave this pin open if unused.
ADC1	96	AI	General A/D interface	-	12-bit, detectable voltage range: 0.1 V - VBAT. Leave this pin open if unused.
I2C Interface					
I2C2_SDA	66	B	I2C data	P2	Pulling this pin up to VDD_EXT is required.
I2C2_SCL	67	DO	I2C clock	P2	Pulling this pin up to VDD_EXT is required.
I2C3_SDA	69	B	I2C data	P2	Pulling this pin up to VDD_EXT is required.
I2C3_SCL	68	DO	I2C clock	P2	Pulling this pin up to VDD_EXT is required.
PCM interface					
PCM_CLK	30	DO	PCM data clock	P2	-
PCM_SYNC	31	DO	PCM data frame	P2	-

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			synchronization		
PCM_DIN	32	DI	PCM data input	P2	-
PCM_DOUT	33	DO	PCM data output	P2	-
LCD interface					
LCD_SDC	51	DO	SPI data or command control	P2	-
LCD_SIO	50	B	SPI data input/output	P2	-
LCD_CS	52	DO	SPI chip select signal of the slave device	P2	-
LCD_CLK	53	DO	SPI clock	P2	-
LCD_RST	49	DO	LCD reset	P2	-
LCD_TE	78	DO	LCD data frame synchronization	P2	-
ISINK	102	PI	LCD sink current input pin, used to adjust backlight brightness.		Connect this pin to the cathode of an LCD and its brightness is adjusted by a sink current. Imax = 81 mA.
FLASH interface					
SPI_FLASH_CS	79	DO	SPI FLASH chip select	P2	-
SPI_FLASH_CLK	101	DO	SPI FLASH clock	P2	-
SPI_FLASH_SIO0	100	B	SPI FLASH data 0	P2	
SPI_FLASH_SIO1	108	B	SPI FLASH data 1	P2	
SPI_FLASH_SIO2	109	B	SPI FLASH data 2	P2	
SPI_FLASH_SIO3	107	B	SPI FLASH data 3	P2	

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CAM interface					
CAM_VDD	8	PO	CAM analog power	V_{min}=1.61 V V_{norm}=1.8 V V_{max}=3.2 V	This analog power is disabled by default. If enabled, the default output is 1.8 V / 100 mA.
CAM_PWDN	81	DO	CAM power-down control	P2	Leave this pin open if unused.
CAM_DATA0	55	B	CAM SPI data 0	P2	Camera-dedicated SPI interface
CAM_DATA1	56	B	CAM SPI data 1	P2	
CAM_SPI_CLK	80	DO	CAM SPI clock	P2	
CAM_RST_N	103	DO	CAM reset	P2	-
CAM_MCLK	54	DO	CAM clock signal	P2	-
CAM_I2C1_SCL	57	DO	CAM I2C clock		
CAM_I2C1_SDA	58	B	CAM I2C data		
Antenna Interfaces					
ANT_GNSS	2	AI	GNSS antenna	-	50 Ω impedance.
ANT_WIFI_SCAN	98	AI	WLAN antenna	-	50 Ω impedance.
ANT_MAIN	35	AIO	Main antenna	-	50 Ω impedance.
Matrix keypad interface					
KEYOUT5	74	DO	Matrix keypad output 5	P2	1.8 V voltage domain. Leave these pins unconnected if unused.
KEYIN5	75	DI	Matrix keypad input 5	P2	
KEYOUT2	76	DO	Matrix keypad output 2	P2	
KEYIN2	77	DI	Matrix keypad input 2	P2	
KEYOUT4	83	DO	Matrix keypad output 4	P2	

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KEYIN6	84	DI	Matrix keypad input 6	P2	
KEYOUT6	85	DO	Matrix keypad output 6	P2	
KEYOUT1	86	DO	Matrix keypad output 1	P2	
KEYIN1	87	DI	Matrix keypad input 1	P2	
Other functional interfaces					
STATUS	25	DO	Operating status indication	P2	Leave this pin open if unused.
NET_STATUS	16	DO	Network status indication	P2	Leave this pin open if unused.
USB_BOOT/ KEYIN4	82	DI	Emergency download control	P2	Ground this pin (or pull up this pin) and then power up the module to enter the USB emergency download mode.
GRFC6	104	DO	General RF control IO6	P2	General RF control IO Leave this pin open if unused.
GRFC7	105	DO	General RF control IO7	P2	
RESERVED	3, 4, 5, 6, 26, 97, 99, 106		Reserved pin	-	Reserved for future function expansion or functions not open to the user. There may be more than one pin named RESERVED, which may have different functions or definitions. Leave these RESERVED pins open.

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4 Application Interfaces

N706-CB provides the control, communications, peripherals, display, and RF interfaces to meet the functional requirements of customers in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

4.1 Power Interfaces

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin SN	I/O	Function description	Remarks
VBAT	42, 43	PI	Main power supply of the module	V_{min}=3.4 V V_{norm}=3.8 V V_{max}=4.2 V
VDD_EXT	24	PO	1.8 V power output	V_{norm}=1.8 V I_{max}=50 mA
VRTC	44	PI	RTC power supply	2.8 V - 3.2 V, typical value 3.0 V
GND	1, 10, 27, 34, 36, 37, 40, 41, 45, 46, 47, 48, 70, 71, 72, 73, 88, 89, 90, 91, 92, 93, 94, 95			Make sure all GND pins are grounded.

4.1.1 VBAT

The design of power supply includes two parts: schematic design and PCB layout.

Power Supply Design

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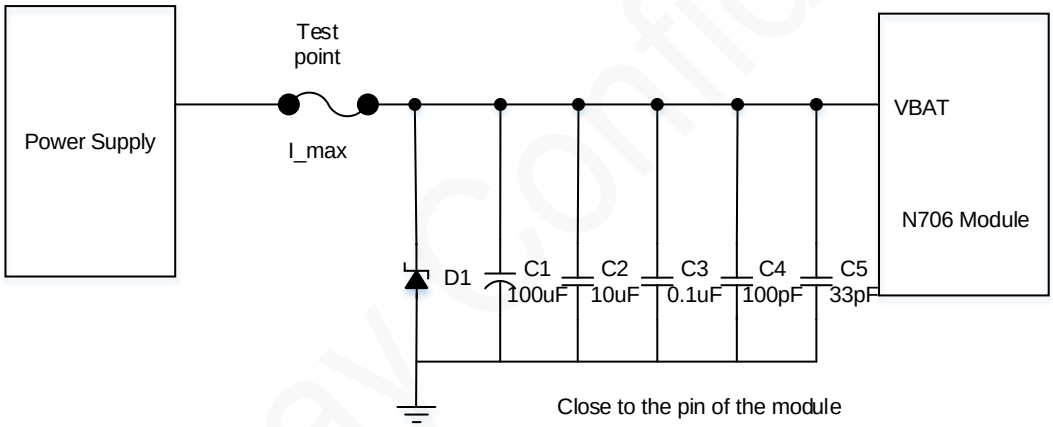
Never use a diode to make the voltage drop between a higher input and the module power supply. The forward voltage drop V_f of diode has two characteristics: one is that it increases with the increase of the forward current. the other is that it increases significantly at a low temperature. Note that, if there is an instantaneous high current, the above characteristics will lead to unstable operating voltage of the module, and even damage the module.

The power supply design of the N706-CB module depends on the input voltage of power supply. There are three power input types:

- 3.4 V - 4.2 V power input (typical value: 3.8 V, provided by a battery)
- 4.2 V - 5.5 V power input (typical value: 5.0 V, provided by a computer internal rectifier)
- 5.5 V - 24 V power input (typical value: 12 V, provided by system DC power for some industries such as automotive industry)

The design recommendations for 3.4 V - 4.2 V power input are as follows:

Figure 4-1 Recommended power supply design 1



- The maximum input voltage of the module power supply is 4.2 V, and the typical value is 3.8 V.
- In order to get a stable power source, it is recommended to select a TVS diode with suggested low reverse voltage (V_{RWM} 4.5 V) and peak power (Ppp = 2800 W (tp = 8/20 us)) at D1. Keep the placement of the TVS diode close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and modules.
- To decrease voltage drops during bursts, a large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1. Its maximum safe operating voltage should be larger than 2 times the voltage of the power supply.
- Keep the low ESR bypass capacitors (C2, C3, C4, C5) as close to the module as possible to filter out high-frequency interference in the power supply.

If it is necessary to control the power supply, the following circuit design is recommended:

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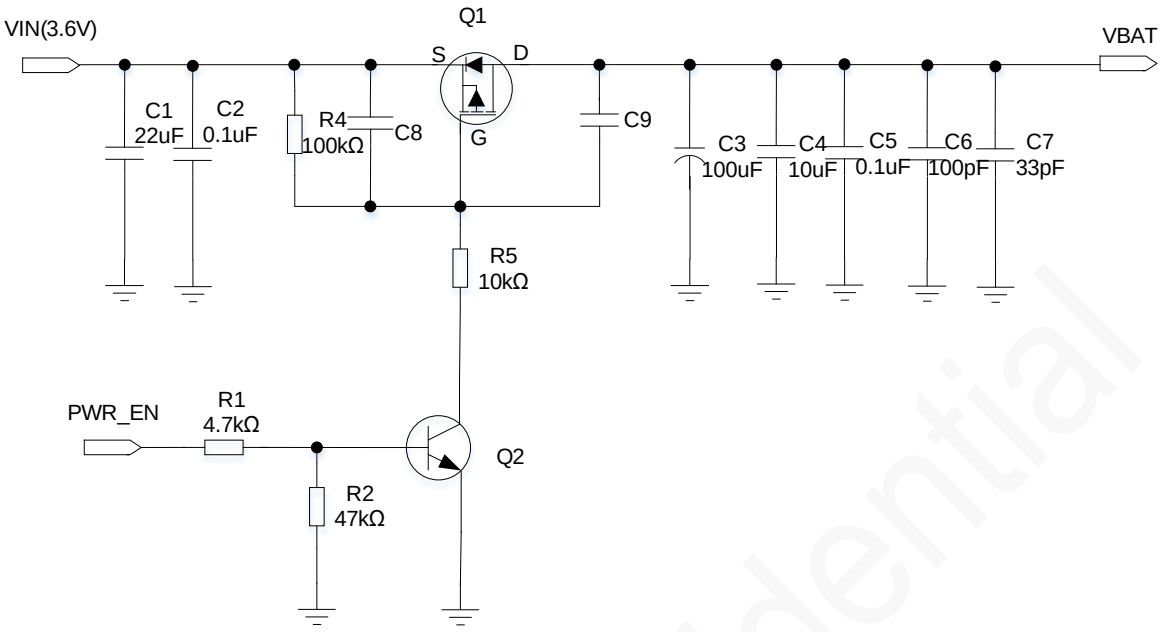
Figure 4-2 Recommended power supply design 2



- Select an enhanced P-MOSFET at Q1, of which the withstand voltage is high (V_{dss} = -12 V), drain current is high ($I_{D(MAX)}$ = -3.5 A) and RDS is low ($R_{ds(on)}$ = 108 mΩ).
- Select a common NPN transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which the break-over voltage on the base of the transistor increases at a low temperature; it is recommended that the value of R2 be at least 10 times that of R1.
- Keep the placement of C3 close to the module. Select a tantalum electrolytic capacitor with large capacitance (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) at C3 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be larger than 2 times the power supply voltage.
- Keep the low ESR bypass capacitors (C4, C5, C6, C7) as close to the module as possible to filter out high-frequency interference in the power supply.

The design recommendations for the 4.2 V - 5.5 V power input are as follows:

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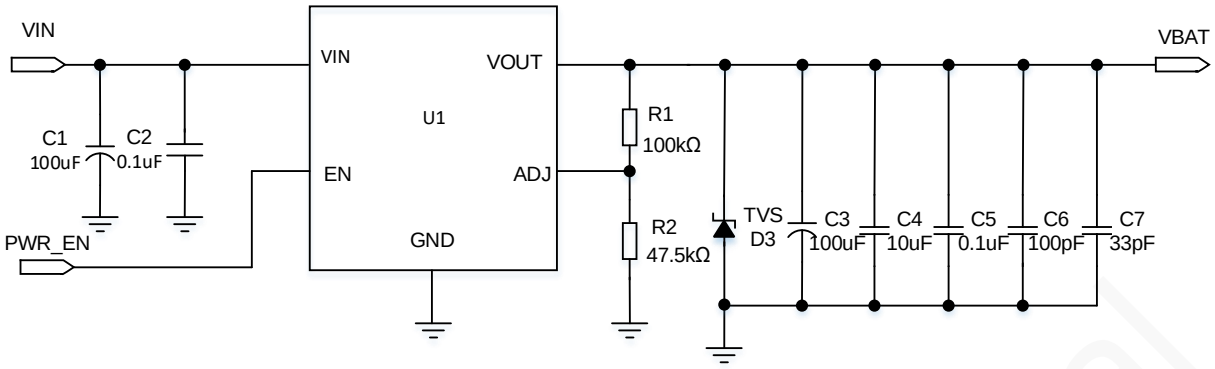
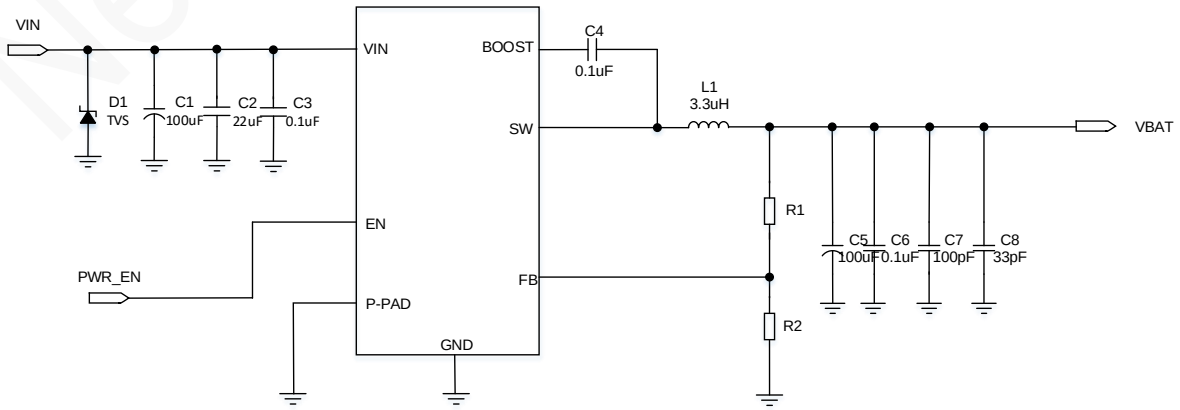
Figure 4-3 Recommended power supply design 3



- Design with LDO is simpler and more efficient when the output of power supply is close to the permissible voltage across VBAT.
- Select an LDO with maximum output current above 2 A at U1 to ensure the normal performance of the module.
- In order to get a stable power source, it is recommended to use a TVS diode with suggested low reverse voltage (V_{RWM} 4.5 V) and peak power (Ppp = 2800 W (tp = 8/20 us)) at D3. Keep the placement of the TVS diode close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and modules.
- Keep the placement of C3 close to the module. Select a large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) at C3 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be larger than 2 times the power supply voltage.
- Keep the low ESR bypass capacitors (C4, C5, C6, C7) as close to the module as possible to filter out high-frequency interference in the power supply.

The design recommendations for the 5.5 V - 24 V power input are as follows:

Figure 4-4 Recommended power supply design 4



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- If there is a high voltage drop between the power input and VBAT, a DC-DC design should be selected for higher efficiency, and the output current should be at least 2 A.
- Keep the TVS diode (D1) close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and modules.
- Keep the placement of C5 close to the module. Select a large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) at C3 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be larger than 2 times the power supply voltage.
- Keep the low ESR bypass capacitors (C6, C7, C8) as close to the module as possible to filter out high-frequency interference in the power supply.

When the module fails to be switched off normally due to abnormality, it is recommended to cut off the power first to shut down the module, and then power on again to restart the module.

PCB Layout

Place an ESR capacitor at the output of the power source to suppress the peak current. Place TVS diodes at the input end of the module to suppress voltage spikes and protect back-end devices. The circuit design is important, and the component placement and PCB routing are equally important. Several key points in power supply design are as follows:

- The TVS diode can absorb instantaneous high-power pulse, and withstand instantaneous pulse current peaks up to tens or even hundreds of amperes, with extremely short response time of voltage clamping. Keep the TVS diode as close to the the power input as possible, ensuring that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB traces.
- Place bypass capacitors as close as possible to the power supply pin of the module to filter out high-frequency noise signals in the power supply.
- For the main power circuit of the module, ensure that the PCB trace is wide enough that 2 A current can be safely passed, with no significant loop voltage drop. Keep the PCB trace width be at least 2 mm and ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make power traces short and wide.
- Keep noise-sensitive circuits, such as audio circuits and RF circuits far away from the power circuitry, especially when the DC-DC power supply is used.
- The voltage frequency of the SW pin of the DC-DC power supply is high, so the loop area should be minimized. Keep sensitive components far away from the SW pin of the DC-DC component to prevent noise coupling. Place feedback components as close as possible to the FB pin.
- The thermal-dissipation pads and GND pins of the DC-DC chip should be grounded to ensure good thermal dissipation and noise signal isolation.

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4.1.2 VDD_EXT

It is recommended to use VDD_EXT only for voltage-level translation and an ESD protector should be added.

N706-CB provides one VDD_EXT interface that supports 1.8 V voltage and up to 50 mA current. There is no output voltage at this pin in PSM mode.

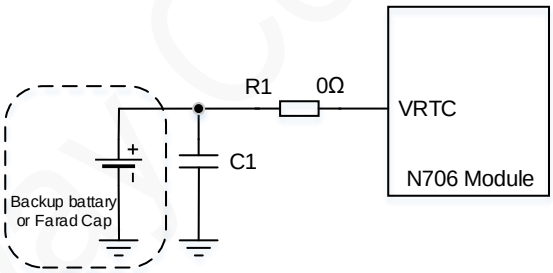
4.1.3 VRTC

VRTC is internally connected to the real-time clock of the module. The VRTC pin can be connected to a button battery or farrar capacitor to supply power for the real-time clock.

When the module is in normal operating mode (with a valid voltage applying at the VBAT), the typical output voltage of VRTC is 3.0 V and the maximum current is 2 mA. After the VRTC pin is connected to a button battery or farrar capacotor, the RTC inside the module can maintain a normal operation for a short time if the voltage at VBAT is disconnected. Leave this pin unconnected if unused.

The following shows the reference design of the VRTC power supply.

Figure 4-5 Reference design of the VRTC power supply



4.2 Control Interfaces

Signal	Pin SN	I/O	Function description	Remarks
RESET_N	15	DI	Module reset input	Active low
PWRKEY	7	DI	Module on/off control	Active low

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4.2.1 Module Power-on

Table 4-1 Power-on description

Notice / Power-on trigger method	Supported or not	Power-off method	Notice
Key	Supported	Press the power-on button for no less than 1.8s and then release it to switch off the module.	For example: When the module is in power-on mode, do not disconnect the power supply directly; otherwise, the flash inside the module will be damaged.
Pulse	Supported	Inputting low pulse (controlled by MCU) for not less than 1.8s can shut down the module.	
Auto power-on	Supported	Send the power-off AT command to the module and then disconnect its power source.	For example: When using AT commands to shut down the module, if the system is not powered down (power-down means not-powered mode), the module may start again after it is shut down.
USB startup	Supported	Disconnect the USB, send the power-off AT command to the module, and then power down it.	For example: When using AT commands to switch off the module, if the system is not powered down and the USB is still connected, the module may start again after power-off.

Power-on Controlled by PWRKEY

The following show two recommended reference designs of module startup:

- Figure 4-6 shows the reference design of push-button startup.

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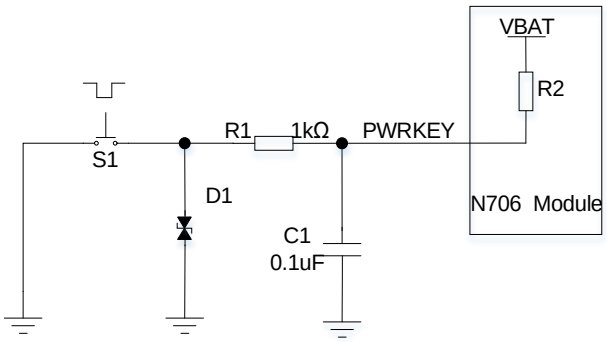
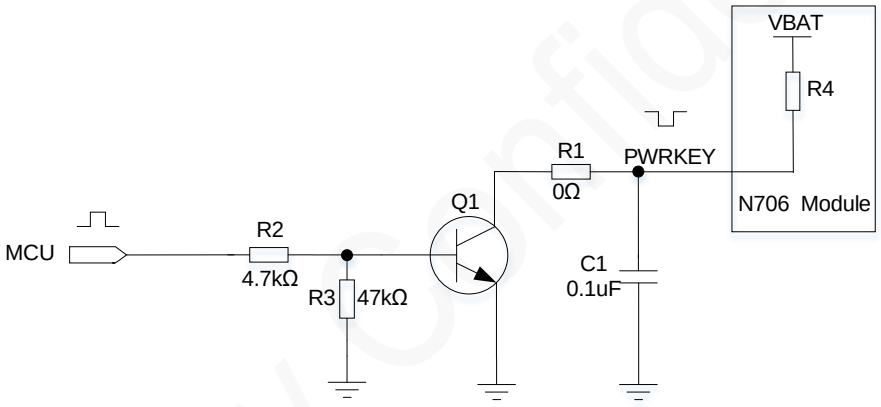
Figure 4-6 Reference design of push-button startup



- Figure 4-7 shows the reference design of module startup through an MCU

Figure 4-7 Reference design of MCU-controlled startup



Power-on process

To switch the module on, you can first apply a voltage at the VBAT module supply input and then input a low pulse for greater than 1.8s at PWRKEY. The AT function is available after 5 seconds. Do NOT connect an external resistor with large resistance in series to the PWRKEY pin (connecting a 1 kΩ resistor is recommended). Otherwise, the module cannot be switched on since the PWRKEY pin is at a high level all the time.

- Do Not perform other operations on the module until it is initialized completely since the states of each pin are uncertain if the initialization process has not been completed. Figure 4-8 shows the power-on process.

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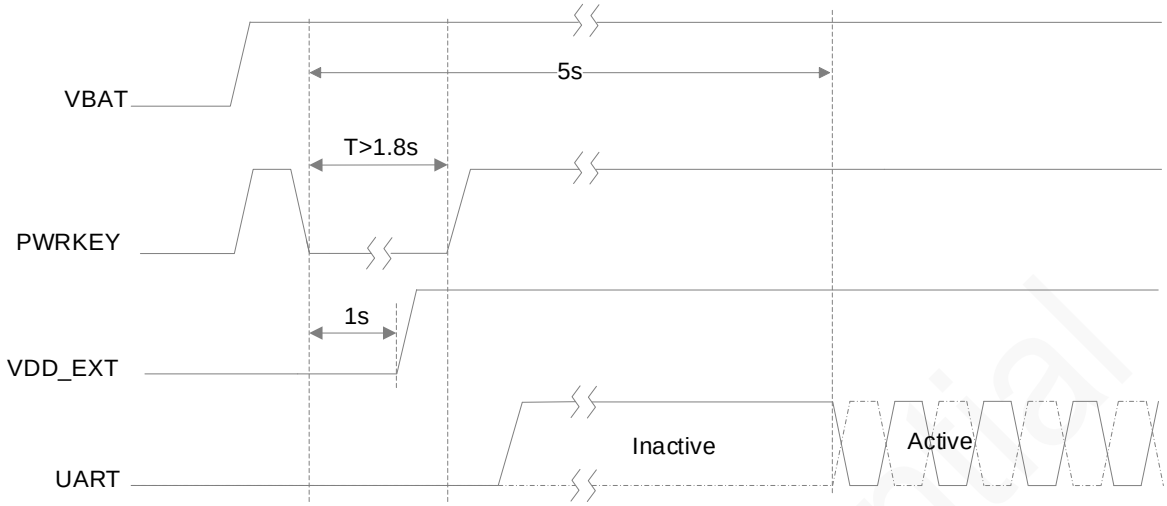
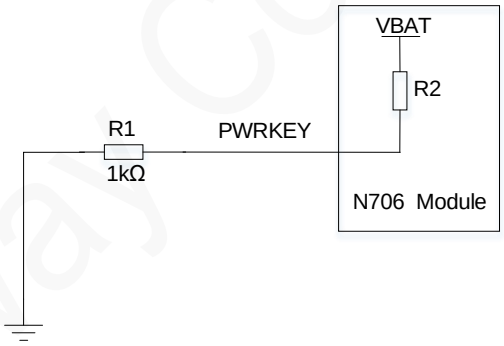
Figure 4-8 Power-on process



Auto Power-on

Figure 4-9 Reference design of automatic startup once powered up



If you implement the automatic startup function but the shutdown function is not required, you can directly pull PWRKEY down to ground. The recommended pull-down resistance is 1 kΩ.

4.2.2 Module Power-off

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When the module is in power-on mode, do not disconnect the power supply directly; otherwise, the flash inside the module will be damaged. It is strongly recommended that before disconnecting the power supply, you should switch off the module through PWRKEY or a dedicated AT command.

After the module is switched off using the dedicated AT command, ensure that PWRKEY is at a high level; otherwise, the module will switch on again after power-off.

Two methods are available to switch off the module: hardware shutdown and software shutdown

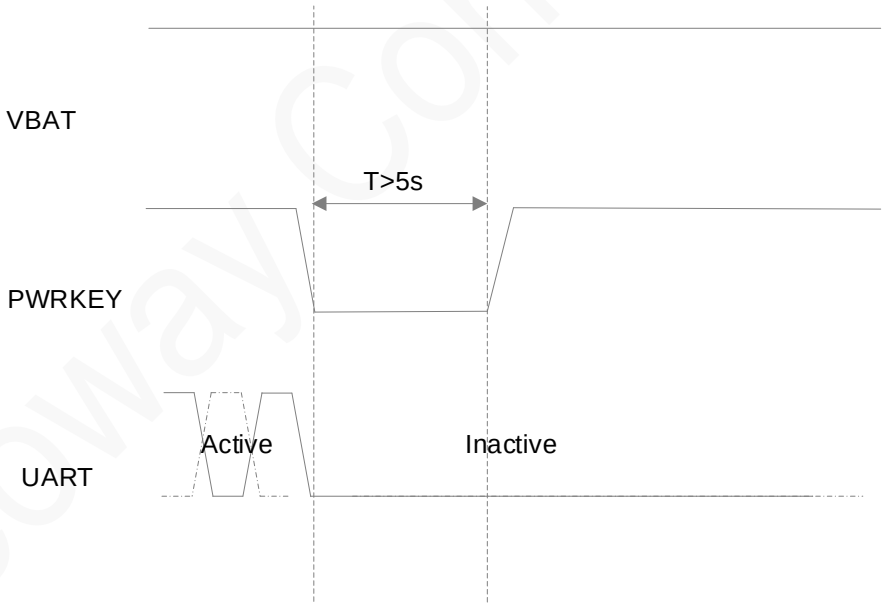
- Power-off controlled by PWRKEY (hardware power-off)
- Power-off controlled by AT command (software power-off)

Hardware Power-off via PWRKEY

PWRKEY is used to hardware power off the module. When the module is in power-on mode, inputting negative pulses at PWRKEY for more than 3 seconds can switch off the module.

The following figure shows the hardware shutdown process:

Figure 4-10 Hardware shutdown process of N706-CB



Software Power-off via AT Command

When the module is in power-on mode, to turn off the module, send it the power-off AT command. Whether the module is switched off by hardware or software method, their mechanisms are the same, that is, by applying a low level at the PWRKEY pin to switch off the module.

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For details, see *Neoway_N706_AT_Commands_Manual*.

4.2.3 Module Reset

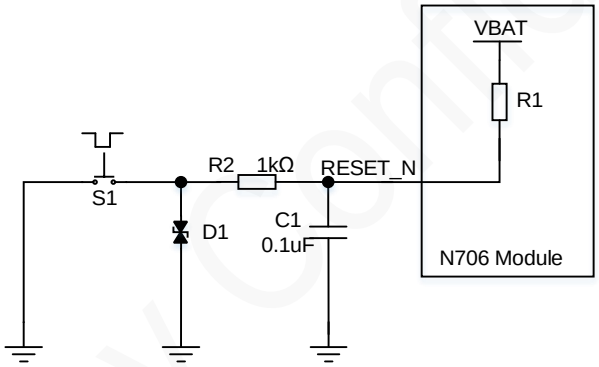
If the module encounters abnormalities such as system crash, you can reset the module system using the RESET_N pin to restore it. Therefore, it is strongly recommended to add a reset solution using the RESET_N pin when designing your PCB by referring to Figure 4-11 or Figure 4-12.

When the module is in power-on mode, inputting a low pulse at RESET_N for more than 50 ms can reset the module. For the module reset process, see Figure 4-11.

The following show two recommended reference designs of resetting N706-CB:

- Reference design of push-button reset

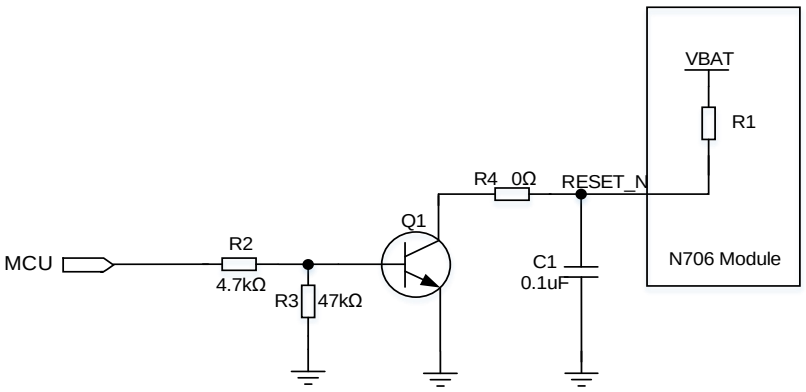
Figure 4-11 Reference design of push-button reset



- Reference design of MCU-controlled reset

  If you use a 1.8 V / 2.8 V / 3.0 V IO system, it is recommended to add a triode to for isolation. Refer to the following figure for specific design.

Figure 4-12 Reference reset circuit in which a triode is used for isolation



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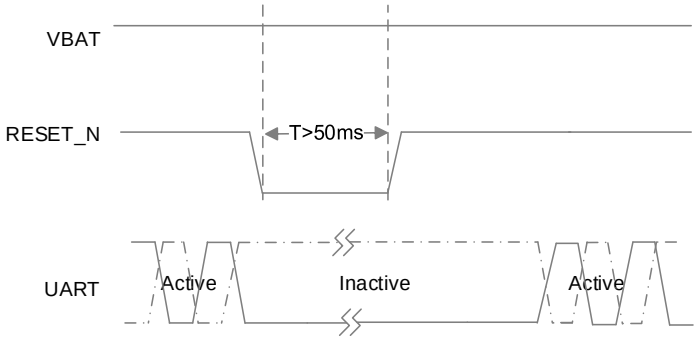
N706-CB module reset process is shown in the following figure.

Figure 4-13 Module reset process



4.3 Peripheral Interfaces

N706-CB provides a variety of peripheral interfaces.

In all reference designs in this section, the I/O direction indicated by the module peripheral interface pin name is based on the module, while the peripheral pin naming is based on the peripheral component itself. For example, UART_TXD of the module indicates the pin of the module for sending data, and MCU_RXD indicates the pin for MCU receiving data, so two pins should be connected.

In the process of MCU model selection and design, please check the pin naming is based on the module or MCU.

4.3.1 USB

The USB interface must be reserved for software debug.

Signal	Pin SN	I/O	Function description	Remarks
USB_VBUS	61	PI	USB power supply	4.75 V < USB_VBUS < 5.25 V, typical value: 5 V.
USB_DP	59	AIO	USB data +	-
USB_DM	60	AIO	USB data -	-

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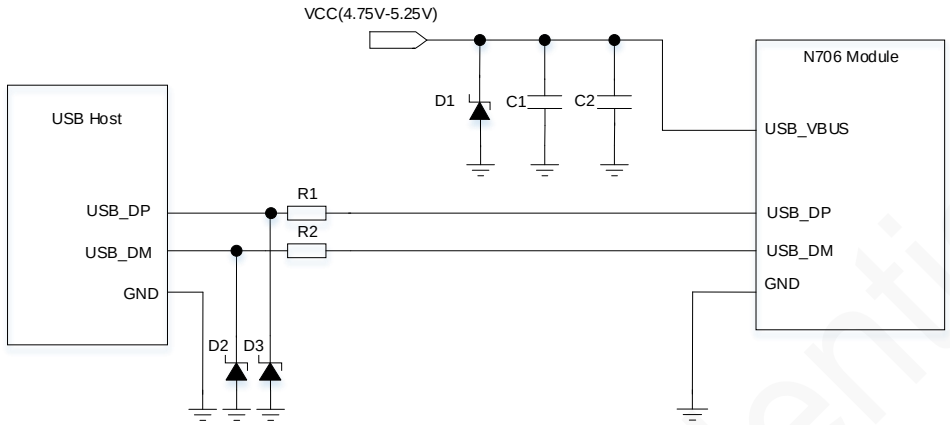
N706-CB can implement program download, data communications, and debugging through the USB interface. Only slave mode is supported for USB of the module, which can be used as required. The recommended USB connection circuit is shown in Figure 4-14.

Figure 4-14 Recommended design of the USB interface



Schematic Design Guidelines

- Connect a 1 μF (C1) and a 33 pF (C2) filter capacitors in parallel to the USB_VBUS trace. An additional component (D1) is needed at the USB_VBUS pin as ESD protection and its reverse working voltage V_{RWM} should be greater than 6 V.
- Ensure that the junction capacitance of the ESD components (D2 and D3) in parallel to the USB_DP and USB_DM traces be smaller than 0.5 pF.
- Resistors of less than 10 Ω are needed in series at the USB_DM and USB_DP pins (R1, R2) to effectively improve the ESD performance of the USB.

PCB Design Guidelines

- Place the filter capacitors (C1, C2) on the USB_VBUS traces as close to the module pins as possible, and place the ESD component (D1) as close to the USB connector as possible.
- Place the paralleled ESD component of the USB_DP and USB_DM traces (D2, D3) as close to the USB connector as possible.
- It is important to route USB signal traces as differential pairs with ground surrounded. The impedance of the USB differential traces should be 90 Ω. The traces from the port to the module must be isolated from other signal traces.

4.3.2 UART

Signal	Pin SN	I/O	Function description	Remarks
MAIN_RXD	17	DI	Data input	Software version (Standard): For communication based on AT
MAIN_TXD	18	DO	Data output	

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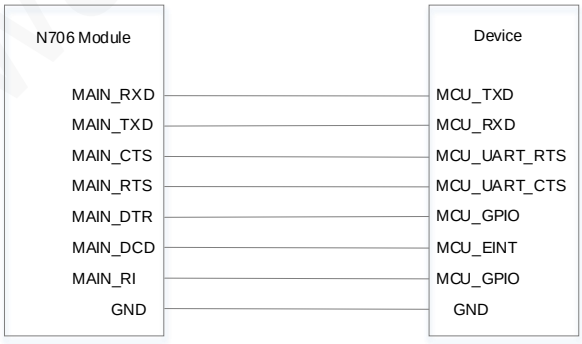
MAIN_DTR	19	B	Data terminal ready (main serial interface)	commands. Software version (Open): For data transmission.
MAIN_RI	20	DI	Ring indicator (main serial interface)	
MAIN_DCD	21	DI	Carrier detect output (main serial interface)	
MAIN_CTS	22	DI	Clear to send (main serial interface)	
MAIN_RTS	23	DO	Request to send (main serial interface)	
AUX_RXD	28	DI	UART data input	AUX_RXD can be used to capture CP-side log.
AUX_TXD	29	DO	UART data output	
DBG_RXD	38	DI	UART data input	DBG_RXD is use only for debugging. Can be used to capture AP log.
DBG_TXD	39	DO	UART data output	

N706-CB provides three UART interfaces, The UART supports a 1.8 V voltage and its default baud rate is 115200 bps. The following figure shows recommended design of the interface.

Figure 4-15 Reference design of the UART interface



Pulling down the MAIN_DTR pin can wake up the module.

When an event occurs and the module reports an URC, the RI pin will output a signal for notification.

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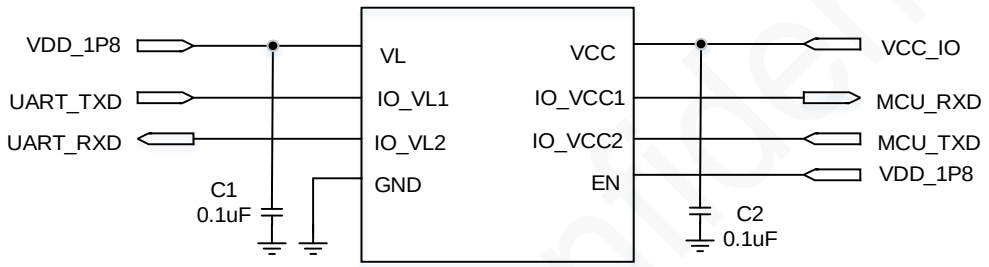
Schematic Design Guidelines

- Pay attention to the correspondence between signal flow direction and connection.
- It is prohibited to use diodes for voltage-level translation.

If the the logic voltage of UART does not match that of the MCU, add a voltage-level translation circuit outside the module. Three voltage-level translation circuits are recommended based on the differences in logic levels and rates.

- If the UART baud rate is greater than 115200 bps, it is recommended to design the voltage-level translation circuit by referring to the recommended voltage-level translation circuit 1. As shown in Figure 4-16.

Figure 4-16 Recommended voltage-level translation circuit 1



  - VL is the reference voltage for IO_VL1 and IO_VL2, and the voltage range is 1.5 V - 5.5 V.
  - VCC is the reference voltage for IO_VCC1 and IO_VCC2, and the voltage range is 1.5 V - 5.5 V.
  - EN is the enable pin, which works at a voltage of greater than VL-0.2 V. In the above circuit, the EN pin is connected to VDD_EXT and the voltage translator is always working.
- Dual-triode voltage-level translation circuit

  If the UART baud rate is less than or equal to 115200 bps, designing the TXD and RXD serial interfaces by referring to recommended voltage-level translation circuit 2 and designing the CTS and RTS serial interfaces by referring to recommended voltage-level translation circuit 3 are recommended. As shown in Figure 4-7 and Figure 4-7.

The actual parameter values of the components used in the voltage-level translation circuit should be adjusted according to the actual test results. Note the differences between different circuit voltage-level translation solutions.

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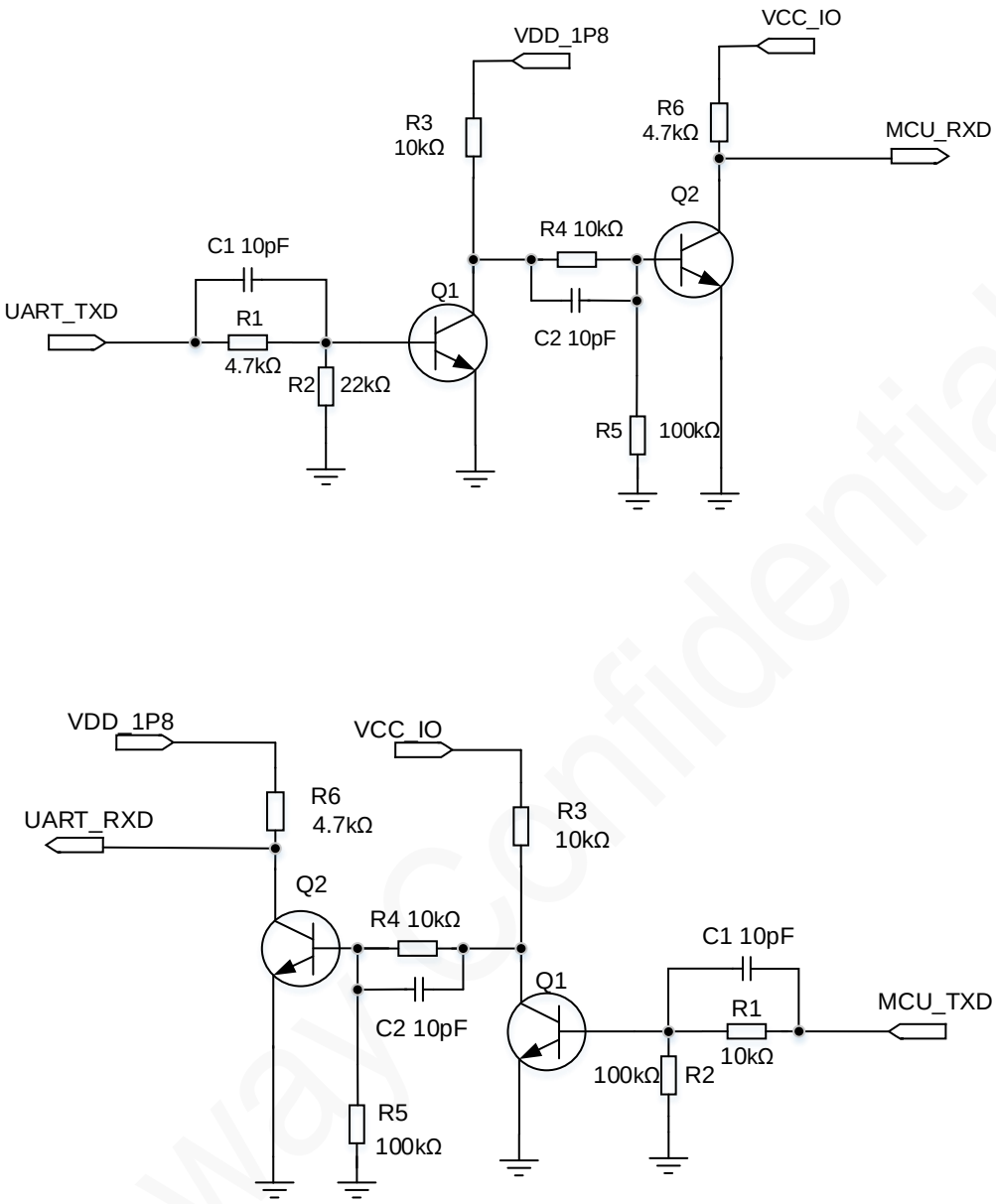
Figure 4-17 Recommended voltage-level translation circuit 2



MCU_TXD and MCU_RXD are the sending and receiving interfaces of MCU respectively, and UART_TXD and UART_RXD are the sending and receiving interfaces of module respectively. VCC_IO is the IO voltage of the MCU. VDD_EXT is the IO voltage of the module.

- Single-triode voltage-level translation circuit

  The circuit translates the voltage through the turn-on and turn-off of the triode, and dual triode can achieve higher pressure difference after voltage translation.

Schematic Design Guidelines

- Ensure that the base voltage of the triode is operating within the temperature range and the transistor can be fully turned on.

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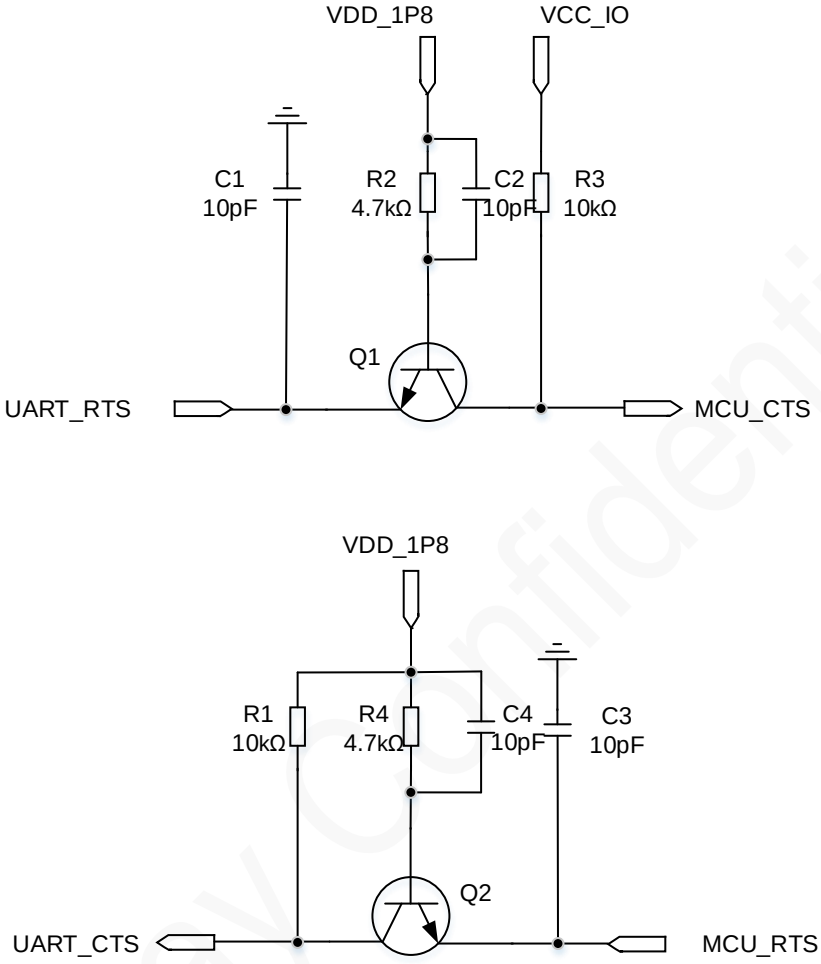
- It is recommended to reserve the acceleration capacitor, which can adjust the delay of the level conversion circuit in some cases.

Figure 4-18 Recommended voltage-level translation circuit 3



MCU_CTS and MCU_RTS are the MCU-side signals, while UART_CTS and UART_RTS are the module-side signals. VCC_IO is the IO voltage of the MCU. VDD_EXT is the IO voltage of the module.

This single-triode voltage-level translation circuit is a one-way translation solution that works by conduction and cutoff of the triode. Please note the signal flow direction.

Schematic Design Guidelines

- The voltage difference between the high level and low level does not exceed 2 V.
- It is recommended to reserve the speed-up capacitor and adjust its capacitance value according to actual test results.
- The transistor base voltage is the lower value of the level between both sides.

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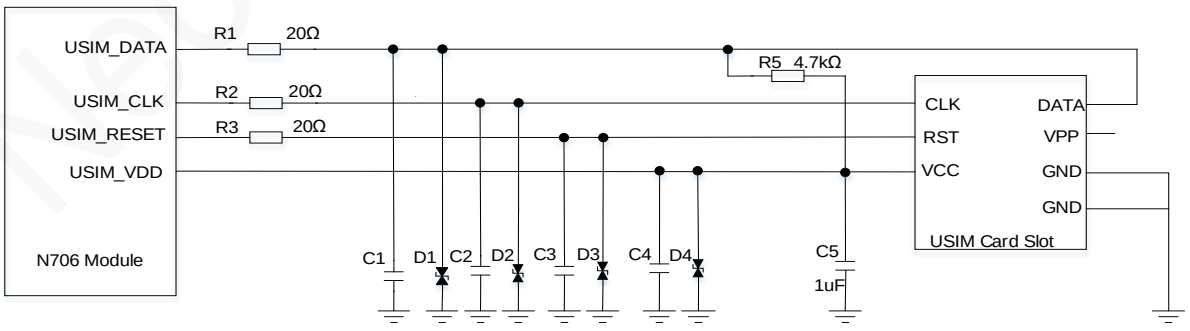
4.3.3 USIM

Signal	Pin SN	I/O	Function description	Remarks
USIM1_DATA	11	B	USIM1 data	This pin is pulled up to USIM1_VDD via a 4.7 kΩ resistor.
USIM1_RESET	12	DO	USIM1 reset	-
USIM1_CLK	13	DO	USIM1 clock	-
USIM1_VDD	14	PO	USIM1 power	Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented.
USIM2_VDD	65	PO	USIM2 power	Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented.
USIM2_RESET	63	DO	USIM2 reset	
USIM2_CLK	62	DO	USIM2 clock	-
USIM2_DATA	64	B	USIM2 data	This pin is pulled up to USIM2_VDD via a 4.7 kΩ resistor.

N706-CB provides two USIM card interfaces and supports dual-SIM single standby. USIM1 is used first by default. Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented. The reference schematic diagram of the USIM card interface is shown in Figure 4-19.

Figure 4-19 Reference design of USIM card interface (without hot-swap)



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Schematic Design Guidelines

- USIM_VDD is the power supply of the USIM card, with load capacity of up to 50 mA. It is only used as power supply for the USIM card and shall not supply power to other loads. Regulator capacitors and filter capacitors must be reserved and is in parallel to the VSIM_VDD pin (C4, D4). The recommended filter capacitance is 0.1 uF. It is recommended to select a regulator capacitor with capacitance greater than 1 uF (C5) in parallel to the VSIM_VDD trace.
- The USIM_DATA pin is not pulled up internally, so connecting it through a 4.7 kΩ external pull-up resistor to USIM_VCC is required.
- USIM_CLK is the clock signal pin for USIM card. In applications with complex electromagnetic environments that have high requirements for ESD protection, it is recommended to add ESD protection diodes (junction capacitance ≤ 7pF) on each signal trace or add an integrated TVS array.
- Resistors of no more than 20 Ω are needed in series at the USIM_DATA, USIM_RESET, USIM_CLK, and USIM_DET pins to enhance ESD performance. The resistors should be placed close to the USIM card slot.
- C1-C3 are in parallel to each USIM signal trace and are used to mount high-frequency filter capacitors. Their capacitance value should be not more than 33 pF. Please adjust it according to the actual debugging results.

The USIM1 interface of the module does not support the hot-swap function in principle. If you need to implement the function, KEYIN6 pin of the module needs to be compatible with the SIM card detection function, and a 47kΩ resistor is needed in series at the KEYIN6 pin to pull it up to 1.8 V. Meanwhile, the software must be compatible with the USIM hot-swap detection function.

PCB Design Guidelines

- USIM signals are like to be jammed by RF radiation, resulting in failure to detect the SIM card. The USIM should be kept far away from the antenna area and RF circuit area.
- Keep the USIM card connector close to the module and keep USIM traces as short as possible.
- On the USIM traces, connect the series resistors and ESD protection components close to the USIM card connector.
- To avoid cross-talk between USIM signal traces, surround them with ground.

4.3.4 I2C

Signal	Pin SN	I/O	Function description	Remarks
I2C2_SDA	66	B	I2C data	Connect this pin to VDD_EXT through a pull-up resistor.
I2C2_SCL	67	DO	I2C clock	Connect this pin to VDD_EXT

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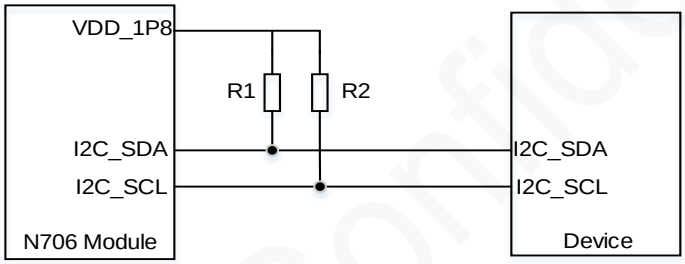
				through a pull-up resistor.
I2C3_SDA	69	B	I2C data	Connect this pin to VDD_EXT through a pull-up resistor.
I2C3_SCL	68	DO	I2C clock	Connect this pin to VDD_EXT through a pull-up resistor.

N706-CB provides two I2C interfaces with 1.8 V level, supporting only the master mode. Their transmission rates in standard mode and fast mode are respectively 100 Kbps and 400 Kbps. For the pull-up resistors, select a proper resistance based on the actual debugging result; it is recommended to select the resistance ranging from 1.8 kΩ to 10 kΩ. Figure 4-20 shows the reference design of the I2C interface.

Figure 4-20 Reference design of I2C interface



4.4 Audio Interfaces

N706-CB provides one 1.8 V digit PCM interface, which can be multiplexed as PCM interfaces.

Signal	Pin SN	I/O	Function description	Remarks
PCM_CLK	30	DO	PCM data clock	-
PCM_SYNC	31	DO	PCM data frame synchronization	-
PCM_DIN	32	DI	PCM data input	-
PCM_DOUT	33	DO	PCM data output	-

The following figure shows the PCM mode connection diagram.

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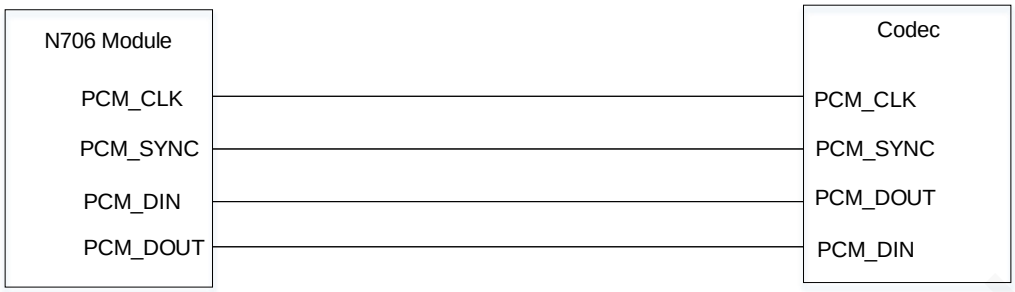
Figure 4-21 Reference design of the PCM interface



Schematic Design Guidelines

- If the logic levels between the N706-CB module and Codec do not match, you should add a voltage-level translation solution.

PCB Design Guidelines

- Avoid crossing of PCM signal traces with other traces. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the traces.
- Route PCM traces as far away as possible from areas where ESD may be introduced.

4.5 Video Interfaces

4.5.1 LCD

N706-CB provides an LCD-dedicated SPI interface, supporting frame rates up to QVGA @ 30fps for LCD display. The following shows the LCD interface pin description.

Table 4-2 LCD interface description

Signal	Pin SN	I/O	Function description	Remarks
LCD_SDC	51	DO	SPI data or command control	
LCD_SIO	50	B	SPI data input/output	
LCD_CS	52	DO	SPI chip select signal of the slave device	
LCD_CLK	53	DO	SPI clock	
LCD_RST	49	DO	LCD reset	
LCD_TE	78	DO	LCD data frame synchronization	-
ISINK	102	PI	LCD sink current input pin, used to adjust backlight brightness.	Connect this pin to the cathode of an LCD and

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				its brightness is adjusted by a sink current. Imax = 81 mA.

4.5.2 Camera

N706-CB provides a camera-dedicated SPI interface, supporting frame rates up to 0.3M@24fps for cameras. The following shows the camera interface description.

Table 4-3 Camera interface description

Signal	Pin SN	I/O	Function description	Remarks
CAM_VDD	8	PO	CAM analog power	This analog power is disabled by default. If enabled, the default output is 1.8 V / 100 mA.
CAM_PWDN	81	DO	CAM power-down control	-
CAM_DATA0	55	B	CAM SPI data 0	Camera-dedicated SPI interface
CAM_DATA1	56	B	CAM SPI data 1	
CAM_SPI_CLK	80	DO	CAM SPI clock	
CAM_RST_N	103	DO	CAM reset	-
CAM_MCLK	54	DO	CAM clock signal	
CAM_I2C1_SCL	57	DO	CAM I2C clock	
CAM_I2C1_SDA	58	B	CAM I2C data	

Schematic Design Guidelines

- Notably, CAM_VDD is an LDO output ranging from 1.61 V to 3.2 V (1.8 V by default), which is used to supply power cameras, with a maximum load capacity of 100 mA. Do Not use it for other loads. A filter capacitor must be reserved on the pin in design.

4.6 Other Functional Interfaces

4.6.1 ADC

The module provides two 12-bit ADC channels, with measurable voltage range 0.1 V - VBAT, which can be used for temperature measurement and other related measurement. For details, see the

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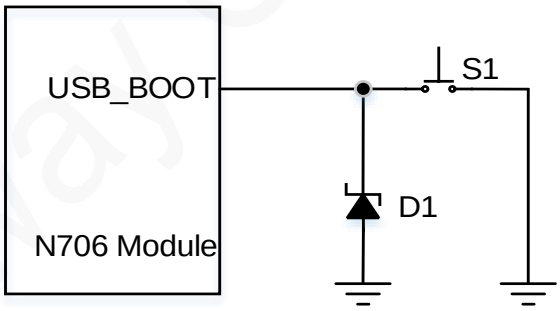
Signal	Pin SN	I/O	Function description	Remarks
ADC0	9	AI	General A/D interface	-
ADC1	96	AI	General A/D interface	-

4.6.2 USB_BOOT

Signal	Pin SN	I/O	Function description	Remarks
USB_BOOT/ KEYIN4	82	B	Emergency download control	-

N706-CB provides a USB_BOOT pin, which is used to enter the emergency download mode. To enter emergency download mode you should connect USB_BOOT of the module to ground and then power up the module. This is the last method to handle issues that result in startup or running failures. To facilitate the subsequent software upgrade and debugging of the product, it is recommended to reserve this pin. The following figure shows the reference design of this pin. Adding an ESD component to protect USB_BOOT in the circuit is required.

Figure 4-22 Reference design of USB_BOOT pin



4.6.3 NET_STATUS

Signal	Pin SN	I/O	Function description	Remarks
NET_STATUS	16	DO	Network status indication	Leave this pin open if unused.

NET_STATUS is the network status indicator pin of the module. It outputs PMW waves of duty cycle varying with the status of the module and drives an LED indicator to blink at different modulation

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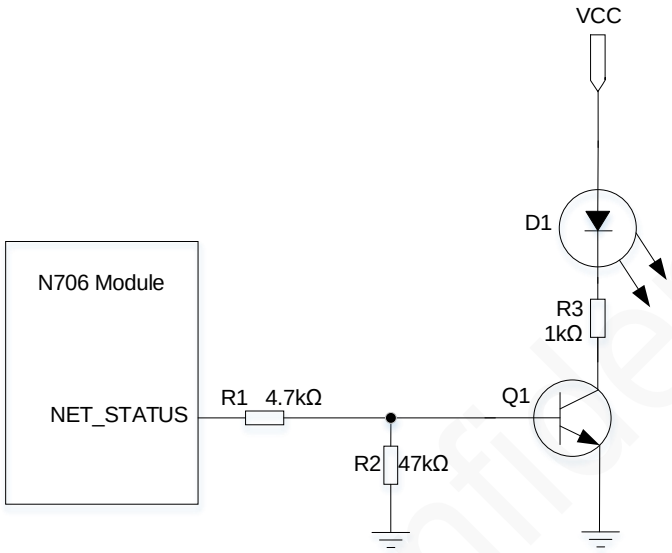
frequencies. You can send AT commands to enable the LED indicator to blink in different states. For details, see *Neoway_N706_AT_Commands_Manual*.

The NET_STATUS indication pin outputs a high level of 1.8 V. Do not use this pin to directly drive LED indicator. It is recommended to drive LED indicators through a triode.

Figure 4-23 Driving LED indicators with a triode



4.6.4 STATUS

Signal	Pin SN	I/O	Function description	Remarks
STATUS	25	DO	Operating status indication	Leave this pin open if unused.

STATUS is a network status indicator pin of the module. It outputs PMW waves of duty cycle varying with the status of the module and drives LED indicators to blink at different modulation frequencies. You can send AT commands to enable the LED indicator to blink in different states. For details, see *Neoway_N706_AT_Commands_Manual*.

The STATUS indication pin outputs a high level of 1.8 V, and do not use this pin to directly drive LED indicator. It is recommended to drive LED indicators by controlling a triode.

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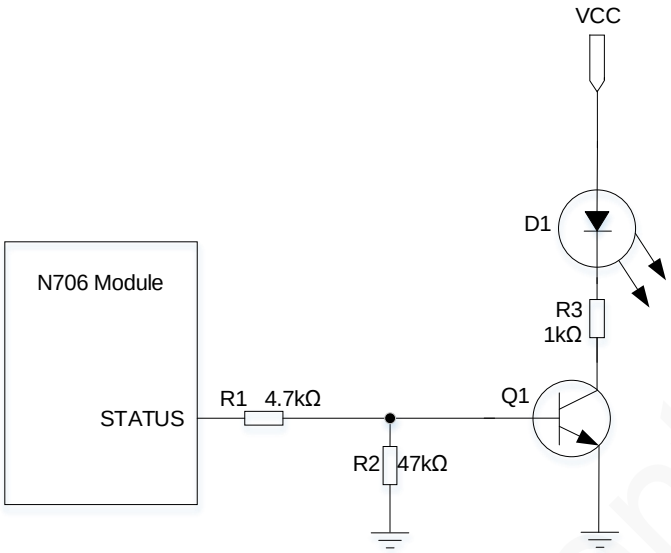
Figure 4-24 Driving LED indicators with a triode



4.7 Signal Multiplexing

Table 4-4 Pin definitions

Signal	Pin No.	Voltage	GPIO	Multiplexing signal 1	Multiplexing signal 2	Remarks
MAIN_RI	20	1.8 V	GPIO1	GPIO_1	/	If multiplexing is not required, this pin can be used for a GPIO.
MAIN_DCD	21	1.8 V	GPIO2	GPIO_2	PWM_10	
MAIN_DTR	19	1.8 V	GPIO4	GPIO_4	PWM_12	
STATUS	25	1.8 V	GPIO6	GPIO_6	/	It is not recommended to use it as GPIO.
NET_STATUS	16	1.8 V	GPIO7	GPIO_7	PWM_2	
KEYIN6	84	1.8 V	GPIO8	KEYIN_4	USIM1_DET	Compatible with the detection pin of USIM 1 and cannot be configured simultaneously with pin #79.
KEYOUT6	85	1.8 V	GPIO10	KEYOUT_4	GPIO_10	
KEYOUT4	83	1.8 V	GPIO11	KEYOUT_5	GPIO_11	
MAIN_RXD	17	1.8 V	GPIO12	UART_1_RXD	GPIO_12	
MAIN_TXD	18	1.8 V	GPIO13	UART_1_TXD	GPIO_13	

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MAIN_CTS	22	1.8 V	GPIO14	UART_1_CTS	GPIO_14	
MAIN_RTS	23	1.8 V	GPIO15	UART_1_RTS	GPIO_15	
I2C3_SCL	68	1.8 V	GPIO16	GPIO_16	UART_3_TXD	
I2C3_SDA	69	1.8 V	GPIO17	GPIO_17	UART_3_RXD	
SPI_FLASH_CLK	101	1.8 V	GPIO18	GPIO_18	SPI_2_CLK	
CAM_SPI_CLK	80	1.8 V	GPIO18	SPI_CAMERA_SCK	PWM_9	
SPI_FLASH1_CS	79	1.8 V	GPIO19	GPIO_19	USIM1_DET	Compatible with the detection pin of USIM 1 and cannot be configured simultaneously with pin #84.
PCM_CLK	30	1.8 V	GPIO19	I2S1_BCK	/	If multiplexing is not required, this pin can be used for a GPIO.
PCM_SYNC	31	1.8 V	GPIO20	I2S1_LRCK	/	If multiplexing is not required, this pin can be used for a GPIO.
SPI_FLASH_SIO0	100	1.8 V	GPIO20	GPIO_20	SPI_2_DIO_0	
SPI_FLASH_SIO1	108	1.8 V	GPIO21	GPIO_21	SPI_2_DI_1	
PCM_DIN	32	1.8 V	GPIO21	I2S1_SDAT_I	/	If multiplexing is not required, this pin can be used for a GPIO.
SPI_FLASH_SIO2	109	1.8 V	GPIO22	GPIO_22	/	If multiplexing is not required, this pin can be used for a GPIO.
PCM_DOUT	33	1.8 V	GPIO22	I2S1_SDAT_O	PWM_11	
SPI_FLASH_SIO3	107	1.8 V	GPIO23	GPIO_23		
USB_BOOT/KEYIN4	82	1.8 V	GPIO28	KEYIN_0	GPIO_28	
CAM_I2C1_SCL	57	1.8 V	GPIO29	I2C_M1_SCL	/	If multiplexing is not required, this pin can be used for a GPIO.
KEYIN1	87	1.8 V	GPIO29	KEYIN_1	GPIO_29	
CAM_I2C1_SDA	58	1.8 V	GPIO30	I2C_M1_SDA	/	If multiplexing is not required, this pin can be used for a GPIO.
USIM2_CLK	62	1.8 V	GPIO30	SIM_1_CLK	/	If multiplexing is not required, this pin can be

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						used for a GPIO.
KEYIN2	77	1.8 V	GPIO30	KEYIN_2	GPIO_30	
AUX_RXD	28	1.8 V	GPIO31	UART_2_RXD	/	If multiplexing is not required, this pin can be used for a GPIO.
USIM2_DATA	64	1.8 V	GPIO31	SIM_1_DIO	/	If multiplexing is not required, this pin can be used for a GPIO.
KEYIN5	75	1.8 V	GPIO31	KEYIN_3	GPIO_31	
AUX_TXD	29	1.8 V	GPIO32	UART_2_TXD	/	If multiplexing is not required, this pin can be used for a GPIO.
USIM2_RST	63	1.8 V	GPIO32	SIM_1_RST	GPIO_32	
DBG_RXD	38	1.8 V	GPIO33	UART_4_RXD	/	If multiplexing is not required, this pin can be used for a GPIO.
KEYOUT1	86	1.8 V	GPIO33	KEYOUT_1	GPIO_33	
DBG_TXD	39	1.8 V	GPIO34	UART_4_TXD	/	If multiplexing is not required, this pin can be used for a GPIO.
KEYOUT2	76	1.8 V	GPIO34	KEYOUT_2	GPIO_34	
LCD_SIO	50	1.8 V	GPIO35	SPI_LCD_SIO	/	If multiplexing is not required, this pin can be used for a GPIO.
KEYOUT5	74	1.8 V	GPIO35	KEYOUT_3	GPIO_35	
LCD_SDC	51	1.8 V	GPIO36	SPI_LCD_SDC	GPIO_36	
LCD_CLK	53	1.8 V	GPIO37	SPI_LCD_CLK	GPIO_37	
LCD_CS	52	1.8 V	GPIO38	SPI_LCD_CS	GPIO_38	
LCD_TE	78	1.8 V	GPIO40	LCD_FMARK	GPIO_40	
LCD_RST	49	1.8 V	GPIO41	LCD_RSTB	GPIO_41	
I2C2_SCL	67	1.8 V	GPIO42	I2C_M2_SCL	GPIO_42	
I2C2_SDA	66	1.8 V	GPIO43	I2C_M2_SDA	GPIO_43	
CAM_RST_N	103	1.8 V	GPIO44	CAMERA_RST_L	GPIO_44	
CAM_PWDN	81	1.8 V	GPIO45	CAMERA_PWDN	GPIO_45	
CAM_MCLK	54	1.8 V	GPIO46	CAMERA_REF_CLK	GPIO_46	

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4.8 RF Interfaces

Signal	Pin SN	I/O	Function description	Remarks
ANT_GNSS	2	AI	GNSS antenna	
ANT_WIFI_SCAN	98	AI	2.4 GHz WLAN antenna	50 Ω impedance control.
ANT_MAIN	35	AIO	Main antenna	

4.8.1 ANT_MAIN Antenna Interface

For the module to be applicable to your PCB, the characteristic impedance of the antenna interface should be controlled at 50 Ω and the impedance of the trace from the module's antenna interface to the antenna needs to be kept at 50 Ω to allow reception of radio frequency (RF) signals. In the circuit design, a matching network is essential for antenna matching in the circuit design. The matching network is generally divided into three types: L type, T type, and π type, which are shown in the following figure. The π-type matching circuitry is preferred.

Figure 4-25 L-type RF matching schematics

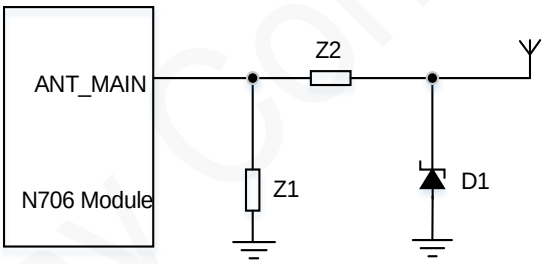


Figure 4-26 T-type RF matching schematics

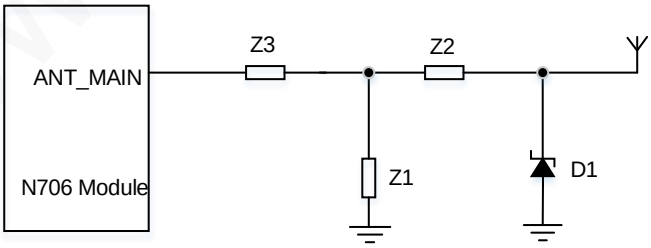
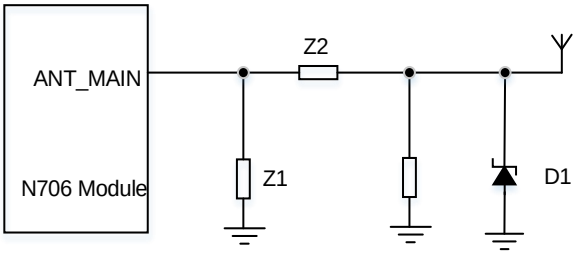


Figure 4-27 π-type RF matching schematics



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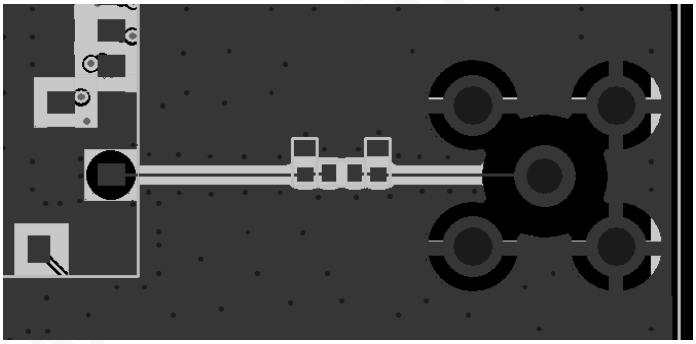
Schematic Design Guidelines

- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- If static electricity may be introduced through the antenna, it is recommended to add ESD components with ultra-low junction capacitance for static electricity protection. TVS diodes with junction capacitance less than 0.5 pF are preferred. Besides, it is necessary to ensure that the reverse breakdown voltage of TVS diodes is greater than 10 V, and TVS diodes with reverse breakdown voltage above 15 V are preferred.

PCB Design Guidelines

- Lay grounding copper foil around the RF traces and provide a dense line of ground via-holes along the RF traces for isolation.
- Keep the RF traces as short as possible and control their characteristic impedance at 50 Ω
- To avoid antenna performance being affected significantly by the parasitic capacitance of a large RF pad when using SMA connector, remove the copper on the first and fourth layers or all layers of a multiple-layer PCB under the RF solder pad. The following is the recommended RF PCB design.

Figure 4-28 Recommended RF PCB design



- A reasonable distance should be kept among ANT_MAIN, ANT_WIFI_SCAN, and ANT_GNSS to avoid mutual interference that may affect reception performance.
- On the PCB, keep the RF signals and components far away from digital circuits, switching power supplies, power transformers, power inductors, clock signals, etc.

4.8.2 ANT_GNSS Antenna Interface

GNSS Impedance Control

ANT_GNSS is the GNSS RF interface of the N706-CBmodule, which requires a characteristic impedance of 50 Ω. The following shows the GNSS structure inside the module.

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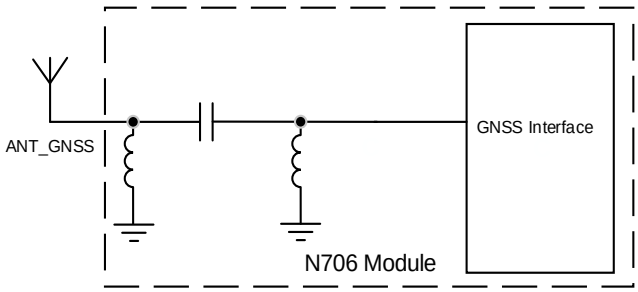
Figure 4-29 GNSS RF structure



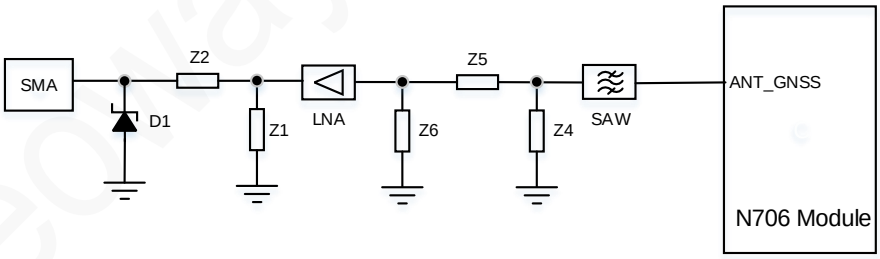
Schematic Design Guidelines

- For the matching circuitry between the module interface and GNSS antenna, please refer to the principle design in section 4.8.1 ANT_MAIN Antenna Interface.
- Add LNAs close to the feeder because the module does not contain one internally. The module's matrix keyboard pins can be used to enable external LNA. For specific pin selection and driver development, contact Neoway FAEs.

Reference design of passive GNSS antenna

After the GNSS antenna receives the GNSS satellite signal, it is transmitted to the ANT_GNSS pin of the N706-CBmodule through PCB traces. The following figure shows a reference design of the passive GNSS antenna.

Figure 4-30 Reference design of passive GNSS antenna



PCB Design Guidelines

- For cautions of PCB design between GNSS interface and antenna, refer to the PCB design guidelines in section 4.8.1 ANT_MAIN Antenna Interface.
- Keep the GNSS RF circuit away from the main and WLAN antenna circuits as far as possible on your application PCB. Otherwise, the RF performance may be affected.

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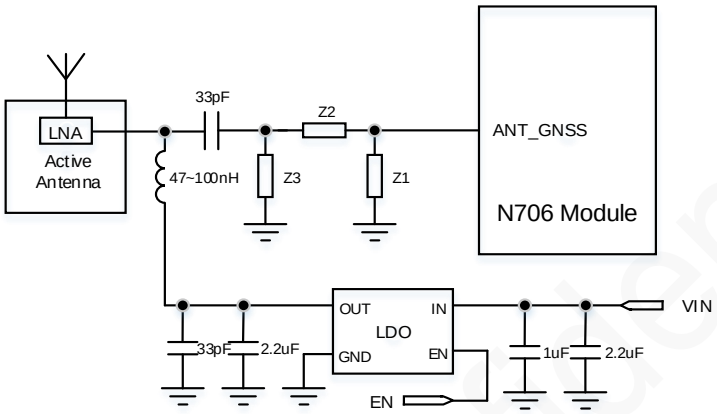
Reference design of active GNSS antenna

After the GNSS antenna receives GNSS satellite signals, the signals are amplified by the front LNA (Low Noise Amplifier) inside the active antenna and then sent to the ANT_GNSS pin of the module through the feeder and PCB traces. The following figure shows the reference design of the active GNSS antenna.

Figure 4-31 Reference design of active GNSS antenna



PCB Design Guidelines

- For cautions of PCB design between GNSS interface and antenna, refer to the PCB design guidelines in section 4.8.1 ANT_MAIN Antenna Interface.
- 50 Ω impedance control is required for both antenna feeders and the PCB traces between the antenna interface and LNA, and the traces should not be too long. The power supply of the active antenna is fed via an inductor of 47 nH - 100 nH from the signal line of the antenna.
- The output voltage of the LDO used to supply power to the active antenna is related to the selection of the LNA. You can select the appropriate LDO to supply power to the antenna according to the selected LNA device. As shown in the above figure.
- Keep the GNSS RF circuit away from the main and WLAN antenna circuits as far as possible on your application PCB. Otherwise, the RF performance may be affected.

4.8.3 ANT_WIFI_SCAN Antenna Interface

The WLAN radio interface only supports the 2.4 GHz frequency band, and its impedance characteristic is required to be 50 Ω.

For the schematic diagram design and PCB design of WLAN antenna interface, please refer to the requirements in section 4.8.1 ANT_MAIN Antenna Interface.

4.8.4 Antenna Assembling

The antenna used by the module must comply with the mobile device standard. The standing wave

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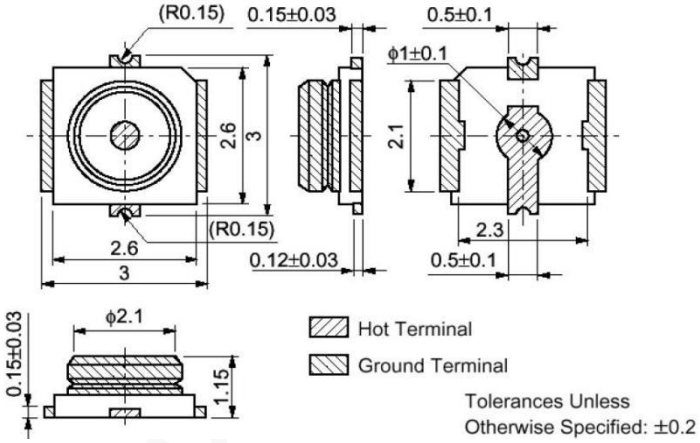
ratio should be between 1.1 and 1.5, and the input impedance should be 50 Ω. Requirements for antenna gain vary according to the application environment. You can choose an appropriate antenna according to specific application scenarios and environments.

The module antenna interface can be connected with rubber rod antenna, sucker antenna or internal Picofarad antenna, and good shielding is required between the external antenna and the RF pin. While using an external RF antenna, keep the external RF cables far away from all interference sources, especially digital signals and switching power supply.

The following methods are commonly used to assemble antennas:

- Reference design for external antennas (GSC RF connector)
  MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

Figure 4-32 Murata RF connector encapsulation specifications



- Connecting to an external antenna by soldering
  It is not recommended to solder the RF cables to the module directly since the stability, consistency, and RF performance are not good.

  The following show the two types of connections.

Figure 4-33 RF cable connections

- PCB printing or SMT

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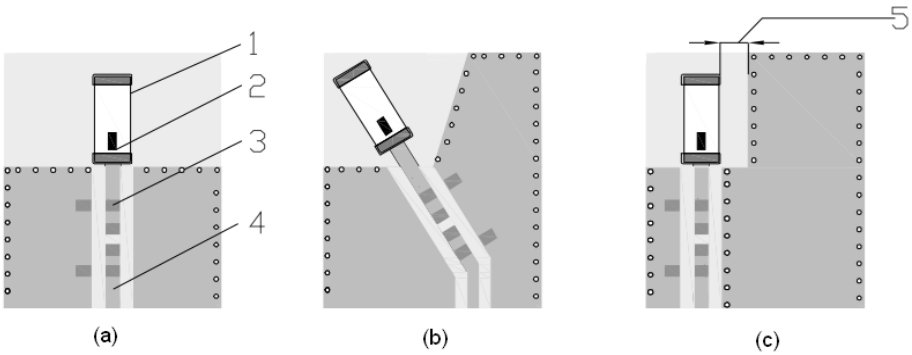
The module works in a wide frequency range, but it is difficult for PCB antennas or ceramic antennas to cover a wide frequency. Therefore, this connection method is recommended only for 2.4 GHz Wi-Fi or BT/ BLE antennas.

The following figure shows the layout of the 2.4 GHz ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

Figure 4-34 Antenna layout

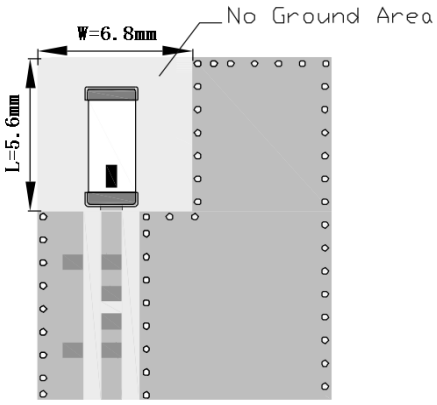


If your PCB is large enough, you can adopt the layout shown in Figure 4-34 (a).

- 1 Chip antenna
- 2 Feeding mark
- 3 Solder pad of the matching circuitry
- 4 50 Ω characteristic impedance RF trace

Figure 4-35 shows the "No Dround Area" between the antenna and ground that is marked as "5" in Figure 4-34.

Figure 4-35 Clearance area (No Ground Area) around the antenna on the PCB board



For more details, please refer to the antenna manual and instruction documentation.

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5 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the N706-CB module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

5.1 Electrical Characteristics

If the voltage is lower than the threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.

Table 5-1 N706-CB operating conditions

Parameter		Minimum value	Typical value	Max. value	Unit
VBAT	V_{in}	3.4	3.8	4.2	V
	I_{in}	N/A	N/A	TBD	A

Table 5-2 Current consumption of N706-CB (Typical)

States / Frequency band	Sleep (mA)	Idle (mA)	Active (mA)	Unit
FDD-LTE: B1, B3, B5, B8	TBD	150	570	mA
TDD-LTE: B34, B39, B40, B41	TBD	97	320	mA

5.2 Temperature Characteristics

Parameter	Minimum value	Typical value	Max. value	Unit
Operating	-30	25	75	℃
Extended*	-40*	25	85*	℃
Storage	-40	25	90	℃

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If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse and cannot meet the requirements of 3GPP specification, but it will not have a great impact on the normal use of the module. After the temperature is restored, the RF performance can be restored to meet the 3GPP specification.

5.3 ESD Protection Characteristics

As electronic products need to undergo strict ESD testing, the following items are the electrostatic protection capabilities of the main pins of the module. When designing related products, you need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25℃

Table 5-3 ESD protection characteristics

Test point	Contact discharge	Air discharge	Unit
GND	8	15	kV
ANT	4	4	kV
Cover	8	15	kV

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6 RF Characteristics

The module provides connectivity on FDD-LTE (Cat 1) and TDD-LTE (Cat 1) networks. This chapter details the wireless RF characteristics.

6.1 Operating Frequency Bands

Table 6-1 N706-CB operating bands

Operating band	Uplink	Downlink	Unit
FDD-LTE B1	1920 - 1980	2110 - 2170	MHz
FDD-LTE B3	1710 - 1785	1805 - 1880	MHz
FDD-LTE B5	824 - 849	869 - 894	MHz
FDD-LTE B8	880 - 915	925 - 960	MHz
TDD-LTE B34	2010-2025	2010-2025	MHz
TDD-LTE B39	1880 - 1920	1880 - 1920	MHz
TDD-LTE B40	2300 - 2400	2300 - 2400	MHz
TDD-LTE B41	2535 - 2655	2535 - 2655	MHz

6.2 TX Power and RX Sensitivity

Table 6-2 N706-CB RF transmit power

Frequency band	Max power	Min. power
FDD-LTE B1	23 dBm±2 dB	< -40 dBm
FDD-LTE B3	23 dBm±2 dB	< -40 dBm
FDD-LTE B5	23 dBm±2 dB	< -40 dBm
FDD-LTE B8	23 dBm±2 dB	< -40 dBm
TDD-LTE B34	23 dBm±2 dB	< -40 dBm
TDD-LTE B39	23 dBm±2 dB	< -40 dBm

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TDD-LTE B40	23 dBm±2 dB	< -40 dBm
TDD-LTE B41	23 dBm±2 dB	< -40 dBm

Table 6-3 RX sensitivity

Frequency band	RX sensitivity	Unit
FDD-LTE B1	≤ -97	dBm
FDD-LTE B3	≤ -96	dBm
FDD-LTE B5	≤ -97	dBm
FDD-LTE B8	≤ -97	dBm
TDD-LTE B34	< -99	dBm
TDD-LTE B39	≤ -99	dBm
TDD-LTE B40	≤ -98	dBm
TDD-LTE B41	≤ -98	dBm

The preceding indicators are tested in a shielded environment in a laboratory. The LTE band indicators are the test results when the bandwidth is 10 MHz, the modulation mode is QPST and RB is set according to the protocol. On no-shielded environments, deviations may exist in the receiver sensitivity of some individual bands due to the interference.

6.3 GNSS Technical Parameters

Table 6-4 GNSS technical parameters

Parameter	Notice
GPS L1 operating frequency	1575.42±1.023 MHz
GLONASS operating frequency	1597.5 - 1605.9 MHz
BDS operating frequency	1559.1 - 1563.1 MHz
Tracking sensitivity	TBD
Acquisition sensitivity	TBD
Positioning accuracy (open space)	TBD
Hot start (open space)	TBD
Cold start (open space)	TBD

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Update frequency	TBD
Max. positioning altitude	TBD
Max. positioning speed	TBD
Max. positioning acceleration	TBD
CNRin/CNRout	TBD
GNSS data type	TBD
GNSS antenna type	Passive/active antenna

The tracking sensitivity, and recapture sensitivity are obtained from the signaling test on GSS7000. The values are the maximum values obtained from multiple measurements performed on samples. External LNA was used during the test.

6.4 WLAN Characteristics

Table 6-5 WLAN TX power and RX sensitivity

Operating frequency band	Transmitting rate	TX power	RX sensitivity
802.11b (2.4G)	1/2/5.5/11 Mbps	N/A	-98 dBm

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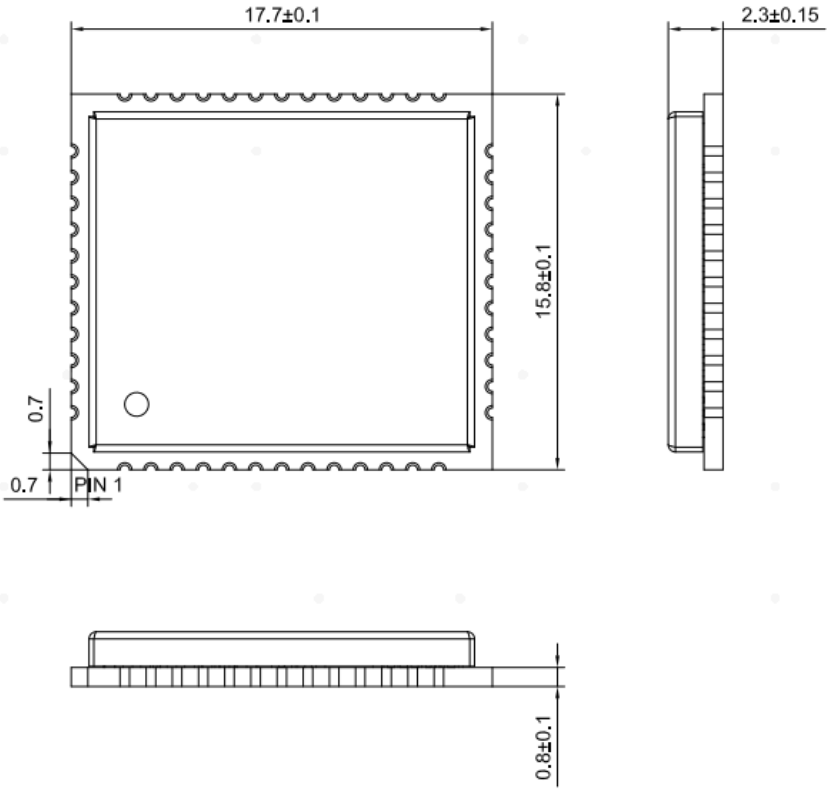
7 Mechanical Characteristics

This chapter introduces mechanical characteristics of N706-CB.

7.1 Dimensions

Figure 7-1 Top and side view dimensions (unit: mm)



7.2 Labeling

N706-CB module labels are laser-engraved and can withstand high temperatures of up to 260°C.

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Figure 7-2 N706-CB label

The above figure is for reference only. For authentic appearance, please refer to the module that you receive from Neoway.

7.3 Packaging

N706 modules are packed in sealed bags on delivery to guarantee a long shelf life. Follow the same package of the modules again in case of opened for any reason.

7.3.1 Reel

Neoway modules are delivered as reeled tapes as shown below:

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7.3.2 Moisture Sensitivity Level

N706-CB modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. The MSL standard is available in IPC/JEDEC J-STD-020.

After the module is unpacked, if it is exposed to air for a long time, the module will get damped, and may be damaged during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at temperatures higher than 90 degrees for more than 12 hours. Do not bake Neoway modules while contained in a tape and rolled up in reels. For baking, place modules individually onto the oven tray.

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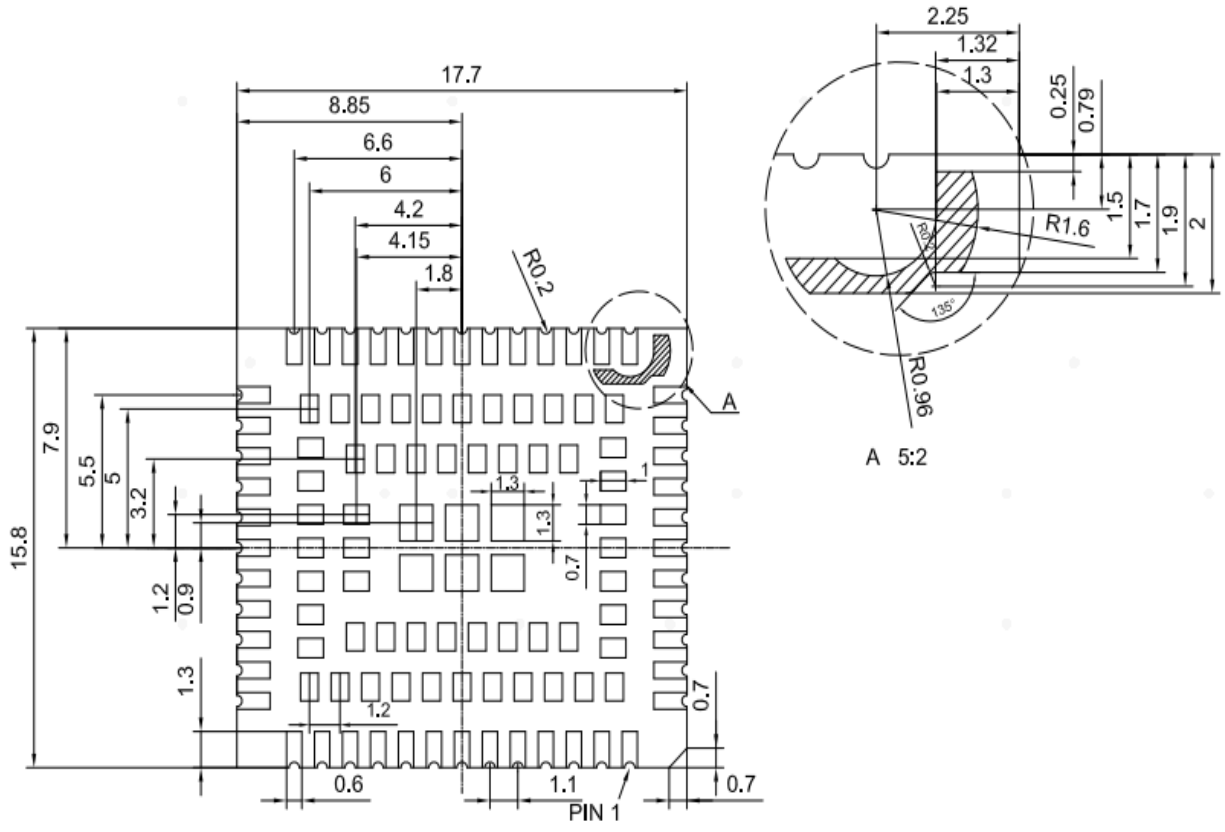
8 Mounting N706-CB onto Application Board

This chapter describes the package of N706-CB, the recommended footprint of the application PCB, and SMT specifications.

8.1 N706-CB PCB Package

Figure 8-1 Bottom view of N706-CB PCB package (unit: mm)



8.2 Application PCB Package

N706-CB is equipped with 109 pads, which are introduced in LCC + LGA package.

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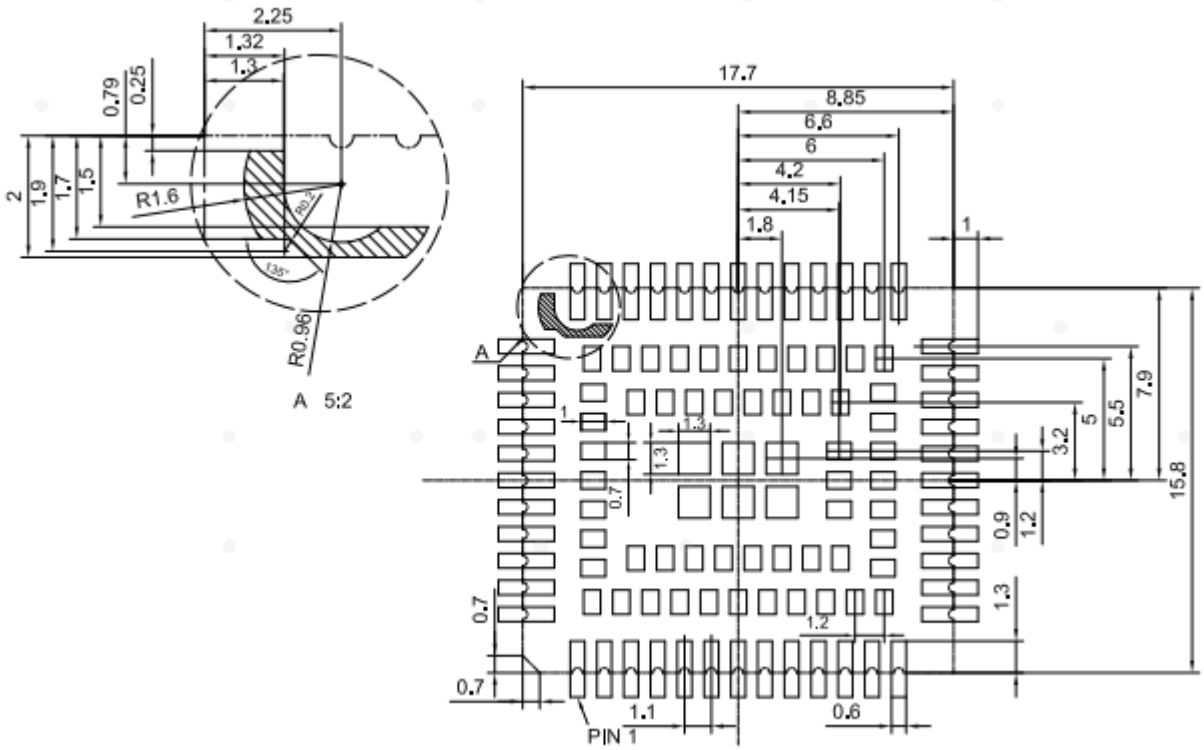
Figure 8-2 N706-CB PCB foot print (top view, unit: mm)



8.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm, which can be fine-tuned according to the actual situation.

8.4 Solder Paste

The thickness of solder paste and the flatness of PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LCC/LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the time above 220°C (reflow temperature) exceeds 45 seconds and the peak temperature does not exceed 240°C.

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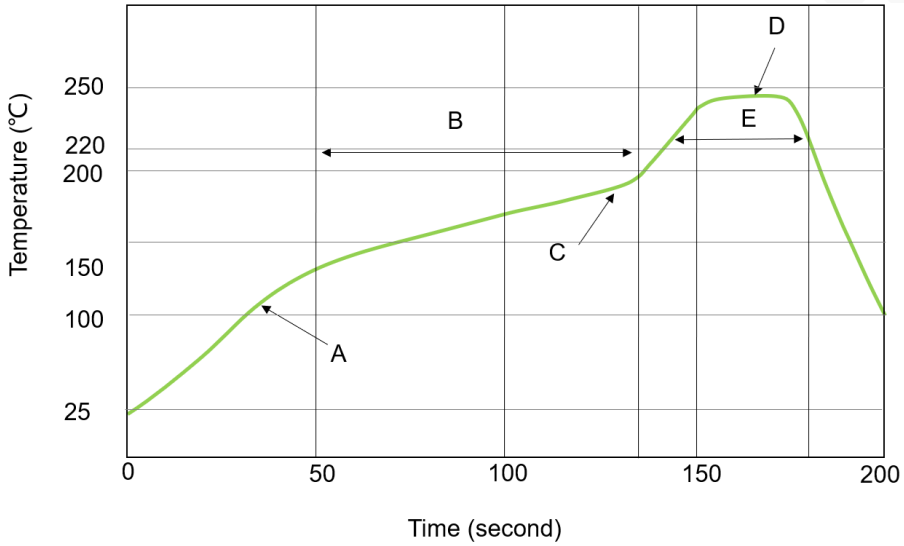
8.5 Oven Temperature Profile

Neoway will not provide warranties for temperature-sensitive element abnormalities caused by improper temperature control.

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 8-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4°C/sec
- Ramp down rate: -3 to -1°C/sec
- Soaking zone: 150 - 180°C, Time: 60 - 100s
- Reflow zone: >220°C, Time: 40 - 90s
- Peak temperature: 235 – 245℃

For information about cautions in storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When removing the module manually from your application PCB board is required, use heat guns with great opening, adjust the temperature to about 245°C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module at high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

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A Abbreviations

Abbreviation	Full name
ADC	Analog-to-Digital Converter
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
ARM	Advanced RISC Machine
BT	Bluetooth
bps	Bits per Second
CCC	China Compulsory Certification
CEP	Circular Error Probable
CNR	Carrier to Noise Rate
CS	Chip Select
CTS	Clear to Send
DC	Direct Current
DCS	Digital Cellular System
DI	Digital Input
DIO	Digital Input/Output
DL	Downlink
DO	Digital Output
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DRX	Discontinuous Reception
DTR	Data Terminal Ready
ECM	Ethernet Control Model
eDRX	Extended DRX
EGSM	Enhanced GSM
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance

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EVK	Evaluation Kit
FDD	Frequency Division Duplexing
FPC	Flexible Printed Circuit
FTP	File Transfer Protocol
GFSK	Gauss Frequency Shift Keying
GLONASS	GLOBAL NAVIGATION SATELLITE SYSTEM
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
3GPP	3rd Generation Partnership Project
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
IO	Input/Output
ISP	Image Signal Processor
LCC	Leadless Chip Carriers
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCLK	Main Clock
MCU	Microcontroller Unit
MIC	Microphone
PCB	Printed Circuit Board
PCS	Personal Communications Service
PWM	Pulse Width Modulation
QVGA	Quarter Video Graphics Array
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output

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SPK	Speaker
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless Fidelity
WCDMA	Wide-band Code Division Multiple Access
WCI	Wireless Coexistence Interface
WLAN	Wireless Local Area Network

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