1. Description

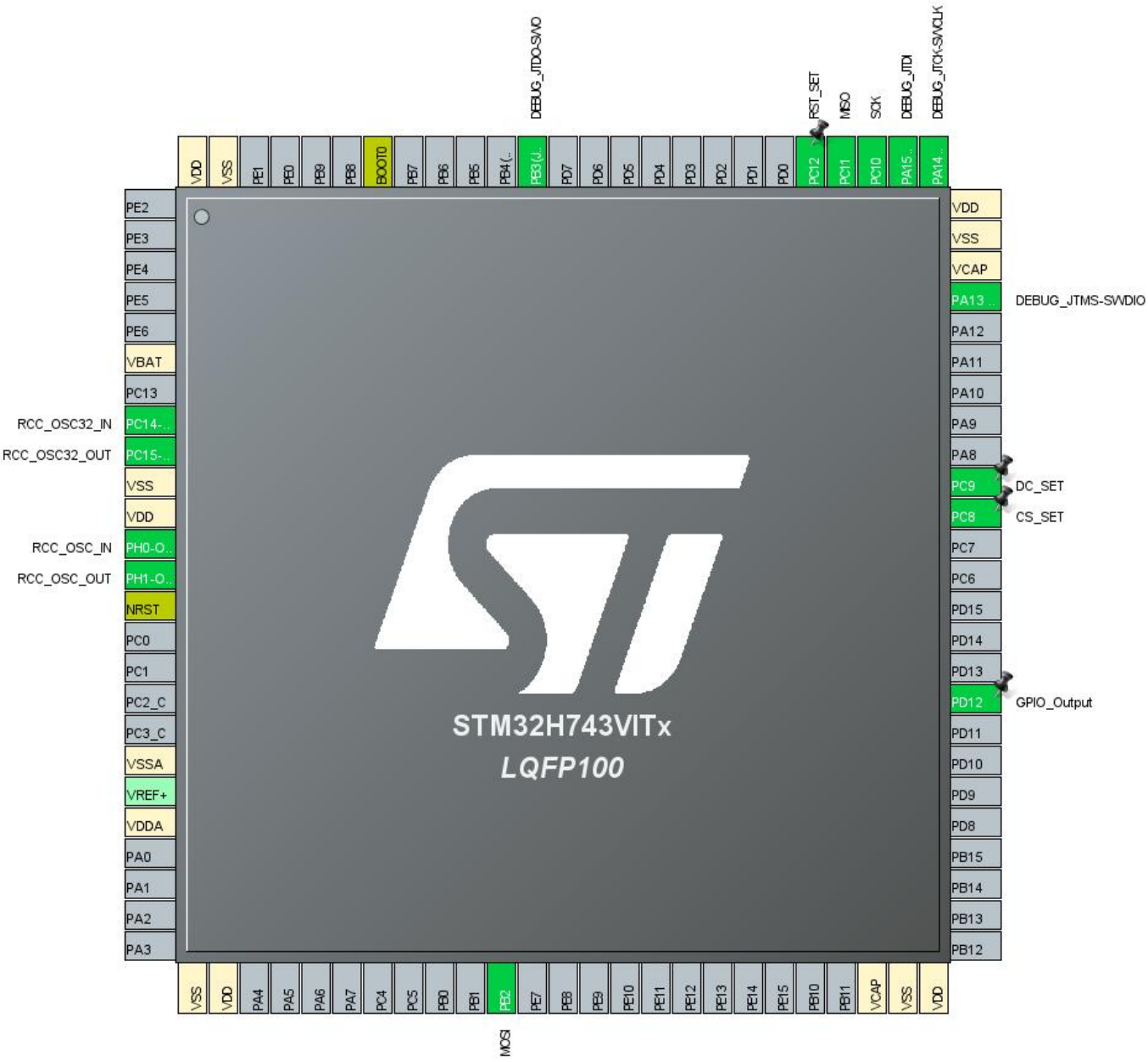
1.1. Project

Project Name	LCDAdapterForH7
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	09/20/2019

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

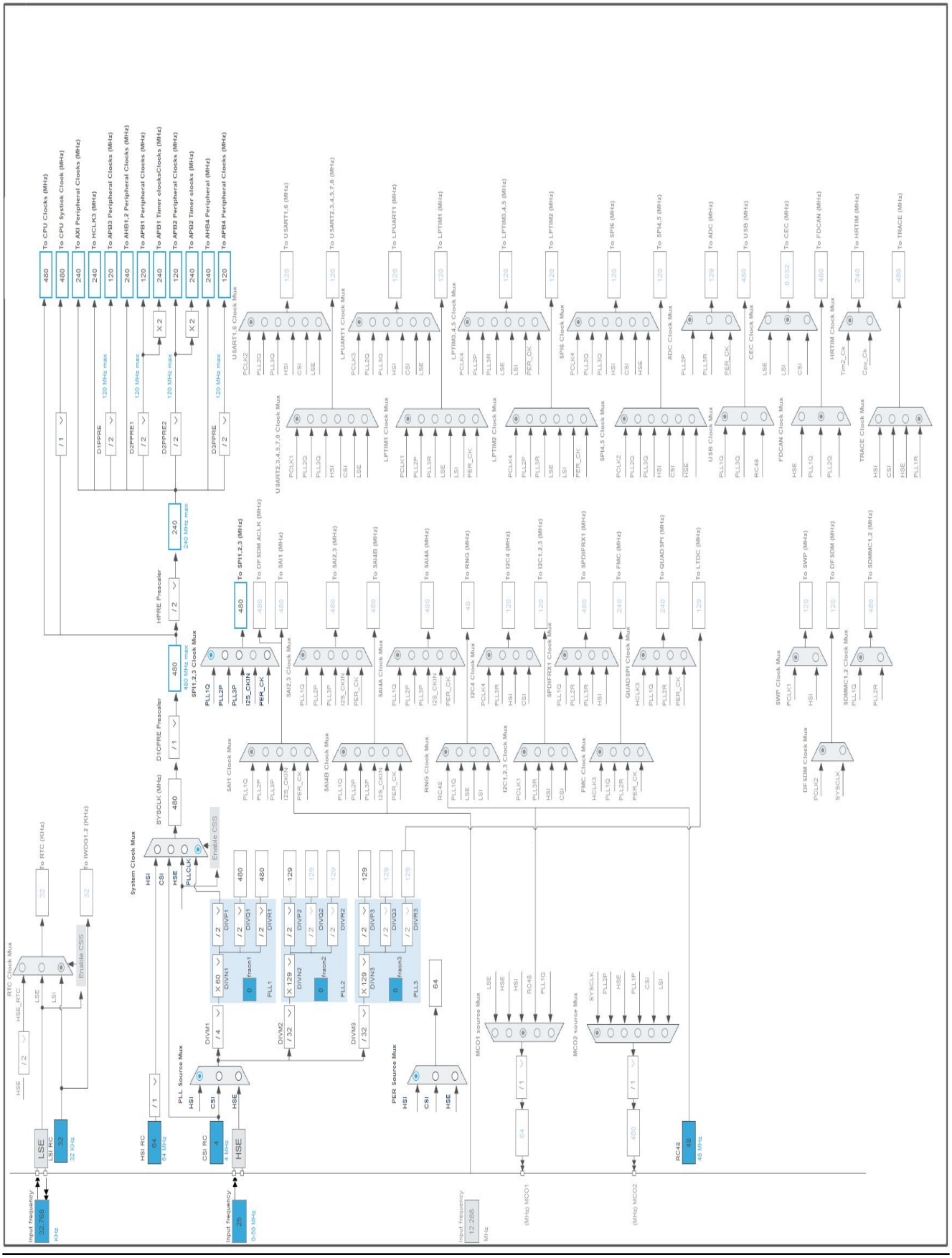


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
21	VDDA	Power		
26	VSS	Power		
27	VDD	Power		
36	PB2	I/O	SPI3_MOSI	MOSI
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
59	PD12 *	I/O	GPIO_Output	
65	PC8 *	I/O	GPIO_Output	CS_SET
66	PC9 *	I/O	GPIO_Output	DC_SET
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	DEBUG_JTDI	
78	PC10	I/O	SPI3_SCK	SCK
79	PC11	I/O	SPI3_MISO	MISO
80	PC12 *	I/O	GPIO_Output	RST_SET
89	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	LCDAdapterForH7
Project Folder	C:\Users\pan39\Desktop\Singlechip\arm\LCDAdapterForH7
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.5.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743VITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.2. DEBUG

Debug: JTAG (4 pins)

7.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 0

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range

7.4. SPI3

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**30.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.5. SYS

Timebase Source: SysTick

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PA15 (JTDI)	DEBUG_JTDI	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PB2	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOSI
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SCK
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MISO
GPIO	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CS_SET
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC_SET
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	RST_SET

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report