

ISE Project Navigator (P. 20131013) - C:\vedz\adder\adder.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

Summary

- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing
- Errors and Warnings
- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- ALL Implementation Messages

Detailed Reports

- Synthesis Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report
- Bitgen Report
- Secondary Reports

Design Properties

- ☐ Enable Message Filtering
- ☐ Optional Design Summary Contents
- ☐ Show Clock Report
- ☐ Show Failing Constraints
- ☐ Show Warnings
- ☐ Show Errors

adder Project Status

Project File:	adder.xise	Parser Errors:	No Errors
Module Name:	adder	Implementation State:	Synthesized
Target Device:	xc7a100t-3csg324	Errors:	No Errors
Product Version:	ISE 14.7	Warnings:	1 Warning (0 new)
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of bonded IOBs	0	210	0%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	星期四 四月 2 11:11:00 2015	0	1 Warning (0 new)	0
Translation Report	Out of Date	星期四 四月 2 11:10:42 2015	1 Error (1 new)	1 Warning (1 new)	0
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports

Report Name	Status	Generated

Date Generated: 09/13/2017 - 09:52:08

Start Design Files

Design Summary

Errors

Console Errors Warnings Find in Files Results

开始 ISE Project Navigator 09:52

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Bitgen Report					

Secondary Reports

Report Name	Status	Generated

Date Generated: 09/13/2017 - 09:52:08

Start Design Files

Design Summary

Errors

Console Errors Warnings Find in Files Results

开始 ISE Project Navigator 新建 Microsoft Word 09:54

New Project Wizard

Create New Project

Specify project location and type.

Enter a name, location, and comment for the project

Name: SSMK

Location: C:\vedz\SSMK

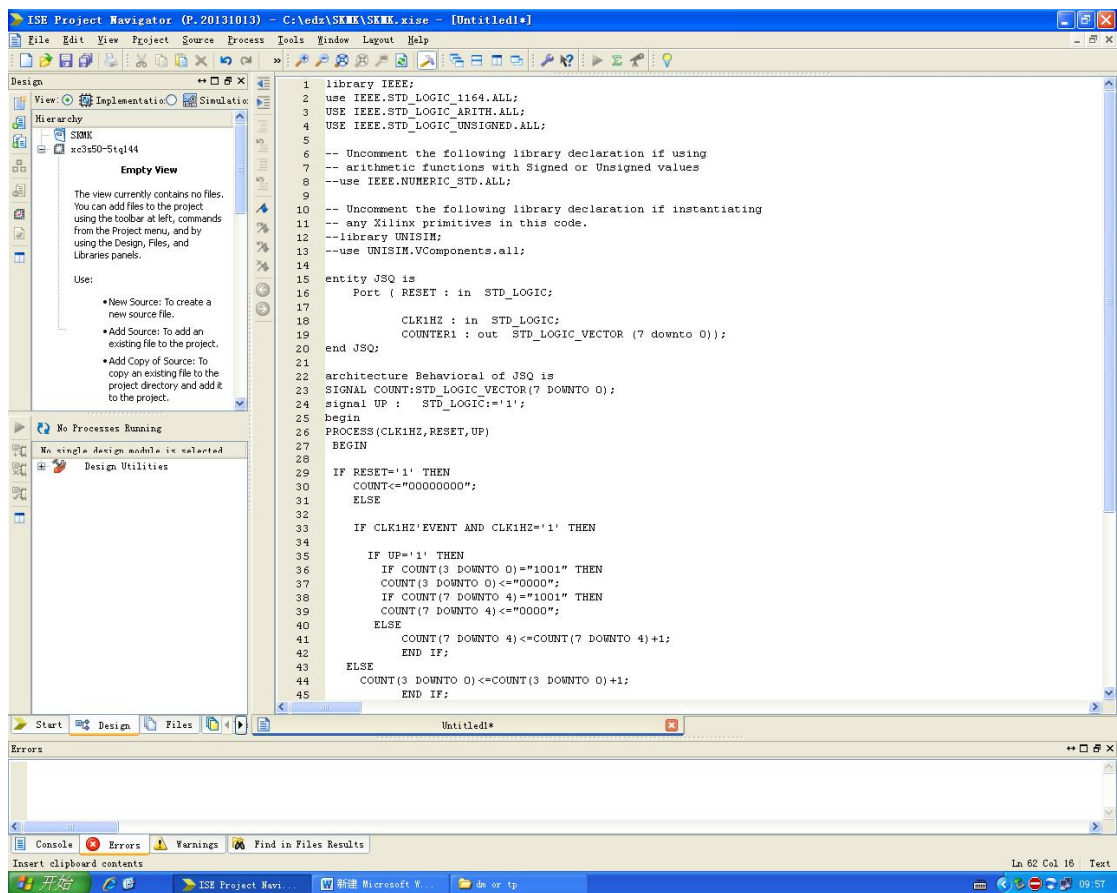
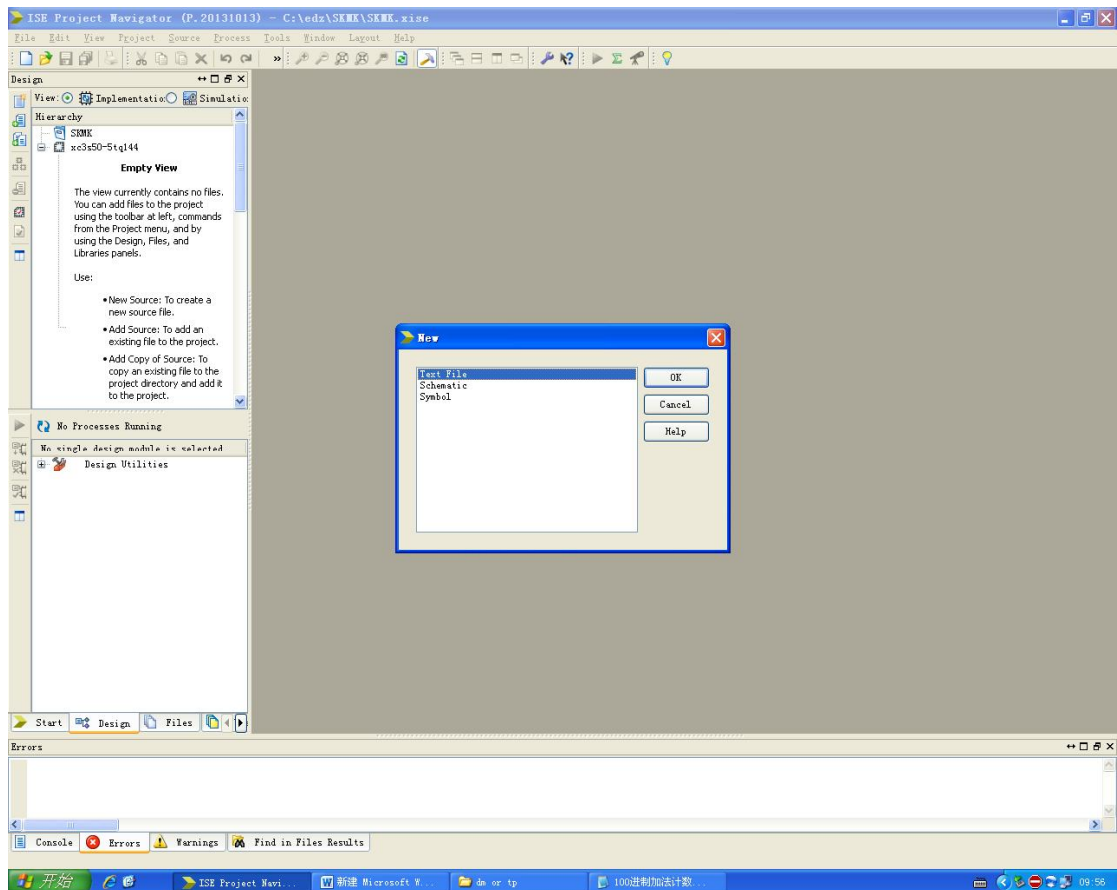
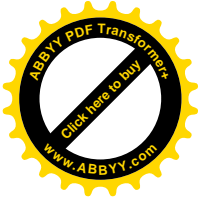
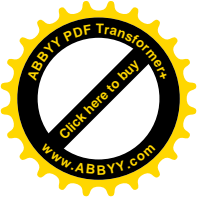
Working Directory: C:\vedz\SSMK

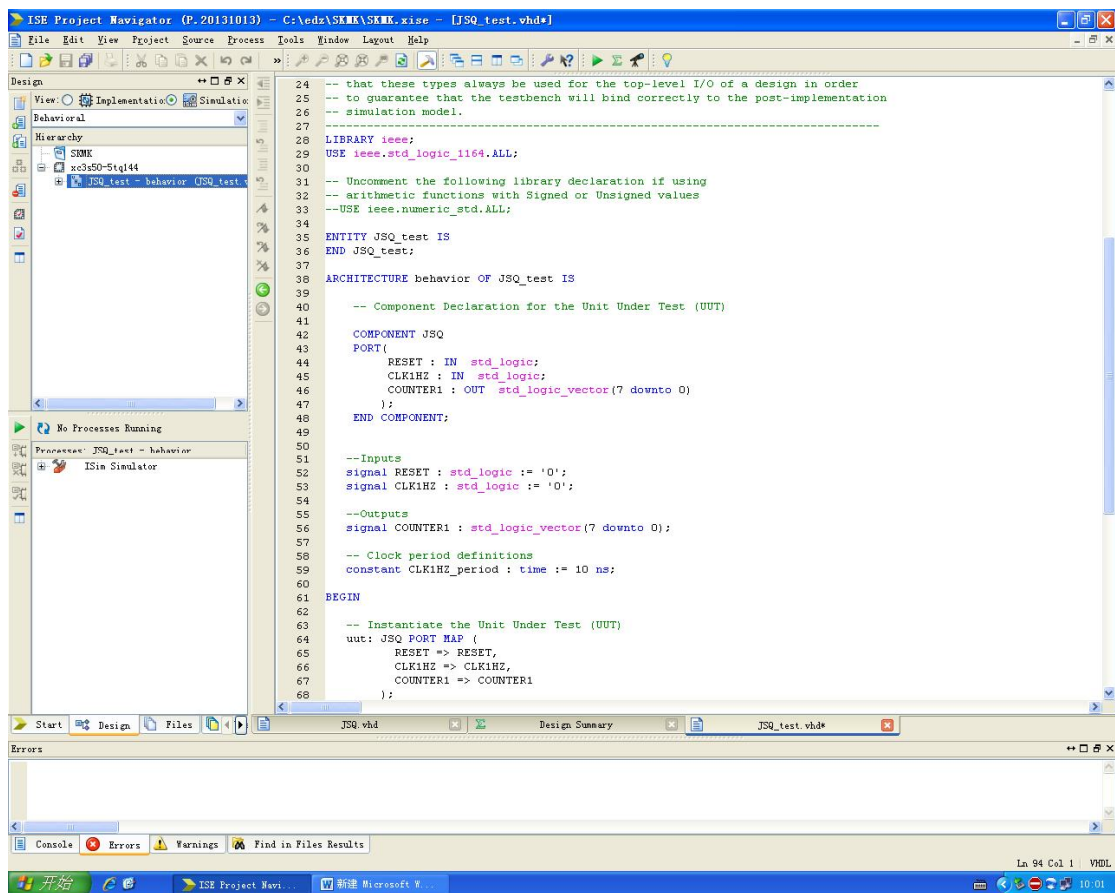
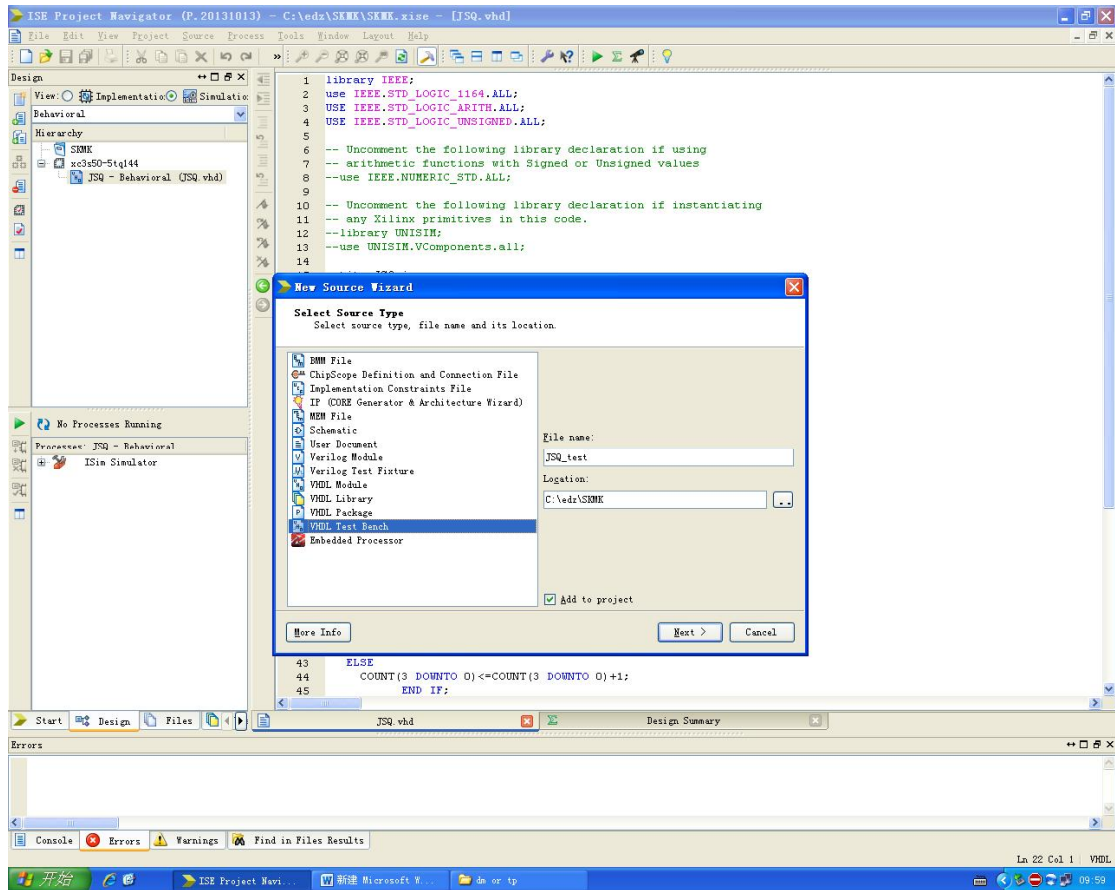
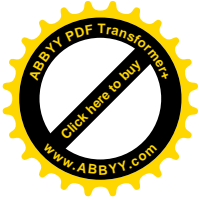
Description:

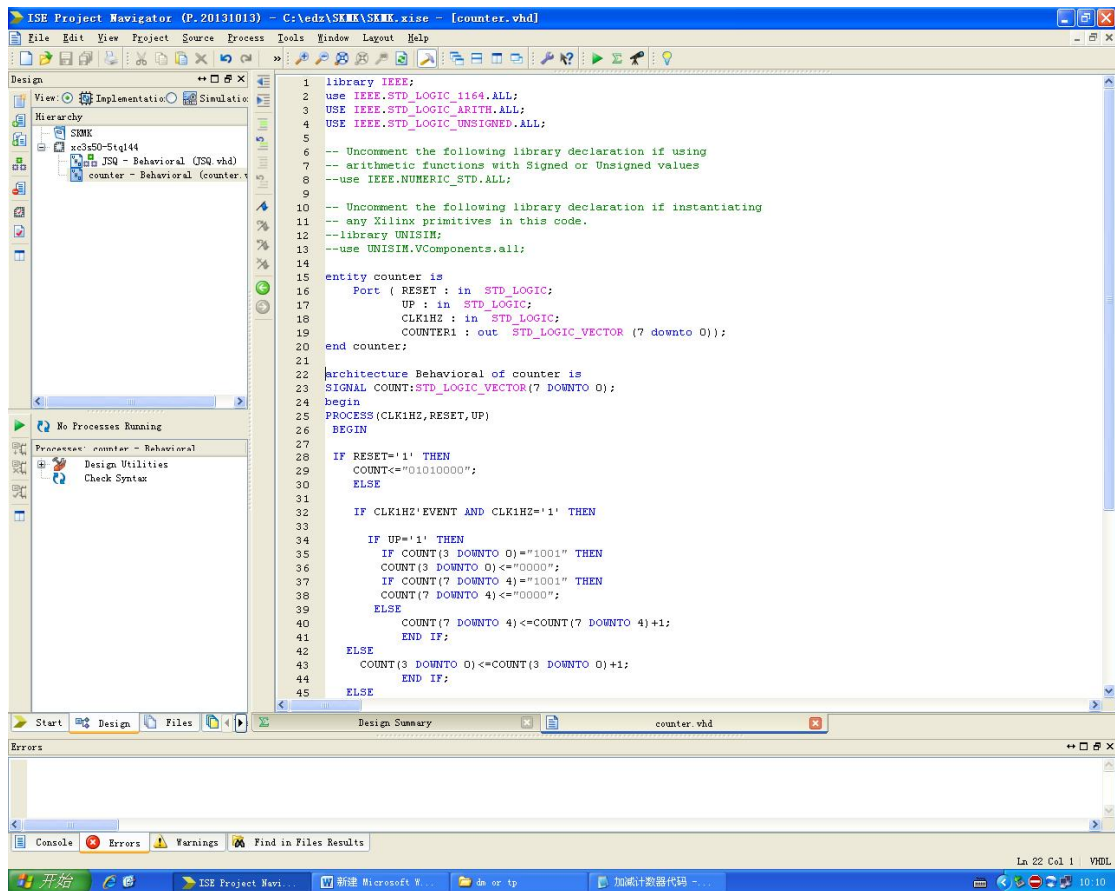
Select the type of top-level source for the project

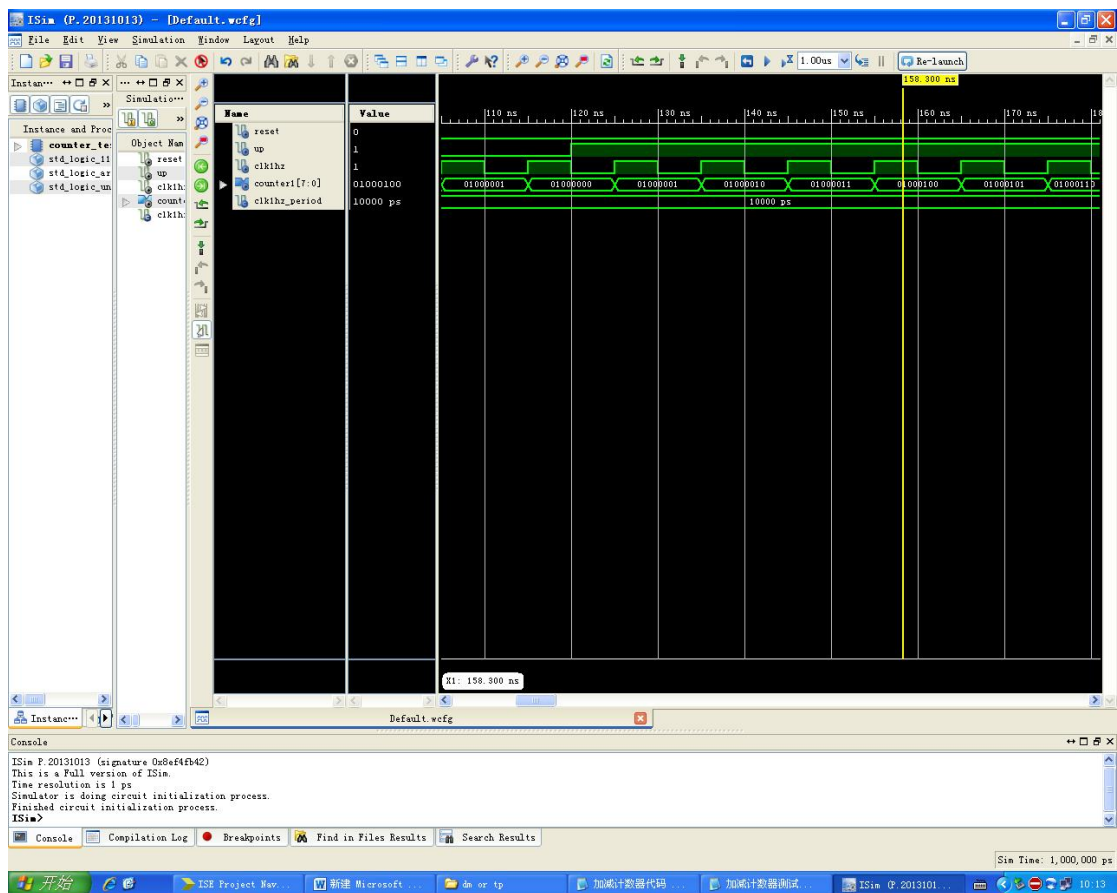
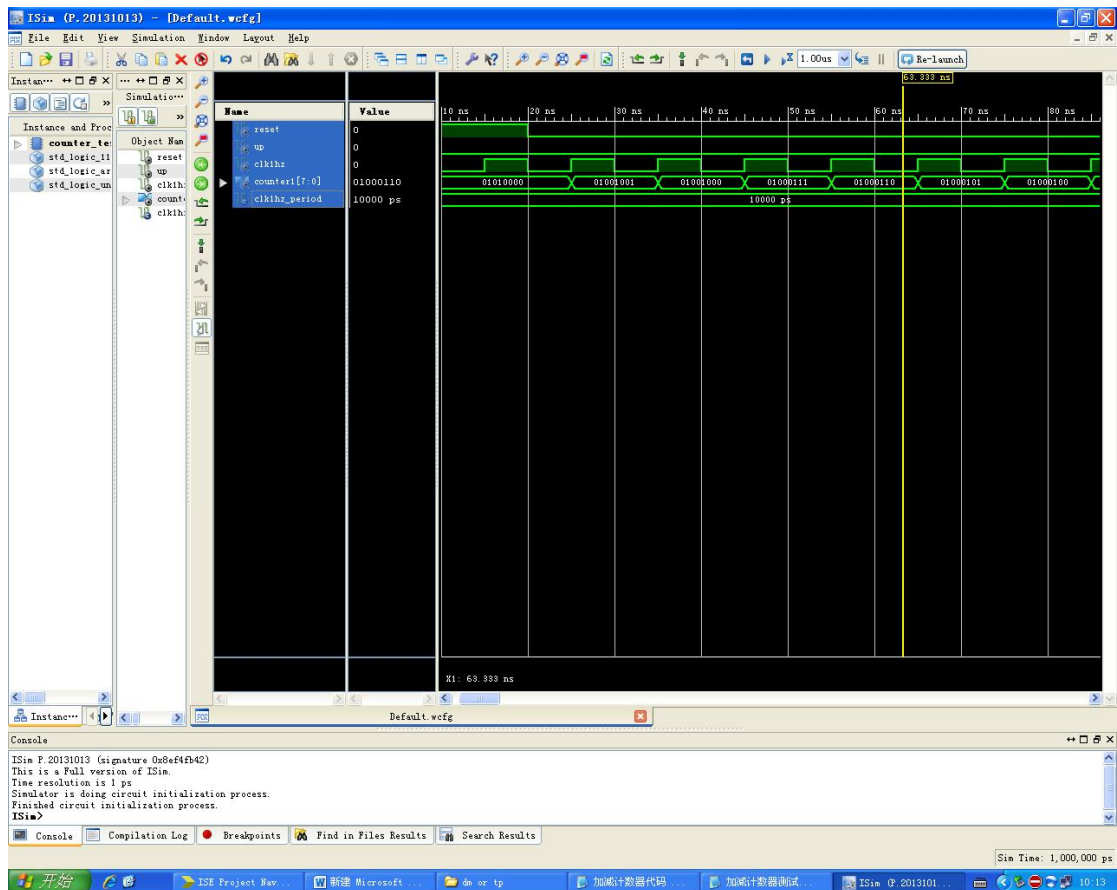
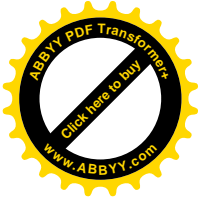
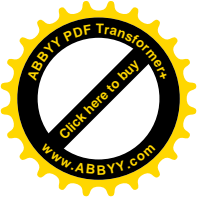
Top-level source type: HDL

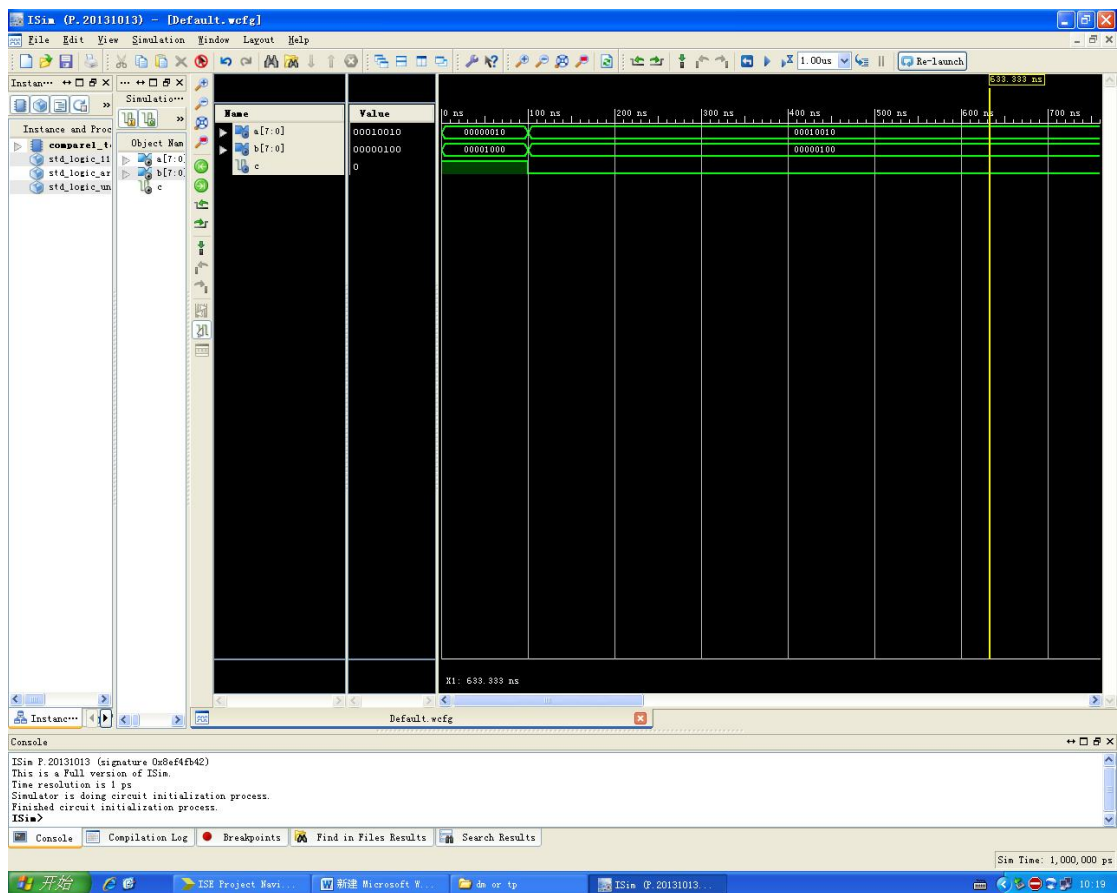
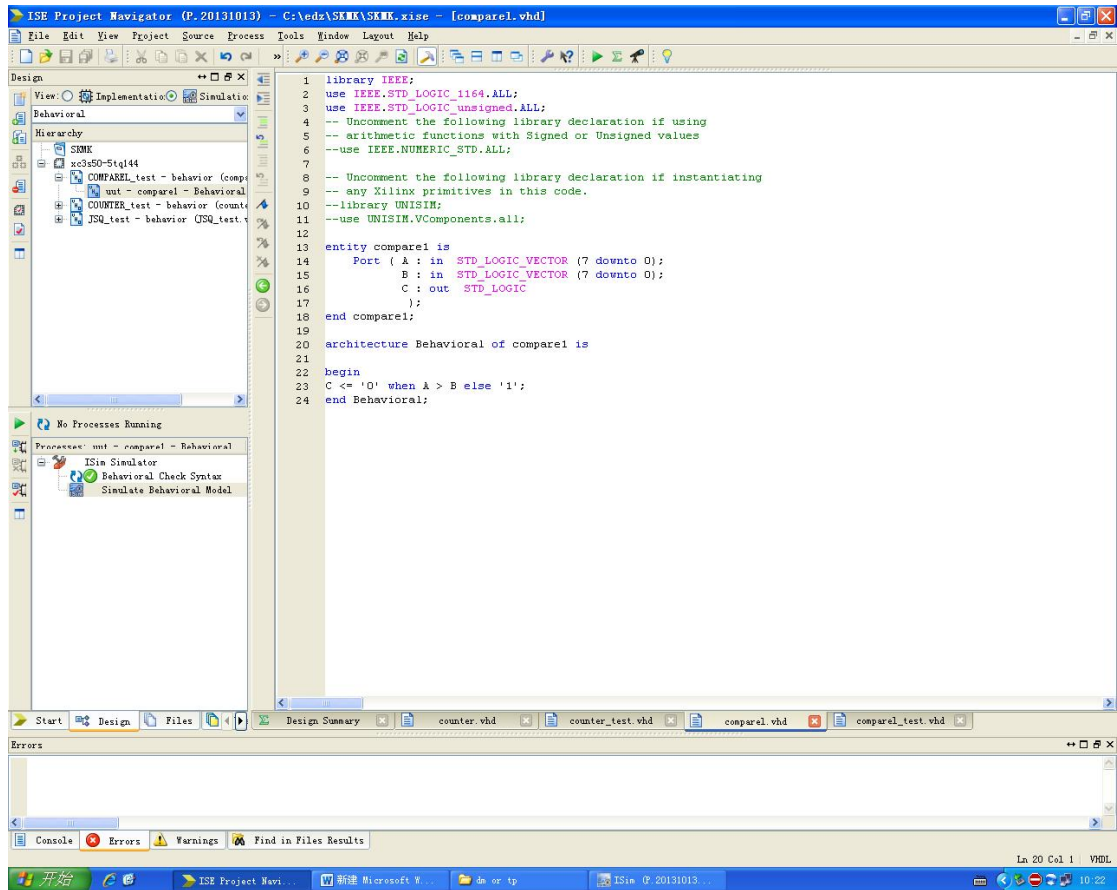
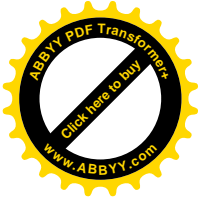
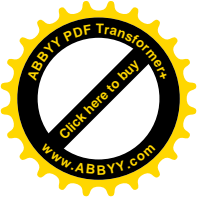
More Info Next > Cancel

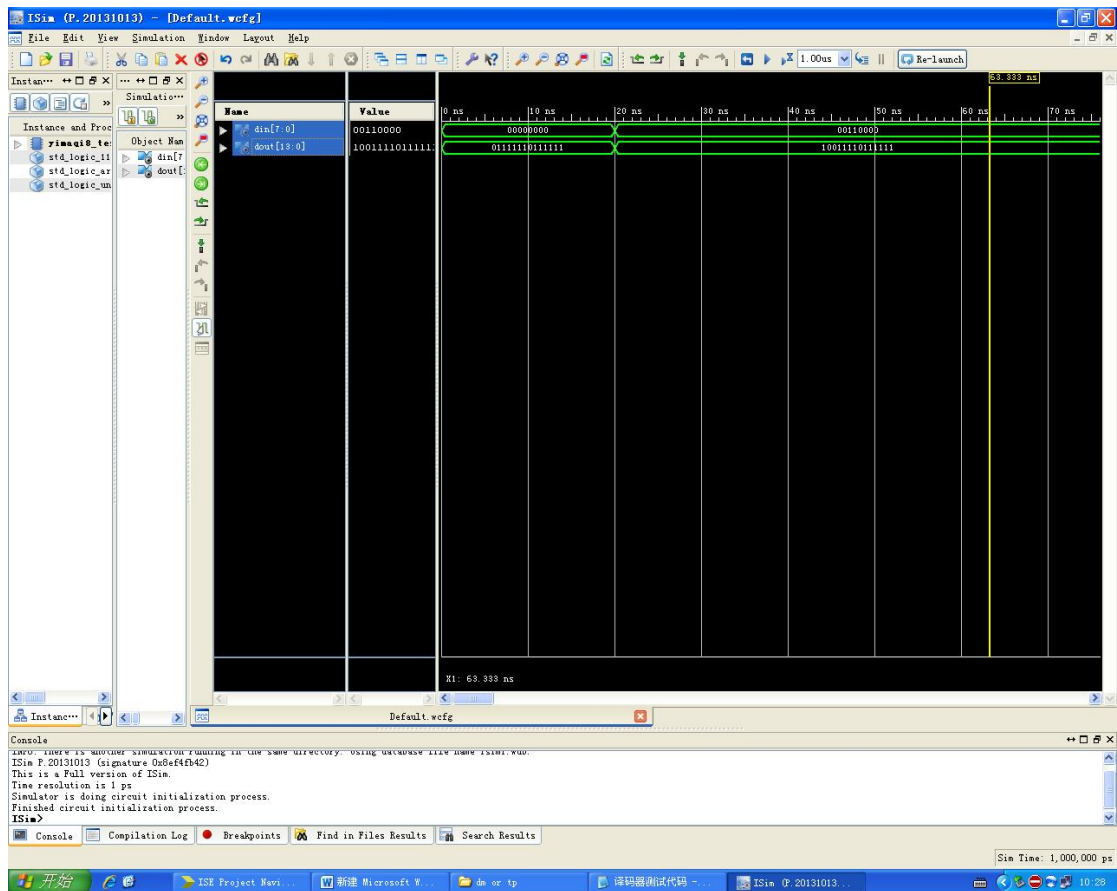
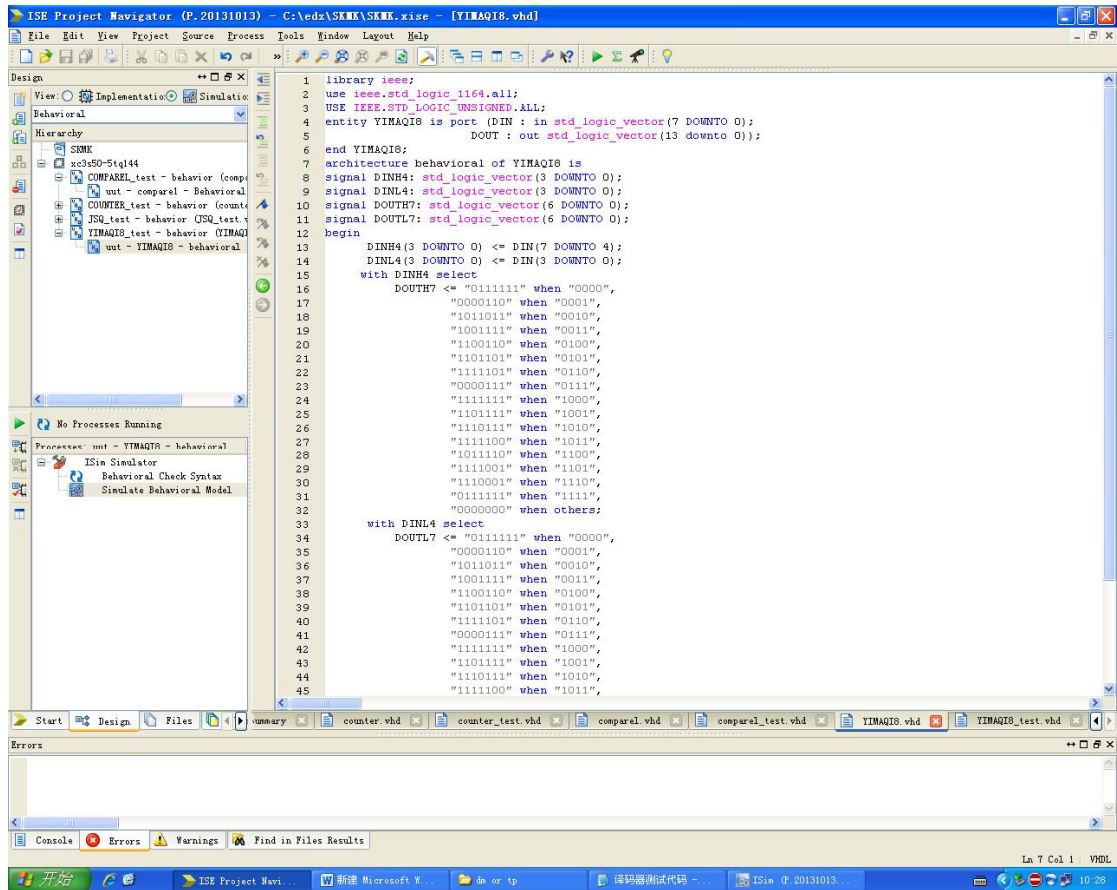
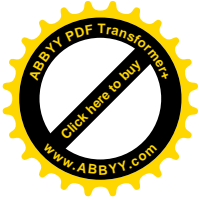


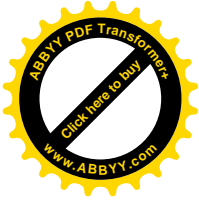












ISE Project Navigator (P. 20131013) - C:\eda\SKMK\SKMK.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

Summary

Project File: SKMK.xise
Module Name: JSQ
Target Device: xc3s50-5tql44
Product Version: ISE 14.7
Design Goal: Balanced
Design Strategy: Milrow Default (unlocked)
Environment:

Parser Errors: No Errors
Implementation State: New
Errors:
Warnings:
Routing Results:
Timing Constraints:
Final Timing Score:

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					

Secondary Reports

Status	Generated
Report	星期三 九月 13 10:32:25 2017

Generated: 09/13/2017 - 10:33:09

No Processes Running

Processes: counter - Behavioral

Design Utilities

Create Schematic Symbol

View HDL Instantiation Text

Check Syntax

Design Properties

Enable Message Box

Optional Design Summary

Show Clock Report

Show Failing Constraints

Show Warnings

Show Errors

Start Design Files

Design Summary

Errors

Console Errors Warnings Find in Files Results

开始 ISE Project Navigator 新建 Microsoft Word 桌面快捷方式 仿真及图片 - Mic...

ISE Project Navigator (P. 20131013) - C:\eda\SKMK\SKMK.xise - [UntitledSchematic.sch]

File Edit View Project Source Process Add Tools Window Layout Help

Symbols

Categories

<--All Symbols-->

Arithmetic

Buffer

Carry Logic

Comparator

Counter

DOR Flip_Flop

Decoder

Flip_Flop

General

IO

IO_FlipFlop

IO_Latch

LUT

Latch

Logic

Map

Memory

Symbols

JSQ

YIMAGI8

compare1

counter

Symbol Name Filter

Orientation

Rotate 0

Symbol Info

Libraries Symbols Options

Design Summary

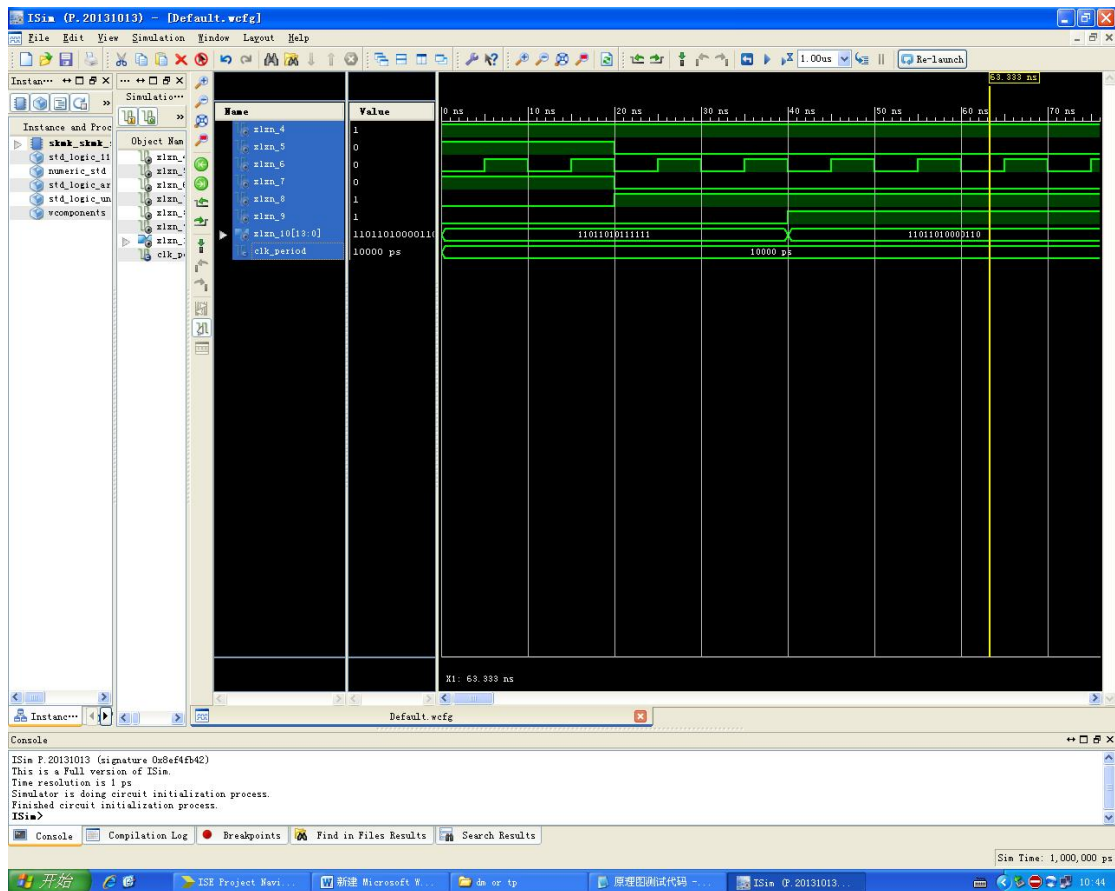
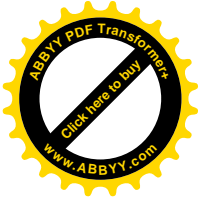
UntitledSchematic.sch

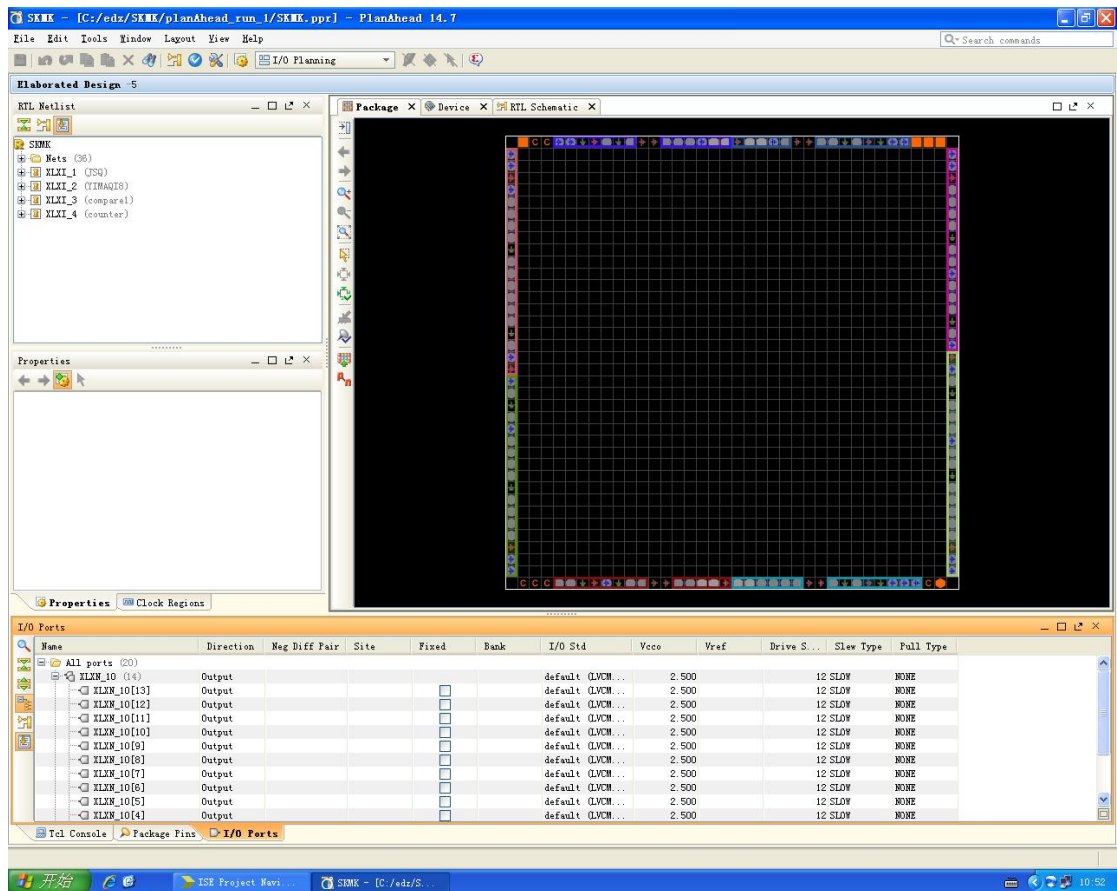
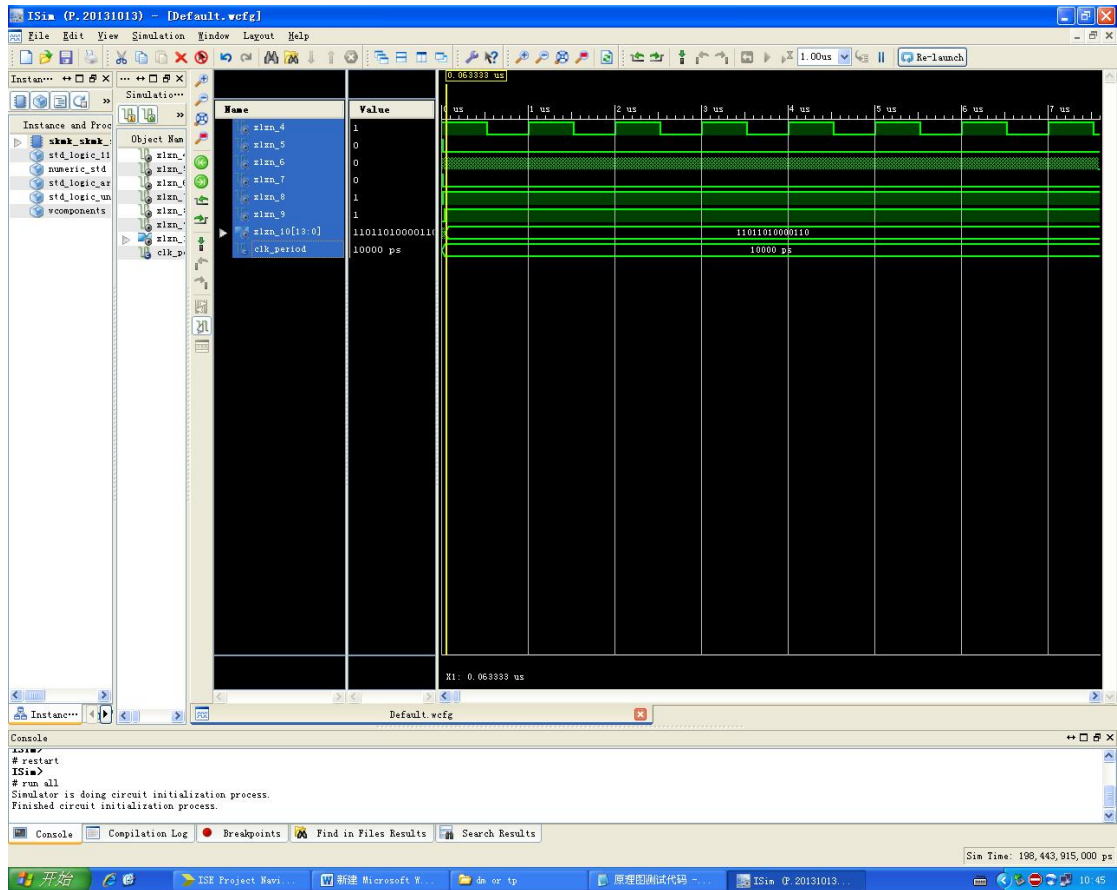
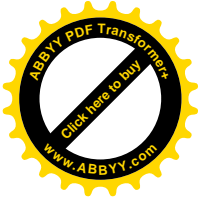
Errors

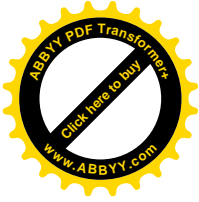
Console Errors Warnings Find in Files Results

Change the editor to add symbol mode

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ISE iMPACT (P.20131013) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

iMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PROM File Form...
- WebTalk Data

Right click device to select operations

TDI — [X] — xc3s50
skmk.bit

TDO —

iMPACT Processes

Available Operations are:

Boundary Scan

Console

INFO:iMPACT:501 - '1': Added Device xc3s50 successfully.

Console Errors Warnings

No Cable Connection No File Open

开始 ISE Project Navi... SKMK - [C://eds/S... 新建 Microsoft V... ISE iMPACT (P.20... 10:53