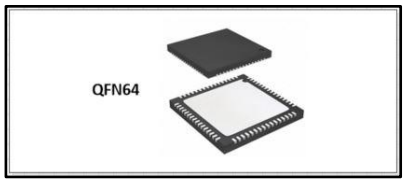
CSK4002
Datasheet V2.3

CSK4002 Datasheet

AndesCore V3 32-bit MCU, up to 8 MB Flash, 8M SRAM, QFN64

Datasheet - production data

- **Core**
  - AndesV3 N10，Maxim speed: 250MHz
  - Hardware accelerator inside: MVA
  - Hardware multiplier and hardware divider
  - 5-stage pipeline
  - Support 2wire and 5 wire debug port
- **Memory**
  - 8MB Flash
  - 8MB PSRAM
  - 1MB internal SRAM
- **Clock**
  - Programmable clock source select
    - External 12.288Mhz high speed crystal
    - Internal 3.072MHz high speed oscillator
    - Internal 32KHz low speed oscillator
    - PLL up to 250Mhz
- **Interrupt**
  - Internal Vectored Interrupt Controller(IVIC)
  - Support watch breakpoint
- **General IO**
  - Up to 50 general IO
- **Communication interface**
  - 3 UART standard communication port
  - 2 SPI standard communication port
  - 2 I2C standard communication port
  - 1 I2S standard communication port
  - 4 DMIC Input
  - USB1.1 full speed Device
  - SDIO standard communication port
  - Touch function support
  - 2 CLASSD output



- **PDMA**
  - Support 18 channels DAM for automatic data transfer between SRAM and peripherals
  - Support external DMA through SPI
- **PIT**
  - 2 programmable interval timer
  - Each of them supports up to 4 timer channels
- **IWDG**
  - 32KHz low speed oscillator
  - 32 bit free running counter
- **UART**
  - 3 UART interface
  - Support hardware flow control
  - Support the hardware handshake for DMA
  - Support by 8 or by 16 over-sampling frequency
- **Working Condition**
  - Voltage between 2.7V to 3.6V
  - Core voltage 1.15V±5%
  - Working temperature: -40°C to +85°C
- **Development tools**
  - Full function embedded debugging environment
- **Package: QFN64**

Contents

1 General Description

CSK4002 is a medium-cost 32-bit microcontroller with embedded Andes D1088 core. CSK4002 is designed for 32-bit microcontroller applications, offering performance, low power, simple instruction set and addressing together with reduced code size compared to exiting solutions. With CPU running at high speed and dedicated DSP for audio processing, it can support the sampling and processing of eight channel audio inputs.

Target applications: Bluetooth speaker, smart home appliance, automobile electronic application

The CSK4002 can run up to 250MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The CSK4002 has up to 1M bytes internal data SRAM and can support large external flash through QSPI and OPI interface. A parallel PSRAM can be packaged together with CSK4002 to support large memory application such as Linux.
Many system level peripheral functions, such as IO port, Timer, Watchdog Timer, UART, SPI, I2C, DMA, PLL, USB1.1 (Full speed), RTC, Quad SPI, SDIO are supported. Additionally, CSK4002 is equipped with Flash Memory Controller, which allows the user to update the program memory without removing the chip from the actual end product.

2 IC Main Function

2.1 Core

- AndesCore D1088 core runs up to 250 MHz
- Internal Vectored Interrupt Controller (IVIC)
- Hardware multiplier and hardware divider.
- Embedded Debug Module (EDM) supports serial debug port(2-wire) and JTAG debug
- port(5-wire).

2.2 Memory

- External flash through QSPI interface
- Totally 256KB SRAM+80KB cache configurable according to the following different configurations
- Additional 640KB SRAM shared between CPU and MVA block
- Dedicated 128KB SRAM for MVA block

	Instruction cache	Data cache	Instruction RAM	Data RAM
Configuration 1	64KB	16KB	128K	128KB
Configuration 2	64KB	16KB		256KB
Configuration 3		16KB	64KB	256KB

2.3 Clock Control

- Programmable system clock source.
- External 12.288 MHz high speed crystal input to provide reference clock for both RF and system.
- Internal 3.072MHz high speed oscillator with calibration (±2% @ 25° C)
- Internal 32 KHz low speed oscillator with calibration.
- PLL allows CPU operation up to 250MHz with the system oscillator.

2.4 PDMA

- Support 18 channels DMA for automatic data transfer between SRAM and peripherals. 3 SPI TX, 3 SPI RX, 3 UART TX, 3 UART RX, 2 I2C, 1PDM2PCM, 1 ADPCM TX,
  1ADPCM RX, 1 I2S TX, 1 I2S RX, 1 ClassD.
- Reception frame error detection
- Support external DMA through SPI

2.5 IO Port

- Up to 50 general-purpose I/O(GPIO) pins.
- GPIO configuration:
- Quasi-bidirectional (Pull-up Enable)
- Push-pull (Output)
- Input only (high-impedance)
- I/O pin can be configured as interrupt source with edge/level setting.
- Flexible IO function select.
- 4 GPIO can be configured to support wake up and interrupt

2.6 PIT

The multi-function timer provides the following 6 usage scenarios depending on the ChMode register bit configurations

- one 32-bit timer.
- two 16-bit timers.
- four 8-bit timers.
- one 16-bit PWM.
- one 16-bit timer and one 8-bit PWM.
- two 8-bit timers and one 8-bit PWM

The features of the PIT controller include:

- Supports AMBA 2.0 APB bus.
- Each multi-function timer provides 6 usage scenarios (combinations of timer and PWM).
- Supports up to 4 multi-function timers.
- Programmable source of timer clock.

2.7 IWDG

- Clocked from an internal 32 KHz low speed oscillator or from 32768HZ crystal if avalilable
- 32-bit free running counter
- Selectable timer-out interval

2.8 UART

- Three UART interface(1 for debug)
- Compatible to the 16C550A register structure.
- One UART Supportthe hardware flow control (CTS/RTS) so that WIFI can be supported through UART interface.
- Supports the hardware handshake for DMA.
- Supports by 8 or by 16 over-sampling frequency.
- Configurable 16/32/64/128 entry transmit/receive FIFOs.

2.9 SPI

- Three SPI interfaces (1 QSPI for flash, the other two SPI to share with UART and PWM)
- One can be used to support QSPI for external flash
- The other two can be configured to 3 wire SPI and share IO with UART and PWM
- Supports the master mode and the slave mode.
- Supports memory mapped access (read-only) through AHB bus.
- Supports memory mapped access (read-only) through EILM bus.
- Supports the hardware handshake for DMA.
- Supports the dual I/O and quad I/O modes.
- Supports the 3-line mode.

2.10 I2C

- Two I2C interface is available.
- Programmable to be a master or a slave device.
- Programmable clock/data timing.
- Supports the I2C-bus Standard-mode (100 kb/s), Fast-mode (400 kb/s) and Fast-mode plus (1 Mb/s).
- Supports the hardware handshake for DMA.
- Supports the master-transmit, master-receive, slave-transmit and slave-receive modes.
- Supports the multi-master mode.
- Supports 7-bit and 10-bit addressing.
- Supports general call addressing.
- Supports auto clock stretch.

2.11 RTC

- Supports software compensation by setting frequency compensate register (FCR)
- The frequency of clock source (before the clock divider) for the counter is 32.768KHz.
- Separate second, minute, hour and day counters.
- Periodic interrupts: half-second, second, minute, hour and day interrupts.
- Programmable alarm interrupt with specified second, minute and hour numbers.

2.12 MVA

- Matrix and vector operation accelerator
- AHB master interface for data read and write
- APB interface for register configuration
- Has interrupt signals
- Support reverse order storage, overflow detection, shift location

2.13 FCC ram controller

- Arbitrate the data access request from CPU, MVA and DMAC
- Partition the MVA memory into several spaces
- If the access from different agents are in different spaces, all of them can be done without wait
- If the accesses from different agents are in the same space, CPU has the highest priority and other agents would wait. (MVA is aware of the wait needed while CPU do not know)

2.14 PDM2PCM

- Support data conversion of PDM data from digital microphone to standard PCM data
- CIC filter in always on domain, half-band and memory in main power domain

2.15 ADPCM

- Support data conversion of PCM data to ADPCM data to save storage area and speed up data transmission
- APB interface for register and data operations
- Interrupt signal to notify CPU

2.16 CRYPTO

- Support inside chip AES128 + SHA256 for secure communication
- AHB master interface for data read and write
- APB interface for register configuration
- Interface with eFuse control to get the eFuse configuration directly

2.17 EFUSE controller

- Read EFuse content after receiving reset release signal from the reset sequence control
- Provide the data to Crypto engine for encryption/decryption usage
- Provide the data to QSPI encrypt wrapper to protect the content of NOR flash

2.18 PSRAM interface

- Support the access of SQPI PSRAM
- Register is configurable through APB bus
- Reading and writing PSRAM data is processed through AHB bus
- Support SPI/QPI mode
- SPI clock is divisible (divided by 2,3,4,5,6,7)

2.19 True random number generator

- True random generator with mixed analog digital implementation to provide true random number
- Register configuration and generated random number can be accessed through APB bus

2.20 PWM interface for class D amplifier

- Two signal PWM data output to class D amplifier to boost performance
- Register configuration and data operation through APB bus
- GPIO pins configurable as PWM output

2.21 I2S interface

- Support extended microphone inputs
- Support I2S audio outputs
- Four outputs signal and two inputs signal supported
- Input signal can be TDM extended to support more microphone inputs
- Register configuration and data operation through APB bus

2.22 Reset Sequence controller

- Generate reset signal to EFuse controller to read the EFuse data out, configure analog IP registers before CPU execute the ROM boot code
- Generate reset signal to CPU for it to start executing boot code from ROM
- Delay Brown-Out Detection (BOD) signal for enough time to generate global reset signal to all the blocks

2.23 USB2.0 full speed Device

- One set of USB 2.0 FS Device 12 Mbps
- On-chip USB Transceiver
- Supports Control, ISO in/out, Bulk in/out, Interrupt in/out transfers
- Provides 6 programmable endpoints
- Supports maximum 512 Bytes for isochronous transfer and maximum 64 Bytes for Bulk and interrupt transfer
- Each endpoint is configurable

2.24 SDIO

- Compliant with SD host controller standard specification, version 3.0
- Supports both DMA and non-DMA data transfers
- Compliant with SD physical layer specification, version 3.0
- Supports UHS50/UHS104 SD cards
- Supports configurable SD bus modes: 4-bit mode and 8-bit mode
- Compliant with SDIO card specification, version 3.0
- Compliant with eMMC card specification, version 5.1 mandatory part
- Supports configurable 1-bit/4-bit SD card bus and 1-bit/4-bit/8-bit EMMC card bus
- Configurable CPRM function for security
- Built-in generation and check for 7-bit and 16-bit CRC data
- Card detection (Insertion/Removal)

2.25 Power Management Unit

- Supports Sleep mode to reduce power consumption
- Supports the wake up through RTC, USB, SPI and Key-in from IO

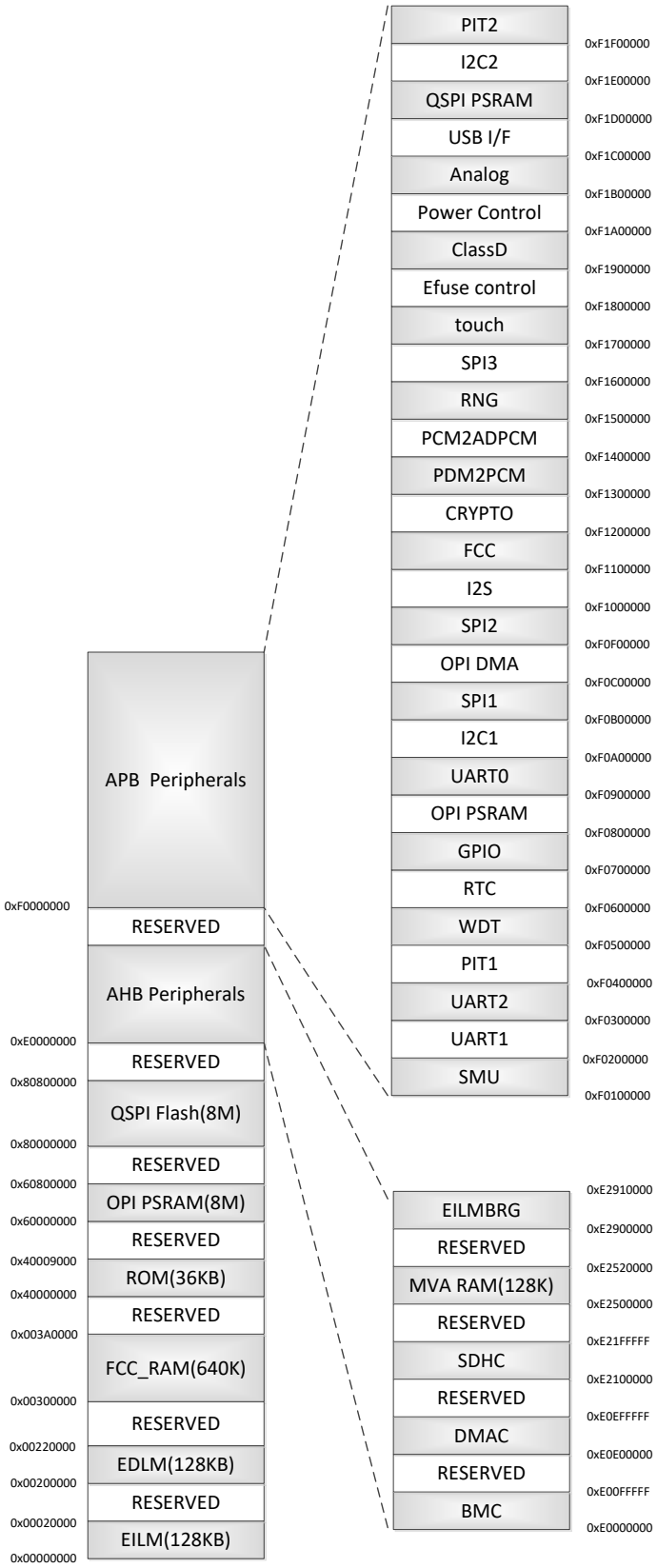
2.26 Touch

- Supports up to 6 touch point detection
- Supports system wakeup through touch

2.27 Analog Top

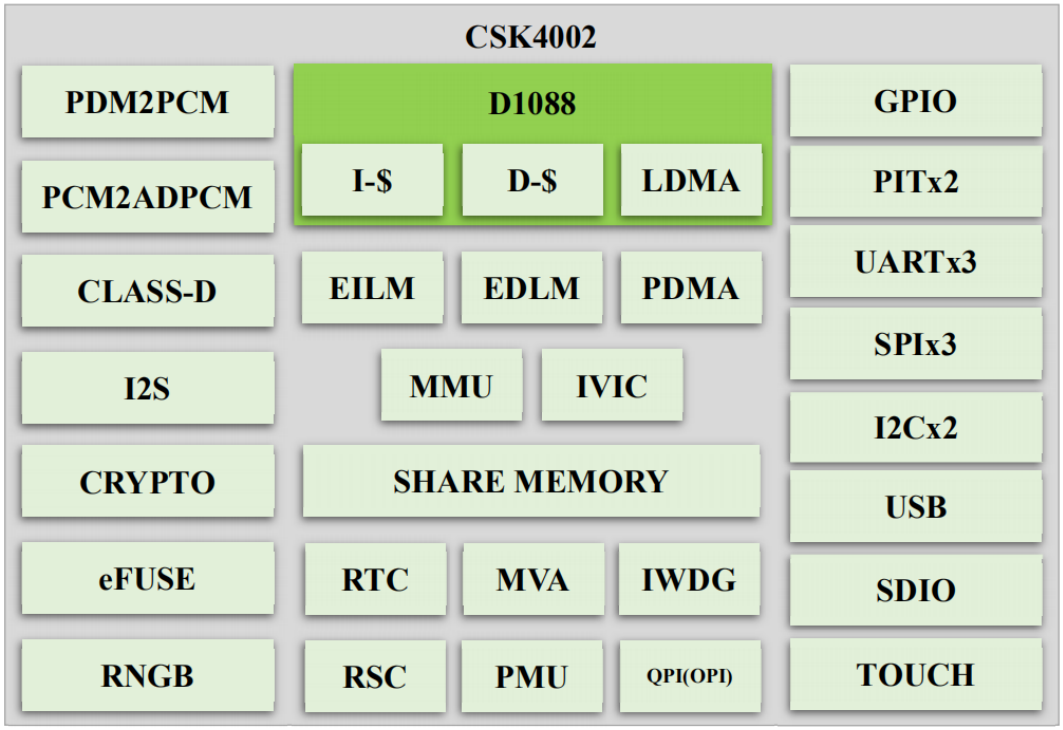
- Control Analog IP registers
- Control through APB bus

3 Memory mapping

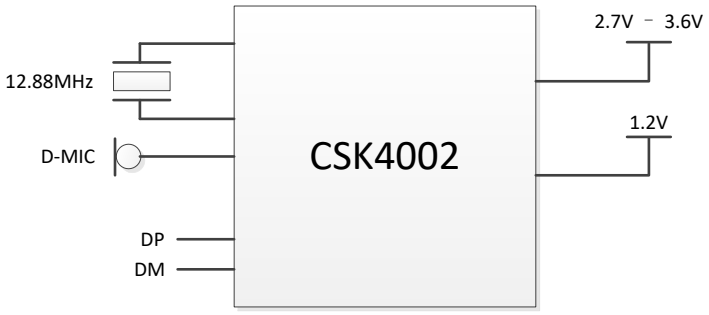


4 Block Diagram

4.1 Block diagram



4.2 External interface



As shown in figure, the chip uses single 3.3V power supply. Digital core uses 1.15V power supply.
The LDO need external capacitance. The chip supports RTC clock through internal 32K ROSC. 12.288MHZ crystal is also needed for internal PLL to generate inside clocks. The chip accepts input from digital microphone, does processing and then communicate with other devices through USB, I2S, ClassD, SDIO and other interfaces. There are also general programmable IOs to communicate with other devices.

5 PIN mapping and Description

5.1 Pin mapping

5.2 Pin descriptions

PIN name	IOMUX options	QFN64 Pin number	Descriptions
VDD_DDR	VDD_DDR	63	VDD 1.8V internal LDO out for OPI PSRAM
VDD_FUSE	VDD_FUSE, RESET	64	VDD 2.5V internal LDO out for Efuse Burn. During POR, it is reset input. After POR, software can program it to disconnect from internal reset logic. The connected capacitor is suggested to be 2.2uF.
VCC_RTC	VCC_RTC	1	
VOUT_11	VOUT_11	2	

VDD_CORE	VDD_CORE	3	
USBDP	0: *USBDP 1: I2C2_SCL 2: TXD2 3: PWM_CH0	4	
USBDM	0: *USBDM 1: I2C2_SDA 2: RXD2 3: PWM_CH1	5	
NC	NC	6	NC
NC	NC	7	NC
NC	NC	8	NC
XOUT	0: *XOUT 1: TXD0 2: PC0 3: RXD0	9	If external crystal is used, it must be used as XOUT. If internal RCOSC or active external OSC is used, it can be muxed to be other functions. (The iomux control and PC0 read/write is in analogtop module XTAL_REG)
XIN	0: *XIN 1: RXD0 2: PC1	10	If external crystal is used, it must be used as XIN. If internal RCOSC is used, it can be muxed to be other functions. (The iomux control and PC1 read/write is in analogtop module XTAL_REG)
PA3	0: *PA3 1: I2S_DOUT3 2: PWM_CH5	11	
PA4	0: *PA4 1: PWM_CH0 2: SPI2_CLK 3: SDIO_CLK	12	
PA5	0: *PA5 1: PWM_CH1 2: SPI2_CS 3: SDIO_IO1	13	
PA6	0: *PA6 1: PWM_CH2 2: SPI2_MISO 3: SDIO_IO0	14	
PA7	0: *PA7 1: PWM_CH3 2: SPI2_MOSI 3: SDIO_CMD	15	
VCC	VCC	16	VCC 3.3 input
PA8	0: *PA8	17	

	1: SDIO_CLK 2: 3: SPI2_CLK		
PA9	0: *PA9 1: SDIO_CMD 2: I2S_DOUT1 3: SPI2_CS	18	
PA10	0: *PA10 1: SDIO_IO0 2: RXD2 3: SPI2_MISO	19	
PA11	0: *PA11 1: SDIO_IO0 2: RXD1 3: SPI2_MISO	20	
VDD_CORE	VDD_CORE	21	VDD 1.15V input
PA12	0: *PA12 1: QSPI_D0 2: PWM_CH3 3: SPI3_MOSI	22	
PA13	0: *PA13 1: QSPI_CLK 2: PWM_CH4 3: SPI3_CLK	23	
PA14	0: *PA14 1: QSPI_D3 2: PWM_CH5 3: SPI3_CS	24	
PA15	0: *PA15 1: QSPI_D2 2: SDIO_IO1 3: SPI3_MISO	25	
PA16	0: *PA16 1: QSPI_D1 2: SDIO_IO2 3: I2C2_SDA	26	
PA17	0: *PA17 1: QSPI_CS 2: SDIO_IO3 3: I2C2_SCL	27	
VCC	VCC	28	VCC 3.3V input
PA18	0: *PA18 1: PWM_CH0	29	

	2: I2C2_SCL 3: SDIO_IO3		
PA19	0: *PA19 1: PWM_CH1 2: I2C2_SDA 3: SDIO_IO2	30	
PA20	0: *PA20 1: I2C1_SCL 2: PWM_CH0 3: I2S_DATAIN1	31	
PA21	0: *PA21 1: I2C1_SDA 2: PWM_CH1 3: I2S_DATAOUT1	32	This is BOOT LED pin used by ROM code. (The LED is connected in common anode mode.)
PA22	0: *PA22 1: I2S_FCLK 2: PWM_CH2 3: SPI3_CLK	33	
PA23	0: *PA23 1: I2S_BCLK 2: PWM_CH3 3: SPI3_CS	34	
PA24	0: *PA24 1: I2S_DOUT0 2: 3: SPI3_MISO	35	
PA25	0: *PA25 1: I2S_DIN0 2: PWM_CH5 3: SPI3_MOSI	36	
PA26	0: *PA26 1: I2S_MCLK 2: I2S_DIN1 3: I2C2_SCL	37	
PA27	0: *PA27 1: TXD1 2: PWM_CH5 3: I2C2_SDA	38	
NC		39	NC
NC		40	NC
NC		41	NC
PA31	0: *PA31	42	

	1: SDIO_IO1 2: RXD2 3: SPI3_CS		
PB0	0: *PB0 1: SDIO_IO0 2: I2S_DOUT2 3: SPI3_MISO	43	
PB1	0: *PB1 1: SDIO_CLK 2: I2S_DOUT1 3: SPI3_CLK	44	
PB2	0: *PB2 1: SDIO_CMD 2: I2S_DIN1 3: SPI3_MOSI	45	
SWCLK	0: *SWCLK 1: PB3 2: PWM_CH0 3: CTS1	46	When debug via ICE is not used, this pin can be used by software as functional pin
SWDIO	0: *SWDIO 1: PB4 2: PWM_CH1 3: RXD2	47	When debug via ICE is not used, this pin can be used by software as functional pin
VDD_CORE	VDD_CORE	48	VDD 1.1V input.
PB5	0: *PB5 1: CLASSD0_P 2: PWM_CH2 3: CTS1	49	
PB6	0: *PB6 1: CLASSD0_M 2: PWM_CH3 3: RXD2	50	
VCC	VCC	51	VCC 3.3V input
PB7	0: *PB7 1: CLASSD1_M 2: PWM_CH4 3: CTS1	52	
PB8	0: *PB8 1: CLASSD1_P 2: PWM_CH5 3: RXD2	53	
PB9	digital： 0: *PB9	54	This pad is a mixed signal pad. When the corresponding control in

	1: DMIC_D3 2: TXD2 3: PWM_CH0 analog: TOUCH5		POWER_CTRL[TOUCH_EN_REG] is 1’b1, it is used as analog pad as TOUCH5
PB10	digital： 0: *PB10 1: DMIC_D2 2: TXD1 3: PWM_CH1 analog: TOUCH4	55	This pad is a mixed signal pad. When the corresponding control in POWER_CTRL[TOUCH_EN_REG] is 1’b1, it is used as analog pad as TOUCH4
PB11	digital： 0: *PB11 1: DMIC_D1 2: RXD1 3: PWM_CH2 analog: TOUCH3	56	This pad is a mixed signal pad. When the corresponding control in POWER_CTRL[TOUCH_EN_REG] is 1’b1, it is used as analog pad as TOUCH3
PB12	digital： 0: *PB12 1: DMIC_D3 2: RTS1 3: PWM_CH3 analog: TOUCH2	57	This pad is a mixed signal pad. When the corresponding control in POWER_CTRL[TOUCH_EN_REG] is 1’b1, it is used as analog pad as TOUCH2
PB13	digital： 0: *PB13 1: DMIC_D1 2: PWM_CH0 3: I2C2_SCL analog: TOUCH1	58	This pad is a mixed signal pad. When the corresponding control in POWER_CTRL[TOUCH_EN_REG] is 1’b1, it is used as analog pad as TOUCH1
PB14	digital： 0: *PB14 1: DMIC_D2 2: PWM_CH1 3: I2C2_SDA analog: TOUCH0	59	This pad is a mixed signal pad. When the corresponding control in POWER_CTRL[TOUCH_EN_REG] is 1’b1, it is used as analog pad as TOUCH0
PB15	0: *PB15 1: TXD2 2: RXD2	60	PB15 can also be used to trigger external PMIC for wakeup from low-power mode. Active low to wake up.

PB16	0: *PB16 1: RXD0 2: DMIC_CLK 3: DMIC_CLK	61	
PB17	0: *PB17 1: TXD0 2: DMIC_DATA0 3: DMIC_DATA0	62	
GND	GND	65	The common ground

Notes:

1. All GPIO pads can only be pulled up, and they cannot be pulled down.

6 Electrical characteristics

6.1 Test condition

Beside special notification, all of voltages are based on V_{SS}

6.2 Absolute maximum rating

Stresses above the absolute maximum ratings listed in *Table 1. Voltage Characteristics*, *Table 2. Current Characteristics*, and *Table 3. Thermal Characteristics* may cause permanent damage to the device.

Table 1. Voltage Characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD1V1} - V_{SS}$	External 1.15 V supply voltage (including VDDA and VDD) (1)	－0.3	1.21	V
$V_{DD3V3} - V_{SS}$	External 3.3 V supply voltage (including VDDA and VDD) (2)	－0.3	3.63	V
V_{IL}	Input Low Voltage on signal pin	-0.3	0.8	V
V_{IH}	Input High Voltage on signal pin	2	3.63	V
V_{OL}	Output Low Voltage on signal pin		0.4	V
V_{OH}	Output High Voltage on signal pin	2.4		

1. All 1.15 V power (V_{DD1V1}) and ground (V_{SS}) pins must always be connected to the external 1.15 V supply.
2. All 3.3 V power (V_{DD3V3}) and ground (V_{SS}) pins must always be connected to the external 3.3V supply.

Table 3. Std. IO Pad Resistor Characteristics

Symbol	Rating	Min	Nom	Max	Unit
R_{pu}	Pull-Up Resistor of std IOs	58K	86K	133K	Ω
R_{pd}	Pull-Down Resistor of std IOs	52K	78K	128K	Ω

Table3. Thermal Characteristics

Symbol	Rating	Value	Unit
T_{STG}	Storage temperature range	-55 to +150	° C
T_a	Maximum ambient temperature	－40 to +85	° C
Tj	Working junction temperature	105	°C
θ JA	Package Thermal Resistance Conditon: Four layer PCB, zero airflow	27	°C/W

Table 4. external crystal Characteristics

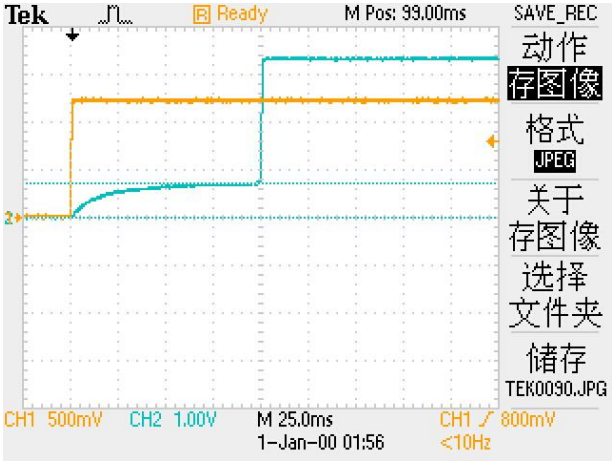
Symbol	Rating	Min	Nom	Max	Unit
F_{HS}	Clock Source Frequency(1)	10	12.288	40	MHz
$Ducy_{HS}$	Duty Cycle	40	50	60	%

Cin_{HS}	Load Capacitance		15		pF

6.3 Operating conditions

6.3.1 POR validity vs Power on sequence of Vcore and VIO

The power on sequence of Vcore and VIO do not affect the POR's validity. Below pictures show the relationship between Vcore and VIO, no matter the core voltage rises up to the target value faster or slower than the IO voltage, the CSK4002 Power On Reset succeed. Usually recommended that the core voltage reach to the setting value faster than the IO voltage's.



6.3.2 ESD

Symbol	Ratings	Conditions	Class	Maximum Value	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	T_A = 25℃		4000	V
VESD(CDM)	Electrostatic discharge voltage (charge device model	T_A = 25℃		2000	V

6.3.3 IO port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Input low level voltage			TBD		
	IO FT input low level voltage			TBD		
V_{IH}	Standard IO input high level voltage			TBD		
	IO FT input high level voltage			TBD		
V_{OL}	Low level output voltage Sink Current			TBD		
V_{OH}	High level output voltage Source Current			TBD		
V_{hys}	Standard IO Schmitt trigger voltage hysteresis			TBD		

	IO FT Schmitt trigger voltage hysteresis			TBD		
I_{lkg}	Input leakage current			1uA		

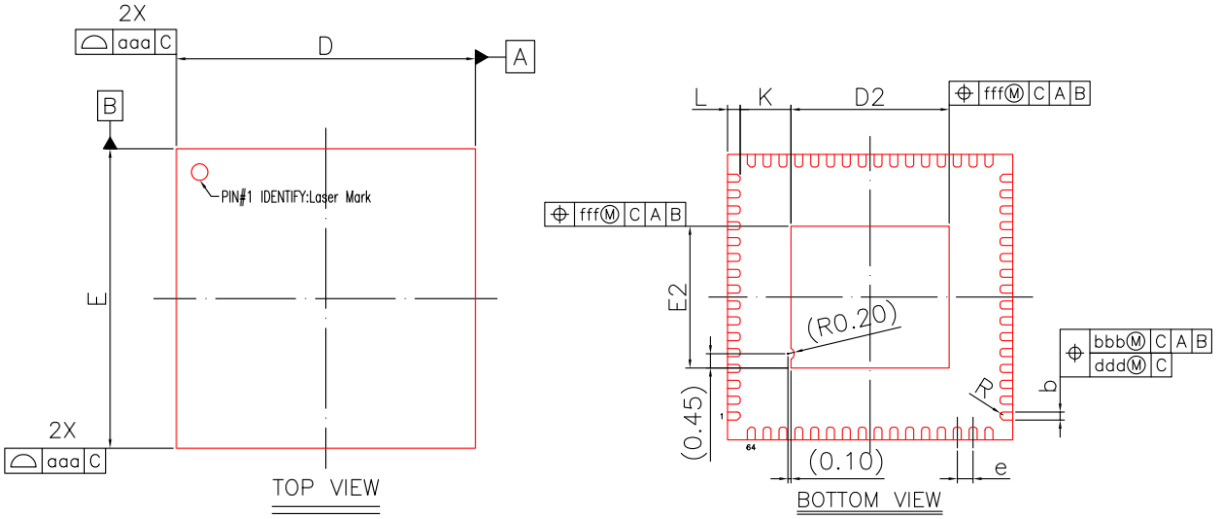
6.3.4 CLASS D

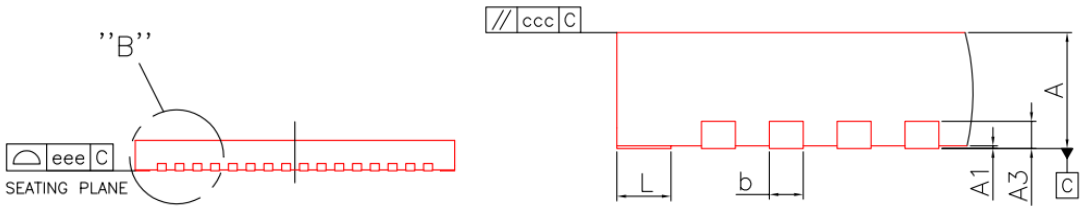
测试项目	Frequency(Hz)		RMS Level(Vrms)		THD+N(%)		SNR(dB)	
	Channel1	Channel2	Channel1	Channel2	Channel1	Channel2	Channel1	Channel2
CLASSD 信号100%幅输出	1000	1000	1.72	1.71	3.10	3.00	120	116
CLASSD 信号50%幅度输出	1000	1000	0.88	0.87	0.27	0.23	114	110
CLASSD 信号25%幅度输出	1000	1000	0.44	0.43	0.31	0.27	106	104

7 Package

CSK4002 有三种封装形式，对应的尺寸再 EPAD 上有差异，具体的尺寸区别可以参考下图所示，同时，对应的不同封装型号的差异，是在芯片的丝印第三行可以看到差异。

7.1 CSK4002 NSxxxxxxG





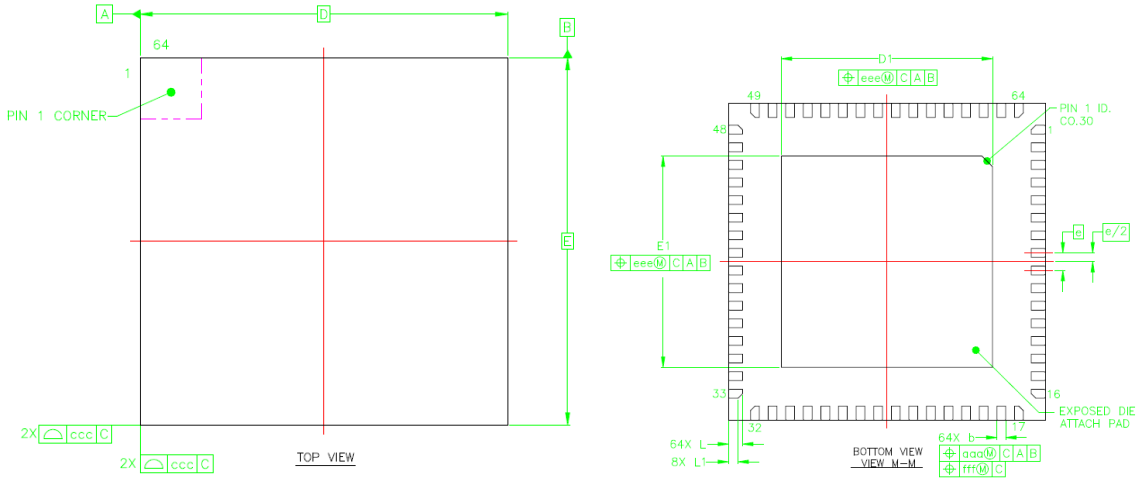
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	8.90	9.00	9.10	0.350	0.354	0.358
D2	4.89	4.99	5.09	0.193	0.196	0.200
E2	4.37	4.47	4.57	0.172	0.176	0.180
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.09	---	0.14	0.004	---	0.006
K	0.20	---	---	0.008	---	---
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

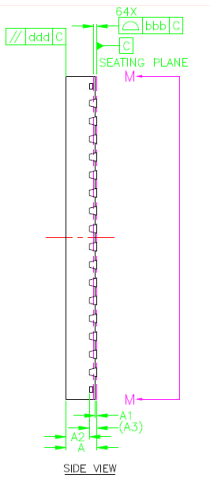
NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENCE DOCUMENT: JEDEC MO-220.

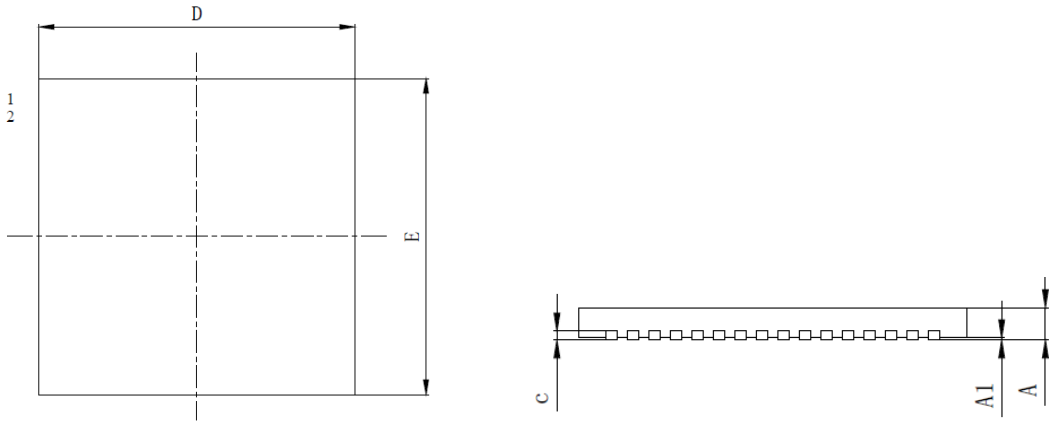
7.2 CSK4002 NAxxxxxxG

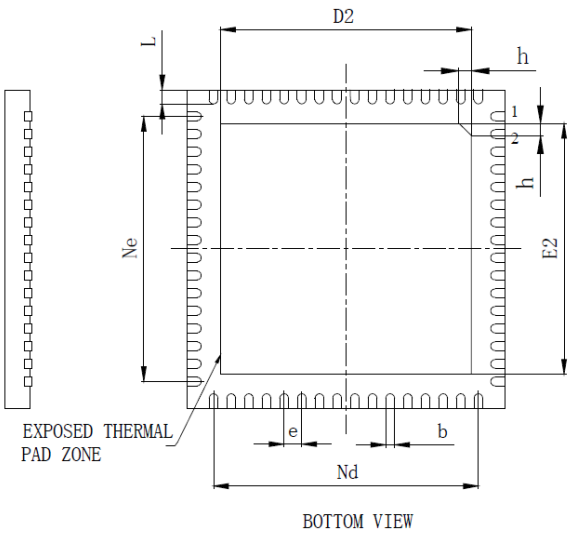




FOR CUSTOMER ONLY				
PACKAGE TYPE		QFN		
PIN COUNT		64		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0	0.035	0.050
MOLD THICKNESS	A2	–	0.65	0.67
MATERIAL THICKNESS	A3	–	0.203 REF	–
PACKAGE SIZE	D	8.90	9.00	9.10
	E	8.90	9.00	9.10
EP SIZE	D1	5.90	6.00	6.10
	E1	5.90	6.00	6.10
LEAD LENGTH	L	0.30	0.40	0.50
LEAD PITCH	e	0.5 BSC		
LEAD WIDTH	b	0.20	0.25	0.30
LEAD POSITION OFFSET	aaa	0.10		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.15		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		
	L1	0.171	0.271	0.371

7.3 CSK4002 NHxxxxxxG

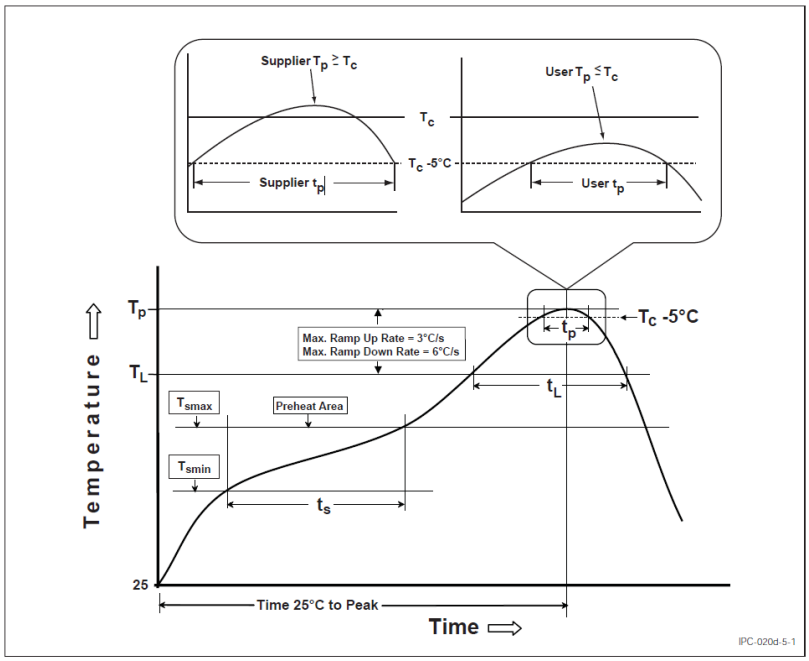




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	7.00	7.10	7.20
e	0.50BSC		
Ne	7.50BSC		
Nd	7.50BSC		
E	8.90	9.00	9.10
E2	7.00	7.10	7.20
L	0.35	0.40	0.45
h	0.30	0.35	0.40
载体尺寸（mil）	289*289/ 311*311		

8 Reflow profile

8.1 Reflow graph



8.2 SMT Reflow condition

Parameter	Requirement
N2 purge reflow usage	Yes
O2 ppm level	<1500 ppm
Temperature Min(T_{smin})	150℃
Temperature Max(T_{smax})	200℃
Time(t_s)from(T_{smin} to T_{smax})	60-120 seconds
Ramp-up rate(T_L to T_P)	3℃/second max
Liquidous temperature(T_L)	217℃
Time(t_L) maintained above T_L	60-150 seconds
Peak package body temperature(T_P)	Tp must not exceed the Classification temp（T_C） in table below
Time(t_p)within 5℃ of the specified classification temperature(T_C)	30 seconds max
Ramp-down rate(T_P to T_L)	6℃/second max
Time 25℃ to peak temperature	8 minutes max

Package Thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6mm	260℃	260℃	260℃
1.6mm-2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

9 Silk-Screen

Description:

- ○ represents Pin1 Mark position
- NHYYWWXXG is batch number
- N: reserved
- H: package factory
- YY: year
- WW: week
- XX: lot number
- G: environmental protection level--Green

10 Weight

240mg

11 Application Diagram