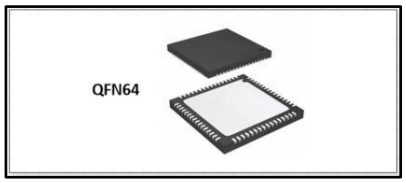
6011A
Datasheet V1.3

聆思科技
LISTENAI

6011A Datasheet

ARM Star&HIFI4 Dual Core, up to 8M PSRAM, QFN64

Datasheet - production data



- **Core**
  - ARM STAR，Maxim speed: 300MHz
  - HIFI4, Maxim speed 300MHz
  - NPU(128G), Maxim speed 300MHz
  - Hardware multiplier and hardware divider
  - Support 2wire(SWD) and 4 wire(JTAG) debug port
- **Memory**
  - 8MB PSRAM
  - Total 1MB internal SRAM(ARM&HIFI4 share)
- **Clock**
  - Programmable clock source select
    - External 24Mhz high speed crystal
    - External 32KHz low speed oscillator(option)
    - Internal 32KHz low speed oscillator
    - PLL up to 300Mhz
- **Power supply**
  - Single power 2.7V to 5.5V
- **Audio Codec**
  - 2 channel differential audio ADC input
  - 2 channel single-ended audio DAC output
- **General Digital IO**
  - Up to 33 general digital IO
- **Communication interface**
  - 1 DVP input
  - 4 UART standard communication port
  - 2 SPI standard communication port
  - 2 I2C standard communication port
  - 3 I2S standard communication port
  - 4 DMIC Input
  - 1 USB1.1 full speed Device
  - 1 SDIO standard communication port
  - 6 touch pad input support
- **General Purpose Timer**
  - 1 timer with 8 independent channels
  - Support 4 LEDC output and 8 PWM output
- **DVP**
  - Data Format: YUV422, YUV420, Raw Data
  - 8-bit to 12-bit configurable
  - Scalable image size (raw data specified):
    1280x720 / 60 fps
    640x480 / 120 fps
  - Higher rates are possible with smaller images
- **SAR ADC**
  - Up to 4 external channels input
  - 3 internal channels(1/6 VDD, 1/8 VCC, Keysense)
  - Resolution: 12bit, Sample Rate: 1MHz(Max)
- **Touch Pad**
  - Up to 6 touch pad input
- **IWDG**
  - 32KHz low speed oscillator
  - 32 bit free running counter
- **UART**
  - 4 UART interface
  - Infrared supported
- **Working Condition**
  - Working temperature: -40°C to +85°C
- **Development tools**
  - Full function embedded debugging environment
- **Package: QFN64**

Contents

Contents 3
1 General Description 5
2 Block Diagrams 5
3 PIN mapping and Description 6
3.1 Pin mapping 6
3.2 Pin descriptions 6
4 Function overview 10
4.1 Core 10
4.2 Memory 10
4.3 Clock Control 10
4.4 IO Port 10
4.5 GPT 10
4.6 SAR ADC 10
4.7 Audio Codec 11
4.8 DVP 11
4.9 IWDG 11
4.10 UART 11
4.11 SPI 11
4.12 I2C 12
4.13 RTC 12
4.14 NPU 12
4.15 FCC ram controller 12
4.16 PDM2PCM 12
4.17 CRYPTO 12
4.18 EFUSE controller 13
4.19 True random number generator 13
4.20 I2S interface 13
4.21 USB1.1 full speed Device 13
4.22 SDIO 13
4.23 Power Management Unit 13

4.24 Touch 14
5 Electrical characteristics 15
5.1 Parameter conditions 15
5.1.1 Minimum and Maximum values 15
5.1.2 Typical values 15
5.1.3 Loading capacitor 15
5.1.4 Pin input voltage 15
5.2 Operating conditions 15
5.2.1 Absolute maximum ratings 15
5.2.2 I/O port characteristics 16
5.2.3 IO AC characteristics 16
5.2.4 nRESET pin characteristics 17
5.2.5 Supply current characteristics 17
5.2.6 Wakeup time from sleep modes 17
5.2.7 External clock source characteristics 17
5.2.8 Internal clock source characteristics 17
5.2.9 PLL characteristics 18
5.2.10 EMC 18
6 Package information 18
6.1 QFN64(8*8mm) Package information 18
6.2 Thermal characteristics 19
7 Reflow profile 20
7.1 Reflow graph 20
7.2 SMT Reflow condition 20
8 Weight 21
9 Application Diagram 21

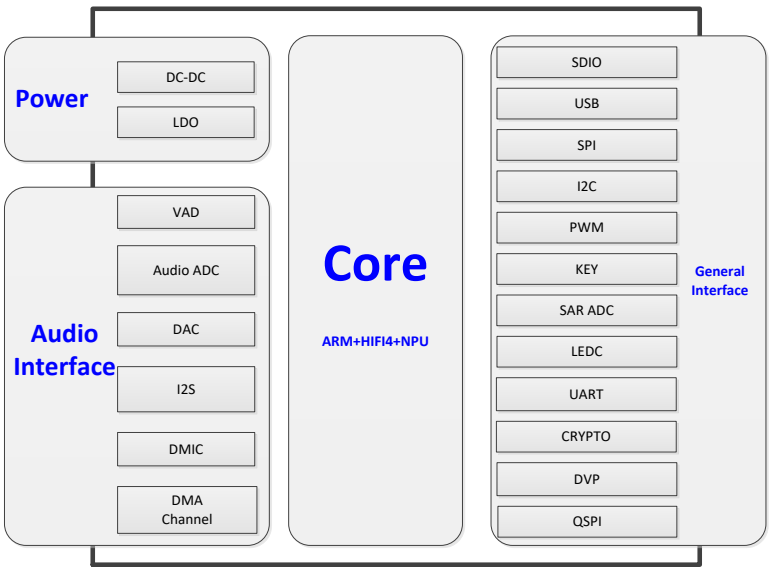
1 General Description

CSK6 serial is a dual core microcontroller with embedded ARM STAR core & HIFI4 core. ARM Star is designed for 32-bit microcontroller applications, offering performance, low power, simple instruction set and addressing together with reduced code size compared to exiting solutions. HIFI4 is designed for audio coder and decoder such as mp3, AAC, flac….. Independent NPU is designed for neural network operation.

Target applications: smart home appliance

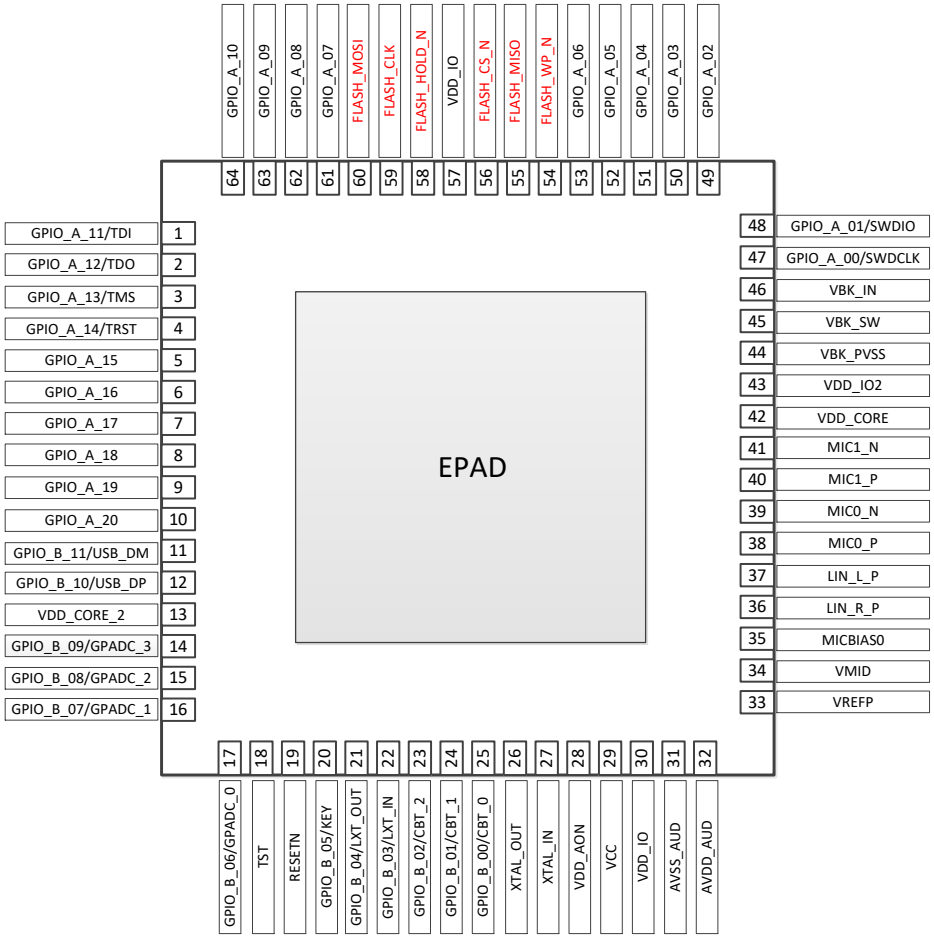
The CSK6 serial can run up to 300MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The CSK6 serial has up to 1M bytes internal data SRAM.
Many system level peripheral functions, such as IO port, DVP, Timer, Watchdog Timer, UART, SPI, I2C, DMA, PLL, USB1.1 (Full speed), RTC, SDIO are supported.

2 Block Diagrams



3 PIN mapping and Description

3.1 Pin mapping



3.2 Pin descriptions

Pin number	Pin name	Descriptions
1	GPIO_A_11	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
2	GPIO_A_12	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
3	GPIO_A_13	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
4	GPIO_A_14	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
5	GPIO_A_15	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions, (Boot ROM UART programming pin)
6	GPIO_A_16	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions

7	GPIO_A_17	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
8	GPIO_A_18	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions, (Boot ROM UART programming pin)
9	GPIO_A_19	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
10	GPIO_A_20	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
11	GPIO_B_11/USB_DM	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
12	GPIO_B_10/USB_DP	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
13	VDD_CORE_2	Should connect with VDD_CORE
14	GPIO_B_09/GPADC_3	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
15	GPIO_B_08/GPADC_2	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
16	GPIO_B_07/GPADC_1	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
17	GPIO_B_06/GPADC_0	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
18	TST	Test pin, default pull up. 0: test mode 1: normal mode
19	RESETN	Reset pin input, default pull up
20	GPIO_B_05/KEYSENSE	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
21	GPIO_B_04	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
22	GPIO_B_03	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
23	GPIO_B_02/CBT_2	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
24	GPIO_B_01/CBT_1	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
25	GPIO_B_00/CBT_0	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
26	XTAL_OUT	24MHz crystal
27	XTAL_IN	24MHz crystal
28	VAD_AON	Internal LDO output, 1uf cap recommended
29	VCC	Power input : 2.7V-5.5V
30	VDD_IO	Internal LDO output, 4.7uF cap recommended
31	AVSS_AUD	GND
32	AVDD_AUD	Internal LDO output, 2.2uF cap recommended

33	VREF	Audio codec reference input
34	VMID	Internal LDO output, 4.7uF cap recommended
35	MICBIAS0	Mic bias output，Cload=2.2uF
36	LIN_R_P	LINE right channel differential outputs positive
37	LIN_L_P	LINE left channel differential outputs positive
38	MIC0_P	Mic input positive
39	MIC0_N	Mic input negative
40	MIC1_P	Mic input positive
41	MIC1_N	Mic input negative
42	VDD_CORE	internal LDO output, 4.7uF cap recommended, should connect with VDD_CORE_2
43	VDD_IO2	Internal power output, 10uF cap recommended
44	VBK_PVSS	DC-DC GND
45	VBK_SW	DC-DC switch out, 3.3uH inductor connected
46	VBK_IN	DC-DC Input power: 2.7V-5.5V
47	GPIO_A_00/SWDCLK	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
48	GPIO_A_01/SWDTMS	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
49	GPIO_A_02	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
50	GPIO_A_03	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
51	GPIO_A_04	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
52	GPIO_A_05	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
53	GPIO_A_06	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
54	FLASH_WP_N	Connect with external QSPI Flash
55	FLASH_MISO	Connect with external QSPI Flash
56	FLASH_CS_N	Connect with external QSPI Flash
57	VDD_IO_1	Input power connect with VDD_IO
58	FLASH_HOLD_N	Connect with external QSPI Flash
59	FLASH_CLK	Connect with external QSPI Flash
60	FLASH_MOSI	Connect with external QSPI Flash
61	GPIO_A_7	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
62	GPIO_A_8	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
63	GPIO_A_9	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions

65	EPAD	Connect with GND

Note: pull up resister is configured as 80K

4 Function overview

4.1 Core

- ARM STAR&HIFI4 dual core runs up to 300 MHz
- Independent NPU
- Hardware multiplier and hardware divider.
- Embedded Debug Module supports serial debug port(2-wire) and JTAG debug(4-wire)

4.2 Memory

- External flash through QSPI interface
- Totally 1088KB SRAM shared by ARM and HIFI4
- Dedicated 96KB SRAM for NPU block

4.3 Clock Control

- Programmable system clock source.
- External 24 MHz high speed crystal input to provide reference clock for system.
- Internal 32 KHz low speed oscillator with calibration.
- PLL allows CPU operation up to 300MHz with the system oscillator.

4.4 IO Port

- GPIO configuration:
- Quasi-bidirectional (Pull-up Enable)
- Pull down
- Push-pull (Output)
- Input only (high-impedance)
- I/O pin can be configured as interrupt source with edge/level setting.
- Flexible IO function select.

4.5 GPT

The multi-function timer provides the following 6 usage scenarios depending on the Channel Mode register bit configurations

- Timer mode
- Input capture mode
- PWM mode
- LEDC output mode

4.6 SAR ADC

- 12-bit resolution, up to 1Msps, 24MHz ADC clock
- Configurable hardware ADC trigger sources
- User configurable n-times ADC sampling
- Dedicated ADC Data FIFO for each ADC channel

- Configurable ADC sampling duration
- Configurable waiting time for next Round A/D conversion
- switch on/off control
- ADC trimming
- ADC channel selection
- External/internal VREF selection

4.7 Audio Codec

- Audio sample rates support 8KHz to 96KHz in playback (DAC) path
- Audio sample rates support 8KHz，16KHz，44.1KHz or 48KHz in record (ADC) path
- DAC SNR about 95dB，THD -85dB (‘A’-weighted @ 8-48ks/s)
  ADC SNR about 95dB，THD -85dB (‘A’-weighted @ 8-48ks/s)
- 32bit APB Control Interface to ADC01separately.
- 32bit APB Control Interface to ADC23 and DAC01separately.
- Programmable gain setting and soft mute control in digital part
- Programmable ALC Loop / Noise Gate setting in ADC path
  Programmable ADC High Pass Filter (wind noise reduction included)
  Programmable ADC Notch Filter is selectable.
- Two stereo digital Microphone support for ADC01and ADC23.
- Output Gain/Volume and mute control

4.8 DVP

- Designed as an AHB Master component that can access the memory without DMAC service
- Image frame complete notice and buffer switching
- Support separate components 4:2:2 output format in line buffer for JPEG encoding.

4.9 IWDG

- Clocked from an internal 32 KHz low speed oscillator or from 32768Hz crystal if avalilable
- 32-bit free running counter
- Selectable timer-out interval

4.10 UART

- Four UART interface(1 for debug)
- Three UART Support the hardware flow control (CTS/RTS) so that WIFI can be supported through UART interface.
- Supports the hardware handshake for DMA.

4.11 SPI

- Three SPI interfaces
- One is used to support QSPI for external flash
- Supports the master mode and the slave mode.
- Supports memory mapped access (read-only) through AHB bus.
- Supports the hardware handshake for DMA.
- Supports the dual I/O and quad I/O modes(QSPI).

4.12 I2C

- Two I2C interface is available.
- Programmable to be a master or a slave device.
- Programmable clock/data timing.
- Supports the I2C-bus Standard-mode (100 kb/s), Fast-mode (400 kb/s) and Fast-mode plus (1 Mb/s).
- Supports the hardware handshake for DMA.
- Supports the master-transmit, master-receive, slave-transmit and slave-receive modes.
- Supports the multi-master mode.
- Supports 7-bit and 10-bit addressing.
- Supports general call addressing.
- Supports auto clock stretch.

4.13 RTC

- Supports software compensation by setting frequency compensate register
- The frequency of clock source (before the clock divider) for the counter is 32.768KHz.
- Separate second, minute, hour and day counters.
- Periodic interrupts: half-second, second, minute, hour and day interrupts.
- Programmable alarm interrupt with specified second, minute and hour numbers.

4.14 NPU

- Matrix and vector operation accelerator
- AHB master interface for data read and write
- APB interface for register configuration
- Has interrupt signals
- Support reverse order storage, overflow detection, shift location

4.15 FCC ram controller

- Arbitrate the data access request from CPU, HIFI4, NPU and DMAC
- Partition the NPU memory into several spaces
- If the access from different agents are in different spaces, all of them can be done without wait
- Flexible priority setting: If the accesses from different agents are in the same space, the priority can be set be user through register.

4.16 PDM2PCM

- Support data conversion of PDM data from digital microphone to standard PCM data
- CIC filter in always on domain, half-band and memory in main power domain

4.17 CRYPTO

- Support inside chip AES128 + SHA256 for secure communication
- AHB master interface for data read and write
- APB interface for register configuration

4.18 EFUSE controller

- Read EFuse content after receiving reset release signal from the reset sequence control
- Provide the data to Crypto engine for encryption/decryption usage
- Provide the data to QSPI encrypt wrapper to protect the content of NOR flash

4.19 True random number generator

- True random generator with mixed analog digital implementation to provide true random number
- Register configuration and generated random number can be accessed through APB bus

4.20 I2S interface

- Support extended microphone inputs
- Support I2S audio inputs and outputs
- 3 independent I2S modules
- Input or output signal can be TDM extended
- Register configuration and data operation through APB bus

4.21 USB1.1 full speed Device

- One set of USB 1.1 FS Device 12 Mbps
- On-chip USB Transceiver
- Supports Control, ISO in/out, Bulk in/out, Interrupt in/out transfers
- Provides 8 programmable endpoints
- Supports maximum 1K Bytes for isochronous transfer and maximum 64 Bytes for Bulk and interrupt transfer
- Each endpoint is configurable

4.22 SDIO

- Compliant with SD host controller standard specification, version 3.0
- Supports both DMA and non-DMA data transfers
- Compliant with SD physical layer specification, version 3.0
- Supports UHS50/UHS104 SD cards
- Supports configurable SD bus modes: 4-bit mode and 8-bit mode
- Compliant with SDIO card specification, version 3.0
- Compliant with eMMC card specification, version 5.1 mandatory part
- Supports configurable 1-bit/4-bit SD card bus and 1-bit/4-bit/8-bit EMMC card bus
- Configurable CPRM function for security
- Built-in generation and check for 7-bit and 16-bit CRC data
- Card detection (Insertion/Removal)

4.23 Power Management Unit

- Supports Sleep mode to reduce power consumption
- Supports the wake up through RTC, timer and Key-in from IO
- Supports the wake up through VAD
- Supports system wakeup through touch

4.24 Touch

- Supports touch point detection

4.25 Audio ADC&DMIC&I2S

- Audio adc share internal memory with DMIC, I2S

Occupied ADC/DAC	Available I2S	Available DMIC	Description
ADC01 only, no DAC	I2S1, I2S2	DMIC2, DMIC3	
ADC23 only, no DAC	I2S0, I2S1 or I2S2	DMIC0, DMIC1	I2S1 or I2S2 (either-or)
ADC01+ADC23, no DAC	I2S1 or I2S2	None	I2S1 or I2S2 (either-or)
ADC01 only, with DAC	I2S0, I2S2(IN)	DMIC2, DMIC3	I2S2(IN)
ADC23 only, with DAC	I2S0, I2S1 or I2S2(IN)	DMIC0, DMIC1	I2S1 or I2S2(IN) (either-or)
ADC01+ADC23, with DAC	I2S1 or I2S2(IN)	None	I2S1 or I2S2(IN) (either-or)

4.26 Boot mode

GPIOB0	GPIOB1	Mode Description
1	1	Nor Flash boot
1	0	UART
0	1	Reserved
0	0	DSP boot only

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

5.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at 25 °C and max temperature in the range.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, VCCIN = 5 V (for the 2.7 V ≤ VCCIN ≤ 5 V voltage range). They are given only as design guidelines and are not tested.

5.1.3 Loading capacitor

The loading capacitor used for pin parameter measurement is 10pf.

5.1.4 Pin input voltage

The input voltage measurement on a pin of the device is through current source device.

5.2 Operating conditions

5.2.1 Absolute maximum ratings

Table. Voltage Characteristics

Symbol	Ratings	Min	Max	Unit
$V_{CCIN} - V_{SS}$	External supply voltage	− 0.3	5.5	V
V_{IL}	Input Low Voltage on signal pin	-0.3	0.8	V
V_{IH}	Input High Voltage on signal pin(PortA)	2	5.5	V
V_{IH}	Input High Voltage on signal pin(PortB)	2	3.6	V
V_{OL}	Output Low Voltage on signal pin		0.4	V

V_{OH}	Output High Voltage on signal pin	2.4		V

5.2.2 I/O port characteristics

Table 6.2.2 I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Input low level voltage	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C	-0.3		0.8	V
V_{IH}	Standard IO input high level voltage(PortA)	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C	2		5.5	V
V_{IH}	Standard IO input high level voltage(PortB)	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C	2		3.6	V
V_{hys}	Standard IO Schmitt trigger voltage hysteresis	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		220		mV
V_{OL}	Output Low Voltage	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C			0.4	V
V_{OH}	Output High Voltage	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C	2.4			V
I_{OL}	Low Level Output Current	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		15		mA
I_{OH}	High Level Output Current	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		22		mA
I_{lkg}	Input leakage current	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		1		uA
R_{PU}	Pull up equivalent resistor		74k	80k	158k	Ω
R_{PD}	Pull down equivalent resistor		62k	75k	203k	Ω
C_{IO}	I/O pin capacitance			5		pF

Note: Only PORT A is 5V tolerance IO, Input voltage can be 5.5V maxium

5.2.3 IO AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{max(io)out}$	Maximum frequency	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C,C_L=10pf		100		MHz
$T_{f(IO)out}$	Output high to low level fall time and output low to high level rise time	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C, C_L=10pf		2.5		ns
		2.7V ≤ VCCIN ≤ 5.5V T_A=25°C, C_L=10pf		2.5		ns

5.2.4 nRESET pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Pull up equivalent resistor	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		80k		Ω
$V_{(nRESET)}$	nRESET input pulse	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C, C_L=10pf		1		ms

5.2.5 Supply current characteristics

Symbol	Parameter	Conditions	f_{sysclk}(MHz)	Typical	Unit
I_{DD}	Supply current in RUN mode	VCCIN = 5V, , External 24MHz T_A=25°C, PLL ON, AP ON, CP ON,NPU ON PSRAM off, nor flash cached	100	20	mA
	Supply current in VAD&DEEPSLEEP mode	T_A=25°C,deep sleep mode entered, VAD mode enabled with 1 audio ADC on(analog mic not included)	24	1.8	mA
	Supply current in DEEPSLEEP mode	T_A=25°C,deep sleep mode entered	24	700	uA

5.2.6 Wakeup time from sleep modes

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wakeup from Sleep	External pin wakeup(ROM boot not included)	<2	ms

5.2.7 External clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	External clock source frequency			24		MHz
V_{OSCH}	OSC IN input pin high level voltage			3.3		V
V_{OSCL}	OSC IN input pin low level voltage			0		V
$C_{IN(OSC)}$	OSC IN input capacitance			5		pF
$Ducy_{(OSC)}$	Duty cycle		45		55	%
I_L	OSC IN input leakage current			430		uA

5.2.8 Internal clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		32		KHz
$t_{su(LSI)}$	LSI oscillator startup time	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C		5		s

$I_{DD(LSI)}$	LSI oscillator power consumption	2.7V ≤ VCCIN ≤ 5.5V T_A=25°C			1	uA

5.2.9 PLL characteristics

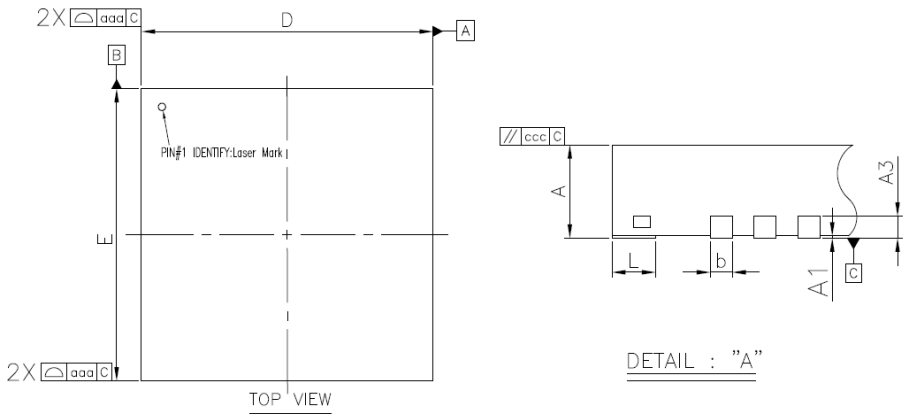
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock			24		MHz
f_{PLL_OUT}	PLL output clock			300		MHz
Jitter	Cycle-to cycle jitter			10		ps

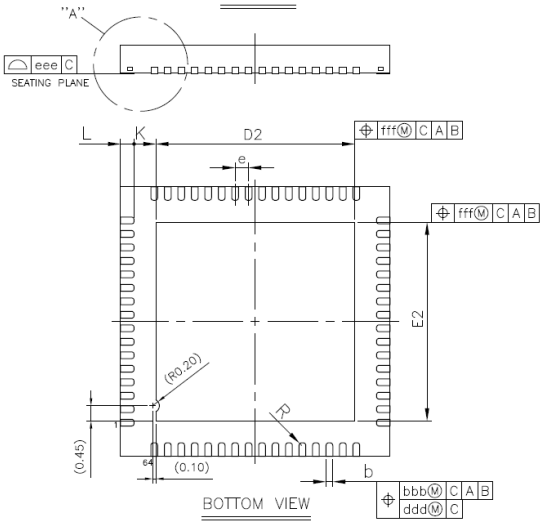
5.2.10 EMC

Symbol	Ratings	Conditions	Class	Maximum Value	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	T_A = 25℃	2	2000	V
VESD(CDM)	Electrostatic discharge voltage (charge device model)	T_A = 25℃		1000	V

6 Package information

6.1 QFN64(8*8mm) Package information





Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D2	5.80	5.90	6.00	0.228	0.232	0.236
E2	5.80	5.90	6.00	0.228	0.232	0.236
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.08	---	0.13	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

6.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \theta_{JA})$

where:

- T_A max is the maximum ambient temperature in ℃,
- θ_{JA} is the package junction-to-ambient thermal resistance, in ℃/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O} \text{ max} = \Sigma(V_{OL} \times I_{OL}) + ((V_{DD} - V_{OH}) \times I_{OH})$,

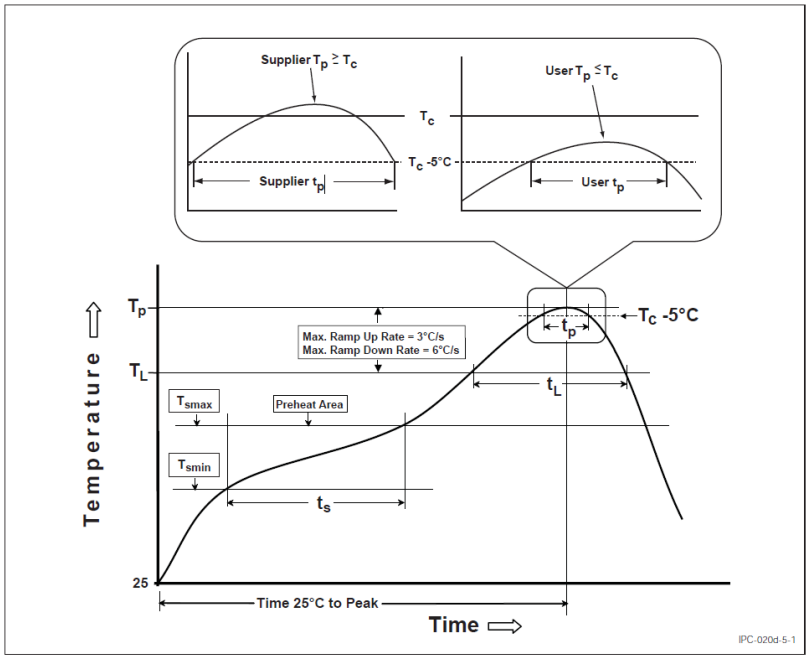
taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table: Package thermal characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	**Thermal resistance junction-ambient** QFN64 – 8*8 mm	28	℃/W
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

7 Reflow profile

7.1 Reflow graph



7.2 SMT Reflow condition

Parameter	Requirement
N2 purge reflow usage	Yes
O2 ppm level	<1500 ppm
Temperature Min(T_{smin})	150℃
Temperature Max(T_{smax})	200℃
Time(t_s)from(T_{smin} to T_{smax})	60-120 seconds
Ramp-up rate(T_L to T_P)	3℃/second max
Liquidous temperature(T_L)	217℃
Time(t_L) maintained above T_L	60-150 seconds
Peak package body temperature(T_P)	Tp must not exceed the Classification temp（T_C） in table below
Time(t_p)within 5℃ of the specified classification temperature(T_C)	30 seconds max
Ramp-down rate(T_P to T_L)	6℃/second max
Time 25℃ to peak temperature	8 minutes max

Package Thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
＜1.6㎜	260℃	260℃	260℃

1.6mm-2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

8 Weight

200mg

9 Application Diagram