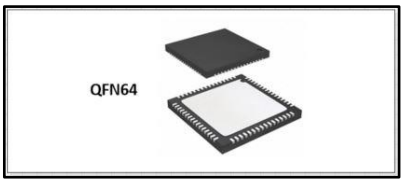
600X
Datasheet V0.3

600X Datasheet

ARM Star&HIFI4 Dual Core, up to 8 MB Flash, 8M SRAM, QFN64

Datasheet - production data

- **Core**
  - ARM STAR，Maxim speed: 300MHz
  - HIFI4, Maxim speed 300MHz
  - Hardware accelerator inside
  - Hardware multiplier and hardware divider
  - Support 2wire and 5 wire debug port
- **Memory**
  - 8MB Flash
  - 8MB PSRAM
  - Total 1MB internal SRAM
- **Clock**
  - Programmable clock source select
    - External 24Mhz high speed crystal
    - External 32KHz low speed oscillator(option)
    - Internal 32KHz low speed oscillator
    - PLL up to 300Mhz
- **Power supply**
  - Single power 2.7V to 5.5V
- **Audio Codec**
  - 4 channel differential audio ADC input
  - 2 channel differential audio DAC output
- **General Digital IO**
  - Up to 33 general digital IO
- **Communication interface**
  - 1 DVP input
  - 4 UART standard communication port
  - 2 SPI standard communication port
  - 2 I2C standard communication port
  - 3 I2S standard communication port
  - 4 DMIC Input
  - 1 USB1.1 full speed Device
  - 1 SDIO standard communication port
  - 6 touch pad input support



- **General Purpose Timer**
  - 2 timer with 8 independent channels
  - Support 4 LEDC output and 8 PWM output
- **DVP**
  - VGA@120fps
- **SAR ADC**
  - Up to 8 channels input
  - Resolution: 12bit, Sample Rate: 1MHz
- **IWDG**
  - 32KHz low speed oscillator
  - 32 bit free running counter
- **UART**
  - 4 UART interface
  - Infrared supported
- **Working Condition**
  - Working temperature: -40°C to +85°C
- **Development tools**
  - Full function embedded debugging environment
- **Package: QFN64**

Contents

1 General Description

600X is a dual core microcontroller with embedded ARM STAR core & HIFI4 core. ARM Star is designed for 32-bit microcontroller applications, offering performance, low power, simple instruction set and addressing together with reduced code size compared to exiting solutions. HIFI4 is designed for audio coder and decoder such as mp3, AAC, flac….. Independent NPU is designed for neural network operation.

Target applications: smart home appliance

The 600X can run up to 300MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The 600X has up to 1M bytes internal data SRAM and can support large external flash through QSPI and OPI interface.
Many system level peripheral functions, such as IO port, Timer, Watchdog Timer, UART, SPI, I2C, DMA, PLL, USB1.1 (Full speed), RTC, Quad SPI, SDIO are supported.

2 Function overview

2.1 Core

- ARM STAR&HIFI4 dual core runs up to 300 MHz
- Independent NPU
- Hardware multiplier and hardware divider.
- Embedded Debug Module supports serial debug port(2-wire) and JTAG debug(5-wire)

2.2 Memory

- External flash through QSPI interface
- Totally 1088KB SRAM shared between ARM and HIFI4
- Dedicated 96KB SRAM for NPU block

2.3 Clock Control

- Programmable system clock source.
- External 24 MHz high speed crystal input to provide reference clock for system.
- Internal 32 KHz low speed oscillator with calibration.
- PLL allows CPU operation up to 300MHz with the system oscillator.

2.4 IO Port

- Up to 33 general-purpose I/O(GPIO) pins.
- GPIO configuration:
- Quasi-bidirectional (Pull-up Enable)
- Push-pull (Output)
- Input only (high-impedance)
- I/O pin can be configured as interrupt source with edge/level setting.
- Flexible IO function select.

2.5 GPT

The multi-function timer provides the following 6 usage scenarios depending on the ChMode register bit configurations

- one 32-bit timer.
- two 16-bit timers.
- four 8-bit timers.
- one 16-bit PWM.
- one 16-bit timer and one 8-bit PWM.
- two 8-bit timers and one 8-bit PWM

The features of the GPT controller include:

- Supports AMBA 2.0 APB bus.
- Each multi-function timer provides 6 usage scenarios (combinations of timer and PWM).
- Each GPT supports up to 4 multi-function timers.
- Programmable source of timer clock.
- LEDC supported

2.6 SAR ADC

- 12-bit resolution, up to 8 channels, up to 1Msps, 24MHz ADC clock
- Configurable hardware ADC trigger sources
- User configurable n-times ADC sampling
- Dedicated ADC Data FIFO for each ADC channel
- Configurable ADC sampling duration
- Configurable waiting time for next Round A/D conversion
- ADC configuration and test logic
- switch on/off control
- ADC trimming
- ADC channel selection
- External/internal VREF selection

2.7 Audio Codec

- Audio sample rates support 8KHz to 48KHz in playback (DAC) path
- Audio sample rates support 8KHz，16KHz，44.1KHz or 48KHz in record (ADC) path
- DAC SNR about 95dB，THD -85dB (‘A’-weighted @ 8-48ks/s)
  ADC SNR about 95dB，THD -85dB (‘A’-weighted @ 8-48ks/s)
- 32bit APB Control Interface to ADC01separately.
- 32bit APB Control Interface to ADC23 and DAC01separately.
- Programmable gain setting and soft mute control in digital part
- Programmable ALC Loop / Noise Gate setting in ADC path
  Programmable ADC High Pass Filter (wind noise reduction included)
  Programmable ADC Notch Filter is selectable.
- Two stereo digital Microphone support for ADC01and ADC23.
- Output Gain/Volume and mute control

2.8 DVP

- AMBA2.0 compatible interface
- Designed as an AHB Master component that can access the memory without DMAC service
- Image frame complete notice and buffer switching
- Support separate components 4:2:2 output format in line buffer for JPEG encoding.

2.9 IWDG

- Clocked from an internal 32 KHz low speed oscillator or from 32768HZ crystal if avalilable
- 32-bit free running counter
- Selectable timer-out interval

2.10 UART

- Four UART interface(1 for debug)
- Two UART Support the hardware flow control (CTS/RTS) so that WIFI can be supported through UART interface.
- Supports the hardware handshake for DMA.

2.11 SPI

- Three SPI interfaces (1 QSPI for flash, the other two SPI to share with UART and PWM)
- One can be used to support QSPI for external flash
- The other two can be configured to 3 wire SPI
- Supports the master mode and the slave mode.
- Supports memory mapped access (read-only) through AHB bus.
- Supports the hardware handshake for DMA.
- Supports the dual I/O and quad I/O modes.
- Supports the 3-line mode.

2.12 I2C

- Two I2C interface is available.
- Programmable to be a master or a slave device.
- Programmable clock/data timing.
- Supports the I2C-bus Standard-mode (100 kb/s), Fast-mode (400 kb/s) and Fast-mode plus (1 Mb/s).
- Supports the hardware handshake for DMA.
- Supports the master-transmit, master-receive, slave-transmit and slave-receive modes.
- Supports the multi-master mode.
- Supports 7-bit and 10-bit addressing.
- Supports general call addressing.
- Supports auto clock stretch.

2.13 RTC

- Supports software compensation by setting frequency compensate register
- The frequency of clock source (before the clock divider) for the counter is 32.768KHz.
- Separate second, minute, hour and day counters.
- Periodic interrupts: half-second, second, minute, hour and day interrupts.

- Programmable alarm interrupt with specified second, minute and hour numbers.

2.14 NPU

- Matrix and vector operation accelerator
- AHB master interface for data read and write
- APB interface for register configuration
- Has interrupt signals
- Support reverse order storage, overflow detection, shift location

2.15 FCC ram controller

- Arbitrate the data access request from CPU, HIFI4, NPU and DMAC
- Partition the NPU memory into several spaces
- If the access from different agents are in different spaces, all of them can be done without wait
- Flexible priority setting: If the accesses from different agents are in the same space, the priority can be set be user through register.

2.16 PDM2PCM

- Support data conversion of PDM data from digital microphone to standard PCM data
- CIC filter in always on domain, half-band and memory in main power domain

2.17 CRYPTO

- Support inside chip AES128 + SHA256 for secure communication
- AHB master interface for data read and write
- APB interface for register configuration

2.18 EFUSE controller

- Read EFuse content after receiving reset release signal from the reset sequence control
- Provide the data to Crypto engine for encryption/decryption usage
- Provide the data to QSPI encrypt wrapper to protect the content of NOR flash

2.19 True random number generator

- True random generator with mixed analog digital implementation to provide true random number
- Register configuration and generated random number can be accessed through APB bus

2.20 I2S interface

- Support extended microphone inputs
- Support I2S audio inputs and outputs
- 3 independent I2S modules
- Input signal can be TDM extended to support more microphone inputs
- Register configuration and data operation through APB bus

2.21 USB1.1 full speed Device

- One set of USB 1.1 FS Device 12 Mbps

- On-chip USB Transceiver
- Supports Control, ISO in/out, Bulk in/out, Interrupt in/out transfers
- Provides 8 programmable endpoints
- Supports maximum 1K Bytes for isochronous transfer and maximum 64 Bytes for Bulk and interrupt transfer
- Each endpoint is configurable

2.22 SDIO

- Compliant with SD host controller standard specification, version 3.0
- Supports both DMA and non-DMA data transfers
- Compliant with SD physical layer specification, version 3.0
- Supports UHS50/UHS104 SD cards
- Supports configurable SD bus modes: 4-bit mode and 8-bit mode
- Compliant with SDIO card specification, version 3.0
- Compliant with eMMC card specification, version 5.1 mandatory part
- Supports configurable 1-bit/4-bit SD card bus and 1-bit/4-bit/8-bit EMMC card bus
- Configurable CPRM function for security
- Built-in generation and check for 7-bit and 16-bit CRC data
- Card detection (Insertion/Removal)

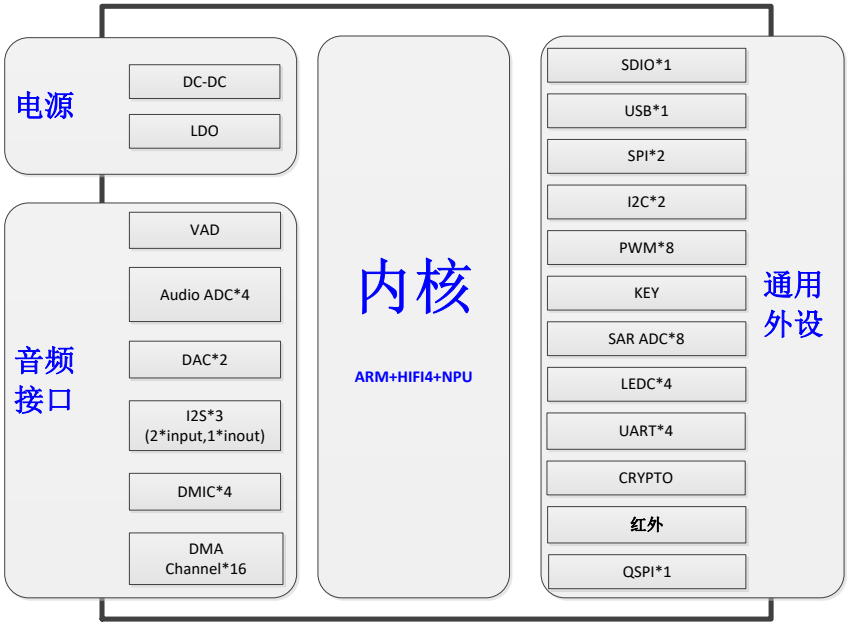
2.23 Power Management Unit

- Supports Sleep mode to reduce power consumption
- Supports the wake up through RTC and Key-in from IO
- Supports the wake up through VAD
- Supports system wakeup through touch

2.24 Touch

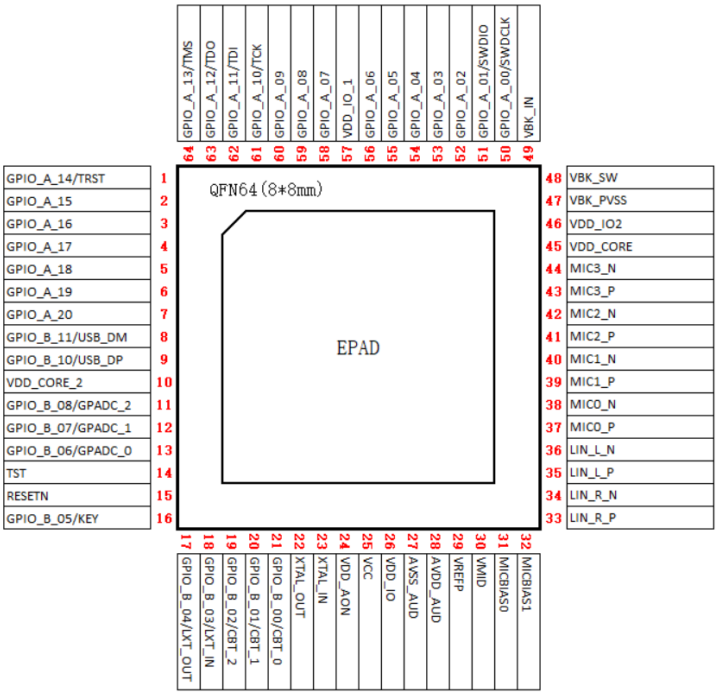
- Supports up to 6 touch point detection

3 Block Diagram



4 PIN mapping and Description

4.1 Pin mapping



4.2 Pin descriptions

Pin number	Pin name	Descriptions
1	GPIO_A_14	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
2	GPIO_A_15	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
3	GPIO_A_16	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
4	GPIO_A_17	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
5	GPIO_A_18	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
6	GPIO_A_19	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
7	GPIO_A_20	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
8	GPIO_B_11	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
9	GPIO_B_10	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
10	VDD_CORE_2	芯片内核供电输入引脚，建议外接 1uF 电容
11	GPIO_B_08	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
12	GPIO_B_07	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
13	GPIO_B_06	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
14	TST	测试功能引脚
15	RESETN	复位引脚输入
16	GPIO_B_05	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
17	GPIO_B_04	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
18	GPIO_B_03	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
19	GPIO_B_02	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
20	GPIO_B_01	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
21	GPIO_B_00	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
22	XTAL_OUT	24MHz 晶体引脚
23	XTAL_IN	24MHz 晶体引脚
24	VAD_AON	芯片内部 LDO 输出，建议外接 1uF 电容
25	VCC	芯片电源输入，2.7V-5.5V（和 49 管脚共同作为整个芯片的电源输入，接 10uF）
26	VDD_IO	芯片内部 LDO 输出，建议外接 1uF 电容
27	AVSS_AUD	地引脚
28	AVDD_AUD	芯片内部 LDO 输出，建议外接 2.2uF 电容
29	VREF	音频 Codec 的外部参考输入
30	VMID	内部输出电压，建议外接 4.7uF 电容
31	MICBIAS0	麦克风偏置电压输出，建议外接 2.2uF 电容
32	MICBIAS1	麦克风偏置电压输出，建议外接 2.2uF 电容
33	LIN_R_P	LINE 右声道输出差分正端
34	LIN_R_N	LINE 右声道输出差分负端
35	LIN_L_P	LINE 左声道输出差分正端
36	LIN_L_N	LINE 左声道输出差分负端
37	MIC0_P	麦克风输入正端
38	MIC0_N	麦克风输入负端

39	MIC1_P	麦克风输入正端
40	MIC1_N	麦克风输入负端
41	MIC2_P	麦克风输入正端
42	MIC2_N	麦克风输入负端
43	MIC3_P	麦克风输入正端
44	MIC3_N	麦克风输入负端
45	VDD_CORE	内部 LDO 输出，建议外接 1uF 电容
46	VDD_IO2	内部电压输出，建议外接 10uF 电容
47	VBK_PVSS	地引脚
48	VBK_SW	与 VBK_IN 连接在一起，外界 3.3uH 电感
49	VBK_IN	芯片电源输入，2.7V-5.5V（和 25 管脚共同作为整个芯片的电源输入，接 10uF）
50	GPIO_A_00	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
51	GPIO_A_01	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
52	GPIO_A_02	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
53	GPIO_A_03	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
54	GPIO_A_04	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
55	GPIO_A_05	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
56	GPIO_A_06	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
57	VDD_IO_1	电源输入，与 26PIN VDD_IO 连接
58	GPIO_A_07	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
59	GPIO_A_08	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
60	GPIO_A_09	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
61	GPIO_A_10	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
62	GPIO_A_11	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
63	GPIO_A_12	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明
64	GPIO_A_13	通用数字功能引脚，共 16 种复用功能，详细复用参见 excel 说明

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to Vss.

5.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at 25 °C and max temperature in the range.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, VCCIN = 5 V (for the 3.0 V ≤ VCCIN ≤ 5 V voltage range). They are given only as design guidelines and are not tested.

5.1.3 Loading capacitor

The loading capacitor used for pin parameter measurement is 50pf.

5.1.4 Pin input voltage

The input voltage measurement on a pin of the device is through current source device.

5.2 Operating conditions

6 Package information

QFN64

7 Application Diagram