AXI总线简介

协议与通道

两种节点

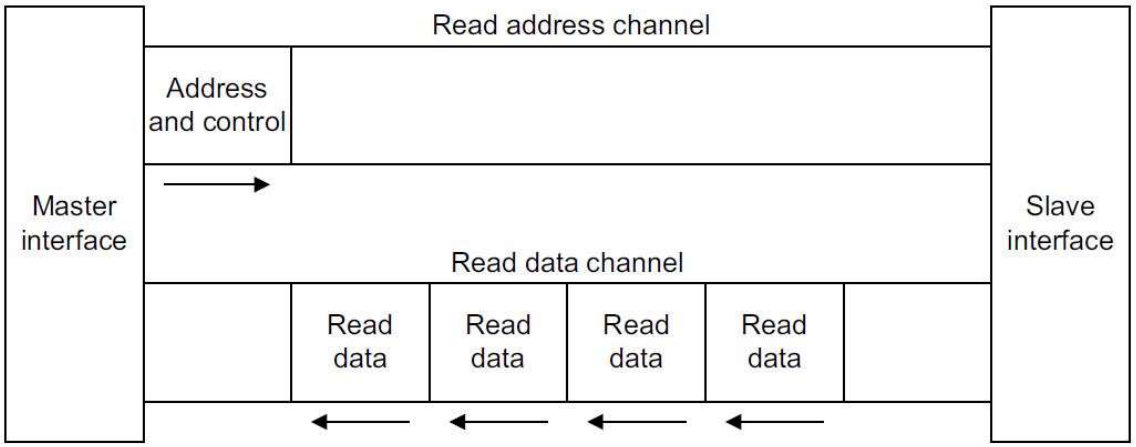
AXI协议是一种主从协议，它包含两类节点:

- **Master Interface**: 发起读写命令
- **Slave Interface**: 响应读写命令

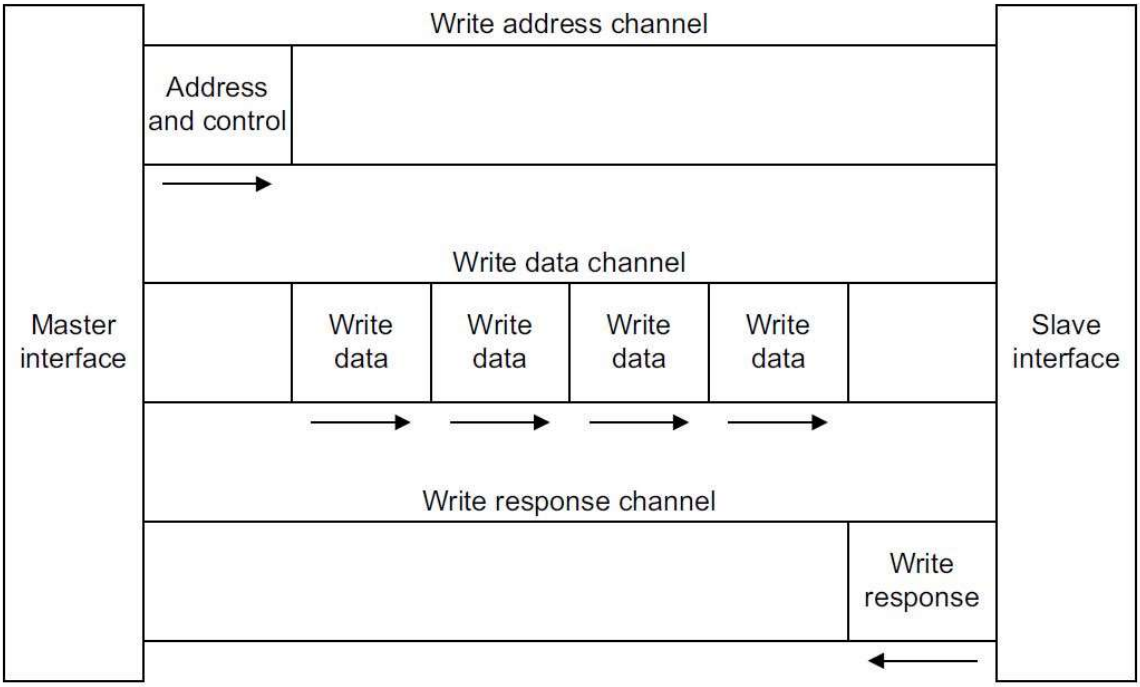
五个通道

一套主从设备包含五个通道:

- **read address**:从master到slave，发送读取数据的地址及控制信号
- **read data**:从slave到master，返回读数据



- **write address**:从master到slave，发送写数据的地址及控制信号
- **write data**:从master到slave，发送写数据
- **write response**:从slave到master，返回写完成信号



多通道设计充分考虑**效率**，通道间采用**握手**方式同步。

总线信号

五个通道的所有信号

全局信号

Table 2-1 Global signals

Signal	Source	Description
ACLK	Clock source	Global clock signal. All signals are sampled on the rising edge of the global clock.
ARESETn	Reset source	Global reset signal. This signal is active LOW.

读地址通道(以AR开头)

Table 2-5 Read address channel signals

Signal	Source	Description
ARID[3:0]	Master	Read address ID. This signal is the identification tag for the read address group of signals.
ARADDR[31:0]	Master	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
ARLEN[3:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. See Table 4-1 on page 4-3.
ARSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. See Table 4-2 on page 4-4.
ARBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. See Table 4-3 on page 4-5.
ARLOCK[1:0]	Master	Lock type. This signal provides additional information about the atomic characteristics of the transfer. See Table 6-1 on page 6-2.
ARCACHE[3:0]	Master	Cache type. This signal provides additional information about the cacheable characteristics of the transfer. See Table 5-1 on page 5-3.
ARPROT[2:0]	Master	Protection type. This signal provides protection unit information for the transaction. See *Protection unit support* on page 5-5.
ARVALID	Master	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid and will remain stable until the address acknowledge signal, **ARREADY**, is high. 1 = address and control information valid 0 = address and control information not valid.
ARREADY	Slave	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

读数据通道(以R开头)

Table 2-6 Read data channel signals

Signal	Source	Description
RID[3:0]	Slave	Read ID tag. This signal is the ID tag of the read data group of signals. The **RID** value is generated by the slave and must match the **ARID** value of the read transaction to which it is responding.
RDATA[31:0]	Slave	Read data. The read data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide.
RRESP[1:0]	Slave	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
RLAST	Slave	Read last. This signal indicates the last transfer in a read burst.
RVALID	Slave	Read valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = read data available 0 = read data not available.
RREADY	Master	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready 0 = master not ready.

写地址通道(以AW开头)

Table 2-2 Write address channel signals

Signal	Source	Description
AWID[3:0]	Master	Write address ID. This signal is the identification tag for the write address group of signals.
AWADDR[31:0]	Master	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
AWLEN[3:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. See Table 4-1 on page 4-3.
AWSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update. See Table 4-2 on page 4-4.
AWBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. See Table 4-3 on page 4-5.
AWLOCK[1:0]	Master	Lock type. This signal provides additional information about the atomic characteristics of the transfer. See Table 6-1 on page 6-2.
AWCACHE[3:0]	Master	Cache type. This signal indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction. See Table 5-1 on page 5-3.
AWPROT[2:0]	Master	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access. See *Protection unit support* on page 5-5.
AWVALID	Master	Write address valid. This signal indicates that valid write address and control information are available: 1 = address and control information available 0 = address and control information not available. The address and control information remain stable until the address acknowledge signal, **AWREADY**, goes HIGH.
AWREADY	Slave	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

写数据通道(以W开头)

Table 2-3 Write data channel signals

Signal	Source	Description
WID[3:0]	Master	Write ID tag. This signal is the ID tag of the write data transfer. The **WID** value must match the **AWID** value of the write transaction.
WDATA[31:0]	Master	Write data. The write data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide.
WSTRB[3:0]	Master	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore, **WSTRB[n]** corresponds to **WDATA[(8 × n) + 7:(8 × n)]**.
WLAST	Master	Write last. This signal indicates the last transfer in a write burst.
WVALID	Master	Write valid. This signal indicates that valid write data and strobes are available: 1 = write data and strobes available 0 = write data and strobes not available.
WREADY	Slave	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready 0 = slave not ready.

写响应通道(以B开头)

Table 2-4 Write response channel signals

Signal	Source	Description
BID[3:0]	Slave	Response ID. The identification tag of the write response. The **BID** value must match the **AWID** value of the write transaction to which the slave is responding.
BRESP[1:0]	Slave	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
BVALID	Slave	Write response valid. This signal indicates that a valid write response is available: 1 = write response available 0 = write response not available.
BREADY	Master	Response ready. This signal indicates that the master can accept the response information. 1 = master ready 0 = master not ready.

几点说明

- `ID`信号指示的是传输任务序号，`Master`可以设置传输任务的序号指示执行的顺序:
  - 来自同一个`Master`，同一个序号的指令只能顺序执行;
  - 来自同一`Master`不同序号的或来自不同`Master`的传输任务没有执行顺序的要求;
  - 因此当存在明确的先后顺序时，可以用相同的任务`ID`标识。
- `VALID`信号表明地址、数据有效，`READY`表明接收方准备好接收请求、数据，这是一组握手信号。**VALID置有效不依赖于READY信号。**
- `LAST`信号指示最后一个写数据或最后一个读数据,它与最后一个数据的`VALID`信号同步拉高。
- `AXI`中的`ADDRESS`信号指的是**起始地址**，需要配合以下信号来使用:
  - `LEN`：表明一次传输的长度`(beat number)`;

Table 4-1 Burst length encoding

ARLEN[3:0] AWLEN[3:0]	Number of data transfers
b0000	1
b0001	2
b0010	3
. . .	
b1101	14
b1110	15
b1111	16

- `SIZE`：表明每一拍数据的字节数，大于总线上`DATA`宽度的传输会通过固定地址分多次传输的方式实现,小于则通过选通信号实现;

Table 4-2 Burst size encoding

ARSIZE[2:0] AWSIZE[2:0]	Bytes in transfer
b000	1
b001	2
b010	4
b011	8
b100	16
b101	32
b110	64
b111	128

- `BRUST`：表明传输的类型;

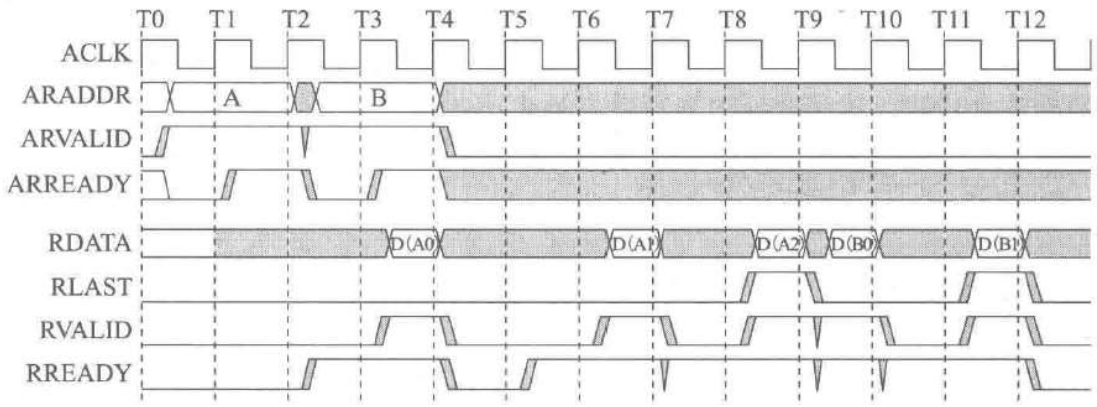
Table 4-3 Burst type encoding

ARBURST[1:0] AWBURST[1:0]	Burst type	Description	Access
b00	FIXED	Fixed-address burst	FIFO-type
b01	INCR	Incrementing-address burst	Normal sequential memory
b10	WRAP	Incrementing-address burst that wraps to a lower address at the wrap boundary	Cache line
b11	Reserved	-	-

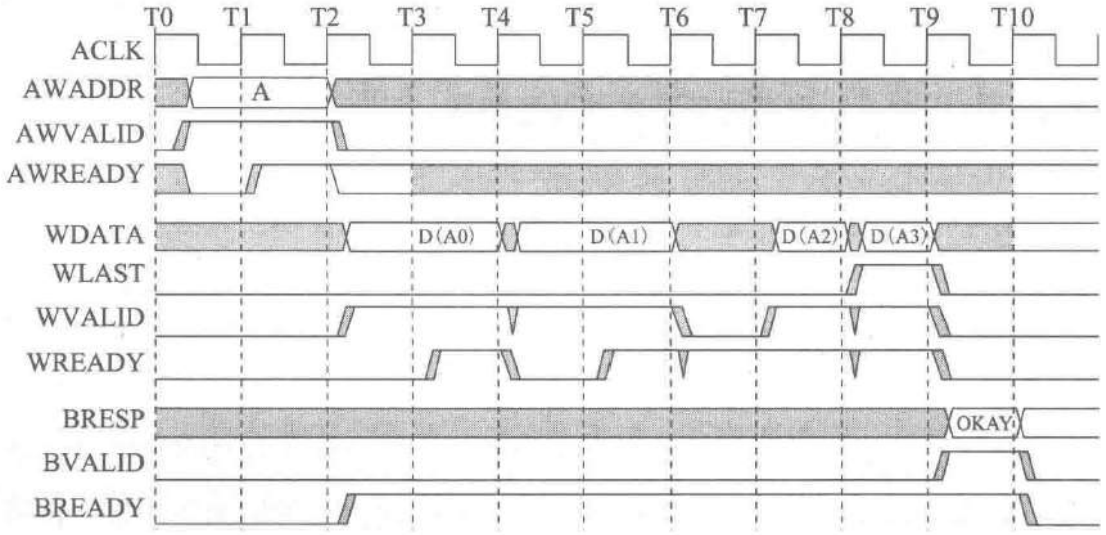
- `AXI`协议是按照**字节**寻址，写数据中有一个字节选通位`WSTRB`.
  - `WSTRB[n]=1`时，表明`DATA`[`8n+7`:`8n`]有效.
- 在`AXI`协议中，一但传输开始便无法停止，必须等待指定`len`长度的传输完成，如果想要丢弃读数据，`Master`只需要将读到的数据忽略即可；如果要丢弃写数据，将对应数据的选通位置`0`即可。

例子

连续读事务



写事务

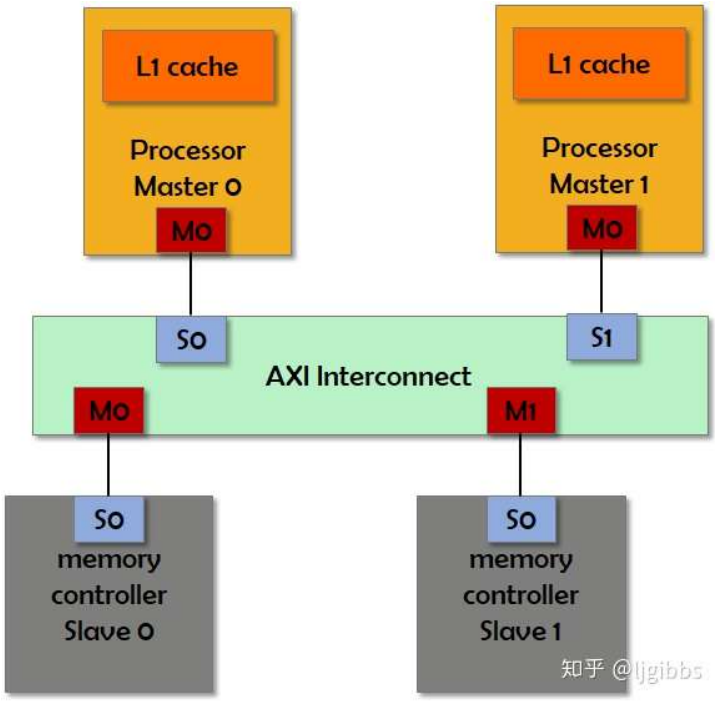


传输事务

- 一次总线事务`(Transaction)`对应于一次完整的读或者写过程；
- 一次总线传输`(Transfer)`指的是`vaild`和`ready`信号同时有效的那个周期；
- 一个总线事务包含多个总线传输.

Interconnect

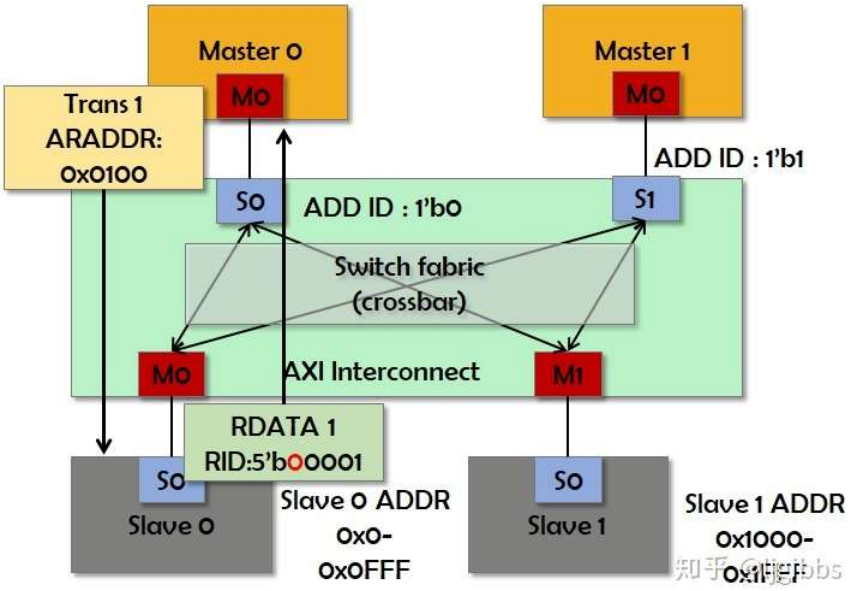
多`Master`多`Slave`场景，需要一个`AXI Interconnect`模块作为中间层。



Interconnect的功能

转发

`Interconnect`内部使用交叉总线连接每一个主机与从机端口，交叉总线的选通由其上的交换结构`(switch fabric)`控制，又称交叉开关`(crossbar)`，结构如下图所示：

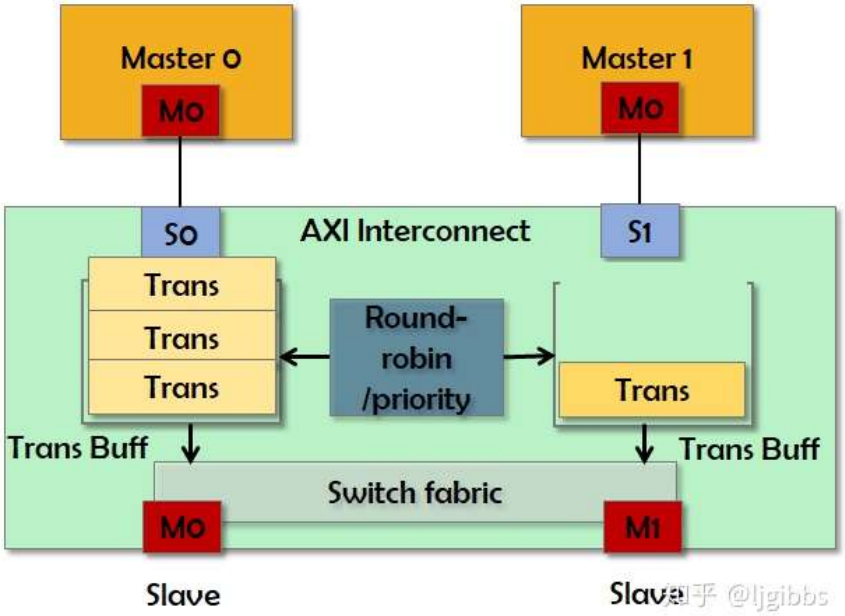


`Interconnect`在接收`Master`发起的传输事务后，`Interconnect`会在该事务`ID`上增加额外字段标识其`Master`端口信息,接着根据地址信号`AxADDR`，转发至对应的`Slave`端口.

`Slave`的地址映射在设计阶段确定，实现后硬编码至`Interconnect`的转发逻辑。

多机仲裁

由于不同主机间的传输事务互相独立，因此有可能不同主机会同时产生传输事务。仲裁`(arbiter)`电路需要决定当前从哪个非空的缓冲区读取事务，输入交换结构。



就`Master`的仲裁主要有`2`种策略:

- 轮询`(round-robin)`，轮流从各个`Master`的缓存通道读取事务。
- 优先级仲裁`(priority)`，优先读取高优先级缓存通道中的事务。

同时对于`Slave`输入的数据，`Interconnect`也有相同的缓存与仲裁结构。

读数据重排序

在多机通信中，`Master`可能向多个`Slave`发出了`ID`一致的传输事务，此时由`Interconnect`负责保证数据返回`Master`的顺序，与`Master`发出事务的顺序一致。这就要求`Interconnect`具有同`Slave`类似的缓存功能以实现重排序。

其它功能

- 总线位宽转换
- 时钟域转换
- `AXI`协议转换
- ……

`Vivado`中有`AXI Interconnect` `IP`可以直接使用