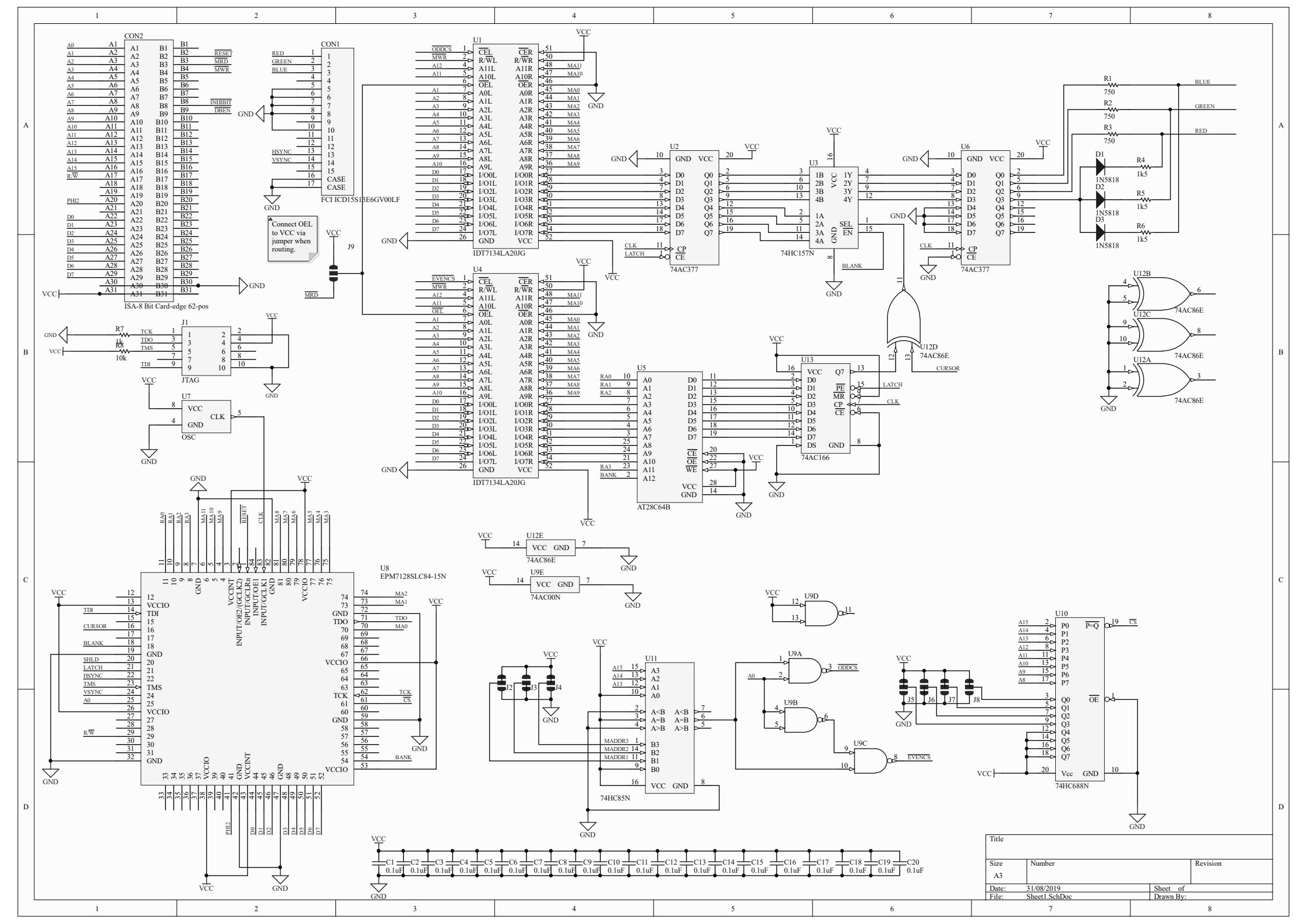
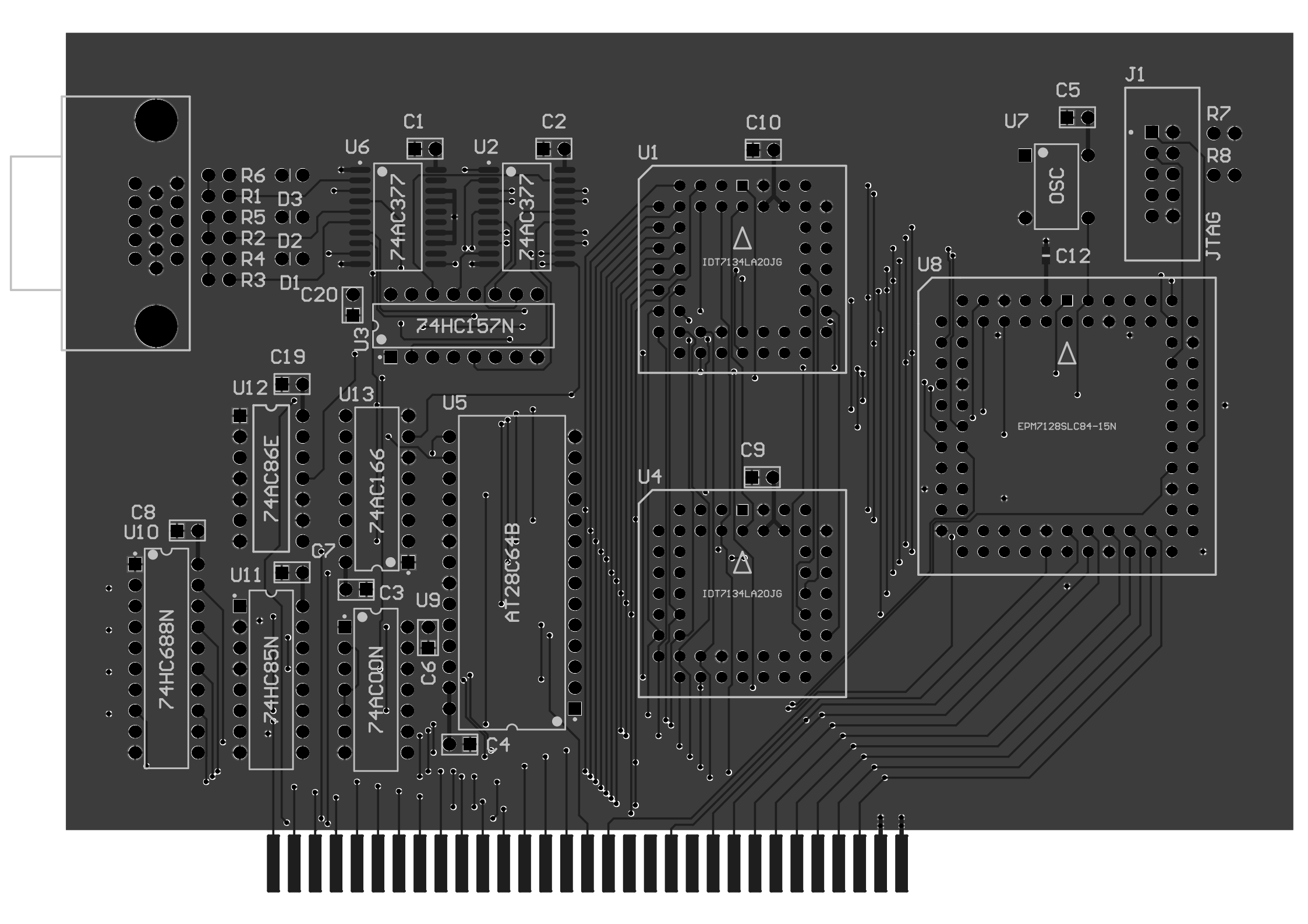
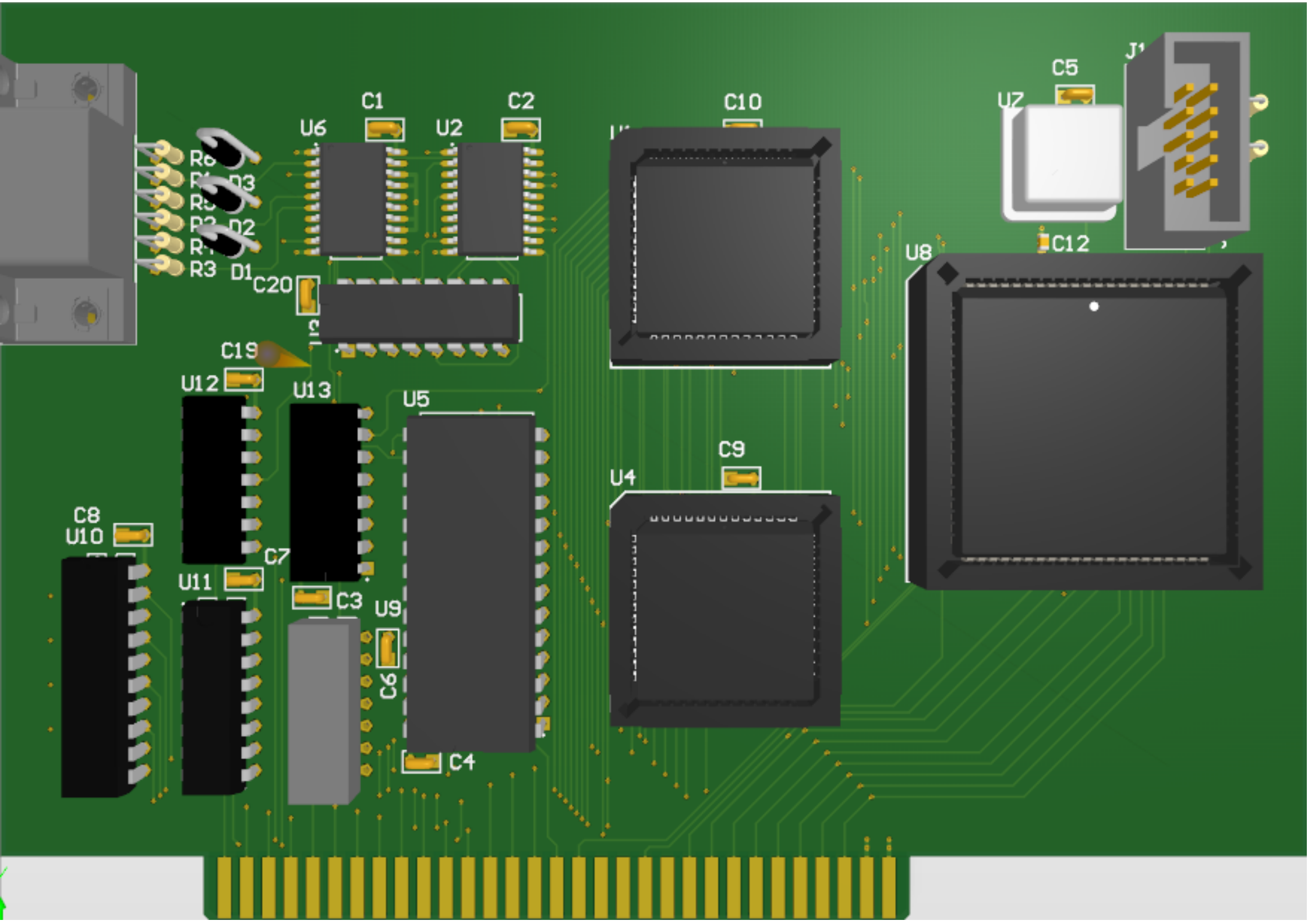

CON2
ISA-8 Bit Card-edge 62-pos
CON1
FCI ICD15S13E6GV00LF
Connect OEL to VCC via jumper when routing.
U1
U2
U3
U4
U5
U6
IDT7134LA20JG
74AC377
74HC157N
AT28C64B
U7
OSC
J1
JTAG
U8
EPM7128SLC84-15N
U9A
U9B
U9C
U9D
U9E
74AC00N
U10
74HC688N
U11
74HC85N
U12A
U12B
U12C
U12D
U12E
74AC86E
U13
74AC166
R1
R2
R3
R4
R5
R6
R7
R8
750
1k5
1k
10k
1N5818
BLUE
GREEN
RED
CURSOR
LATCH
CLK
BLANK
VCC
GND
Title
Size
A3
Number
Revision
Date:
31/08/2019
Sheet of
File:
Sheet1.SchDoc
Drawn By:


R6
R1
R5
R2
R4
R3
D3
D2
D1
C1
C2
U6
U2
74AC377
74AC377
C20
U3
74HC157N
C19
U12
74AC86E
U13
74AC166
U5
AT28C64B
C7
C3
U9
C6
C4
U11
74HC85N
74AC00N
C8
U10
74HC688N
U1
C10
IDT7134LA20JG
U4
C9
IDT7134LA20JG
U7
C5
OSC
C12
U8
EPM7128SLC84-15N
J1
JTAG
R7
R8


C1
C2
C5
C10
C12
C19
C20
C3
C4
C6
C7
C8
C9
D1
D2
D3
J1
R1
R2
R3
U2
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13

Design Rules Verification Report

Filename : C:\ProgramData\Altium\CircuitMaker {0C27520B-6165-4CC0-A894-E2CEC9A420C8}\Projects\9F2A2FF7-EBF2-4E61-8DD4-3DEAB783A5D4\d441547d-5a42-4e30-b991-4ffafa4a72a1\PCB.CMPcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Short-Circuit Constraint (Allowed=Yes) (InNet('NetJ8_2')),(InNet('VCC'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('NetJ7_2')),(InNet('VCC'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('NetJ6_2')),(InNet('GND'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('NetJ5_2')),(InNet('VCC'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('O\E\L\')),(InNet('VCC'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('MADDR3')),(InNet('VCC'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('MADDR2')),(InNet('GND'))	0
Short-Circuit Constraint (Allowed=Yes) (InNet('MADDR1')),(InNet('VCC'))	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Clearance Constraint (Gap=3.5mil) (All),(All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Width Constraint (Min=3.5mil) (Max=20mil) (Preferred=10mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Hole Size Constraint (Min=7.874mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=4mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Unpoured Polygon (Allow unpoured: False)	0
Total	0