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Analysis and Design of a Battery Management System for Hybrid Energy Storage Systems in Autonomous Mobile Robots

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Kurzfassung

Die vorliegende Masterarbeit befasst sich mit aktuellen und zukunftsweisenden passiven und aktiven Technologien zum Ausbalancieren von Spannungsdifferenzen in einem System aus mehreren, in Serie geschalteten Batteriezellen.

Es wird eine Einführung in Balancingsysteme gegeben, die Notwendigkeit dieser Technologien erläutert sowie eine umfassende Literaturrecherche bezüglich Zellchemie und Spannungsausgleichstechniken gemäß industrieller Standards durchgeführt. Dabei werden mehrere Topologien hinsichtlich ihrer Effizienz untersucht und daraus ein Ausgleichssystem basierend auf einem einzeln geschalteten Kondensator abgeleitet. Letzteres wird in *PLECS* und *SIMULINK* simuliert und die Effizienz sowie die Geschwindigkeit des Balancingvorgangs analysiert.

Auf Basis der Simulationsergebnisse wird ein Balancingsystem für eine 48 V Lithium-Ionen-Batterie entwickelt. Das System ist darauf ausgelegt, Spannungsdifferenzen in zufällig verteilten, benachbarten oder nicht benachbarten Zellen auszugleichen. Hierfür soll der Balancingstrom über bidirektionale Halbleiterschalter fließen und die Energie in einem austauschbaren passiven Bauelement zwischengespeichert werden. Das System dient somit zusätzlich als Testplattform für zukünftige Experimente mit unterschiedlichen Speicherelementen. Laborergebnisse, welche die Funktionsweise des Konzepts bestätigen, werden präsentiert, und ein Ausblick auf zukünftige Entwicklungen gegeben.

Abstract

The following thesis analyses state-of-the-art and future passive and active balancing technologies for correcting voltage differences in a system of several series-connected battery cells.

An introduction to balancing systems and the necessity of cell voltage balancing is given, followed by extensive research on battery cell chemistry and industry-leading voltage equalisation methods. Several balancing hardware topologies are compared in terms of balancing efficiency, and a single switched capacitor balancing system is simulated using *PLECS* and *SIMULINK* with a close look at the balancing speed and efficiency.

Based on the simulation results, a balancing system is developed for usage in a 48 V Lithium-Ion battery. The system is designed to balance arbitrary cells using bidirectional semiconductor switching units and an interchangeable balancing energy storing element, allowing the system to be applied as a testing platform for different storage components. Hardware measurements stating a proof of concept are given in the results section, and an outlook on further developments is provided.

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Abbreviations

AC Alternating Current. 14	EEROM Electrically Erasable Programmable Read-Only Memory. 21
AC2C Adjacent Cell-to-Cell. 32	ESS Electric Energy Storage System. vii, 1, 2
ADC Analog-Digital Converter. 22, 64, 73, 80	EIS Electrochemical Impedance Spectroscopy. 14
AIR Accumulator Isolation Relay. 21	EKF Extended Kalman Filter. 13
ASIC Application Specific Integrated Circuit. x, 4, 5, 20–22, 31, 42, 91, 95	EM Emitter. xii, 62
BDPS Bidirectional Protection Switch. 66, 67	EMF Electromotive Force. 13, 16, 17
BJT Bipolar Junction Transistor. 71	EOL End-of-Life. 25
BMS Battery Management System. x–xiii, 1, 2, 5, 19–21, 25, 26, 60, 61, 64, 83, 84, 97	ESL Equivalent Series Inductance. 35
BP Back Propagation. 13	ESR Equivalent Series Resistance. 35, 40
C2CV Cell-to-Cell Variation. 2	ESS Energy Storage System. vii, xi, 1, 2, 5, 7, 11, 19, 21, 26, 32, 43, 53, 95
C2P Cell to Pack. 32	EV Electric Vehicle. 2, 3, 11, 12, 29, 47
CAN Controller Area Network. 59, 62, 64, 69, 74, 94	FET Field Effect Transistor. 66, 95
CHG Charge. 67	GPIO General Purpose Input-Output. 20, 71
CMC Carboxy-Methyl Cellulose. 23	HAL Hardware Abstraction Layer. 79, 80
CMOS Complementary Metal-Oxide Semiconductor. 64	HCP High Current Path. ix, xii, 60, 63, 69, 71, 75, 76, 78, 83, 94
CV Cell Voltage. ix, xii, 26, 47, 59, 62, 76, 77, 80, 81, 86, 94	HESS Hybrid Energy Storage System. xi, 4, 5, 7
CVMIC Cell Voltage Measurement Integrated Circuit. 60, 71, 76, 80, 84, 85, 95	HESS4MRA Hybrid Energy Storage Systems for Mobile Robot Applications. i, vii, 2, 4, 5
DC/DC Direct Current to Direct Current. viii, xii, 32, 40, 61, 62, 64, 68, 76, 84, 94	HV High Voltage. 60–63, 71, 75, 84, 85
DC2C Direct Cell-to-Cell. 32	HVS High Voltage System. 20, 21, 59, 60, 71, 84
DCHG Discharge. 67	I²C Inter-Integrated Circuit. ix, 20, 60, 64, 71, 74, 79, 80, 85
DOD Depth of Discharge. 24	IC Integrated Circuit. ix, xii, 2, 20, 25, 42, 61, 63, 70, 71, 76, 77
	IEC International Electrotechnical Commission. 19

iso-I²C	Isolated Inter-Integrated Circuit.	NTC	Negative Temperature Coefficient.
	21		22
iso-SPI	Isolated Serial Peripheral Interface.	OCV	Open Circuit Voltage.
	21	xi, 13, 14, 16,	
isoSCL	Isolated Serial Clock.	25, 27, 49, 51, 80	
isoSDA	Isolated Serial Data.		
LCO	Lithium Cobalt Oxide.	P2C	Pack to Cell.
vii, 10, 11		P2D	Pseudo-two-Dimensional.
LDO	Low-Dropout.	PCB	xi, 10
25, 63, 64, 68, 71,		Printed Circuit Board.	ix, xii, xiii,
84, 85, 94		xv, 4, 5, 35, 39, 42, 59–62, 69–71,	
LED	Light Emitting Diode.	75–78, 83, 84, 93, 94, 96	
71, 74, 80, 81, 94			
LFP	Lithium Iron Phosphate.	PMOS	P-channel Metal Oxide Semiconductor.
vii, 9, 10		62, 63, 70, 71	
Li-Ion	Lithium-Ion.	PSU	Power Supply Unit.
v, xi, 2, 3, 8–12, 17,		69, 84, 94	
21, 23, 24, 59, 84, 91		PTC	Positive Temperature Coefficient.
LIB	Lithium-Ion Battery.	xi, xiii,	xi, 22, 68
2, 7, 10, 25		34, 35, 39, 40, 42, 51, 53, 61–64, 69,	
LiFePO₄	Lithium Iron Phosphate.	70, 73, 74, 79, 80, 87–89, 95	
xi, 27			
LMO	Lithium Manganese Oxide.	RAM	Random Access Memory.
vii, 9, 11		64	
LMP	Lithium Metal Hybride.	RBF	Radial Basis Function.
xi, 8		13	
LNO	Lithium Nickel Oxide.	RE	Receiver.
vii, 11		xii, 62	
LQFP	Low-Profile Quad Flat Package.	RTC	Real Time Clock.
73, 74		71, 73	
LTO	Lithium Titanium Oxide.	SCL	Serial Clock.
vii, xv, 12, 19		71, 74, 94	
LV	Low Voltage.	SDA	Serial Data.
10, 22, 60–62, 73–76,		71, 74, 94	
78, 84, 88		SDR	Self Discharge Rate.
LVS	Low Voltage System.	19	
21, 59, 60, 68, 71, 84		SEI	Solid Electrolyte Interphase.
		19, 24	
MC2MC	Multi-cell to Multi-cell.	SESS	Single Energy Storage System.
32		4	
MCU	Microcontroller Unit.	SMD	Surface Mounted Device.
20, 21		64, 83	
MOSFET	Metal Oxide Semiconductor	SOC	State of Charge.
Field Effect Transistor.	ix, xi, xv, 31,	vii, viii, 2, 12–14,	vii, viii, 2, 12–14,
35, 36, 47, 48, 56–58, 62–67, 76, 77,	35, 36, 47, 48, 56–58, 62–67, 76, 77,	19, 25–28, 47–52, 56, 64, 79, 95	19, 25–28, 47–52, 56, 64, 79, 95
88, 94, 95	88, 94, 95	SOH	State of Health.
MUX	Multiplexer.	vii, xi, 2, 3, 14, 15,	vii, xi, 2, 3, 14, 15,
ix, xiii, 61, 62, 69–71,		19, 27, 49	19, 27, 49
73–76, 81, 82, 84, 87, 88, 94		SOT	Small Outline Transistor.
		64, 65	
Na-MeCl₂	Sodium Metal Chloride.	SPI	Serial Peripheral Interface.
xi, 8		20, 64	
Na-S	Sodium Sulfur.	SWCLK	Serial Wire Clock.
xi, 8		74	
NCA	Lithium Nickel Cobalt Aluminium	SWDIO	Serial Wire Debug Data In-
Oxides.	Oxides.	put/Output.	put/Output.
vii, 12	12	74	
Ni-Cd	Nickel–Cadmium.	SWO	Serial Wire trace Output.
1, 7–9		74	
Ni-MH	Nickel–Metal Hybrid.	THT	Trough Hole Technology.
1, 7–9		83	
NMC	Lithium Nickel Manganese Cobalt	TQFP	Thin Quad Flat Pack.
Oxide.	Oxide.	64	
vii, xi, 9, 11	9, 11		
NMOS	N-channel Metal Oxide Semicon-	UART	Universal Asynchronous Receiver-
ductor.	ductor.	Transmitter.	Transmitter.
xi, 31, 62, 63, 70, 71	31, 62, 63, 70, 71	20	
		USB	Universal Serial Bus.
		84	
		UVLO	Under Voltage Lockout.
		88	

1 Introduction

The following chapter intends to give a short introduction to Energy Storage Systems (ESS) and to point out the importance of Battery Management Systems (BMS). Furthermore, the project enabling this thesis and its research is presented, and a short overview of the thesis is provided.

1.1 Definition of Terms

1.1.1 Passive and Active Balancing

In the past, the terms „Active Balancing“ and „Passive Balancing“ have not been used consistently. In [1], „Passive Balancing“ was introduced to describe internal processes that ensure no undesired events could occur during the operation if a battery cell is overcharged. The excess energy in such cells is converted into heat or is outgassed. However, this only applies to lead-acid, Ni-Cd or Ni-MH cells resistant to overcharge. The term „Active balancing“ was used to represent external balancing circuits with a transistor as an active element, e.g. to connect a resistor to a cell.

With the rising popularity of energy-transferring balancing circuits and the self-balancing technologies vanishing from the market, the meaning of both terms has changed. In [2], the circuits formerly known as „Active balancing“ were introduced as „Passive balancing“ and the presence of active components no longer defines the difference between both technologies but whether the process of balancing is dissipative (as referred to passive), or recuperative (active). This nomenclature has been popular among various publications in recent years [3].

This thesis will use the term „Passive Balancing“ for dissipative technologies and „Active Balancing“ for energy shuttling or recuperative balancing topologies.

1.1.2 Energy Storage System and Electric Energy Storage System

In the present work, the only Energy Storage Systems (ESS) considered are systems designed for electrical energy storage. Therefore, the terms Energy Storage System and Electric Energy Storage System (EESS) will be used interchangeably.

1.1.3 Battery Pack and Battery Stack

This thesis uses the terms battery pack and battery stack, which describe a variable number of series-connected cells with further possible series-connected cells in parallel.

1.1.4 Galvanic Isolation

During the following work, two systems are considered galvanically isolated if the ohmic resistance between two measuring points following a 4-point measurement at a constant current of 50 mA is at least $500 \Omega V^{-1}$.

1.2 Motivation

Electric Energy Storage Systems (EESS) nowadays play a key role in various sectors of modern living, making great strides towards the electrification of transportation infrastructure. Besides their application in Electric Vehicle (EV), the demand for energy storage in modern logistics, increasingly relying on autonomous robots, is rising [4]. The present thesis is a pivotal part of the Hybrid Energy Storage Systems for Mobile Robot Applications (HESS4MRA) project, with the name-giving research focus on energy storage systems for mobile robots in logistics.

Battery Management Systems (BMS) perform several tasks in terms of monitoring Energy Storage System (ESS) parameters like system voltages and temperatures, ensuring communication with other modules in the system as well as balancing individual cell voltages affected by external and internal sources of imbalance [5], [6]. Internal sources of imbalance include manufacturing variance in charge storage volume, variations in internal impedance, and differences in self-discharge rate. External factors of imbalance are mainly caused by some multi-rank protection Integrated Circuits (IC), which drain charge unequally from different series ranks in the pack. Furthermore, the thermal difference across the pack results, ageing, and misuse result in different capacities, internal resistance and self-discharging rates of the cells [7]. Owing to the merits of high reliability, high energy density, and high cycle, Lithium-Ion Batterys (LIB) are widely used in the automotive sector and smart grid systems. A single LIB cell usually has low voltage and capacity. Thus, any modern LIB pack comprises hundreds or thousands of individual cells in series and parallel configurations to meet the load demand. The effective capacity of LIB is reduced by the inconsistency of individual Li-Ion cells in terms of capacity, voltage and internal resistances [5]. Without balancing systems, Cell-to-Cell Variation (C2CV) would cause individual voltages to drift apart over time, leading to a decrease in the total usable capacity of the battery pack and an imbalance in the State of Charge (SOC) during operation [3].

In an ideal cell with a State of Health (SOH) value of 100 %, the actual capacity C_{act} of the cell is equal to the nominal capacity C_{nom} . The imbalances mentioned above lead to differences in the actual capacities of the cells, which may result in initial differences in the SOC of the cells. These differences are amplified during the following charge and discharge cycles, but can already be noted after the first discharge of the battery pack. The cell with the lower SOH and the resulting lower initial SOC will eventually limit the discharge of the whole series by reaching its lower cut-off voltage first. The stack can then no longer be discharged without damaging the cell with the lowest SOH by draining the voltage below the lower voltage limit given by the manufacturer. After several more charge and discharge cycles, the differences in SOC between the cells are widening. Similar to the event mentioned above, the higher charged cell will limit the charging process of the series by reaching the upper cut-off voltage first. Further charging of the pack would cause an overcharge to the mentioned cell and could induce a thermal run-

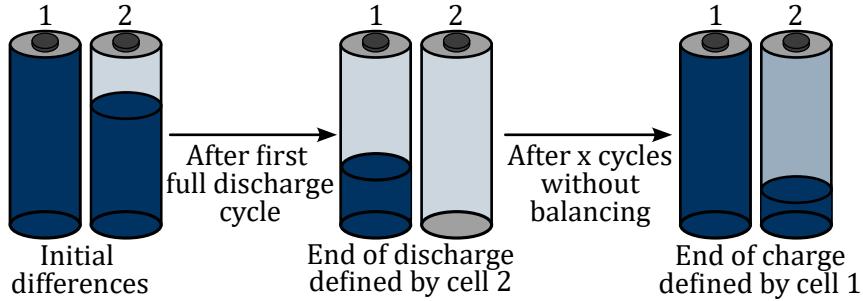


Figure 1.1: Induced imbalance due to initial differences in SOH: cell 1 with capacity $C_{act,1} = C_{nom}$ and cell 2 with capacity $C_{act,2} = C_{nom} \cdot 0.8$ [3].

away, ending in a hard-to-control battery fire. As depicted in Figure 1.1, there is energy left in a battery series that can, however, not be used by the load without discharging the limiting cell below the lower voltage limit. In addition, the battery's full capacity can not be used during charging since all cells need to be stopped from being charged once the first cell has reached its higher cut-off voltage [3].

Various passive and active balancing concepts have been proposed over the last 20 years and can be classified into passive and active topologies according to the description in chapter 2. Passive topologies dissipate the excess of charge from higher charged cells as thermal energy using shunt resistors. Active balancing, as defined by recent literature and defined by the definition of terms in section 1.1, allows the transfer of charge from higher charged cells to lower energy cells, providing substantial benefits over passive balancing, including higher efficiency by achieving balancing efficiencies of over 90 % and reducing balancing time by up to 36.9 % [8]. Further, the service life of a battery can be extended by reducing the ageing rate of the cells and enabling up to 3.1 % higher discharge capacity and an up to 7.7 % longer service life compared to passive balancing [9]. Hybrid balancing systems, consisting of passive and active balancing topologies, have demonstrated balancing speeds 41.50 % faster and bleeding lesser energy by 97.98 % compared to passive cell balancing systems [10]. Since passive balancing circuits dissipate excess energy in heat, better energy utilisation is achieved by active balancing systems with less energy loss and less battery pack heating. This makes active balancing more suitable for high-power applications like EVs where maintaining battery performance and safety is critical. Despite its complexity and higher cost, the benefits of active balancing in terms of efficiency and battery longevity make it a preferable choice for modern battery management systems [11].

1.3 Objectives and Requirements

The present work aims to perform a literature review on state-of-the-art active and passive balancing topologies, comparing different topologies focusing on efficiency and implementation complexity. Several simulations concerning switched resistor balancing systems and switched capacitor topologies are performed and analysed in terms of balancing speed and efficiency using *PLECS*, *MATLAB* and *SIMULINK*. Subsequently, a single switched capacitor active balancing system for a 16s Li-Ion-stack, allowing arbitrary cell balancing using bidirectional semiconductor switches, is designed using *ALTIUM DESIGNER*.

SIGNER. The Printed Circuit Board (PCB) is designed in a way that the storing element for the balancing energy can be changed to allow further research on storing elements for active balancing circuits. A prototype is constructed and tested under laboratory conditions, allowing an outlook on the feasibility of bidirectional switching units for the use-case in cell balancing systems as Application Specific Integrated Circuits.

The prototype is designed for operating in a Hybrid Energy Storage System (HESS) for mobile robot applications as described in section 1.4.

1.4 The HESS4MRA Project

The goal of the Hybrid Energy Storage Systems for Mobile Robot Applications (HESS4MRA) project [12], funding the present work, is to develop Hybrid Energy Storage Systems for mobile, often autonomously operating robot units. Such mobile robot platforms are the emerging backbone of modern logistics and find rising application in modern warehousing and distribution facilities, acting in pick-and-place functions and short-haul transportation. Currently, these units are powered by battery systems, internal combustion engines, fuel cells, or solar power systems. However, since the market is expected to grow to an anticipated number of 50 billion robots by 2025, the power supply will become a significant issue [13]. Therefore, highly efficient systems are required to convert the storable energy to ensure efficient power transfer from the energy storage systems to the electric drivetrain. This task can either be carried out by Single Energy Storage Systems (SESS) or by HESSs [14].

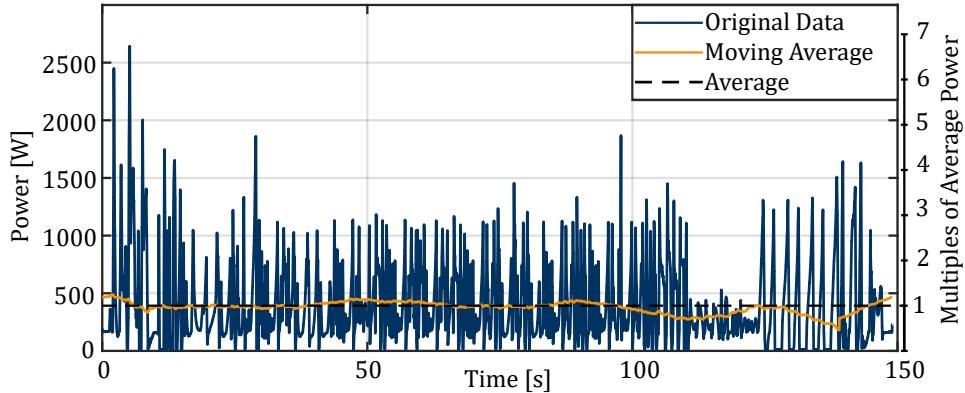


Figure 1.2: Power waveform of a robot arm: Derived from real-world power consumption pattern of a robotic arm during its operational tasks [15].

Figure 1.2 shows the power waveform of a mobile robot pick-and-place robot during operation. It is clearly visible that the average power required for, e.g., driving with a constant velocity, is a fraction of the peak power required for, e.g., picking up an object by operating a robot arm. This implies that the power supply system needs to provide enough storage capability for the required average power and deliver peak powers up to 7 times higher than the average power. This task can not be fulfilled efficiently by a Single Energy Storage System but requires power modules with high energy density to provide the average power in parallel to power modules with high power densities for peak power delivery. To satisfy this requirement, Hybrid Energy Storage Systems use

battery cells with a high energy density as a main energy storage system but further include super-capacitors, which are charged during operation from the battery cells. The super-capacitors offer a higher power density than conventional battery cells and can supply power peaks by discharging in a short time without experiencing damage. However, the implementation of such hybrid systems requires the development of highly efficient 4-port energy converters [14]–[16].

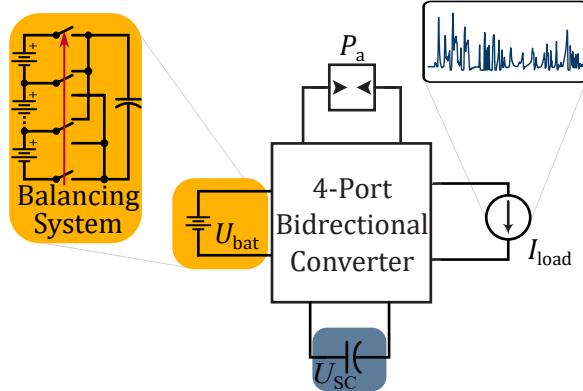


Figure 1.3: Hybrid Energy Storage System [15].

The funding HESS4MRA-project aims to combine battery storage systems with supercapacitor modules by a 4-port bidirectional converter as shown in Figure 1.3. The present work deals with the development of the Battery Management System (BMS) for the battery module of this system. Further work outside of the present thesis deals with the balancing system for the super-capacitor modules as well as with the 4-port bidirectional converter.

1.5 Structure of the Thesis

An introduction to the fundamentals of Energy Storage Systems is given in chapter 2. State-of-the-art passive and active balancing topologies are reviewed in chapter 3 and analysed by simulation regarding balancing speed and efficiency in chapter 4. Design criteria, technical component requirements, and suitable parts for the prototype development are selected and discussed in chapter 5. The documentation of the designed Printed Circuit Board is written down in chapter 6 whilst chapter 7 includes the measurement setups as well as the experimental results of the designed BMS under laboratory conditions. chapter 8 discusses the obtained results and demonstrates the proof of concept of the proposed hardware circuit and control algorithm. Hardware bugs and potential software improvements of the prototype revision are pointed out in chapter 9 while further discussing the feasibility of the proposed circuit for large-scale use and possible ASIC integration.

2 Fundamentals

2.1 Energy Storage Systems

Energy Storage Systems can be classified according to the energy storing element or technology. Different technologies are presented in Figure 2.1 with respect to their respective energy density and power density.

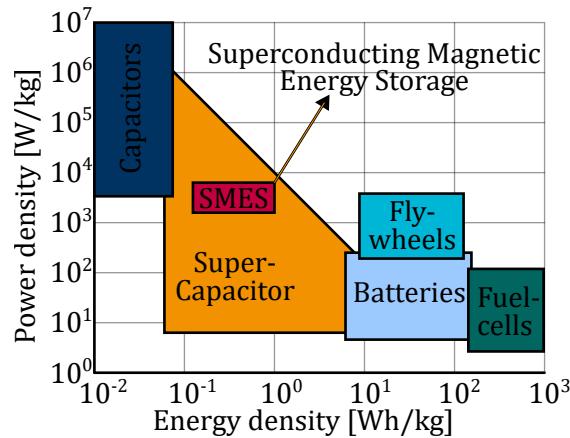


Figure 2.1: Overview on State of the Art Energy Storage System [14], [17].

Figure 2.1 demonstrates that the design of the ESS greatly depends on the power and energy demands of the application, which can also result in specific combinations of ESS to meet the requirements. However, mobile systems mostly rely on batteries in terms of hybrid Energy Storage Systems, where battery cells act as high-energy storage and super-capacitors act as high-power storage. This work aims to focus on battery systems and will therefore exhibit different cell chemistries used in various industrial and consumer applications.

2.2 Cell Chemistry

While there are many varieties of power batteries, lead-acid, Nickel–Metal Hybrid (Ni-MH), Nickel–Cadmium (Ni-Cd), as well as Lithium-Ion Battery (LIB) are applied as electrochemical Energy Storage Systems in electric vehicles as well as mobile robot applications. Lead-acid batteries were found to be used in early-stage developments of electric automobility. Ni-MH batteries experienced breakthroughs and were industri-

alised in the 1980s. The good characteristics of Lithium-Ion cells further promoted the development of electric vehicles. Main features of cell technologies are compared in Figure 2.2.

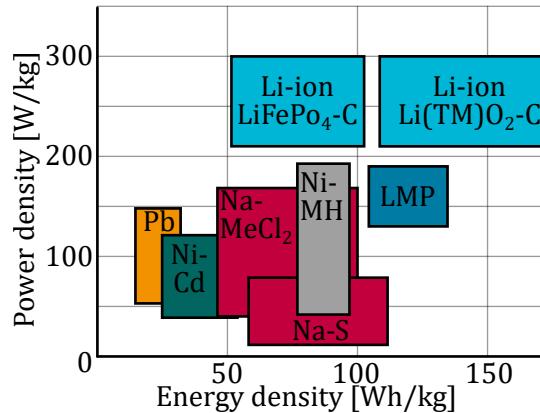
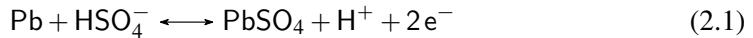


Figure 2.2: Power and energy density of cell chemistries, including Lithium Metal Hydride (LMP), Sodium Sulfur (Na-S) and Sodium Metal Chloride (Na-MeCl₂) [18].

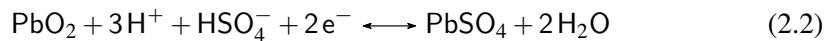
In general, lead-acid, Ni-Cd, and Ni-MH batteries are safer to operate and less expensive than Li-Ion cells. However, they are not competitive for the application in the automotive sector any more due to their lower energy density [19].

2.2.1 Lead-Acid Battery

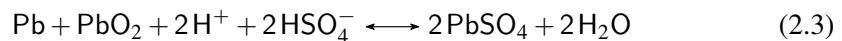
Lead-acid batteries are among the oldest electrochemical energy storage technologies, using PbO_2 and Pb as cathode and anode material. The electrolyte is provided by the H_2SO_4 solution. During discharge, electrons are released from the anode and $PbSO_4$ is formed. Electrons then travel in the direction of the cathode to reduce the local Pb^{4+} to Pb^{2+} , forming $PbSO_4$. The concentration of H_2SO_4 is decreased, and the voltage potential drops. During charging process, $PbSO_4$ from the cathode generated during while discharging, reacts with H_2O and forms PbO_2 . Pb^{2+} is reduced to Pb in the anode, and the H_2SO_4 increases, resulting in a higher voltage between cathode and anode. The reaction in the anode is described in Equation 2.1[19].



The reaction in the cathode follows Equation 2.2 [19].



The overall reaction results in [19]:



2.2.2 Nickel-Cadmium Battery

Nickel–Cadmium (Ni-Cd) batteries are widely used in consumer electronics and offer high capacity, low costs and simple fabrication in different formats. Ni-Cd-batteries can

be categorized as alkaline batteries since a *KOH* solution is used as electrolyte. The cathode is made of *NiOOH* and the anode material is *Cd*. According to Equation 2.4, *Cd* is oxidized into *Cd(OH)₂* during discharge and *NiOOH* is reduced to *Ni(OH)₂*, releasing *H₂O* from the electrolyte. Ni-Cd batteries suffer from memory effects, reducing the capacity when the cells are not always fully discharged [19].

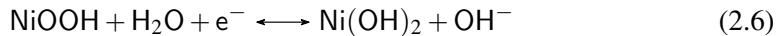


2.2.3 Nickel–Metal Hydride Battery

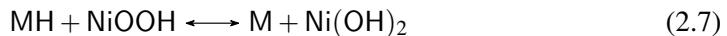
The design of Nickel–Metal Hybrid (Ni-MH) batteries is based on Ni-Cd batteries but with major improvements on the memory effect and pollution aspects. Ni-MH batteries also belong to the group of alkaline batteries due to their use of *KOH* as electrolyte. The cathode material is *Ni(OH)₂/NiOOH* and the anode material is made from an *M/MH_x* hybrid. Various types exist for *M/MH_x*, such as *TiMn₂* (AB₂), *LaNi₅* (AB₅), *TiFe* (AB) and *Mg₂Ni* (A₂B). The reaction on the anode follows Equation 2.5 [19].



The equation in the cathode can be described as [19]:



Thus, the overall reaction results in [19]:



H₂O and *OH⁻* are only involved in charge transfer and do not act as reacting compounds in the chemical reaction, resulting in a constant *KOH* concentration [19].

2.2.4 Lithium Ion Battery

Compared with lead-acid, Ni-Cd and Ni-MH cells, Lithium-Ion batteries provide higher energy densities and higher cycling lifetimes. Furthermore, Li-Ion cells support higher C-rates, meaning they can be discharged at much higher currents. While several Li-Ion-based cell technologies exist, the general structure remains the same. According to Figure 2.3, Lithium-Ion batteries comprise electrodes, a separator and an electrolyte. Common cathode materials include Lithium Iron Phosphate (LFP), Lithium Nickel Manganese Cobalt Oxide (NMC) and Lithium Manganese Oxide (LMO).

Although lithium is the focus of attention and as a label in the Li-Ion batteries, surprisingly, it's a less affecting factor in determining Li-Ion batteries cost. Usually, lithium is found in the electrolyte and cathode, where the cathode only has a very small portion [20] of lithium. Among the components of the Li-Ion battery, the major contributing factors are the processing costs and the cathode material. Reducing the cost and enhancing the performance can amazingly extend their flexibility when applied in most modern technologies, which depend on energy storage. Research and discussions of Li-Ion batteries mainly put the focus on the electrode materials. Higher charge-discharge capacity, long life cycle and high voltage electrode material from abundant and cheap resources can greatly increase the energy and the power output of Li-Ion batteries and lower their cost.

During charging of the cell, Lithium ions (Li^+) are released from the atomic grid of the cathode material and migrate through the electrolyte to the anode material, where they join the atomic grid of the anode material. Electrons reach a negative potential by travelling through an external circuit and passing on the electric energy to the load. Li^+ is transferred between the cathode and the anode during charge and discharge. The process is depicted in 2.3, where the electrodes are considered as a porous matrix.

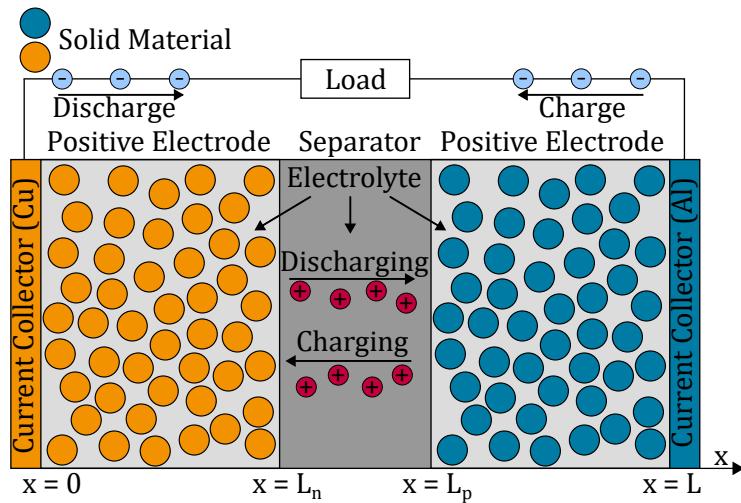


Figure 2.3: Structure of a Li-Ion cell using the Pseudo-two-Dimensional model (P2D) [18], [19], [21].

2.2.4.1 Lithium Iron Phosphate

Lithium Iron Phosphate (LFP), also known as LiFePO_4 , became popular by the end of the 1990s, offering good chemical and thermal stability and cheap and easy production. This allowed the use in Low Voltage applications without the need for supervision units. LFP batteries are characterised by a flat voltage plateau and a two-phase structure. The reversible extraction of lithium from the LiFePO_4 and insertion of lithium into FePO_4 undergoes a two-phase reaction between Li-rich and Li-poor phases and follows Equation 2.8 and Equation 2.9 [22]–[24]. During discharge, Li-Ions are extracted from the cathode



During the charging process, Li-Ions are inserted back into the FePO_4 grid.



2.2.4.2 Lithium Cobalt Oxide

Lithium Cobalt Oxide (LCO) was introduced by Sony in 1991 for the mass production of LIBs and is still widely used due to its easy manufacturing and mass-production capabilities. LCO is characterised by a high operating potential but comes with a stability problem of the structure. When the amount of lithium to be desorbed increases due to

charging and discharging, a problem arises due to a phase change. In this state, the structure becomes unstable, the Co ions are eluted, and the electrolyte's oxidation/reduction reaction may occur. Therefore, the amount of lithium to be desorbed must be limited to realise its use in a battery. As a result, the actual capacity is lowered to approximately 120 mAh g^{-1} to 130 mAh g^{-1} in comparison with the theoretical capacity of 272 mAh g^{-1} [25], [26].

2.2.4.3 Lithium Nickel Oxide

Lithium Nickel Oxide (LNO) is a material with an increased reversible capacity compared to LCO since a higher amount of lithium can be desorbed. Even if LNO itself is not a promising material for commercial Li-Ion cells, mixed $\text{LiNi}_{1-y}\text{Co}_y\text{O}_2$ phases can overcome the main drawbacks by both LCO and LNO oxides, e.g. that $\text{LiNi}_{0.85}\text{Co}_{0.15}\text{O}_2$ and $\text{LiNi}_{0.80}\text{Co}_{0.15}\text{Al}_{0.05}\text{O}_2$ have demonstrated good electrochemical properties with a reversible capacity of around 180 mAh g^{-1} with excellent cycling capacities [25], [27].

2.2.4.4 Lithium Manganese Oxide

Lithium Manganese Oxide (LMO) is a spinel structure composed of LiMn_2O_4 with a higher operating voltage and lower material costs than Cobalt, whilst offering a capacity of 120 mAh g^{-1} to 130 mAh g^{-1} . Thus, it is suitable as a commercial material for large lithium-ion batteries for EV applications. Current research activities focus on improving electrochemical and safety aspects of LMO batteries [25].

2.2.4.5 Lithium Nickel Manganese Cobalt Oxide

Lithium Nickel Manganese Cobalt Oxide (NMC) combines the advantages like the high capacity of LNO, the thermal stability and the low costs of LMO as well as the stable electrochemical properties of LCO. The cathode material consists of $\text{LiNi}_x\text{Mn}_y\text{Co}_z\text{O}_2$, with $x + y + z = 1$ [25]. The influence of Nickel, Cobalt and Manganese on the cell chemistry is shown in Figure 2.4. Since irreversible phase transition is low even if the amount of lithium to be desorbed is large, high capacities can be realised with excellent lifetime expectation, raising the usage of NMC as primary material in mainstream applications such as Energy Storage Systems or EVs.

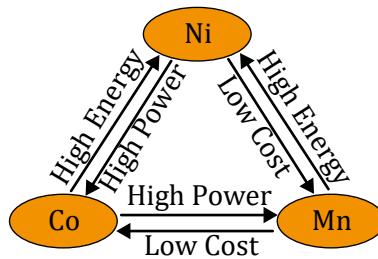


Figure 2.4: Transition metal characteristics of NMC [25].

Unfortunately, cation-mixing (in which Ni and Li change their positions and form crystal structures) frequently occurs when the concentration of Ni increases. This re-

sults in reduced battery performance and lifetime. Recent research activities focus on improving stability while increasing Ni content [25].

2.2.4.6 Lithium Titanium Oxide

Lithium Titanium Oxide (LTO) is a spinel material consisting of $\text{Li}_4\text{Ti}_5\text{O}_{12}$ with promising characteristics to be a good anode material for Li-Ion batteries due to its good cycle stability, rate capability and safety properties at high and low temperatures. Another advantage is the flat potential result for the two-phase LTO reaction. However, low capacity and gassing issues hindered the wide application of LTO cells. Research activities indicated that LTO performances may be enhanced by heterogeneous phase control, surface engineering or overlithiation. Table 2.1 provides an overview of the properties and demonstrates the cycle advantage of LTO to other anode materials [28].

Table 2.1: Comparison of LTO cells to other technologies [28].

Anode materials	Density (g cm^{-3})	Theoretical specific capacity	Cycle life (cycles)	Full cell energy density (Wh kg^{-1})	Full cell power density (kW kg^{-1})
$\text{Li}_4\text{Ti}_5\text{O}_{12}$	3.5	175	> 10000	~ 100	10
Graphite	2.25	372	> 1000	~ 200	5
Silicon	2.33	4200	> 200	~ 250	0.5
Lithium	0.53	3862	> 100	~ 300	0.1

2.2.4.7 Lithium Nickel Cobalt Aluminium Oxides

With a theoretical capacity of 279 mA h g^{-1} using $\text{LiNi}_{0.80}\text{Co}_{0.15}\text{Al}_{0.05}\text{O}_2$, Lithium Nickel Cobalt Aluminium Oxides (NCA) offers a combination of high energy and high power density, what makes them suitable for EV batteries, hence they are widely used in the automotive sector. However, NCA may be replaced in the future due to the critical supply chain for Cobalt as 65 % of it comes from the Democratic Republic of Congo, a country with an unstable security situation, resulting in unpredictable price trends [29], [30].

2.3 Performance Parameters of Power Batteries

2.3.1 State of Charge

The State of Charge (SOC) of a battery cell is defined as the ratio of the current capacity $Q(t)$ to the nominal capacity Q_n , as in Equation 2.10. It is given in percent, where a SOC of 100 % is considered as a fully charged battery with respect to the nominal capacity given by the manufacturer.

$$SOC(t) = \frac{Q(t)}{Q_n} \quad (2.10)$$

The SOC can not be measured directly but is subject to various estimation methods, requiring substantial knowledge of the cell electrochemistry over a long period of time.

The Open Circuit Voltage, temperature and the instantaneous charge or discharge current are used as input values for the estimation of the SOC. The classification of SOC estimation methods varies across literature [31], [32] but can often be found as divided into four categories.

Direct measurement: This method uses the physical properties of a battery, such as the voltage and the impedance.

Book-keeping estimation: This method uses the charging and discharging current as an input variable and defines the SOC by integrating with respect to time as per Equation 2.11.

Adaptive systems: Adaptive systems are self-adjusting systems that modify the SOC according to the charge or discharge conditions. Various adaptive systems have been developed in recent years.

Hybrid methods: Hybrid methods benefit from the advantages of each SOC-method mentioned above and have allowed the optimization of the SOC-estimation performance in recent years. Literature stated that hybrid methods generally produce more accurate estimations than individual methods.

The estimation methods mentioned above include the mathematical methods according to Table 2.2[33].

Table 2.2: Classification of SOC estimating mathematical methods [33].

Categories	Mathematical Methods
Direct measurement	Open circuit voltage method Terminal voltage method Impedance method Impedance spectroscopy method
Book-keeping estimation	Coulomb counting Modified Coulomb counting method
Adaptive systems	BP neural network RBF neural network Support vector machine Fuzzy neural network Kalman filter
Hybrid methods	Coulomb counting and EMF combination Coulomb counting and Kalman filter combination Per-unit system and EKF combination

Among the mathematical methods mentioned in Table 2.2, the Coulomb counting is the most popular estimation approach for the State of Charge, which is based on the integration of the current over time according to Equation 2.11 to determine the remaining charge in the battery. This method, however, does not consider noise and other disturbances. Furthermore, the accuracy of the Coulomb counting method depends on the initial SOC value estimation and the measurement of the battery current [34].

$$SOC(t) = SOC(t_0) \pm \frac{1}{C_{\text{actual}}} \int_{t_0}^t \eta_i I(t) dt \quad (2.11)$$

$$\eta_i = \frac{Q_{\text{discharge}}}{Q_{\text{charge}}} \cdot 100\% \quad (2.12)$$

$\text{SOC}(t)$ represents the State of Charge at a given time t with respect to the initial SOC at the time t_0 . Equation 2.11 shows that the SOC estimation significantly relies on the accurate estimation of the initial SOC from previous states of the battery. C_{actual} is the actual or nominal capacity of the battery and $I(t)$ is the charge or discharge current at a given time t . The factor η_i calculated by Equation 2.12 stands for the coulombic efficiency, which typically is within a range of 0.9 to 1 depending on the temperature and charging rate. It describes the ratio between the charges removed during discharge of the cell and the charges delivered to the cell during the charging process. It may also be defined as the ratio between a cell's discharging and charging capacity [35].

2.3.2 State of Health

The SOH gives feedback on the remaining energy inside the battery cell, referring to the battery lifetime and providing information on the total battery capacity. In vehicular applications, the battery capacity can fade by up to 20 % while the internal resistance of the battery cell can increase by up to 160 % [36]. Both the State of Charge and the State of Health can not be measured directly. Still, they refer to various estimation techniques like pulse measurements and adaptive battery models like Kalman filters or neural networks, which require substantial knowledge of cell electrochemistry over a long period of time. The SOH can either be defined using the capacity as per Equation 2.13 or by using the battery internal resistance according to Equation 2.14 [19].

$$SOH = \frac{Q_{\text{aged}}}{Q_{\text{new}}} \quad (2.13)$$

With Q_{aged} being the current capacity and Q_{new} the nominal initial capacity.

$$SOH = \frac{R_{\text{EOL}} - R}{R_{\text{EOL}} - R_{\text{new}}} \quad (2.14)$$

A well-known experimental approach for battery fault diagnosis and prognosis is the estimation of the State of Health from the battery internal resistance. To measure the DC-resistance, current pulses are applied and the internal resistance R_i is calculated by Ohm's law according to Equation 2.15 where ΔV corresponds to the voltage drop and refers to the applied current pulse of 1 C.

$$R_i = \frac{\Delta I}{\Delta V} \quad (2.15)$$

The polarisation resistance can also be determined by comparing the discharge curves at different temperatures and different currents. It is affirmed in [37] that the internal resistance increases with the temperature and affects the battery lifetime. Further, the voltage measurement highly depends on the timing as the OCV depends on the time elapsed after the current pulse.

Another way of determining the SOH is to estimate the actual value of the battery impedance by Electrochemical Impedance Spectroscopy (EIS), where a small amplitude AC signal at different frequencies is used to probe the impedance characteristics of a cell. At high frequencies, inductive effects in the cells' wiring and porous structure dominate,

while the resistance becomes purely ohmic and capacitive effects arise at low frequencies [38].

Until now, the estimation of the SOH has not found its way into many commercial and industrial applications since the complexity and unknown variations are yet to be deduced[34].

2.3.3 Battery Capacity

The available charge that can be drained from a battery under certain discharge conditions is denoted as the battery capacity and is given in Ah. The battery capacity is categorised into theoretical, rated, and practical capacity. The theoretical capacity C_T is given by Equation 2.17 following Faraday's law according to Equation 2.16 with the variables stated in Table 2.3[19].

$$Q = n \cdot F \cdot \frac{m}{M} \quad (2.16)$$

Table 2.3: Symbols used in Equation 2.16 and Equation 2.17 [19].

Symbol	Description	Unit
Q	Charge in reaction	Ah
n	Number of gained or lost electrons	pcs.
F	Faraday constant	C mol ⁻¹
m	Mass of active material	g
M	Molar mass	g mol ⁻¹
m_0	Mass of electrodes in reaction	g

$$C_T = 26.8 \cdot n \cdot \frac{m_0}{M} \quad (2.17)$$

The rated capacity is defined as the minimum expected capacity when a new, but fully formed cell is measured under standard conditions, e.g. temperature, cut-off voltage and charge rate [19], [39]. The practical capacity C_P is the actual charge that can be drained from a battery cell before reaching its cut-off voltage and is influenced by many factors, including the discharge rate, the cut-off voltage, the temperature and the sample history [40]. Practical capacity is obtained by integrating the discharge current $i(t)$ over time, according to Equation 2.18, where t_0 is the initial time and t_{cut} is the time where the cut-off voltage is reached [19].

$$C_P = \int_{t_0}^{t_{\text{cut}}} i(t) dt \quad (2.18)$$

Since the active material does not fully react during battery drainage, the practical and the rated capacity are always lower than the theoretical capacity. At high discharge rates, polarisation is more substantial and the voltage decreases faster, resulting in a lower practical capacity. At low discharge rates, the polarisation is weak and the decrease in voltage is slower. Consequently, the practical capacity is high, even higher than the rated capacity [19].

2.3.4 Battery Voltage

The single cell voltage, denoted as U_{cell} , is defined as the electric potential difference between the cell's positive and negative terminals. It is composed of the Electromotive Force (EMF) of the electrochemical cell reaction and the voltage drop due to the application of charge or discharge current and the occurrence of self-discharge during battery lifetime. If no load is connected to the battery cell, meaning that no charge or discharge current is applied, the voltage across the terminals is denoted as the Open Circuit Voltage (OCV). In steady state, the OCV may become close to the theoretical EMF [41].

In case of a connected load, the voltage potential difference is denoted as U_{cc} and given by Equation 2.19, where R_{Ω} is the internal ohmic resistance of the battery cell and R_f is the contact resistance of the cell terminals [19].

$$\begin{aligned} U_{\text{cc}} &= \text{EMF} - I \cdot R_i \\ &= \text{EMF} - I \cdot (R_{\Omega} + R_f) \end{aligned} \quad (2.19)$$

U_{cc} is affected by discharge time, discharge current, ambient temperature, and cut-off voltage. The battery cell must not be discharged below its cut-off voltage to avoid damaging the cell. The rated voltage may differ depending on the cell chemistry [19].

2.3.5 Internal Resistance

The internal resistance is one of the most critical characteristic parameters in terms of performance and lifetime of a battery cell. According to Figure 2.5, it is divided into ohmic resistance and polarisation resistance. The ohmic resistance is the sum of the resistance of electrode materials, electrolytes, separator resistance, and contact resistance of many components. The polarisation resistance is defined as the induced resistance by the polarisation in the electrochemical reaction. This includes the resistance caused by electrochemical polarisation as well as concentration polarisation. The overall internal resistance is affected by the battery's chemical composition, the cell's structure and various other factors [42].

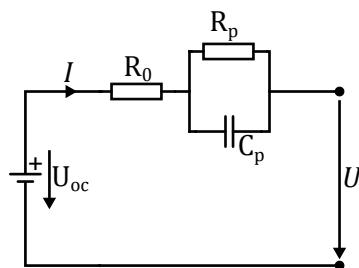


Figure 2.5: First order equivalent cell model [43].

The internal resistance of a battery cell can not be measured directly, but it can only be derived by measuring the voltage and current during discharge. A typical and simple method is the pulse discharge method as depicted in Figure 2.6.

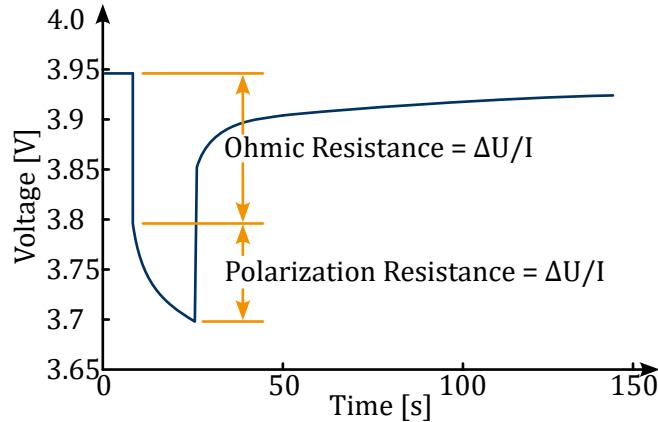


Figure 2.6: Pulse discharge response curve of Li-Ion cell [42].

The battery voltage experiences a jump-decline at first when the discharge current is applied. The voltage then slowly declines further. After removing the discharge current, the voltage similarly experiences a jump-like increase followed by a slower rise. The internal resistance is obtained by dividing the voltage loss by the discharge current. This provides a simple and accurate method for the calibration of the internal resistance, however it does not allow continuous real-time determination. Further methods for identifying the internal resistance are presented in [42].

2.3.6 Energy and Power

In battery applications, the energy is defined by the charge the battery cell can provide to the outside of its enclosure. The chemical energy stored inside the electrochemical system can be calculated using the theorem of Gibbs free energy by the laws of electrochemical thermodynamics. This energy is the theoretical energy W_T inside the cell. According to Equation 2.20, it is the product of the number of electrons n , the Faraday constant F and the Electromotive Force E_{EMF} .

$$W_T = -\Delta G = n \cdot F \cdot E_{EMF} \quad (2.20)$$

The energy available to the load is always less than the theoretical energy. It can be calculated as the integral of the product of the voltage $U(t)$ and the current $I(t)$ over time.

$$W_A = \int_{t_0}^t U(t) \cdot I(t) dt \quad (2.21)$$

In a practical application, the actual energy can also be estimated by the product of the rated capacity C_R and the rated voltage U_R .

$$W_A = C_R \cdot U_R \quad (2.22)$$

The energy density is defined as the energy per unit volume or mass. It is either given by Equation 2.23 for the mass energy density or by Equation 2.24 for the volumetric energy density.

$$W'_m = \frac{W}{m} \quad (2.23)$$

where W is the stored energy and m is the mass. The unit of W'_m is Whkg^{-1} .

$$W'_V = \frac{W}{V} \quad (2.24)$$

where V is the volume element. In this case, the unit of W'_V is WhL^{-1} .

The battery power is defined as the output energy per unit time and is given in W or in kW. Like the energy density, the power density can be calculated by dividing the available power by the mass or volume element. This results in Equation 2.25 and Equation 2.26, given in Wkg^{-1} and WL^{-1} .

$$P'_m = \frac{P}{m} \quad (2.25)$$

$$P'_V = \frac{P}{V} \quad (2.26)$$

[19]

2.3.7 Discharge and Charge current

As the performance of a battery cell is significantly affected by the charge and discharge current, those should always lie within the manufacturer's given range. The recommended maximum continuous charge or discharge current is denoted by the *C-rate*, which describes the relation between the battery capacity and the current. For example, the *C-rate* for a current of 3 A in a battery cell with a rated capacity of 10 Ah is 0.3 C. Operating a cell outside the given limitations may damage the cell in the long term and may even cause a thermal runaway, meaning that the cell catches fire. Another characteristic is the *hour-rate*, which describes the required time to fully discharge a battery cell with a given rated capacity at a given constant current. For example the *hour-rate* for a discharge current of 10 A in a battery cell with a capacity of 50 Ah is 5 h. This implies that the lower the *hour-rate*, the higher the rated discharge current. The rated capacity of a battery cell should always be given along with the *C-rate* to provide rigorous information about the performance limitations of the battery cell [19].

2.3.8 Lifetime and Self-Discharge

Different degradation mechanisms lead to a decrease in battery performance following many charge and discharge cycles. Those mechanisms that cause a limited battery lifetime can be classified into degradation models. The first model describes the loss of

lithium, which is the result of lithium-consuming side reactions including the formation of a Solid Electrolyte Interphase (SEI) film, electrolyte decomposition and lithium plating. The second mechanism involves the loss of material, resulting in a loss of storage capacity. Since both mechanisms greatly vary depending on the material, different cell chemistries show different ageing and lifetime properties. For example, the working voltage of a graphite anode is lower than the electrochemical window of usual electrolytes, which leads to the formation of a SEI film. An LTO cell would not experience SEI film formation in the Lithium Titanium Oxide since the LTO's potential is located in the electrochemical window of the electrolyte [44].

Self-discharge describes the capacity loss due to parasitic chemical reactions arising from thermodynamic instability of electrodes and their respective redox reactions. Self-discharge differs between reversible and irreversible capacity loss. The capacity lost during reversible self-discharge can be regained if the battery is recharged, which is impossible for irreversible capacity loss. The used materials influence the self-discharge process and vary across different cell chemistries. The Self Discharge Rate (SDR), describing the capacity loss due to self-discharge, is given by Equation 2.27, where t is the storage time, C_0 is the initial capacity and $C(t)$ is the remaining capacity at a given time t [19].

$$SDR = \frac{C_0 - C(t)}{C_0 \cdot t} \quad (2.27)$$

2.4 Key Technologies of a Battery Management System

2.4.1 Design Requirements

The Battery Management System is the supervision and control unit required to safely operate large Energy Storage Systems, consisting of many battery cells providing high currents at high voltage levels. BMSs are widely used across all areas where energy is stored using electrochemical storage systems. This includes but is not limited to industrial and personal transportation applications, grid storage systems and logistics. According to the regulations established by the International Electrotechnical Commission (IEC) in 1995 (IEC 61508 [45]), the main task of a BMS is to monitor electrical parameters of an ESS, including cell voltages, temperatures and stack current, ensuring the operation of a battery stack within its operating range. The acquired data by the BMS enables overall performance improvement of ESSs in terms of efficiency and storage capacity whilst avoiding the cells being charged or discharged above or below their respective limits. Performance enhancement is mainly achieved by equalising cell voltages in a system of series-connected cells, see section 2.5. The continuous measurement of battery parameters also allows for an estimation of the State of Charge and State of Health of the ESS by analysing each charge-discharge cycle of every cell inside a stack [34]. To allow a safe operation of high voltage Energy Storage Systems, it is crucial to include a galvanic isolation between the high voltage system of the battery and the surrounding control system, requiring the BMS to work with isolated serial communication protocols.

2.4.2 BMS Architecture

The principle of operation to meet the requirements mentioned above is structured into the following categories, whereas this work will focus on the task of battery equalisation.

- Data acquisition
- Data management, processing, storage and communication
- Battery equalisation management
- Battery thermal management

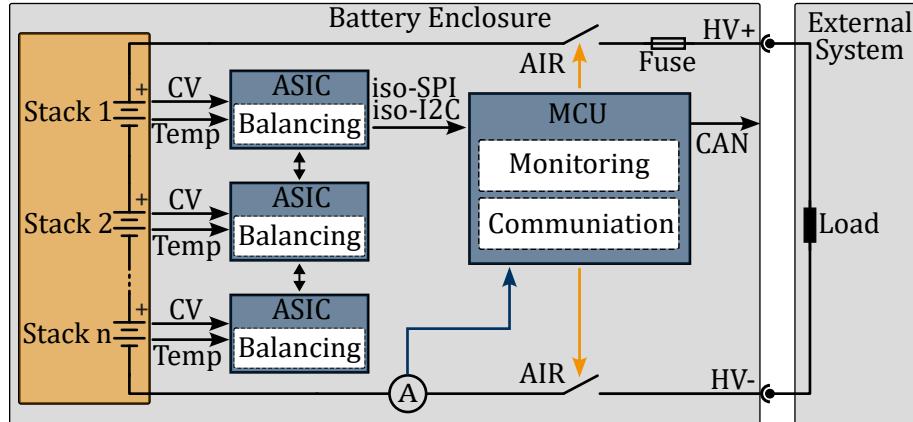


Figure 2.7: Structure of a Battery Management System.

The typical structure of a BMS is depicted in Figure 2.7. To allow safer working and maintenance conditions and enhance fire protection, battery packs are often divided into several stacks, each storing a limited amount of energy. Cells inside a stack are connected in series to reach a desired stack voltage. Common stack voltages typically range from 48 V to 100 V. Numerous series-connected cells may be connected in parallel to increase the overall capacity, with the advantage that parallel-connected cells always have the same voltage. The stacks may then be further connected in series to reach the system voltage. Typical system voltages vary depending on the application, ranging from 48 V in mobile robot applications to up to 1000 V in automotive applications. Stacks are usually separated by fire-retardant material. Cell voltages and temperatures are measured by an appropriate Application Specific Integrated Circuit (ASIC), acting as slave-elements in a Master-Slave system. Single chips usually allow monitoring of up to 16 cells, resulting in one chip per stack. Commercially available chips are for example the LTC6811-series [46] from *ANALOG DEVICES*, the BQ76952-series [47] from *TEXAS INSTRUMENTS* or the TLE9012DQU-series [48] from *INFINEON*. These ASICs also provide digital outputs to control switched resistor balancing circuits, see 3.1.3 and are equipped with further General Purpose Input-Output ports (GPIO) to control multiplexers and allow temperature measurements. The ASICs are daisy-chained with a galvanically isolated communication protocol passing through each. The first and/or last IC is connected to the Master-element of the system, which is usually a Microcontroller Unit (MCU). Cell voltages and temperatures sampled by each stack's ASIC are transmitted to the MCU by serial communication. Typical communication protocols are Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I^2C) or Universal Asynchronous Receiver-Transmitter (UART). To maintain isolation between the High Voltage

System (HVS) and the Low Voltage System (LVS), serial communications inside the ESS are isolated from the Microcontroller Unit, requiring bidirectional isolators between the serial communication line and the MCU interface (e.g. iso-SPI or iso-I²C). The actual monitoring of the ESS-parameters takes place inside the MCU, which usually can also block the power transmission to the load by opening the Accumulator Isolation Relay (AIR) on both poles of the battery stack in case of critical system values.

2.4.3 Data Acquisition and Management

The overall operation of a BMS rests on accurately measuring the cell parameters inside a battery stack. The most critical input signals are the main current sensor measuring the output current of the battery pack, the cell voltage signals and the cell temperature signals. Other sensors, e.g. for humidity measurement, may be added to the system according to the requirements of the operating environment. Measurement accuracies usually range from 0.1 % to 0.5 % for currents up to 450 A, 1 mV to 2 mV for cell voltages, 0.1 % for total battery voltage and 0.5 % for temperatures ranging from -10°C to 85°C [34], [49]. The required accuracies vary depending on the application and the used cell chemistry type. Lithium-Ion cell types usually require high measurement accuracy for voltages and temperatures. The data acquisition rate is determined by the sampling rate and the priority of the assessment, in which higher sampling rates are usually required for cell voltages and current measurements to allow precise state estimation. In comparison, lower sampling rates are primarily sufficient for temperature measurements. Based on the acquired data, the BMS controls interfaces such as switching signals for isolation relays, speed control for cooling fans and communication interfaces [34].

Most sampling chips cannot store sampled data but transmit raw data upon request through serial communication by the controller. If the application requires data storage within the isolated peripheral, it may be implemented using Electrically Erasable Programmable Read-Only Memory (EEPROM) or similar technologies. The hardware of the voltage sampling circuit follows the design recommendations from the manufacturer of the sampling chips, but usually consists of a low-pass filter unit on each port of the voltage measurement section. The typical hardware circuit is depicted in Figure 2.8 where commonly used values are $20\ \Omega$ for R_f and $220\ \text{nF}$ for C_f , both components acting as low-pass filter elements to stabilize the input signals on the voltage measurement pins of the ASIC [47].

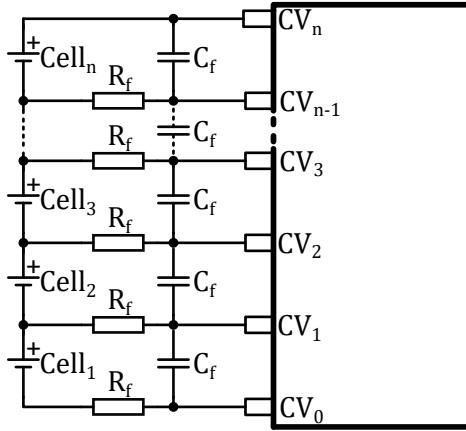


Figure 2.8: Typical schematic of the cell voltage measurement circuit.

The voltage of cell 1 is measured with reference to the most negative cell tab of the series, and the subsequent voltages are then measured with respect to the adjacent lower cell voltage. This means that each cell voltage is calculated by the difference of the stack voltage at the positive pin U_n of the desired cell and the adjacent lower cell voltage U_{n-1} , as described in Equation 2.28.

$$CV_n = U_n - U_{n-1} \quad (2.28)$$

The cell temperatures are usually measured using Positive Temperature Coefficient (PTC) or NTC resistors. A typical schematic is shown in Figure 2.9, where commonly used pull-down resistors have a resistance of $10\text{ k}\Omega$ and the input capacitor at the ADC port is usually in the range of 100 nF . An auxiliary resistor R_1 may be used to adjust the input voltage level. The voltage V_{ref} is usually generated by a built-in voltage regulator in the sampling chip and is galvanically isolated from the Low Voltage system. The circuit output is sampled on a defined time base by an ADC-pin of the cell voltage sampling chip. In most cases, multiplexers are required to route the temperature signal to the sampling chip since there are more cells in the stack than available ADC-pins on the ASIC.

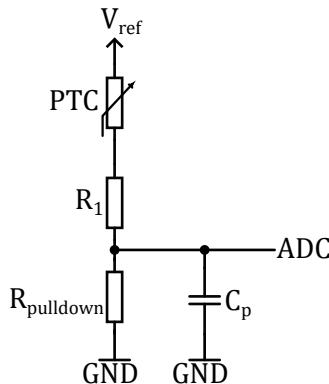


Figure 2.9: PTC temperature measurement schematic.

The charge or discharge current can be measured by hall-effect sensors or shunt resistors. A similar circuit, as described above, may be used to filter the input signal.

2.5 Cell Voltage Equalization

2.5.1 Sources of Imbalance

Due to the voltage of an individual battery cell being limited by its electrochemical characteristics, a large number of cells are usually connected in series to meet the voltage criteria and in parallel to respect the power and energy criteria required for vehicular applications. The primary difficulty in operating serially connected cells is the cell imbalance in cell voltage, storage capacity, and internal resistance. The imbalance has various sources and begins during the manufacturing process of the cell, after which the actual capacities of the cells follow a normal distribution with a standard deviation of 1.3 % to the nominal capacity [50]. Manufacturing imbalances can be avoided by sorting out differing cells after the steps mentioned below, however this does not apply to cells once they are in operation.

The manufacturing process of a battery cell includes several steps and begins with the dry mixing of the active materials with eventual additives and binders. For Li-Ion cells, the anode material is usually made up of 90 wt.% graphite mixed with nano-microscopic carbon and a binder material, e.g. Carboxy-Methyl Cellulose (CMC). The cathode material consists of e.g. $\text{Li}(\text{NiMnCo})\text{O}_2$ (90 wt.%) with added nano-microscopic carbon and binder material. The dry-mixing step is followed by wet-mixing, where solvents, e.g. N-Methyl-2-Pyrrolidone, are added. This process can be executed under vacuum conditions to avoid gas intrusions. Next, a copper or aluminium foil is coated with the previously mixed slurry. The solvent is removed by heat supply during the drying process. The coated foil is then compressed by a rotating pair of rollers, statically discharged and cleaned by brushes or airflow. The wide electrode foil is cut into several smaller foils by rolling blades during slitting. The smaller rolls are then stored in a vacuum oven and dried for 12 h to 30 h where residual moisture and solvents are removed from the coil. For the production of pouch cells, the rolls are then unrolled again, and the cathode, anode and separator sheets are separated from the rolls using shear cut punching tools. The cathode and anode material, separated by a separation sheet, are then stacked multiple times, where a blank edge is left for the welding of the tabs in the next step. Afterwards, the stacks are packed and the electrolyte is filled in under vacuum [51].

All manufacturing steps mentioned above require tolerances, leading to slightly different properties of each cell. Manufacturing differences have their seeds within the purity of the manufacturing materials and the subsequent homogeneity of the mixing process, the particle size and the viscosity. During the coating process, inconsistencies in the coating thickness in and across the coating direction may affect the surface quality and the adhesion between the coating and the substrate. The drying process further influences the adhesion between the coating, substrate, and surface finish. It is affected by residual humidity, temperature consistency, and other factors. During the pair of rollers' compression, the porosity, surface texture, and adhesion between the coating and substrate are once again subject to characteristic inhomogeneity. The subsequent cutting may produce a cutting burr on the edge geometry and induce thermal and mechanical stress to the coating. Further, a particle contamination of the material might occur during

the cutting process. During assembly, the position accuracy of the cathode and anode, as well as the damage gradient of the surfaces and edges, directly impacts the cell's final capacity [51].

The second source of imbalance is ageing mechanisms, which further support characteristic variation of the cells as they affect each cell with a slightly different effect. Ageing mechanisms can be observed during use and storage. Battery cycle life is commonly defined as the number of charge/discharge cycles the battery can sustain while keeping a given percentage of its initial capacity, usually 80 %. It depends on the operating conditions, including charge and discharge protocols, surrounding temperature and the Depth of Discharge (DOD). Ageing mechanisms result from a number of side reactions, whereas the positive and negative electrodes are the most critical areas, more specifically, the interface area between the electrolyte and the electrode. Degradation modes can generally involve either loss of lithium ions that become no longer available to shuttle between both electrodes, or loss of active material in the electrodes. The loss of lithium ions results from parasitic reactions like film formation, electrolyte decomposition or lithium plating, leading to a consumption of lithium ions. Loss of active material is a fallout from transition metal dissolution, particle cracking or decohesion related to mechanical stress during operation [52].

2.5.1.1 Negative Electrode

Negative electrodes are usually composed of graphite, carbon, titanate or silicone, and the choice of material greatly affects the ageing and safety properties of the cell. The main factor of ageing in time is the development of a SEI. The SEI film is created during the first charge of the cell. Its role is to protect the negative electrode from eventual corrosion and the electrolyte from possible reductions. This occurs mostly during the beginning of the battery life cycle and acts as a natural barrier between the negative electrode and the electrolyte. However, the SEI is unstable as the Li-Ion battery operates at voltages outside of the electrochemical stability range of the electrolyte. This leads to a further development of the SEI, which induces a loss of lithium ions and provokes an electrolyte decomposition [53]. Furthermore, the loss of available lithium due to side reactions at the graphite negative electrode was reported as a major source of ageing during storage periods [54], meaning that the SEI itself is relatively stable within its stability window allowing a usage of Li-Ion batteries over a long period of time [53].

2.5.1.2 Positive Electrode

The positive electrode is subject to a low alteration over time, depending on the used material. A SEI is also created on the interface between the positive electrode and the electrolyte, however this is more difficult to detect due to the higher voltages present at the positive electrode. The principal sources of ageing on the positive electrode are electrolyte degradation, oxidation, and dissolution of the positive electrode in the electrolyte [55].

Nevertheless, various studies confirmed that the main ageing effect occurs at the negative electrode [56].

2.5.1.3 Calendar Ageing

Calendar ageing describes the irreversible degradation during storage, highly dependent on the self-discharge rate according to the storage conditions, such as storage temperature [57]. At high temperatures, parasitic side reactions are accelerated, leading to a higher loss of lithium than in moderate temperatures, inducing a fade of capacity. Low temperatures tend to limit the development of these phenomena but accelerate the loss of material diffusion and alter the battery chemistry [53].

The principal variable of calendar ageing is the SOC during storage, defining the proportion of ions on electrodes. A more significant potential disequilibrium on the electrode and electrolyte interface promotes parasitic side reactions. Thus, for equal temperatures but different SOC, the cells do not age in the same way. A higher battery degradation at higher SOC was shown in [58]. Furthermore, degradation and the resulting capacity fade and resistance augmentation are not linear with time, implying a strong interaction of the ageing behaviour with the elapsed time [53].

2.5.1.4 Cyclic Ageing

Cyclic ageing takes place during charge or discharge of the battery. It is directly affected by temperature conditions, the utilisation mode, the previous state of the battery, and the charge and discharge current. All parameters influencing calendar ageing also affect cyclic ageing. Further, the ΔSOC has a great impact on the ageing behaviour, as it was shown in [59] that high ΔSOC during usage results in a loss of power over numerous cycles. In addition, it was demonstrated that high charging voltages reduce the End-of-Life (EOL) capacity may be only 70 % when continuously raising the charging voltage by 0.1 V [60]. Likewise, the discharge voltage influences the ageing behaviour by affecting the internal impedance [61].

2.5.1.5 External Sources

While the sources of cell voltage imbalance within a stack originate from chemical and manufacturing differences, they may be further amplified during operation by external consumers or differences in thermal stress. External consumers are electronic circuits within the stack and often act as slave elements of the BMS. These may be ICs for cell voltage measurements, temperature measurement or serial communication. While hardware designs should aim to strain all cells equally, low voltage applications may draw their supply voltage from single cells instead of the stack voltage in combination with an Low-Dropout (LDO) regulator.

The second source of imbalance is the uneven distribution of heat generated during operation. Excessive heat generation not only reduces the efficiency of LIBs but also accelerates the lifetime degradation. Various sources have analysed the heat distribution across cell stacks and have demonstrated that the inner cells experience a higher heat-induced stress than cells on the outer circle of the stack [62]–[64]. Furthermore, cooling techniques are less effective for inner cells [65]. Since the properties of cells depend on the operating temperature, parameters like internal impedance vary across the battery during charge or discharge. This leads to an unequal voltage drop due to the resistance in each cell, resulting in different OCVs after the operation.

2.5.2 Implication of Imbalance

After several charge and discharge cycles, the ESS finds itself in an unbalanced state due to the internal and external sources mentioned subsection 2.5.1, meaning the single cells connected in series inside the battery pack have different SOCs. During the next charging phase, the cell with the highest initial SOC will reach the upper cut-off voltage first and require the charging process to end to avoid internal damage to the cell. The remaining cells, hence, have an unused capacity that can not be used for energy storage, as the safety and protection systems will trigger an error for overcharging if the stack gets further charged.

During the discharge phase, the cell with the lowest SOC will reach the lower cut-off voltage while the other cells still have remaining energy left, however the whole series can not be further discharged. As shown in Figure 2.10, this results in an unused stack capacity during charging and an unused energy during discharging. This leads to a lower energy efficiency of the ESS [6].

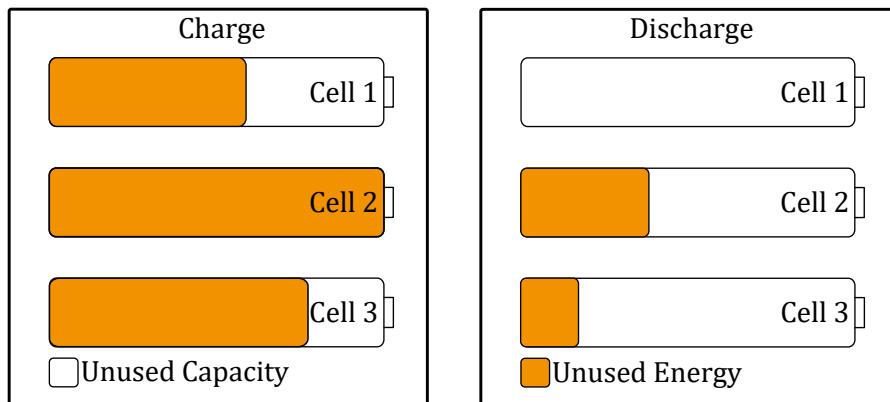


Figure 2.10: Unbalance of battery cells [6].

2.5.3 Balancing Control Variables

State variables play a key role in the balancing control for ESS. Suitable state variables can reduce the complexity of the algorithms and improve balancing efficiency [19], [66]. The critical factors of the balancing control variables are the relation between the variable and the SOC, the complexity of measurement, the sampling accuracy of the control variable and the possible sampling frequency. Balancing control can be based on the actual battery voltage, the State of Charge or the battery capacity. The characteristics of the three methods are compared in Table 4.6, while the direct voltage measurement is the most commonly used in modern BMSs [19].

Since battery capacity is barely used as a control variable in modern systems, this topic will not be further discussed in this work.

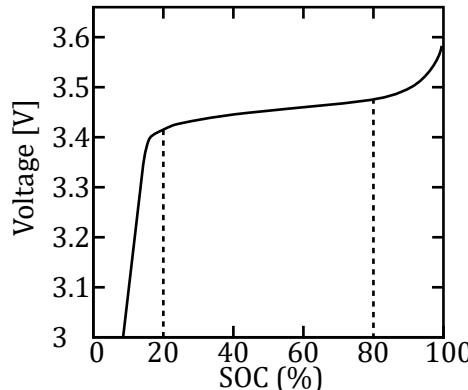
2.5.3.1 Voltage-based Balancing Control

The Cell Voltage is the most commonly used input variable for commercially available balancing chips and standard control algorithms. Its main advantage is that it is the only

Table 2.4: Comparison of the characteristics of each balancing control variable [19].

	Balancing variables		
	Actual voltage	SOC	Battery capacity
Advantage	High accuracy High sampling frequency	Reflect system inconsistencies	Reflect system status
Disadvantage	Voltage plateau in discharge curve Difference between OCV and actual voltage	Poor accuracy High estimation complexity Poor real-time performance	No direct measurement Complex calculation

variable to be directly measured, and the sampling frequency can be adjusted without extra effort. However, only the instant voltage can be measured during the cell's charge or discharge phase. Hence, the OCV and the difference between the actual voltage that is measured and the OCV remain unknown, allowing only limited accuracy on the reflection of the system status. As shown in Figure 2.11, the difference between the Open Circuit Voltage and the State of Charge is small in the SOC area between 20 % to 80 % but causes large variations when the SOC is below 20 % or above 80 % [19].

Figure 2.11: OCV-SOH curve of a Lithium Iron Phosphate (LiFePO₄) battery cell [19].

The real-time OCV can not be measured directly during operation due to voltage hysteresis and the required time delay as described in subsection 2.3.5. Figure 2.11 displays the second major issue concerning voltage-based balancing control, namely the voltage plateau if the SOC is between 20 % to 80 %. It can be observed that the voltage drops very slowly when charging or discharging a cell between the given range. This effect further reduces the accuracy of the reflection of the system state [19].

2.5.3.2 SOC-estimation based Balancing Control

While the SOC is one of the most common parameters to display the remaining energy stored in a cell, it can not be measured directly. As described in subsection 2.3.1, different

estimation methods such as Coulomb counting according to Equation 2.11 apply. This is a rather simple estimation method, but errors may accumulate. For a better real-time estimation, model-prediction methods, divided into physics-based models and data-driven models, are used. Online SOC estimation is performed in physics-based models based on filter algorithms. These models offer the advantage that they work with fewer parameters than other electrochemical models, e.g. the first-order cell model as described in Figure 2.5, working with three parameters and offering a capture of the dynamic behaviour of a cell. Electrochemical models provide high accuracy since they are based on chemical reactions. This, however, involves many parameters, resulting in a problematic parameterisation, requiring the usage of Kalman filters and information filters for model prediction. Kalman filters are pretty popular as they offer high estimation accuracies with decent computational costs [19].

3 Literature Review

3.1 Passive balancing

In passive balancing, the energy excess in higher-charged cells is dissipated as thermal energy. Although remnant capacity is released from the higher-charged cells, lower-capacity cells cannot be charged by the released energy. The main advantage of such circuits is their simplicity in terms of implementation and cost. They are therefore often applied in EV energy storage systems. As depicted in Figure 3.1, three passive balancing topologies are currently available, among them switched resistor balancing is the most commonly used [7], [19].

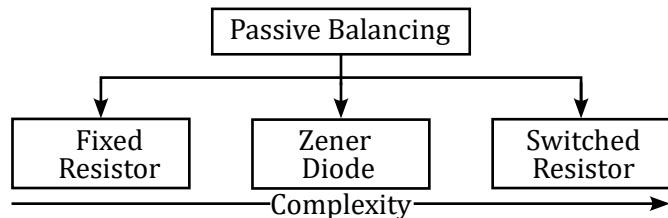


Figure 3.1: Passive balancing topologies [7], [19], [67].

The heat generation in all passive circuits follows Joules' Law according to Equation 3.1 with I_{balance} being the current passing as shown in Figure 3.2[19] and R_{tot} being the total resistance of the balancing circuit.

$$P_{\text{dissipation}} = I_{\text{balance}}^2 \cdot R_{\text{tot}} \quad (3.1)$$

3.1.1 Fixed Resistor Balancing

Among passive balancing topologies, the fixed resistor topology, as depicted in Figure 3.2, is the simplest and cheapest to implement.

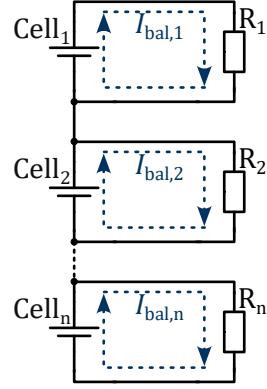


Figure 3.2: Fixed Resistor balancing circuit [7].

Since the resistors act like a voltage divider connected in parallel to the cells, the cell voltages aim to match the voltage drop on the resistors, leading to all cells having the same voltage. Equation 3.1 applies for the heat generation, where the total balancing resistance R_{tot} is the sum of the internal resistance R_i of the cell and the balancing resistor R_n . Hence, Equation 3.1 results in Equation 3.2.

$$P_{\text{dissipation}} = I_{\text{balance}}^2 \cdot (R_i + R_n) \quad (3.2)$$

3.1.2 Zener Diode Balancing

The circuit shown in Figure 3.2 can be modified by adding a Zener diode in series to the resistor like depicted in Figure 3.3 [68], allowing a more precise balancing as the fixed resistor topology.

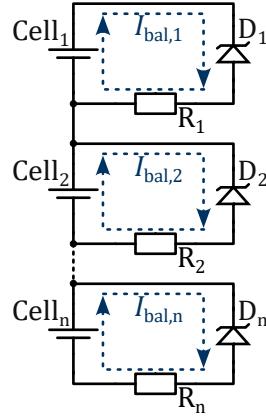


Figure 3.3: Zener Diode balancing circuit [68].

When the cell voltage is below the Zener diode's breakdown voltage, the Zener diode is in its reverse-bias state and non-conducting. If the cell exceeds the Zener diode's breakdown voltage U_z , the Zener diode starts conducting in reverse, shunting the excess charge through the resistor, which also acts as a current limiting device for the balancing

current according to Equation 3.3.

$$I_{\text{bal}} = \frac{U_{\text{Cell}} - U_z}{R_{\text{tot}}} \quad (3.3)$$

The balancing resistance R_{tot} must be elaborated from Equation 3.2 but with the added resistance of the Zener diode in conducting mode R_D . Hence, the power loss equation results in Equation 3.4

$$P_{\text{dissipation}} = \frac{(U_{\text{Cell}} - U_z)^2}{R_n + R_i + R_D} \quad (3.4)$$

This technology is primarily used to prevent overcharging the battery cell.

3.1.3 Switched Resistor Balancing

The Zener diode in Figure 3.3 can be replaced by a switch, which in most cases is a MOS-FET. This allows for a more accurate balancing but requires more parts and a control system. ASICs like the *LTC6811*-series from *ANALOG DEVICES* [46], the *BQ76952*-series from *TEXAS INSTRUMENTS* [47] or the *TLE9012DQU*-series from *INFINEON* [48] offer analogue input pins to measure each cell voltage of a stack and to control the switches. The balancing circuit known from the figures above can hence be further developed to the circuit depicted in Figure 3.4.

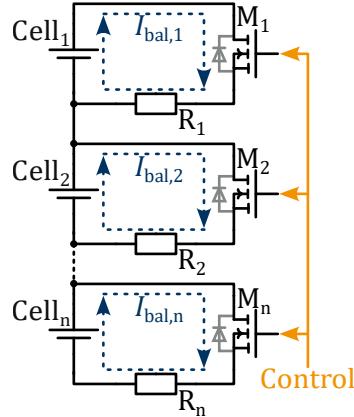


Figure 3.4: Switched Resistor balancing circuit with NMOS-switches [19], [68], [69].

Once again, the power loss is deduced from Equation 3.1 but extended with the resistance of the transistor in conducting mode. This results in Equation 3.5. The control system allows for stopping balancing when the difference between the cell voltages is within an acceptable range and avoids energy loss due to balancing minimal voltage differences.

$$P_{\text{dissipation}} = \frac{U_{\text{cell},n}^2}{R_n + R_i + R_{\text{DSon}}} \quad (3.5)$$

3.2 Active balancing

Active balancing topologies use non-dissipative circuits, and cell balancing is done by moving charge from high-energy cells to lower-energy cells. Figure 3.5 shows the classi-

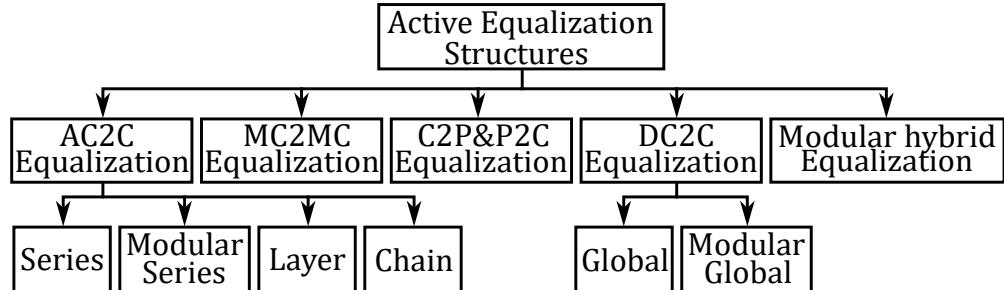


Figure 3.5: Classification of active equalisation structures according to the energy path [70].

fication of active equalisation structures according to the energy equalisation path. Adjacent Cell-to-Cell (AC2C) describes the energy transfer between two adjacent cells inside a stack and is the simplest and cheapest implementation. It can act on many levels, ranging from balancing two single adjacent cells up to balancing two high-energy modules of a grid-scale energy storage system [71]. Direct Cell-to-Cell (DC2C) equalisation includes topologies capable of balancing two arbitrary cells inside a stack or moving charge between two modules of an energy storage system. DC2C can further be enhanced to Multi-cell to Multi-cell (MC2MC) equalisation, enabling energy transfer directly from highly charged cells to lower charged cells with the ability to balance multiple cells simultaneously [72]. Cell to Pack (C2P) or Pack to Cell (P2C) is an equalisation structure feeding energy excesses from overcharged cells back to the entire pack to prevent single cells from overcharging [73]. Modular hybrid equalisation adjusts the cell voltages inside a stack using passive or active equalisation and furthermore balances stack voltages of all arbitrary modules of large-scale ESS [74]. Active balancing circuits can further be classified according to their energy storing element as shown in Figure 3.6. Three main categories are available, where energy is either stored in capacitors, inductors or is transferred by DC/DC-Converters.

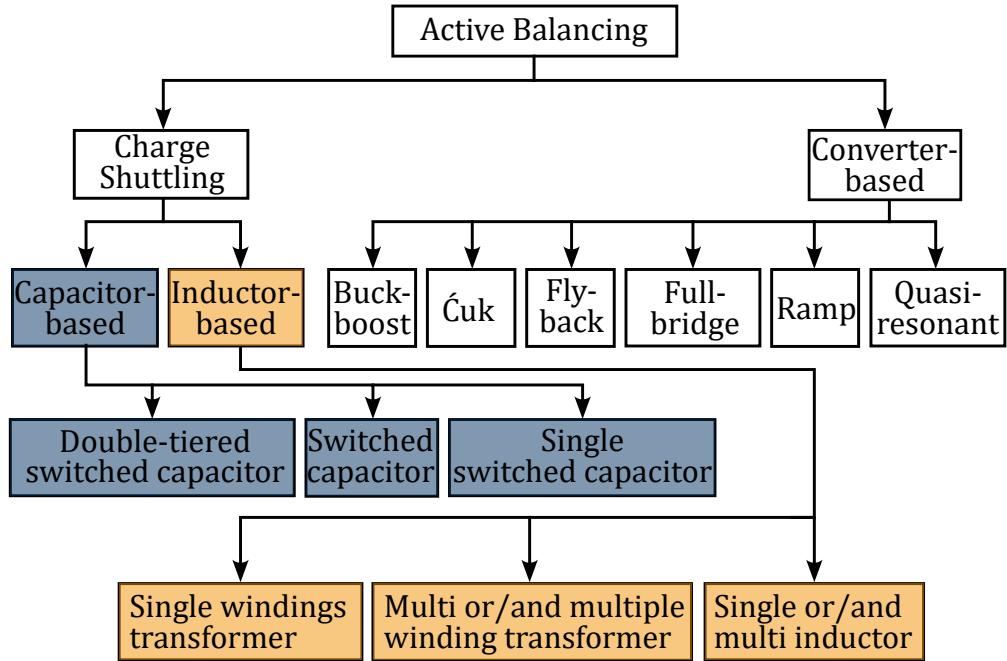
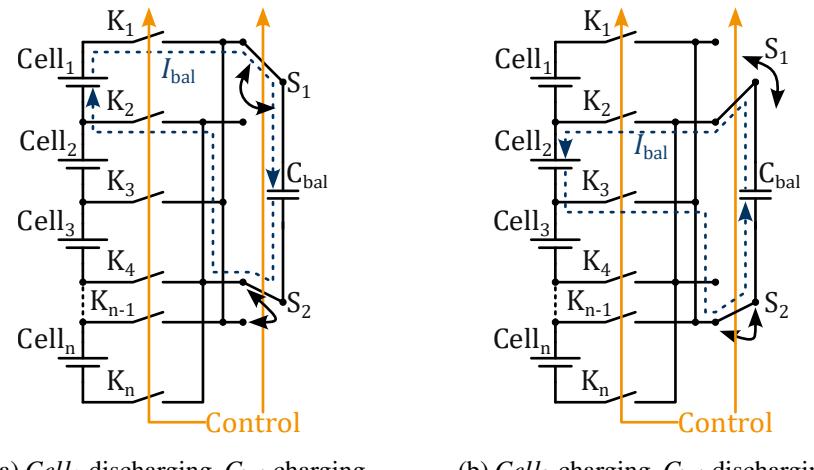


Figure 3.6: Classification of active balancing circuits according to their energy storing element [67].

3.2.1 Capacitance-based Balancing

Active balancing based on capacitors as energy storing elements is simple and low cost while still offering balancing efficiencies up to 94.5 % [75]. The simplest implementation concept is the single switched capacitor topology as shown in Figure 3.7. The positive and negative poles of each cell are connected by switches to a balancing grid. The grid is further connected to the balancing capacitor C_{bal} . The actual implementation of switches and the current path may differ, see chapter 5.



(a) $Cell_1$ discharging, C_{bal} charging. (b) $Cell_2$ charging, C_{bal} discharging.

Figure 3.7: Single Capacitor topology [19].

The signal waveform is depicted in Figure 3.8, where the control of the switches is performed by a Pulse Width Modulation (PWM). During the phase $t_0 < t < \frac{T}{2}$, where the PWM signal is at a logical *HIGH*, the higher charged cell is discharged, resulting in a positive balancing current draining from cell C_2 and a voltage drop of C_2 . As a result of the positive balancing current, the balancing capacitor gets charged. The PWM-signal drops to logical *LOW* at the timestamp $t = \frac{T}{2}$, inducing a negative balancing current and causing the capacitor voltage to drop exponentially. Current now flows from the balancing capacitor to the lower charged cell, causing the voltage of the receiving cell to rise until it reaches the falling capacitor voltage. Both voltages then slowly drain until they equalise on a steady level. At the timestamp $t = T$, the charging process of the lower charged cell and the discharging phase of the balancing capacitor end and the process can be started again.

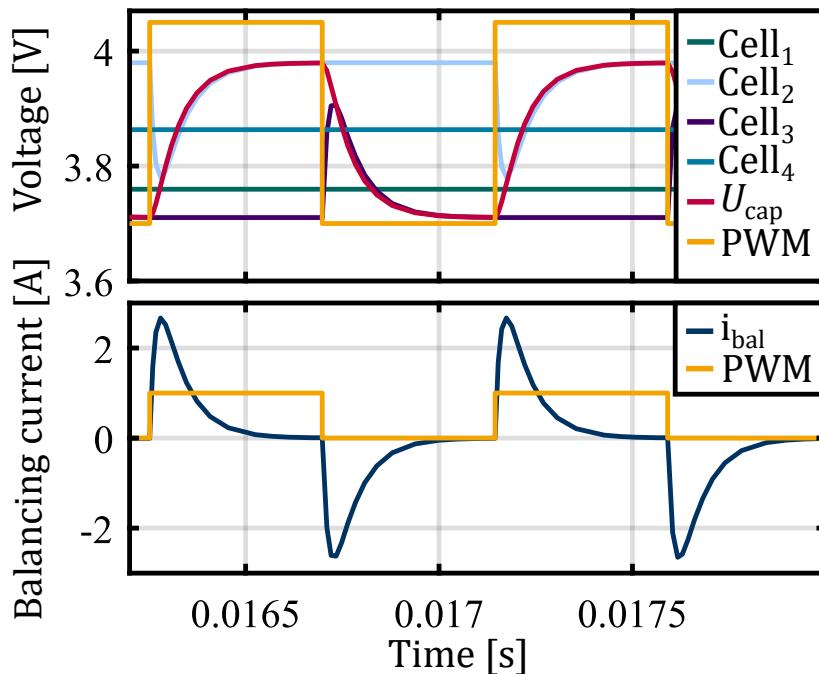


Figure 3.8: Cell voltage waveform and balancing current at an optimal PWM-frequency and a duty cycle of 50 %. C_2 is emitting charge and C_3 is receiving charge. The voltage of the other two cells remains unchanged. The PWM-signal is scaled and without a unit [66].

The balancing current can be approximated using the equivalent circuit depicted in Figure 3.9.

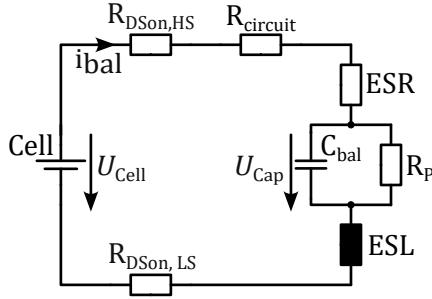


Figure 3.9: Single Switched Capacitor equivalent circuit.

A single switched capacitor balancing circuit's equivalent circuit in conducting mode consists of the drain-source resistance R_{DSon} of both the high-side and the low-side switch. In addition, a parasitic resistance of the circuit (e.g. track resistance on a PCB) needs to be added. Furthermore, the balancing capacitor C_{bal} has an Equivalent Series Resistance (ESR), a parasitic resistance R_p , connected in parallel to the capacitor and an Equivalent Series Inductance (ESL). The corresponding equation can be written as follows.

$$U_{Cell} = U_{HS} + U_{R,circuit} + U_{ESR} + U_C + U_{ESL} + U_{LS} \quad (3.6)$$

Applying Ohm's law and the voltage equation for inductors, Equation 3.6 can be extended to Equation 3.7.

$$U_{Cell} = i_{bal} \cdot \underbrace{(R_{DSon,HS} + R_{circuit} + R_{ESR} + R_p + R_{DSon,LS})}_{R_{tot}} + L_{ESL} \cdot \frac{\partial i_{bal}}{\partial t} \quad (3.7)$$

The balancing current can be deducted from the general equation applying for currents on a capacitor as per Equation 3.8.

$$i_{bal}(t) = C \cdot \frac{\partial U(t)}{\partial t} \quad (3.8)$$

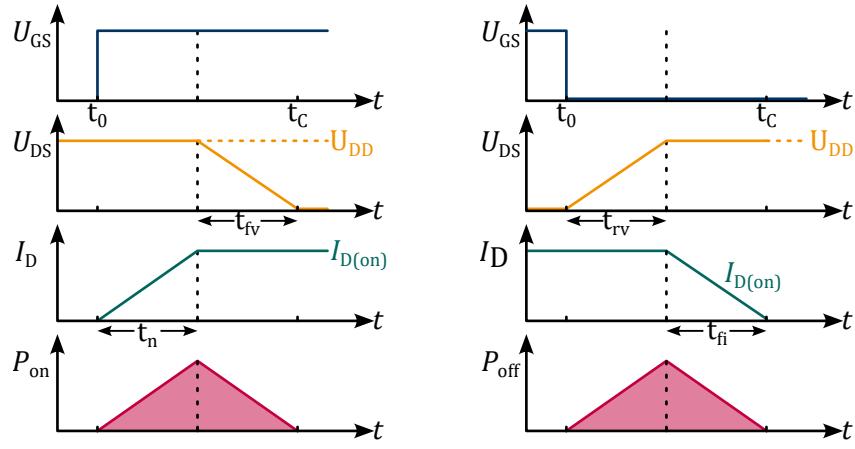
where $\partial U(t) = U_{Cell}(t) - U_{Cap}(t)$.

3.2.1.1 Power Loss

Figure 3.9 and the equations mentioned above allow for an estimation of the power loss during balancing. The power loss can be divided into two phases, which are defined by the phase of the MOSFET, namely its conduction phase and its switching phase. During the conduction phase, the power loss as a function of the balancing current as per Equation 3.8 is given by Equation 3.9, where R_{tot} is the sum of all resistances in the balancing circuit as described in Equation 3.7 and D is the duty cycle of the PWM-signal.

$$P_{loss,conducting} = i_{bal}^2(t) \cdot R_{tot} \cdot D \quad (3.9)$$

The switching losses can be approximated by analysing the general switching behaviour of MOSFETs as depicted per Figure 3.10. The following calculations display a simplified approach to switching losses; real applications often require the use of more complex numerical methods.



(a) Switching losses during MOSFET turn-on.
(b) Switching losses during MOSFET turn-off.

Figure 3.10: MOSFET switching behaviour [76], [77].

Turn-on losses

Figure 3.10a shows the gate-source voltage U_{GS} , the drain-source voltage U_{DS} , the drain current I_D and the power loss P_{on} during the switching phase of a MOSFET into conduction mode. Once the gate-source voltage is set to a high level, the drain current rises, charging the gate-source capacitance of the MOSFET. After rise-time t_{ri} , the drain-source voltage begins to fall from the systems U_{DD} -voltage during the fall-time t_{fv} given by the manufacturers datasheet to almost 0 V. The energy lost during this process is calculated by Equation 3.10.

$$E_{on} = I_{D(on)} \cdot V_{DD} \cdot \frac{t_{ri} + t_{fv}}{2} \quad (3.10)$$

The power loss P_{on} is calculated by multiplying the energy loss by the switching frequency f_{sw} as per Equation 3.11 [77].

$$P_{on} = E_{on} \cdot f_{sw} \quad (3.11)$$

Turn-off losses

The power loss during switching off can be calculated similarly by analysing the voltages depicted in Figure 3.10b. When the gate-source voltage U_{GS} is pulled to GND, the drain-source voltage U_{DS} starts to rise during the time t_{rv} until reaching the system's U_{DD} voltage. After that, the drain current I_D begins to fall until reaching 0 A. This phase takes the time denoted as fall-time t_{fi} . The energy loss during this phase is calculated by Equation 3.12.

$$E_{off} = I_{D(on)} \cdot V_{DD} \cdot \frac{t_{rv} + t_{fi}}{2} \quad (3.12)$$

Once again, the power loss P_{off} is calculated by multiplying the energy loss by the switching frequency f_{sw} as per Equation 3.13 [77].

$$P_{off} = E_{off} \cdot f_{sw} \quad (3.13)$$

3.2.1.2 Energy Shutting

According to Figure 3.11 [66], the voltage U_{Cap} across the balancing capacitor follows Equation 3.14, where $U_{\text{Cap},i}$ is the initial voltage of the balancing capacitor and $U_{\text{Cap},f}$ is the final voltage after the capacitor has been charged by the charge-emitting cell [78].

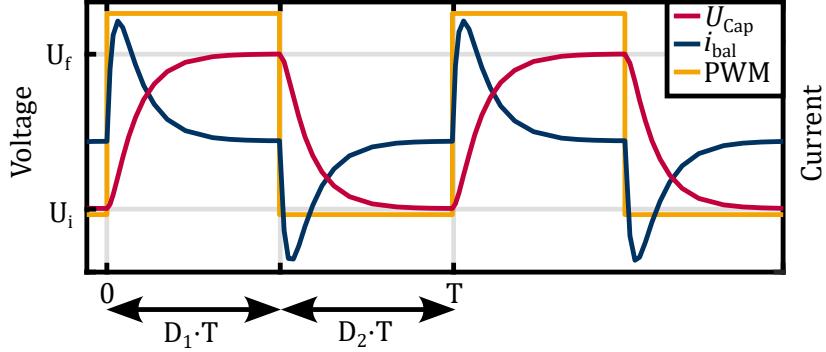


Figure 3.11: Voltage waveform over the period T with $D_1 = D_2 = D = 0.5$ [66].

Further, the time constant τ is a function of the internal resistance of the battery cell.

$$\begin{aligned} U_{\text{Cap,Charging}}(t) &= \underbrace{(U_{\text{Cap},f} - U_{\text{Cap},i})}_{U_{\text{diff}}} \cdot (1 - e^{-\frac{t}{\tau(R_{i,EM})}}) + U_{\text{Cap},i} \\ &= U_{\text{diff}} \cdot (1 - e^{-\frac{t}{\tau(R_{i,EM})}}) + U_{\text{Cap},i} \end{aligned} \quad (3.14)$$

The charging current $i_{\text{Cap,Charging}}$ is obtained by deriving the charging voltage with respect to the time t , where $R_{\text{seq}(R_{i,EM})} = R_{\text{tot}} - R_P$.

$$\begin{aligned} i_{\text{Cap,Charging}}(t) &= C_{\text{bal}} \cdot \frac{dU_{\text{Cap,Charging}}}{dt} \\ &= C_{\text{bal}} \cdot \frac{1}{\tau(R_{i,EM})} \cdot U_{\text{diff}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \\ &= \frac{U_{\text{diff}}}{R_{\text{seq}(R_{i,EM})}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \end{aligned} \quad (3.15)$$

The transferred energy E_{Charging} per pulse D is given by integrating the product of the capacitor voltage $V_{\text{C,Charging}}(t)$ and the balancing current $i_{\text{C,Charging}}(t)$ with respect to the time over half the period T as per Equation 3.16 [78].

$$\begin{aligned}
E_{\text{Charging}} &= \int_0^{DT} U_{\text{Cap,Charging}}(t) \cdot i_{\text{Cap,Charging}}(t) dt \\
&= \int_0^{DT} \left[U_{\text{diff}} \cdot \left(1 - e^{-\frac{t}{\tau(R_{i,EM})}} \right) + U_{\text{Cap,i}} \right] \cdot \frac{U_{\text{diff}}}{R_{\text{seq}(R_i,EM)}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}} dt \\
&= \int_0^{DT} \left[\frac{U_{\text{diff}}^2 \cdot e^{-\frac{t}{\tau(R_{i,EM})}}}{R_{\text{seq}(R_i,EM)}} - \frac{U_{\text{diff}}^2 \cdot e^{-\frac{2t}{\tau(R_{i,EM})}}}{R_{\text{seq}(R_i,EM)}} + \frac{U_i \cdot U_{\text{diff}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}}}{R_{\text{seq}(R_i,EM)}} \right] dt \\
&= \frac{U_{\text{diff}}}{R_{\text{seq}(R_i,EM)}} \int_0^{DT} \left[U_{\text{diff}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}} - U_{\text{diff}} \cdot e^{-\frac{2t}{\tau(R_{i,EM})}} + U_i \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \right] dt \\
&= \frac{U_{\text{diff}}}{R_{\text{seq}(R_i,EM)}} \left[\begin{array}{l} -\tau(R_{i,EM}) \cdot U_{\text{diff}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \\ + \frac{\tau(R_{i,EM})}{2} \cdot U_{\text{diff}} \cdot e^{-\frac{2t}{\tau(R_{i,EM})}} \\ - \tau(R_{i,EM}) \cdot U_i \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \end{array} \right] \Big|_0^{DT} \\
&= C_{\text{bal}} \cdot U_{\text{diff}} \left[-U_{\text{diff}} \cdot e^{-\frac{t}{\tau(R_{i,EM})}} + \frac{U_{\text{diff}}}{2} \cdot e^{-\frac{2t}{\tau(R_{i,EM})}} - U_i \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \right] \Big|_0^{DT} \\
&= C_{\text{bal}} \cdot U_{\text{diff}} \left[\frac{U_{\text{diff}}}{2} \cdot e^{-\frac{2t}{\tau(R_{i,EM})}} - e^{-\frac{t}{\tau(R_{i,EM})}} \cdot \underbrace{(U_{\text{diff}} + U_i)}_{=U_f} \right] \Big|_0^{DT} \\
&= C_{\text{bal}} \cdot U_{\text{diff}} \left[\frac{U_{\text{diff}}}{2} \cdot e^{-\frac{2t}{\tau(R_{i,EM})}} - U_f \cdot e^{-\frac{t}{\tau(R_{i,EM})}} \right] \Big|_0^{\frac{D}{F}} \\
&= C_{\text{bal}} \cdot U_{\text{diff}} \left[\left(\frac{U_{\text{diff}}}{2} \cdot e^{-\frac{2D}{\tau(R_{i,EM}) \cdot F}} - U_f \cdot e^{-\frac{D}{\tau(R_{i,EM}) \cdot F}} \right) \right. \\
&\quad \left. - \left(\frac{U_{\text{diff}}}{2} \cdot \underbrace{e^0}_{=1} - U_f \cdot \underbrace{e^0}_{=1} \right) \right] \quad [\text{J/pulse}] \tag{3.16}
\end{aligned}$$

Multiplying the charging energy E_{Charging} with the switching frequency F gives the transferred energy in Js^{-1} or in Whh^{-1} . The shuttled energy during the discharging phase of the capacitor ($D_1 \cdot T < t < T$) can be calculated by integrating the product of the discharge current as well as the discharging capacitor voltage over time, see Equation 3.17. The time constant τ is a function of the internal resistance of the charge-receiving cell[78].

$$E_{\text{Discharging}} = \int_{DT}^T \left[U_{\text{diff}} \cdot e^{-\frac{t}{\tau(R_{i,RE})}} + U_i \right] \cdot \left[\frac{-U_{\text{diff}}}{R_{\text{seq}(R_i,RE)}} \cdot e^{-\frac{t}{\tau(R_{i,RE})}} \right] dt \tag{3.17}$$

Since the duty cycle is set to 50 %, the integration boundaries may be set to 0 and DT , facilitating the calculation as per Equation 3.18 [78].

$$E_{\text{Discharging}} = C_{\text{bal}} \cdot U_{\text{diff}} \left[\left(\frac{U_{\text{diff}}}{2} \cdot e^{-\frac{2D}{\tau(R_{i,RE}) \cdot F}} + U_i \cdot e^{-\frac{D}{\tau(R_{i,RE}) \cdot F}} \right) - \left(\frac{U_{\text{diff}}}{2} + U_i \right) \right] \cdot F \quad [\text{Whh}^{-1}] \tag{3.18}$$

3.2.2 Inductance-based Balancing

Inductance-based balancing topology uses inductors as the main element for energy storage during transfer between cells. Common setups are depicted in Figure 3.12. This topology is less popular since it comes with higher hardware costs and often higher energy losses due to magnetisation losses. Further, inductors require more space on PCBs due to their bulky geometries and external capacitors required to filter high-frequency effects.

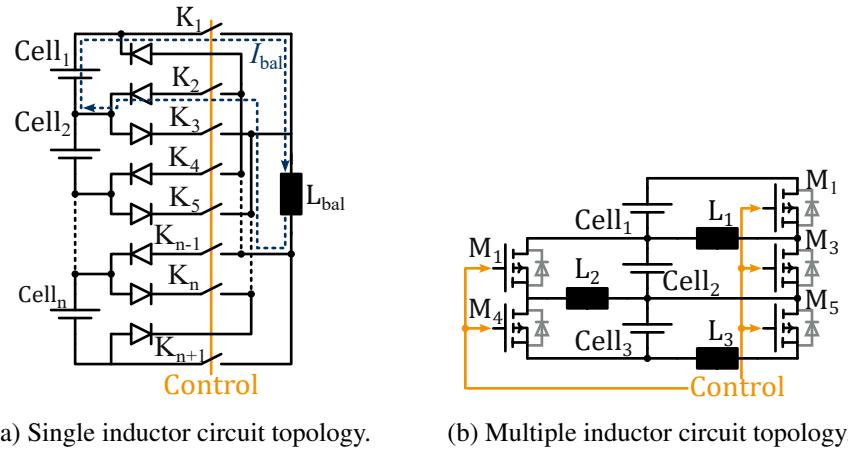


Figure 3.12: Inductance-based balancing topology [19].

Figure 3.12a displays the energy transfer from the higher charged $Cell_1$ to the inductor. According to the difference between the cell voltages, the inductor is magnetically charged or discharged by the switch control and the balancing energy is stored as a function of the inductance L of the inductor. During the discharge phase of the higher charged $Cell_1$, the switches S_1 and S_2 are closed and the voltage across the inductance L_{bal} starts rising with respect to the right-hand rule. Afterwards, the switches S_1 opens and S_2 as well as S_3 close. Either the lower charged $Cell_2$ is charged, or an additional capacitor is charged, as the energy inside the inductance can only be saved for a short period of time. The control of the switches is usually performed by PWM. A similar topology can also be implemented using several inductors as shown in Figure 3.12b, which allows for faster balancing. However, the balancing time increases fast with a rising number of battery cells [19].

3.2.3 Transformer-based Balancing

The single inductance as an energy storage element can be exchanged by a single or multi-winding transformer, where single-winding transformers are also referred to as switched transformers. Figure 3.13 shows the structure of a multi-winding transformer circuit for a battery pack with several cell stacks. The proposed structure by [79] further allows balancing between cells inside a stack, and enables energy transfer between cell stacks inside the battery pack using a boost converter.

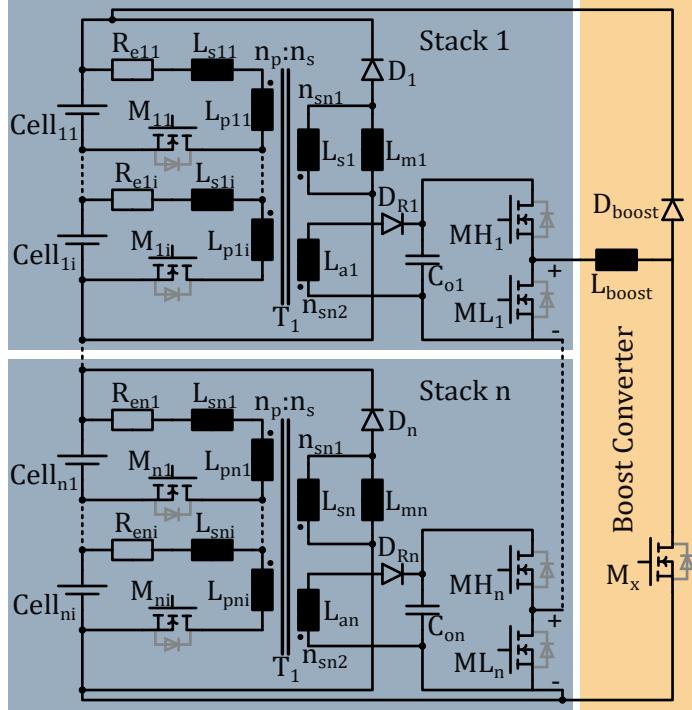


Figure 3.13: Topology of a modularized multi-winding transformer balancing circuit [79].

The cells are connected to the primary winding of the transformer T_n by the switches M_{ni} . R_{eni} is denoted as the ESR of the current path and L_{sni} is the leakage inductance of the circuit. The secondary side of the transformer is made up of two windings that transfer the magnetisation energy. In case that the voltage of one stack is higher than the average stack voltage, this stack can be discharged, and the magnetisation energy is transferred to the capacitor C_{on} by the winding n_{sn2} . The switch MH_n is then turned on and the stored energy inside the capacitor C_{on} is transferred back to the battery pack using the boost converter. This topology offers the advantage that the voltage balancing control inside the stacks is completely decoupled, and the degree of modularisation is high. The multi-winding transformer topology acts as a fly-back converter, allowing high balancing currents and short balancing times. Since the stacks are separated from each other, the PWM frequency can be adapted individually in accordance to the voltage differences of the cells inside the respective stack [79].

3.2.4 DC/DC Converter based Balancing

DC/DC-converter-based balancing control is implemented by half-bridge or whole bridge converters like Buck, Boost, Buck-Boost or Ćukconverters. The balancing energy is stored in inductors or transformers. DC/DC-converters allow for more precise balancing than the technologies mentioned above, with decent efficiency but at higher costs.

3.2.4.1 Ćuk-Converter

Ćuk-converters offer bidirectional energy transfer capabilities at reported high efficiencies [80]. Whilst the conventional Ćuk-converter circuit requires $(2n - 1)$ switches for n cells, various concepts have been proposed recently, using n switches and $(n + 1)$ inductors for a number of n cells. This concept results in fewer components and reduced energy loss compared to conventional circuits.

The principle of operation can be described in a simplified way by reducing the battery series to two cells as shown in Figure 3.14. During the first stage, the switch M_1 is turned on while the switch M_2 is turned off.

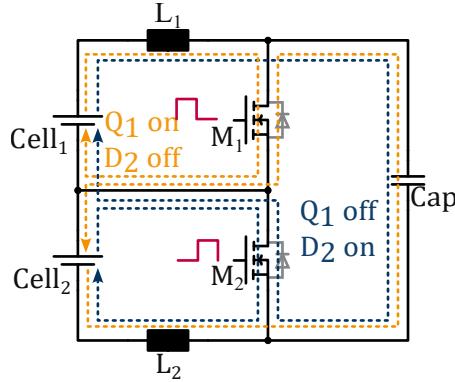


Figure 3.14: Reduced Ćuk-converter circuit for two cells [80].

The voltage equations can be written as

$$\begin{aligned} U_{\text{Cell}_1} &= L_1 \frac{di_{L_1}}{dt} \\ U_{\text{Cell}_2} &= -L_2 \frac{di_{L_2}}{dt} + U_{\text{Cell}_1} \end{aligned} \quad (3.19)$$

In the next stage, M_1 is turned off and the body diode of M_2 is conducting. The equivalent equation is given by

$$\begin{aligned} U_{\text{Cell}_1} &= L_1 \frac{di_{L_1}}{dt} + U_{\text{Cell}_1} \\ U_{\text{Cell}_2} &= -L_2 \frac{di_{L_2}}{dt} \end{aligned} \quad (3.20)$$

Applying the volt-second balance theory across the inductor L_1 as per Equation 3.21, where D is the duty cycle.

$$U_{\text{Cell}_1} \cdot DT + (U_{\text{Cell}_1} - U_{\text{Cap}}) \cdot (1 - D) \cdot T = 0 \quad (3.21)$$

Similarly, the volt-second balance can be applied across the inductor L_2 .

$$(-U_{\text{Cell}_2} + U_{\text{Cap}}) \cdot DT + (-U_{\text{Cell}_2}) \cdot (1 - D) \cdot T = 0 \quad (3.22)$$

The average inductor current can be obtained by Equation 3.23, where F_S is the switching frequency.

$$i_{L_1}(1 - D) \cdot F_S - i_{L_2}D F_S = 0 \quad (3.23)$$

The average inductor current can further be expressed by Equation 3.24.

$$\begin{aligned} i_{L_1} &= \left[\frac{1}{2} \left(\frac{U_{\text{Cell}_1}}{L_1} D^2 + \frac{-U_{\text{Cap}} + U_{\text{Cell}_1}}{L_1} (1-D)^2 \right) \right] \cdot F_S \\ i_{L_2} &= \left[\frac{1}{2} \left(\frac{U_{\text{Cap}} - U_{\text{Cell}_2}}{L_2} D^2 + \frac{-U_{\text{Cell}_2}}{L_2} (1-D)^2 \right) \right] \cdot F_S \end{aligned} \quad (3.24)$$

[80]

3.2.5 Performance and Feature Comparison

Table 3.1 summarises key performance points of various balancing topologies as reported in recent literature. The table motivates the rising popularity of capacitors as energy-

Table 3.1: Comparison of published performance data of selected balancing topologies [3], [19], [81]–[83].

Balancing topology		Balancing time	Balancing current	Balancing efficiency	System complexity	System volume	Total cost
Passive	Fixed Resistor	Medium	1 A	0 %	Low	Small	Low
	Zener Diode	Medium	0.8 A	0 %	Low	Small	Low
	Switched Resistor	Medium	1 A	0 %	Low	Small	Low
Capacitance-based	Single Switched Capacitor	Medium	2 A	83 %	Low	Low	Low
	Double-tiered capacitor	Short	2 A	83 %	Medium	Medium	Medium
Inductance-based	Switched Inductor	Medium	0.8 A	80 %	Medium	High	Medium
	Multiple inductors	Medium	5 A	85 %	High	High	High
Transformer-based	Switched transformer	Medium	0.25 A	70 %	High	High	Medium
	Multi-winding transformer	Short	4 A	90 %	High	High	High
Converter-based	Cuk	Medium	N/A	81.98 %	High	Medium	High
	Buck-Boost	Short	N/A	97.7 %	High	Medium	High
	Flyback	Short	N/A	94.19 %	Medium	High	Medium

storing elements in active balancing circuits due to their high efficiency and low implementation complexity. Further, capacitors require less space and volume on PCBs than inductors or transformers.

3.2.6 Control of Active Balancing

The switches in active balancing systems are usually controlled by PWM, which may output from a programmable IC or a specific ASICs for active balancing, e.g. the LTC3300-series [84] from *LINEAR TECHNOLOGY* using two-winding transformers. Microcontroller-based Master/Slave systems allow for more powerful control algorithms, which may shorten the balancing time and increase balancing efficiency by reducing the amount of charge being moved inside a battery stack [66]. Optimising control design is crucial for increasing balancing efficiency. Literature indicates that control optimisation can reduce balancing time and energy loss during the process by 9.59 % and 19.5 %, respectively [70]. As shown in [66], balancing speed can be significantly enhanced by hardware capable of balancing arbitrary cells, though this requires more complex hardware configurations. Balancing only adjacent cells, C_n and C_{n+1} , creates imbalances with their neighbouring cells, C_{n-1} and C_{n+2} , necessitating a greater number of balancing iterations to equalise the battery stack. It is possible to further reduce the maximum offset of a single cell to the average stack voltage by charging or discharging arbitrary cells only

until the first cell reaches a predefined target voltage, which can be the average stack voltage or a defined cut-off voltage during charging or discharging stages of the ESS. An example control algorithm to achieve this is demonstrated in Figure 3.16 and Figure 3.17 as simulated in [66] and further described in chapter 4.

3.2.6.1 Controller

The full literature source published as part of the present thesis can be found in the appendix. The simulations in [66] were done using the model depicted in Figure 3.15 implemented in *PLECS* and *SIMULINK*.

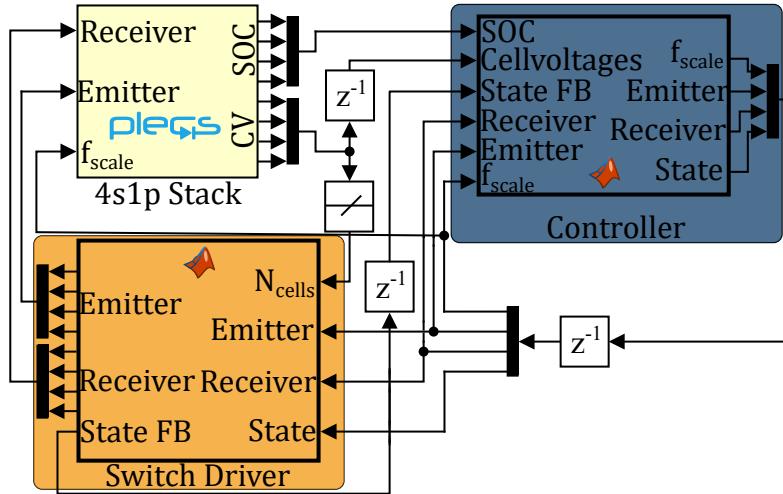


Figure 3.15: Simulink Model showcasing cell identifier (blue), switch driver (orange) and 4s1p-battery stack implemented using *PLECS BLOCKSET* [66]

”Triggered by the initialisation state of the algorithm of the switch driver as shown in Figure 3.17, the controller starts by reading out the cell voltages and calculating the target cell voltage. Typically, this target voltage can be the average stack voltage in most cases or a predefined voltage, e.g. the cut-off voltage if the ESS is in charging or discharging phase. The cell with the highest positive deviation to the target voltage is designated as the emitter cell, the receiver cell is selected based on the highest negative offset to the target voltage. The algorithm concludes if the highest absolute offset is below a predefined threshold, meaning that all cell voltages are within a tolerated range. Else the switching frequency for the PWM generator is calculated concerning the state of charge of the two cells as follows, whilst the duty cycle is always set to 50 %.

$$f_{sw} = \frac{1}{T_{charge} + T_{discharge}} \quad (3.25)$$

Where T_{charge} marks the required time to charge the switched capacitor C_{bal} that can be calculated by the generally valid time constant $\tau = R_{tot} \cdot C_{bal}$,

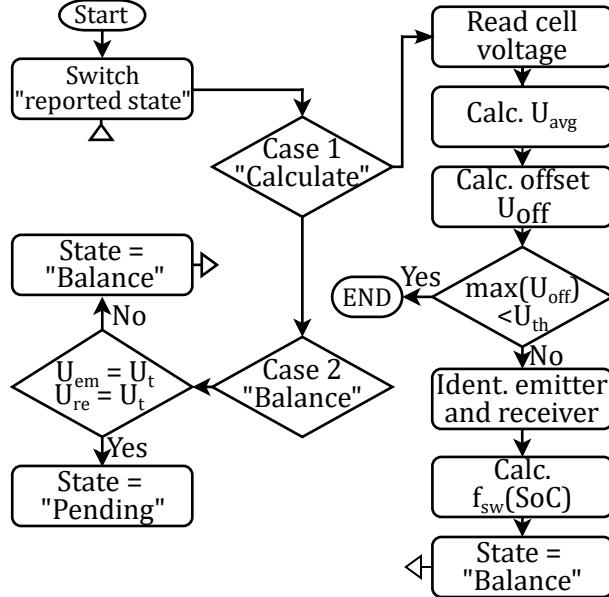


Figure 3.16: Control algorithm of the blue-marked controller block implemented as *MATLAB* function [66]

assuming that $T_{\text{charge}} = 5 \cdot \tau$ and R_{tot} being the total series resistance of the circuit including $R_{\text{ds},\text{on}}$ of the FETs and the conductor resistance.

$$T_{\text{charge}} = 5 \cdot R_{\text{tot}}(SoC_{\text{emitter}}) \cdot C_{\text{bal}} \quad (3.26)$$

The capacitor voltage $u(t)$ of a capacitor with the capacitance C_{bal} , an initial voltage U_0 and a circuit resistance of R_{tot} during discharge is given by

$$u(t) = U_0 \cdot e^{\frac{-t}{R_{\text{tot}} \cdot C_{\text{bal}}}} \quad (3.27)$$

Hence, the time required to discharge the capacitor is obtained from Equation 3.28, where the initial voltage U_0 is determined by the voltage of the emitter cell and the voltage at the time t is given by the voltage of the receiver cell at the start of the discharge process.

$$T_{\text{discharge}} = R_{\text{tot}} \cdot C_{\text{bal}} \cdot \ln \left(\frac{U_{\text{emitter},t_0}}{U_{\text{receiver},t_0}} \right) \quad (3.28)$$

According to Equation 3.26 and Equation 3.28, the capacitance of the balancing capacitor can be freely chosen, however high capacitance will result in high charging currents as stated by Equation 3.29. With a capacitance of $C_{\text{bal}} = 1 \text{ mF}$, the switching frequency is $f_{\text{sw}} = 1.113 \text{ kHz}$. During simulations, the balancing capacitor C_{bal} is initially precharged to a voltage close to the average stack voltage to avoid high peak currents on initial charge.

$$i(t) = C \cdot \frac{\partial U(t)}{\partial t} \quad (3.29)$$

After identification, the flag to start balancing is sent to the switch driver. The switch driver confirms entering the balancing state by sending the flag back to the controller which then also switches to case 2 of the algorithm in Figure 3.16. The controller remains in the balancing state by further sending the balancing flag until either the emitter cell or the receiver cell reaches the target voltage. In that case, the flag “Pending” is sent to the switch driver, causing it to keep on balancing until the cell indices of the new emitter and receiver cells are received.

3.2.6.2 Switch Driver

The cell indices as well as the flag to enter the balancing state are received by the orange-marked switch driver in Figure 3.15 from the controller. The switch driver sets the output vectors of the emitter circuit and receiver circuit by setting the elements with the respective indices to 1 whilst setting the other vector elements to 0. The received state from the controller is then confirmed by sending the flag back to the controller. As seen in Figure 3.17, the initial state of the switch driver is “Startup”, where all circuits are opened, meaning that all elements of the output vectors are 0. The identification of the emitter and receiver cells is then triggered by reporting the state “Calculate” to the controller.

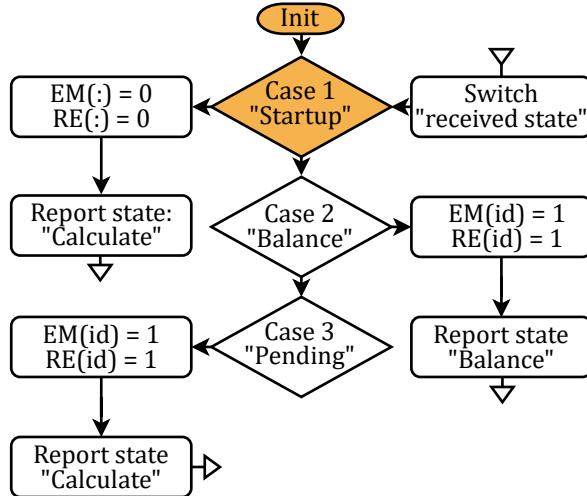


Figure 3.17: Control algorithm of the orange-marked switch driver block implemented as *MATLAB* function.

3.2.6.3 Energy Storage Block

The energy storage block is implemented as a subsystem within *SIMULINK* using *PLECS BLOCKSET*. It consists of 4 series-connected cells using accurate battery models proposed in [85]. As the used battery model offers the configuration of cell systems within the same model, each model is configured as a 1s1p-battery. The electric battery model consists of a

capacitor $C_{Capacity}$, connected in parallel to a self-discharge resistor and a current-controlled current source. With respect to the SoC of $C_{Capacity}$, an open-circuit voltage U_{OC} is generated. The transient voltage response is modelled by a series of one resistor R_{series} and two RC parallel networks $R_{Transient,S}$, $C_{Transient,S}$ and $R_{Transient,L}$, $C_{Transient,L}$. R_{series} describes the instantaneous voltage drop of the step response. $R_{Transient,S}$, $C_{Transient,S}$ and $R_{Transient,L}$, $C_{Transient,L}$ model the short-term and long-term constants respectively of the step response [85]. The cell model provides real-time SOC and U_{OC} measurement. As demonstrated in Figure 3.18, the bidirectional

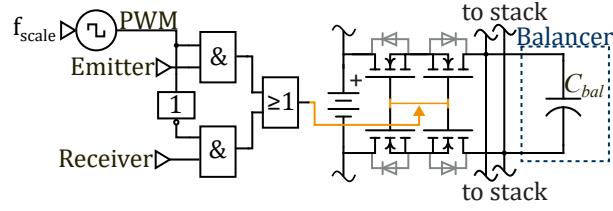


Figure 3.18: Energy storage block including balancer capacitor hardware and control logic for one cell [66]

switches are implemented using two mirrored N-Channel field-effect transistors (FET). Current may pass either through the N-Channel if a positive voltage is applied at the gate and through the body diode of the reversed FET connected in series if a negative voltage is applied. The current direction and hence the actual current path inside the FET depends on the applied polarity on the bidirectional switch and thus on the current state of operation of the balancing circuit. The FETs conduct only if the signal from the switch driver and the PWM-signal are on logical *HIGH*. The PWM signal is inverted between the emitter and receiver circuits to avoid setting two circuits into conductive mode simultaneously.” [66]

The balancer module is implemented using a single switched capacitor.

4 Simulation

During the following simulations, two cells are considered as “balanced” if their voltage difference is equal to or less than 5 mV.

4.1 Switched Resistor Balancing

As switched resistor topologies are among the most popular balancing topologies used in EVs, the balancing characteristics are analysed per simulation.

4.1.1 Simulation Setup

The balancing circuit, including the battery cells, the switches and the balancing resistors, is built in *PLECS BLOCKSET* following the basic model as shown in Figure 3.4 but with additional features as per Figure 4.1. The control of the switches is performed in *MATLAB* and *SIMULINK*. The cell stack is implemented by four series-connected cells

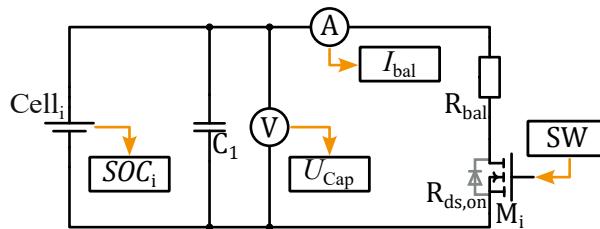


Figure 4.1: Switched resistor simulation circuit setup.

using the second-order battery model described in [85]. The cell model returns its State of Charge. The Cell Voltage is measured across the capacitor C_1 , which is precharged to the cell voltage prior to the start of the simulation. Further, the discharge current across the resistor R_1 and the MOSFET M_1 is measured. The voltage across each capacitor connected in parallel to each cell is passed to the output vector of the *PLECS* block. The minimum voltage is measured and set as the target voltage to which every cell shall be discharged. According to Figure 4.2, the minimum voltage is passed to a subtraction block where the difference between the voltage of the current cell and the voltage of the lowest charged cell is calculated and passed to the compare function. The compare function takes the voltage difference of each cell to the target voltage as well as a given threshold (5 mV) as an input and returns an output flag which is *HIGH* in case that the voltage difference is above the threshold and *LOW* for the case that the voltage difference is equal or smaller than the given threshold to the switch-control vector. The

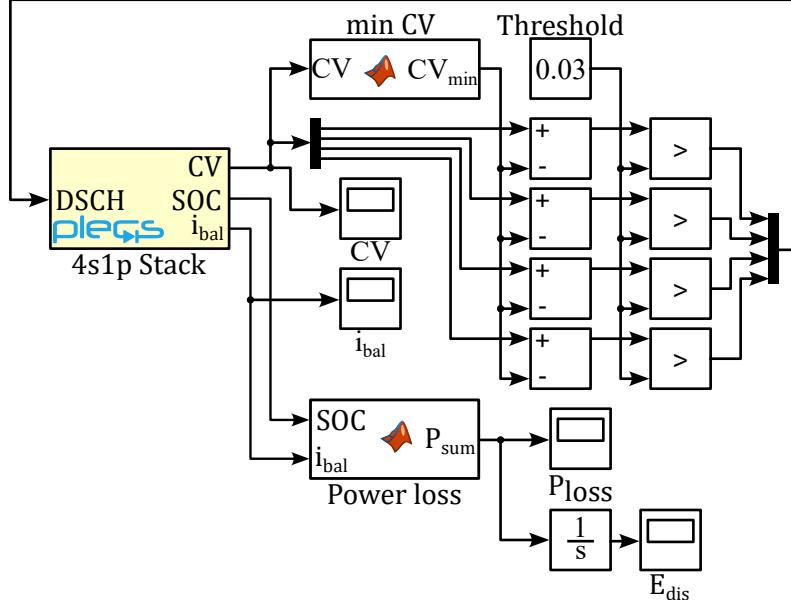


Figure 4.2: Switched resistor simulation control setup in *SIMULINK*.

switch-control vector is returned to the *PLECS* model and acts as the gate signal for each MOSFET of the circuit. The balancing current as well as the State of Charge is passed to the power loss calculation function, which returns the instant power loss, which is further integrated with respect to time to obtain the energy dissipated during the balancing process. The power loss is calculated as the sum of the power loss of each balanced cell as a function of its SOC using the total resistance R_{tot} and the balancing current $i_{\text{bal}}(t)$ of each circuit as per Equation 4.1. $R_{\text{ds},\text{on}}$ is the resistance of the MOSFET in conduction mode, R_{bal} is the balancing resistor, R_{contact} is the metallic contact resistance of the cell and R_i is the constant part of the cells internal resistance. The total internal resistance of the cell is the sum of the constant resistance R_i as well as the short-term and long-term transient resistance $R_{\text{Transient,S}}(\text{SOC}_i)$ and $R_{\text{Transient,L}}(\text{SOC}_i)$ [85]. Since the excessive charge in the higher charged cells is dissipated during balancing, no efficiency calculations are required.

$$P_{\text{loss},i}(t) = i_{\text{bal}}^2(t) \cdot \left(R_{\text{ds},\text{on}} + R_{\text{bal}} + R_{\text{contact}} + R_i + \underbrace{0.3208^{-29.14 \cdot \text{SOC}_i(t)} + 0.04669}_{R_{\text{Transient,S}}(\text{SOC}_i(t))} + \underbrace{6.603 \cdot e^{-155.2 \cdot \text{SOC}_i(t)} + 0.04984}_{R_{\text{Transient,L}}(\text{SOC}_i(t))} \right) \quad (4.1)$$

The dissipated energy is calculated as per Equation 4.2.

$$E_{\text{dis}} = \sum_{i=1}^n \int_{t_{\text{start}}}^{t_{\text{end}}} P_{\text{loss},i}(t) dt \quad (4.2)$$

4.1.2 Simulation Results - Homogenous Cell Capacity

The first simulation assumes that every battery cell has the same SOH and therefore the same capacity, but each cell has a different SOC as noted in Table 4.1. Note that the cell capacity is selected to be very small to reduce the simulation runtime of the *SIMULINK* model. The principle of operation remains the same and is scalable to higher energy capacities.

Table 4.1: Simulation setup, Switched Resistor, homogenous cell capacity.

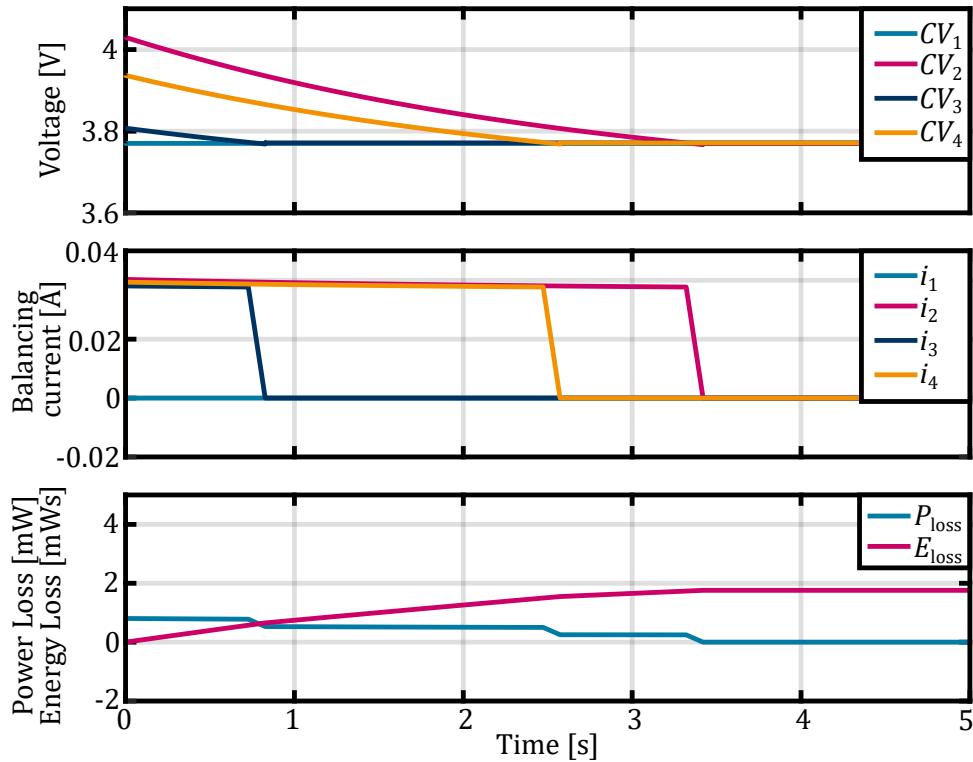
Parameter	Value	Unit
$\text{SOC}(Cell_1)$	39	%
$\text{SOC}(Cell_2)$	92	%
$\text{SOC}(Cell_3)$	52	%
$\text{SOC}(Cell_4)$	79	%
Capacity $Cell_1$	6.94×10^{-5}	Ah
Capacity $Cell_2$	6.94×10^{-5}	Ah
Capacity $Cell_3$	6.94×10^{-5}	Ah
Capacity $Cell_4$	6.94×10^{-5}	Ah
C_1	1×10^{-8}	F
R_{bal}	100	Ω
$R_{\text{ds,}on}$	1×10^{-3}	Ω
R_{contact}	1×10^{-3}	Ω
R_i	7.456×10^{-2}	Ω
$V_{\text{threshold}}$	5 mV	mV

The upper graph in Figure 4.3 shows the cell voltage shows the cell voltage of each of the four series-connected cells. The middle graph shows the balancing current passing each parallel shunt resistor of the respective cell. The lower graph displays the total power loss during the balancing process as per Equation 4.1 with the blue line and the integrated power loss resulting in the total dissipated energy during the process as the pink line.

The simulation results in Figure 4.3 demonstrate the principle of operation of dissipative balancing topologies. The voltage of the lowest charged cell remains unchanged during the whole process. The higher-charged cells are discharged continuously. The balancing topology allows all cells to be discharged simultaneously, which speeds up the balancing process.

The balancing current i_{bal} is nearly constant at around 40 mA across the whole balancing time and only drops once the cell voltage reaches the voltage of the lowest charged cell. It can be observed that the cell voltages drop slightly below the voltage of the lowest charged cell until discharging is stopped, and then reach OCV in steady state, which is a little higher than the voltage under load. The instant power loss is the highest when all three cells are discharged and drops each time a cell reaches the desired voltage. The energy loss is the integrated power loss over time according to Equation 4.2.

The elapsed time until each cell reaches the voltage margin to be considered balanced is 3.4198 s.

Figure 4.3: Switched Resistor simulation control setup in *SIMULINK*.

4.1.3 Simulation Results - Inhomogeneous Cell Capacity

During the second simulation, it is assumed that the cells have a different initial capacity according to Table 4.2; the other simulation parameters, especially the SOC, stay consistent with Table 4.1.

Table 4.2: Simulation setup, Switched resistor, inhomogeneous cell capacity.

Parameter	Value	Unit
Capacity <i>Cell</i> ₁	7.94×10^{-5}	Ah
Capacity <i>Cell</i> ₂	5.94×10^{-5}	Ah
Capacity <i>Cell</i> ₃	6.94×10^{-5}	Ah
Capacity <i>Cell</i> ₄	4.94×10^{-5}	Ah

The balancing time during this simulation is 2.9188 s. It shows that the differences in capacity between the cells do not imply a longer balancing time. In dissipative balancing, the balancing time benefits from cells with a lower capacity, since less energy needs to be dissipated before reaching the targeted voltage.

4.2 Switched Capacitor Balancing

4.2.1 Simulation Setup

For the switched capacitor simulations, the same *SIMULINK* model as developed in [66], see Figure 3.15, is used. The energy storage block is implemented as a *4s1p*-cell circuit, and the control logic as described in Figure 3.18 using *PLECS BLOCKSET*. The *PLECS* circuit returns the voltage of each cell inside the circuit as well as their SOC and the balancing current i_{bal} . The cell voltages and the SOC are passed to the algorithm described in Figure 3.16, which identifies the stack's highest and lowest charged cell and the average stack voltage. The highest charged cell, which unarguably has the highest positive offset to the average stack voltage, is defined as the emitter cell, meaning that it will emit charge during the balancing process to the balancing capacitor. The lowest charged cell is the receiver cell, which will receive charge from the balancing grid during the balancing phase. In case that no two cells have a voltage difference higher than the predefined threshold (5 mV), a stop-flag is set and the simulation is terminated. Since the used control algorithm as described in [66] measures the cell voltages between two balancing cycles and hence performs a more accurate measurement of the Open Circuit Voltage, a more precise balancing is possible allowing voltage difference between two cells to be much smaller before two cells are considered as balanced. A resistance of 0.1Ω is integrated in the circuit to simulate conductor and other parasitic resistances and limit the capacitor charging current.

Depending on the SOC of the emitter and receiver cell, the optimal switching frequency f_{sw} is calculated according to Equation 3.25. Since the PWM generator in *PLECS* works with a carrier frequency, the control algorithm does not output the actual switching frequency but a scaling factor f_{scale} for the carrier frequency according to Equation 4.3.

$$f_{\text{scale}} = \frac{f_{\text{sw}}}{f_{\text{carrier}}} \quad (4.3)$$

The duty cycle is set to 0.5 for the entire balancing phase.

The balancing efficiency describes the energy dissipated during the balancing process and can be expressed by the power efficiency or the energy efficiency. The power efficiency η_{power} describes the ratio between the total power P_{total} of the balancing process and the useful power P_{balance} which is actually used to balance the cells. The useful power is the absolute difference between the total power P_{total} and the dissipation power P_{loss} . Hence, the power efficiency is given by Equation 4.4

$$\eta_{\text{power}}(t) = \frac{P_{\text{balance}}(t)}{P_{\text{total}}(t)} = \frac{|P_{\text{total}}(t) - P_{\text{loss}}(t)|}{P_{\text{total}}(t)} = 1 - \frac{P_{\text{loss}}(t)}{P_{\text{total}}(t)} \quad (4.4)$$

As per the general definition, the power loss is expressed as the product of the total circuit resistance R_{tot} and the squared balancing current $i_{\text{bal}}(t)^2$. The total instant power $P_{\text{total}}(t)$ is the product of the balancing current and the voltage of the balancing capacitor $u_{\text{Cap}}(t)$. Hence, Equation 4.4 can be written as in Equation 4.5.

$$\begin{aligned} \eta_{\text{power}}(t) &= 1 - \left| \frac{R_{\text{tot}} \cdot i_{\text{bal}}(t)^2}{u_{\text{Cap}}(t) \cdot i_{\text{bal}}(t)} \right| \cdot 100 \% \\ \eta_{\text{power}}(t) &= 1 - \left| \frac{R_{\text{tot}} \cdot i_{\text{bal}}(t)}{u_{\text{Cap}}(t)} \right| \cdot 100 \% \end{aligned} \quad (4.5)$$

The energy efficiency is defined as the ratio between the energy that the cell stack stores after the balancing process has ended and the energy initially stored inside the cells, see Equation 4.6

$$\eta_{\text{energy}} = \frac{E_{\text{Output}}}{E_{\text{Init}}} \quad (4.6)$$

The energy inside the stack is calculated as the sum of the energies stored in each cell at the beginning and end of the balancing process. Hence, Equation 4.6 can be extended as per Equation 4.7. The energy stored inside each cell is calculated as the product of the cell capacity E_{Cell} and the cell voltage U_{Cell} .

$$\eta_{\text{energy}} = \frac{\sum_{i=1}^n U_{\text{Cell}_i, \text{Output}} \cdot E_{\text{Cell}_i}}{\sum_{i=1}^n U_{\text{Cell}_i, \text{Init}} \cdot E_{\text{Cell}_i}} \quad (4.7)$$

4.2.2 Simulation Results - Homogeneous Cell Capacity

The balancing procedure with the control setup described in [66] is set up with the parameters noted in Table 4.3, similar to the simulations made above.

Table 4.3: Simulation Setup, Switched Capacitor, homogeneous cell capacity

Parameter	Value	Unit
SOC(Cell_1)	39	%
SOC(Cell_2)	92	%
SOC(Cell_3)	52	%
SOC(Cell_4)	79	%
Capacity Cell_1	6.94×10^{-5}	Ah
Capacity Cell_2	6.94×10^{-5}	Ah
Capacity Cell_3	6.94×10^{-5}	Ah
Capacity Cell_4	6.94×10^{-5}	Ah
Balancing capacity C_{bal}	1×10^{-4}	F
C_1	1×10^{-8}	F
R_{bal}	100	Ω
$R_{\text{ds, on}}$	1×10^{-3}	Ω
R_{contact}	1×10^{-3}	Ω
R_i	7.456×10^{-2}	Ω
$V_{\text{threshold}}$	5	mV

The cell voltages during balancing are depicted in Figure 4.4. It can be observed how the algorithm described in Figure 3.16 [66] selects the two cells with the highest positive and negative voltage offset to the target voltage and balances them until the first cell reaches the target voltage. This may either be the higher-charged cell or the lower-charged cell. Once a cell reaches the target voltage, two new cells are selected to be balanced according to their offset to the target voltage. In the present case, the target voltage is the average stack voltage, however, it may also be another voltage in real-life

applications, e.g. the charging threshold when the ESS is being charged by an external charging device.

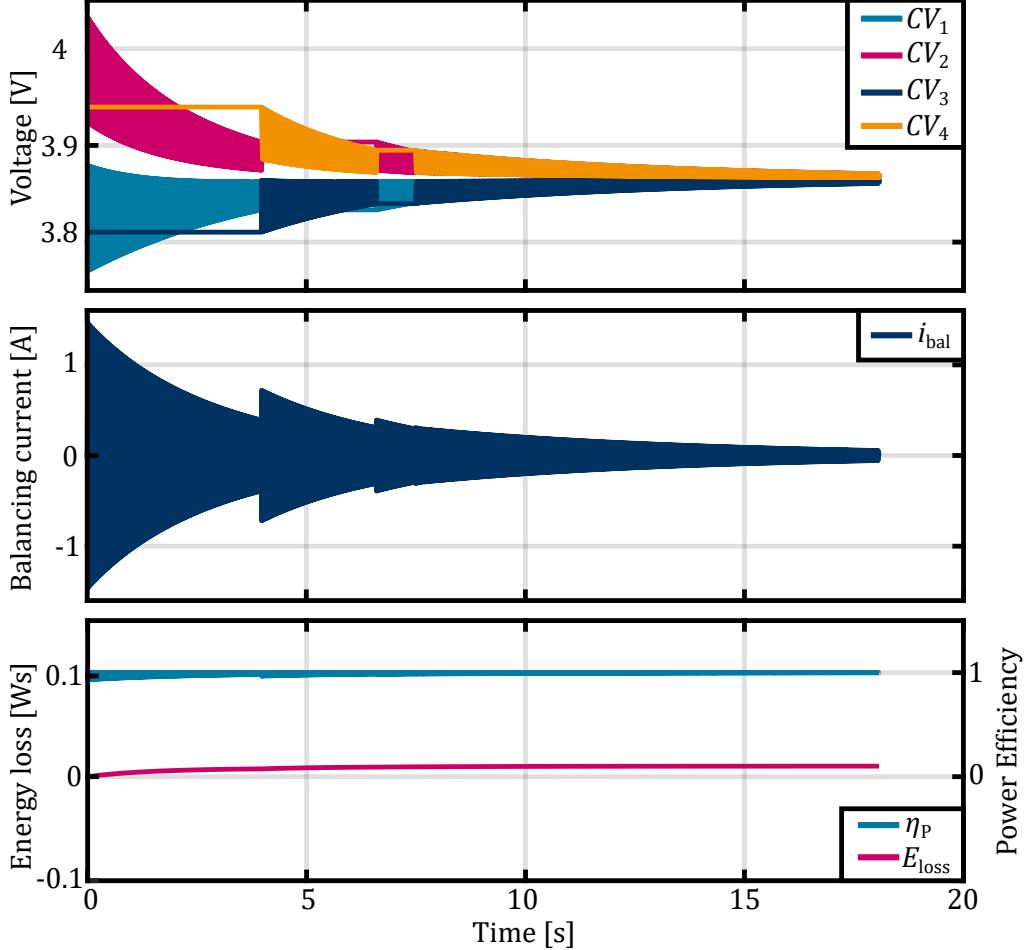


Figure 4.4: Cell voltages, Balancing Current i_{bal} , Power Efficiency η_P and Energy Loss E_{Loss} during balancing using the control algorithm described in [66] and homogenous cell capacities.

The waveform of the battery cells and the balancing capacitor is described in Figure 4.5. When the PWM signal switches to a logical high ($0 < t < \frac{T}{2}$), the higher charged cell (CV_1) starts charging the balancing capacitor. This induces a voltage drop in the charge-emitting cell and a peak amplitude in the balancing current i_{ba} . The capacitor voltage U_{cap} reaches a steady state and matches the voltage CV_1 of the emitting cell 1. During the timespan $\frac{T}{2} < t < T$, the PWM signal drops to a logical *LOW* and the balancing capacitor is discharged by charging cell 2. This leads to a temporary rise of the voltage CV_2 and a drop of the capacitor voltage U_{cap} . Both voltages then reach a steady state, and the capacitor voltage U_{cap} matches the voltage of the receiver cell CV_2 . Figure 4.4 shows that the switching frequency may be higher as the voltages find themselves in a steady state for the majority of each half-period.

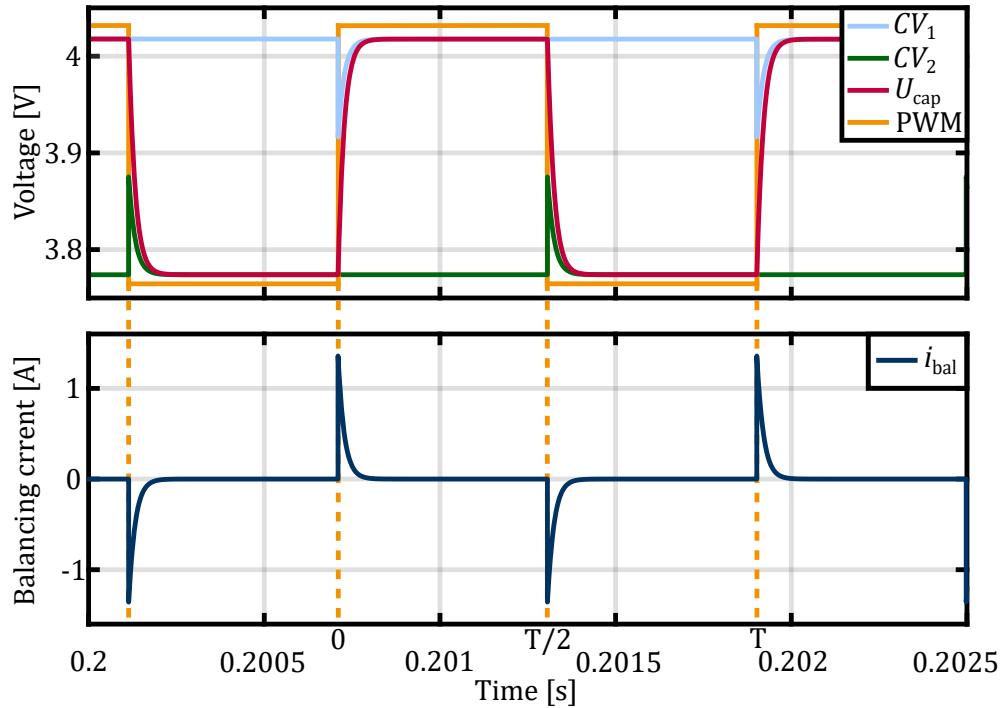


Figure 4.5: Voltage waveforms with $Cell_1$ under discharge and $Cell_2$ under charge.

4.2.3 Simulation Results - Inhomogeneous Cell Capacity

The setup is equal to the settings mentioned in Table 4.3 but with different cell capacities according to Table 4.4.

Table 4.4: Simulation setup, Switched Capacitor, inhomogeneous cell capacity.

Parameter	Value	Unit
Capacity $Cell_1$	8.94×10^{-5}	Ah
Capacity $Cell_2$	5.94×10^{-5}	Ah
Capacity $Cell_3$	7.94×10^{-5}	Ah
Capacity $Cell_4$	3.94×10^{-5}	Ah

Figure 4.6 shows that a variation of the cell capacity inside the same stack does not affect the balancing speed or efficiency in a significant way. Similar to balancing with dissipative technologies, voltage equalisation is faster the less energy is stored inside the battery stack.

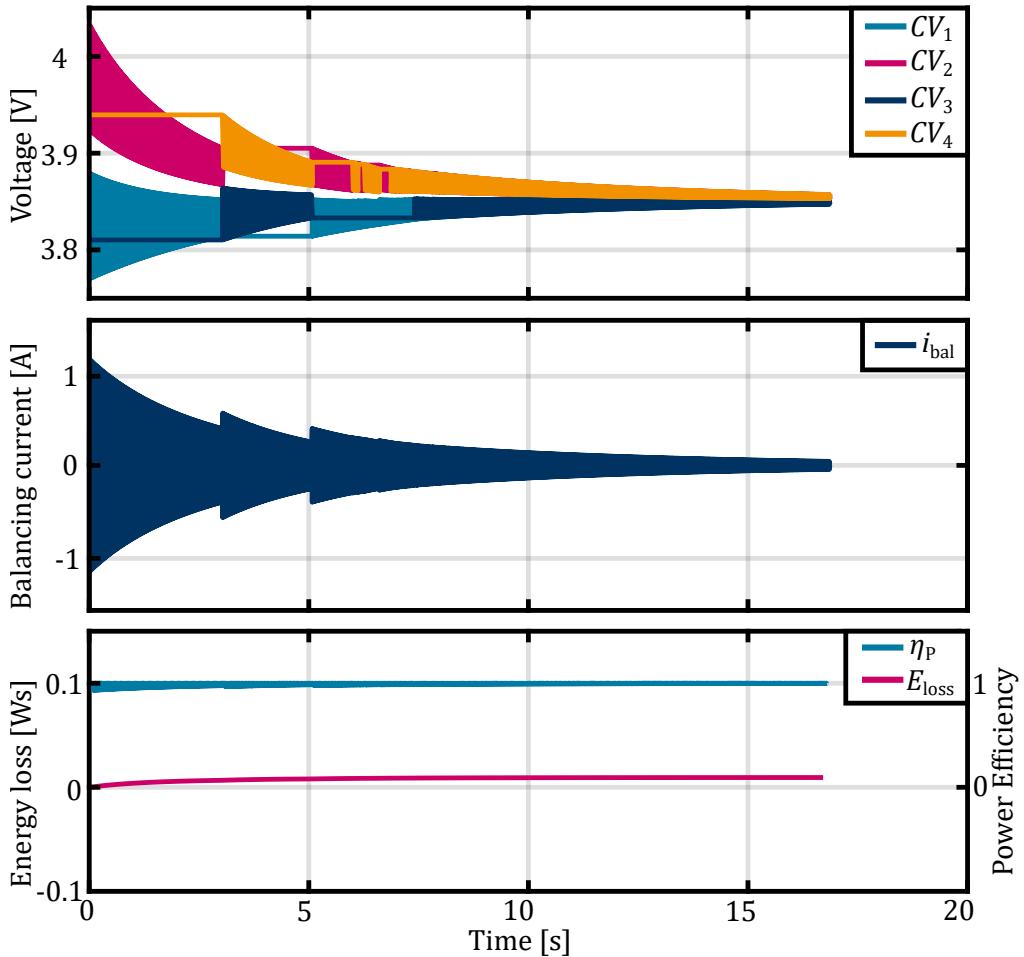


Figure 4.6: Cell voltages, Balancing Current i_{bal} , Power Efficiency η_P and Energy Loss E_{Loss} during balancing using the control algorithm described in [66] and inhomogeneous cell capacities.

Table 4.5: Balancing time and efficiency comparison between Switched Resistor and Switched Capacitor voltage equalisation in a 4s1p-stack.

Balancing Topology	Results						
	Homogenous Cell Capacity			Inhomogeneous Cell Capacity			Power Efficiency
	Balancing Time	Energy Efficiency	Power Efficiency	Balancing Time	Energy Efficiency	Power Efficiency	
Switched Resistor	3.4189 s	97.0303 %	n/a	9.9188 s	97.0181 %	n/a	
Switched Capacitor	18.045 s	99.4200 %	99.9300 %	16.865 s	99.4175 s	99.9305 s	

4.2.4 Balancing Capacity and Switching Frequency Effects

In the following section, simulations to analyse the effect of the balancing capacitance and the switching frequency on the balancing time are done. The balancing time and efficiency are two opposing factors since higher balancing currents result in a faster balancing time. Still, the ohmic losses increase with the square of the balancing current. Table 4.6 shows the simulation results of the simulation depicted in Figure 3.15 and described in subsection 4.2.1 with different balancing capacities. During the simulations, each cell has a capacity of 6.94×10^{-5} A h and the same SOC as in the simulations above. The switching frequency is dynamically adapted to the SOC of the cells according to [66] and is usually around 1 kHz.

Table 4.6: Balancing capacity effects on balancing time and efficiency during simulated voltage equalisation.

Balancing Capacity	Results		
	Energy Efficiency	Power Efficiency	Balancing Time
1×10^{-6} F	n/a	n/a	< 60 s
1×10^{-5} F	n/a	n/a	< 60 s
1×10^{-4} F	99.42 %	99.93 %	18.045 s
1×10^{-3} F	99.4203 %	99.5253 %	1.95 s
1×10^{-2} F	99.4015 %	99.2752 %	1.142 s
1×10^{-1} F	99.3559 %	99.2819 %	1.142 s
1 F	98.8821 %	99.3091 %	1.187 s
10 F	99.1336 %	99.2568 %	1.11 s
100 F	99.8881 %	99.3613 %	1.366 s

The simulation results in Table 4.6 demonstrate that the time it takes to balance all cells dramatically depends on the used balancing capacity. If the balancing capacity is too small, only small amounts of energy can be shuttled during each balancing cycle. However, higher capacitance can only speed up the process to a certain amount, as capacitors with a high capacitance take more time to charge and therefore can only operate under lower switching frequencies. The mathematical optimisation of the balancing capacitance and the switching frequency is subject to future work and is not included in the present thesis.

4.3 Switching Unit

The bidirectional switch shown in Figure 3.18 is an essential part of the whole implementation concept of balancing arbitrary cells with a single switched capacitor. In the simulations above, the switches were simplified and went into conduction mode when they received a logical *HIGH* on their gate pin. The switching unit should be implemented as a stand-alone unit to enable or disable the connection between a battery cell without requiring an external power supply. This requires P-Channel MOSFETs on the

positive side and N-Channel MOSFETs on the negative side of the cell or the balancing capacitor, respectively. The switching unit's operation principle is depicted in Figure 4.7.

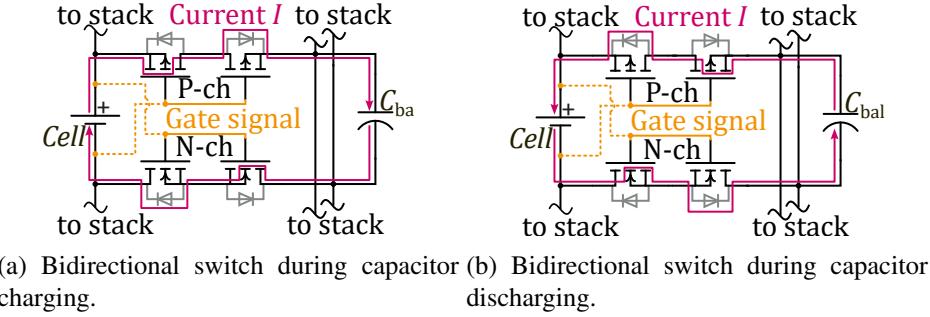


Figure 4.7: Bidirectional switching unit with gate voltages supplied by the battery cell.

As shown in Figure 4.7, current can flow in both directions by passing either through the N-or P-Channel respectively or by flowing through the body diode of the MOSFET. The high side of the circuit, connecting the positive pole of the battery cell with the anode of the balancing capacitor, is made up of two P-Channel MOSFETs, which are mirrored along the vertical axis in reference to each other. This way, both drain pins of the MOSFETs are connected directly, whereas the source pin of the left-side MOSFET is connected to the positive pole of the battery cell. The source-pin of the right MOSFET is connected to the anode of the balancing capacitor C_{bal} . In non-conducting mode, the gate potential matches the source potential of the left MOSFET, resulting in the gate-source voltage to be equal to 0V. In conducting mode, the gate is connected to the negative pole of the battery cell, resulting in a negative gate-source voltage U_{gs} , so that $U_{gs} = -U_{Cell}$. This opens the P-Channel and current can flow. As per Figure 4.8, current

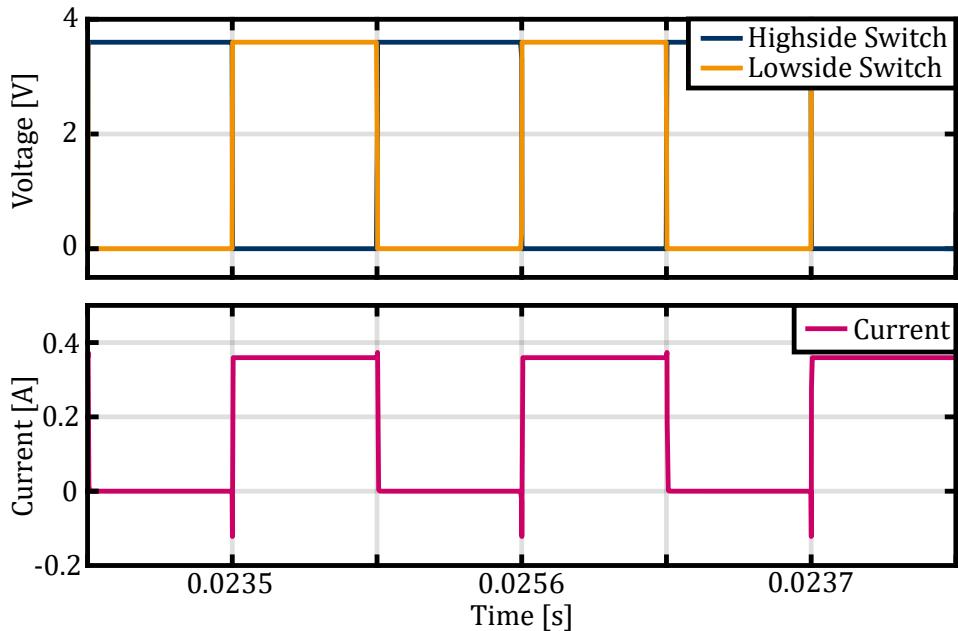


Figure 4.8: Gate signal waveform and Drain current of the bidirectional switch.

can only flow if the gate voltages are complementary to each other. This implies that the potential of the gate-source voltage of the low-side N-Channel MOSFETs is positive if the gate-source voltage of the high-side switch is negative. The positive gate-source voltage is achieved by applying the potential of the positive pole of the battery cell to the gates of the N-Channel MOSFET, meaning that $U_{gs} = U_{Cell}$. The simulation results of the simulated switching unit in *LTspice* are depicted in Figure 4.8. The simulation works for the case that the battery cell is on the right or the left side of the switching unit, meaning that current can flow in both directions.

5 Design Requirements and Concept Development

5.1 Design Requirements

Following the analysis in the chapters above, the design requirements mentioned below for the balancing system implementation can be established. Since the analysis performed in chapter 3 and chapter 4 demonstrated good balancing properties and easy, cost-effective implementation of single switched capacitor systems, this will be the considered balancing method for the following PCB development.

- Arbitrary cell balancing for Li-Ion batteries
- Current flow from and to the cell through bidirectional semiconductor switches
- Interchangeable Balancing Energy Storing Element
- Galvanic isolation between HVS and LVS
- LVS supplied by HVS
- Individual Cell Voltage measurement
- Cell Temperature measurement
- Current measurement
- Fuse over-current protection
- Circuit Breaker over-current protection
- Suitable for a 16s1p battery pack with a nominal voltage of 48 V
- Nominal power of 1.5 kW with a peak power of 130 % of the nominal power
- CAN-interface

The ability to balance arbitrary cells is the most crucial criterion for the present design, since the literature presented in chapter 3 has demonstrated much higher balancing speeds for this topology. This requirement demands bidirectional switches as presented in Figure 4.7. Since further investigations on the storage element of the balancing energy are planned, it should be interchangeable. To meet this requirement, the balancing energy storing element is soldered onto a second PCB, which can be stacked onto the main PCB using pin headers. The fourth design criterion is required to meet safety standards, which implies that the HVS is galvanically isolated from the LVS. Even if the present system only operates on a nominal voltage of 48 V, that design criterion is still essential to keep the system scalable.

5.2 Concept Development

5.2.1 Basic Implementation Concept

The concept of the Battery Management System (BMS) is depicted in Figure 5.1. Each cell's positive and negative pole is connected to a bidirectional switching unit. The switching unit provides a connection to the balancing energy storage element. The cell voltage and the cell temperature are measured on each cell. A fuse and a circuit breaker protect the battery pack against overcurrent events. This should reduce maintenance costs as the circuit breaker can open the circuit before the fuse would trigger, hence needing to be replaced.

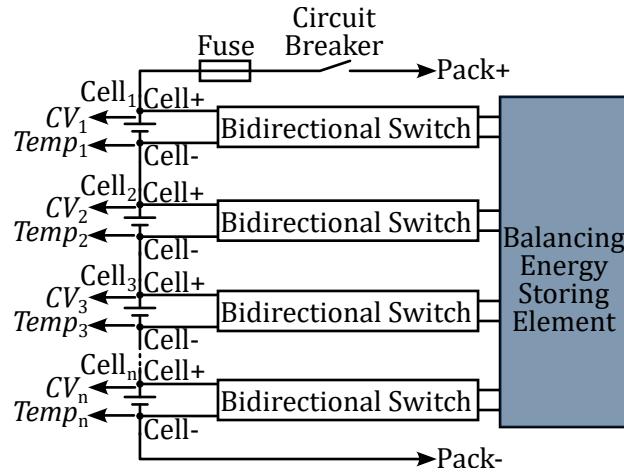


Figure 5.1: Basic concept of the BMS. The positive and negative pole of each cell is connected to a bidirectional switching unit, enabling charge transfer to the balancing energy storing element.

5.2.2 Concept Elaboration

The basic concept described in subsection 5.2.1 is further elaborated as depicted in Figure 5.2 to allow the selection of components at a later stage. The positive and negative poles of the 48 V battery stack are connected to the BMS PCB by the *Connector Stack+* as well as the *Connector Stack-*. Both connectors are part of the orange-coloured High Current Path (HCP) and must be rated for high currents, but at least for the highest theoretical short-circuit current as calculated in 5.3.6. The HCP can be opened either by the fuse or the high-side circuit breaker, which can be a high-current relay or a semiconductor device. The current is monitored by measuring the voltage drop across the shunt resistor R_{Shunt} . The High Current Path (HCP) is connected to the VSS-potential by a 0Ω resistance. The VSS-potential is the reference potential for the CVMIC and the I²C isolation device on the High Voltage (HV) side. The High Voltage System (HVS) and the LVS are galvanically isolated and do not share a common reference potential. The voltages on the LV side of the system are referenced to the GND potential. The pink dashed line marks the isolation and must be considered during part selection for the parts in question. The cell voltages and the voltage drop across the shunt resistor R_{Shunt} are measured by the cell

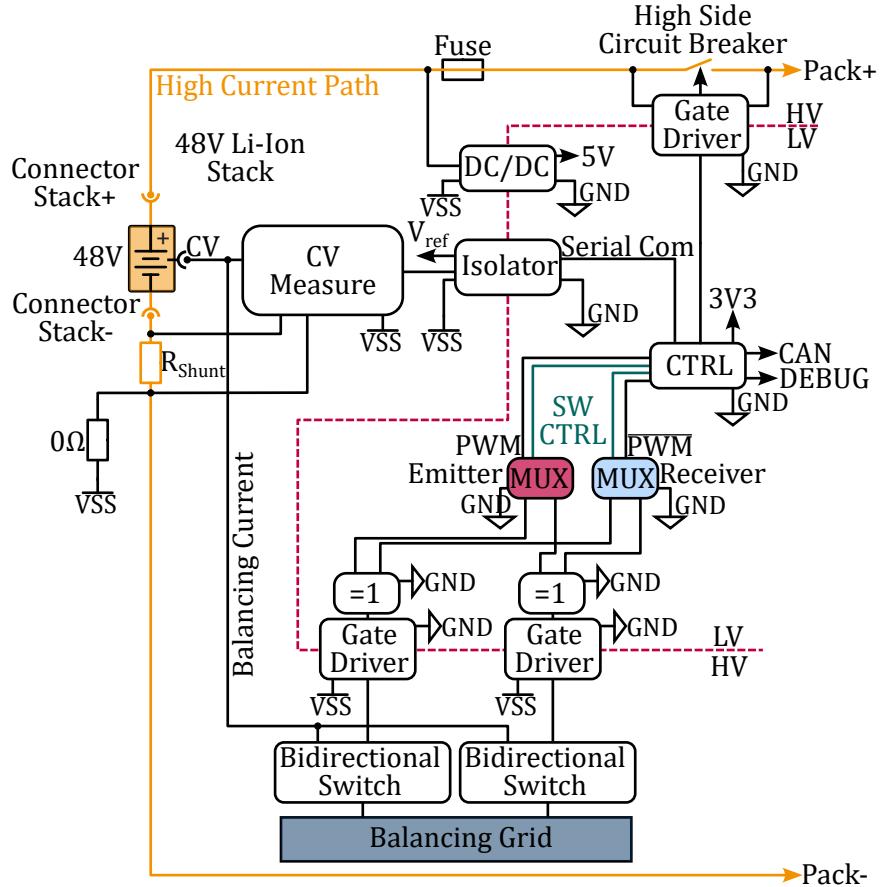


Figure 5.2: Elaborated BMS concept.

voltage measurement IC and sent to the main controller using serial communication. The main controller unit (CTRL) runs the control algorithm as described in [66]. The PWM signal generated by the controller is conducted to the Multiplexer (MUX) of the emitter cell, whilst the complementary PWM signal is conducted to the MUX of the receiver cell. Both signals are then conducted to the respective cells by setting the control pins of the Multiplexers (green SW CTRL lines). The signal is routed through an OR-Gate before it reaches the gate driver, so the gates of the bidirectional switches are switched when either the cell is addressed as a charge-emitting or receiving cell. Since the emitter and the receiver units are controlled by complementary PWM signals, it is avoided that one cell can act as an emitter and receiver cell at the same time.

While Figure 5.2 only features two switching units, one switching unit will be implemented for each cell, resulting in 16 units according to the requirements listed in section 5.1. The switching units are connected to the cells by the cell voltage connector, which provides a wired connection to each cell pole in the stack. The bidirectional switches connect to the removable balancing grid, stacked to the balancing PCB using pin-headers.

The Low Voltage (LV) side of the system is supplied from the HV system using an isolated DC/DC converter, which means that the whole system can operate on its own without an external low-voltage power supply. The converter's input voltage range has

to cover the voltage range of the battery stack during operation. The output voltage of the DC/DC converter is 5 V, which is required for the operation of most available multiplexers. The 5 V output is further regulated down to 3.3 V, which is commonly used as supply voltage for microcontrollers of various manufacturers. The microcontroller has a CAN interface and a debug interface, required to flash the software onto the PCB.

Besides using an isolated DC/DC converter, the isolation between the HV and LV system along the pink dashed line is assured by using isolated gate drivers as well as an isolation device for the serial communication. This ensures galvanic isolation between the Cell Voltages referenced to the VSS-potential and the LV system referenced to LVGND.

5.2.3 Working Principle

The working principle of the circuit to control the switches is depicted in Figure 5.3. The system comprises the emitter and the receiver circuit, where the emitter circuit controls the discharging process of the higher-charged, energy-emitting cell, whilst the receiver circuit controls the charging process of the lower-charged, energy-receiving cell.

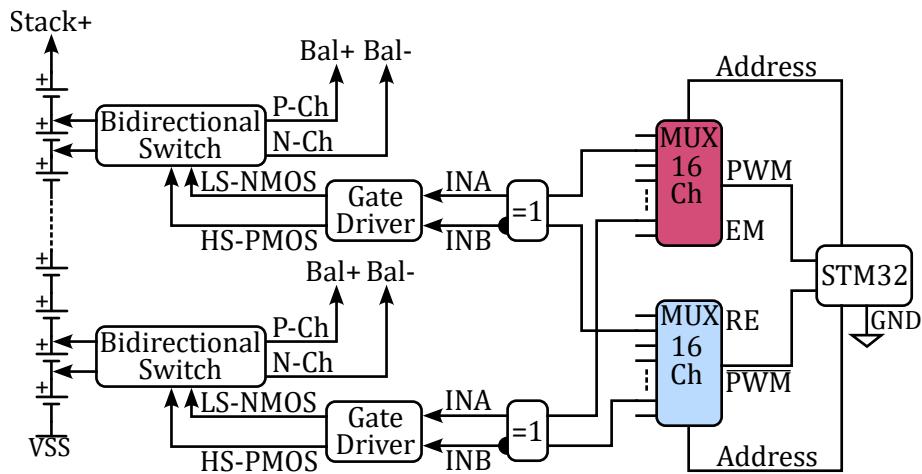


Figure 5.3: Working principle, Emitter (EM) circuit and Receiver (RE) circuit.

Based on the cell voltages measured by the cell voltage measurement chip, the microcontroller defines one cell as the emitter and one cell as the receiver. The non-inverted PWM signal is routed to the emitter MUX whilst the complementary signal is directed to the receiver MUX. The control pins of both the emitter and receiver Multiplexer are set appropriately by the microcontroller so that the PWM signal is routed to the respective switching unit of the correct cell. Each output channel of the MUX is connected to one switching unit of one specific cell.

Upstream to the gate driver, a dual-output OR-gate compares the signal coming from the emitter and receiver Multiplexer. This is necessary so every cell can act as an emitter or receiver. One output of the OR-gate directly connects to the input of the gate driver that controls the low-side NMOS. The other output is inverted and connected to the gate driver input controlling the high-side PMOS. The gate driver can pull the gates of the MOSFETs either to the positive pole of the respective cell or to the negative pole.

In case that the gate of the high-side P-Channel MOSFET is pulled to the negative cell tab potential, a negative gate-source voltage $U_{GS} < 0$ is applied and the high-side part of the switching unit is conducting. If the gate of the high-side PMOS is connected to the positive tab of the cell, the gate-source voltage U_{GS} is at 0 V and the MOSFET blocks any current. Since the high-side is made of two MOSFETs mirrored to each other with their drain pins connected, this operation principle allows to block current or let it pass in both directions.

The same principle but with inverted properties applies for the low-side NMOS. If the gate of the low-side NMOS is connected to the positive cell tab, a positive gate-source voltage $U_{GS} > 0$ is applied, putting the NMOS into conducting mode. If the gate is connected to the negative cell tab, the gate-source voltage is at 0 V and no current can flow.

Using the considerations made above, the following truth table can be established.

Table 5.1: Hardware circuit truth table.

Emitter circuit						
STM PWM output	Emitter PWM	Gate Driver Input A	Gate Driver Input B	Low-side NMOS	High-side PMOS	Switch state
HIGH	HIGH	HIGH	LOW	HIGH	LOW	Conducting
LOW	LOW	LOW	HIGH	LOW	HIGH	Blocking
Receiver circuit						
STM PWM output	Receiver PWM	Gate Driver Input A	Gate Driver Input B	Low-side NMOS	High-side PMOS	Switch state
HIGH	LOW	LOW	HIGH	LOW	HIGH	Blocking
LOW	HIGH	HIGH	LOW	HIGH	LOW	Conducting

5.3 Part Selection

The next step in the development process is the part selection based on the concept elaborated in subsection 5.2.2. The following section includes the design criteria of some key system parts. It should be noted that the packaging of the components was selected to be as small as possible, but still offers good hand-soldering capabilities.

5.3.1 Cell Voltage Measurement IC

The cell voltage measurement chip is one of the key elements of any battery balancing system, whether active or passive. In the present application, the chip must measure the individual voltage of 16 cells connected in series. Further, the option to measure the current on the HCP by measuring the voltage across a shunt resistor should be given. A serial communication interface is required and the possibility to add several more ICs in a daisy chain in case the system should be scaled in a later application. Additionally, an integrated LDO must be included since the isolation IC of the serial communication line requires a lower voltage power supply on the HV side of the system.

The *BQ76952*[47] from *TEXAS INSTRUMENTS* offers the capability to monitor up to 16 cells at a voltage of up to 85 V and supports simultaneous current and voltage monitoring. Communication options include either SPI and I²C, where the I²C operates at a baud rate of up to 400 kHz. Further, an internal LDO unit offers an output voltage of 1.8 V and 3.3 V with reference to GND as per Figure 5.2, which can also be programmed to output voltages of 2.5 V or 5 V while delivering an output current of up to 45 mA each. The device is packaged in a TQFP-48 SMD housing.

5.3.2 Controller

The main controller runs the control algorithm described above and needs to comply with the interface requirements mentioned in section 5.1, meaning that it must be equipped with at least one ADC to perform analogue temperature measurements. Additionally, it needs to provide serial communication interface to connect with the cell voltage measurement chip as well as a CAN-interface to integrate the BMS into larger systems. Those requirements are offered by many industry-standard microcontrollers such as the *STM32F103RBT6* [86] from *STMicroelectronics*, which offer one or more 12 bit ADCs with several channels, an I²C and a CAN interface. It can operate at a clock frequency of up to 72 MHz and uses a flash memory of 128 kB and a RAM of 20 kB. These specifications are sufficient to meet the requirements for the present developments, however, microcontrollers from other manufacturers could also be used.

5.3.3 Multiplexer

Since the system is designed to operate with 16 cells, the PWM signal must be routed to 16 switching units. However, the microcontroller has only one output for the PWM signal and one for the complementary signal, which implies the usage of multiplexers on both channels. The *74HC4067PW,118* [87] is a 16-channel high-speed CMOS logic analogue multiplexer, which is controlled by four digital control pins. The multiplexer operates at a typical supply voltage of 5 V, which needs to be provided by an isolated DC/DC converter described below. The high level input voltage is at 1.5 V (minimum) and the low level input voltage is at 0.5 V (maximum), making it suitable for the operation with the PWM output signal of the *STM32* controller.

5.3.4 MOSFETs

The MOSFET used for the switching unit, as described in section 4.3 are general purpose MOSFETs, since they do not need to comply with highly specific prerequisites. Since each MOSFET only acts within the voltage range of a single cell, the voltage ratings only have to cover the cell voltage at the highest SOC. The balancing current did not exceed 2 A during simulations performed in chapter 4, so this is the minimum requirement for the drain current I_D . The P-Channel MOSFET for the high-side switch is an *IRLML2246TRPBF* from *INFINEON*, which is a 1-channel silicon switch in a SOT-23-3 package. The specifications are listed in Table 5.2.

The low side part of the switch is implemented using two mirrored general-purpose N-Channel MOSFETs from the type *INFINEON IRLML6346TRPBF* with the specifications as listed in Table 5.3.

Table 5.2: *INFINEON IRLML2246TRPBF* P-Channel MOSFET specifications [88].

Specification	Symbol	Value	Unit
Drain-Source voltage	U_{DS}	20	V
Drain current	I_D	2.6	A
DS-on resistance	$R_{DS_{on}}$	157	$\text{m}\Omega$
Gate-Source voltage	U_{GS}	± 12	V
Threshold voltage	$U_{GS_{th}}$	1.1	V
Dissipation power	P_{diss}	1.3	V
Temperature	T	-55 to 150	$^{\circ}\text{C}$
Gate Charge	Q_g	2.9	nC
Package		SOT-23-3	

Table 5.3: *INFINEON IRLML6346TRPBF* N-Channel MOSFET specifications [89].

Specification	Symbol	Value	Unit
Drain-Source voltage	U_{DS}	30	V
Drain current	I_D	3.1	A
DS-on resistance	$R_{DS_{on}}$	63	$\text{m}\Omega$
Gate-Source voltage	U_{GS}	± 12	V
Threshold voltage	$U_{GS_{th}}$	0.8	V
Dissipation power	P_{diss}	1.3	V
Temperature	T	-55 to 150	$^{\circ}\text{C}$
Gate Charge	Q_g	2.9	nC
Package		SOT-23-3	

5.3.5 Gate Driver

The gate driver of the switching unit plays a crucial role in the whole system. It is required to have full input-output isolation and two input and two output channels. These requirements are met by the *INFINEON 2EDF7275FXUMA2* [90], which further offers a channel-to-channel isolation on the output side, which, however, is not necessary. The output capacitance of the gate driver, which is charged or discharged to put the MOSFET into conducting or blocking mode, is calculated as demonstrated in [91]. The author claims that Equation 5.1 is valid for the output capacitance C_{boot} , where Q_g is the gate charge of the MOSFET and ΔU_{tol} is the acceptable voltage drop following the charging process of the input capacitance of the MOSFET.

$$C_{boot} = \frac{Q_g}{\Delta U_{tol}} \quad (5.1)$$

Each output of the gate driver controls the gate of two MOSFETs. Both the N-Channel MOSFET and the P-Channel MOSFET have a gate charge of 2.9 nC and ΔU_{tol} is set to be 0.1 V. Since the high-side and the low-side switch share the same output capacitance

of the gate driver, Equation 5.1 results in Equation 5.2.

$$C_{\text{boot}} = \frac{4 \cdot 2.9 \times 10^{-9} \text{ C}}{0.1 \text{ V}} \quad (5.2)$$

$$C_{\text{boot}} = 116 \text{ nF}$$

The value of 116 nF is the absolute minimum required for reliable switching. However, experience over time has shown that a higher output capacitance often delivers better performance, hence the output capacity is set to 330 nF.

5.3.6 Circuit breaker

The circuit breaker is designed as a bidirectional switch, referring to the reference design in [92], using the gate driver described in subsection 5.3.5. The switching unit consists of two power MOSFETs that can either be connected in source-to-source or drain-to-drain configuration, both are also referred to as back-to-back configuration. In a source-to-source configuration, both MOSFETs are placed in series with their source pins connected to each other and the drain terminals form the input and output of the switch. This configuration offers faster switching and is less expensive since only one charge pump or isolated power supply is required, which allows an implementation with a single channel gate driver, resulting in a less complex design. Yet in case of gate driver failure, both MOSFETs will likely fail. Further, this circuit has less thermal dissipation area for FETs with standard drain down packages. The drain-to-drain configuration as shown in Figure 5.4, where the drain pins of the FETs are connected to each other and the source terminals form the input and output, usually requires a more complex design and needs an additional charge pump to drive both MOSFETs. Nevertheless, this offers the possibility to control both FETs independently and an easier way to implement safe communication technologies. The need for two separate or dual-channel gate drivers results in a higher safety standard for the switching unit. The implementation of the Bidirectional Protection Switch (BDPS) can be done using two N-Channel or P-Channel FETs, however N-Channel FETs are usually preferred due to their lower $R_{DS_{on}}$ and lower cost compared to P-Channel FETs [93].

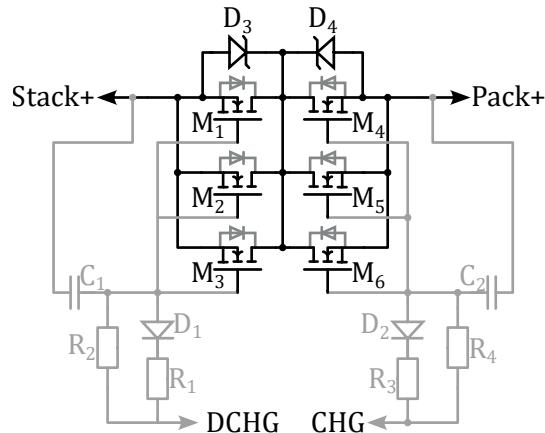


Figure 5.4: Circuit Breaker and intermediate gate circuit [93].

As depicted in Figure 5.2, the BDPS is built as a high-side protection switch configuration, which entails the implementation on the positive pole of the battery stack. The benefit of a high-side protection is that no bypass of the ground potential is necessary, implying no hanging ground. However, this configuration requires gate drivers with integrated charge pumps to drive the gates of the MOSFETs. In contrast, the low-side protection is more straightforward to implement as no charge pumps are required for the gate drivers. However, this circuit has the drawback of a hanging ground with the potential of ground bypass via the battery housing impacting communication and operation [93]. The MOSFETs used to implement the BDPS (INFINEON PTG014N10NM5 [94]) are rated for a continuous drain current of 37 A, hence, as drafted in Figure 5.4, three MOSFETs are connected in parallel to handle a maximum continuous current of 111 A. The gates are connected to the dual gate driver via the grey-coloured intermediate circuit. Both the charging pin (CHG) and the discharge pin (DCHG) can be controlled independently by the microcontroller.

5.3.7 Fuse

As stated in section 5.1 and confirmed by Figure 1.2, the battery stack to be balanced is rated for a nominal power P_N of 1500 W and a peak power P_{Peak} of 130 % of the nominal power as calculated in Equation 5.3.

$$\begin{aligned} P_{\text{Peak}} &= 130\% \cdot P_N \\ P_{\text{Peak}} &= 130\% \cdot 1500 \text{W} \\ P_{\text{Peak}} &= 1950 \text{W} \end{aligned} \tag{5.3}$$

At a nominal stack voltage U_N of 48 V, the nominal current I_N can be calculated by Equation 5.4.

$$\begin{aligned} I_N &= \frac{P_{\text{Peak}}}{U_N} \\ I_N &= \frac{1950 \text{W}}{48 \text{V}} \\ I_N &= 40.625 \text{A} \end{aligned} \tag{5.4}$$

This implies the fuse must be rated for a current of at least 40.625 A. However, current spikes may lead to short-term higher currents, which do not damage the hardware, so a current rating of 50 A is selected. To meet safety standards, the voltage rating of the fuse is chosen to be at least two times higher than the nominal stack voltage. In the present case, this results in $2 \cdot 48 \text{V} = 96 \text{V}$, which is round up to 100 V.

The rated current of a fuse only gives information about the current at which the fuse will open the circuit. It does not specify the highest current under which a fuse can still open and cut the line. This specification is referred to as the interrupt rating and is usually selected based on the highest theoretical short-circuit current that can occur in the system. It is calculated using the battery's internal resistance and the highest possible stack voltage. Assuming every cell is charged to its highest voltage of 4.2 V, the short circuit current I_{SC} results is calculated as per Equation 5.5, using an internal resistance R_i of 48 mΩ as given by the manufacturer of the used battery stack under laboratory

conditions.

$$\begin{aligned} I_{SC} &= \frac{U_{max}}{I_{SC}} \\ I_{SC} &= \frac{16 \cdot 4.2V}{48 \times 10^{-3} \Omega} \\ I_{SC} &= 1400A \end{aligned} \quad (5.5)$$

5.3.8 Low voltage Power Supply

As per the draft in Figure 5.2, the Low Voltage System is supplied by the stack voltage whilst still respecting the galvanic isolation between the two systems. This implies the usage of an isolated DC/DC converter. The input voltage of the converter needs to cover the stack voltage range during operation, which can be assumed to be in the range of 44.8 V to 67.2 V at a cell voltage of 2.8 V or 4.2 V respectively. An output current of around 50 mA at a voltage of 5 V is required to supply the low-voltage components of the system. Such specifications are provided, e.g. by the *TMR 1-4811SM (TRACO POWER)* [95], offering an input-output isolation of 1500 V. Care must be taken during the design of the appurtenant circuit to keep the isolation valid. This primarily concerns the link capacitors C_{link} between the negative stack and the isolated ground potential VSS and GND as shown in Figure 5.5. The 5 V output is used to supply the multiplexers and serves as the

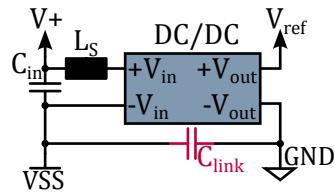


Figure 5.5: DC/DC schematic.

reference voltage for the PTC temperature sensors. It is further regulated to 3.3 V by a general purpose Low-Dropout (LDO) to provide supply voltage to the *STM32* controller as well as the control logic of the switching units and the primary side of the gate drivers.

6 Schematic Design and Layout

This chapter explains some parts of the schematics designed for the prototype following the requirements as of section 5.1. The completed schematics as well as the layout of both the balancer PCB and the PCB containing the balancing energy storage element can be found in Appendix A. Note that during testing of the PCB described on the following pages under laboratory conditions, several bugs were found which are not updated in the referred schematics, see Appendix A of the initial revision (HW.RV1-1). A complete list of known hardware bugs and enhancement features is provided in Table 9.1.

6.1 Schematic Design

The following section describes the schematic design of the electrical circuits for the prototype.

6.1.1 Schematic Structure

The schematic documents are structured into several layers, each layer containing one or more functional units. Functional units may be composed of one or more electrical circuits that may be reproduced several times inside the same layer.

6.1.1.1 Top Level Schematics

The top-level schematics are structured into several sheets according to page 3 of the appended schematic document. The *PSU_CAN* sheet contains the PSU circuit and the CAN transceiver circuit. A connection via the transmitting and receiving CAN lines is established to the *STM32* sheet containing the board's main control unit. Several bus and signal and signal harness connections depart from the *STM32* sheet with destination amongst others of the *CV-MEASURE* sheet, where the cell voltage measurement unit is implemented. Several bus connections containing the multiplexer control signals, as well as single line connections transferring the PWM signals, are routed to the *MUX* sheet, where all multiplexing units are implemented. The output of the *MUX* sheet is connected to the switch top layer, which contains the switching units and the respective control logic as described in subsubsection 6.1.1.2. All sheets are connected to the *CONNECTOR* sheet, which contains all the PCB interface connectors, including the pin header to stack up the balancing grid. Further, this sheet contains the High Current Path (HCP) including the fuse and the circuit breaker schematic.

6.1.1.2 Switch Top Layer

The bidirectional balancing switches are grouped by four switches, making up one top-layer switching unit as per Figure 6.1. Each top-layer switching unit receives four cell voltages on the input side and the PWM signals from the emitter and receiver MUX. The outputs of each switching unit are the positive and negative connections of each of the four cells, which are then routed to the balancing grid, which is implemented on a separate PCB.

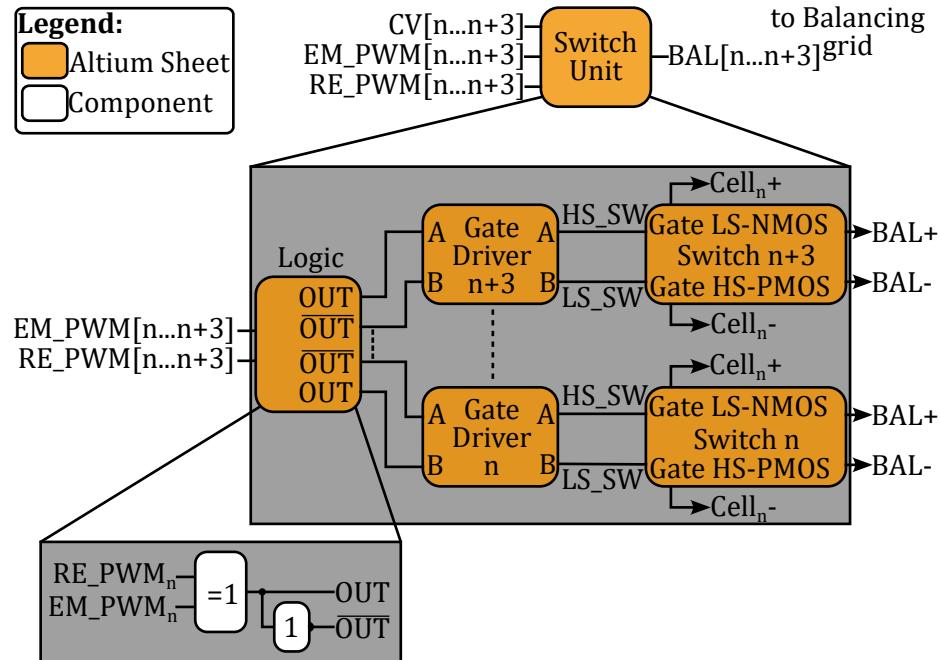


Figure 6.1: Schematic Hierarchy of a Switch Unit consisting of the Control Logic, four Gate Driver circuits and four bidirectional switches.

6.1.1.3 Switch Unit

The next layer consists of three subsystems. The first subsystem includes the digital logic block. Its central element is a quad two-input OR-gate. The input in each case is the PWM signal coming from the emitter Multiplexer or the receiver Multiplexer (MUX), meaning that each cell has its own OR gate so that the cell can act as receiver or as emitter. The output of each OR-gate is split, where one signal is directly sent to the output of the logic block and one signal is inverted using a dual inverter IC. The non-inverted output is routed to the Input A of the dual gate driver, which controls the low-side NMOS whilst the inverted signal is sent to the Input B, controlling the high-side PMOS.

6.1.2 Gate Driver Schematic

The non-inverted and the inverted signal, as described in subsubsection 6.1.1.3, are connected to the pins 1 and 2 of the *INFINEON 2EDF7275FXUMA2[90]*. The primary side

of the gate driver is supplied by the 3.3 V generated by the LDO as explained in subsection 5.3.8 with reference to the isolated low voltage ground potential. The supply on the secondary side (HV side) is provided by the voltage of the cell that the gate driver belongs to. This implies that both VDDA (Pin 16) and VDBB (Pin 11) are connected to the positive cell tab of the respective cell, while GNDA (Pin 14) and GNDB (Pin 10) are connected to the negative cell tab. Between both potentials, an output capacitor is placed with a capacitance of 330 nF as discussed in subsection 5.3.5. The output A (Pin 15) of the gate driver is connected to the low side NMOS, and the output B is connected to the high side PMOS of the bidirectional switch. The bidirectional switch itself is implemented as described in section 4.3.

6.1.3 Cell Voltage Measurement and Microcontroller

The cell voltages are measured by the *TEXAS INSTRUMENTS BQ7695202PFBR*, which further determines the load current by measuring the voltage drop across a shunt resistor in the High Current Path. The CVMIC is supplied by the battery stack using the BAT-pin (Pin 47), including a reverse polarity protection diode, a current limiting resistor of $100\ \Omega$ and several voltage stabilisation capacitors. An important feature of the used IC is its integrated LDO to generate a low voltage supply which is needed to supply the isolated side of the I²C communication isolation module as well as the SCL and the SDA line. The LDO consists of an NPN Bipolar Junction Transistor (BJT) (*DIODES INCORPORATED FCX495TA* [96]), which has to withstand a collector-emitter voltage of at least twice the maximum system voltage, and is controlled by the BREG-pin (Pin 37) of the CVMIC. The input voltage is picked from the common drain of the bidirectional switch that forms the circuit breaker. A reverse polarity protection diode and a current limiting resistor block designed for a rated maximum power of $P_{max} = 2.5\text{ W}$ is connected between the voltage pickup point and the collector pins of the BJT. The circuit's output voltage is fed back to the CVMIC and stabilised by capacitors. The measured cell voltages and the load current are transmitted to the microcontroller using the I²C serial communication protocol. To maintain galvanic isolation between the HVS and LVS, the communication of the SDA and the SCL lines are isolated by a bidirectional capacitive isolation device (*TEXAS INSTRUMENTS ISO1541DR* [97]), that can withstand a voltage of 2.5 kV_{rms} .

The microcontroller (*STM32F103RBT6*) receives the cell voltages transmitted via I²C from the CVMIC, where a default baud rate of 100 kHz is used, that can however be scaled up to 400 kHz if a higher sampling rate is required. The microcontroller itself runs at a clock frequency of 8 MHz, which is generated by a quartz crystal (*WÜRTH ELEKTRONIK WE-XTAL Quartz Crystal* [98]). It is further equipped with a Real Time Clock (RTC) oscillator running at a frequency of 32.768 kHz (*WÜRTH ELEKTRONIK WE-XTAL Watch Crystal* [99]). The controller can be manually reset and put into boot mode by pushing the respective push button integrated on the PCB. Information on its state can be given out by programming the three status LEDs, which can be controlled by setting or resetting the respective GPIOs. The microcontroller runs the software described in section 6.3, defining the emitter and receiver cell and controlling the address pins of the Multiplexers by switching the STMs GPIOs accordingly.

The pin assignment on the STM32 can be deducted from subsection 6.1.4.

6.1.4 Pin Assignment and Signal Label Convention

The schematic document uses the following convention for signal labelling, except for a few cases where the source or other label information is obsolete. The signal label consists of the signal source, the signal nature (analogue or digital) and the signal name, which can have multiple parts. Underscores separate the information.

Source_Input/Output_Analog/Digital_Name

e.g.

STM_O_D_TEMP_SEL

The pin assignments of the microcontroller as for the hardware revision *HW.RV1-1* are given in Table 6.1 and Table 6.2

Table 6.1: STM32 Pin assignment *HW.RV1-1* (Pin 1 to 32).

Pin (LQFP-64)	Pin name	Hardware Signal	Description
1	VBAT		-
2	PC13		-
3	PC14	OSC32_IN	RTC-Oscillator In
4	PC15	OSC32_OUT	RTC-Oscillator Out
5	OSC_IN	OSC_IN	System Clock In
6	OSC_OUT	OSC_OUT	System Clock Out
7	NRST	NRST	Negated Hardware Reset
8	PC0	STM_O_D_TEMP_SEL_S3	Temperature MUX Address input 3
9	PC1	STM_O_D_TEMP_SEL_S2	Temperature MUX Address input 2
10	PC2	STM_O_D_TEMP_SEL_S0	Temperature MUX Address input 0
11	PC3	STM_O_D_TEMP_SEL_S1	Temperature MUX Address input 1
12	VSSA	GND	LV Ground
13	VDDA	3V3	3.3 V supply
14	PA0-WKUP		-
15	PA1		-
16	PA2		-
17	PA3		-
18	VSS_4	GND	LV Ground
19	VDD_4	3V3	3.3 V supply
20	PA4	MUX_O_D_TEMP_ADC	Temperature signal ADC input
21	PA5		-
22	PA6		-
23	PA7	O_D_RE_PWM	Receiver PWM
24	PC4	STM_O_D_EM_SEL_S3	Emitter MUX Address input 3
25	PC5	STM_O_D_EM_SEL_S2	Emitter MUX Address input 2
26	PB0	STM_O_D_EM_SEL_S1	Emitter MUX Address input 1
27	PB1	STM_O_D_EM_SEL_S0	Emitter MUX Address input 0
28	PB2		-
29	PB10		-
30	PB11		-
31	VSS_1	GND	LV Ground
32	VDD_1	3V3	3.3 V supply

Table 6.2: STM32 Pin assignment *HW.RVI-1* (Pin 33 to 64).

Pin (LQFP-64)	Pin name	Hardware Signal	Description
33	PB12	O_D_STS_LED_RD	Status LED Red
34	PB13	O_D_STS_LED_BL	Status LED Blue
35	PB14	O_D_STS_LED_GN	Status LED Green
36	PB15		-
37	PC6	STM_O_D_RE_SEL_S2	Receiver MUX Address input 2
38	PC7	STM_O_D_RE_SEL_S3	Receiver MUX Address input 3
39	PC8	STM_O_D_RE_SEL_S0	Receiver MUX Address input 0
40	PC9	STM_O_D_RE_SEL_S1	Receiver MUX Address input 1
41	PA8	O_D_EM_PWM	Receiver PWM signal
42	PA9		-
43	PA10		-
44	PA11	CAN_RX	CAN1 Receiver Pin
45	PA12	CAN_TX	CAN1 Transmitter Pin
46	PA13	SYS_SWDIO	SWDIO Debug Pin
47	VSS_2	GND	LV Ground
48	VDD_2	3V3	3.3 V supply
49	PA14	SYS_SWCLK	SWCLK Debug Pin
50	PA15		-
51	PC10		-
52	PC11		-
53	PC12		-
54	PD2		-
55	PB3	SYS_SWO	SWO Debug Pin
56	PB4	STM_O_D_DCHG	Circuit breaker discharge
57	PB5	STM_O_D_CHG	Circuit breaker charge
58	PB6	I2C1_SCL	I ² C SCL
59	PB7	I2C1_SDA	I ² C SDA
60	BOOT0	BOOT0	Boot mode
61	PB8		-
62	PB9		-
63	VSS_3	GND	LV Ground
64	VDD_3	3V3	3.3 V supply

6.2 PCB Layout

The following section describes the structure and layout of the main Printed Circuit Board containing the High Current Path, the switching units, the cell voltage measurement unit as well as the microcontroller and the control logic. The PCB containing the balancing energy storing element that is stacked up onto the main PCB using a pin-header. A 3-dimensional model of the PCB is depicted in Figure 6.2.

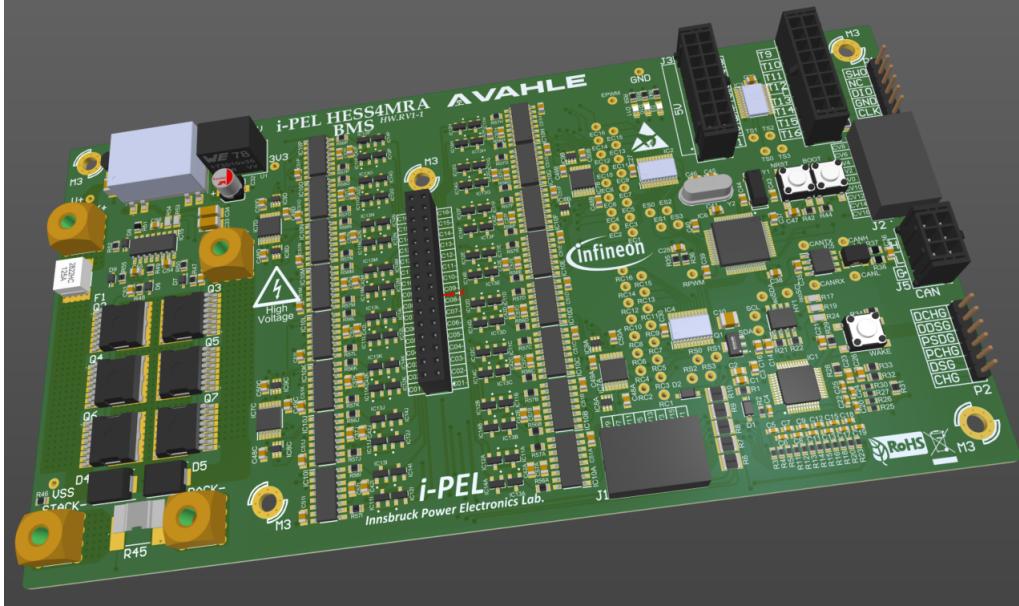


Figure 6.2: Perspective view on a 3D-model of the Printed Circuit Board (PCB) designed using *ALTIUM DESIGNER 19.0*.

6.2.1 General PCB Setup

The circuit is implemented on a 4-layer PCB with the main layer function as per Table 6.3. The top layer routes most low-voltage signals, especially the logic circuits,

Table 6.3: PCB layer properties.

Layer	Name	Function
1	Top Layer	Signal 1
2	Internal 1	GND/VSS
3	Internal 2	LV supply (5 V & 3.3 V)
4	Bottom Layer	Signal 2

including the Multiplexer circuitry and the microcontroller signals. The second layer is used for the reference potential in both voltage systems, meaning that it carries both the LV ground as well as the reference potential for the High Voltage system (VSS). The third layer is used as a LV supply layer, carrying the isolated supply voltages of 5 V and

3.3 V. The bottom layer is a second signal layer that offers space for further control signals, but mainly for the path between the cell voltage connectors and the measuring circuit. In addition, the balancing current between the cells, the switching units and the balancing tank is routed on the bottom layer.

The PCB layout is divided into three parts, the left section includes the HCP with the DC/DC converters and the power connectors. The middle part contains the switching units, including the gate driver circuits and the MOSFETs as well as the pin-header to stack up the balancing board. The right part is used to place the LV components such as the microcontroller, the Multiplexers and the cell voltage measuring circuit. Further, the temperature signals and the communication interfaces are connected here.

6.2.2 High Current Path

The High Current Path is routed from the *STACK+* connector (most positive cell pole) across the fuse to the circuit breaker until it reaches the *PACK+* connector, where the positive pole of the load is connected. The negative pole of the load is connected to the *PACK-* connector that leads to the current measuring shunt resistor and the *STACK-* connector (most negative cell pole). The power connectors are implemented as high-current

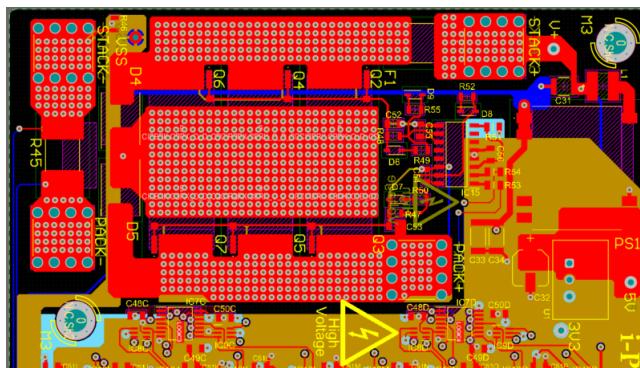


Figure 6.3: High Current Path consisting of copper polygons and thermal vias connecting all four layers for thermal management of the high power devices.

screw terminals that are press-fitted onto the PCB. The high-current tracks (minimum trace-width of 7.3 mm on each layer) are routed across all four layers, which are connected using through-hole copper vias as seen in Figure 6.3 to reduce the thermal stress on each track. A connection with a trace-width of 4 mm is also routed to the DC/DC converter.

6.2.3 Cell Voltage Measurement Circuit

The layout of CV measurement circuit is designed with regard to placing the filter units as close to the input pins of the CVMIC. Those parts' footprint is selected as 0603, allowing a placement close to each other directly at the pins of the IC. The layout is shown in Figure 6.4.

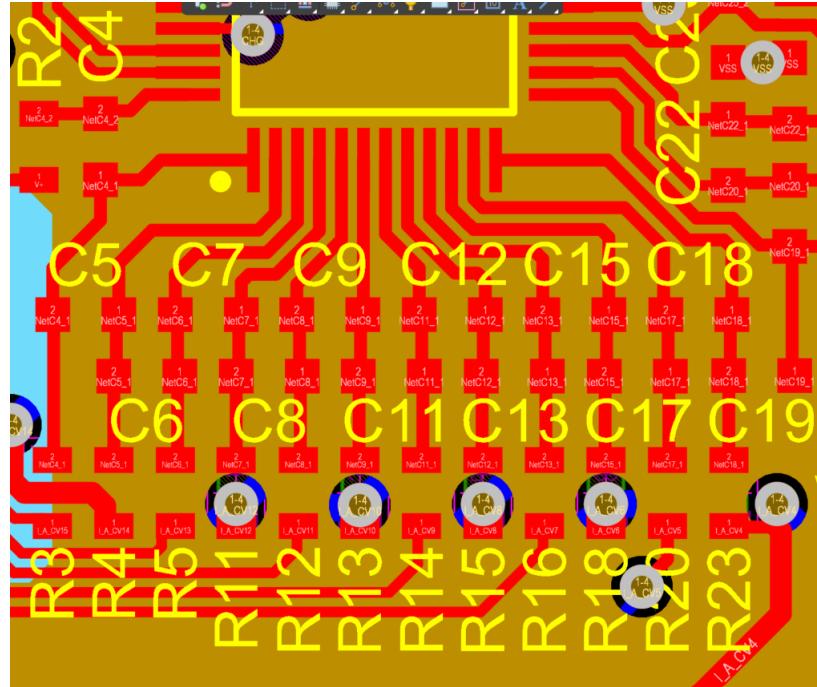


Figure 6.4: Cell Voltage measurement Integrated Circuit (IC) input layout.

6.2.4 Switching Unit and Balancing Tank

All 16 switching units are designed identically using rooms in *ALTIUM DESIGNER*. Each unit includes one gate driver, two N-Channel MOSFETs and two P-Channel MOSFETs. The current carrying tracks are designed with a trace-width of 0.7 mm, which is broadly enough to carry the balancing current peaks of 2 A as calculated in chapter 4. After passing the switching unit, the tracks connecting the positive and negative poles of each cell are routed to the pin-header leading to the balancing tank PCB.

The balancing tank PCB is designed as a small board stacked up to the main Printed Circuit Board (PCB). It connects every positive and negative output of each cell in parallel so that every cell can be connected in series to the balancing energy storing element when the respective switching unit is put into conduction mode. The energy-storing element on the balancing tank can be replaced, or the actual value can be changed. Several 0805 and 1206 footprints are placed on the PCB to allow a simple modification of the balancing capacitance, see Figure 6.5.

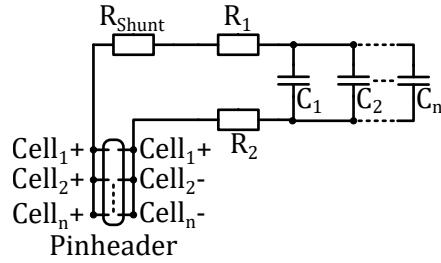


Figure 6.5: Balancing tank schematics. R_{Shunt} is a shunt resistor with a constant value of $25 \text{ m}\Omega$ to measure the balancing current. The resistors R_1 and R_2 are used to limit the balancing current but may be set to 0Ω . The capacities C_1 to C_n are the balancing energy storage capacitors whose capacitances may be changed throughout the testing phase.

6.2.5 Power Supply

The LV supply is generated above the High Current Path and routed using polygons to the required areas. A large plane on the third layer supplies the switching units and the microcontroller with 3.3 V . Similar routing is applied to the 5 V polygon. The ground reference plane is routed across the whole section below the LV-supply on the second layer. The VSS-plane is routed in a similar way to the ground layer. The low voltage signal routing is done according to common PCB design standards on the top and bottom layers.

6.3 Software Design

The following section describes the design of the software running on the prototypes *STM32* microcontroller.

6.3.1 Balancing Algorithm and Unit Testing

The initial code to test the balancing system contains a reduced balancing algorithm that allows the user to predefine an array with four physical addresses of switching units. These four cells are then balanced against each other, making unit testing much faster than balancing all 16 cells of a stack. The implementation code programmed in C using the HAL library is listed below. The algorithm as described in Figure 6.6 starts by reading out the cell as 16-bit unsigned integers using the I²C protocol as described in subsection 6.3.2. It then verifies if any difference between two cell voltages is higher than

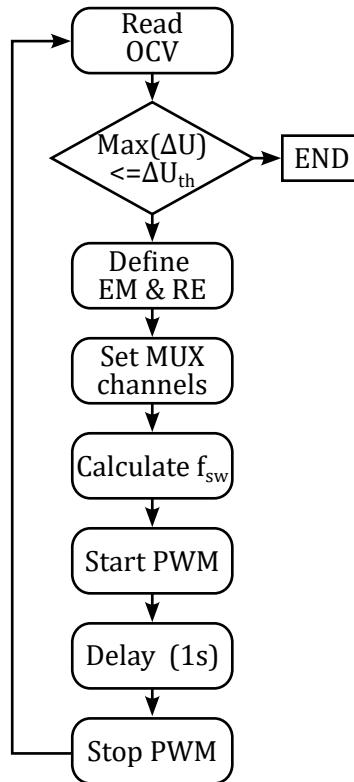


Figure 6.6: Software flowchart.

the global threshold of 30 mV. If no difference is higher, the function returns a boolean *TRUE* and stops the algorithm. In any other case, the emitter and receiver cells are defined based on the highest and lowest voltage inside the four-cell array. The respective channels of the emitter and receiver multiplexers are then set using the logic described in subsection 6.3.3. Afterwards, the PWM generator is started with a frequency of 1000 Hz. Note that in the present testing case, the switching frequency as well as the duty cycle are hard-coded constant values, however, this may be changed to adaptive values with respect to the SOC of the discharging and charging cell as described in [66]. Cells are

then balanced for 1 s until the PWM signal is stopped and boolean *FALSE* is returned. The interruption of the balancing process permits the measurement of the Open Circuit Voltage of the cells without the voltage experiencing a drop due to the balancing currents. The function is called in an endless *while-loop* from the main function until the return flag is set to logical *TRUE*.

```

1  bool FourcellBalancer(TIM_HandleTypeDef * htim1, I2C_HandleTypeDef * 
2    hi2c, uint16_t threshold){
3    const uint8_t Balancingcells = 4; // Number of balancing cells
4    uint16_t EmitterIndex, ReceiverIndex;
5    uint8_t cellAddress[4] = {2,3,4,6}; // Physical unit addresses
6      on PCB
7    uint8_t cellIndex; uint16_t CV[4]; // Index & Cell voltage array
8
9    for (int i = 1; i < Balancingcells; i++){ // Read cell voltages
10      cellIndex = cellAddress[i] - 1;
11      CV[i] = ReadCellVoltage(&hi2c, cellIndex);
12    }
13    if (abs(Min(CV))-Max(CV) < threshold){ // Stop balancing if
14      within threshold
15      switchLED(2, true); return true; // Turn on blue LED
16    }
17
18    EmitterIndex = findMaxIndex(CV, Balancingcells); // Define
19      emitter
20    ReceiverIndex = findMinIndex(CV, Balancingcells); // Define
21      receiver
22
23    SetMuxChannel(EmitterIndex, 'E'); // Set Multiplexers
24    SetMuxChannel(ReceiverIndex, 'R');
25    HAL_TIM_PWM_Start(&htim1, TIM_CHANNEL_1); HAL_TIMEx_PWMN_Start(&
26      htim1, TIM_CHANNEL_1);
27    Set_PWM_Frequency(1000); Set_PWM_DutyCycle(50); // Start PWM
28    HAL_Delay(1000); // Balance for 1 second
29    HAL_TIM_PWM_Stop(htim1, TIM_CHANNEL_1);
30    HAL_TIMEx_PWMN_Stop(htim1, TIM_CHANNEL_1); // Stop PWM
31    return false;
32 }
```

6.3.2 I²C Communication

The I²C communication is implemented using the standard functions provided by the HAL library. The register addresses of the cell voltages are stored in the arrays *CV_REG_HIGH* and *CV_REG_LOW* as hexadecimal values where $CV_REG_LOW[i] = 0x14 + 2 \cdot i, i \in [0..15]$ and $CV_REG_HIGH[i] = 0x14 + (2 \cdot i - 1), i \in [0..15]$. In a first step, the bus status is checked and the status LEDs are switched on in a hardware error case. The 8-bit unsigned integers are then extracted from CVMIC at the respective registers according to the datasheet [47] using the *HAL_I2C_Mem_Read* function, which first transmits the command to read the cell voltage by sending the respective hexadecimal command from the arrays mentioned above and then reads the register after a short time delay. This means the memory-read function can be implemented by simply transmitting the command and reading the register afterwards. The Cell Voltages are the raw 24-bit digital output of the ADC as the voltage difference between two adjacent cells

$(CV[i] = CV_{i+1} - CV_i)$ and are stored with a 16-bit resolution using units of 1 mV. The Cell Voltage measurement supports the recommended voltages from -0.2 V to 5.5 V and may report incorrect values if the recommended voltages are exceeded [47].

The transmission of the Cell Voltage is done in two steps since only 8 bits can be transmitted per frame. In a first step, the lower byte of the 16-bit value is transmitted to the microcontroller and after a time delay of 10 ms, the upper byte is transmitted. In case of a communication error, the transmission is aborted and the red status-LED is switched on. The process is restarted upon the following function call. If the transmission is successful, both bytes are combined by shifting the upper byte's 8 bits to the left and appending the lower byte.

```

1  uint16_t ReadCellVoltage(I2C_HandleTypeDef *hi2c, int index){
2      uint8_t cell_voltage_low, cell_voltage_high;
3      uint16_t cell_voltage, CV_REG_LOW = CELL_REG_ADD_LOW[index],
4              CV_REG_HIGH = CELL_REG_ADD_HIGH[index];
5      bool StatusHighByte = false, StatusLowByte = false;
6
7      if(HAL_I2C_GetState(hi2c) != HAL_I2C_STATE_READY) { // Handle
8          bus not ready state
9          switchLED(2, true);
10         switchLED(3, true);
11         HAL_Delay(100);
12         return 0;
13     }
14
15     if (HAL_I2C_Mem_Read(hi2c, BQ76952_I2C_ADDRESS, CV_REG_LOW,
16                           I2C_MEMADD_SIZE_8BIT, &cell_voltage_low, 1, HAL_MAX_DELAY)
17     != HAL_OK) {
18         HAL_GPIO_WritePin(O_D_STS_LED_RD_Port, O_D_STS_LED_RD_Pin,
19                           GPIO_PIN_RESET);
20     } else { StatusLowByte = true; }
21
22     HAL_Delay(10); // Short delay before next read
23
24     if (HAL_I2C_Mem_Read(hi2c, BQ76952_I2C_ADDRESS, CV_REG_HIGH,
25                           I2C_MEMADD_SIZE_8BIT, &cell_voltage_high, 1, HAL_MAX_DELAY)
26     != HAL_OK) {
27         HAL_GPIO_WritePin(O_D_STS_LED_RD_Port, O_D_STS_LED_RD_Pin,
28                           GPIO_PIN_RESET);
29     } else { StatusHighByte = true; }
30
31     if (StatusHighByte && StatusLowByte) switchLED(2, true); // Turn
32     on LED if successful
33
34     cell_voltage = (cell_voltage_high << 8) | cell_voltage_low; // Combine bytes
35
36     return cell_voltage;
37 }
```

6.3.3 Multiplexer Control

The logic to control the Multiplexers is described below. The cell index is handed over to the function as an unsigned 8-bit value, where the index is the physical output port of the multiplexer, ranging from 1 to 16. The MUX has four digital input control pins

to set the output ports, these are linked to the variables s_1 to s_3 in the software of the microcontroller. The state of the variables is determined by subtracting 1 from the input value and comparing it with a linkage value using a bitwise AND operator. The linkage value of the port n is determined by $x_n = 2^n$. The output value of the bitwise AND operation is shifted to the right by n bits, resulting in a logical 1 or 0 which is used to set the respective hardware port of the microcontroller and hence the control pin of the Multiplexer accordingly.

```
1 void SetMuxChannel(uint8_t cellIndex){  
2     uint8_t s0, s1, s2, s3;  
3     s0 = (cellIndex-1 & 0x01);  
4     s1 = (cellIndex-1 & 0x02) >> 1;  
5     s2 = (cellIndex-1 & 0x04) >> 2;  
6     s3 = (cellIndex-1 & 0x08) >> 3;  
7  
8     // Set ports 0 to 3 of multiplexer  
9     HAL_GPIO_WritePin(O_D_EM_S0_Port, O_D_EM_S0_Pin, s0);  
10    HAL_GPIO_WritePin(O_D_EM_S1_Port, O_D_EM_S1_Pin, s1);  
11    ...  
12 }
```

7 Results

The following section describes the assembled prototype PCB and the test results under laboratory conditions. Two PCBs were assembled in a first stage, serving as testing prototypes.

7.1 Assembled Printed Circuit Board

The PCB is assembled using reflow soldering for the SMD components and hand-soldering for the THT components. The high-current connectors are pressed into the appropriate drilling in the PCB to avoid large solder areas in the High Current Path as this induces spots with a higher parasitic resistance, resulting in a higher thermal stress.



Figure 7.1: BMS main PCB without balancing capacitor.



Figure 7.2: BMS main PCB with balancing capacitor stacked up.

7.2 Test Setup

The prototype PCB is tested using 16 capacitors ($5600\ \mu\text{F}$) connected in series since they store less energy than a Li-Ion pack and are hence faster to balance. The capacitor voltages are connected to the voltage sense connectors of the PCB. The capacitors are charged to an initial voltage of 3.6 V, which emulates the cells in a Li-Ion cell stack. The Gate Drivers are supplied on their secondary side by the external PSUs. The LV potentials at the outputs of the DC/DC and LDO are supervised by multimeters. The Low Voltage control signals, especially the ϕ and the Multiplexer output signals are directly measured using a two channels of a *TEKTRONIX MDO3054* Mixed Domain Oscilloscope, where the reference potential in this case is the LVGND potential. The other two channels of the oscilloscope are used to measure the output signals of the gate drivers as well as the voltage across the balancing capacitor. Since these signals do not reference to LVGND, they are captured using High Voltage differential probes (*TEKTRONIX THDP0200* 200 MHz). The software is flashed onto the *STM32* using an *STM32F103RB NUCLEO* debugger which is connected to via USB to a laptop. The configuration of the microcontroller interfaces as well as the timer and pinout settings is done using the *STM32CubeIDE* (16.1.1), which is also used to edit the source code of the algorithms described in section 6.3. The test procedure is structured into several unit tests, which include a verification of the ohmic resistance between the High Voltage System and the Low Voltage System to ensure the galvanic isolation between the two systems as documented in section 7.3. The next step contains the measurement of the stack voltage on the input of the LDO of the CVMIC and the DC/DC output voltage (5 V and 3.3 V), serving as a low voltage supply for the control components. The voltage is measured on the stabilisation capacitor of every Low Voltage component and compared with the expected value as per Table 7.2. Care must be exercised to measure the HVS-potentials against the VSS-reference and low voltages against GND.

The next step is to verify the correct reading of the cell voltages using the code explained in section 6.3. Afterwards, the switching units are tested to confirm if current can flow in both directions, allowing arbitrary cell balancing.

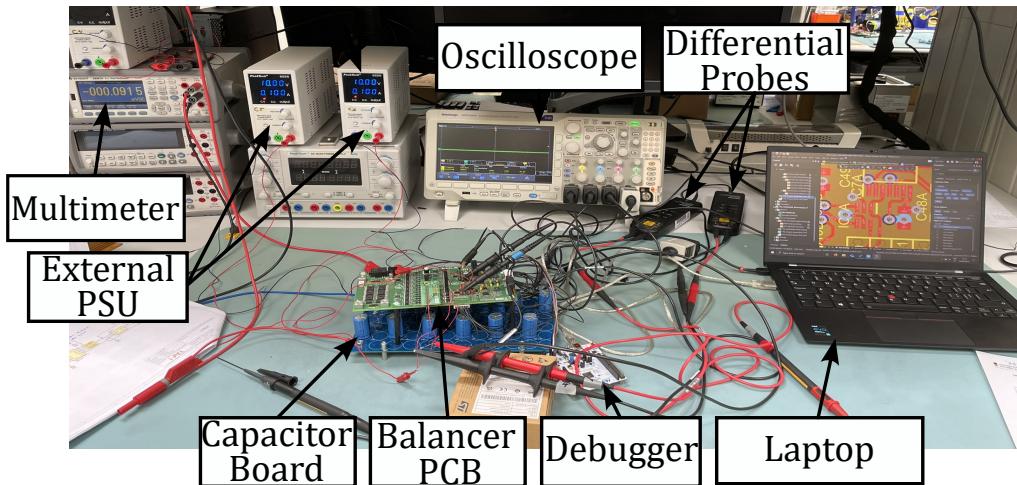


Figure 7.3: Test Setup.

7.3 Galvanic Isolation Verification

The galvanic isolation measurements are performed using specific iso-meters applying voltage pulses close to the maximum system voltage (67.2 V). Caution must be taken when using iso-meters to ensure that components are not damaged by applying a measurement voltage higher than the respective parts' maximum rated isolation voltage. The results of the isolation measurements are documented in Table 7.1.

Table 7.1: Initial resistance measurements.

Point 1	Point 2	Resistance
STACK +	STACK -	358.3 kΩ
STACK +	5 V	>1 MΩ
VSS	GND	>1 MΩ
5 V	GND	1.6 kΩ
3.3 V	GND	4.1 kΩ
PACK+	PACK-	>1 MΩ

7.4 Supply Voltage Verification

Table 7.2 shows the voltages measured across various measurement points to verify the supply of the low-voltage components. Further, the input voltage of the LDO integrated into the Cell Voltage Measurement Integrated Circuit was measured as well as the output voltage to supply the HV side of the I²C isolation chip.

Table 7.2: Initial voltage measurements ($V_{\text{Stack}} = 40.0 \text{ V}$).

Measurement point	Reference potential	Expected voltage	Measured voltage
D1 Anode	VSS	40.0 V	40.0 V
D1 Cathode	VSS	39.55 V	39.4 V
D2 Anode	VSS	38 V to 39.6 V	39.6 V
D2 Cathode	VSS	38.7 V to 39.3 V	39.3 V
Q1 Collector	VSS	39.2 V	39.2 V
REG1	VSS	3.3 V	3.3 V
REG18	VSS	1.8 V	1.8 V
PS1 Pin 14	VSS	40 V	40 V
PS1 Pin 8	GND	5 V	5.028 V
U1 Pin 1	GND	5 V	5.013 V
U1 Pin 3	GND	3.3 V	3.3089 V
IC5 Pin 3	GND	5 V	5.026 V
IC6 Pin 64	GND	3.3 V	3.315 V
IC7 Pin 14	GND	3.3 V	3.315 V
IC8 Pin 5	GND	3.3 V	3.315 V
IC9 Pin 5	GND	3.3 V	3.315 V
IC10 Pin 3	GND	3.3 V	3.315 V
IC2 Pin 24	GND	5 V	5.026 V
IC3 Pin 24	GND	5 V	5.026 V
IC4 Pin 24	GND	5 V	5.026 V
IC15 Pin 3	GND	3.3 V	3.315 V

7.5 Cell Voltage Measurement

The cell voltages gathered using the code described in subsection 6.3.2 and are displayed as 16-bit values in the array `uint16_t CV[]` as documented in Table 7.3. The *TEXAS INSTRUMENTS BQ7695202PFBR* returns the voltages in mV. The measurements were captured using 60 F supercapacitors connected in series.

Table 7.3: 5600 μ F supercapacitor voltages.

Array element	Data type	Value
CellVoltage[0]	uint16_t	3355 mV
CellVoltage[1]	uint16_t	3128 mV
CellVoltage[2]	uint16_t	3345 mV
CellVoltage[3]	uint16_t	3401 mV
CellVoltage[4]	uint16_t	3371 mV
CellVoltage[5]	uint16_t	3155 mV
CellVoltage[6]	uint16_t	3119 mV
CellVoltage[7]	uint16_t	3220 mV
CellVoltage[8]	uint16_t	3159 mV
CellVoltage[9]	uint16_t	3196 mV
CellVoltage[10]	uint16_t	3136 mV
CellVoltage[11]	uint16_t	3125 mV
CellVoltage[12]	uint16_t	3341 mV
CellVoltage[13]	uint16_t	3140 mV
CellVoltage[14]	uint16_t	3019 mV
CellVoltage[15]	uint16_t	3362 mV

7.6 Multiplexer Output Signals

Figure 7.4 shows the output of the Multiplexer when a PWM-signal is applied on the input. The control pins are set to forward the signal to the output channel 1. The neighbouring channels 2 and 3 still experience signal noise, affecting the gate drivers of other switching units, resulting in an unwanted conducting mode. This may damage the switching units if several switching units are in conduction mode at the same time. The problem can be avoided by using pull-down resistors on the output pins of the MUX as stated in Table 9.1.

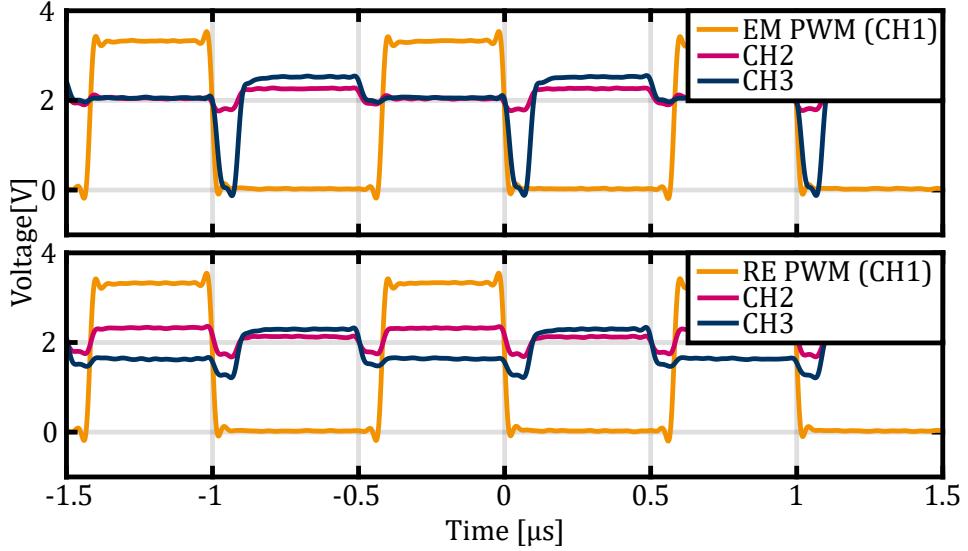


Figure 7.4: Emitter and Receiver Multiplexer signal noise on neighbour output channels.

7.7 Gate Driver Signals and Balancing Capacitor Voltage

Figure 7.5 shows the signals to control the balancing procedure. *INA* is the input PWM signal of channel A of the dual gate driver. *INB* is the input signal input control signal of channel B, which corresponds to the complementary PWM-signal. Both signals have a voltage of 3.3 V for a logical *HIGH* and are pulled to Low Voltage ground potential for a logic *LOW* level. *OUTB* is the gate driver output signal on the output channel B, which is decoupled from the input signals by an inductive Input-to-Output isolation. The voltage level of 10.5 V with reference to the negative cell potential is supplied by an external power supply to prevent the gate driver from entering the Under Voltage Lockout state. The output signal corresponds to the input signal without a significant time delay. U_{Cap} is the voltage across the balancing capacitor. This plot validates the simulation made in Figure 4.5, however, for this specific measurement, no more than one cell was connected to the balancing system to avoid short circuits. To avoid short circuits triggered by the rise or fall time of the MOSFETs and the consecutive time delay leaving potentially two switching units in conducting mode at the same time, a dead-time is integrated in the Pulse Width Modulation signal. Figure 7.6 shows the signal waveforms for a measurement performed with two cells connected to the balancing system. It can be seen that the voltage across the balancing capacitor behaves the same way as in Figure 7.5, demonstrating the working principle and proving the concept of balancing.

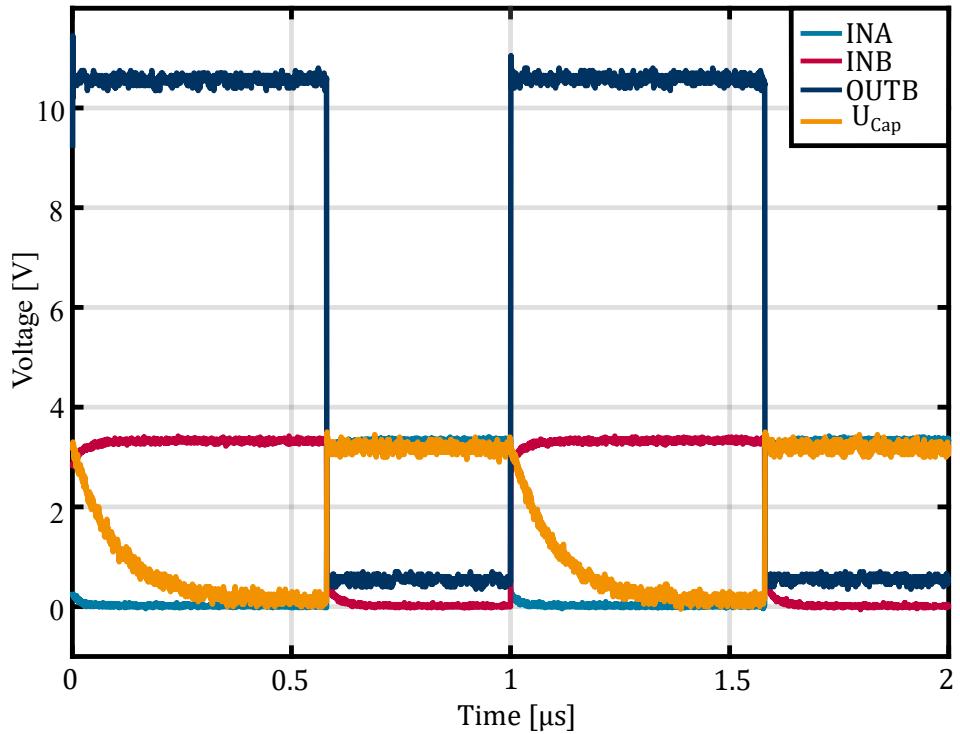


Figure 7.5: Gate Driver input signals INA and INB, corresponding Gate Driver output signal OUTB and balancing capacitor voltage U_{Cap} .

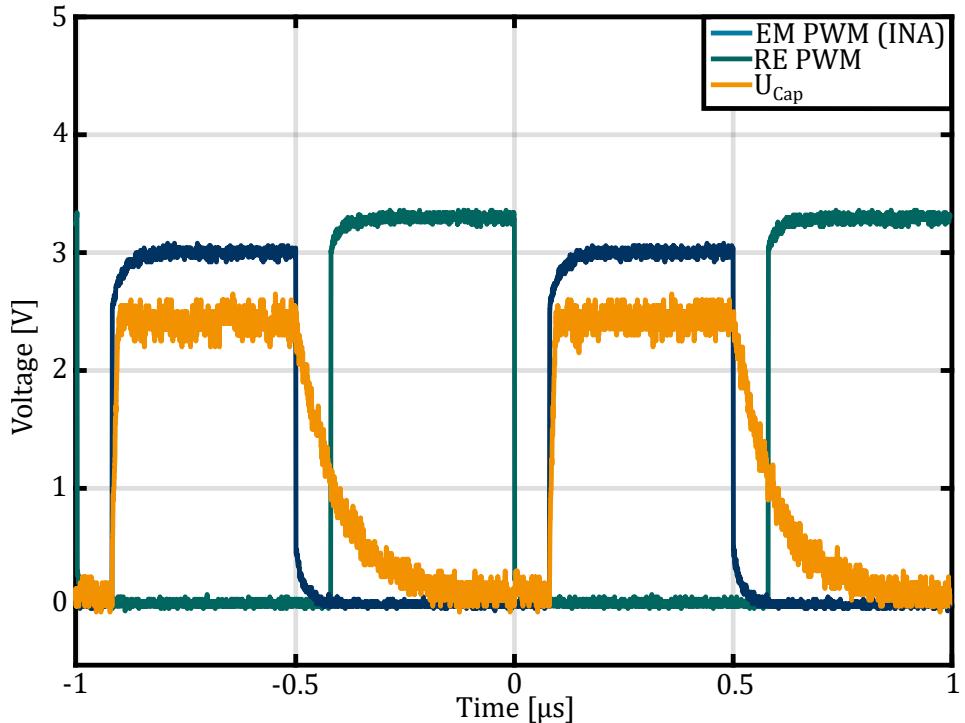


Figure 7.6: Emitter PWM-signal (INA) and Receiver PWM signal with dead-time in between. Balancing capacitor voltage U_{Cap} .

8 Conclusion

Extensive research on state-of-the-art battery management and balancing technologies was performed in chapter 2 and chapter 3. Further, simulations on balancing efficiency and speed were conducted using *PLECS* and *MATLAB/SIMULINK*. Out of the analysis and simulation results, it was deduced that arbitrary cell balancing, allowing to balance each cell with any other cell inside a stack, would lead to faster balancing time and less charge movement, resulting in an overall more efficient voltage equalisation. Based on this insight, a concept was elaborated for the implementation of a single switched capacitor balancing system using bidirectional semiconductor switches to allow the connection of each cell to a balancing grid. Further, a control algorithm was developed to reduce the movement of charge inside a stack, allowing faster balancing while reducing ohmic losses.

A prototype system for a 16s Li-Ion battery stack was designed and constructed with the option to interchange the balancing energy storage element by stacking it up on a pin-header. The software was designed to read the voltage of each cell in every loop cycle using serial communication. The battery stack and the balancing circuit are fully galvanically isolated from the low-voltage control system. The switching units are designed to act as stand-alone units by supplying the secondary side of the gate driver using the voltage of the cell in question. This allows for the potential integration of the switch into an ASIC device. Even if current only flowed in one direction through the bidirectional switch, this result can still be accepted as validation of the previously made simulation, proving the concept of balancing using bidirectional switches. Hence, the operation principle, as analysed during the simulation, was validated by measurement.

This demonstrates that the proposed balancing system offers the possibility for fast and efficient battery balancing, albeit at a slightly higher implementation complexity and cost. It could further be validated that the ability to balance arbitrary cells is a significant advantage compared to adjacent cell balancing. Generally, the considerable efficiency advantage of active balancing topologies compared to passive or dissipative technologies was demonstrated. The comparison of both implementation topologies showed that passive balancing techniques have a significant cost and hardware complexity advantage.

9 Outlook

9.1 Known Hardware Issues

The issues, according to Table 9.1, were identified during hardware testing of the revision *HW.RV1-1*, see appendix A, of the PCB described in chapter 5 up to the submission date of the present thesis.

Table 9.1: Hardware issues of *HW.RV1-1*.

Nb.	Sheet name Sheet number	Part	Description	Type
1	CV Measurement Sheet 4 of 14	Q1	Add 100 Ω base resistor	Bug
2	PSU CAN Sheet 6 of 14	PS1 U1	Add 5 V and 3.3 V LEDs on DC/DC and LDO output pins	Enhancement
3	CV Measurement Sheet 4 of 14	HY1	Add 1.5 k Ω Pull-Up resistors on isoSDA and isoSCL lines	Bug
4	CV Measurement Sheet 4 of 14	HY1	Change Pull-Up resistors on SDA and SCL lines	Bug
5	PCB Layout	C14 C15	Move position in layout for better soldering	Enhancement
6	CV Measurement Sheet 4 of 14	HY1	Change ISO1541 to ISO1540	Bug
7	Connector & HCP Sheet 13 of 14	J1	Mirror pins	Bug
8	ISO 2-CH Gate Driver Sheet 11 of 14	IC10	Change supply voltage at the secondary side to $4 \cdot V_{Cell}$	Bug
9	PCB Layout	C42 C57	Move closer to gates	Enhancement
10	Bidirectional Switch Sheet 12 of 14	IC12 IC14	Increase capacity	Enhancement
11	Bidirectional Switch Sheet 12 of 14	IC10 IC13	Add Pull-Up Resistor between Low-Side gate and Gate Driver supply	Bug
12	Bidirectional Switch Sheet 12 of 14	IC13 IC14	Mirror N-Channel MOSFETs	Bug
13	STM32F103RBT6 Sheet 7 of 14	IC6	Add digital input for general purpose button	Enhancement
14	MUX Sheet 5 of 14	IC2 IC4	Add Pull-Down resistors to outputs of MUX	Bug
15	Bidirectional Switch Sheet 12 of 14	IC11 IC12 IC13 IC14	Reduce voltage drop-down caused by body diode	Enhancement
16	Connector & HCP Sheet 13 of 14	F1	Select higher interrupt current	Safety critical enhancement
17	Bidirectional Switch Sheet 12 of 14	IC11 IC12 IC13 IC14	Select switches with matching switching behaviour	Enhancement
18	Bidirectional Switch Sheet 12 of 14	IC11 IC12 IC13 IC14	Select switches with lower body diode drop-down voltage	Enhancement

9.2 Hardware Improvements

The prototype designed during the present thesis can only balance cells within the same stack. However, large Energy Storage System are often made up of several stacks connected in series. Even if the cells inside a stack are balanced to the same voltage, differences in State of Charge and cell stack voltages may occur that the presented system can currently not balance. To comply with this requirement, the prototype must be redesigned to be daisy-chained, and a balancing connection between two stacks can be established. This would end up in a master-slave configuration where the master unit contains the *STM32* controller and is connected by an isolated serial communication protocol to the slave devices containing only the Cell Voltage Measurement Integrated Circuit and the switching units.

Further research on the switching topology can be done to reduce the number of required parts for the implementation.

The single switched capacitor topology can be developed into a double-tiered one, enabling several cells to be balanced simultaneously.

The current prototype can not balance voltage differences lower than 0.8 V since the drop-down voltage of the body diode from the N-Channel and P-Channel does not enable current flow below this voltage. As stated by issue number 18 in Table 9.1, further prototypes should aim to use FETs with a low drop-down body diode.

9.3 Software Improvements

The initial version of the software running on the *STM32* microcontroller is designed to comply with the essential requirements and run the control algorithm as presented in section 6.3. To make the system more efficient, a sleep mode should be implemented that is entered when the cells are balanced and the ESS is under no external load. This can be achieved by putting the Cell Voltage Measurement Integrated Circuit into the available sleep mode and only periodically measuring the cell voltages.

An optimisation of the switching frequency and balancing capacity may be done to improve the balancing efficiency further. Using a higher capacity allows for the transfer of more charge per cycle; however, higher capacitance results in higher charging currents, raising the ohmic losses induced by the balancing current. Further, the higher capacity takes more time to charge and discharge, resulting in a lower switching frequency. This problem requires further research by using mathematical optimisation methods.

The reliability of the balancing system can be improved by adjusting the PWM-properties, especially the dead-time, which is essential to avoid short circuits by connecting two cells with different voltages directly in parallel over the balancing grid. Rising and falling time of the switches must be taken into account to optimise the dead-time, this can be enhanced by selecting N-Channel and P-Channel MOSFETs with matching properties.

9.4 ASIC Design

The presented bidirectional switching unit is potentially suited for the integration into an ASIC. The circuit can be used as a stand-alone unit, which is supplied by the voltage

of the cell to which it is connected. Integrating the switching unit into a semiconductor, including the gate driver circuit, would significantly reduce the hardware complexity and the required PCB space. The device can be controlled by a single digital pin, putting the bidirectional switch into conducting or blocking mode.

Appendix

A - Battery Management System Circuit Diagram

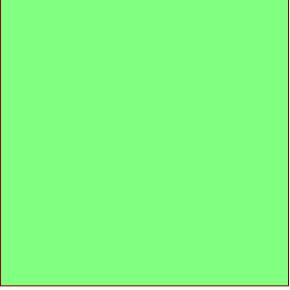
BATTERY MANAGEMENT SYSTEM

UNIVERSITY OF INNSBRUCK
INNSBRUCK POWER ELECTRONICS LABORATORIES

HESS4MRA

REVISION	DATE	NAME	CHANGES
1-1	23/09/2024	P. Mootz	RELEASE HW.RV1-1

TOP LEVEL SCHEMATICS
SCH_CTRL.SchDoc



LEGEND:

	MOST POSITIVE CELL TAB
	ISOLATED 5V FROM DCDC
	LDO FROM 5V TO 3V3
	POWER GROUND (PACK-)
	VSS (CONNECTED VIA 0ohm to PGND)
	ISOLATED SIGNAL GROUND



Mechanical
SCH_Mechanical.SchDoc

Remarks:

BALANCER GRID AND STORING ELEMENT ARE
IMPLEMENTED ON A SEPARATED PCB. SEE PROJECT BalancingCap.

MINIMUM SPACING BETWEEN HIGH AND LOW VOLTAGE ON PCB: 1.6mm

BALANCER GRID IS DONE ON SEPARATE BALANCER PCB
Date: 19/12/2024
Designed by: P. Mootz
Drawn by: P. Mootz
Checked by: A. J. Hanschek
Approved by: Univ. Prof. Dr. Petar J. Grbović

Project Name: i-PEL_Project_HESS4MRA_BMS_RV01.PjPcb
Sheet Name: COVER PAGE

Document Name: i-PEL_Project_HESS4MRA_BMS_CSC_RV01.SchDoc
Revision: 1-1 Sheet: 1 of 14 Status: Preliminary

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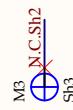
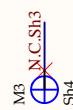
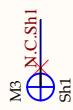
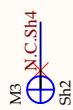
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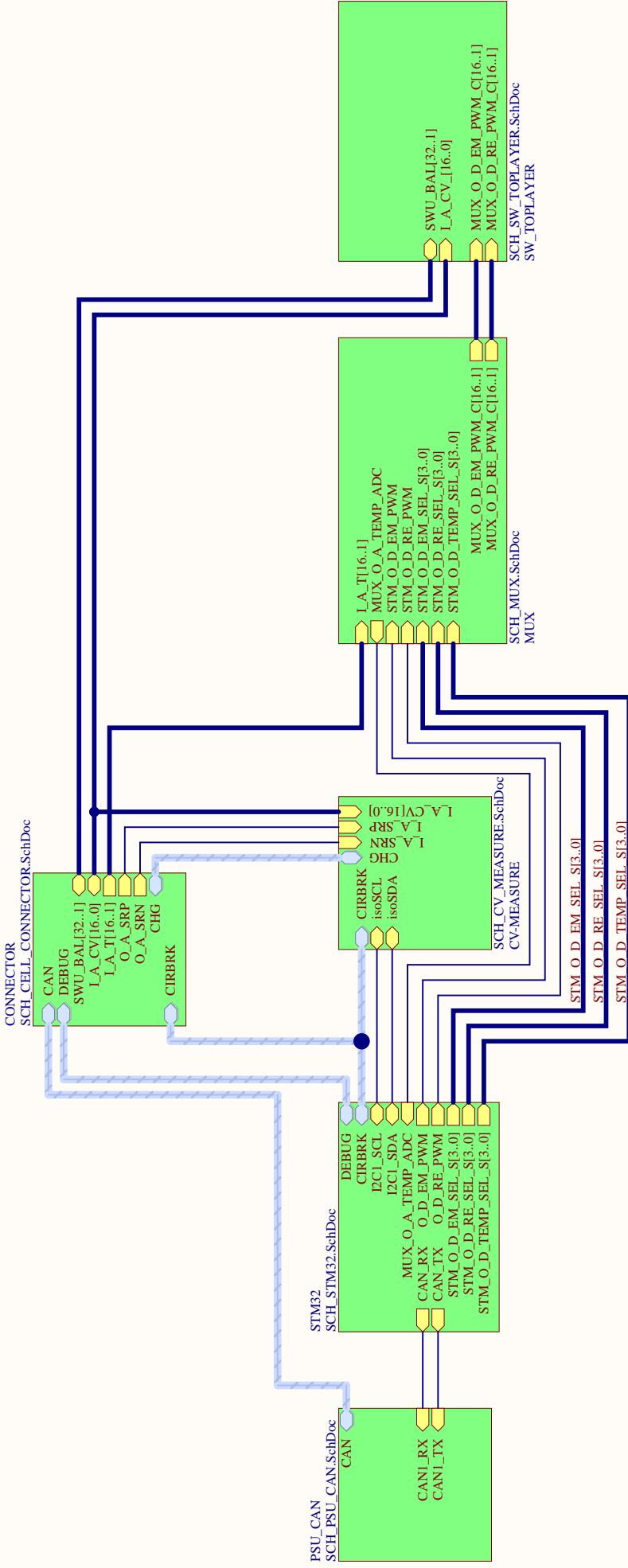
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PCB Dimensions: MAX 205x120mm

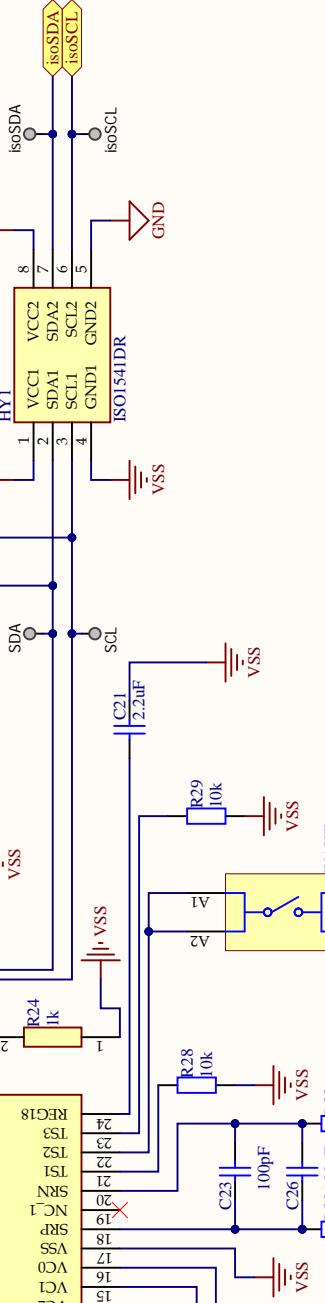
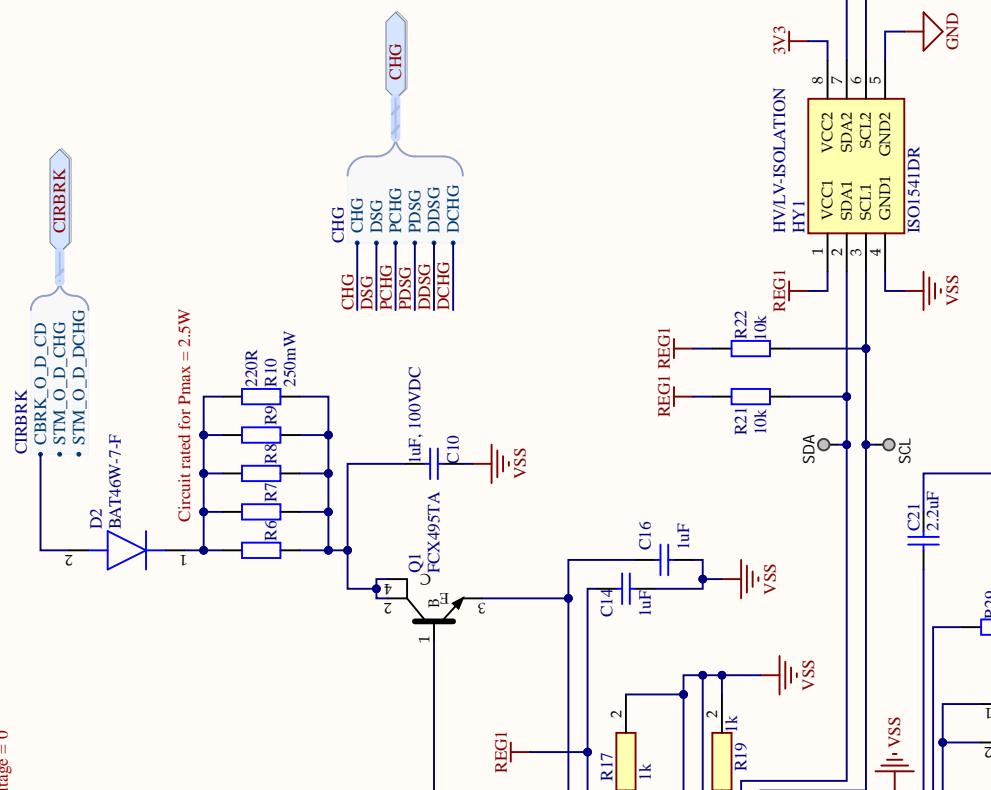
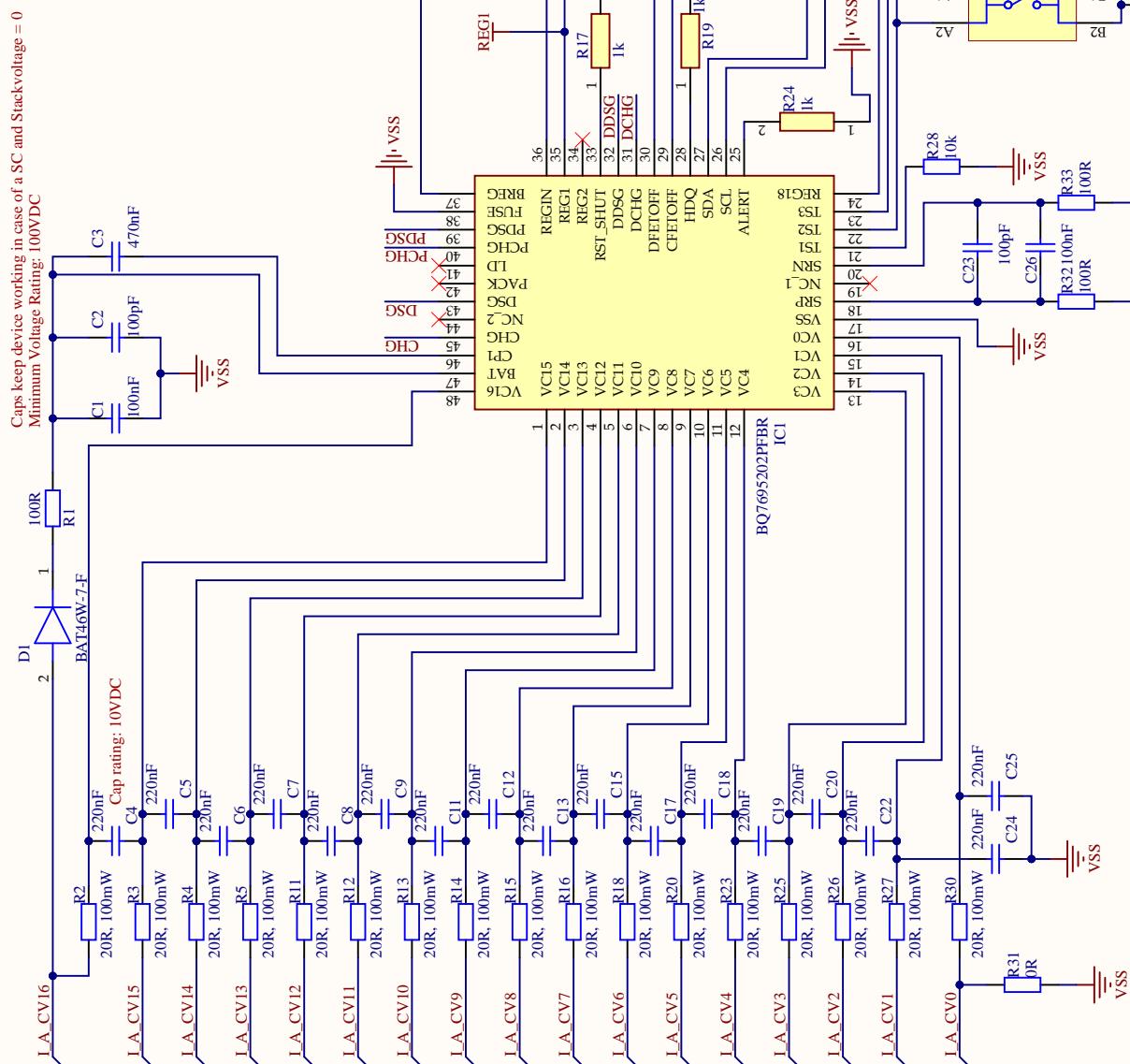
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Drawn by:	P. Mootz		
Checked by:	A. J. Hanschek		
Approved by:	Univ. Prof. Dr. Petar J. Gribović		
i-PEL		Document Name:	SCH_Mechanical.SchDoc
Innsbruck Power Electronics Lab.		Revision:	1-1 Sheet: 2 of 14 Status: Preliminary
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TOP LEVEL SCHEMATICS



Date:	23/11/2024	Project Name: i-PEL_Project_iHESSAM/R&D/RV01_PrijbC													
Designed by:	P. Mootz	Sheet Name:													
Drawn by:	P. Mootz	TOP LEVEL SCHEMATIC													
Checked by:	A. J. Hanschek														
Approved by:	Univ. Prof. Dr. Peter J. Grbović														
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Drawn by:	P. Mootz		
Checked by:	A. J. Hanschek		
Approved by:	Univ. Prof. Dr. Petar J. Grbović		
TOP LEVEL SCHEMATICS		Document Name:	SCH_CTRL.SchDoc
		Revision:	1-1 Sheet: 3 of 14
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Cell Voltage Measurement

Variant: [No Variations]

Status: Preliminary

Sheet: 4 of 14

Revision: 1-1

Document Name: SCH_CV_MEASURE.SchDoc

Project Name: i-PEL_Project_HESS4MRA_BMS_RV01.PrfPcb

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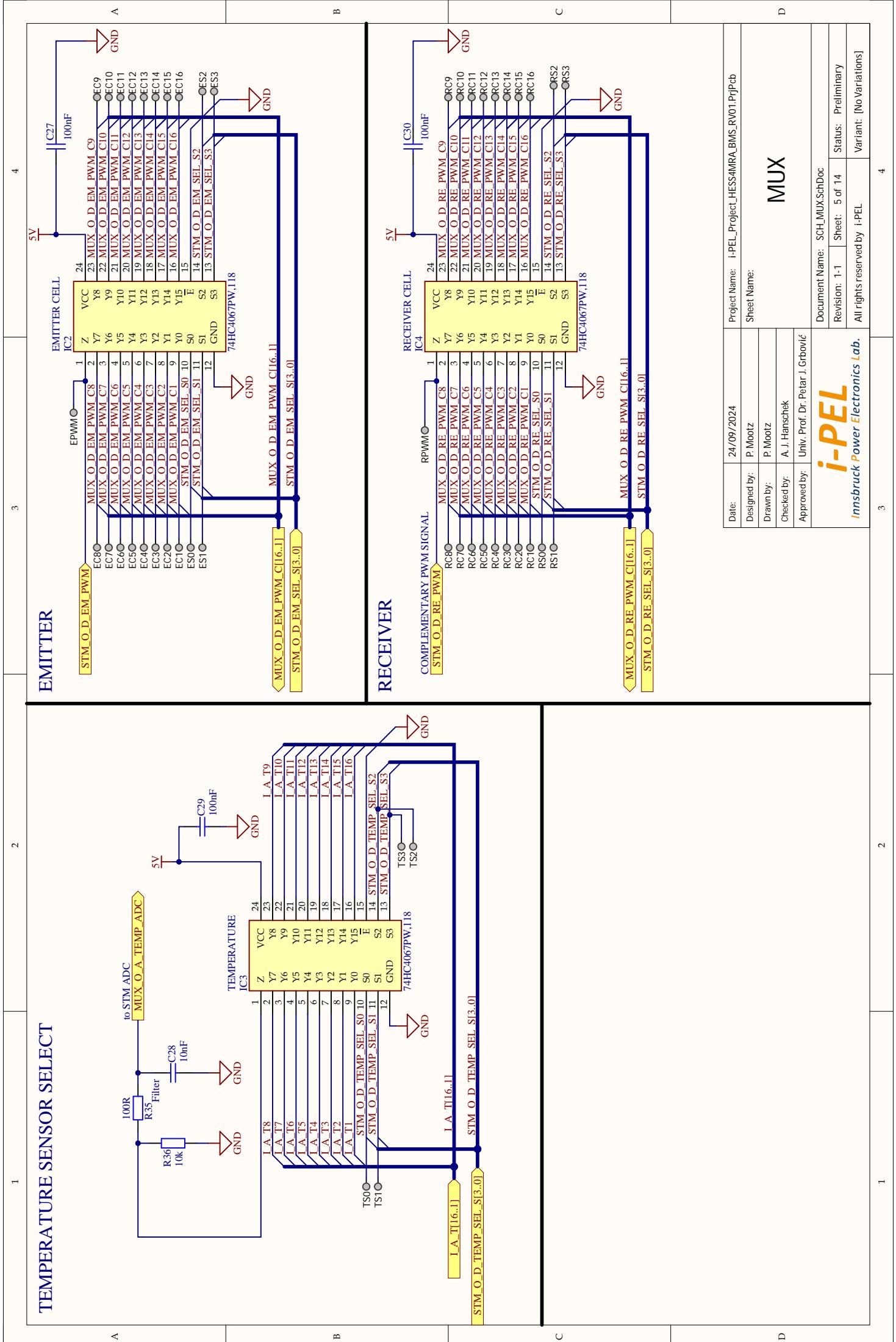
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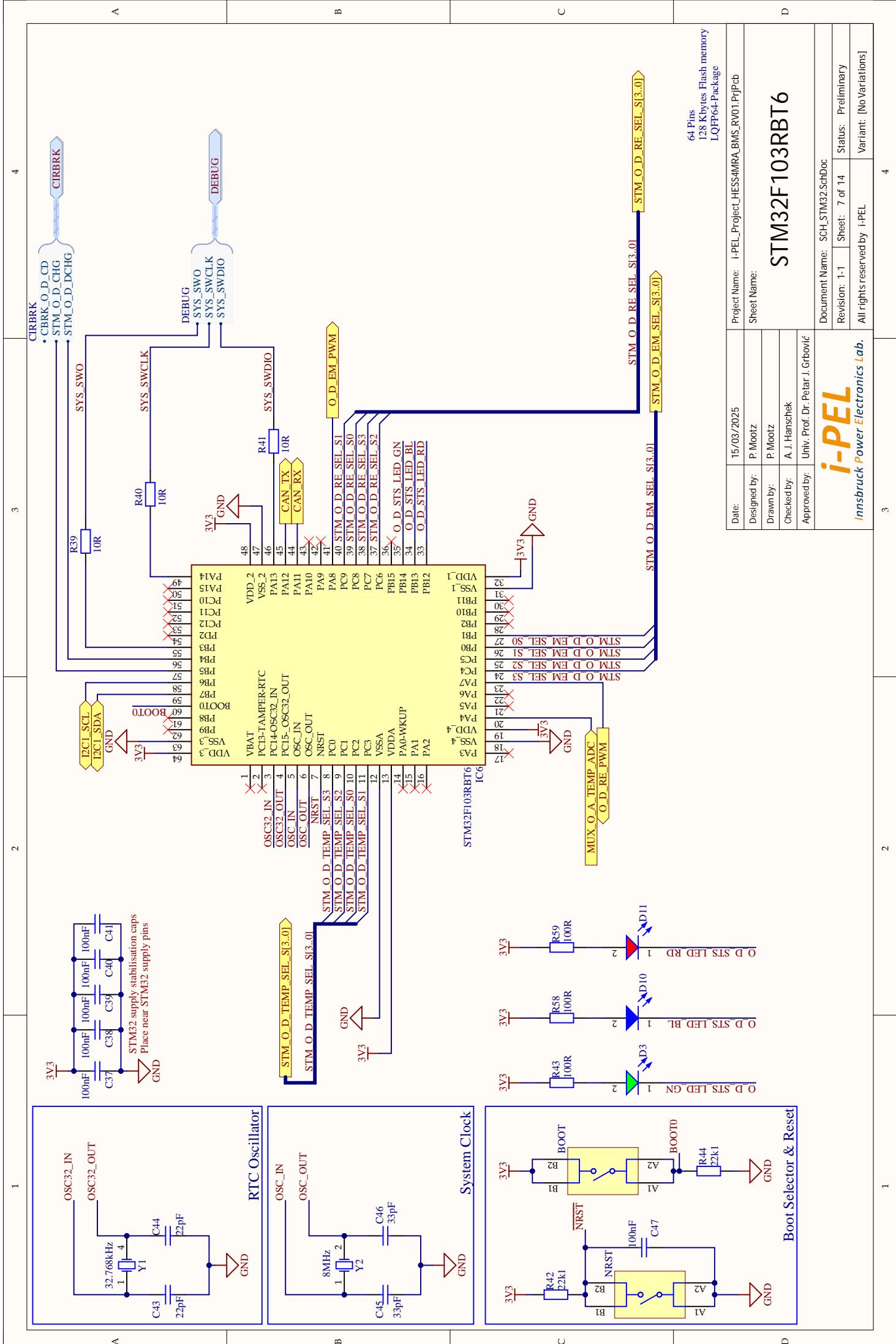
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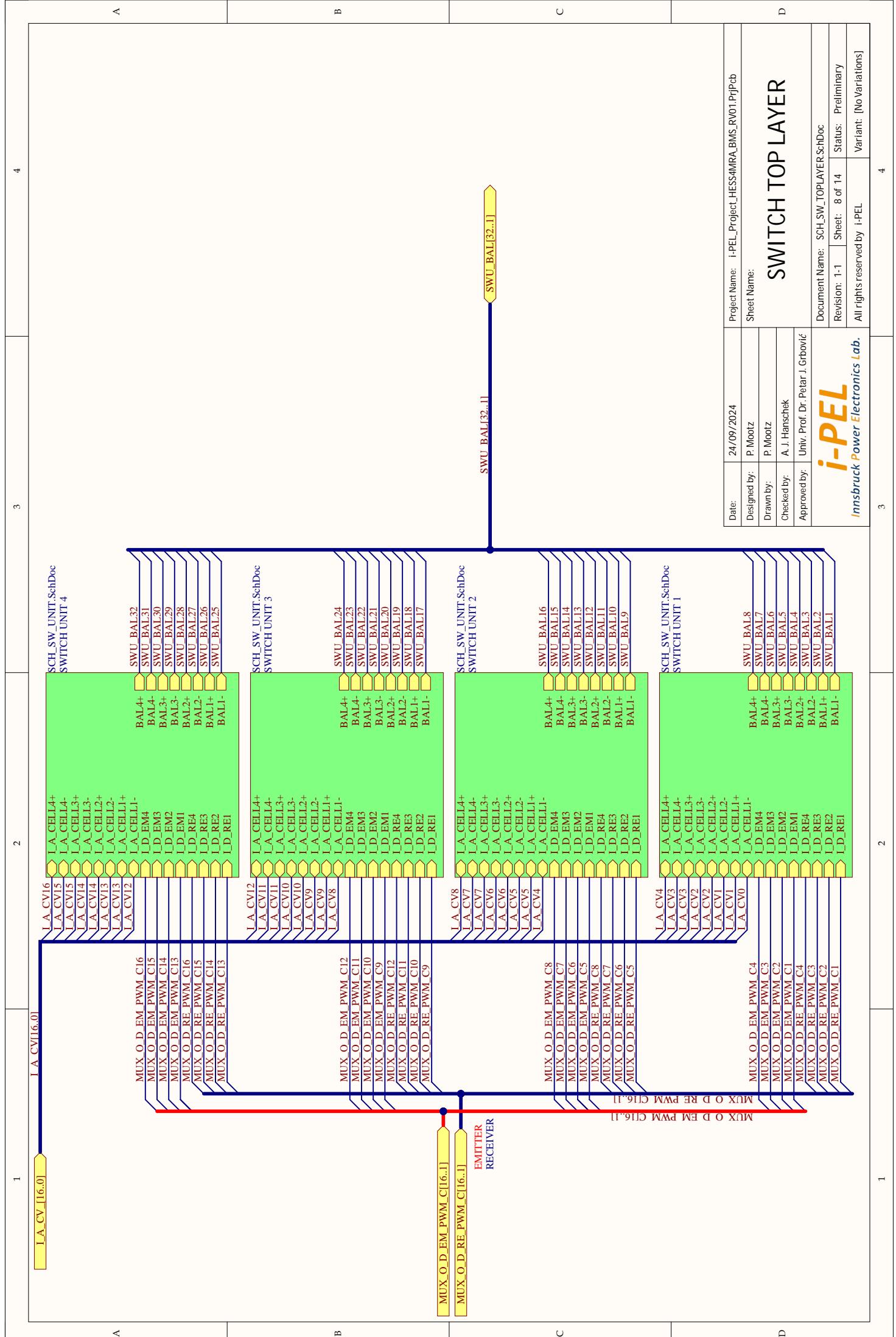
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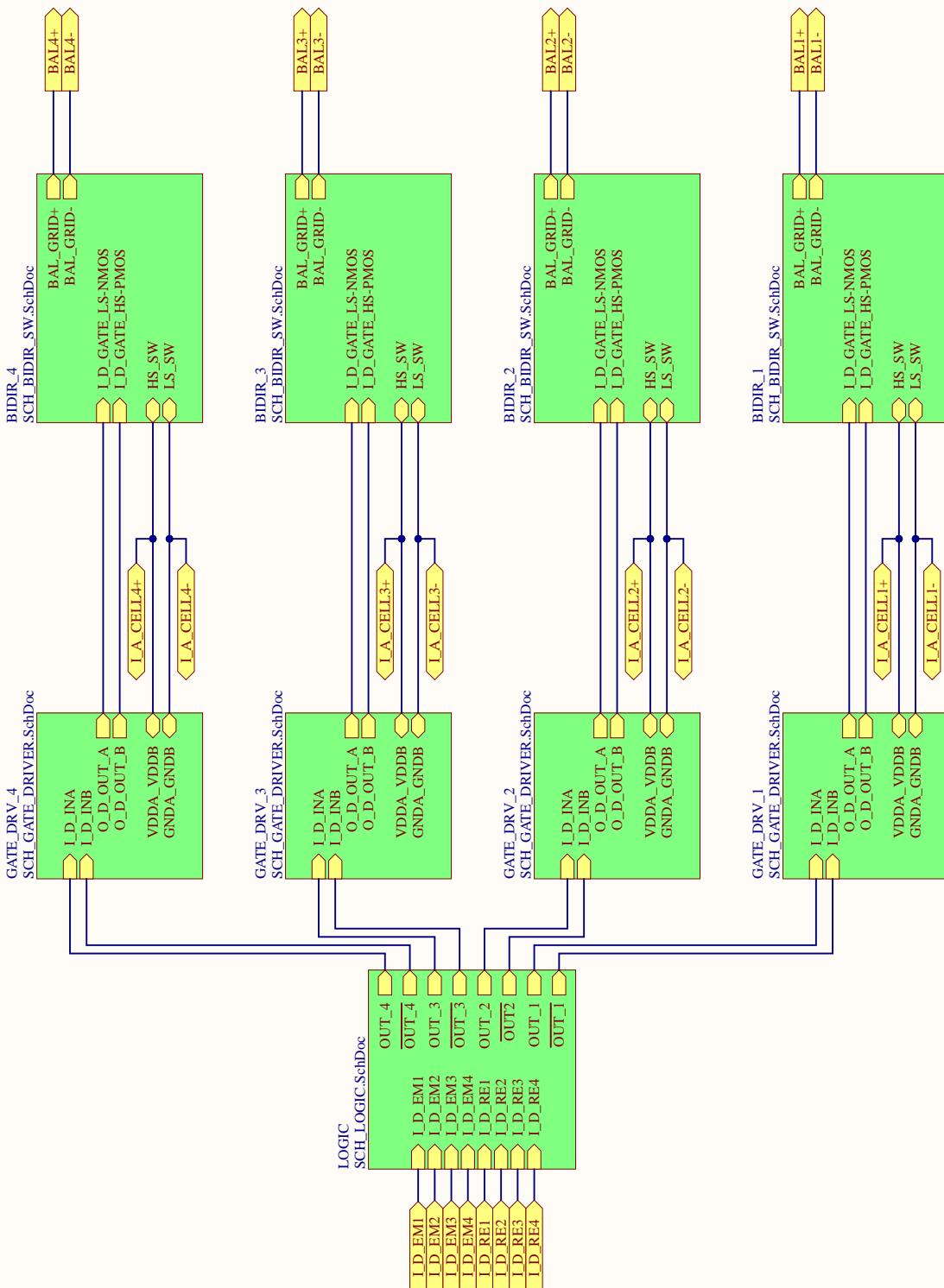
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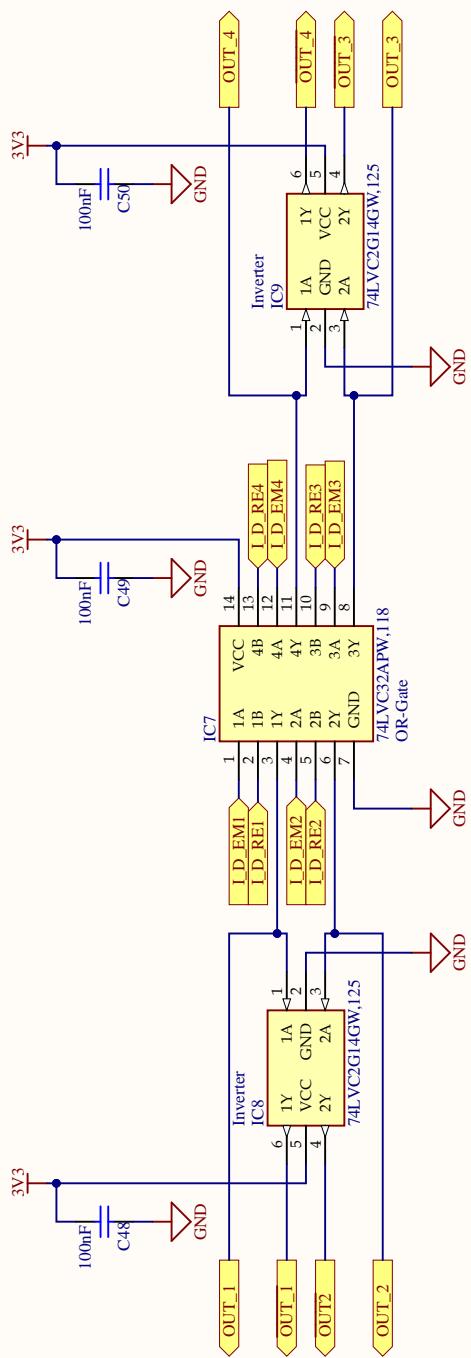






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Designed by:	P.Mootz	Sheet Name:		
Drawn by:	P.Mootz	SWITCH UNIT		
Checked by:	A.J.Hanschek			
Approved by:	Univ. Prof. Dr. Peter J. Gribovici			
i-PEL Innsbruck Power Electronics Lab.				
Document Name: SCH_SWIUNIT.SchDoc				
Revision: 1-1 Sheet: 9 of 14 Status: Preliminary				
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Date:	24/09/2024	Project Name: i-PEL_Project_HESSAMRA_BIMS_RV01_PjPcb		
Designed by:	P. Mootz	Sheet Name:		
Drawn by:	P. Mootz			
Checked by:	A. J. Harschek			
Approved by:	Univ. Prof. Dr. Petar J. Gborović			
LOGIC				
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		Document Name: SCH_LOGIC.SchDoc		
		Revision: 1-1	Sheet: 10 of 14	Status: Preliminary
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Approved by: Univ. Prof. Dr. Petar J. Grbović

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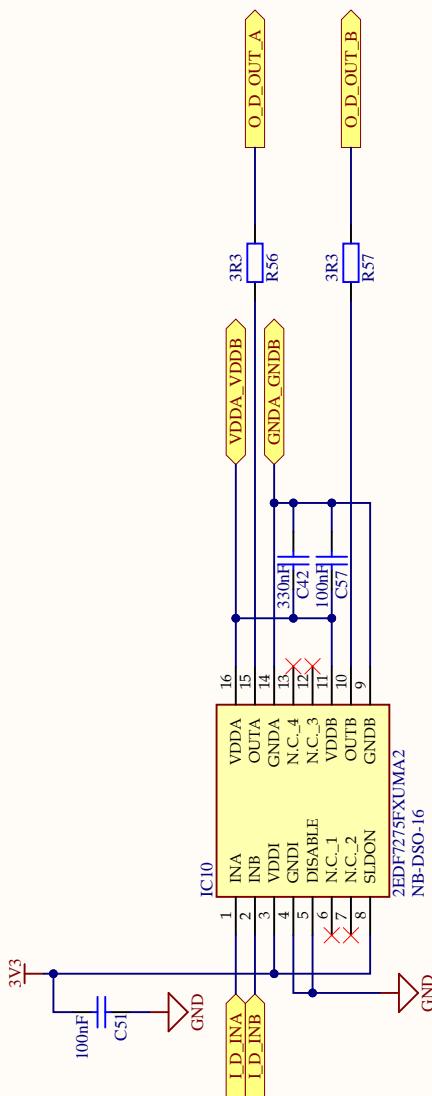
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Designed by:	P. Mootz	Sheet Name:	
Drawn by:	P. Mootz		
Checked by:	A. J. Hanschek		
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ISO 2-CH GATE DRIVER

Document Name:	SCH_GATE_DRIVER.SchDoc
Revision:	1-1
Status:	Preliminary

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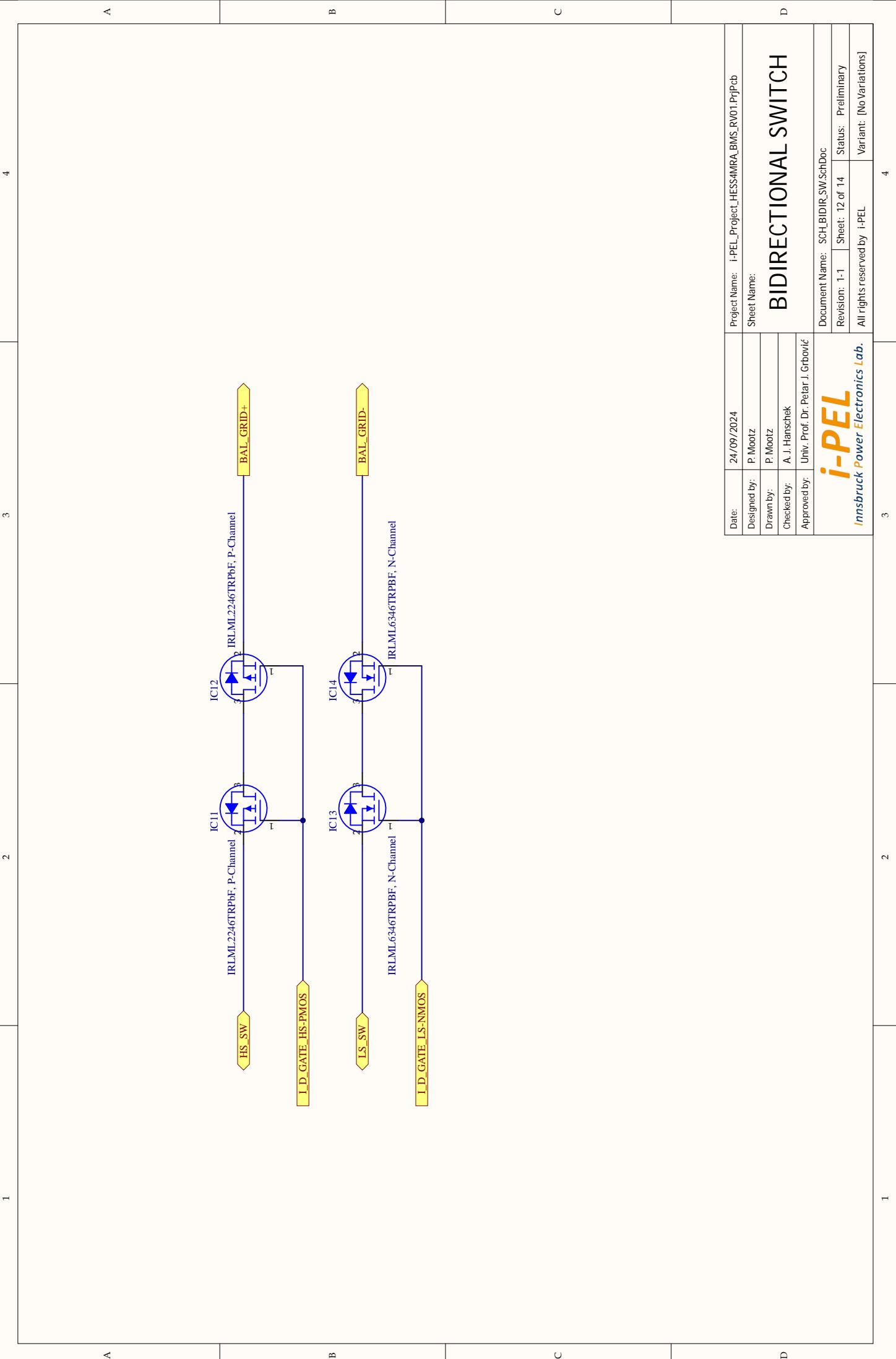
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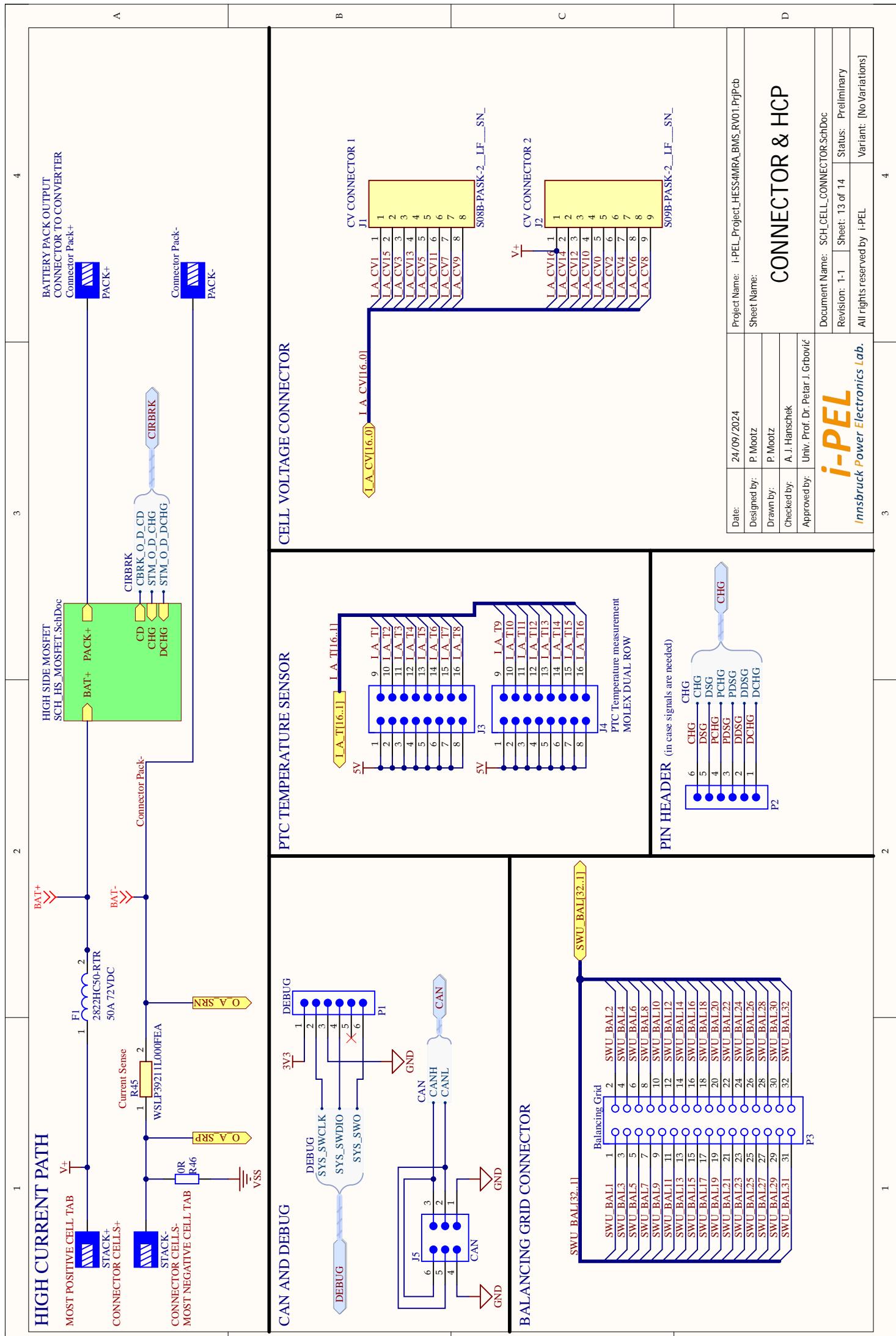
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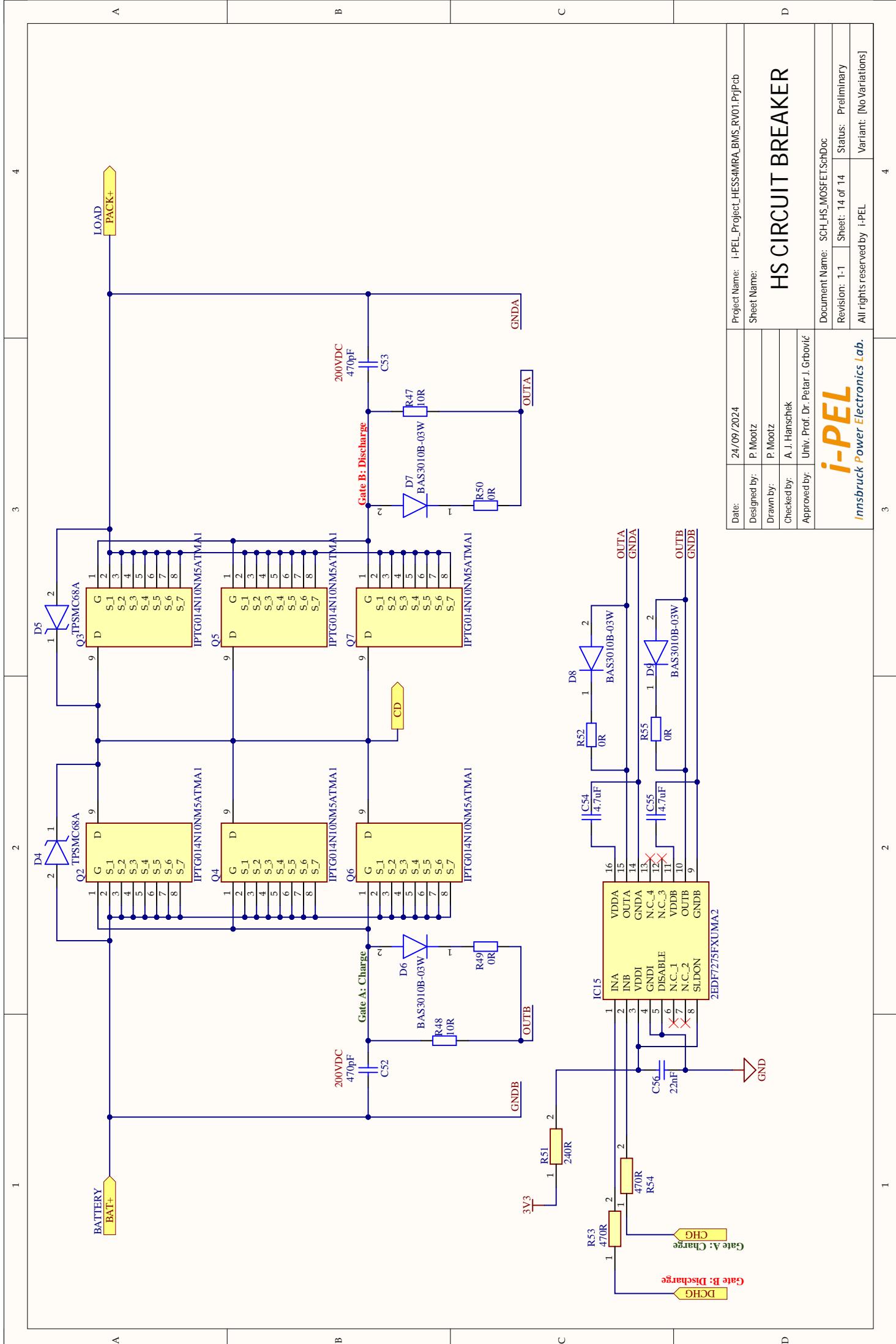
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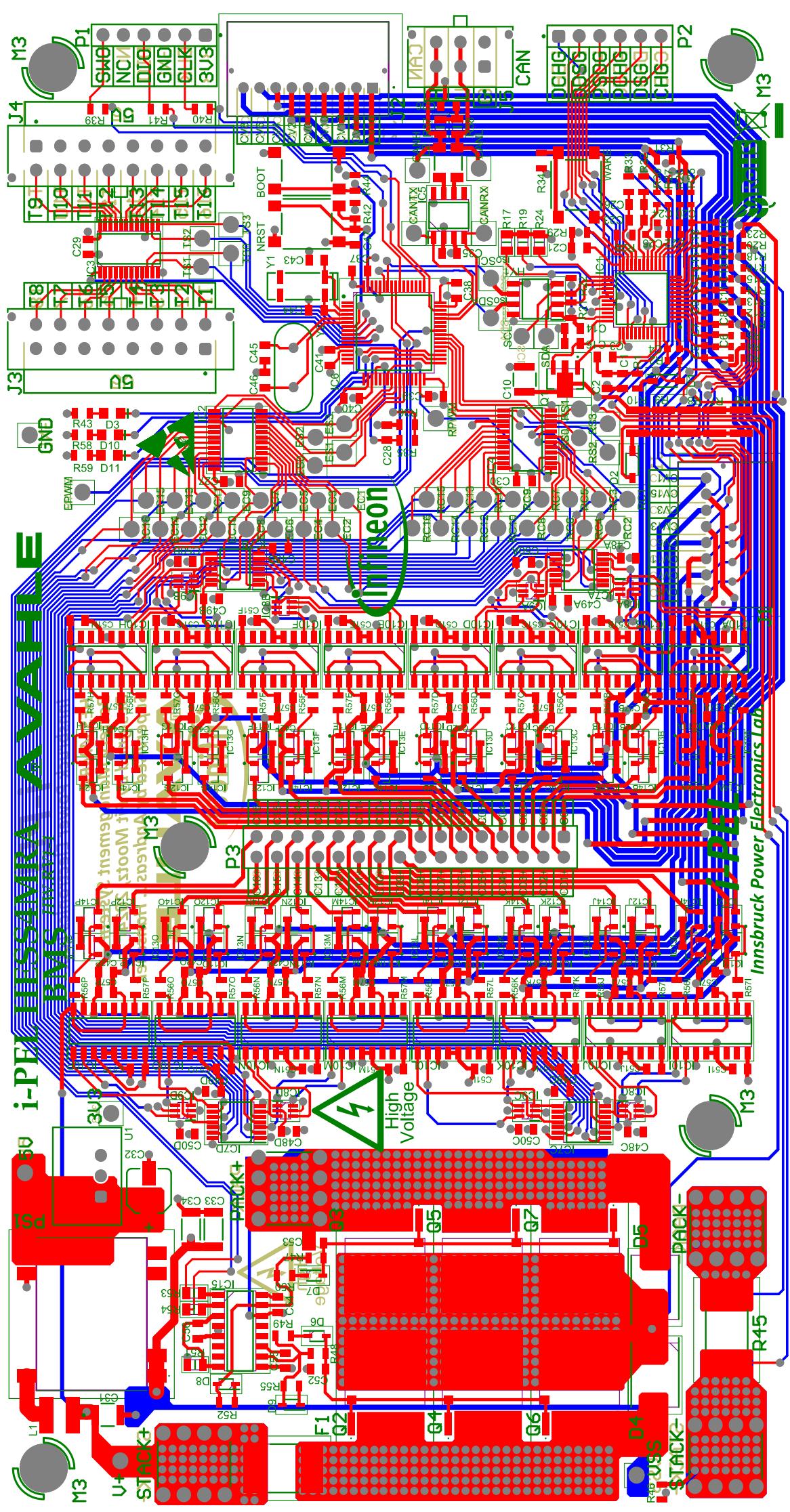
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B - Balancing Capacitor Circuit Diagram

HESS4MRA BALANCING CAPACITOR

UNIVERSITY OF INNSBRUCK
INNSBRUCK POWER ELECTRONICS LABORATORIES

REVISION	DATE	NAME	CHANGES
1-1	09/09/2024	P.Mootz	Initial Schematics

Balancing Capacitor
BalancingCap.SchDoc

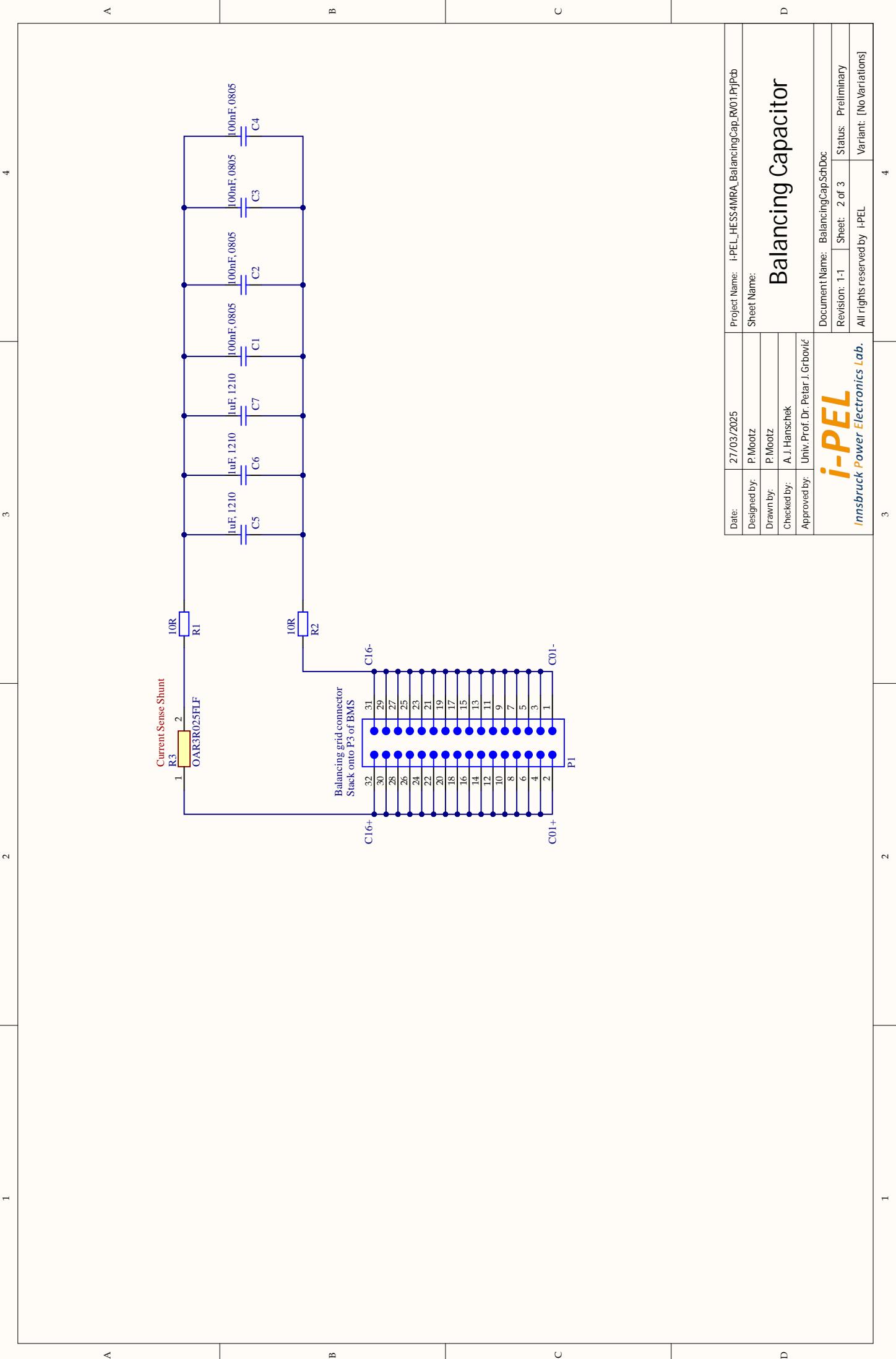
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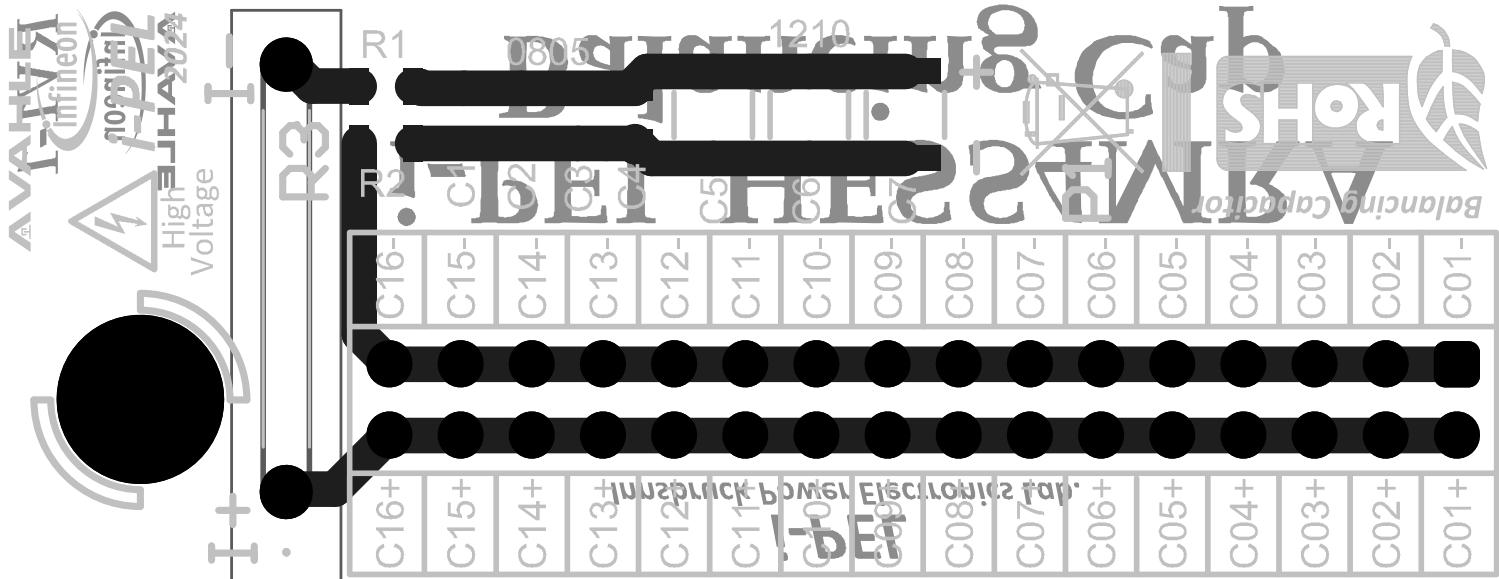
Date: 09/09/2024
Designed by: P.Mootz
Drawn by: P.Mootz
Checked by: A.J.Hansschek
Approved by: Univ. Prof. Dr. Petar J. Grbović

Project Name: i-PEL_HESS4MRA_BalancingCap.RV01.PjPdb
Sheet Name:

Top Level Schematics

Document Name: i-PEL_HESS4MRA_BalancingCap.RV01.SchDoc
Revision: 1-1 Sheet: 1 of 3 Status: Preliminary
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C - Publication

Improved control algorithms for battery management systems to reduce redistribution of charge within energy storage systems

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*Innsbruck Power Electronics Lab. (i-PEL), University of Innsbruck, Innsbruck, Austria

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Abstract—With the growing reliance on lithium-ion batteries (LIBs) for energy storage systems (ESS) in various applications, addressing cell imbalance becomes crucial for enhancing operational efficiency, lifespan, and safety. Although several balancing topologies are available, depending on their energy storage element, balancing speed, and efficiency can further be improved by software control. This paper proposes a balancing control method based on a direct cell-to-cell (DC2C) single-switched capacitor that aims to reduce the redistribution of charge by balancing each cell to the average stack voltage. A proof of concept is demonstrated through simple *Matlab* scripts. The control strategy is further elaborated through simulations using a 1s4p battery stack implemented in *PLECS Blockset* and *Simulink*. An overall energy efficiency of 99.36 % was achieved during simulations.

Index Terms—Active balancing, battery management system, switched capacitor, simulink, control system

I. INTRODUCTION

The demand for energy storage systems (ESS) is steadily increasing due to the rising electrification of transportation in various domains, including electric vehicles (EV) and autonomous robotic systems as the emerging backbone of modern logistics. The safe operation of electrochemical-based storage systems, especially those rated for high power and energy densities, necessitates reliable battery management systems. Due to their high reliability and energy density, lithium-ion batteries (LIBs) are the preferred choice for ESS across mobility and smart grid applications [1]. To meet the requirements for energy storage, low-voltage LIBs are connected in series and parallel configurations to achieve the desired stack terminal voltage and energy capacity. However, chemical differences resulting from manufacturing imperfections, such as coating, winding, and electrolyte filling, as well as temperature variations and current effects during operation, lead to imbalances across the stack. These imbalances affect the state of charge (SoC) of the cells and result in inconsistent life-cycle behavior [2], [3].

Cell imbalance directly impacts the total capacity of a battery stack, as cells with the lowest state-of-health (SoH) restrict the operation of the ESS within its optimal range. These cells reach the upper/lower voltage limit before others, requiring an early termination of the charging/discharging

process. Consequently, a specific amount of energy and storage capacity remains unused during operation, which in turn shortens the cycle life of the battery pack [4]. Various hardware and control topologies for achieving cell balancing have been proposed [2], [5]–[7], differing in hardware complexity and control strategies, as shown in Figure 1. Existing literature

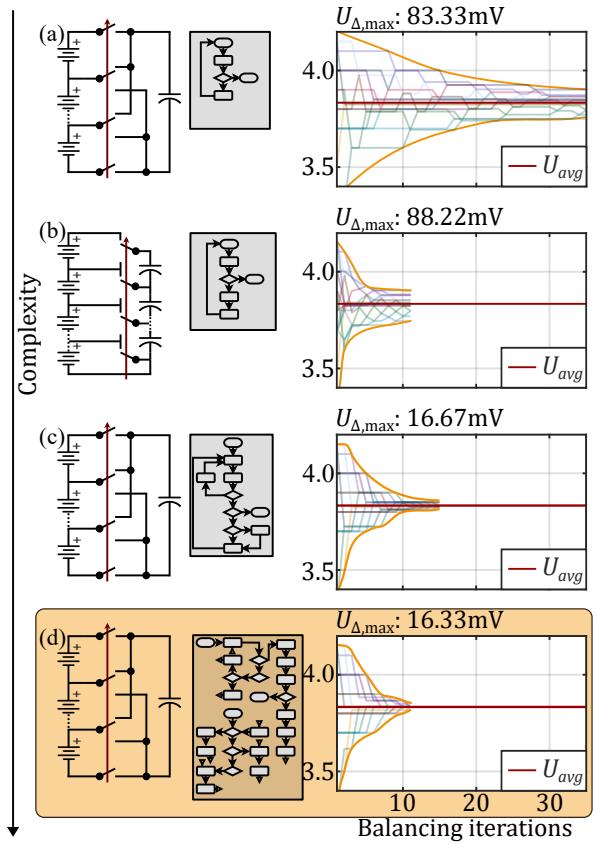


Fig. 1: Hardware and control complexity of 4 balancing strategies (a) Adjacent cells, single switched capacitor, (b) Adjacent cells, simultaneously switched capacitors, (c) Arbitrary cells, single switched capacitor, (d) Arbitrary cells, single switched capacitor and PWM-control with a predefined target voltage

primarily focuses on hardware implementation concepts for

balancing topologies [2], [5], [6]. While some hardware considerations are discussed in section II, this work aims to demonstrate that the efficiency of individual circuits can be further enhanced by applying advanced control strategies to the switching elements of existing hardware. This approach minimizes the redistribution of charge and reduces total power loss attributable to copper resistance, internal cell resistance and switching losses.

An analysis of four balancing control concepts is presented in Figure 1, where initial simulations were conducted using simplified *Matlab* scripts without the implementation of specific balancing hardware. The algorithm depicted in Figure 1 (d), is elaborated in section III and aims to balance a stack more efficiently by charging or discharging cells to a specified voltage during the balancing process. The selection of the target voltage can vary according to the operation state of the ESS but typically could be the average cell voltage of a stack or a higher voltage if the ESS is in a charging state. The control system is demonstrated using a battery stack modeled in *PLECS Blockset* within a *Simulink* environment, with a controller implemented in *Matlab*. An evaluation of the obtained simulation results is discussed in section IV.

II. LITERATURE REVIEW OF CELL BALANCING TOPOLOGIES AND CONTROL STRATEGIES

A. Hardware Review

Balancing strategies are generally categorized into passive and active topologies. The simplest approach to stack balancing is the removal of excess charge from higher-charged cells through heat dissipation using shunt resistors. Passive topologies benefit from low-cost hardware implementation, as fixed resistor and zener-diode concepts do not require external control and can act as standalone units. However, these strategies significantly reduce the overall efficiency of the ESS and accelerate temperature degradation. The rate of heat generation follows Joule's Law, as described in Equation 1, where I_{balance} represents the current through the balancing circuit, R_{balance} is the balancing resistor, and R_{par} represents the series parasitic resistance of the circuit. This includes the internal resistance of the cell, the resistance of pn-junctions of the switches, and the copper resistance of the conductor [7]. Since passive balancing topologies only permit discharging of cells, the final State of Charge (SoC) of the balanced ESS equals that of the lowest charged cell. The total energy loss of the balancing cycle over a time span $t \in [t_{\text{start}}, t_{\text{end}}]$ is given by Equation 2.

$$P_{\text{dissipation}} = I_{\text{balance}}^2 \cdot (R_{\text{balance}} + R_{\text{par}}) \quad (1)$$

$$E_{\text{dissipation}} = \int_{t_{\text{start}}}^{t_{\text{end}}} I_{\text{balance}}^2 \cdot (R_{\text{balance}} + R_{\text{par}}) dt \quad (2)$$

Active balancing circuits transfer charge from higher to lower charged cells with reported efficiencies of up to 95 % [8]. Switched capacitor (SC) circuits are particularly popular,

allowing for active balancing without bulky magnetic components. These circuits can be controlled using a fixed frequency and duty cycle, which regulates the charging and discharging currents, thus enabling the implementation of converters with low hardware complexity and costs [9]. Such approaches can extend the lifetime of a battery pack by up to 19.8 % [6], [10]. Various structures of switched capacitor circuits allow for charge transfer from a higher to any lower charged cell within a stack, with total capacitance provided by a single capacitor in single-switched capacitor topologies or distributed among several capacitors in more complex designs [11].

B. Control Design Considerations

Optimizing control design is crucial for increasing balancing efficiency. Literature indicates that control optimization can reduce balancing time and energy loss during the process by 9.59 % and 19.5 %, respectively [12]. As shown in Figure 1, balancing speed can be significantly enhanced by hardware capable of balancing arbitrary cells, though this requires more complex hardware configurations. Balancing only adjacent cells, C_n and C_{n+1} , creates imbalances with their neighbouring cells, C_{n-1} and C_{n+2} , necessitating a greater number of balancing iterations to equalize the battery stack. It is possible to further reduce the maximum offset of a single cell to the average stack voltage by charging or discharging arbitrary cells only until the first cell reaches a predefined target voltage, which can be the average stack voltage or a defined cut-off voltage during charging or discharging stages of the ESS. This work focuses on developing a control setup for balancing a cell stack using direct cell-to-cell (DC2C) balancing while charging or discharging each cell only to the target voltage. The employed balancing circuit utilizes a DC2C topology with a single switched capacitor, as demonstrated in Figure 1.

III. CONTROL ALGORITHM AND SIMULATION MODEL

The simulation model consists of three subsystems as illustrated in Figure 2 using *Simulink* and *Plecs Blockset*. The control algorithm is coded in *Matlab*.

A. Controller

The blue-marked controller block's algorithm, as depicted in Figure 2 is detailed in Figure 3. Triggered by the initialization state of the algorithm of the switch driver as shown in Figure 4, the controller starts by reading out the cell voltages and calculating the target cell voltage. Typically, this target voltage can be the average stack voltage in most cases or a predefined voltage, e.g. the cut-off voltage if the ESS is in charging or discharging phase. The cell with the highest positive deviation to the target voltage is designated as the emitter cell, the receiver cell is selected based on the highest negative offset to the target voltage. The algorithm concludes if the highest absolute offset is below a predefined threshold, meaning that all cell voltages are within a tolerated range. Else the switching frequency for the PWM generator is calculated concerning the

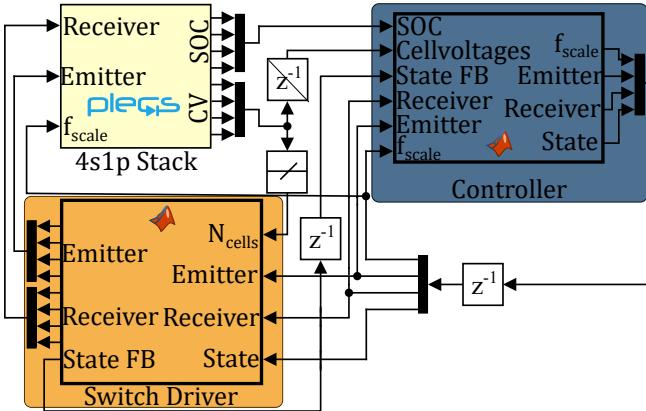


Fig. 2: Simulink Model showcasing cell identifier (blue), switch driver (orange) and 4s1p-battery stack implemented using *PLECS* Blockset.

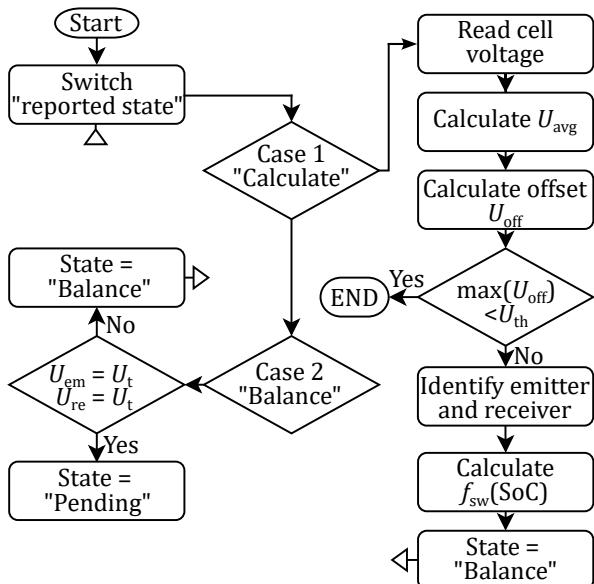


Fig. 3: Control algorithm of the blue-marked controller block implemented as *Matlab* function.

state of charge of the two cells as follows, whilst the duty cycle is always set to 50 %.

$$f_{sw} = \frac{1}{T_{charge} + T_{discharge}} \quad (3)$$

Where T_{charge} marks the required time to charge the switched capacitor C_{bal} that can be calculated by the generally valid time constant $\tau = R_{tot} \cdot C_{bal}$, assuming that $T_{charge} = 5 \cdot \tau$ and R_{tot} being the total series resistance of the circuit including $R_{ds,on}$ of the FETs and the conductor resistance.

$$T_{charge} = 5 \cdot R_{tot}(SoC_{emitter}) \cdot C_{bal} \quad (4)$$

The capacitor voltage $u(t)$ of a capacitor with the capacitance C_{bal} , an initial voltage U_0 and a circuit resistance of R_{tot}

during discharge is given by

$$u(t) = U_0 \cdot e^{\frac{-t}{R_{tot} \cdot C_{bal}}} \quad (5)$$

Hence, the time required to discharge the capacitor is obtained from Equation 6, where the initial voltage U_0 is determined by the voltage of the emitter cell and the voltage at the time t is given by the voltage of the receiver cell at the start of the discharge process.

$$T_{discharge} = R_{tot} \cdot C_{bal} \cdot \ln \left(\frac{U_{emitter, t0}}{U_{receiver, t0}} \right) \quad (6)$$

According to Equation 4 and Equation 6, the capacitance of the balancing capacitor can be freely chosen, however high capacitance will result in high charging currents as stated by Equation 7. With a capacitance of $C_{bal} = 1 \text{ mF}$, the switching frequency is $f_{sw} = 1.113 \text{ kHz}$. During simulations, the balancing capacitor C_{bal} is initially precharged to a voltage close to the average stack voltage to avoid high peak currents on initial charge.

$$i(t) = C \cdot \frac{\partial U(t)}{\partial t} \quad (7)$$

After identification, the flag to start balancing is sent to the switch driver. The switch driver confirms entering the balancing state by sending the flag back to the controller which then also switches to case 2 of the algorithm in Figure 3. The controller remains in the balancing state by further sending the balancing flag until either the emitter cell or the receiver cell reaches the target voltage. In that case, the flag "Pending" is sent to the switch driver, causing it to keep on balancing until the cell indices of the new emitter and receiver cells are received.

B. Switch Driver

The cell indices as well as the flag to enter the balancing state are received by the orange-marked switch driver in Figure 2 from the controller. The switch driver sets the output vectors of the emitter circuit and receiver circuit by setting the elements with the respective indices to 1 whilst setting the other vector elements to 0. The received state from the controller is then confirmed by sending the flag back to the controller. As seen in Figure 4, the initial state of the switch driver is "Startup", where all circuits are opened, meaning that all elements of the output vectors are 0. The identification of the emitter and receiver cells is then triggered by reporting the state "Calculate" to the controller.

C. Energy Storage Block

The energy storage block is implemented as a subsystem within Simulink using *PLECS* Blockset. It consists of 4 series-connected cells using accurate battery models proposed in [13]. As the used battery model offers the configuration of cell systems within the same model, each model is configured as a 1s1p-battery. The electric battery model consists of a capacitor $C_{Capacity}$, connected in parallel to a self-discharge resistor and a current-controlled current source. With respect

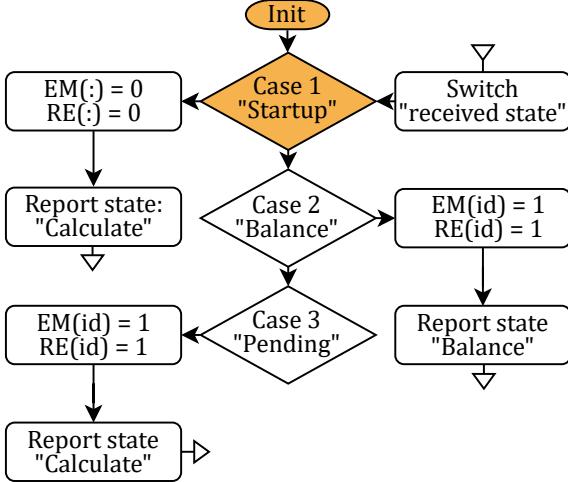


Fig. 4: Control algorithm of the orange-marked switch driver block implemented as *Matlab* function.

to the SoC of $C_{Capacity}$, an open-circuit voltage U_{OC} is generated. The transient voltage response is modeled by a series of one resistor R_{series} and two RC parallel networks $R_{Transient,S}, C_{Transient,S}$ and $R_{Transient,L}, C_{Transient,L}$. R_{series} describes the instantaneous voltage drop of the step response. $R_{Transient,S}, C_{Transient,S}$ and $R_{Transient,L}, C_{Transient,L}$ model the short-term and long-term constants respectively of the step response [13]. The cell-model provides real-time SOC and U_{OC} measurement. As demonstrated in Figure 5, the

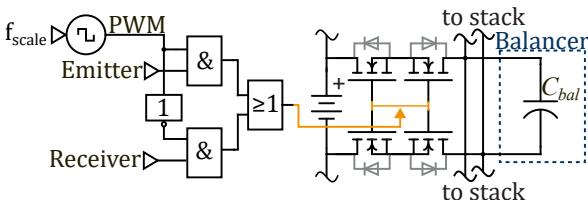


Fig. 5: Energy storage block including balancer capacitor hardware and control logic for one cell.

bidirectional switches are implemented using two mirrored N-channel field effect transistors (FET). Current may pass either through the N-channel if a positive voltage is applied at the gate and through the body diode of the reversed FET connected in series if a negative voltage is applied. The current direction and hence the actual current path inside the FET depends on the applied polarity on the bidirectional switch and thus on the current state of operation of the balancing circuit. The FETs conduct only if the signal from the switch driver and the PWM-signal are on logical *HIGH*. The PWM signal is inverted between the emitter and receiver circuit to avoid setting two circuits into conductive mode simultaneously. The balancer itself is implemented as a single switched capacitor as shown in Figure 1 (d).

IV. SIMULATION RESULTS

A. Voltage and Current Waveform

Figure 6 and Figure 7 show the waveform and principle of operation of the switched capacitor at a cell energy storage capacity of $E_{cell} = 50 \cdot E_{cap}$ in order to scale down simulation runtime. The PWM-signal enables the charging process of the capacitor at logic *HIGH*. The capacitor voltage U_{cap} starts rising and causes a voltage drop of the emitting cell C_2 as charge is transferred between the cell and the balancing capacitor. The balancing current i_{bal} rises at the start of the balancing cycle and follows Equation 7, changing direction when the PWM-signal switches to logic *LOW*, causing the voltage of the receiving cell C_3 to take the voltage of the capacitor until U_{cap} is equal to the steady-state voltage of the receiver cell.

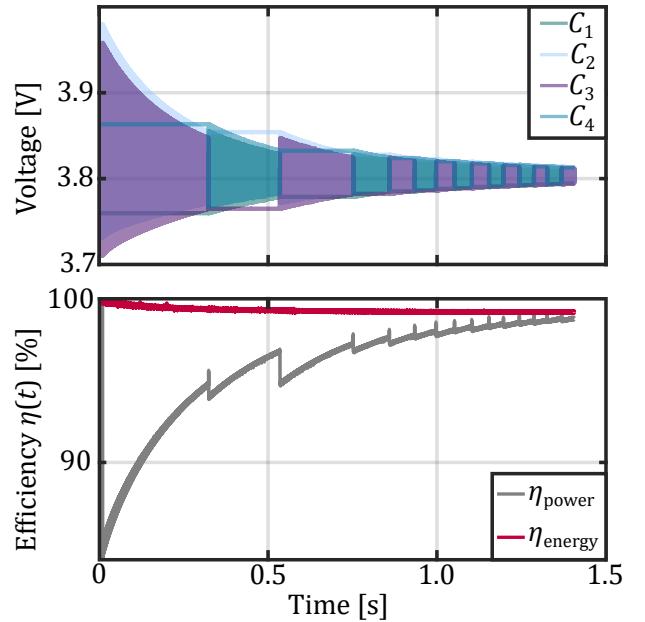


Fig. 6: Cell voltages and efficiency during balancing process.

B. Power Efficiency

The instant power efficiency η_{power} is generally defined by Equation 8 and can be calculated by assuming that the useful power to balance the cells is the absolute difference of the total power and the power loss.

$$\eta_{power} = \frac{P_{useful}}{P_{total}} = \frac{P_{total} - P_{loss}}{P_{total}} = 1 - \frac{P_{loss}}{P_{total}} \quad (8)$$

The power loss is defined as the product of the squared balancing current $i_{bal}(t)^2$ and the total conductor resistance R_{tot} of the circuit, meanwhile the total power is the product of the voltage $u_{cap}(t)$ of the switched capacitor and the balancing current so that Equation 8 can be written as:

$$\eta_{power}(t) = 1 - \left| \frac{R_{tot} \cdot i_{bal}(t)}{u_{cap}(t)} \right| \quad (9)$$

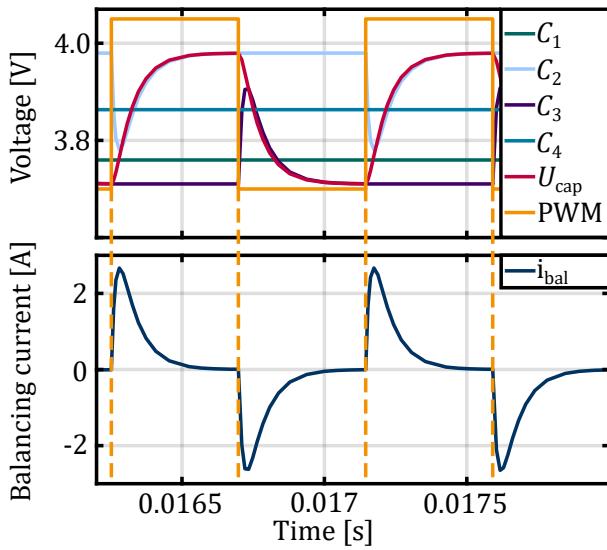


Fig. 7: Cell voltage waveform and balancing current at an optimal PWM-frequency and a duty cycle of 50 % where C_2 is emitting charge and C_3 is receiving charge. Cell voltages of C_1 and C_4 remain unchanged. (PWM-signal scaled and unitless)

An increase in efficiency is observed by the end of the balancing cycle. This is due to lower voltage offsets since the cells are already balanced to similar voltages at a further stage of the balancing cycle. The subsequent lower balancing currents result in a decreased power loss according to Equation 9. The average power efficiency of the balancing cycle can be calculated as average value of the instant efficiency shown in Figure 6 and results in $\eta_{pow,avg} = 98.78\%$.

C. Energy Efficiency

The instant energy efficiency η_{energy} as shown in Figure 6 is calculated by Equation 10 where $E_{instant}(t)$ is the instant energy stored inside the cells during the balancing process and $E_{initial}$ is the energy initially stored inside the battery stack. Both values are calculated as the product of the cell voltages CV and the cell capacity E_{cell} .

$$\eta_{energy}(t) = \frac{E_{output}(t)}{E_{initial}} = \frac{CV(t) \cdot E_{cell}}{CV_{initial} \cdot E_{cell}} \quad (10)$$

The overall energy efficiency is calculated by the energy initially stored inside the stack $E_{initial}$ and the energy E_{output} leftover inside the stack after the balancing process as follows:

$$\eta_{energy,overall} = \frac{E_{output}}{E_{initial}} \quad (11)$$

During simulations, an overall energy efficiency of $\eta_{energy,overall} = 99.36\%$ was achieved.

D. Frequency Effects

If all cells inside a stack have a similar SoC, the internal resistance of each cell is within a small range. In that case, computational complexity may be reduced by running the PWM with a fixed frequency with respect to the average SoC as the internal resistance of each cell and hence charging and discharging times are similar.

E. Hardware Complexity

The hardware complexity for implementation of the circuit in Figure 5 for one cell is given in Table I.

TABLE I: Hardware complexity of the circuit shown in Figure 5

Hardware element	Amount per stack
PWM generator	1
Field effect transistors	$4 \cdot N_{cells}$
AND-gate	$2 \cdot N_{cells}$
OR-gate	$1 \cdot N_{cells}$
NOT-gate	1

V. SUMMARY

An algorithm to control a switched capacitor balancing circuit was proposed. A proof of concept was made using simple *Matlab* scripts and a concept where cells are balanced to specified voltage was elaborated. The simulation was set up by three subsystems where the energy storage block was built as a *PLECS Blockset* model and the control was implemented using *Matlab* and *Simulink*. Simulations were done using a 4s1p-stack with a downscaled cell capacity to reduce simulation runtime. The balancing circuit was implemented using bidirectional switches and a single switched capacitor. This setup allows DC2C balancing whilst transferring charge between arbitrary cells within a battery stack. A hardware complexity analysis for the required logical circuit was done and the control algorithms implemented in *Matlab* were presented. Efficiency analysis show an average power efficiency of 98.78 % while the balancing efficiency increases if the cell voltages are within a smaller range. An overall energy efficiency of 99.36 % was reached.

VI. CONCLUSION

Simulations of the proposed balancing control algorithm showed an overall energy efficiency of 99.36 %, which is about 4 % higher than reported efficiencies in similar works. However the presented balancing strategy requires a higher hardware and computational complexity which are generally not offered by state-of-the-art balancer ICs. This suggests a primary use for small ESS where a high computational power is provided by a microcontroller and a higher hardware complexity is tolerated. Future work will include research on an optimal design of the balancing capacitor as well as a possible implementation as a resonant circuit with the use of an inductor as a current limiting device to allow efficient operation with lower balancing currents. Furthermore, a hardware setup will be used to validate simulations.

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Verpflichtungs- und Einverständniserklärung

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Innsbruck am
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