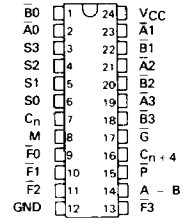
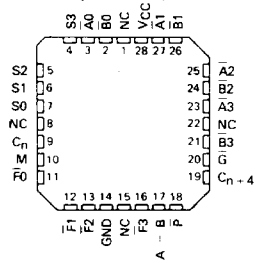
- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

SN54181, SN54LS181, SN54S181 . . . J OR W PACKAGE
SN74181 . . . J OR N PACKAGE
SN74LS181, SN74S181 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS181, SN54S181 . . . FK PACKAGE
SN74LS181, SN74S181 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES USING '181 AND '182	ADDITION TIMES USING 'LS181 AND '182	ADDITION TIMES USING 'S181 AND 'S182	PACKAGE COUNT ARITHMETIC/ LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	24 ns	24 ns	11 ns	1		NONE
5 to 8	36 ns	40 ns	18 ns	2		RIPPLE
9 to 16	36 ns	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	60 ns	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54182, SN54S182, SN74182, or SN74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading '182 or 'S182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

description (continued)

The '181, 'LS181, and 'S181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1, which requires an end-around or forced carry to provide A−B.

The '181, 'LS181, or 'S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74LS, and 74S devices are characterized for operation from 0°C to 70°C.

signal designations

The '181, 'LS181, and 'S181 together with the '182 and 'S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators (○) and the bars over the terminal letter symbols (e.g., $\overline{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at $\overline{C}$ means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

TEXAS INSTRUMENTS
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signal designations (continued)

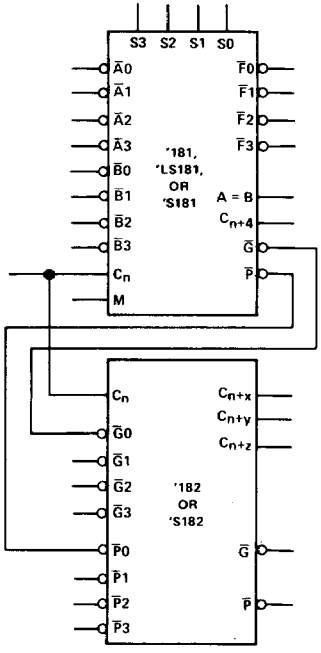

FIGURE 1

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

3

TTL DEVICES

signal designations (continued)

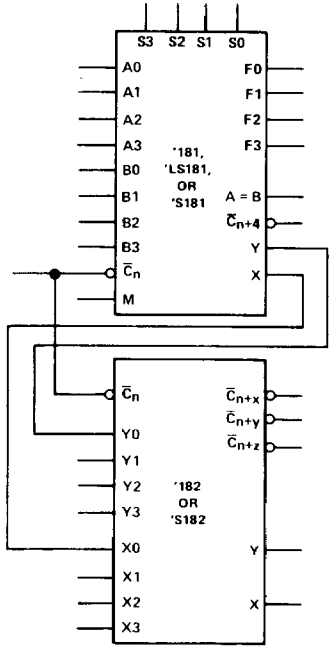

FIGURE 2

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

TEXAS INSTRUMENTS
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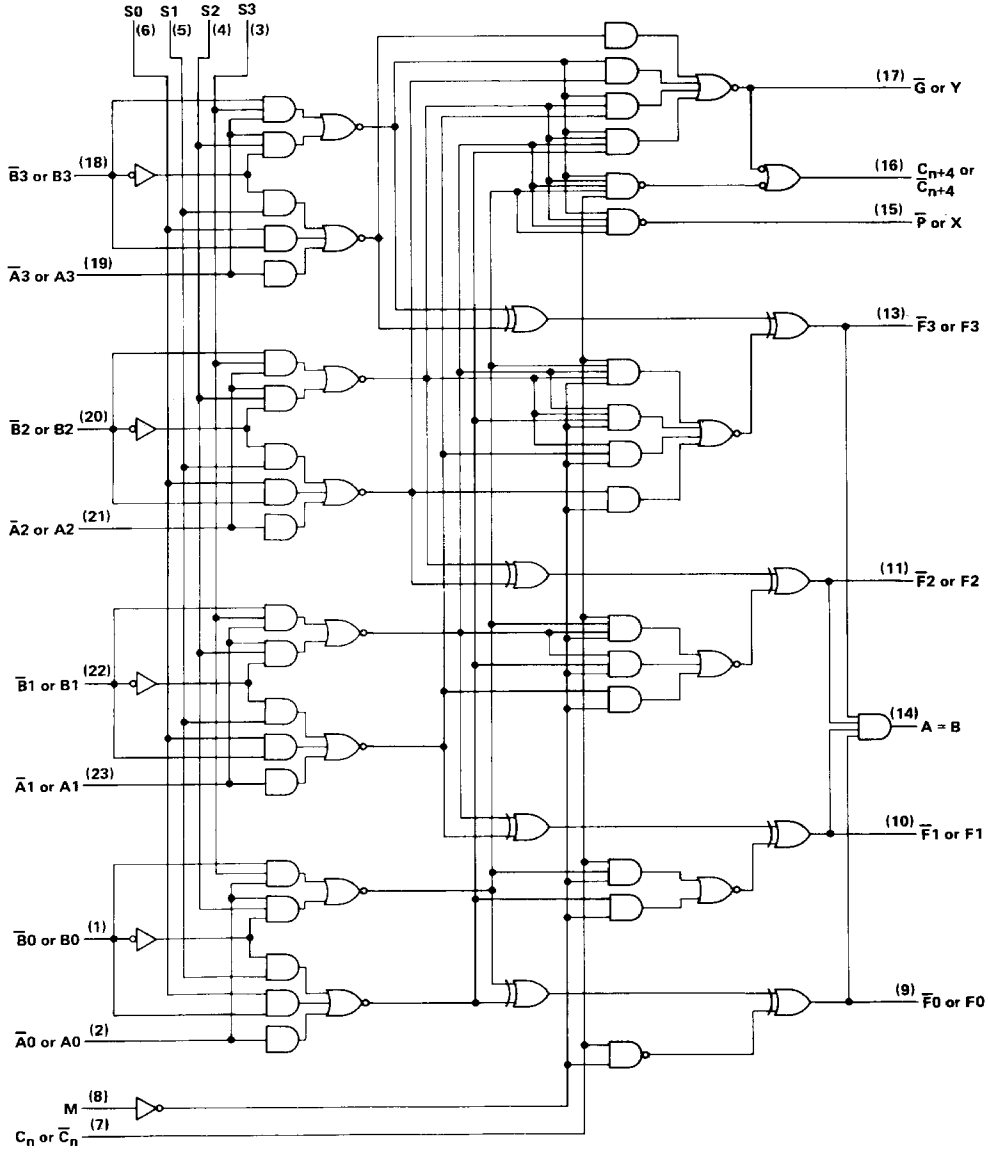
logic diagram



Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54181 . . . . . −55°C to 125°C
SN74181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54181			SN74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54181			SN74181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Any $\overline{A}$ or $\overline{B}$ input					120			120	
		Any S input					160			160	
		Carry input					200			200	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		Any $\overline{A}$ or $\overline{B}$ input					−4.8			−4.8	
		Any S input					−6.4			−6.4	
		Carry input					−8			−8	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−20		−55	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		88	127		88	140	mA
				Condition B		94	135		94	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

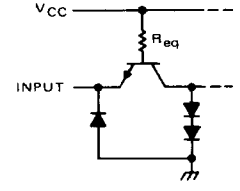
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 400 Ω, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			12	18	ns
t_{PHL}					13	19	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		28	43	ns
t_{PHL}					27	41	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		35	50	ns
t_{PHL}					33	50	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		13	19	ns
t_{PHL}					12	18	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}					13	19	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}					17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}					17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		28	42	ns
t_{PHL}					21	32	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (logic mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		35	50	ns
t_{PHL}					32	48	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: See General Information Section for load circuits and voltage waveforms.

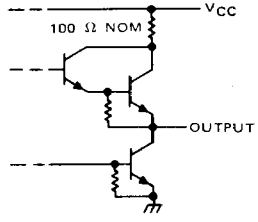
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

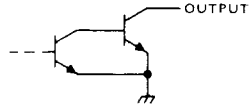


Mode control: R_{eq} = 4 kΩ NOM
Any $\overline{A}$ or $\overline{B}$: R_{eq} = 2 kΩ NOM
Any S: R_{eq} = 1.3 kΩ NOM
C_n: R_{eq} = 1 kΩ NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS181 . . . . . −55°C to 125°C
SN74LS181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54LS181			SN74LS181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS181			SN74LS181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	All outputs	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		Output $\overline{G}$		I_{OL} = 8 mA					0.35	0.5	
		Output $\overline{P}$		I_{OL} = 16 mA		0.47	0.7		0.47	0.7	
				I_{OL} = 8 mA		0.35	0.6		0.35	0.5	
I_I	Input current at max. input voltage	Mode input	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
		Any $\overline{A}$ or $\overline{B}$ input					0.3			0.3	
		Any S input					0.4			0.4	
		Carry input					0.5			0.5	
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
		Any $\overline{A}$ or $\overline{B}$ input					60			60	
		Any S input					80			80	
		Carry input					100			100	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		Any $\overline{A}$ or $\overline{B}$ input					−1.2			−1.2	
		Any S input					−1.6			−1.6	
		Carry input					−2			−2	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		20	32		20	34	mA
				Condition B		21	35		21	37	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

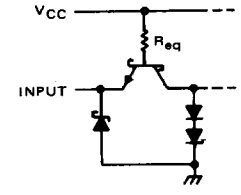
switching characteristics, V_{CC} = 5 V, T_A = 25°C, (C_L = 15 pF, R_L = 2 kΩ, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			18	27	ns
t_{PHL}					13	20	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		25	38	ns
t_{PHL}					25	38	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		27	41	ns
t_{PHL}					27	41	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		17	26	ns
t_{PHL}					13	20	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		19	29	ns
t_{PHL}					15	23	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		21	32	ns
t_{PHL}					21	32	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, ($\overline{SUM}$ mode)		20	30	ns
t_{PHL}					20	30	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		20	30	ns
t_{PHL}					22	33	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		21	32	ns
t_{PHL}					13	20	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		21	32	ns
t_{PHL}					21	32	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (logic mode)		22	33	ns
t_{PHL}					26	38	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		33	50	ns
t_{PHL}					41	62	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: See General Information Section for load circuits and voltage waveforms.

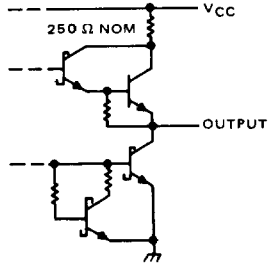
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

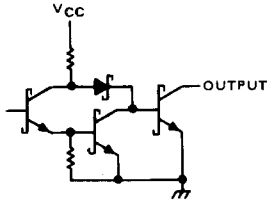


Mode control: R_{eq} = 17 kΩ NOM
Any $\overline{A}$ or $\overline{B}$: R_{eq} = 5.67 kΩ NOM
Any S: R_{eq} = 4.25 kΩ NOM
C_n: R_{eq} = 2.86 kΩ NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature: SN54S181 . . . . . −55°C to 125°C
SN74S181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54S181			SN74S181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54S181			SN74S181			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Mode input	V_{CC} = MAX,	V_I = 2.5 V				50			50	μA
		Any $\overline{A}$ or $\overline{B}$ input						150			150	
		Any S input						200			200	
		Carry input						250			250	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX,	V_I = 0.5 V				−2			−2	mA
		Any $\overline{A}$ or $\overline{B}$ input						−6			−6	
		Any S input						−8			−8	
		Carry input						−10			−10	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	T_A = 125°C,	W package only			195				mA
			V_{CC} = MAX,	See Note 3	All packages		120	220		120	220	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured for the following conditions (the typical and maximum values apply to both):
A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.
B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.

TEXAS INSTRUMENTS
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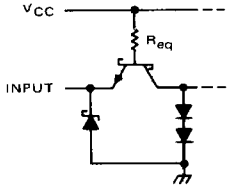
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 280 Ω, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			7	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		12.5	18.5	ns
t_{PHL}					12.5	18.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15.5	23	ns
t_{PHL}					15.5	23	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		7	12	ns
t_{PHL}					7	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		8	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		7.5	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		11	16.5	ns
t_{PHL}					11	16.5	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (logic mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15	23	ns
t_{PHL}					20	30	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: See General Information Section for load circuits and voltage waveforms.

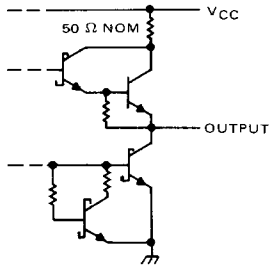
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

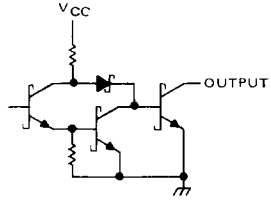


Mode control: R_{eq} = 2.8 kΩ NOM
Any $\overline{A}$ or $\overline{B}$: R_{eq} = 940 Ω NOM
Any S: R_{eq} = 700 Ω NOM
C_n: R_{eq} = 560 Ω NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

DIFF MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	A_i	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase

NOTE 4: See General Information Section for load circuits and voltage waveforms.

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