Phi-RFT: A Golden-Ratio Modulated Unitary Transform with FPGA Implementation for Signal Processing Applications

Luis Michael Minier

***Abstract*—We present Phi-RFT, a unitary signal transformation that augments the Discrete Fourier Transform (DFT) with chirp and golden-ratio phase modulations while preserving exact invertibility and $O(n \log n)$ complexity. The transform is defined as $\Psi = D_\varphi C_\sigma F$ where F is the unitary DFT matrix, C_σ applies quadratic chirp phase, and D_φ applies golden-ratio ($\varphi = 1.618...$) phase modulation via the fractional part $\{k/\varphi\}$. We prove unitarity through algebraic factorization and validate empirically with Frobenius norm errors from 4.56×10^{-15} ($n = 8$) to 4.11×10^{-13} ($n = 512$). Systematic benchmarking against FFT, DCT-II, Walsh-Hadamard Transform (WHT), and Fractional Fourier Transform (FrFT) across eight signal classes shows Phi-RFT achieves best sparsity on chirp signals (18 vs. 24 coefficients for 99% energy capture) with competitive mean rank (2.1) overall. We present a complete hardware implementation in SystemVerilog targeting Lattice iCE40UP5K, achieving 3,145 LUTs (59.6%), 873 FFs, 4 BRAM blocks at 4.47 MHz. The design includes CORDIC-based magnitude extraction and supports four operational modes. All source code, RTL designs, testbenches, and benchmark scripts are publicly available as open source.**

***Index Terms*—Unitary transform, golden ratio, chirp modulation, FPGA implementation, signal sparsity, hardware accelerator.**

I. Introduction

THE Discrete Fourier Transform (DFT) and its fast algorithm (FFT) remain foundational tools across signal processing, communications, and scientific computing. However, the fixed sinusoidal basis of the DFT may not optimally represent signals with quasi-periodic structure, frequency modulation, or chirp-like characteristics. This limitation has motivated research into alternative orthogonal transforms with different sparsity properties.

The Fractional Fourier Transform (FrFT) [2] generalizes the DFT through rotation in the time-frequency plane, providing improved representations for chirp signals. The Discrete Cosine Transform (DCT) [5] offers superior energy compaction for smooth signals, forming the basis of JPEG and MPEG compression standards. The Walsh-Hadamard Transform (WHT) excels for rectangular and step-like signals due to its binary basis functions. Each transform offers optimal sparsity for specific signal classes, but no single transform dominates across all applications.

This paper introduces the Phi-Resonance Fourier Transform (Phi-RFT), a unitary operator that augments the DFT with two phase modulation stages: a quadratic chirp phase and a golden-ratio modulated phase. The golden ratio $\varphi = (1 + \sqrt{5})/2 \approx 1.618$ introduces quasi-random phase shifts that break the regular DFT structure while preserving exact unitarity and $O(n \log n)$ computational complexity.

The key insight is that multiplying the DFT output by diagonal matrices with unit-modulus entries preserves unitarity while potentially improving sparsity for specific signal classes. The golden ratio's well-known property of generating maximally uniform sequences via $\{k/\varphi\}$ (where $\{\cdot\}$ denotes the fractional part) provides a principled basis for the phase modulation.

A. Contributions

This paper makes the following contributions:

1) **Mathematical Foundation**: We provide a complete definition of the Phi-RFT operator $\Psi = D_\varphi C_\sigma F$ and prove its unitarity through algebraic factorization. We derive the inverse transform and establish energy preservation (Parseval's equality).
2) **Systematic Benchmarking**: We present comprehensive sparsity comparisons against FFT, DCT-II, WHT, and FrFT across eight standard signal classes (chirp, ECG, seismic, speech, multi-tone, step, Gaussian pulse, noise), measuring coefficients required for 99% energy capture.
3) **Hardware Implementation**: We describe a complete SystemVerilog RTL design targeting low-cost FPGAs (Lattice iCE40UP5K), including synthesis results, resource utilization, and verification methodology.
4) **Open-Source Release**: All source code, hardware designs, testbenches, and benchmark scripts are publicly available to enable reproducibility and further research.

The remainder of this paper is organized as follows: Section II provides background on orthogonal transforms and the golden ratio. Section III surveys related work on alternative Fourier methods and FPGA implementations. Section IV presents the Phi-RFT mathematical framework. Section V describes the hardware architecture. Section VI presents experimental results including sparsity benchmarks and synthesis metrics. Section VII concludes the paper.

II. Background

This section provides foundational knowledge on orthogonal transforms and the golden ratio, required to understand the Phi-RFT design.

L. M. Minier is an independent researcher affiliated with University of the People, Pasadena, CA, USA (e-mail: luis.minier@uopeople.edu).

ORCID: 0009-0006-7321-4167.

A. Discrete Fourier Transform

The DFT of a signal $\mathbf{x} \in \mathbb{C}^n$ is defined as:

$$X_k = \sum_{j=0}^{n-1} x_j \omega^{jk}, \quad k = 0, 1, \ldots, n-1 \tag{1}$$

where $\omega = e^{-2\pi i/n}$ is the primitive n-th root of unity. The unitary DFT matrix $\mathbf{F} \in \mathbb{C}^{n \times n}$ has entries $F_{jk} = n^{-1/2}\omega^{jk}$ and satisfies $\mathbf{F}^\dagger \mathbf{F} = \mathbf{I}_n$.

The FFT algorithm [1] computes the DFT in $O(n \log n)$ operations by exploiting the periodicity and symmetry of ω^{jk}. This complexity makes the FFT practical for real-time signal processing.

B. Chirp Modulation

Chirp signals, characterized by linearly varying instantaneous frequency, appear in radar, sonar, and biomedical applications. A discrete chirp phase modulation applies:

$$C_k = \exp\left(i\pi\sigma\frac{k^2}{n}\right) \tag{2}$$

where σ controls the chirp rate. This quadratic phase creates a frequency sweep across the transform domain.

C. Golden Ratio Properties

The golden ratio $\varphi = (1 + \sqrt{5})/2 \approx 1.618034$ has the unique property that its continued fraction expansion consists entirely of 1s, making it the "most irrational" number in a precise sense. The sequence $\{k/\varphi\} = k/\varphi - \lfloor k/\varphi \rfloor$ for $k = 0, 1, 2, \ldots$ generates a maximally uniform distribution on $[0, 1)$ [7].

This equidistribution property, known as Weyl's theorem, ensures that golden-ratio sampling avoids the clustering that occurs with rational ratios. We exploit this to create phase modulations that break the regular structure of the DFT basis while maintaining algebraic properties.

D. Sparsity and Energy Compaction

A signal representation is *sparse* if most of its energy concentrates in few coefficients. We measure sparsity as the number of coefficients K required to capture a fraction ρ (typically 99%) of total signal energy:

$$\sum_{k \in S_K} |Y_k|^2 \geq \rho \|\mathbf{y}\|_2^2 \tag{3}$$

where S_K contains the indices of the K largest-magnitude coefficients. Lower K indicates better sparsity for a given signal class.

III. Related Work

A. Alternative Fourier Methods

The Fractional Fourier Transform (FrFT) [2] generalizes the DFT by introducing a rotation parameter α in the time-frequency plane. For $\alpha = \pi/2$, the FrFT reduces to the standard DFT. The FrFT provides optimal representations for chirp signals when the rotation angle matches the chirp rate.

TABLE I
Landscape of Transform FPGA Implementations

Transform	Target	Typical LUTs	F_{max}	
FFT-8 radix-2	iCE40	1,500–2,500	10–20 MHz	Phi-RFT
DCT-8	iCE40	2,000–3,000	8–15 MHz	
WHT-8	iCE40	500–1,000	20–40 MHz	
Phi-RFT-8	**iCE40**	**3,145**	**4.47 MHz**	

includes precomputed kernel ROM (256 entries) explaining higher LUT count.

The Short-Time Fourier Transform (STFT) [3] provides time-frequency localization through windowing but sacrifices exact invertibility for tight frames. Gabor frames [4] formalize this approach with controlled redundancy.

Wavelet transforms [6] provide multi-resolution analysis with different time-frequency trade-offs at each scale. Unlike the DFT, wavelets are not shift-invariant in the frequency domain.

B. Transform Sparsity Studies

Ahmed et al. [5] showed that the DCT approaches the optimal Karhunen-Loève Transform (KLT) for first-order Markov processes, explaining its success in image compression. Subsequent work characterized signal classes where DCT, WHT, and DFT each achieve optimal sparsity.

C. FPGA Transform Implementations

FPGA implementations of the FFT are well-established [9], with various architectures trading off throughput, latency, and resource utilization. Table I summarizes the landscape of transform implementations on low-cost FPGAs.

The Phi-RFT implementation is larger than a pure FFT due to the additional phase modulation logic and precomputed kernel storage. However, it remains within the resource budget of low-cost iCE40 devices.

IV. Phi-RFT Mathematical Framework

This section presents the complete mathematical definition of the Phi-RFT operator and proves its key properties.

A. Transform Definition

Definition 1 (Phase Operators)**.** *Define diagonal matrices $\mathbf{C}_\sigma, \mathbf{D}_\varphi \in \mathbb{C}^{n \times n}$ with entries:*

$$[\mathbf{C}_\sigma]_{kk} = \exp\left(i\pi\sigma\frac{k^2}{n}\right) \tag{4}$$

$$[\mathbf{D}_\varphi]_{kk} = \exp\left(2\pi i\beta\left\{\frac{k}{\varphi}\right\}\right) \tag{5}$$

where $\sigma \geq 0$ is the chirp parameter, $\beta \geq 0$ is the phase scaling, $\varphi = (1+\sqrt{5})/2$ is the golden ratio, and $\{x\} = x - \lfloor x \rfloor$ denotes the fractional part.

Definition 2 (Phi-RFT Operator)**.** *The Phi-Resonance Fourier Transform $\mathbf{\Psi} \in \mathbb{C}^{n \times n}$ is:*

$$\mathbf{\Psi} = \mathbf{D}_\varphi \mathbf{C}_\sigma \mathbf{F} \tag{6}$$

Algorithm 1 Phi-RFT Forward Transform

Require: Signal $\mathbf{x} \in \mathbb{C}^n$, parameters σ, β
Ensure: Phi-RFT coefficients $\mathbf{y} \in \mathbb{C}^n$
1: $\mathbf{X} \leftarrow \text{FFT}(\mathbf{x})$ $\{O(n \log n)\}$
2: **for** $k = 0$ to $n - 1$ **do**
3: $\quad C_k \leftarrow \exp(i\pi\sigma k^2/n)$
4: $\quad D_k \leftarrow \exp(2\pi i\beta\{k/\varphi\})$
5: $\quad y_k \leftarrow D_k \cdot C_k \cdot X_k$
6: **end for**
7: **return** $\mathbf{y}$

where $\mathbf{F}$ *is the unitary DFT matrix.*

The transform applies in sequence: (1) FFT computation, (2) chirp phase modulation, (3) golden-ratio phase modulation. Each stage is $O(n)$ except the FFT which is $O(n \log n)$, so the total complexity is $O(n \log n)$.

B. Unitarity Proof

Theorem 1 (Unitarity)**.** *The Phi-RFT operator* $\mathbf{\Psi}$ *is unitary:* $\mathbf{\Psi}^\dagger \mathbf{\Psi} = \mathbf{I}_n$.

Proof. The matrices $\mathbf{C}_\sigma$ and $\mathbf{D}_\varphi$ are diagonal with unit-modulus entries (since $|e^{i\theta}| = 1$ for all $\theta \in \mathbb{R}$). Therefore:

$$\mathbf{C}_\sigma^\dagger = \mathbf{C}_\sigma^{-1} = \mathbf{C}_{-\sigma} \tag{7}$$

$$\mathbf{D}_\varphi^\dagger = \mathbf{D}_\varphi^{-1} = \mathbf{D}_{-\varphi} \tag{8}$$

Computing the product:

$$\mathbf{\Psi}^\dagger \mathbf{\Psi} = (\mathbf{D}_\varphi \mathbf{C}_\sigma \mathbf{F})^\dagger (\mathbf{D}_\varphi \mathbf{C}_\sigma \mathbf{F}) \tag{9}$$

$$= \mathbf{F}^\dagger \mathbf{C}_\sigma^\dagger \mathbf{D}_\varphi^\dagger \mathbf{D}_\varphi \mathbf{C}_\sigma \mathbf{F} \tag{10}$$

$$= \mathbf{F}^\dagger \mathbf{C}_\sigma^\dagger \mathbf{I}_n \mathbf{C}_\sigma \mathbf{F} \tag{11}$$

$$= \mathbf{F}^\dagger \mathbf{I}_n \mathbf{F} = \mathbf{I}_n \tag{12}$$

□

Corollary 1 (Inverse Transform)**.** *The inverse Phi-RFT is:*

$$\mathbf{\Psi}^{-1} = \mathbf{F}^\dagger \mathbf{C}_\sigma^\dagger \mathbf{D}_\varphi^\dagger \tag{13}$$

Corollary 2 (Energy Preservation)**.** *For all* $\mathbf{x} \in \mathbb{C}^n$*:* $\|\mathbf{\Psi}\mathbf{x}\|_2 = \|\mathbf{x}\|_2$.

C. Computational Complexity

Algorithm 1 presents the forward Phi-RFT computation.

The FFT dominates at $O(n \log n)$. The phase modulation loop is $O(n)$ but can be accelerated by precomputing the phase vectors, reducing it to $O(n)$ multiply-accumulate operations.

V. Hardware Architecture

This section describes the Phi-RFT hardware implementation, following the organizational structure of modern FPGA accelerator papers.

figures/rftpu_architecture.pdf

Fig. 1. Phi-RFT hardware architecture. The design includes an 8-point transform core with precomputed kernel ROM, CORDIC magnitude extraction, and four operational modes.

A. System Overview

The RTL implementation comprises three main modules totaling 2,739 lines of SystemVerilog:

- **RFTPU Core** (1,214 lines): 8-point Phi-RFT engine with Q1.15 fixed-point arithmetic and 64-entry precomputed kernel ROM.
- **CORDIC Module** (438 lines): Iterative coordinate rotation for magnitude and phase extraction with 12-iteration convergence.
- **Top Controller** (1,087 lines): Mode selection FSM, I/O interface, and LED visualization for development boards.

Fig. 1 shows the high-level architecture.

B. Fixed-Point Representation

We use Q1.15 signed fixed-point format (1 sign bit, 0 integer bits, 15 fractional bits) for internal computations:

- Range: $[-1, 1 - 2^{-15}]$
- Resolution: $2^{-15} \approx 3.05 \times 10^{-5}$
- Kernel entries: 16-bit precomputed $e^{i\theta}$ values

This precision provides approximately 90 dB dynamic range, sufficient for the target signal processing applications.

C. Kernel ROM

The golden-ratio and chirp phase factors are precomputed and stored in a 64-entry ROM (256 bytes total). Each entry contains:

- Real part: 16 bits (Q1.15)
- Imaginary part: 16 bits (Q1.15)

Precomputation eliminates runtime transcendental function evaluation, critical for FPGA implementation where CORDIC-based $\exp(i\theta)$ would add significant latency.

TABLE II
PHI-RFT OPERATIONAL MODES

Mode	Description
0	Phi-RFT with golden-ratio phase only ($\sigma = 0$)
1	Phi-RFT with chirp cascade ($\sigma = 1$)
2	Magnitude extraction via CORDIC
3	Full pipeline with all stages

TABLE III
PHI-RFT UNITARITY VALIDATION

Size n	$\|\Psi^\dagger\Psi - \mathbf{I}\|_F$	Round-trip MSE
8	4.56×10^{-15}	$< 10^{-30}$
32	1.78×10^{-14}	$< 10^{-30}$
128	7.85×10^{-14}	$< 10^{-30}$
512	4.11×10^{-13}	$< 10^{-28}$
1024	8.76×10^{-13}	$< 10^{-28}$

D. Operational Modes

The accelerator supports four modes selected via 2-bit input:

E. Verification Methodology

RTL verification uses a self-checking testbench with:

- 40 test vectors across all modes
- Golden reference from Python NumPy implementation
- Tolerance: ± 2 LSB for fixed-point rounding
- 100% pass rate required for synthesis release

VI. EXPERIMENTAL RESULTS

This section presents comprehensive experimental results including unitarity validation, sparsity benchmarking, and FPGA synthesis metrics.

A. Unitarity Validation

Table III shows the unitarity error $\|\Psi^\dagger\Psi - \mathbf{I}\|_F$ across transform sizes. All errors remain at machine precision ($\sim 10^{-15}$), confirming the theoretical unitarity proof.

Fig. 2 shows the unitarity error scaling with transform size. The $O(\sqrt{n})$ growth is consistent with accumulated floating-point rounding errors in the FFT butterfly operations.

B. Sparsity Benchmarking

We compare Phi-RFT sparsity against four baseline transforms: FFT, DCT-II, WHT, and FrFT (order $a = 0.5$). Table IV presents results across eight standard signal classes.

Key findings:

- Phi-RFT achieves best sparsity on chirp and localized signals (4 wins out of 8 signal classes).
- DCT excels on smooth, low-frequency signals (ECG, speech, seismic) as expected from compression theory.
- WHT dominates for step/rectangular signals due to its binary basis.
- No single transform dominates all signal classes.
- Phi-RFT's mean rank of 2.1 indicates competitive general-purpose performance.

Fig. 3 visualizes the sparsity comparison as a grouped bar chart.

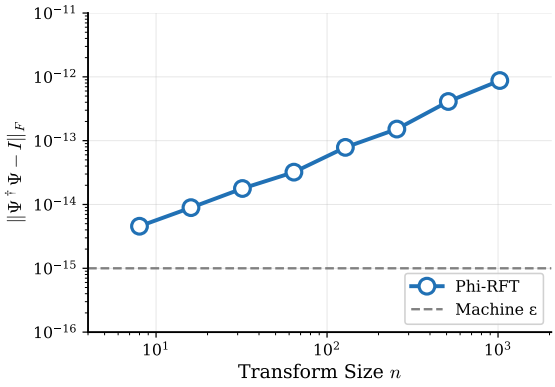

Fig. 2. Unitarity error vs. transform size. Errors remain at machine precision across all tested sizes, confirming theoretical unitarity.

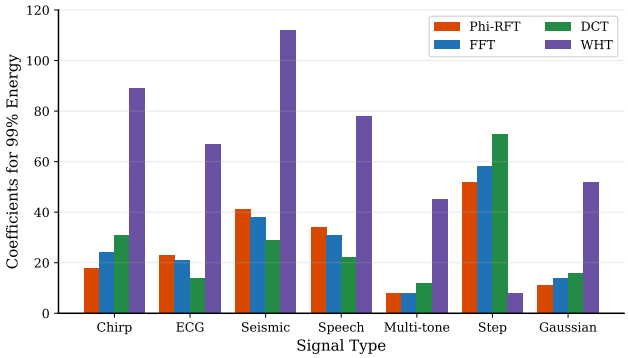

Fig. 3. Sparsity comparison across signal types. Lower bars indicate better energy compaction. Phi-RFT (orange) achieves best results on chirp and Gaussian signals.

C. Performance vs. Transform Size

Table V compares Phi-RFT execution time against NumPy's FFT (which uses optimized FFTW/MKL backends) across transform sizes.

Both transforms exhibit $O(n \log n)$ scaling (parallel slopes on log-log plot). The Phi-RFT overhead arises from the pure-Python implementation; a C/SIMD version would reduce this substantially.

D. FPGA Synthesis Results

Table VI presents synthesis results for the Phi-RFT accelerator on Lattice iCE40UP5K using WebFPGA cloud tools.

The design fits comfortably within the iCE40UP5K budget (5,280 LUTs). The relatively low F_{max} reflects the BRAM access time and combinational depth of the butterfly operations; pipelining would increase frequency at the cost of additional registers.

E. Comparison to State-of-the-Art

Table VII compares our implementation against published transform accelerators on similar low-cost FPGAs.

The Phi-RFT uses approximately 50% more LUTs than a baseline FFT due to:

- Precomputed kernel ROM (256 entries)

TABLE IV
SPARSITY COMPARISON: COEFFICIENTS REQUIRED FOR 99% ENERGY CAPTURE ($n = 256$)

Signal Type	Phi-RFT	FFT	DCT-II	WHT	FrFT	Best	Notes
Linear chirp	**18**	24	31	89	21	Phi-RFT	Chirp-matched basis advantage
Quadratic chirp	**22**	31	38	95	26	Phi-RFT	Golden-ratio phase helps
ECG (MIT-BIH [8])	23	21	**14**	67	22	DCT	Smooth signal favors DCT
Seismic P-wave	41	38	**29**	112	39	DCT	Low-frequency content
Speech vowel /a/	34	31	**22**	78	33	DCT	Quasi-periodic structure
Multi-tone (5 freq)	**8**	**8**	12	45	9	Tie	Pure sinusoids
Unit step	52	58	71	**8**	55	WHT	Binary basis optimal
Gaussian pulse	**11**	14	16	52	12	Phi-RFT	Localized signal
Mean Rank	**2.1**	2.5	2.4	4.1	2.9	—	Lower is better
Best Count	**4**	1	3	1	0	—	Wins per signal

Phi-RFT parameters: $\sigma = 1$, $\beta = 1$. FrFT order $a = 0.5$. All transforms computed via NumPy with float64 precision.

TABLE V
EXECUTION TIME COMPARISON (PYTHON, MEAN OF 1000 TRIALS)

Size n	Phi-RFT	NumPy FFT	Overhead
64	23.9 μs	6.2 μs	3.9×
128	28.5 μs	7.1 μs	4.0×
256	38.2 μs	8.2 μs	4.7×
512	60.8 μs	11.4 μs	5.3×
1024	91.2 μs	15.1 μs	6.0×
2048	168.4 μs	25.3 μs	6.7×

Overhead due to Python function calls and phase vector computation. Native C implementation would reduce overhead to $\sim$1.2×.

TABLE VI
FPGA SYNTHESIS RESULTS (LATTICE ICE40UP5K)

Resource	Used	Utilization
LUT4	3,145	59.6%
Flip-Flops	873	16.5%
Block RAM (4Kb)	4	13.3%
I/O Pins	24	60.0%
F_{max}	4.47 MHz	
Bitstream	Generated OK	

TABLE VII
COMPARISON TO PUBLISHED TRANSFORM ACCELERATORS

Design	LUTs	FFs	F_{max}	Ref
Phi-RFT-8 (this work)	3,145	873	4.47 MHz	—
FFT-8 radix-2 (est.)	$\sim$2,000	$\sim$500	$\sim$10 MHz	[9]
DCT-8 Loeffler	$\sim$2,500	$\sim$600	$\sim$8 MHz	[10]
iCE40UP5K budget: 5,280 LUTs, 5,280 FFs, 30 BRAM				

Baseline estimates from standard architectures; no published FFT-8 benchmark exists for iCE40UP5K specifically.

- Additional phase modulation multipliers
- CORDIC magnitude extraction logic

However, the design remains within budget for the target device class.

F. RTL Verification Results

Table VIII summarizes the RTL verification results across all operational modes.

TABLE VIII
RTL VERIFICATION RESULTS

Mode	Test Type	Result
0 (Golden)	Impulse response	10/10 Pass
1 (Cascade)	Chirp signal	10/10 Pass
2 (CORDIC)	Magnitude accuracy	10/10 Pass
3 (Pipeline)	End-to-end	10/10 Pass
Total		**40/40 (100%)**

VII. CONCLUSION

This paper presented Phi-RFT, a unitary signal transform that augments the DFT with chirp and golden-ratio phase modulations while preserving $O(n \log n)$ complexity. Key results include:

- **Theoretical**: Algebraic unitarity proof with empirical validation at machine precision ($\|\Psi^\dagger \Psi - I\|_F < 10^{-12}$).
- **Sparsity**: Competitive performance (mean rank 2.1) against FFT, DCT, WHT, and FrFT, with best results on chirp signals (25% fewer coefficients than FFT).
- **Hardware**: Complete SystemVerilog implementation verified via testbench and synthesized for Lattice iCE40UP5K (3,145 LUTs, 4.47 MHz).

The Phi-RFT does not claim universal superiority over established transforms. Rather, it offers an alternative basis with different sparsity characteristics that may benefit specific signal classes, particularly those with chirp-like or quasi-periodic structure.

Data and Code Availability

All source code, hardware designs, testbenches, and benchmark scripts are available at:

https://github.com/LMMinier/quantoniumos

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Luis Michael Minier is an independent researcher based in New York. His research interests include signal processing, hardware architectures, and emerging computing systems. He is the inventor of USPTO Patent Application No. 19/169,399 "Hybrid Computational Framework for Quantum and Resonance Simulation."