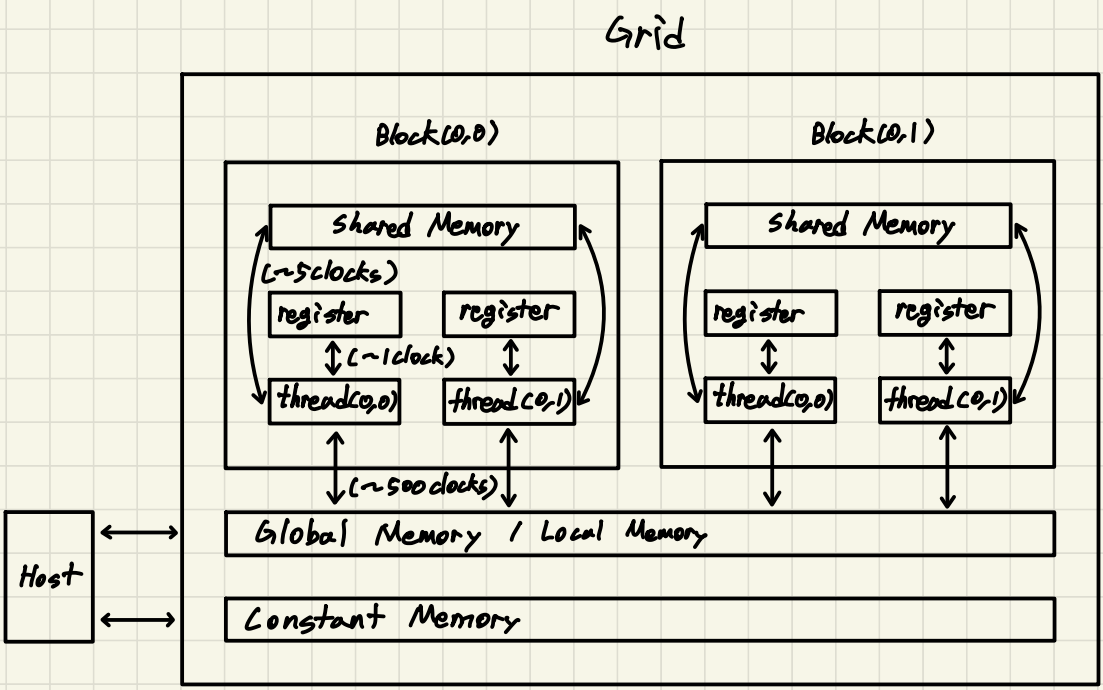
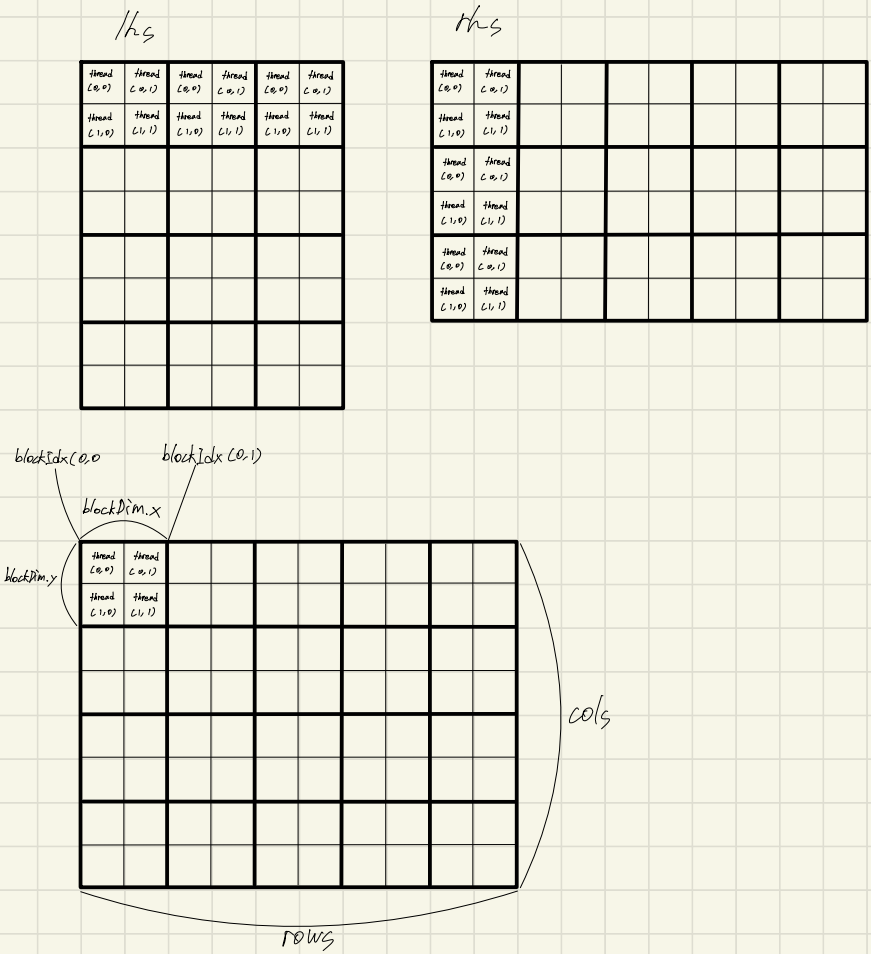
CUDA memory hierarchy



1. max 1024 threads per 1 block
2. 1 block per SM
3. (32 threads = 1 warp) per SM

TILED MATRIX DOT PRODUCT Basic

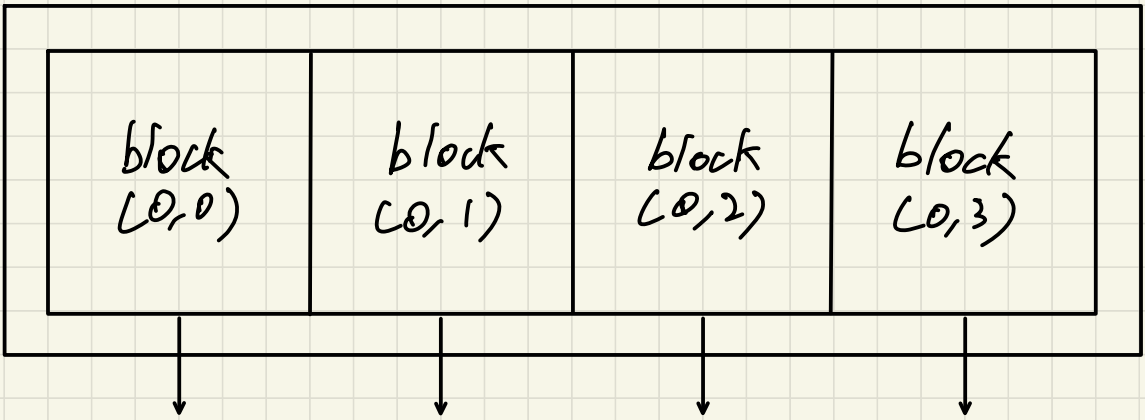


pseudo code

```
int x = blockIdx.x * blockDim.x + threadIdx.x;
int y = blockIdx.y * blockDim.y + threadIdx.y;
double sum = 0.0;
for(int i=0;  i < lhs_cols; ++i)
{
    sum += lhs[y * lhs_cols + i] * rhs[i * rhs_cols + x];
}
result[y * rows + x] = sum;
```

Result matrix dimension 256 x 1
TILED MATRIX DOT PRODUCT

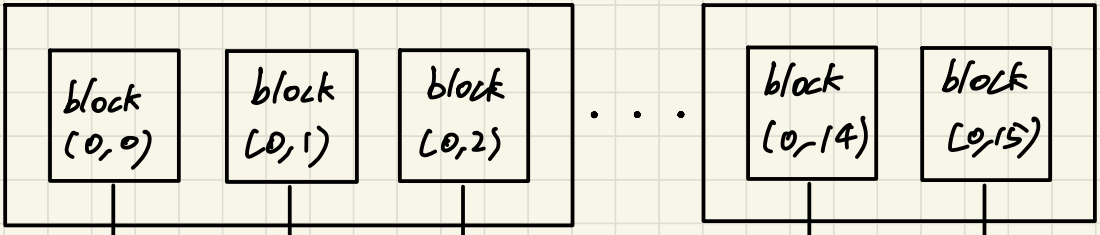
TILED WIDTH = 32



32 warps (=1024 threads) 32 warps 32 warps 32 warps

= total 128 warps

TILED WIDTH = 8



2 warps (=64 threads) 2 warps 2 warps . . . 2 warps 2 warps

= total 64 warps